Bangabandhu Sheikh Mujibur Rahman Science and Technology University

Department of Computer Science and Engineering

2nd Year 1st Semester Final B.Sc. Engineering Examination-2021

Course Code: CSE203 **Course Title: Digital Logic Design**

Total Marks: 60 **Time: 3 (Three) Hours**

N.B.:

i. Answer **SIX** questions taking any **THREE** from each section.

ii. All parts of a question must be answered sequentially.

Section-A

1. a) What is Karnaugh map? Give an example of two and three variables map. **2**

b) Simplify the Boolean function: $F = x'yz + x'yz' + xy'z' + xy'z$. **3**

c) Simplify the following Boolean function in (a) sum of products and (b) product of sums. $F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$ with proper gate implementation. **5**

2. a) What is Universal gate? Implement NOT, AND and OR gates by NAND gate. **3**

b) What is propagation delay? Explain propagation delay with figure. **3**

c) Simplify the Boolean function: $F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$ and the don't care conditions: $d(w, x, y, z) = \sum(0, 2, 5)$. **4**

3. a) Explain design procedure for combinational circuit and difference between combinational circuit and sequential circuit. **5**

b) What is code conversion? Design a BCD-to-access-3 code converter. **5**

4. a) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. **5**

b) A combinational circuit is defined by the functions $F_1(A, B, C) = \sum(3, 5, 6, 7)$ and $F_2(A, B, C) = \sum(0, 2, 4, 7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs. **5**

Section-B

5. a) Design a *D* flip-flop from clocked S-R flip-flop. Write the uses of *D* flip-flop. **4**

b) Using 10's complement, subtract 73542 – 3421. **4**

c) What is a clock in a digital system? Give example. **2**

6. a) Explain sequential circuit with corresponding block diagram. **3**

b) Simplify the following Boolean function by first finding the essential prime implicants: $F(A, B, C, D) = \sum(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$. **7**

7. a) Implement a full adder circuit with a decoder and two OR gates where the combinational circuit in sum of minterms are: $S(x, y, z) = \sum(1, 2, 5, 7)$ and $C(x, y, z) = \sum(3, 4, 6, 7)$. **5**

b) Implement the following function with a multiplexer: **5**

$$F(A, B, C, D) = \sum(0, 2, 5, 7, 8, 9, 14)$$

8. a) What is Decoder? Explain a 3-to-8 line decoder. **4**

b) Design a logic circuit of 4-bit magnitude comparator. **4**

c) Draw the odd-parity generation table and its figure. **2**