

The timing diagram illustrates the operation of a 4-bit ripple-carry adder. The signals are as follows:

- Signal 1 (Blue):** A constant high signal, labeled '1'.
- Signal 2 (Orange):** A sequence of 4-bit numbers. It begins with a glitch (10011001), followed by 1987, 6542, 8, 4, 0, -4, -8, and -10.
- Signal 3 (Green):** A step function that transitions from low to high at approximately 5 ns and back to low at approximately 58 ns.
- Signal 4 (Red):** A signal with three narrow pulses occurring at approximately 11 ns, 48 ns, and 86 ns.
- Signal 5 (Dashed Black):** A constant reference signal at a low level.
- Signal 6 (Purple):** A signal with two narrow pulses occurring at approximately 47 ns and 84 ns.
- Signal 7 (Brown):** A sequence of 4-bit numbers, showing 15 and 1.

Timestamp (125MHz FPGA clock ticks)