

The timing diagram illustrates the operation of a 4-bit ripple-carry adder. The signals are as follows:

- Blue Signal (1):** A constant high signal, likely representing a clock or enable.
- Orange Signal (19 6542):** The input values being added. It shows a sequence of values: 19, 65, 42, 8, 4, 0, -4, -8, and -10.
- Green Signal:** The carry-in signal, which is high from time 5 to 58 and low otherwise.
- Red Signal:** The carry-out signal, which is high at time 10, 48, and 85, and low otherwise.
- Purple Signal:** The sum signal, which is high at time 47 and 83, and low otherwise.

The x-axis represents time from 0 to 90. The y-axis represents the signal level, with a dashed line indicating a reference level.

Timestamp (125MHz FPGA clock ticks)