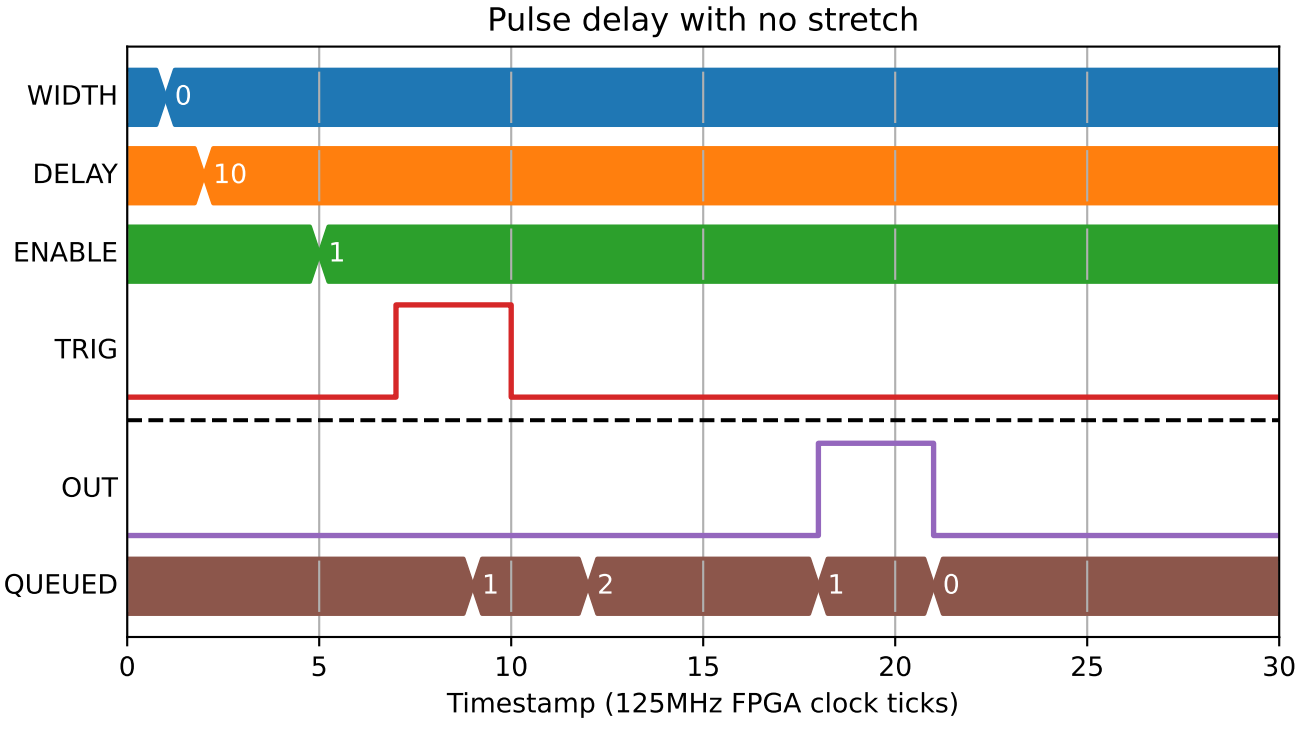
Pulse delay with no stretch
WIDTH
DELAY
ENABLE
TRIG
OUT
QUEUED
0
10
1
1
2
1
0
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)