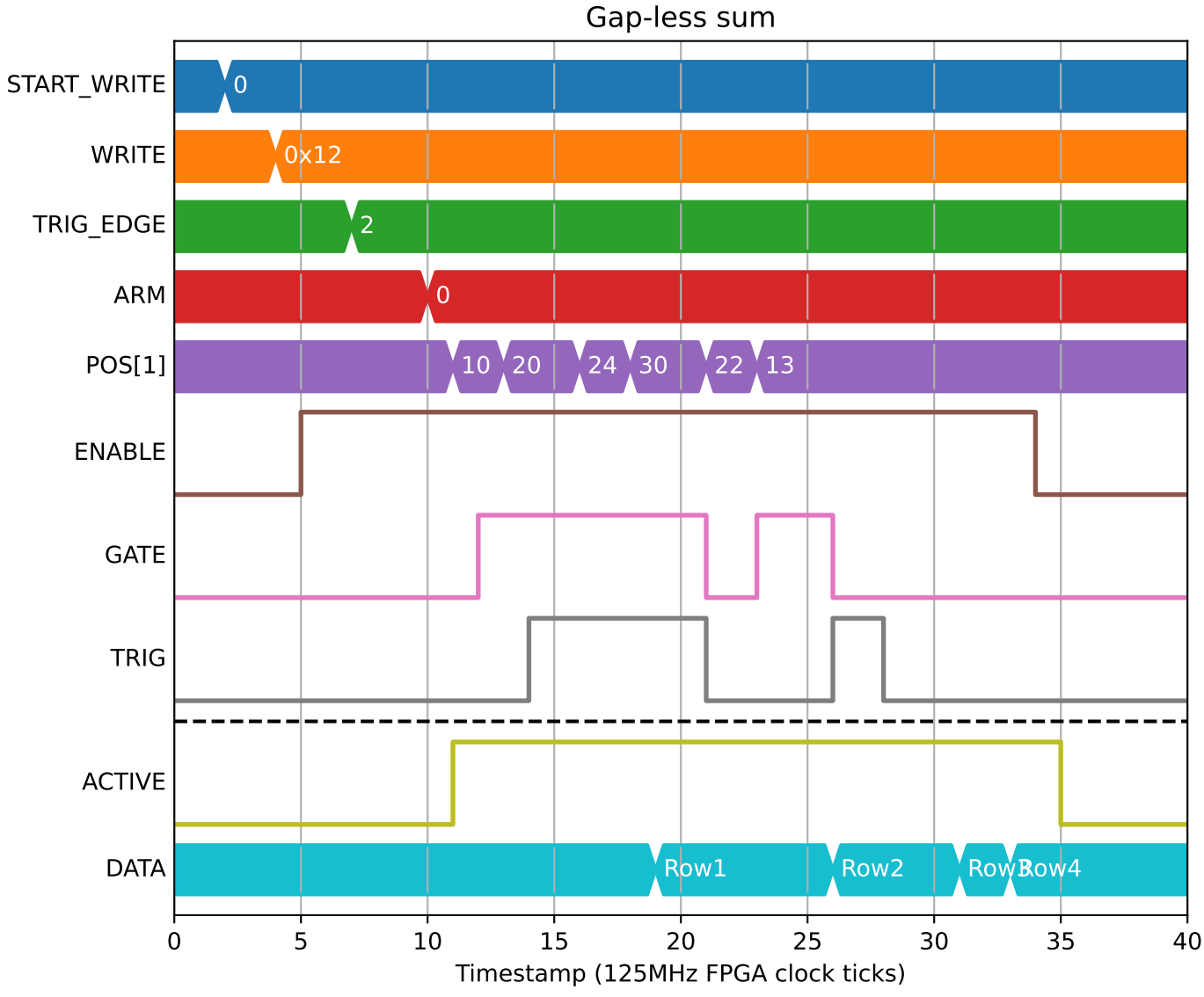
Gap-less sum
START_WRITE
0
WRITE
0x12
TRIG_EDGE
2
ARM
0
POS[1]
10
20
24
30
22
13
ENABLE
GATE
TRIG
ACTIVE
DATA
Row1
Row2
Row3
Row4
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)