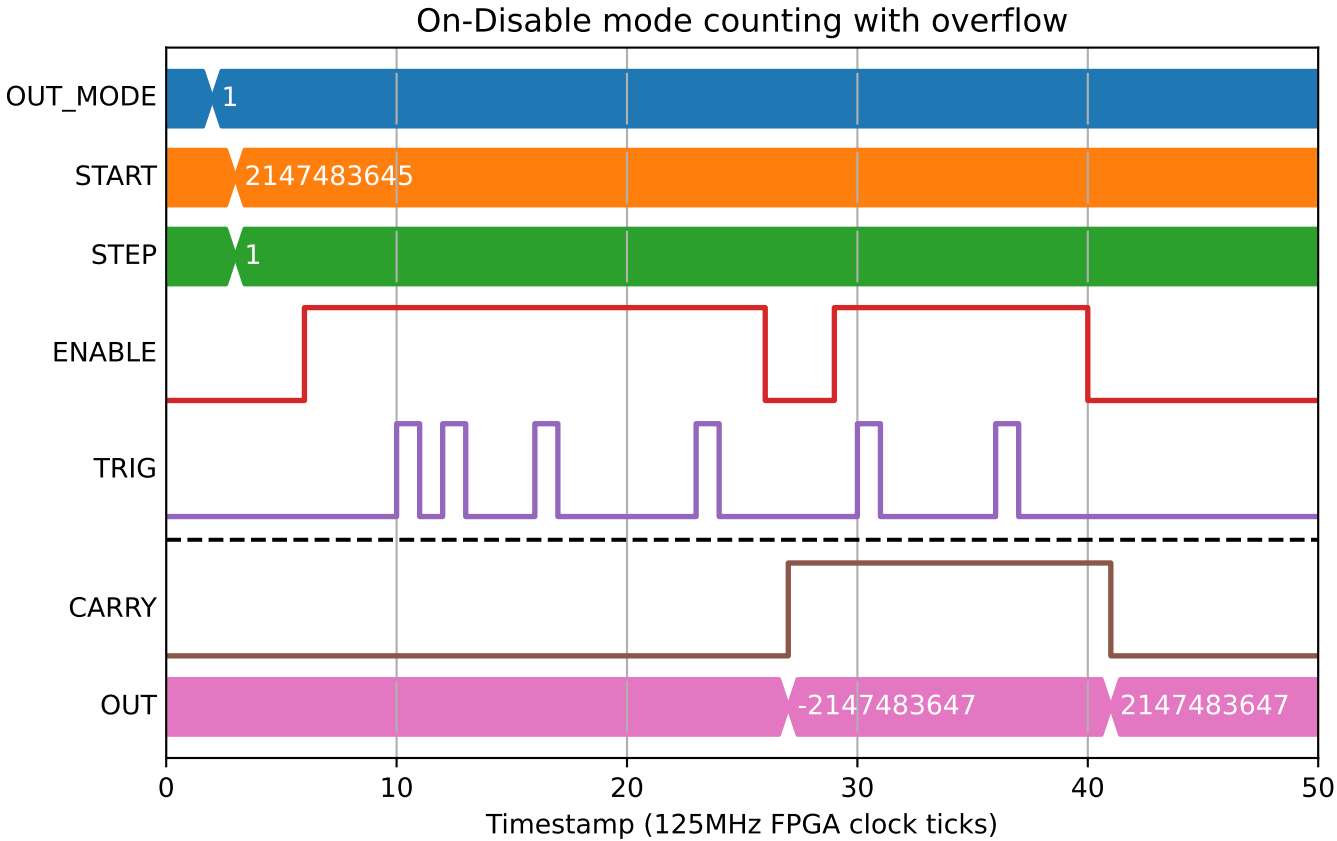
On-Disable mode counting with overflow
OUT_MODE
1
START
2147483645
STEP
1
ENABLE
TRIG
CARRY
OUT
-2147483647
2147483647
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)