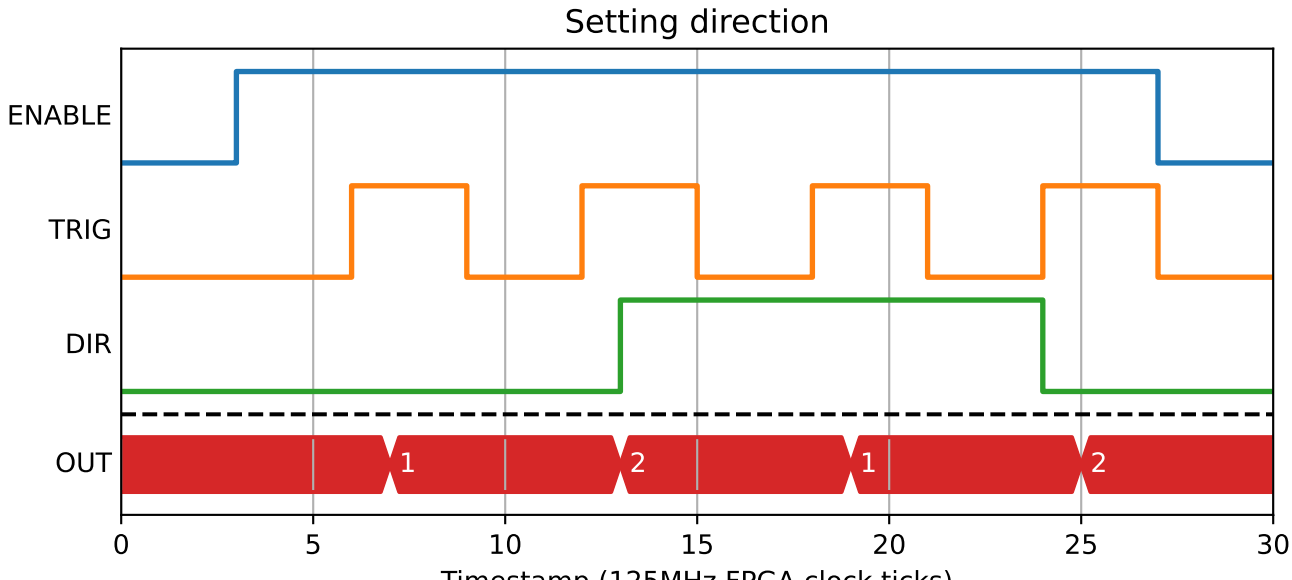
Setting direction
ENABLE
TRIG
DIR
OUT
1
2
1
2
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)