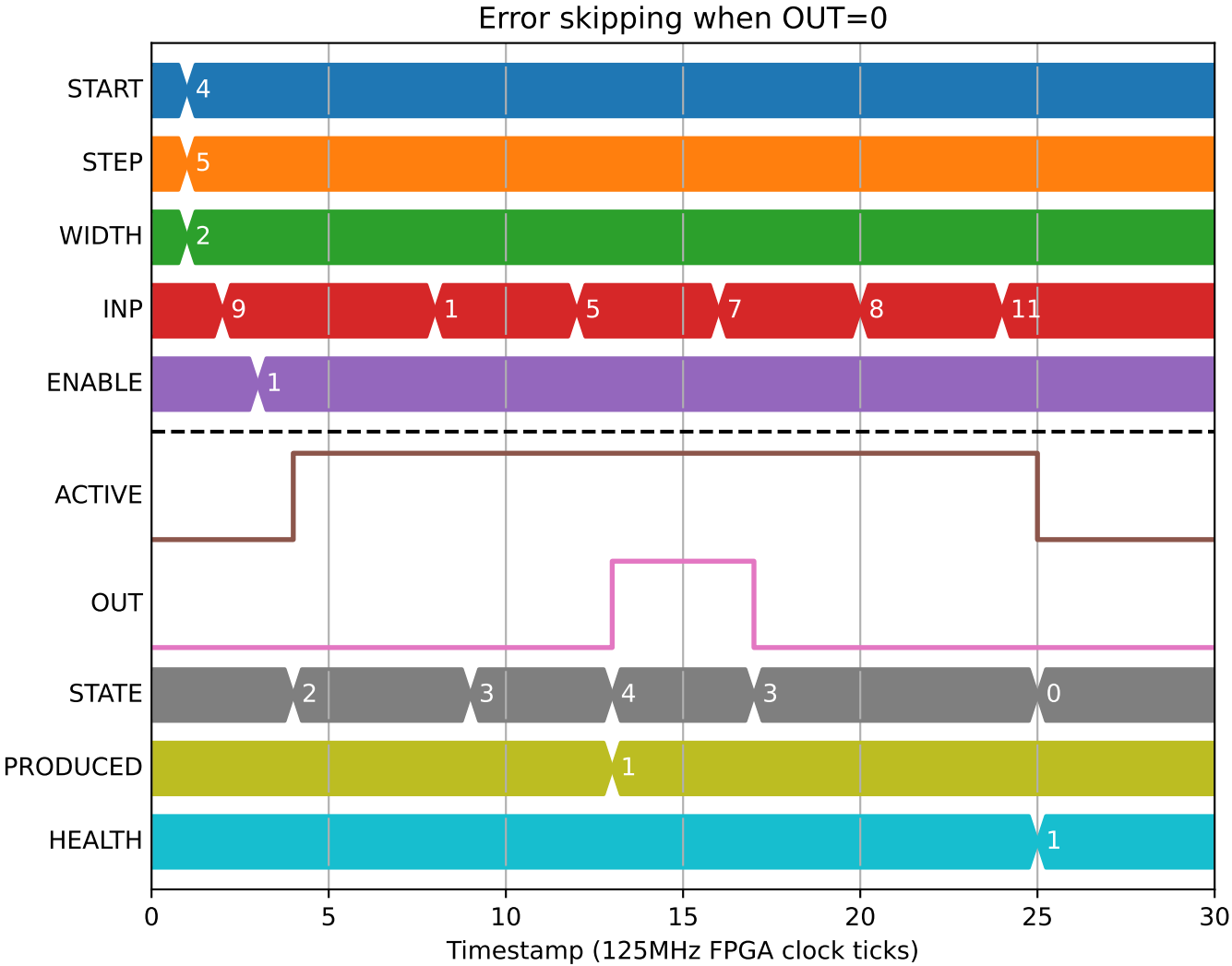
Error skipping when OUT=0
START
STEP
WIDTH
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
HEALTH
4
5
2
9
1
5
7
8
11
1
2
3
4
3
0
1
1
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)