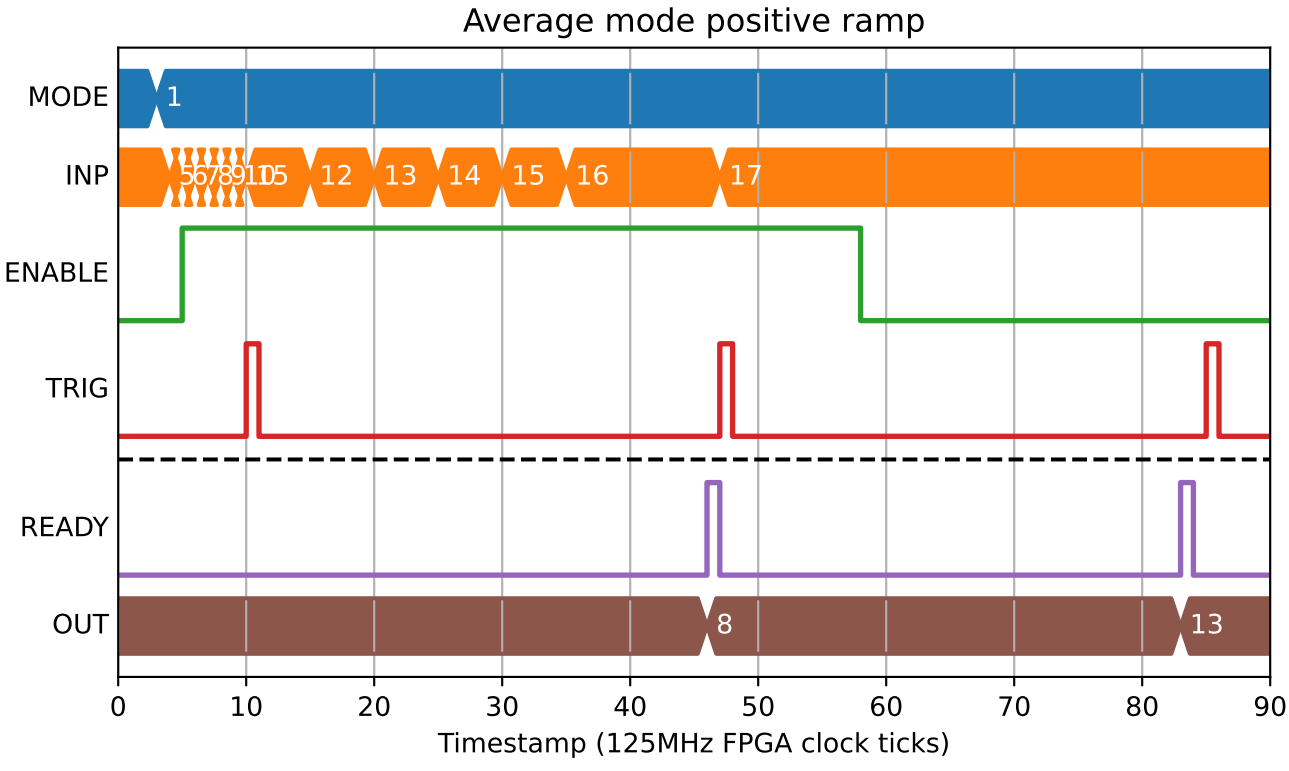
Average mode positive ramp
MODE
INP
ENABLE
TRIG
READY
OUT
1
5
6
7
8
9
10
11
12
13
14
15
16
17
8
13
0
10
20
30
40
50
60
70
80
90
Timestamp (125MHz FPGA clock ticks)