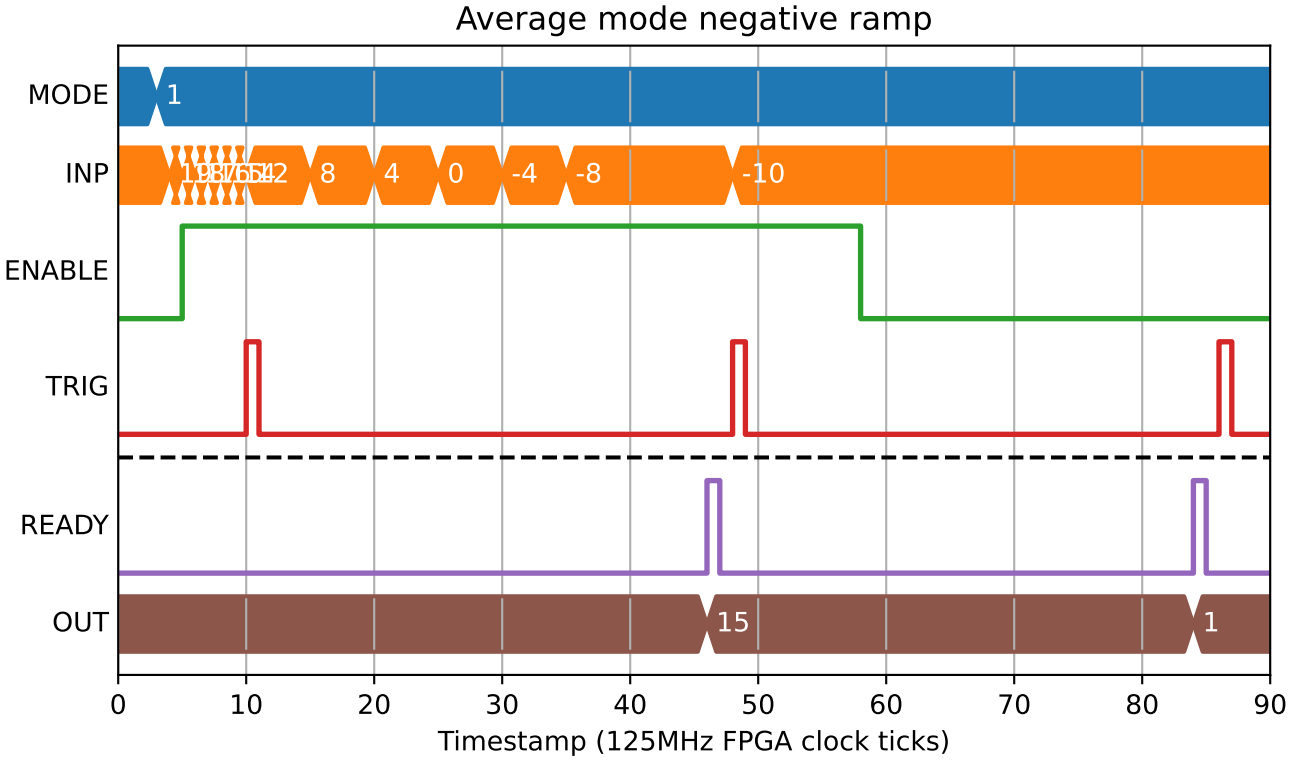
Average mode negative ramp
MODE
INP
ENABLE
TRIG
READY
OUT
1
8
4
0
-4
-8
-10
15
1
0
10
20
30
40
50
60
70
80
90
Timestamp (125MHz FPGA clock ticks)