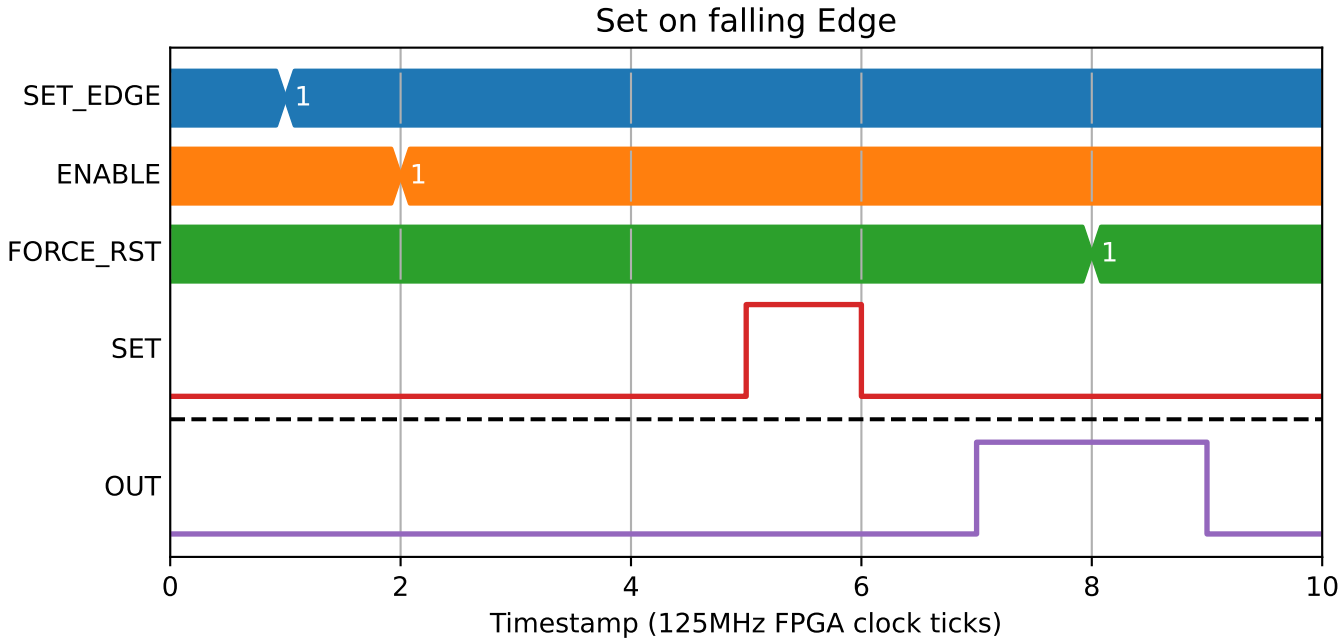
Set on falling Edge
SET_EDGE
ENABLE
FORCE_RST
SET
OUT
1
1
1
0
2
4
6
8
10
Timestamp (125MHz FPGA clock ticks)