

The diagram illustrates the timing of a 3-bit counter. The signals are as follows:

- Signal 3 (Blue):** Constant high.
- Signal 1 (Orange):** Constant high.
- Signal 2 (Green):** Square wave, high for the first half of each clock cycle.
- Signal 0 (Red):** Square wave, high for the second half of each clock cycle.
- Signal 4 (Purple):** Square wave, high for the first half of each clock cycle.

The bottom row shows the counter state (000, 001, 010, 011, 100, 101, 110, 111) in a sequence of 8 states.

Timestamp (125MHz FPGA clock ticks)