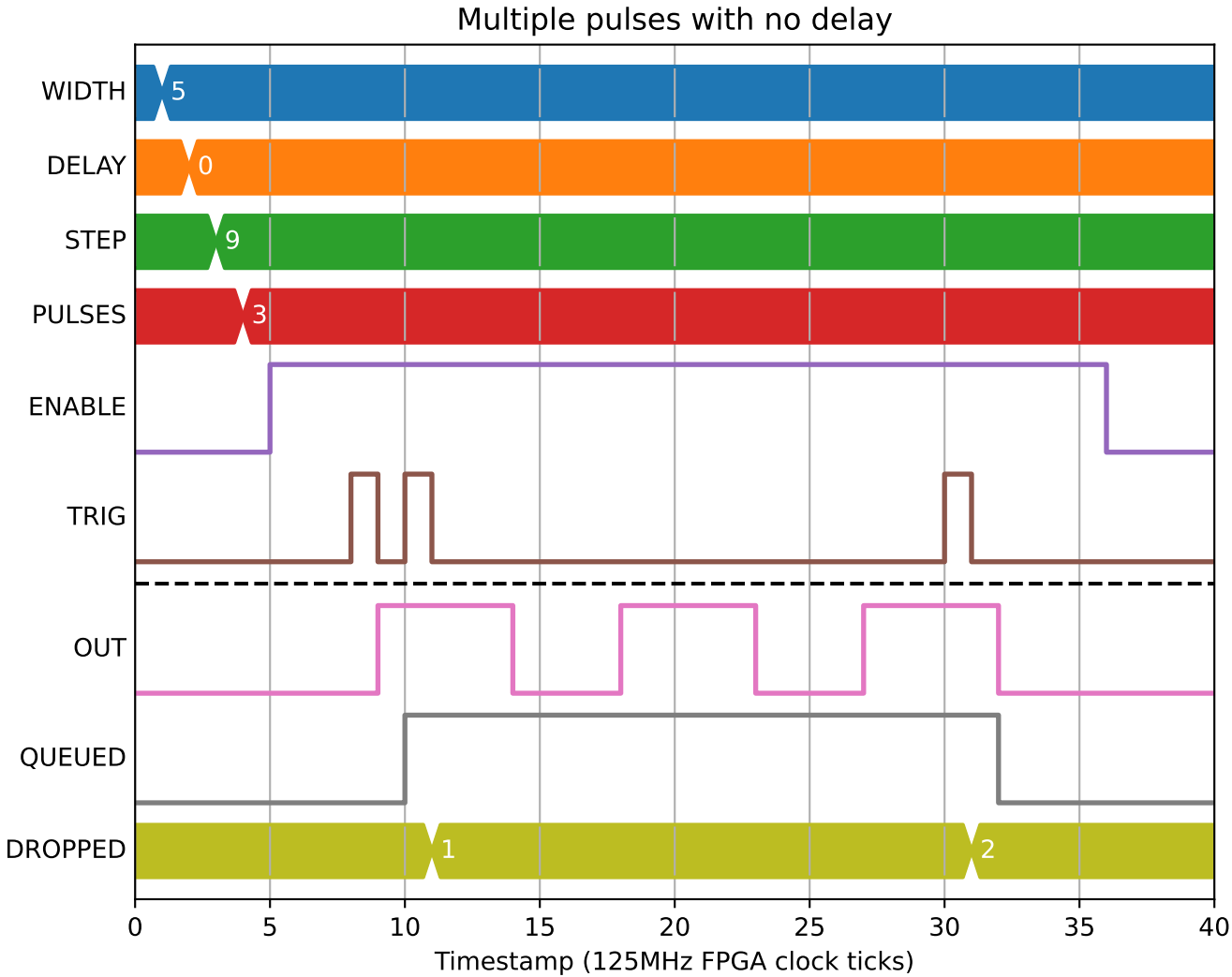
Multiple pulses with no delay
WIDTH
DELAY
STEP
PULSES
ENABLE
TRIG
OUT
QUEUED
DROPPED
5
0
9
3
1
2
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)