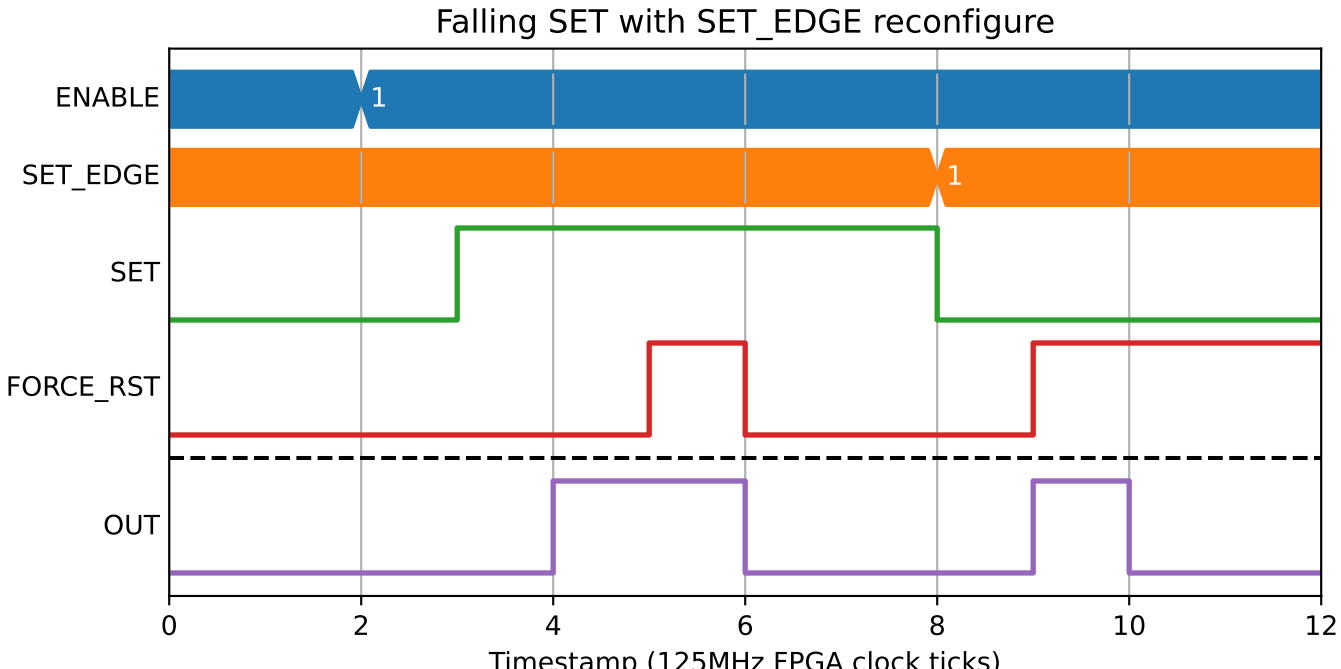
Falling SET with SET_EDGE reconfigure
ENABLE
SET_EDGE
SET
FORCE_RST
OUT
1
1
0
2
4
6
8
10
12
Timestamp (125MHz FPGA clock ticks)