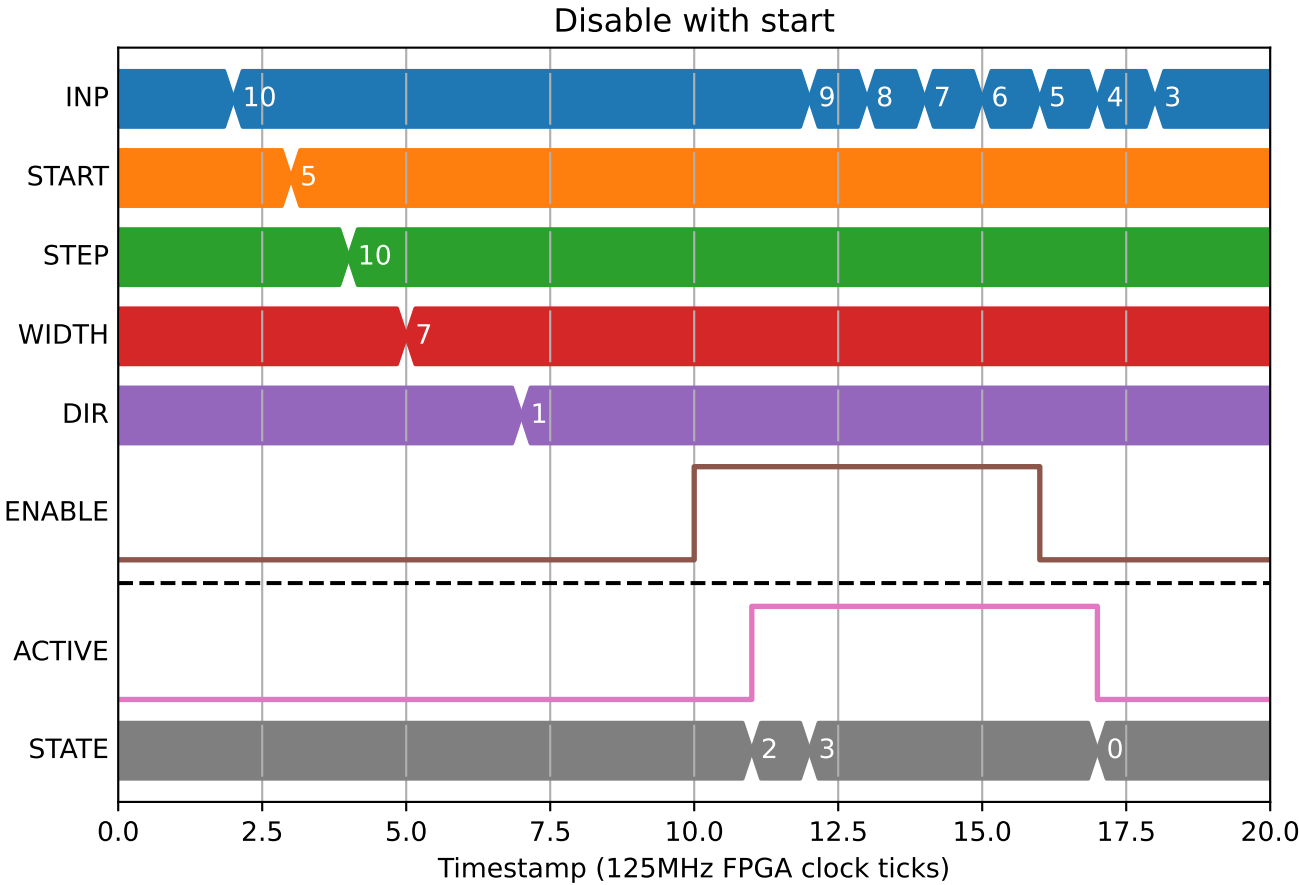
Disable with start
INP
START
STEP
WIDTH
DIR
ENABLE
ACTIVE
STATE
10
9
8
7
6
5
4
3
5
10
7
1
2
3
0
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Timestamp (125MHz FPGA clock ticks)