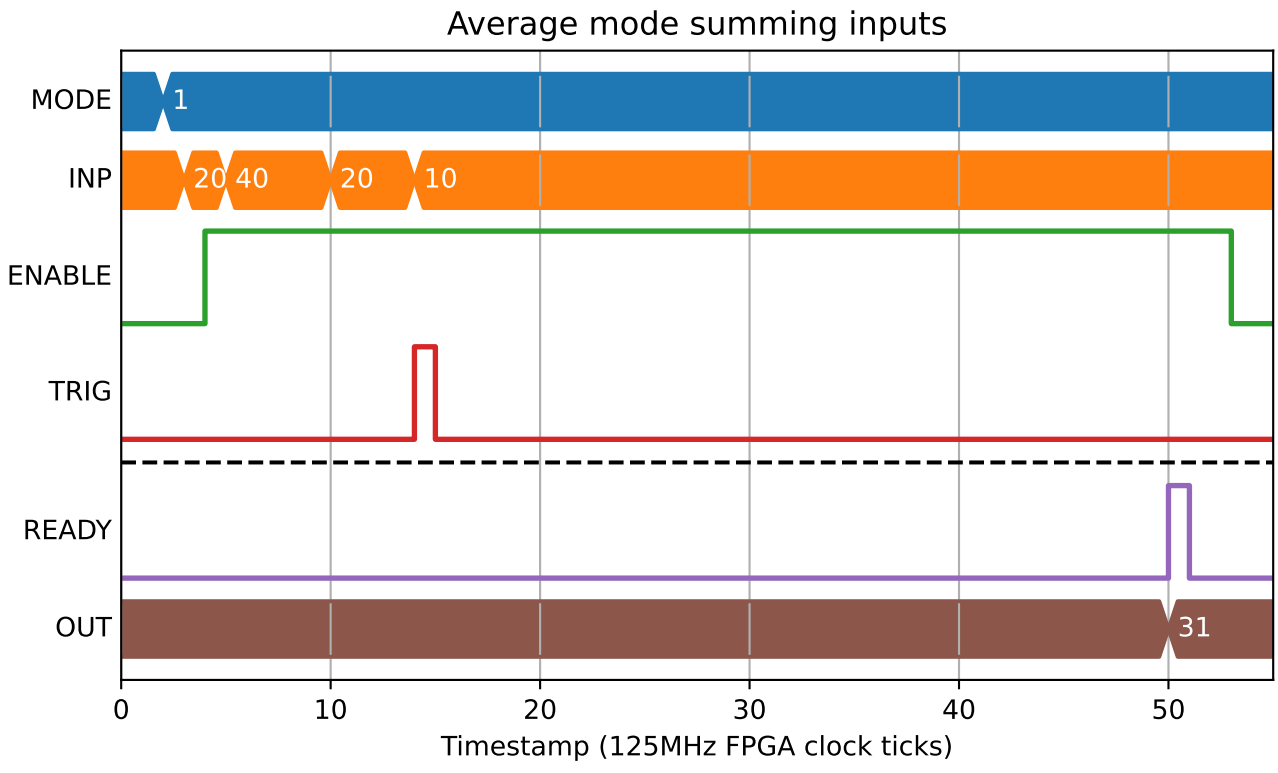
Average mode summing inputs
MODE
1
INP
20
40
20
10
ENABLE
TRIG
READY
OUT
31
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)