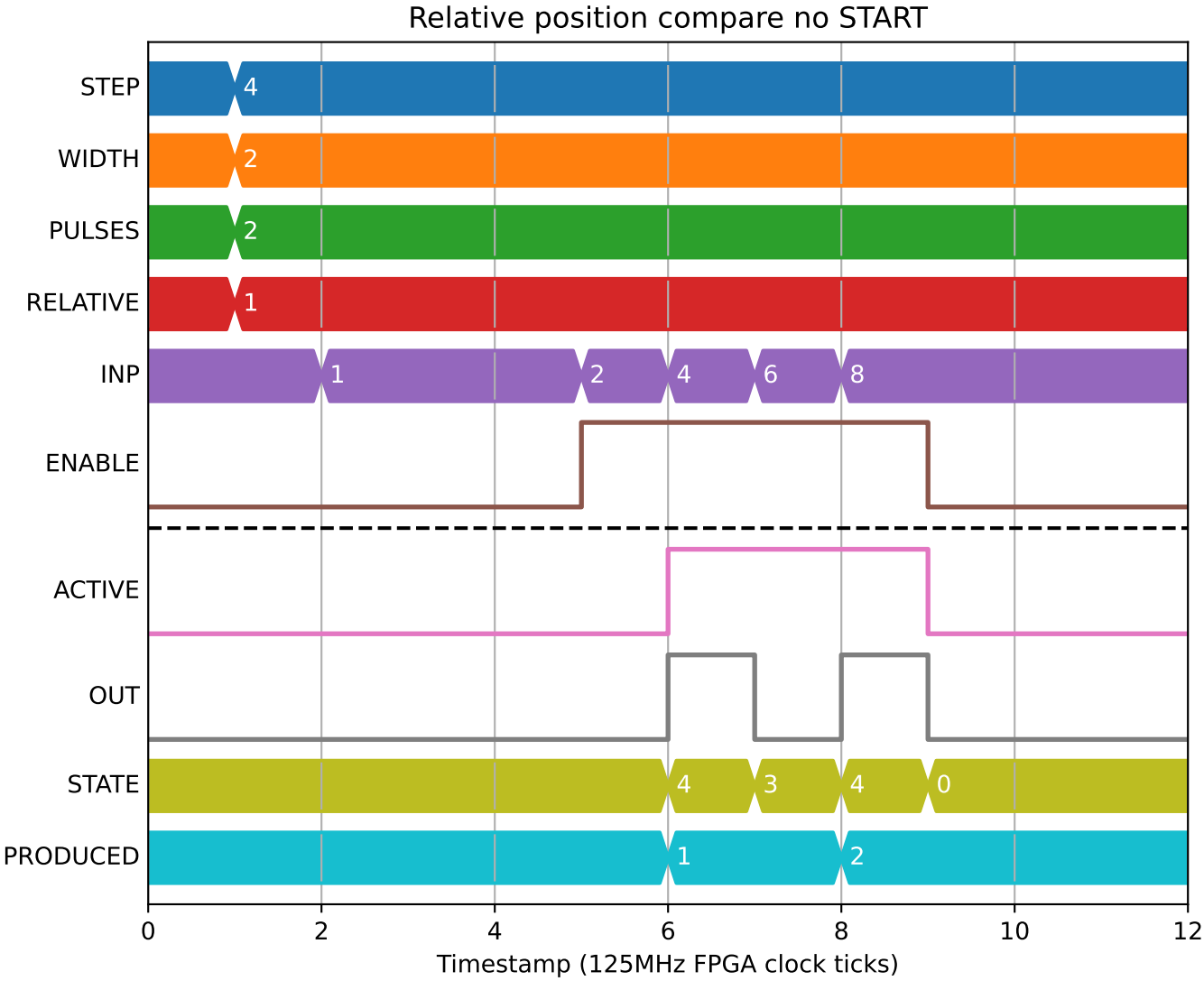
Relative position compare no START
STEP
WIDTH
PULSES
RELATIVE
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
4
2
2
1
1
2
4
6
8
4
3
4
0
1
2
0
2
4
6
8
10
12
Timestamp (125MHz FPGA clock ticks)