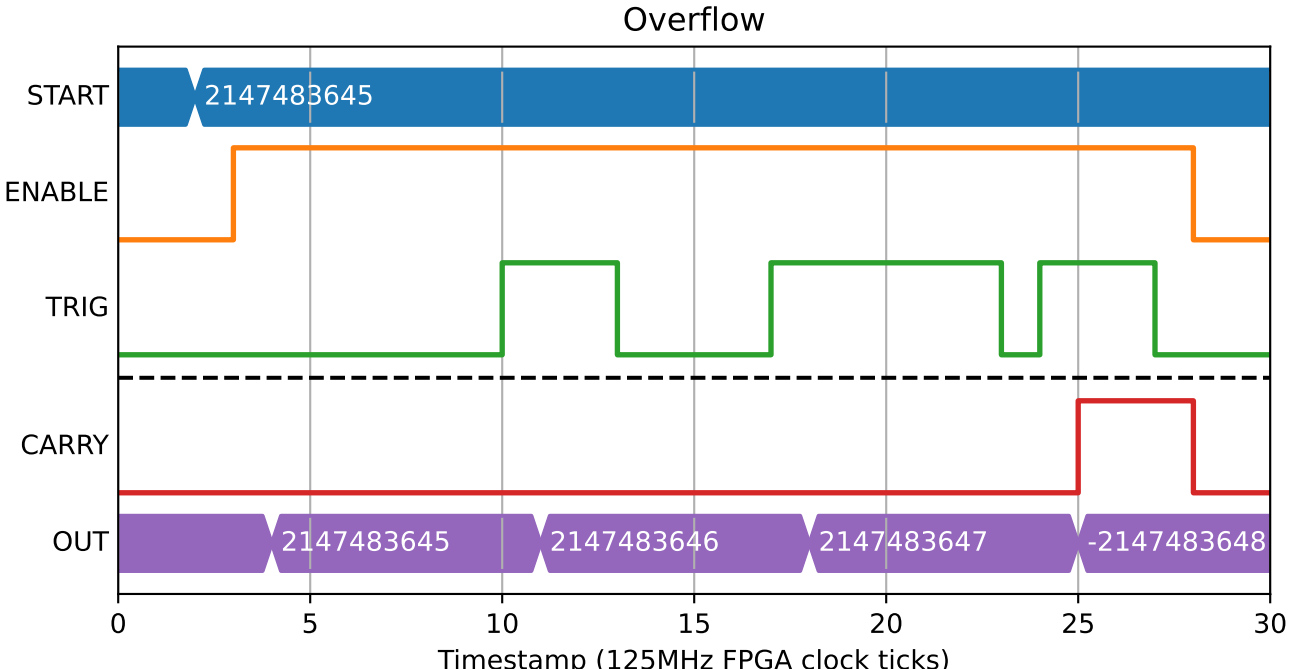
Overflow
START
ENABLE
TRIG
CARRY
OUT
2147483645
2147483645
2147483646
2147483647
-2147483648
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)