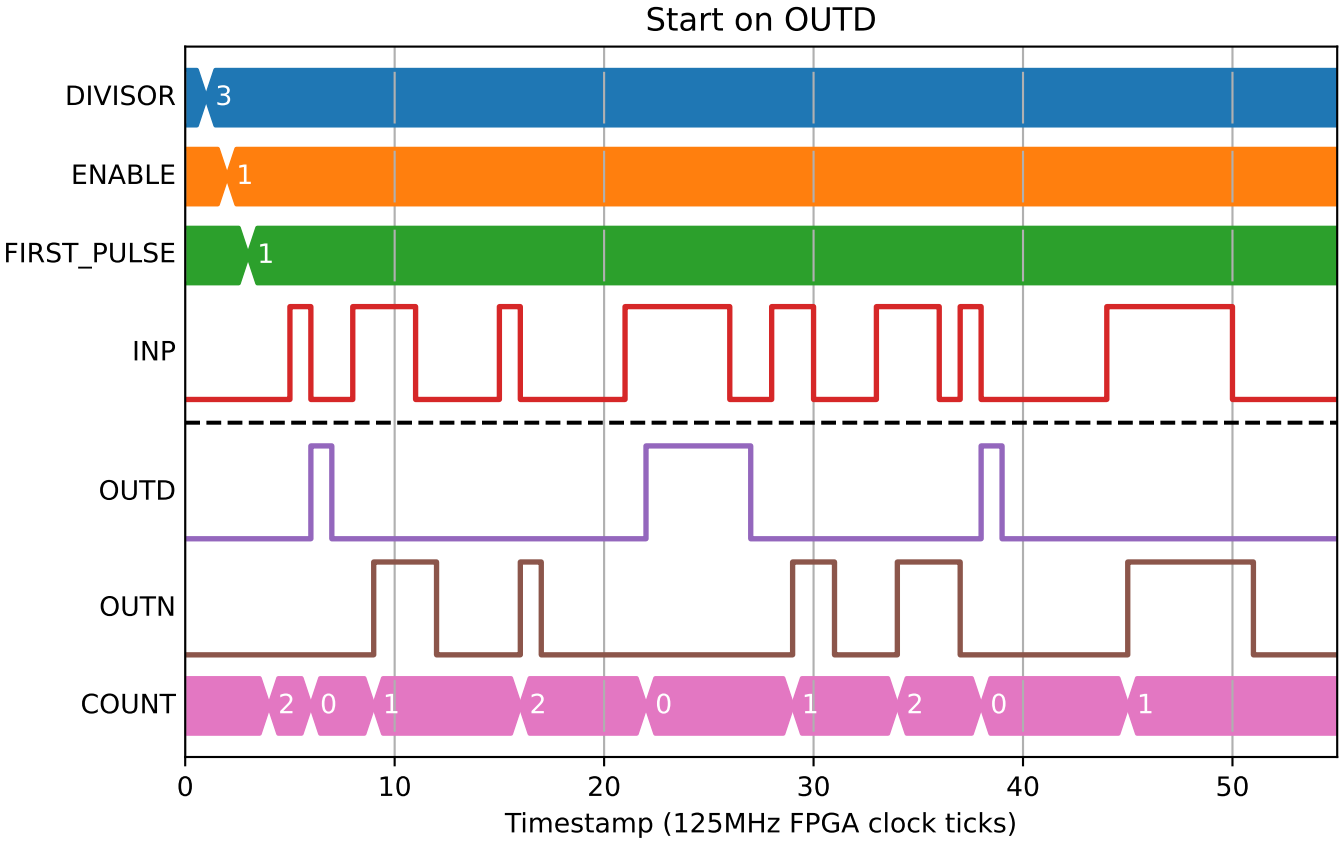
Start on OUTD
DIVISOR
ENABLE
FIRST_PULSE
INP
OUTD
OUTN
COUNT
3
1
1
2
0
1
2
0
1
2
0
1
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)