

The diagram illustrates the timing of a 3-bit counter. The signals are as follows:

- Signal 3 (Blue):** Constant high.
- Signal 1 (Orange):** Constant high.
- Signal 2 (Green):** Square wave with a period of 10 units.
- Signal 0 (Red):** Square wave with a period of 10 units.
- Signal 1 (Purple):** Square wave with a period of 10 units.

The bottom row shows the counter state (1, 2, 0, 1, 2, 0, 1, 2) in brown blocks.

Timestamp (125MHz FPGA clock ticks)