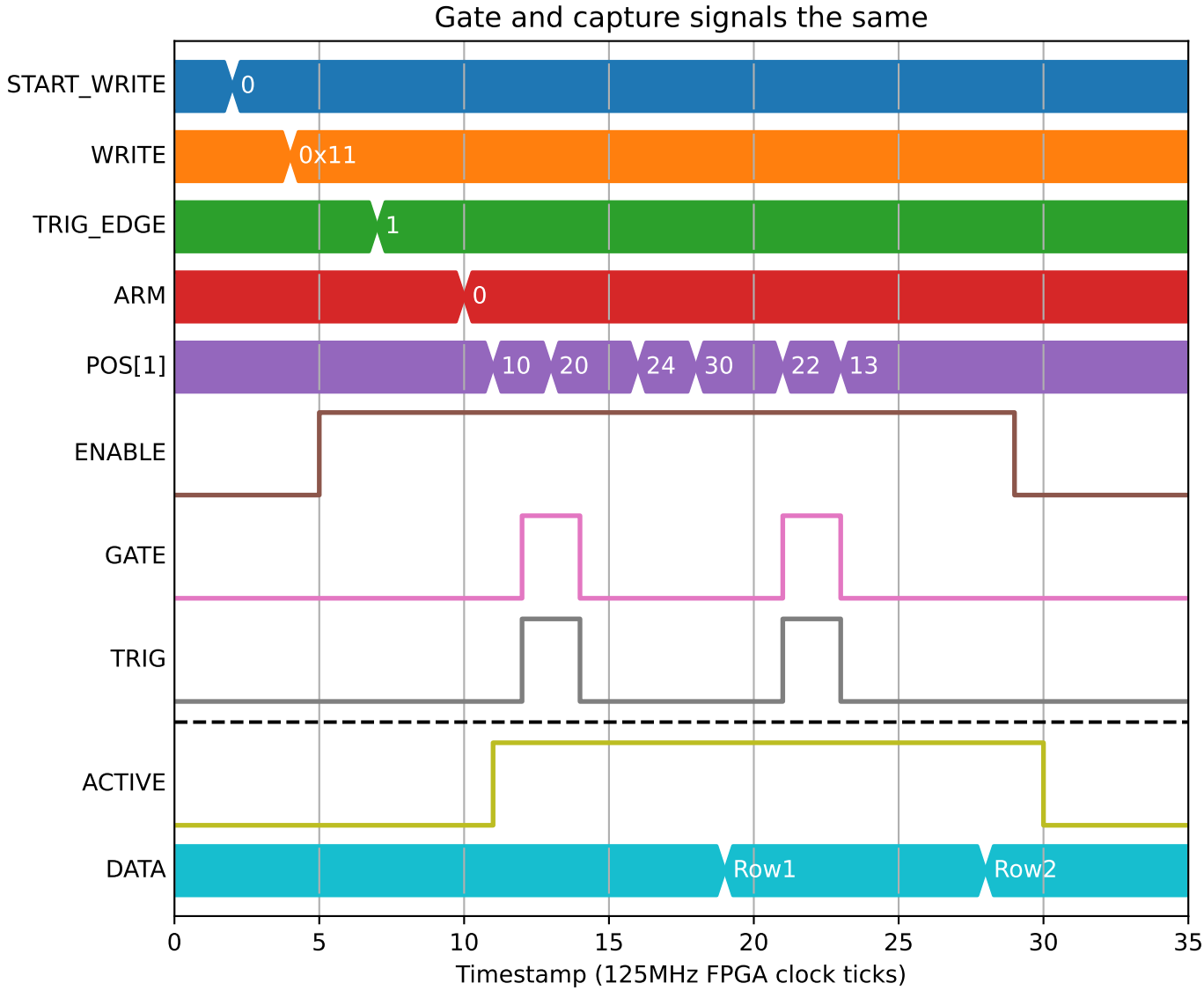
Gate and capture signals the same
START_WRITE
0
WRITE
0x11
TRIG_EDGE
1
ARM
0
POS[1]
10
20
24
30
22
13
ENABLE
GATE
TRIG
ACTIVE
DATA
Row1
Row2
0
5
10
15
20
25
30
35
Timestamp (125MHz FPGA clock ticks)