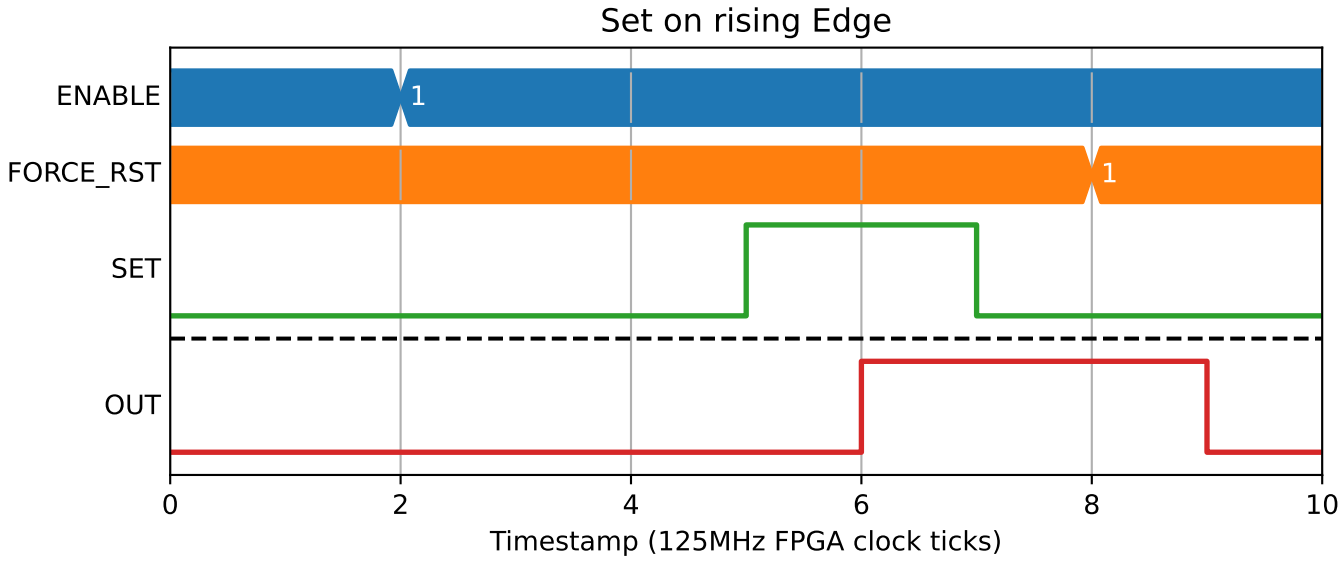
Set on rising Edge
ENABLE
1
FORCE_RST
1
SET
OUT
0
2
4
6
8
10
Timestamp (125MHz FPGA clock ticks)