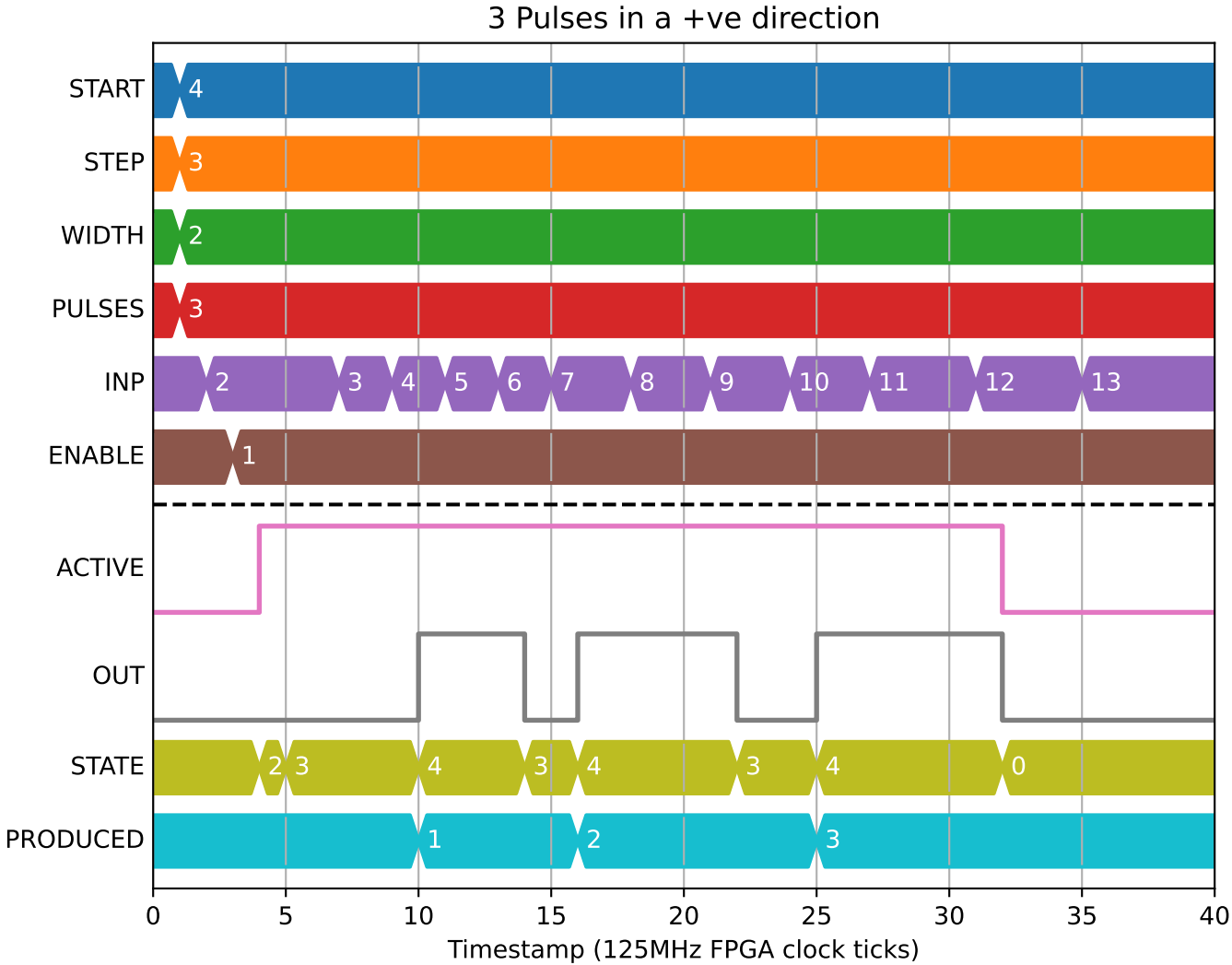
3 Pulses in a +ve direction
START
STEP
WIDTH
PULSES
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
4
3
2
3
2 3 4 5 6 7 8 9 10 11 12 13
1
2 3 4 3 4 3 4 0
1 2 3
0 5 10 15 20 25 30 35 40
Timestamp (125MHz FPGA clock ticks)