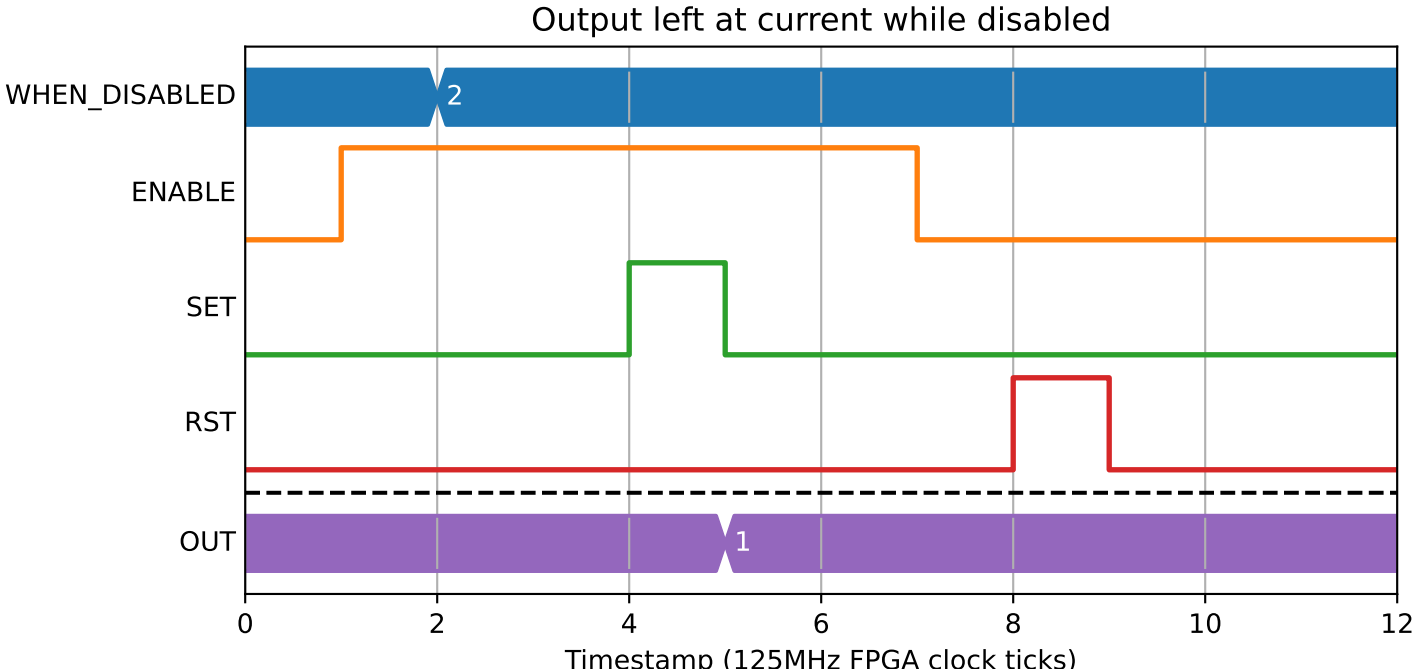
Output left at current while disabled
WHEN_DISABLED
ENABLE
SET
RST
OUT
2
1
0
2
4
6
8
10
12
Timestamp (125MHz FPGA clock ticks)