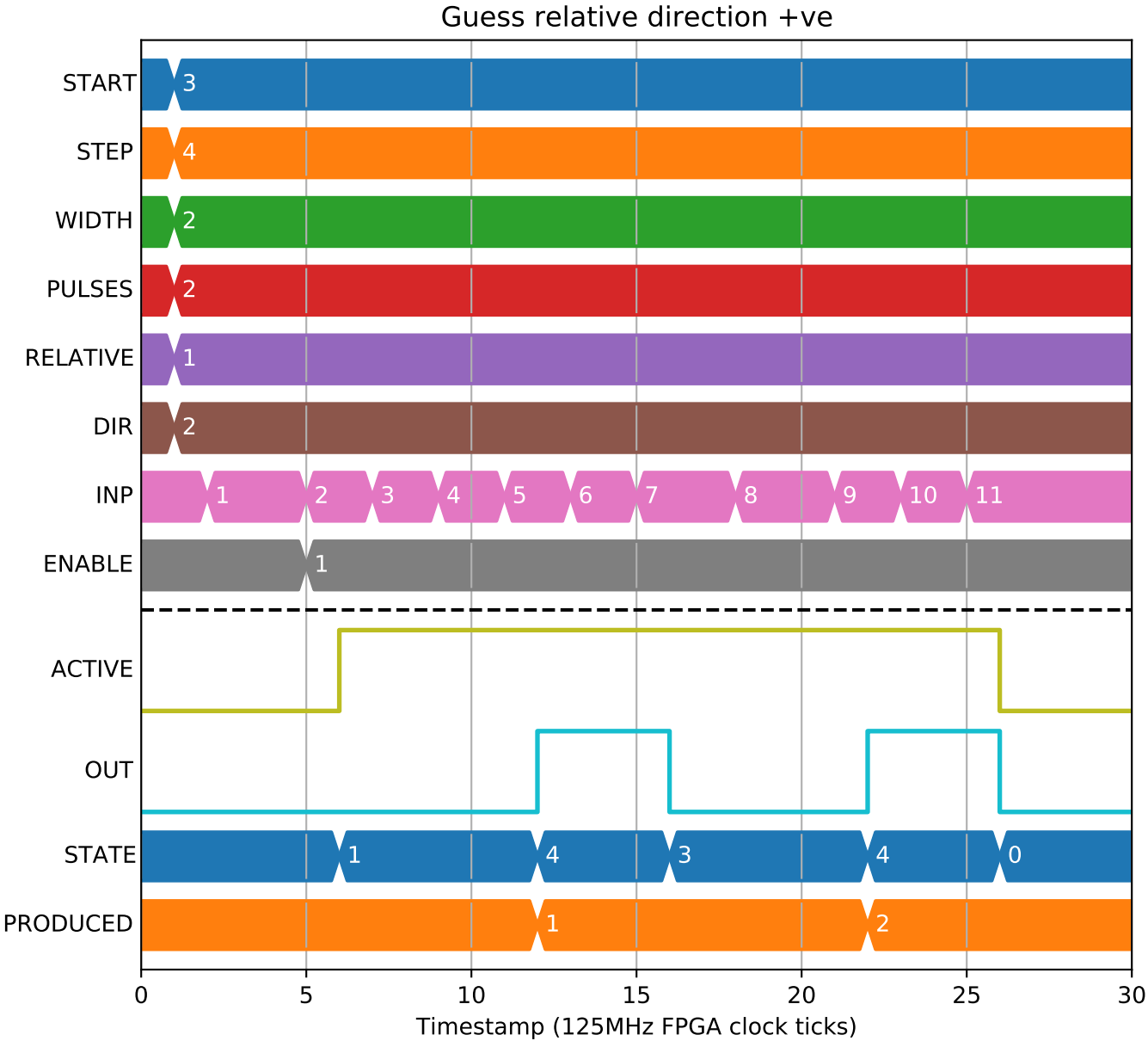
Guess relative direction +ve
START
STEP
WIDTH
PULSES
RELATIVE
DIR
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
3
4
2
2
1
2
1 2 3 4 5 6 7 8 9 10 11
1
1 4 3 4 0
1 2
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)