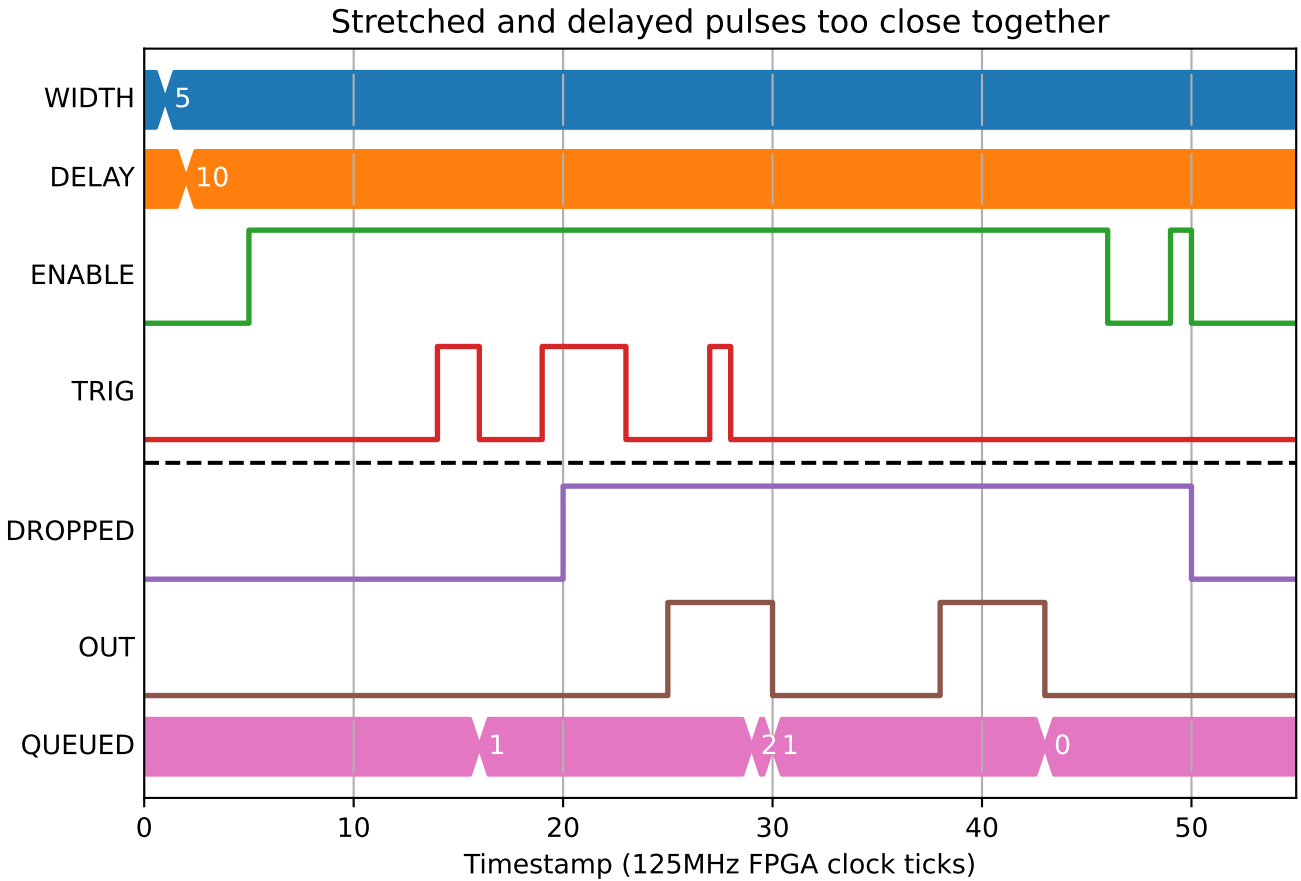
Stretched and delayed pulses too close together
WIDTH
5
DELAY
10
ENABLE
TRIG
DROPPED
OUT
QUEUED
1
2
1
0
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)