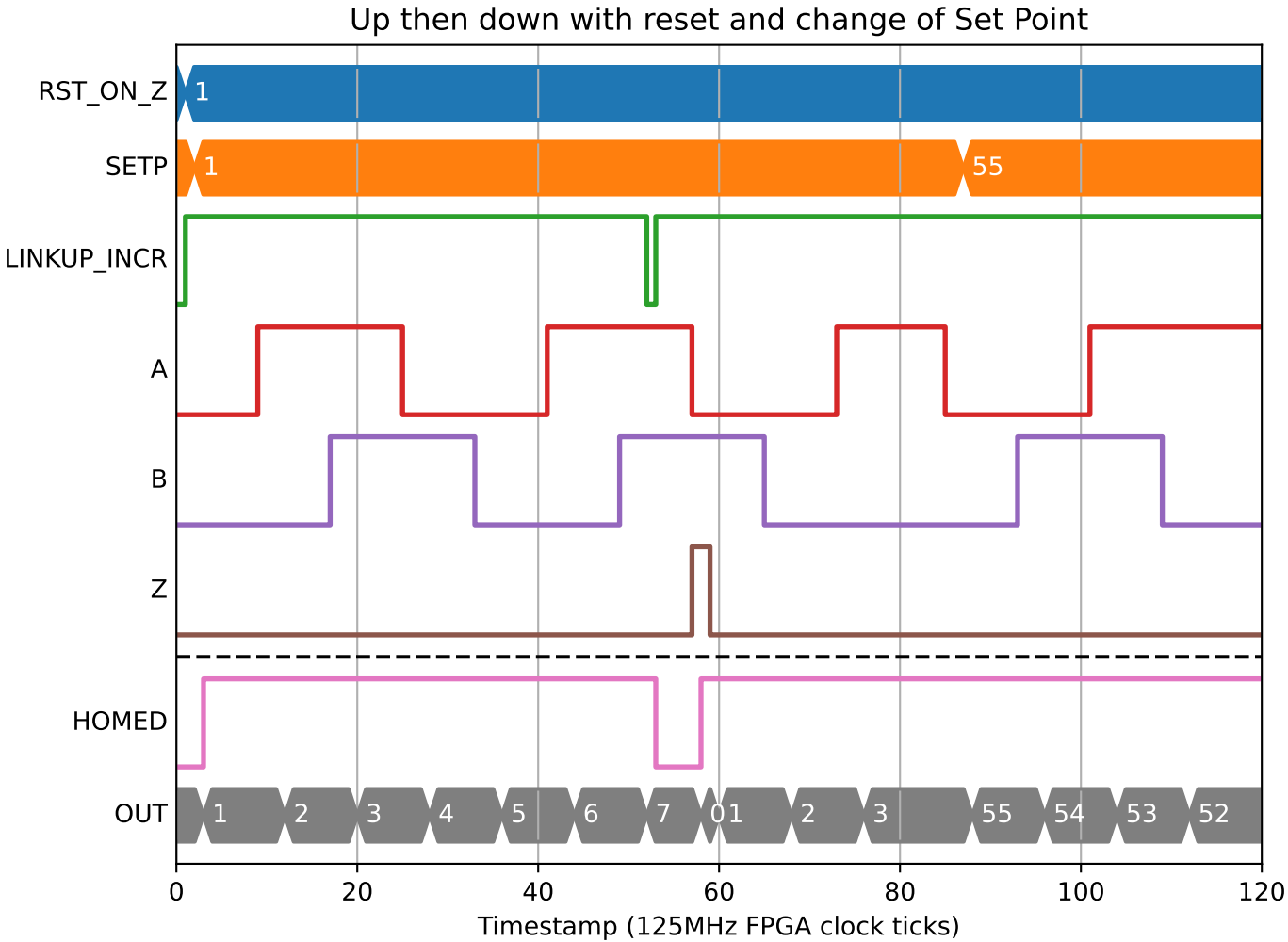
Up then down with reset and change of Set Point
RST_ON_Z
SETP
LINKUP_INCR
A
B
Z
HOMED
OUT
1
1
55
1
2
3
4
5
6
7
0
1
2
3
55
54
53
52
0
20
40
60
80
100
120
Timestamp (125MHz FPGA clock ticks)