CSE 251
Electronic Devices and Circuits

Lecture 13-15

BRAC UNIVERSITY
Inspiring Excellence

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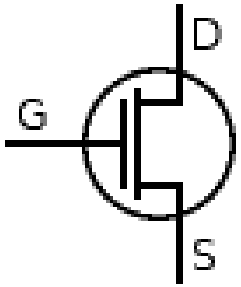
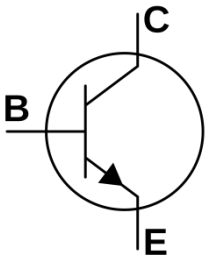
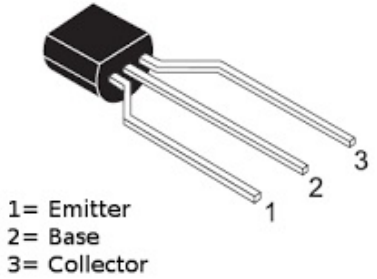
Lecture 13: Introduction to Transistor

- **Transistor:** probably the most impactful invention of the present world
- There are two major types of three-terminal semiconductor devices:
  - Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)
  - Bipolar Junction Transistor (BJT)



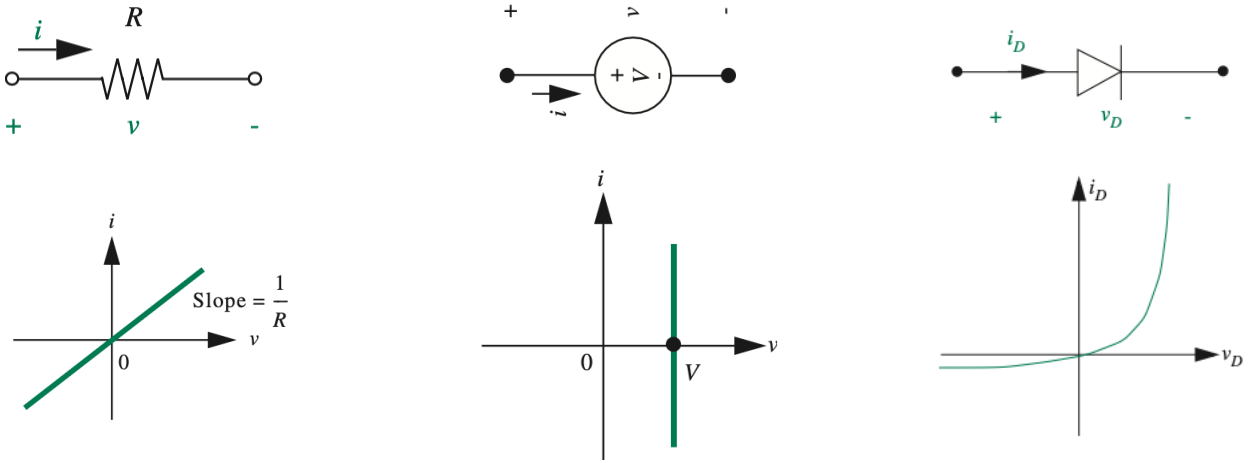




Symbols and images of transistors: MOSFET & BJT

Three terminal devices

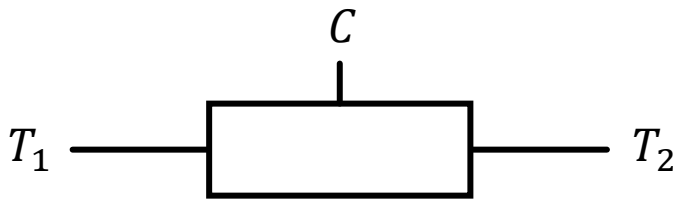
- Two terminal devices have fixed IV characteristics

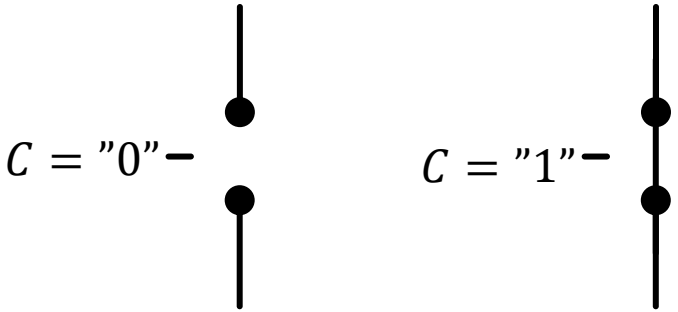


- Three terminal devices: I-V of two terminal can be controlled using the third terminal.
- Examples: Switch (linear), Transistors (non-linear)

Switch – IV Characteristics

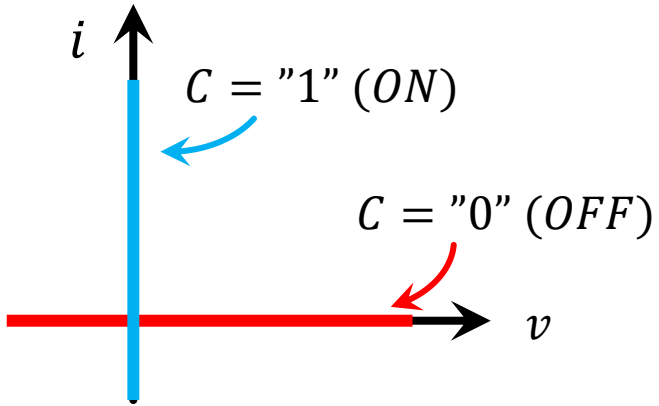
- IV characteristics between terminal T_1 and T_2 is controlled by C





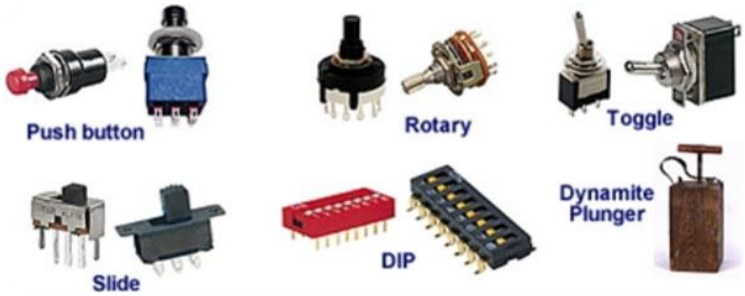
Switch OFF

Switch ON

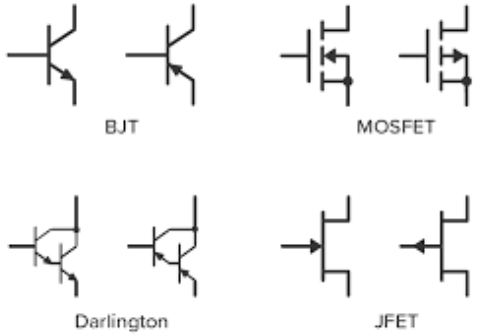


Switch – Types

- Depending on the control, the switch can be
  - **Analog**: Controlled using physical toggle/button
  - **Digital**: Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



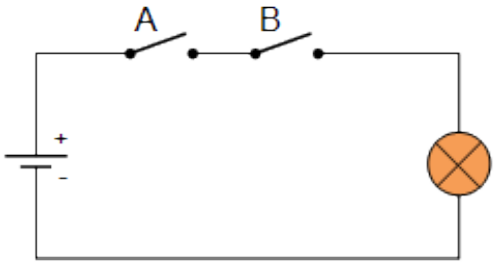
Analog switches



Digital switches (Transistors)

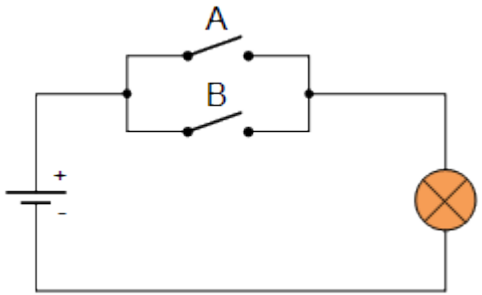
Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

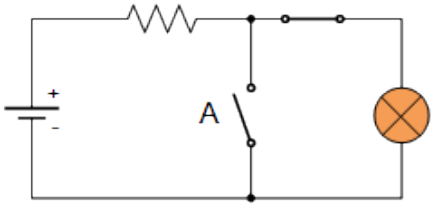
AND operation



A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

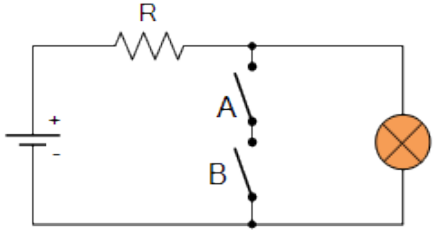
OR operation

Switch Application – Logic Gates



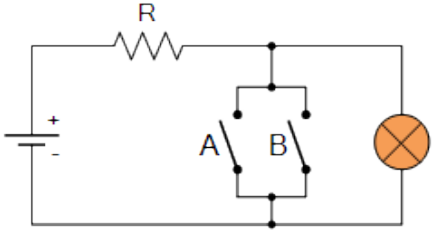
A	Bulb
0	ON
1	OFF

NOT operation



A	B	Bulb
0	0	ON
0	1	ON
1	0	ON
1	1	OFF

NAND operation



A	B	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

NOR operation

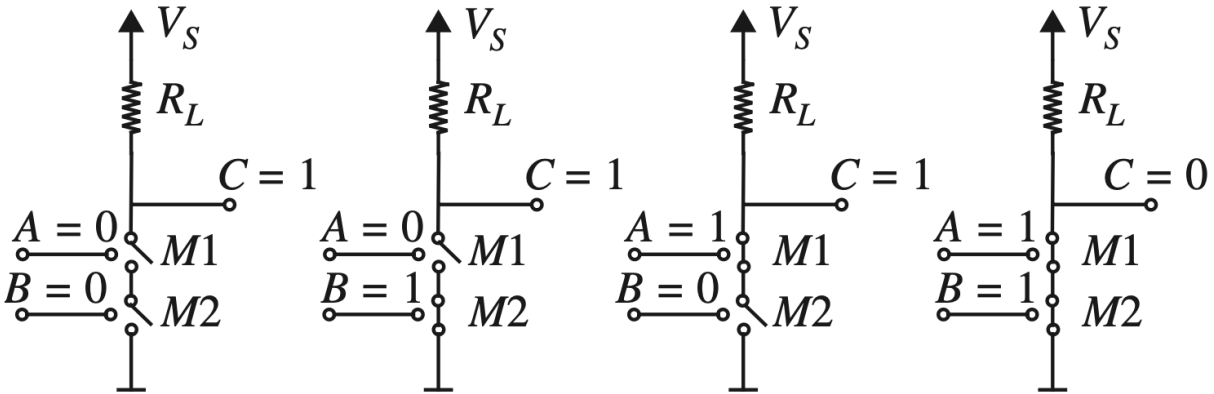
- These circuits are “preferred” – because they can be cascaded to build combinational logic circuit, if we remove the bulb and use the voltage across instead to cascade and drive the next gate

Switch Application – Logic Gates

Alternative representations:

Switch Application – Logic Gates

Alternative representations:



Switch Application – Logic Gates

A	V_{OUT}
0	5V
1	0V

A	B	V_{OUT}
0	0	5V
0	1	5V
1	0	5V
1	1	0V

A	B	V_{OUT}
0	0	5V
0	1	0V
1	0	0V
1	1	0V

Examples

Example

Implement using switches: $f = (A + B)C$

Digital Representation

- Binary → Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

Voltage

5V → 1
0V → 0

0V → 1
3.3V → 0

Current

2mA → 1
3mA → 0

State

ON → 1
OFF → 0

Low resistance → 1
High resistance → 0

Digital Representation

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- Binary variables in circuit, need to use two states of device/parameters

Voltage

5V → 1
0V → 0

0V → 1
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Current

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3mA → 0

State

ON → 1
OFF → 0

Low resistance → 1
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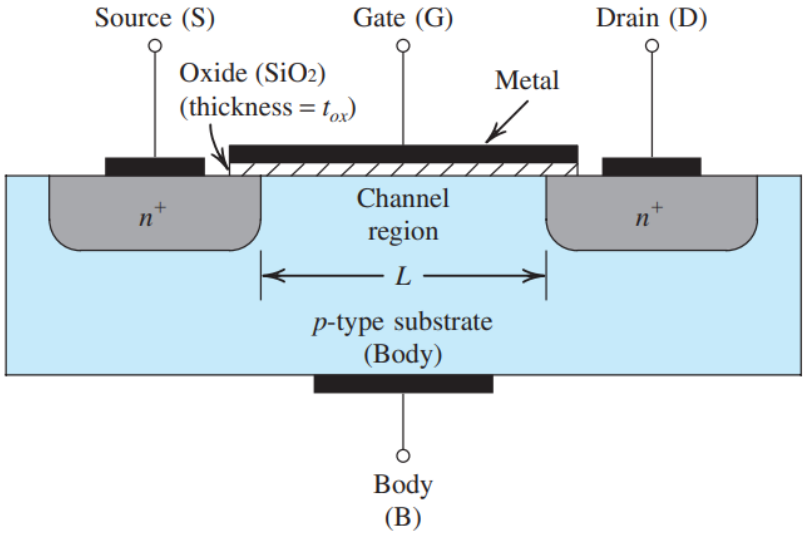
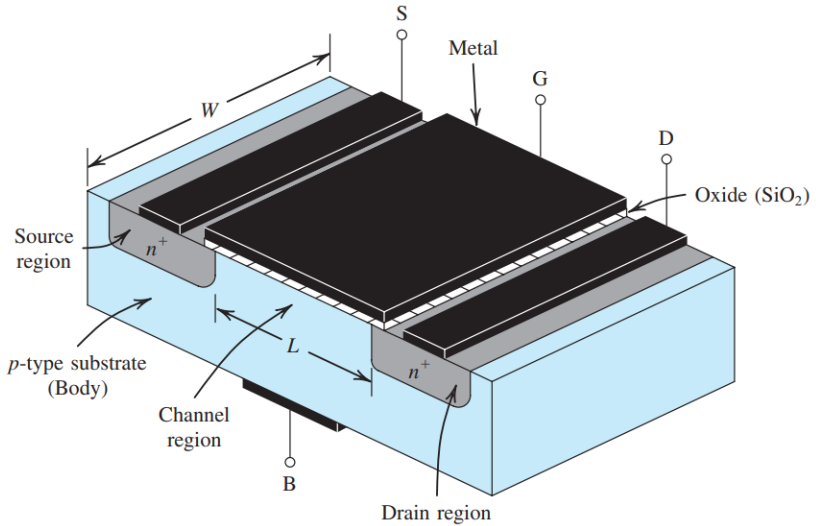
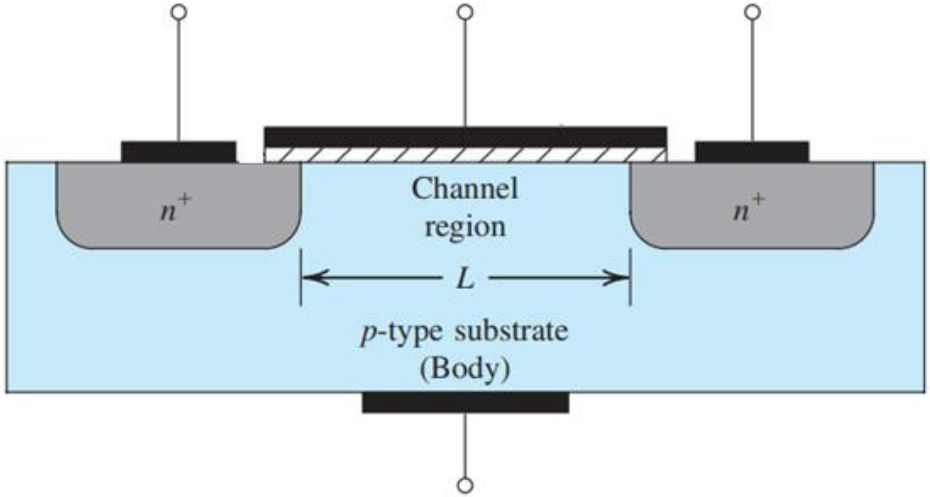
Lecture 14: How does MOSFET work?



NMOS Transistor: perspective view

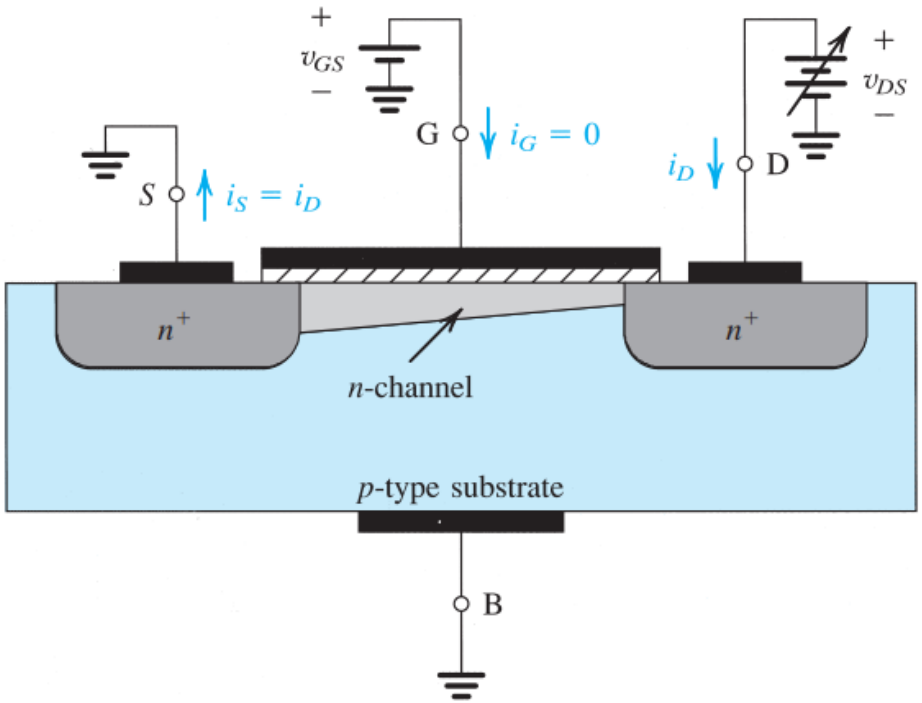


NMOS Transistor: cross section



We analyzed 6 cases to explain the working procedure of MOSFET

Operation of the enhancement NMOS transistor as vDS is increased



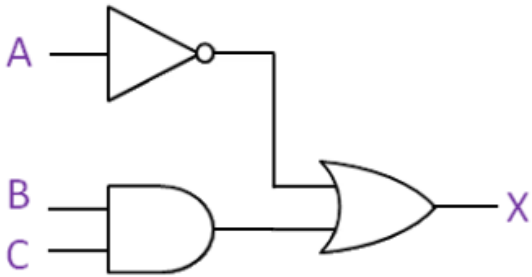
Digital Representation

Suppose you want to send 010110

- Single value based representaion fails in the presence of noise
- Better approach – threshold-based system
- Simplest: Logical 0 = $V < V_T$ Logical 1 = $V > V_T$

Static Discipline

- Specification for digital devices
- Requires devices to adhere to common representation to ensure that **valid input produces valid output**
- This means, if

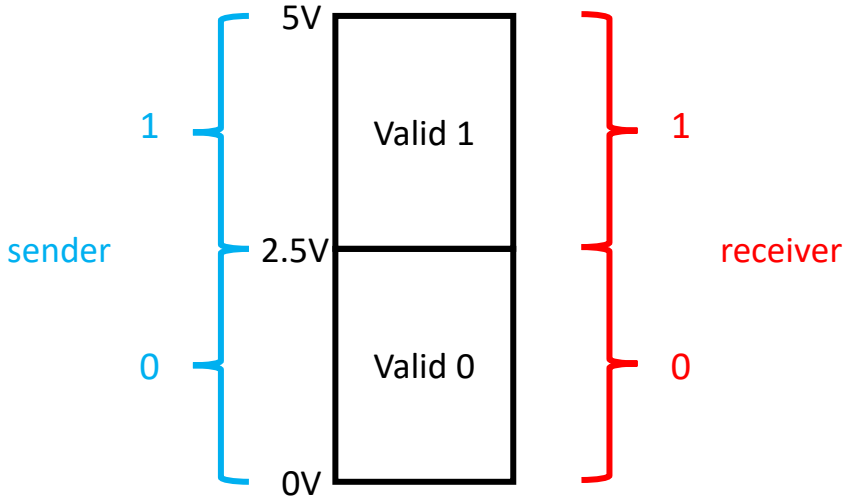


  - Sender sends “0” Receiver interprets as “0”

  - Sender sends ”1” Receiver interprets as “1”

Static Discipline

Naïve approach: Single threshold based system



$V_T = 2.5\ V$

sender

Logical 0: $V_o < V_T$
Logical 1: $V_o > V_T$

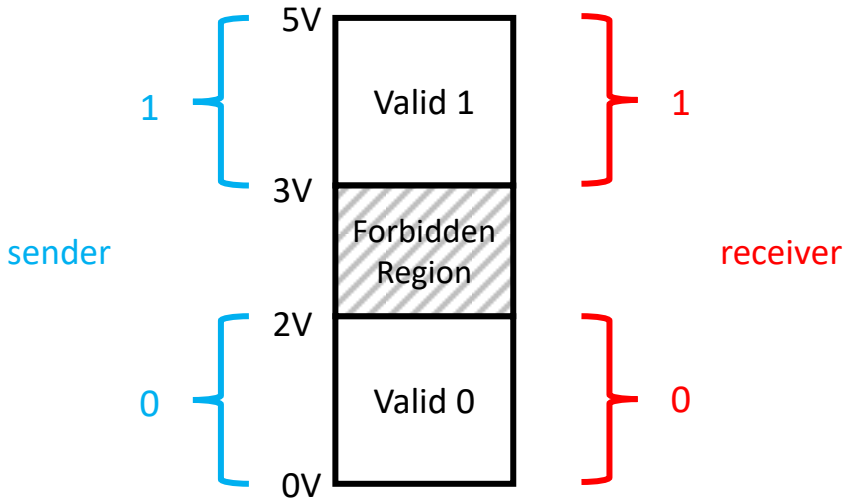
receiver

Logical 0: $V_i < V_T$
Logical 1: $V_i > V_T$

What if $V_i = 2.5V$? Undefined!

Static Discipline

Double threshold based system



V_H = High voltage threshold = $3V$

V_L = Low voltage threshold = $2V$

sender	receiver
Logical 0: $V_o < V_L$	Logical 0: $V_i < V_L$
Logical 1: $V_o > V_H$	Logical 1: $V_i > V_H$

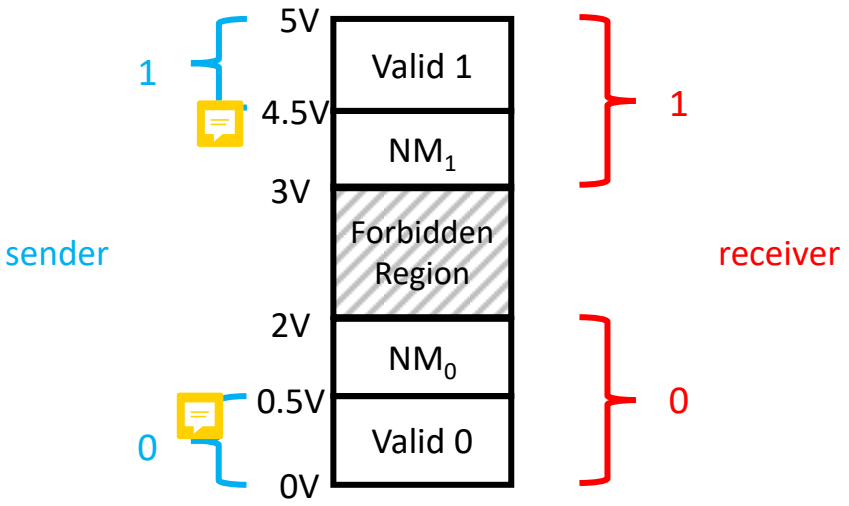
What if $V_o = 1.9V$ and channel noise is $0.5V$?

$V_i = 1.9V + 0.5V = 2.4V =$ invalid

➔ valid output producing invalid input, i.e., no margin for noise

Static Discipline

Four threshold based system → Tighter restriction on sender (**output**)



V_{OH} = Output high voltage threshold = $4.5V$

V_{OL} = Output low voltage threshold = $0.5V$

V_{IH} = Input high voltage threshold = $3V$

V_{IL} = Input low voltage threshold = $2V$

sender	receiver
Logical 0: $V_o < V_{OL}$	Logical 0: $V_i < V_{IL}$
Logical 1: $V_o > V_{OH}$	Logical 1: $V_i > V_{IH}$

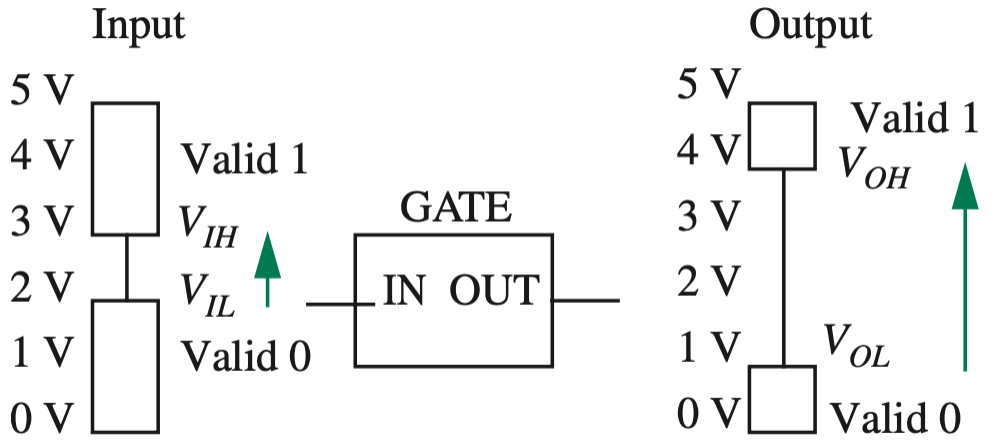
For static discipline, $V_{OL} < V_{IL} < V_{IH} < V_{OH}$

Noise margins (NM):

- $NM_1 = V_{OH} - V_{IH} = 4.5 - 3 = 1.5V$ (significance?)
- $NM_0 = V_{IL} - V_{OL} = 2 - 0.5 = 1.5V$ (significance?)

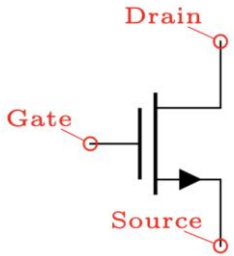
Static Discipline

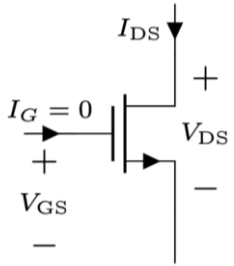
Four threshold based system → Tighter restriction on sender (**output**)

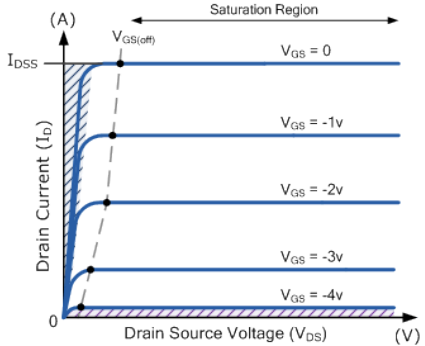


Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – Voltage Controlled, Current Controlled
- **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET) are voltage controlled
- Control, $C = V_{GS}$. The IV characteristics (I_{DS} vs V_{DS}) depends on V_{GS}
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)

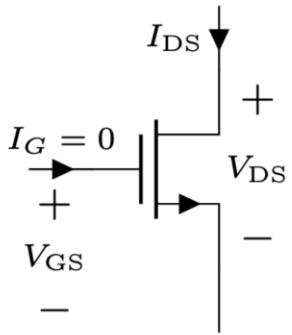


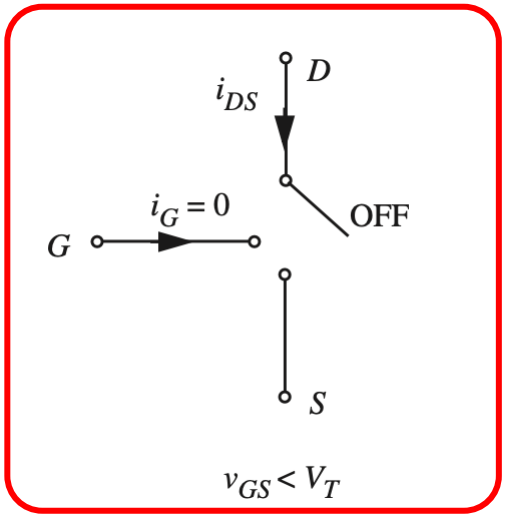


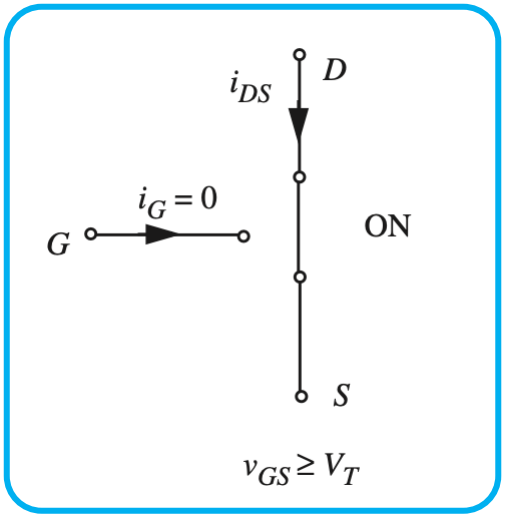


MOSFET S-Model

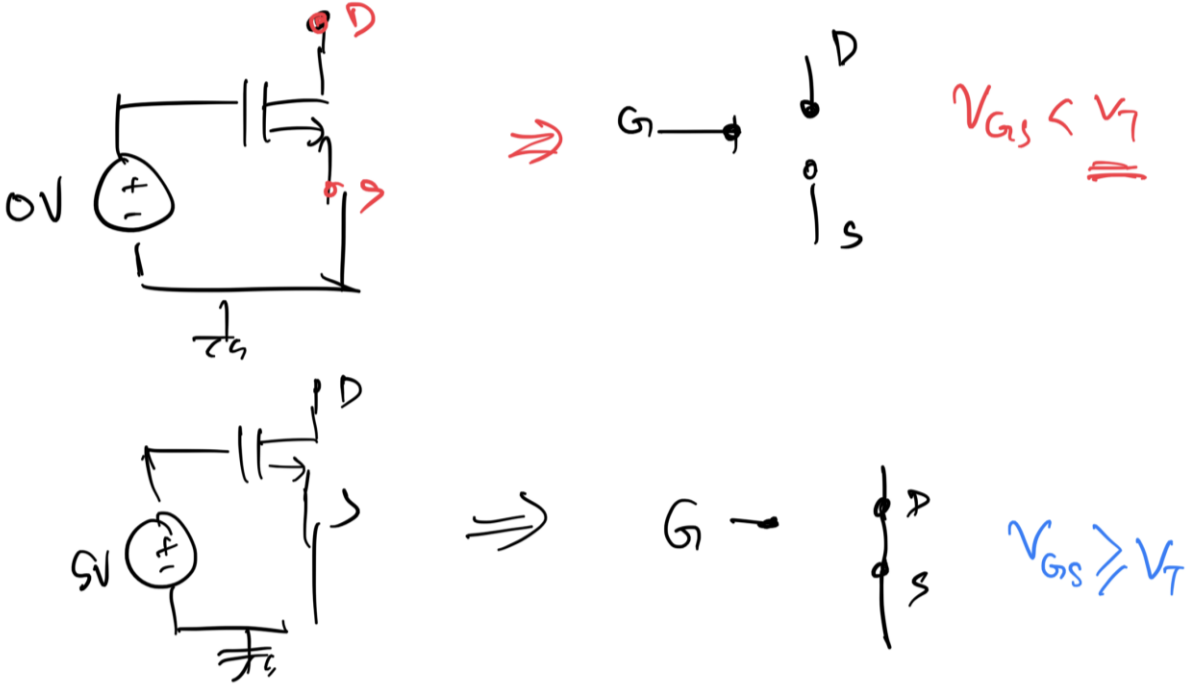
- The MOSFET (approximately) behaves like a switch
- $C = V_{GS}$. Here, $C = \text{“0”} \Rightarrow V_{GS} < V_T$, and $C = \text{“1”} \Rightarrow V_{GS} \geq V_T$



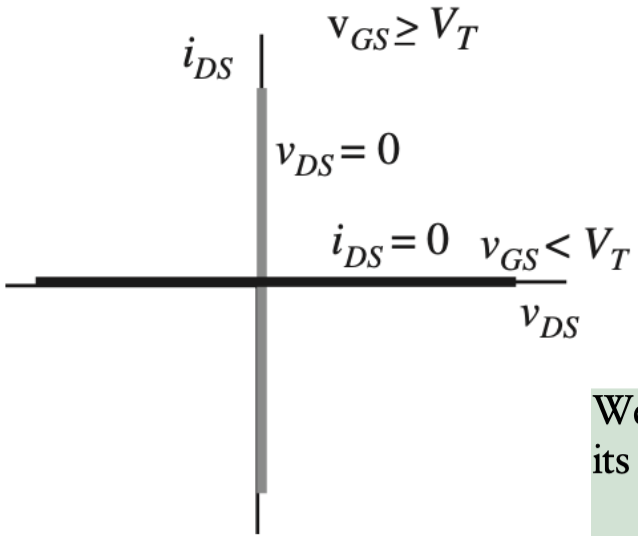




MOSFET S-Model



MOSFET S-Model



We can summarize the S model for the MOSFET in algebraic form by stating its v–i characteristics as follows:

$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

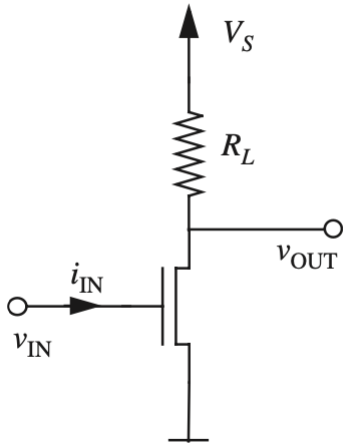
and

$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \qquad (6.2)$$

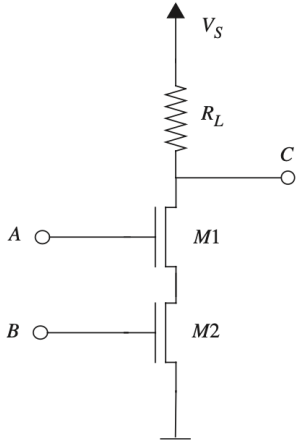
Ref: Agarwal, A. and Lang, J., 2005. *Foundations of analog and digital electronic circuits*. Elsevier.

Logic Gates using MOSFET

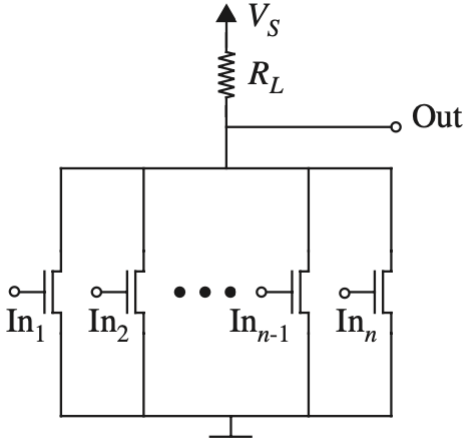
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

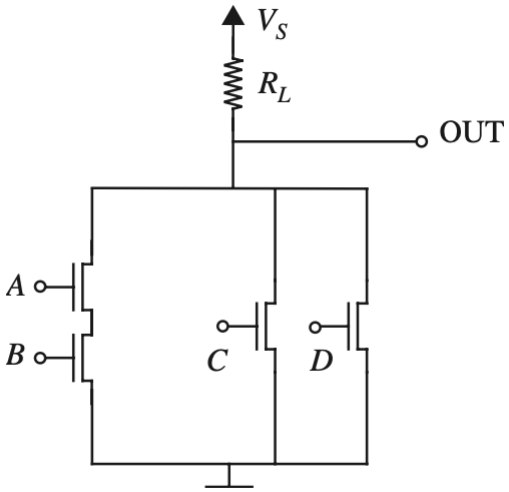


NAND Gate (Inverter)

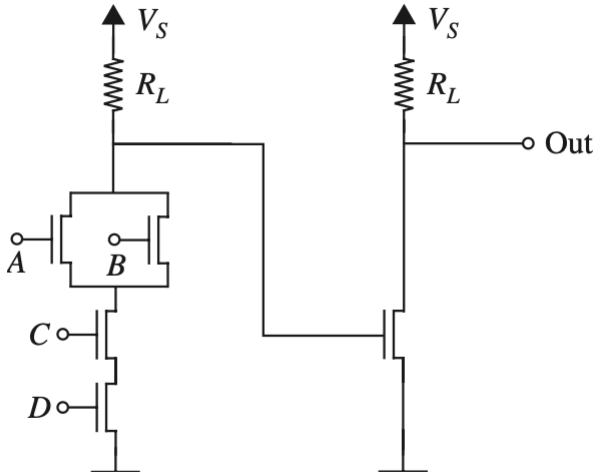


NOR Gate (Inverter)

MOSFET Logic Gates – More Examples



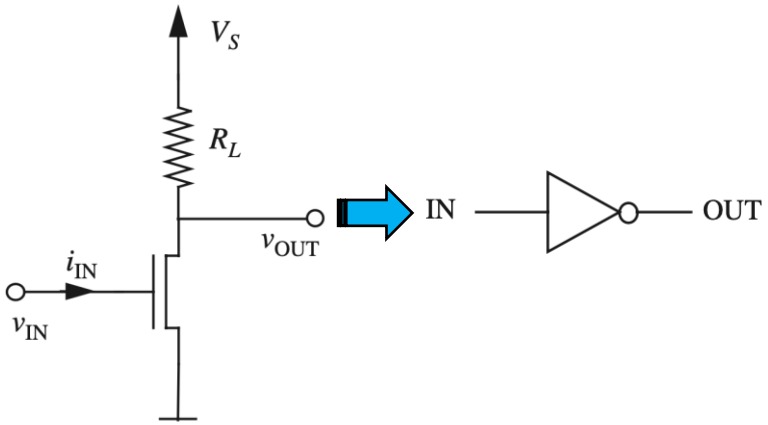
$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

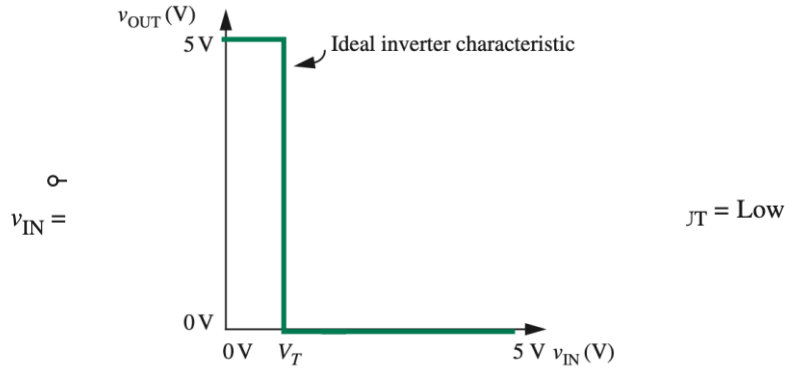
Voltage Transfer Characteristics (VTC)

- Reminder: VTC is a graph where x axis = input voltage, y axis = output voltate
- Why? Design logic gates to follow a given static discipline



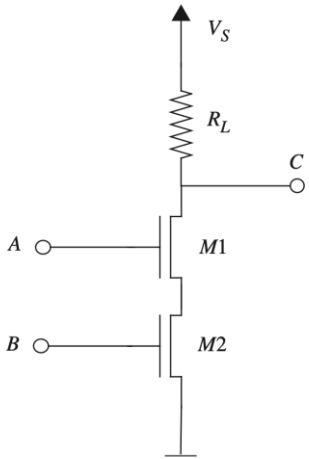
When $v_{IN} < V_T$ (Logical 0), $v_{OUT} = V_s = 5V$ (Logical 1)

When $v_{IN} \geq V_T$ (Logical 1), $v_{OUT} = 0$ (Logical 0)

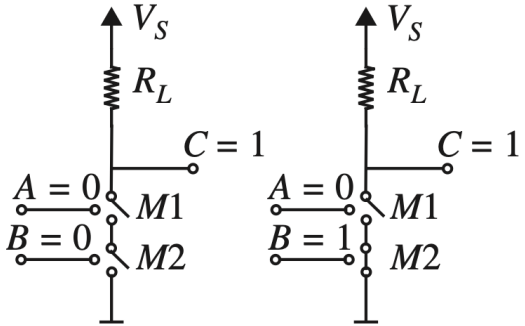


VTC of NAND gate

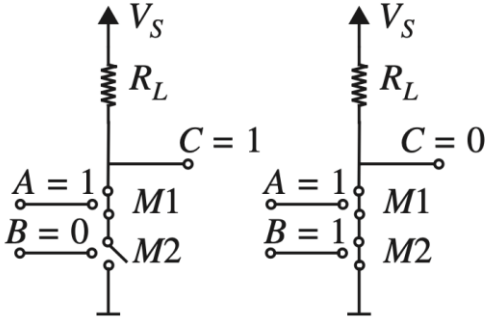
- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering $V_A = 0$, one considering $V_A = 1$



When $V_A = 0$



When $V_A = 1$



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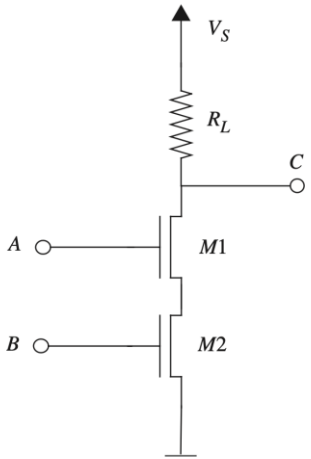
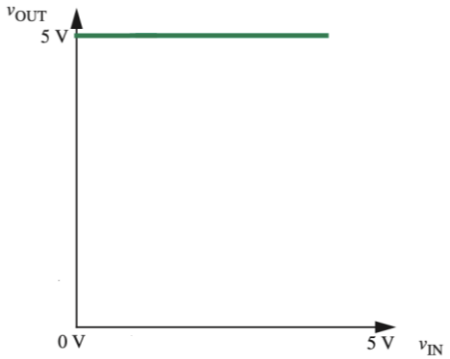
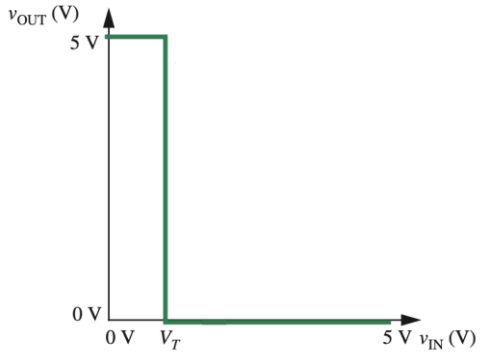
- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering $V_A = 0$, one considering $V_A = 1$



When $V_A = 0$

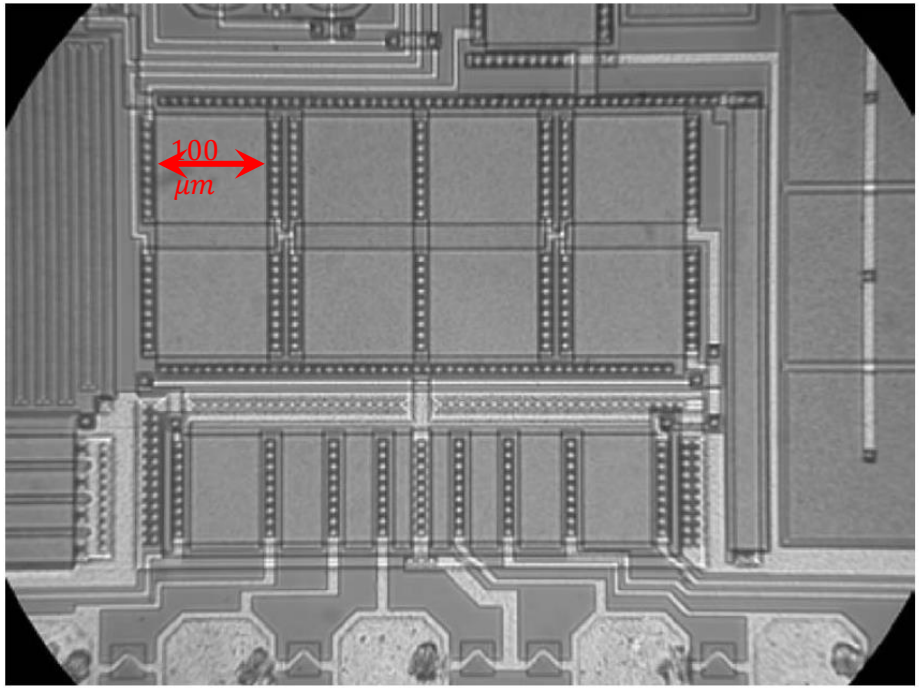


When $V_A = 1$



Homework: Find VTC for NOR gate

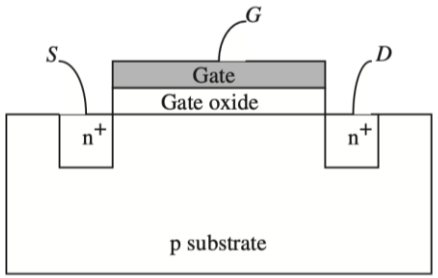
Construction of Real MOSFET

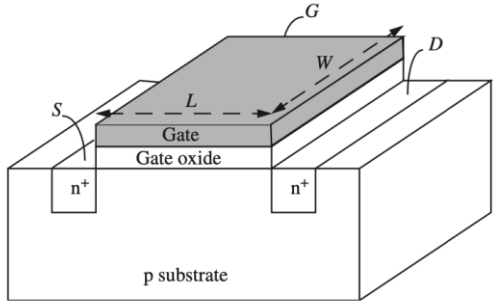


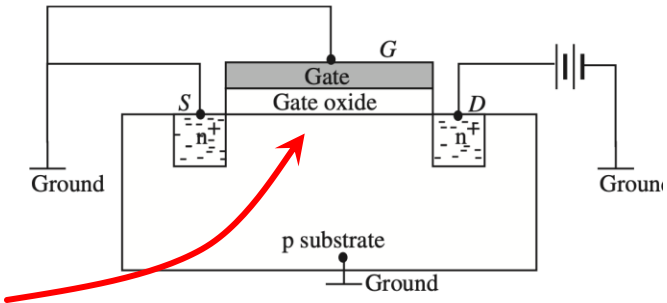
Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100 µm. (Photograph Courtesy of Maxim Integrated Products.)

Construction of Real MOSFET

Simplified cross section and 3D view

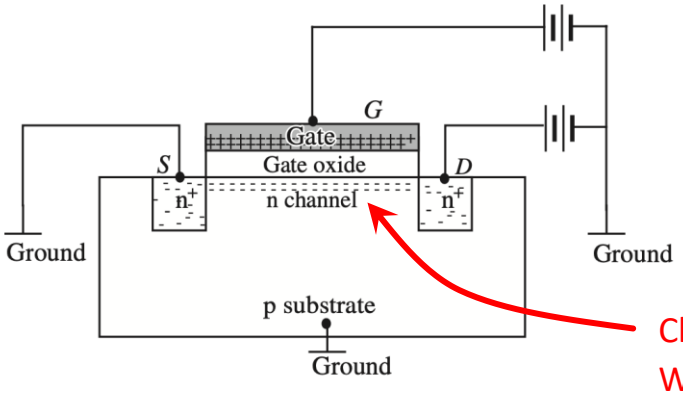






No channel, open ckt

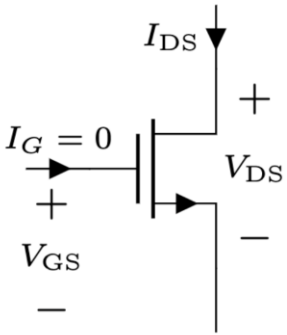
$V_{GS} = 0V$

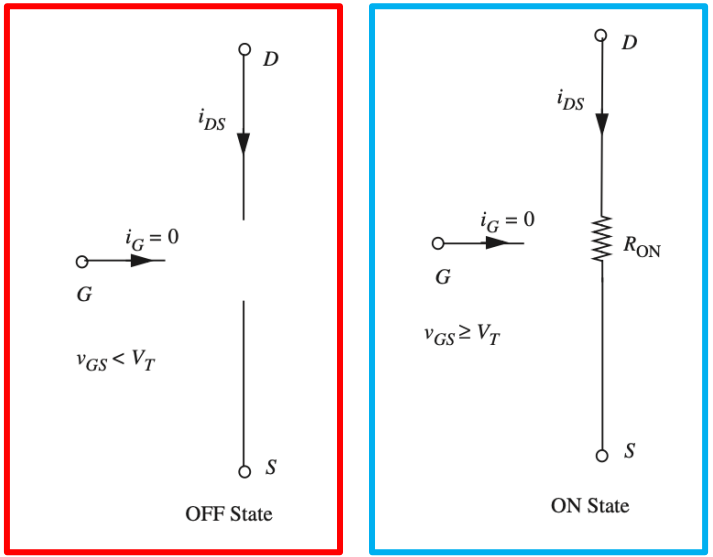


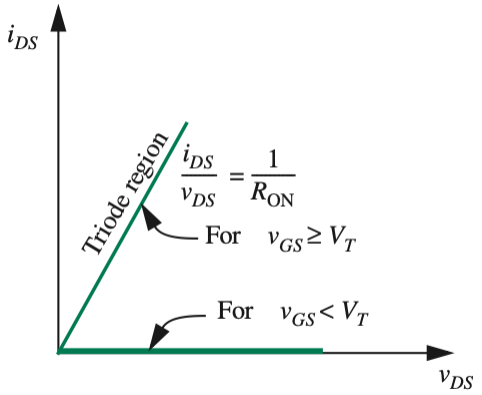
$V_{GS} > V_T$

Channel created
Will have some R
-> SR model

SR Model





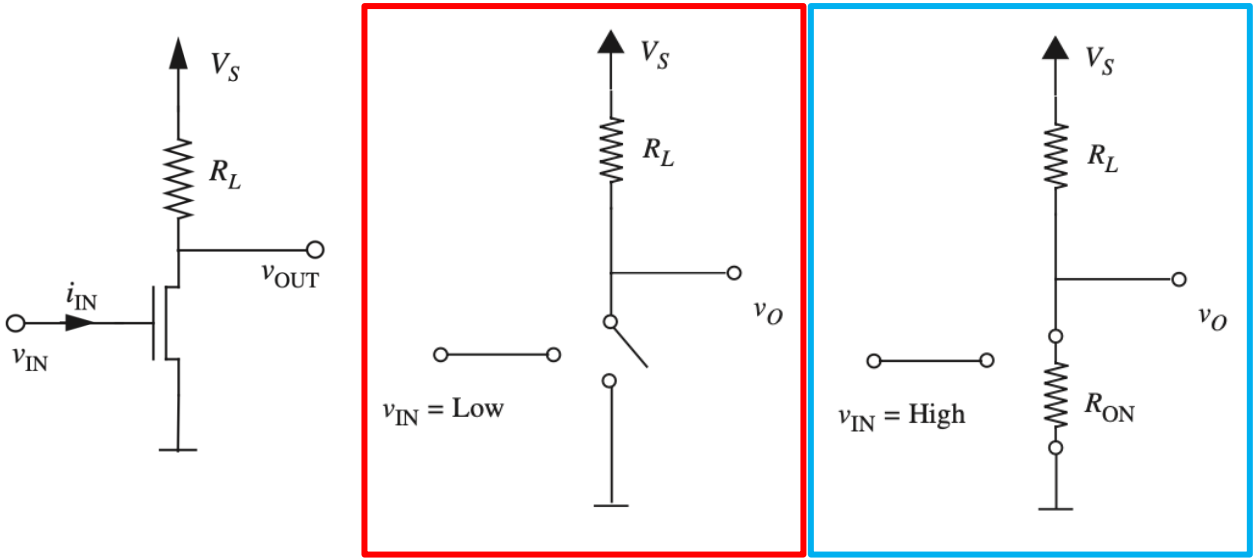


$$R_{ON} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_T)} = \frac{1}{kV_{OV}}$$

Unit of $k = mA/V^2$

- SR model is a better approximation than S model
- However, still an approximation. This model fails when V_{DS} increases to around $V_{GS} - V_T$

SR Model - Inverter

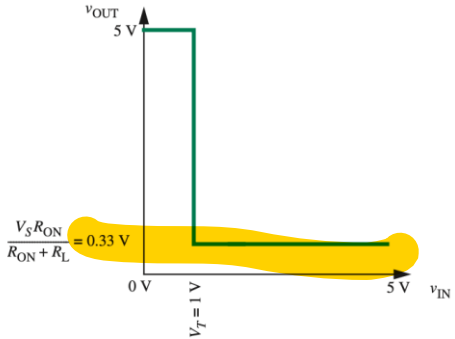


$v_{OUT,High} = V_S$

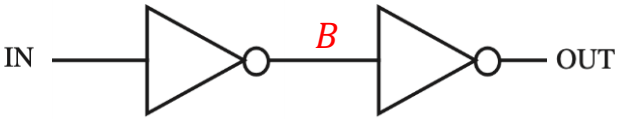
$v_{OUT,Low} = V_S \frac{R_{ON}}{R_{ON} + R_L} \neq 0$

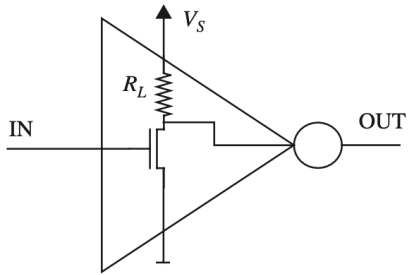
For example, if $V_S = 5V$, $R_{ON} = 1\ k\Omega, R_L = 14\ k\Omega$

$$V_S \frac{R_{ON}}{R_{ON} + R_L} = 0.33\ \text{V}.$$



Design of logic gates





Expected

IN	*B*	*OUT*
Low ($V_{IN} < V_T$)	High ($5V$)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} > V_T$)	Low ($V_{OUT,Low}$)	High (5V)

Actual

IN	*B*	*OUT*
Low ($V_{IN} < V_T$)	High ($5V$)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} > V_T$)	Low ($V_{OUT,Low} = 0.5\ V$)	Low ($V_{OUT} = V_{OUT,Low}$)

$V_T = 0.4\ V, V_S = 5V, R_{ON} = 1\ k\Omega, R_L = 9\ k\Omega$

$V_{OUT,High} = V_S = 5V$

$$V_{OUT,Low} = V_S \frac{R_{ON}}{R_{ON} + R_L} = 5 \frac{1}{1+9} = 0.5\ V$$

Therefore, need to design logic gates properly such that

$$V_S \frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}} + R_L} < V_T.$$

Design of logic gates - Example

Assume the following values for the inverter circuit parameters: $V_S = 5\,V, V_T = 1\,V,$ and $RL = 10\,k\Omega$. Assume, further, that $\frac{1}{k_n' V_{OV}} = 5$ for the MOSFET. Determine a $\frac{W}{L}$ sizing for the MOSFET so that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter.

Solution:

$$V_S \frac{R_{ON}}{R_{ON} + R_L} < V_T$$

$$\Rightarrow 5 \frac{R_{ON}}{R_{ON} + 10} < 1$$

$$\Rightarrow 5R_{ON} < R_{ON} + 10$$

$$\Rightarrow R_{ON} < \frac{10}{4} = 2.5$$

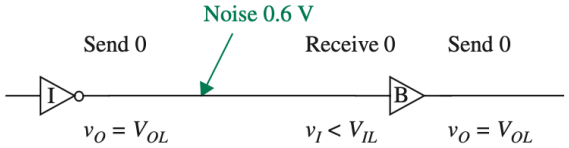
Now, $$R_{ON} = \frac{1}{k_n' \frac{W}{L} V_{OV}} = 5 \times \frac{1}{W/L}$$

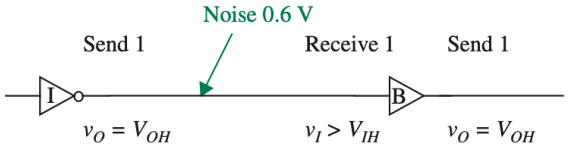
Hence $$\frac{5}{W/L} < 2.5 \Rightarrow \frac{W}{L} > \frac{5}{2.5}$$

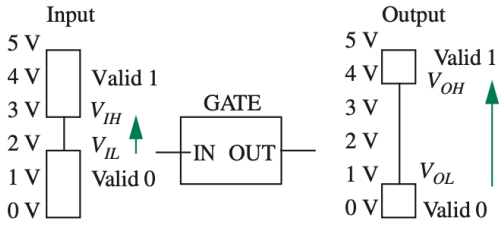
$$\Rightarrow \frac{W}{L} > 2$$

Static Analysis

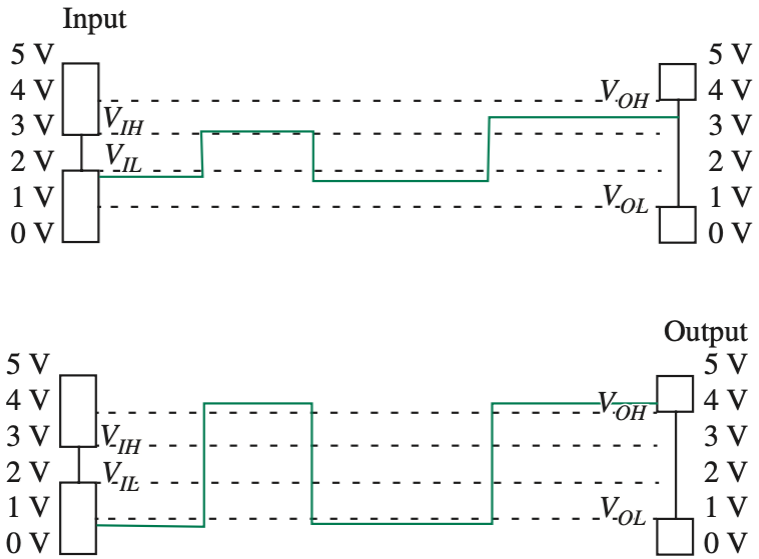
- General design principle – design in such a way that the device adheres to static discipline
- Valid input must produce valid output
- How to check? Analyze the voltage transfer characteristics.
- In short, the VTC should (1) provide |Gain| > 1 during transition (2) provide attenuation other time (3) be non-linear







Static Analysis and VTC – Gain



A non- inverting device such as a must convert an input low to high transition of the form $V_{IL} \rightarrow V_{IH}$ to an output low to high transition of the form V_{OL} (or lower) $\rightarrow V_{OH}$ (or higher)

$$V_{IL} > V_{OL}. \qquad \Delta v_I = V_{IH} - V_{IL}.$$

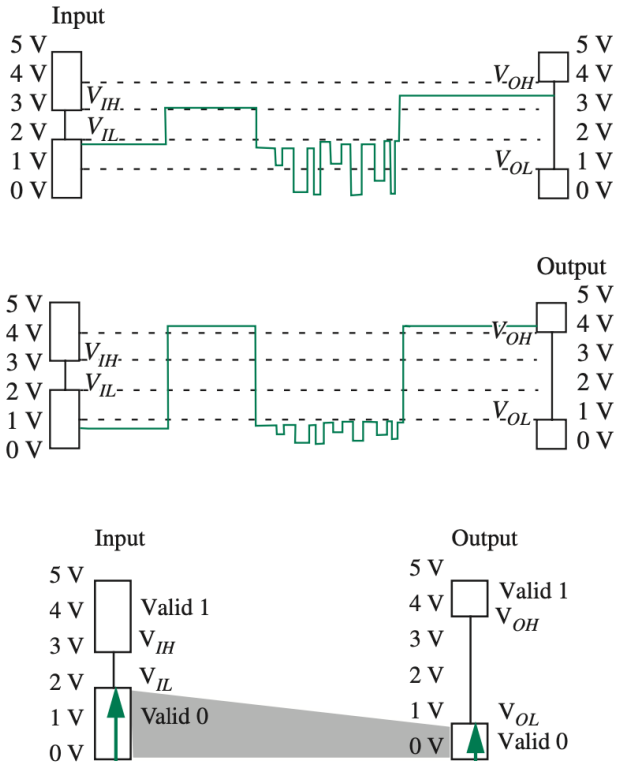
$$V_{OH} > V_{IH}. \qquad \Delta v_O = V_{OH} - V_{OL}.$$

$$\text{Gain} = \frac{\Delta v_O}{\Delta v_I} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}.$$

$$V_{OH} - V_{OL} > V_{IH} - V_{IL}.$$

$$\text{Gain} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} > 1.$$

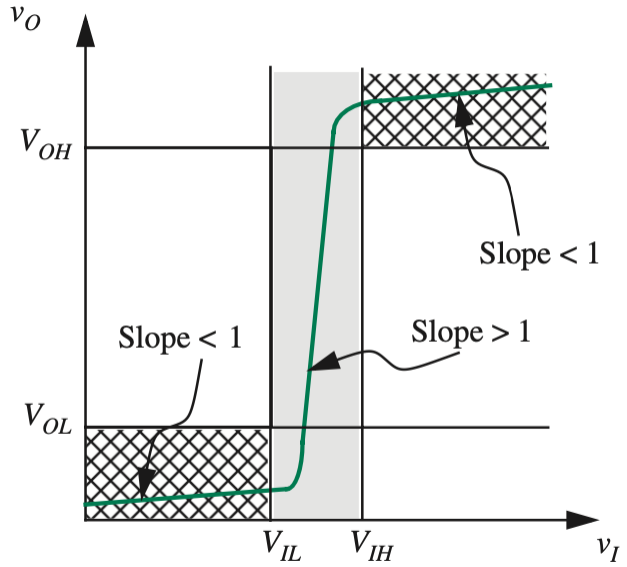
Static Analysis and VTC – Attenuation



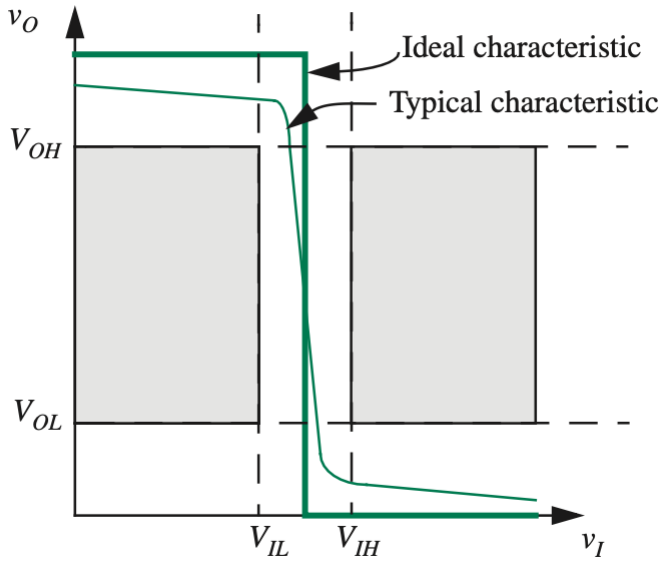
$$\frac{V_{OL} - 0}{V_{IL} - 0} = \frac{V_{OL}}{V_{IL}} < 1.$$

$$\frac{5 - V_{OH}}{5 - V_{IH}} < 1.$$

Static Discipline and VTC



Buffer VTC that follows static discipline



Inverter VTC that follows static discipline

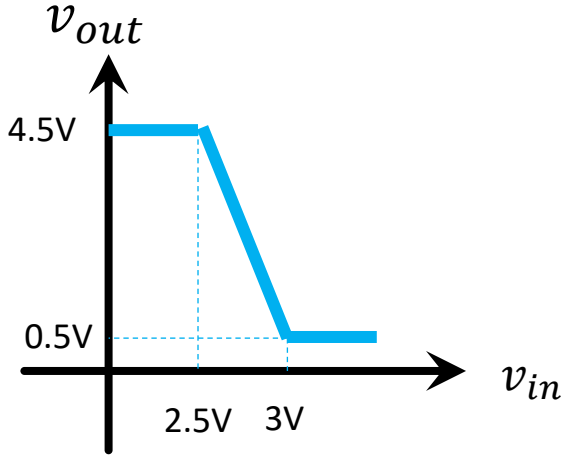
Static Discipline and VTC - Example

The device company **Yehaa Microelectronics, Inc.** has developed a new process technology that is able to produce large quantities of a certain type **inverter** at a very low cost. Their inverters has a VTC as given below. Yehaa's sales team discovers that networking equipment company **Disco Systems Inc.** buys huge quantities of inverters from a competitor Yikes Devices, Inc. Upon further research, the Yehaa sales team finds that the hardware systems in one of Disco's product lines operate under a static discipline with the following voltage thresholds

$V_{IL} = 2V, V_{IH} = 3.5V, V_{OL} = 1.5\ V, \text{and}\ V_{OH} = 4V.$

Yehaa's sales team wishes to sell their inverters to Disco at a lower cost than those from Yikes, but first, Yehaa must determine whether their inverters can safely replace the inverters from Yikes. The sales team asks their development engineers to determine whether Yehaa's adders satisfy the static discipline under which Disco's system operates.

Help the Sales team make the decision



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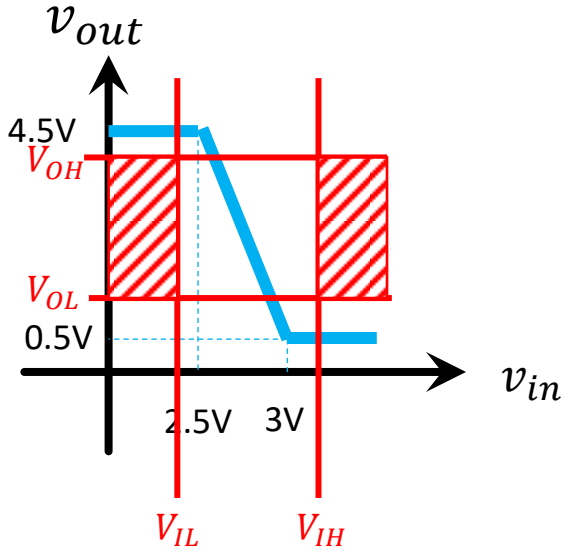
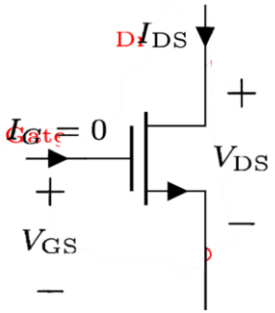
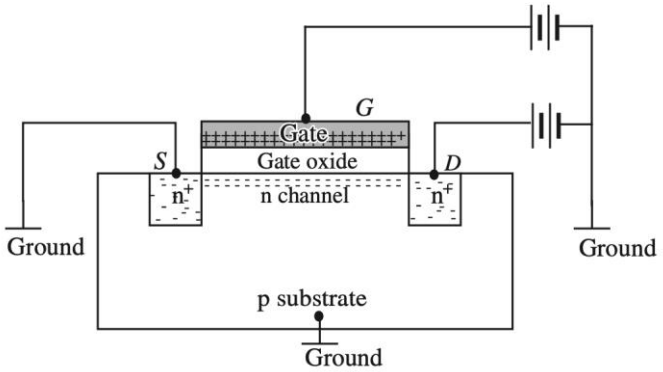


1. Avoids forbidden region
2. |Gain| > 1

Hence, satisfies static discipline

Lecture 15: Method of Assumed State





Control = $V_{GS} = V_G - V_S$, controls the IV between drain-source (I_{DS} vs V_{DS})

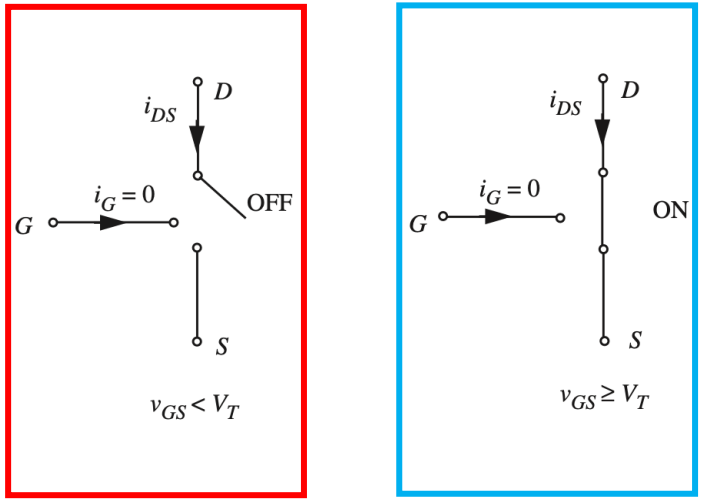
Threshold voltage = V_T, minimum voltage required to create the channel

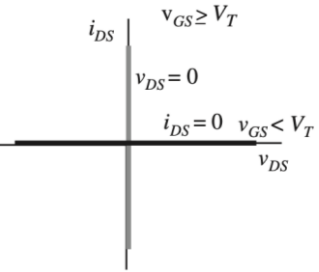
Models

1. **S Mode**: Assumes an ideal channel with zero resistance
2. **SR Model**: Assumes finite channel resistance, R_{ON}, depends on $V_{GS} - V_T = V_{OV}$

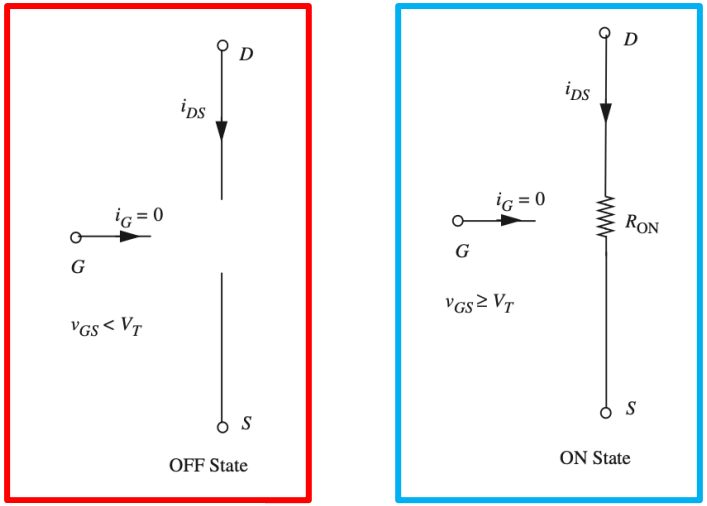
MOSFET Linear Models

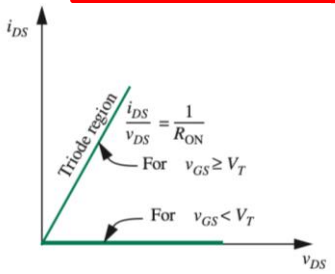
S Model





SR Model

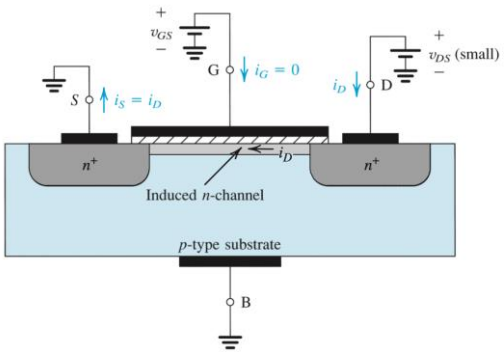


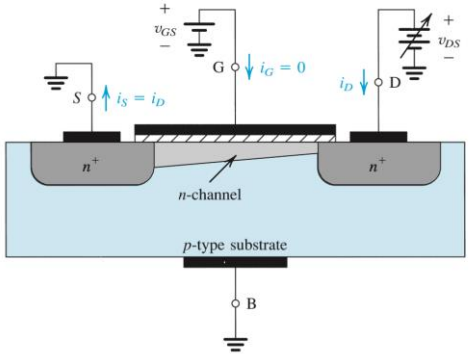


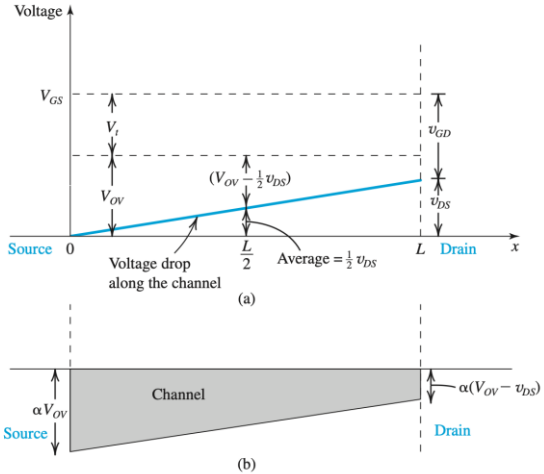
$$R_{ON} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_T)} = \frac{1}{kV_{OV}}$$

Real MOSFET

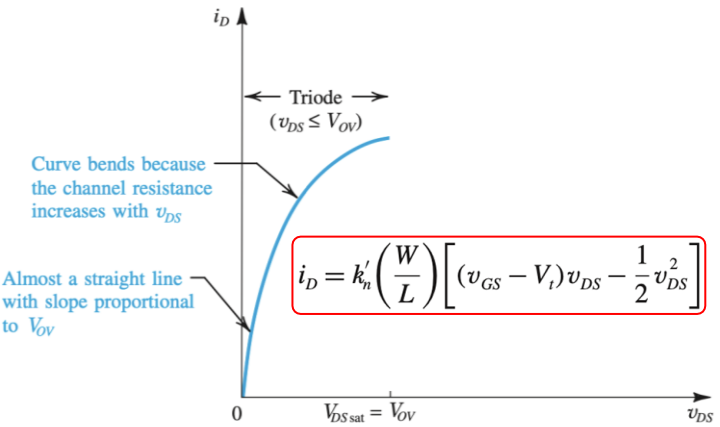
- Why $R_{ON} = \frac{1}{k_n' \frac{W}{L}(V_{GS}-V_T)} = \frac{1}{kV_{OV}}$? Because channel width $\propto V_{OV}$, and $R \propto \frac{1}{\text{width}}$
- For small V_{DS}, uniform channel, hence fixed R_{ON}, therefore SR model valid.
- As V_{DS} is increased, channel becomes tapered cause V_{GD} ↓. Resistance ↑, slope ↓.
- This mode is called the **triode mode**. Condition: $V_{DS} < V_{OV}$

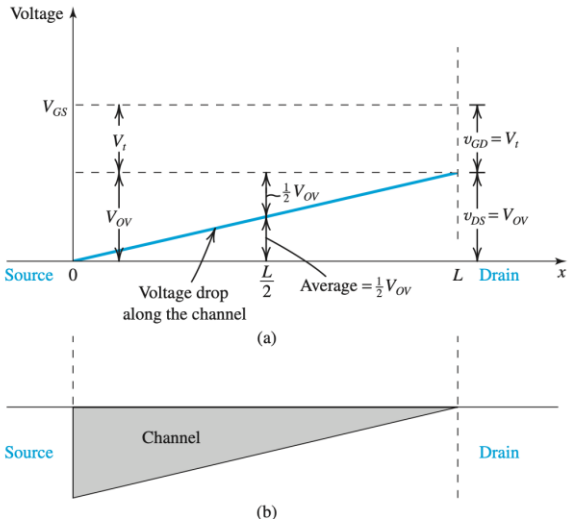


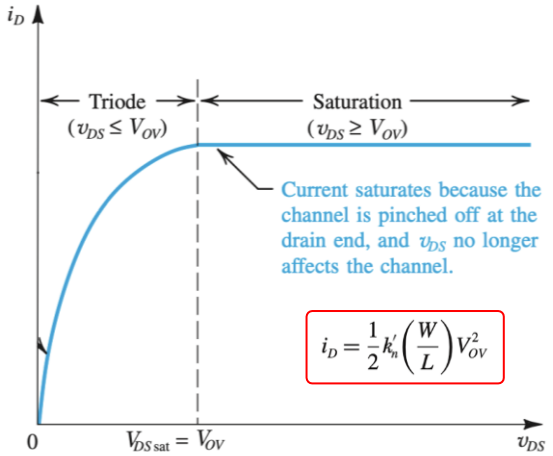




Real MOSFET

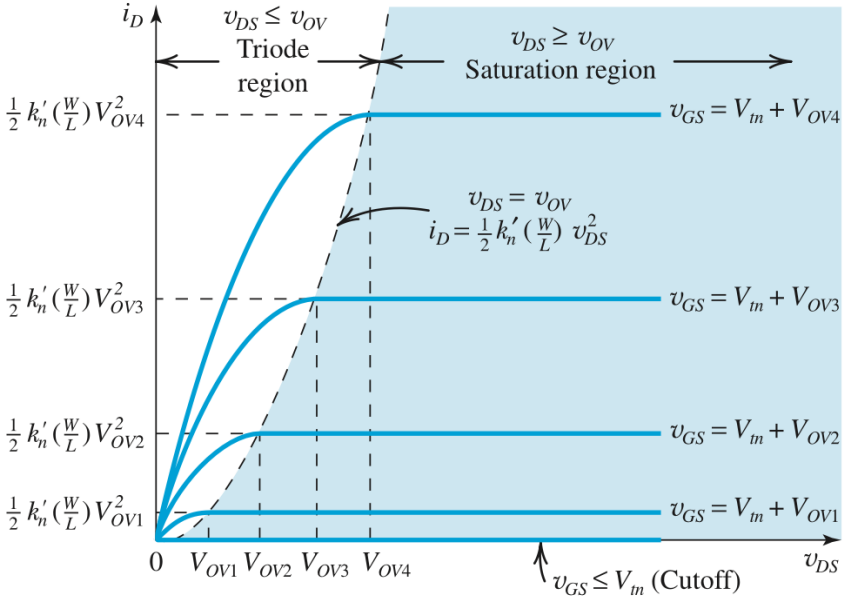






- When $V_{DS} = V_{OV}$, channel pinches off.
- Increasing V_{DS} further have no effect on channel shape. Hence, current <u>saturates</u>
- This mode is called the **saturation mode**. Condition: $V_{DS} \geq V_{OV}$
- Behaves like a **<u>current source</u>** (constant current) that depends on V_{OV}

IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \ge V_T$ $V_{DS} < V_{OV}$	$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$
Saturation	$V_{GS} \ge V_T$ $V_{DS} \ge V_{OV}$	$I_D = \frac{k}{2}V_{OV}^2$

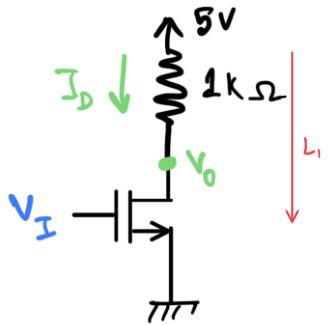
$$V_{OV} = V_{GS} - V_T$$

$$k = k_n'\left(\frac{W}{L}\right)$$

Solving Circuits with MOSFET

- Use **Method of Assumed State**!
- Three steps:
  - **Assume**: One of the modes (Cutoff, Triode, Saturation)
  - **Solve**: Use corresponding equation and KCL+KVL
  - **Verify**: Check if the conditions of V_{GS} and V_{DS} are satisfied. If not, repeat.
- Might need to solve quadratic equation $(ax^2 + bx + c = 0)$.
- If we get two roots, choose the one that's *favorable* to your assumption

Example 1



The MOSFET is specified as $V_T = 1V$ and $k = 0.5\ mA/V^2$. Find I_D and V_O for $V_I = 2V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2}V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 2V$

Therefore, $V_{OV} = V_{GS} - V_T = 2 - 1 = 1V$

$$\therefore I_D = \frac{0.5}{2}(1)^2 = 0.25\ mA$$

Again, $V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$

KVL along L_1: $I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_0 = 5 - I_D \times 1k\Omega$

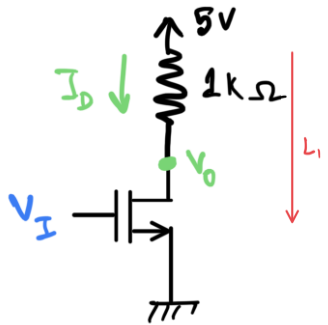
$$\Rightarrow V_o = 5 - 0.25 \times 1 = 4.75\ V = V_{DS}$$

Step 3: $V_{GS} = 2V > V_T$ √ Therefore, **assumption correct**!

$V_{DS} = 1V > V_{OV}$ √

Correct ans: $I_D = 0.25\ mA, V_o = 4.75\ V$

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5\ mA/V^2$. Find I_D and V_O for $V_I = 5V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2}V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$

Therefore, $V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$

$$\therefore I_D = \frac{0.5}{2}(4)^2 = 4\ mA$$

Again, $V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$

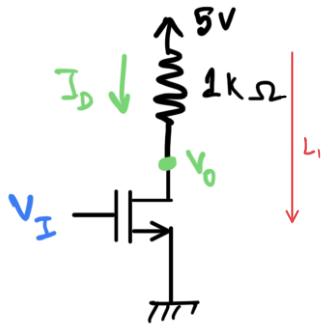
KVL along L_1: $I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_0 = 5 - I_D \times 1k\Omega$

$$\Rightarrow V_o = 5 - 4 \times 1 = 1\ V = V_{DS}$$

Step 3: $V_{GS} = 5V > V_T$ √ Therefore, **assumption wrong**!

$V_{DS} = 1V \not> V_{OV}$ ×

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5\ mA/V^2$. Find I_D and V_O for $V_I = 5V$.

Repeat:

Step 1: Assume the MOSFET in **triode**

Step 2: $I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$

Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$

Therefore, $V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$

Again, $V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$. Assuming $V_{DS} = x$

KVL along L_1: $I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow I_D = \frac{5 - V_{DS}}{1} = 5 - x$

$$\therefore I_D = 0.5\left[4 \times V_{DS} - \frac{1}{2}V_{DS}^2\right] \Rightarrow (5 - x) = 0.5\left[4x - \frac{1}{2}x^2\right]$$

$$\Rightarrow 5 - x = 2x - 0.25x^2 \Rightarrow 0.25x^2 - 3x + 5 = 0$$

Solving, $x = 2V, x = 10V$

Since $V_{DS} = x$ is small in triode, smaller value of x is favorable

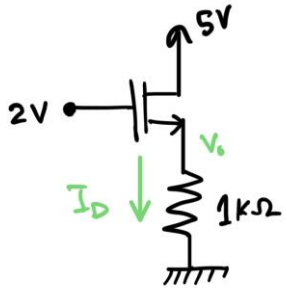
Therfore, $V_o = V_{DS} = x = 2V$, and $I_D = 5 - x = 3\ mA$

Step 3: $V_{GS} = 5V > V_T$ √ Therefore, **assumption correct**!

$V_{DS} = 2V < V_{OV}$ √

Correct ans: $I_D = 3\ mA, V_o = 2\ V$

Example 3



The MOSFET is specified as $V_T = 1V$ and $k = 4\ mA/V^2$.
Find I_D and V_O

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2} V_{ov}^2$

Let's assume $V_0 = V_S = x$

Here, $V_{GS} = V_G - V_S = V_G - V_o = 2 - x$

Therefore, $V_{OV} = V_{GS} - V_T = (2 - x) - 1 = 1 - x$

Again, $V_{DS} = V_D - V_S = V_D - V_0 = 5 - x$

Ohm's law for the resistor: $I_D = \frac{V_0 - 0}{1k\Omega} = x$

$\therefore x = \frac{4}{2}(1 - x)^2 \Rightarrow x = 2(1 - 2x + x^2) \Rightarrow x = 2 - 4x + 2x^2$

$\Rightarrow 2x^2 - 5x + 2 = 0$

Solving, $x = 0.5, \cancel{x = 2V}$

Since $V_{DS} = 5 - x$ is large in saturation, smaller value of x is favorable

$\therefore V_o = V_S = x = 0.5V, I_D = x = 0.5\ mA,$
$V_{DS} = 5 - x = 4.5V, V_{GS} = 2 - x = 1.5V,$ and $V_{OV} = 1 - x = 0.5V$

Step 3: $V_{GS} = 1.5V > V_T$ √ Therefore, **assumption correct**!

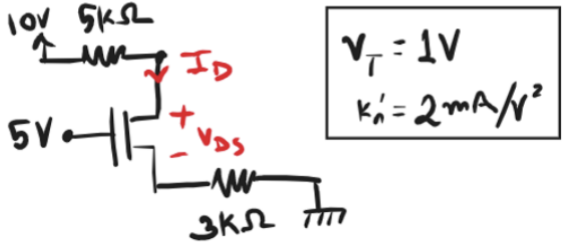
$V_{DS} = 4.5V > V_{OV}$ √

Correct ans: $I_D = 0.5\ mA, V_o = 0.5\ V$

Practice

Question 4 [CO1, CO4] **10**

Analyze the following circuit to find the values of I_D and V_{DS} **using** the Method of Assumed State. You must **validate** your assumptions. [7 + 3]
Hint: Use I_D as unknown x. Use Ohm's law to represent V_D and V_S in terms of x.



Hint Explanation

Assume $I_D = x$. For $5k\Omega$: $I_D = \frac{10-V_D}{5} \Rightarrow V_D = 10 - 5 \times I_D = 10 - 5x$.

For $3k\Omega$: $I_D = \frac{V_S-0}{3} \Rightarrow V_S = 3 \times I_D = 3x$.

Therefore, $V_{GS} = V_G - V_S = 5 - 3x$, and $V_{OV} = V_{GS} - V_T = (5 - 3x) - 1$

Also, $V_{DS} = V_D - V_S = (10 - 5x) - 3x = 10 - 8x$

Now if you assume saturation:

$$I_D = \frac{k}{2}V_{OV}^2 \Rightarrow x = \frac{2}{2}(4 - 3x)^2$$

And if you assume triode:

$$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\Rightarrow x = 2[(4 - 3x)(10 - 8x) - 0.5 \times (10 - 8x)^2]$$

Solve for x, take the _____ root