MIDTERM EXAM

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FALL 23

Ans to Q 1 (A)

Physical address = DS × 10 + 2000

= 10000 + 2000

= 12000h

Ans to Q 1 (B)

smallest seg num:

12000 - FFFF = 02001h

Rounding up = 02010 h

∴ smallest segment number = 0201 h

0201

Now, offset for this, is 1 (A)

① 12000 = 0201 × 10 + offset

offset = FFF0 h

∴ logical add = 0201 : FFF0

Ans to Q1 (c)

Physical add = 12000h

① 12000 = 1200 × 10 + offset

⇒ offset = 0000H

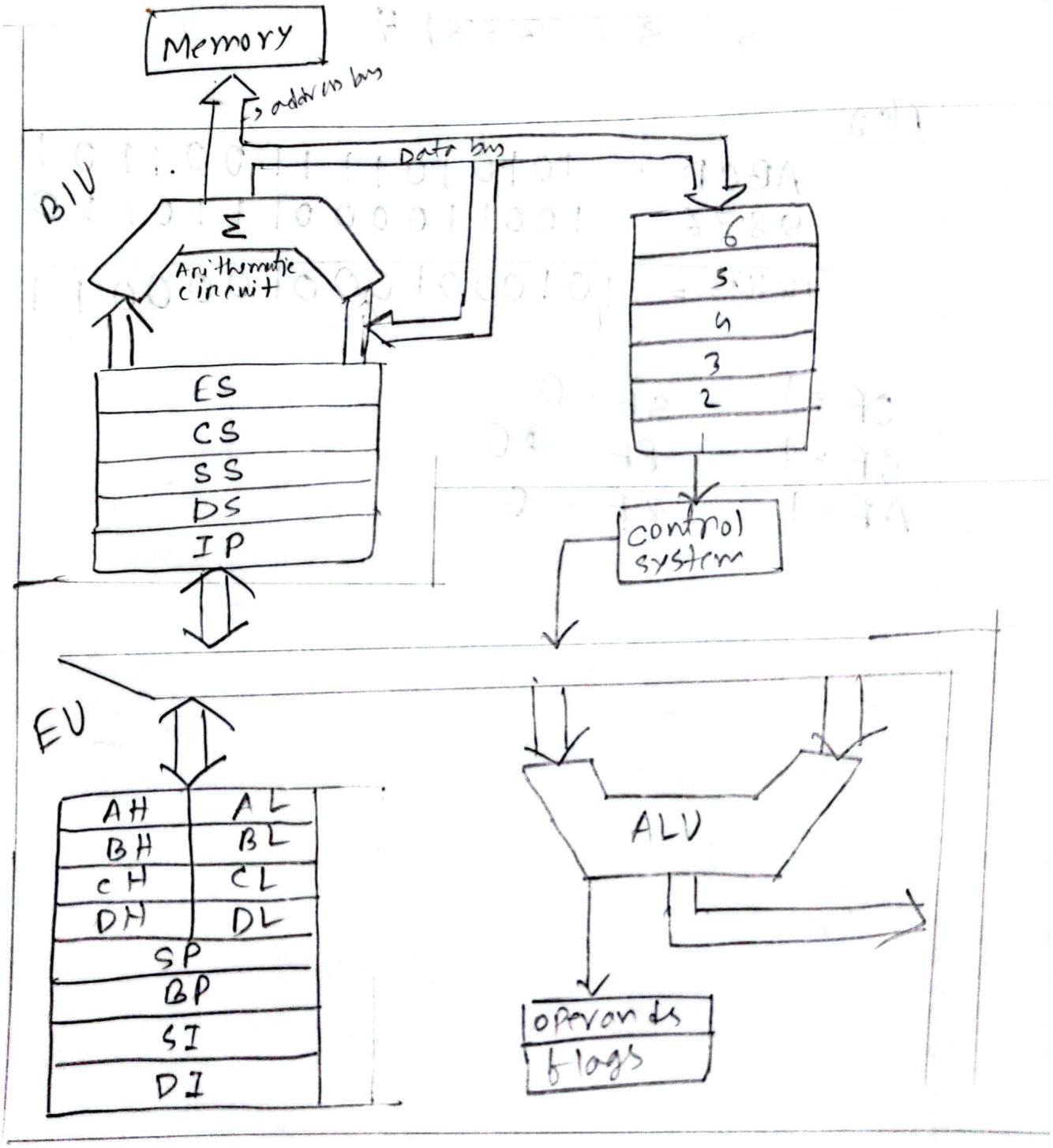
Logical add: **1200 : 0000H**

② 12000 = 1100 × 10 + offset

offset = 1000

Logical add = **1100 : 1000H**

Ans to Q 2 (A)


Memory
address bus
Data bus
BIU
Σ
Arithmetic circuit
ES
CS
SS
DS
IP
6
5
4
3
2
control system
EU
AH
AL
BH
BL
CH
CL
DH
DL
SP
BP
SI
DI
ALU
operands
flags

Ans to or 2(B)

Differences between microprocessor and microcontroller :

Microprocessor	Microcontroller
1. It requires intensive procesing and has changable programme	1. It has predefined task and unchable programme.
2. RAM used is higher and clock speed is higher too.	2. RAM used is lower and clock speed lower too
3. High power consumption needed and high cost.	3. Low power consumption and low cost.

Ans to or no 2(C)

Pipelining fails when there's a brancing problem. for example if there is a condition check, it might just be not true, pipelining still fetches instruction

Again, when ② certain operations are data dependent. Of result of one instruction is needed for another. Then piplining fails.

Ans to Q 3(A)

MOV AX, 2FXY h

MOV BX, FCDF h

```
2FXY ⇒ 0010 1111 0001 1111
FCDF ⇒ 1111 1100 1101 1111
       ---------------------
       1011 0101 1110 1110
```

Min value of X = 0001 = 1H

Max val of Y = 1111 = FH

Ans to Q 3 (B)

① OF = 0 ; since MSB has carry
15th bit also has carry

② AF = 1 , Lower nibble has carry 1

③ SF = 0 , since 16th bit is 0

Ans to 3 (c)

① NMI (Non maskable interrupt) will be active as it cannot be stoppable.
Hence **NMI = 1**

② Since maskable interrupt can be stopped, ($\overline{INTA}$=1) acknowledgement will not send that interrupt accepted so ($\overline{INTA}$ = 1) **INTR = 0** will be set as it will be stopped.

Ans to 4 (a)

1. MOV CL [BX] ⇒ Register indirect

Because the address is stored in register then used as addressing indirectly

2. MOV CL, [BX+SI]

⇒ Base plus index

Since the base register and index register pointing to an offset is used.

3. RET [1234h] ⇒ Invalid

4. MOV AX, [BP] ⇒ Register relative

As BP as base register is a index register.

Ans to 4(B)

MOV DI, [BP+42h]

byte 1:

100010	1	1
opcode	D	W

byte 2:

01	111	110
MOD	REG	R/M

byte 3:

01000010

Hex: 8B7E42 H