Assignment 4



BRAC University

Semester: Fall 2022 Course No: CSE251

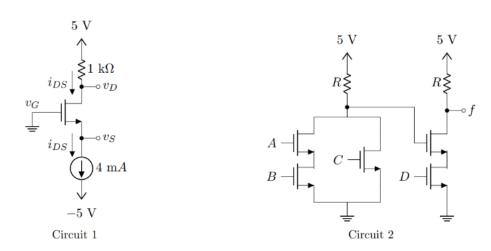
Course Title: Electronic Devices and Circuits

Full Marks: 10×4×2.5=100 [Bonus: 15]

Deadline: 15 December 2022

Note: The formulas for a MOSFET are given in Ques 2.

1.



Part a: Refer to the Circuit 1 above. For the MOSFET, $V_T=1~{\rm V}$ and $k=k_n'\frac{W}{L}=4~{\rm m}A/V^2$.

(a) **Identify** the value of the gate voltage v_G and the drain-source current i_{DS} . [0.5+0.5]

(b) Calculate the value of the drain voltage v_D using the 1 k Ω resistor. [1]

(c) Analyze the circuit to find v_S . Here, use the Method of Assumed State. You must validate your assumptions. [Hint: assume $v_S = x$] [3+2]

Part b: Analyze the Circuit 2 above to find f in terms of boolean inputs A, B, C, and D. [3]

Analyze the following circuit to find the values of I_D and V_{DS} using the Method of Assumed State. You must validate your assumptions.

Hint: Use I_D as unknown x. Use Ohm's law to represent V_D and V_S in terms of x.

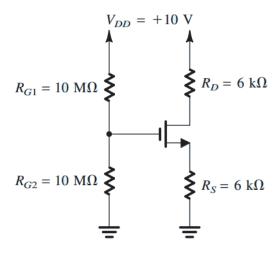
For MOSFET

$$I_{D} = 0, \text{ if } V_{GS} < V_{T}$$

$$I_{D} = k \left[(V_{GS} - V_{T}) V_{DS} - \frac{1}{2} V_{DS}^{2} \right], \text{ if } V_{GS} \ge V_{T} \text{ and } V_{DS} < (V_{GS} - V_{T})$$

$$I_{D} = \frac{1}{2} k (V_{GS} - V_{T})^{2}, \text{ if } V_{GS} \ge V_{T} \text{ and } V_{DS} \ge (V_{GS} - V_{T})$$

- 3. Consider an NMOS transistor fabricated with L = 0.18 μ m and W = 2 μ m. The process technology is specified to have K_n '=387 μ A/V², and V_t = 0.5 V. Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of the saturation region with I_{DS} = 150 μ A.
- **4. Analyze** the circuit shown in the following Figure to determine the voltages at all nodes and the currents through all branches. Let $V_T = 1 \text{ V}$ and $k_n'(W/L) = 1 \text{ mA/V}^2$. **[10]** [Hints: current at the gate terminal is zero for a MOSFET].



BONUS: An NMOS transistor is operating at the edge of saturation with an overdrive voltage V_{OV} and a drain current I_D . If V_{OV} is doubled, and we must maintain operation at the edge of saturation, what should V_{DS} be changed to? **Find** the value of drain current results. Does changing V_{OV} change the process parameter k? [0.5+3+1.5]

1.

b)
$$V_0 = 5 - 4i_{0s} = 5 - 4 \times 1 = 5 - 4 = 1 \vee$$

Let, ... saturation $|DS| = \frac{1}{2} \times (V_{GIS} - V_T)^T$

$$i_{DS} = \frac{1}{2} \times \left(\sqrt{G_{1S}} - \sqrt{T} \right)^{2}$$

$$\Rightarrow 4 = \frac{1}{2} \times 4 \times \left(V_{GIS} - 1 \right)^2$$

$$\Rightarrow (V_{GIS} - 1)^2 = 2 \quad \text{of } V_{OV} = 1.414V$$

Herce, VDS = 1+2.414=3.414 > VOV 0% assumption is correct.

f = AB+CD

Here, For
$$5kL$$
, $I_D = \frac{10 - VD}{5}$ $\frac{1}{5}$ $\frac{1}{$

So. Vors = Vor - Vs = 5-34 Vov = Vas - VT = 5-3x-1=4-3x VDS = VD - Vs = (10-5x) - 3x = 10-8x

loto. arrume this is in roturation region.

$$I_{D} = \frac{k}{2} \sqrt{2}$$

We have to take the smaller re.

... The assumption is convect. This is in naturation rigion. (Am) and the transistor transconductance parameter k_n ,

$$k_n = k'_n \left(\frac{W}{L}\right)$$
$$= 387 \left(\frac{2}{0.18}\right) = 4.3 \text{ mA/V}^2$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two $10\text{-}M\Omega$ resistors,

$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA)×6 (k Ω) = $6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus, I_D is given by

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2$$

= $\frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$

which results in the following quadratic equation in I_D :

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D : 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

 $V_S = 0.5 \times 6 = +3 \text{ V}$
 $V_{GS} = 5 - 3 = 2 \text{ V}$
 $V_D = 10 - 6 \times 0.5 = +7 \text{ V}$

Since $V_D > V_G - V_{tn}$, the transistor is operating in saturation, as initially assumed.

BONUS:

B Bonus:

at the edge of roturation region,

if vor in doubled, VDS = 2 Vor

There, VDS (new) = 2 You = 2 2

·· Vos (new) = 2 · Vov (als)

now In the saturation region.

IDS (new) = K [2 Vov] 2 K [Vov] 2

Ips (new) = 4 you - Vov 2

:. IDS (new) = 4 IDS (ald)

And changing Vor does not change the process parameter K. (Am.)