CSE260 LAB REPORT 5

Experiment Name : Design and Implementation of 4 bit parallel binary adder cum subtractor.

submitted by

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Experiment Name : Design and Implement-ation of 4-bit parallel Binary Adder cum subtractor

2. Objective : Implementation of addition and subtraction by using IC - 74283 and XOR Gate.

3. Required components and Equipments :

i) LOGICSTATE (Input)

ii) LED - GREEN (output)

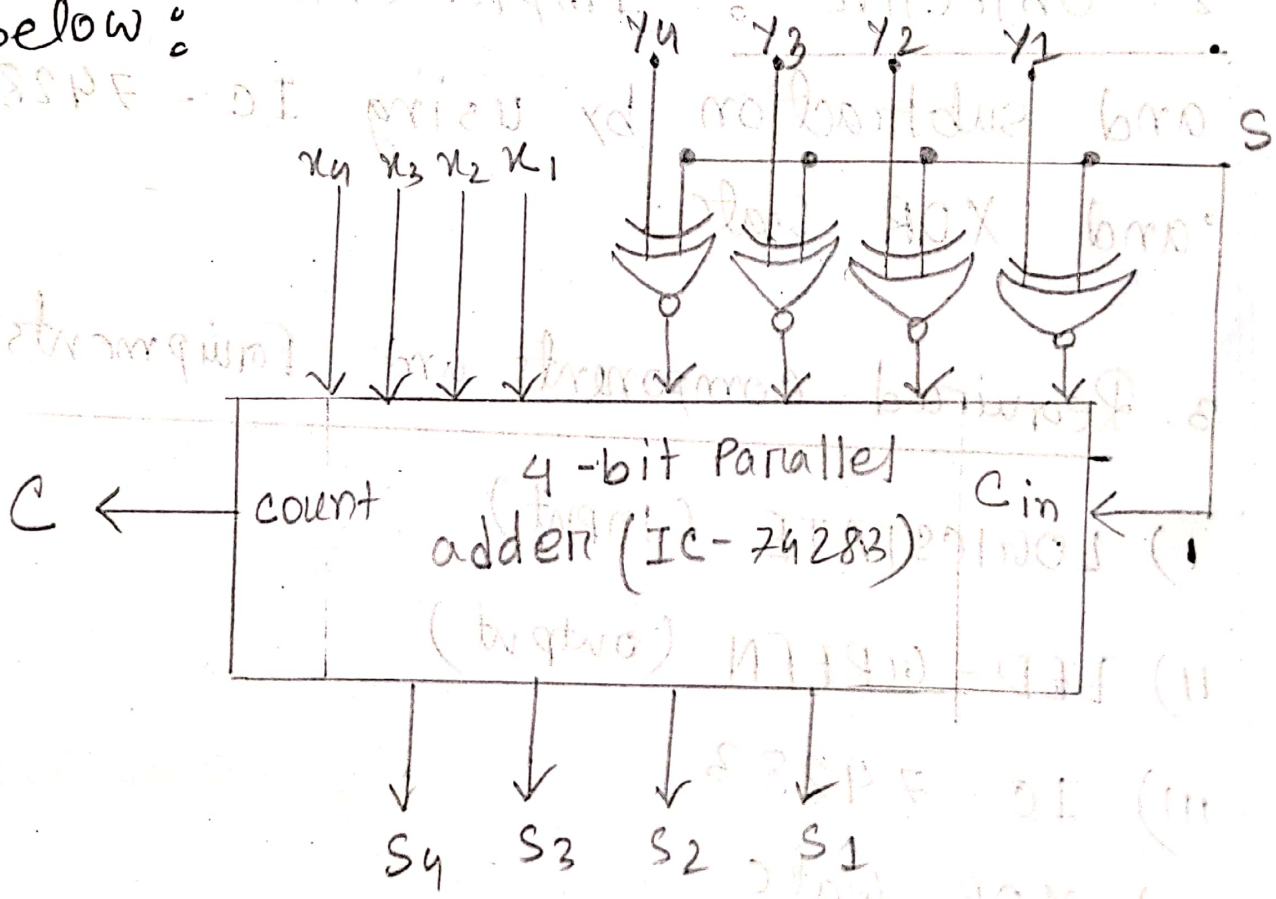
iii) IC - 74283

iv) XOR Gate

v) Ground

4. Experimental setup :

The circuit diagram of a 4 bit full addar cum subtractor is given below :



5. Results (Truth Table) and Discussions:

4 bit full adder cum subtractor truth table is given below:

S(cin)	x_4 x_3 x_2 x_1	y_4 y_3 y_2 y_1	C(out)	s_4 s_3 s_2 s_1
0	0 0 0 0	0 0 0 0	0	0 0 0 0
1	0 0 0 0	0 0 0 0	1	0 0 0 0
0	0 0 0 0	0 0 0 1	0	0 0 0 1
1	0 0 0 0	0 0 0 1	0	1 1 1 1
0	0 0 0 0	0 0 1 0	0	0 0 1 0
1	0 0 0 0	0 0 1 0	0	1 1 1 0
0	0 0 0 0	0 0 1 1	0	0 0 1 1
1	0 0 0 0	0 0 1 1	0	1 1 0 1
0	0 0 0 0	0 1 0 0	0	0 1 0 0
1	0 0 0 0	0 1 0 0	0	1 1 0 0
0	0 0 0 0	0 1 0 1	0	0 1 0 1
1	0 0 0 0	0 1 0 1	0	1 0 1 1
....	.....	.....	...	.....
0	1 1 1 0	1 1 1 0	1	1 1 0 0
1	1 1 1 0	1 1 1 0	1	0 0 0 0
0	1 1 1 1	1 1 1 1	1	1 1 1 0
1	1 1 1 1	1 1 1 1	1	0 0 0 0

A 4 bit full addar cum subtractor is a circuit that can perform both addition and subtraction of any two 4 bit binary numbers. To obtain this circuit we have to use 4 bit parallel adder which we can get using 4 full addars or the IC - 7483. After that we have to give 4 inputs for the 4 bit binary number and for the second binary value we have to input a carry in value with each bit through an XOR gate and alone. As a result we will get a carry bit and 4 sum output bits.

After buiding the curcuit, it we want to perform addition, we have to send 0 as the carry in bit and the values of the two binary numbers. In this way, the second binary input

will not change in the XOR gate and the carry bit being 0, will not make a difference. So the IC-74283 or the 4 bit parallel addar will perform addition.

Again If we want to perform subtraction, we have to input 1 in the carry in bit. As a result, it will perform 1's compliment on the second binary value through the XOR gate. Then that number being added again with the carry in value. 1, gives us the 2's compliment which is the negative value of that number. Then the 4 bit parallel adder adds the negative value of the second number with the positive value of the first binary value which makes the subtraction operation complete and gives us output of 5 bits.

Moreover, It was a fun project to do and I did not find any problems doing it.