BRAC UNIVERSITY

CSE-350: Digital Electronics and Pulse techniques

Exp-03: Study of a TTL NAND gate with totem pole output

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OBJECTIVES

1. Building standard TTL NAND Gate.
2. Measure the voltages and verify the circuit.

Equipments and component list

Equipments

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x5 pieces
- Diode 1N4003 - x1 piece
- Capacitor - 4.7 μF - x1 piece
- Resistors -
  - 4K - x1 piece
  - 1.5K - x1 piece
  - 1K - x1 piece
  - 100 - x1 piece

Task-01: TTL NAND gate

THEORY

In this task, we will implement a Transistor-Transistor Logic (TTL) NAND gate with a totem-pole output. Transistor-Transistor Logic, or TTL, refers to the technology for designing and fabricating digital integrated circuits that employ logic gates consisting primarily of bipolar transistors. TTL is the successor of diode-transistor logic (DTL), overcoming the main problem associated with DTL, i.e., lack of speed. TTL provides

faster switching compared to DTL; in fact, TTL is the fastest saturated logic family. Figure 1 shows a basic 2-input TTL NAND gate with a totem-pole output.

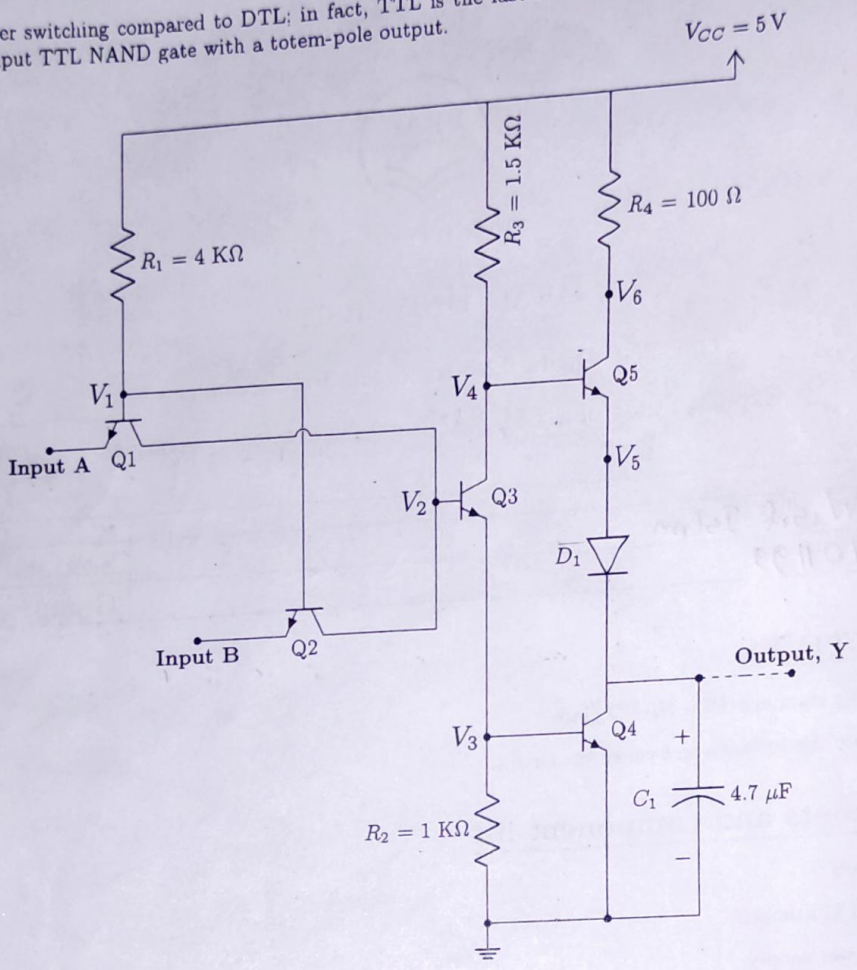


Fig 1: TTL NAND Gate

If any of the inputs A and B is LOW (0.2V), transistor Q1 and/or Q2 will operate in saturation mode and V_2 node will have a voltage of 0.2V + $V_{CE}(sat)$ = 0.4V which causes transistors Q3 and Q4 to be in cut-off mode. Now, node V_4 has 5V while V_6 is obviously less than 5V because of voltage drop in R_4 and Q5 will operate in forward-active mode which means V_{CE} of Q5 is 0.7V. As the diode D_1 has a conducting voltage drop of 0.7V and V_Y will be V_4 - 0.7 - 0.7 = 3.6V approximately which we shall consider as high voltage in output. When both inputs are HIGH (5V), transistors Q1 and Q2 will operate in reverse-active mode. In this case, transistors Q3 and Q4 will be in saturation which ensures that V_{CE} of Q4 is 0.2V and thus the output is 0.2V (LOW).

The most basic TTL circuit has a single output transistor configured as an inverter with its emitter grounded and its collector tied to V_{CC} with a pull-up resistor, and with the output taken from its collector. Most TTL circuits, however, use a totem pole output circuit, which replaces the pull-up resistor with a V_{CC}-side transistor sitting on top of the output transistor. The emitter of the V_{CC}-side transistor (whose collector is tied to V_{CC}) is connected to the collector of the output transistor (whose emitter is grounded) by a diode. The output is taken from the collector of the output transistor.

As mentioned earlier, TTL has a much higher speed than DTL. This is due to the fact that when the output transistor (Q4 in Figure 1) is turned off, there is a path for the stored charge in its base to dissipate through, allowing it to reach cut-off faster than a DTL output transistor. At the same time, the output capacitor is charged from V_{CC} through Q5 and the output diode (D_1), allowing the output voltage to rise more quickly to logic '1' than in a DTL output wherein the output capacitor is charged through a resistor.

Procedure:

1. Connect the circuit as shown in Figure 1.
2. Observe the output for all possible input combinations and fill up table-1.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
0	0	0.67	0.01	0.08	4.91	4.26	4.56	3.72
0	4.92	0.7	0.04	0.1	4.91	4.26	4.56	3.72
4.92	0	0.7	0.05	0.11	4.91	4.26	4.56	3.72
4.92	4.92	2.17	1.52	0.77	0.79	0.33	4.93	0.02

Table 1: Table for TTL NAND gate

Report

Please answer the following questions briefly in the given space.

1. Why is totem-pole output used in place of a passive pull-up resistor?

Ans. totem pole output is use to ensure that the output of the circuit reaches a high voltage when pulled up and low voltage when pull down. which passive pull up resistor fails to do so. That is why totem pol output is used.

2. What is the function of Q3 transistor(phase-splitter)?

Ans. when the inputs A and B is low (0.2V), causing transistor Q_1 and Q_2 to operate in saturation. here Q_3 transistor is cut-off mode. as a result Q_4 is also in cut-off mode. because there is no current flow through Q_3 to it's base. Again,

when input A, B is high Q_1 and Q_2 is in reverse active mode. and Q_3 act as a phase spilter. and this turn on Q_4, allowing current to flow and giving a low output.

3. What may happen if diode D_1 is not used in the circuit?

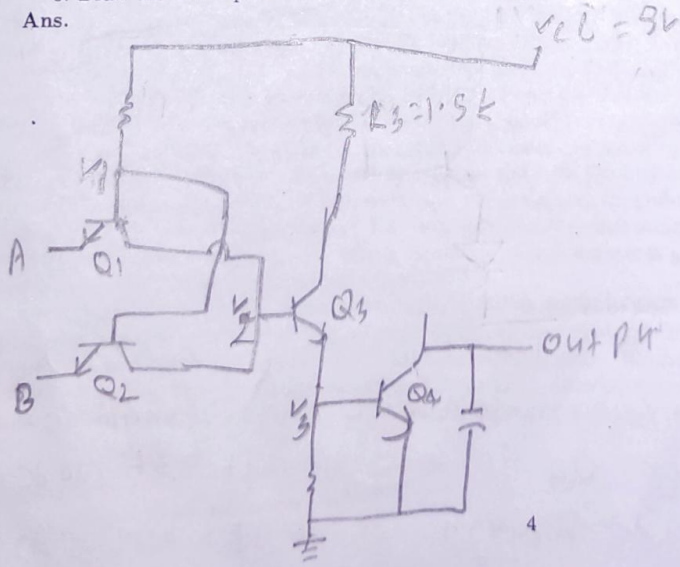
Ans. The diode helps to stabilize the output voltage. The diode prevents reverse current flow. it prevents the output voltage from rising above V_{cc}. if diode was not use we would get inaccurate output.

4. What is the mode of operation of the Q5 transistor when output is HIGH?

Ans. When both output are high. Q_1 and Q are in reverse active mode. Q_3 and Q_4 will be in saturation. with Q_3 and Q_4 in saturation Q_5 will be in cut off. So, the output voltage will be low.

5. Draw the active portion of the circuit when output is LOW.

Ans.



6. What is the operating mode of Q1 and Q4 transistors when Input A is LOW? Verify using experimental data.

Ans. when A_1 is low Q_1 will be in saturation mode V_2 will be 0.4V as found in the experimental data. and the Q4 will will be in cut off and V_3 should be zero or close to zero and we found 0.1V in V_3. so when A is high Q_1 in saturation and Q_4 in cut off has been verified with the use of experimental data.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
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4.92	0	0.7	0.05	0.11	4.91	4.26	4.56	3.92
4.92	4.92	2.17	1.52	0.77	0.79	0.33	4.93	0.02

Table 2: Table for TTL NAND gate

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Signature