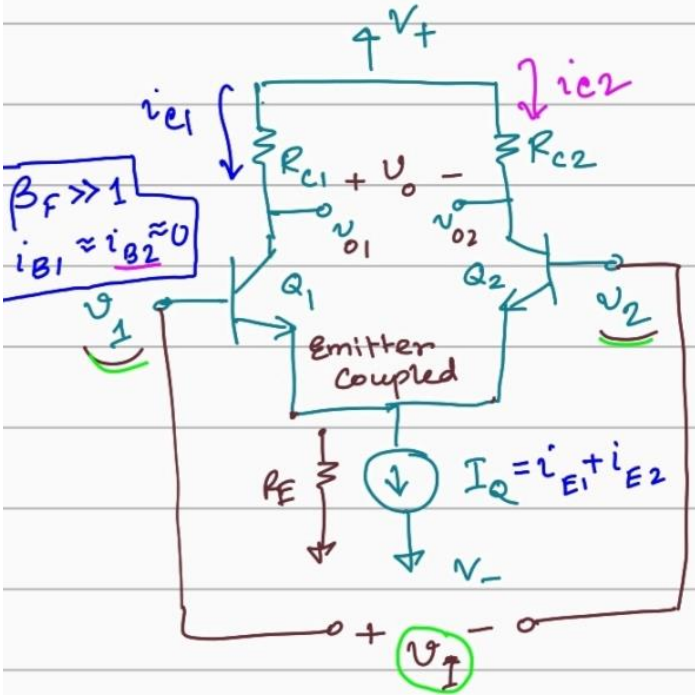
Emitter Coupled Logic
ECL logic family

→ Bipolar → Unsaturated logic family

The logic transistors would operate in forward active or cutoff mode.

The transistors will not saturate. Hence, the storage time would be lower and switching time would be faster.

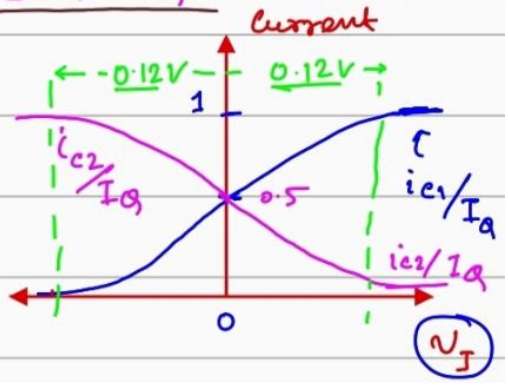
Basic Differential Amplifier:



$v_I = v_1 - v_2$

$v_o = v_{o1} - v_{o2}$

Qualitative description of dc transfer characteristic



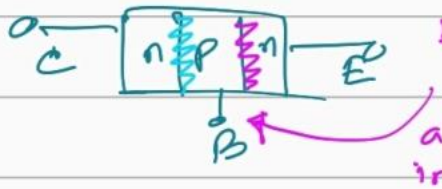
* $\begin{pmatrix} v_1 \gg v_2 \\ v_I \gg 1 \end{pmatrix}$ $Q_1 \rightarrow$ ON (F.A.). $Q_2 \rightarrow$ OFF. $i_{C1} \approx i_{E1} \approx I_Q$

$i_{C2} \approx i_{E2}$, $i_{C1} + i_{C2} = I_Q \Rightarrow i_{C2} \approx 0$

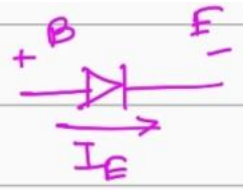
* $(v_1 \ll v_2)$ $Q_1 \rightarrow$ OFF , $Q_2 \rightarrow$ ON (F.A). $i_{C2} \approx i_{E2} \approx I_Q$

$i_{C1} \approx i_{E1} \approx 0$ $[\because i_{C1} + i_{C2} = I_Q]$

Remarks: The coupled emitter causes the total emitter current $i_{E1} + i_{E2}$ to be constant. Also the high value of β_F is responsible for negligible amount of base current. So for ECL circuits we are going to ignore base currents and would take collector currents equal to emitter current if nothing mentioned in question.



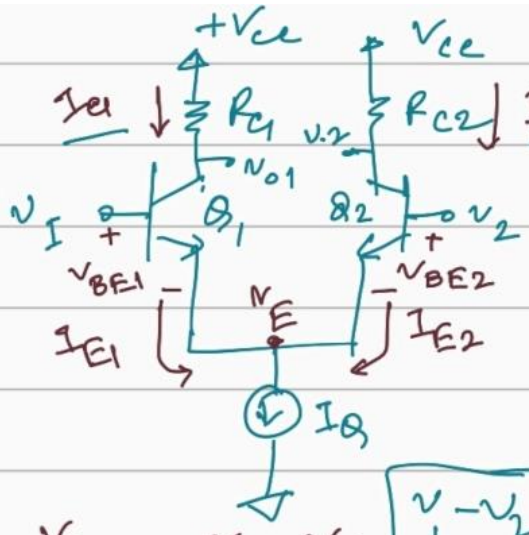
base emitter junction is at forward bias in forward active mode.



$$I_E = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

I_S = reverse saturation current $\sim 10^{-9}/10^{-16}$ A

V_T = thermal voltage = 0.0259 V $[T = 300k]$



$$\frac{I_{E1}}{I_{E2}} = \frac{I_S \exp\left(\frac{V_{BE1}}{V_T}\right)}{I_S \exp\left(\frac{V_{BE2}}{V_T}\right)}$$

$$\Rightarrow \frac{I_{E1}}{I_{E2}} = \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right)$$

$V_{BE1} = V_1 - V_E$

$V_{BE2} = V_2 - V_E$

$V_1 - V_2 = -V_I$

$$\Rightarrow \frac{I_{E1}}{I_{E2}} = \exp\left(\frac{V_1 - V_2}{V_T}\right)$$

$$\Rightarrow \frac{I_{C1}}{I_{C2}} = \exp\left(\frac{V_I}{V_T}\right) \quad [I_B \approx 0$$

∴ Suppose, $I_{C1} \approx 100\, I_{C2}$, then

$$100 \approx \exp\left(\frac{V_I}{0.0259}\right) \Rightarrow V_I = 0.12V$$

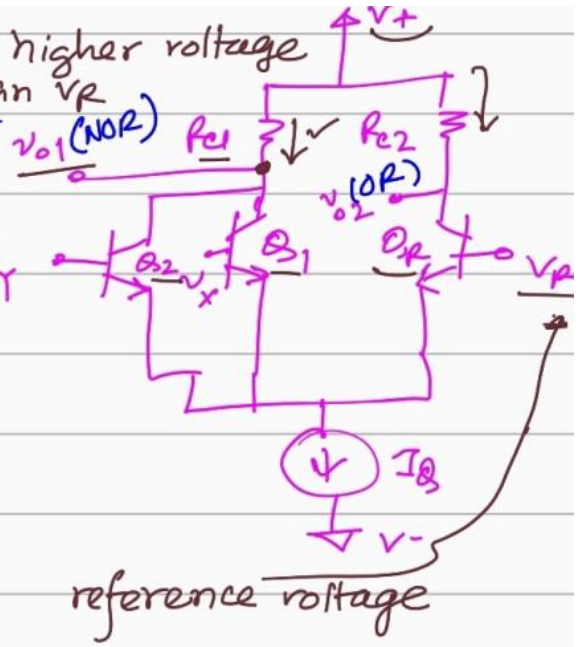
Because, $I_{E1} + I_{E2} = I_{C1} + I_{C2} = I_Q$, we can tell if $V_I > 0.12V$ we have $I_{C1} \approx I_Q$ and $I_{C2} \approx 0$.

Basic NOR gate operation:

Logical high voltage means higher voltage than V_R

v_x	v_y	Q_1	Q_2	Q_R	v_{o1}	v_{o2}
L	L	C	C	FA	H	L
L	H	C	FA	C	L	H
H	L	FA	C	C	L	H
H	H	FA	FA	C	L	H

v_x, v_y, NOR, OR

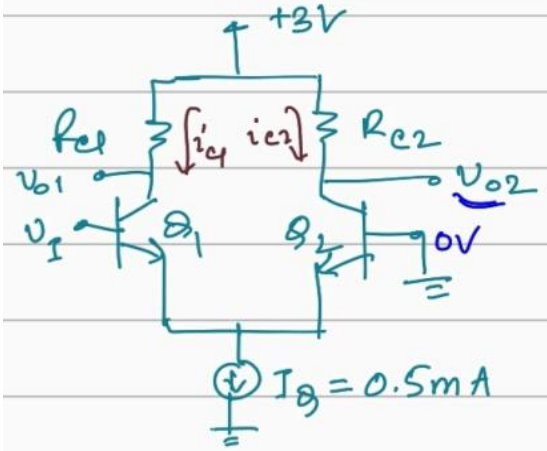


Keamon's 17.31 Neglect the base current for the following circuit.

(a) Determine the value of R_{c2} such that the minimum value of $v_{o2} = 0$.

(b) Determine the value of R_{c1} such that $v_{o1} = 1V$ and $v_I = 1V$.

(c) Determine the value of v_I so $i_{c1} = 0.40mA$ and $i_{c2} = 0.1mA$.



(a) we can achieve minimum voltage v_{o2} if current flows through R_{c2} resistor and voltage drops from 3V to given minimum value 0V.

maximum value of $i_{c2} = I_Q$

$$i_{c2} = \frac{3-0}{R_{c2}} \Rightarrow \boxed{R_{c2} = 3/0.5 = 6k\Omega}$$

We have to turn on Q_2 to make this happen.

(b) When $v_I = 1V > 0V$. $Q_1 \rightarrow$ F.A and $Q_2 \rightarrow$ cutoff. $i_{c2} \approx 0mA$ and $i_{c1} \approx 0.5mA$.

Therefore, $i_{c1} = 0.5mA = \frac{(3 - v_{o1})}{R_{c1}} = \frac{3-1}{R_{c1}}$

$\therefore \boxed{R_{c1} = 4k\Omega}$

(c) $\frac{i_{c1}}{i_{c2}} = \frac{0.1}{0.4} = \exp\left(\frac{v_{BE1} - v_{BE2}}{V_T}\right) = \exp\left(\frac{v_1 - 0}{V_T}\right)$

$\Rightarrow v_1 = V_T \ln\left(\frac{0.1}{0.4}\right) = 0.0259 \ln\left(\frac{1}{4}\right)$

$\boxed{v_I = -0.0359V}$