CSE 260

LAB Assignment 03

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CSE 260 Lab Report

1) Name of the Experiment: Parity Generator and Checker.

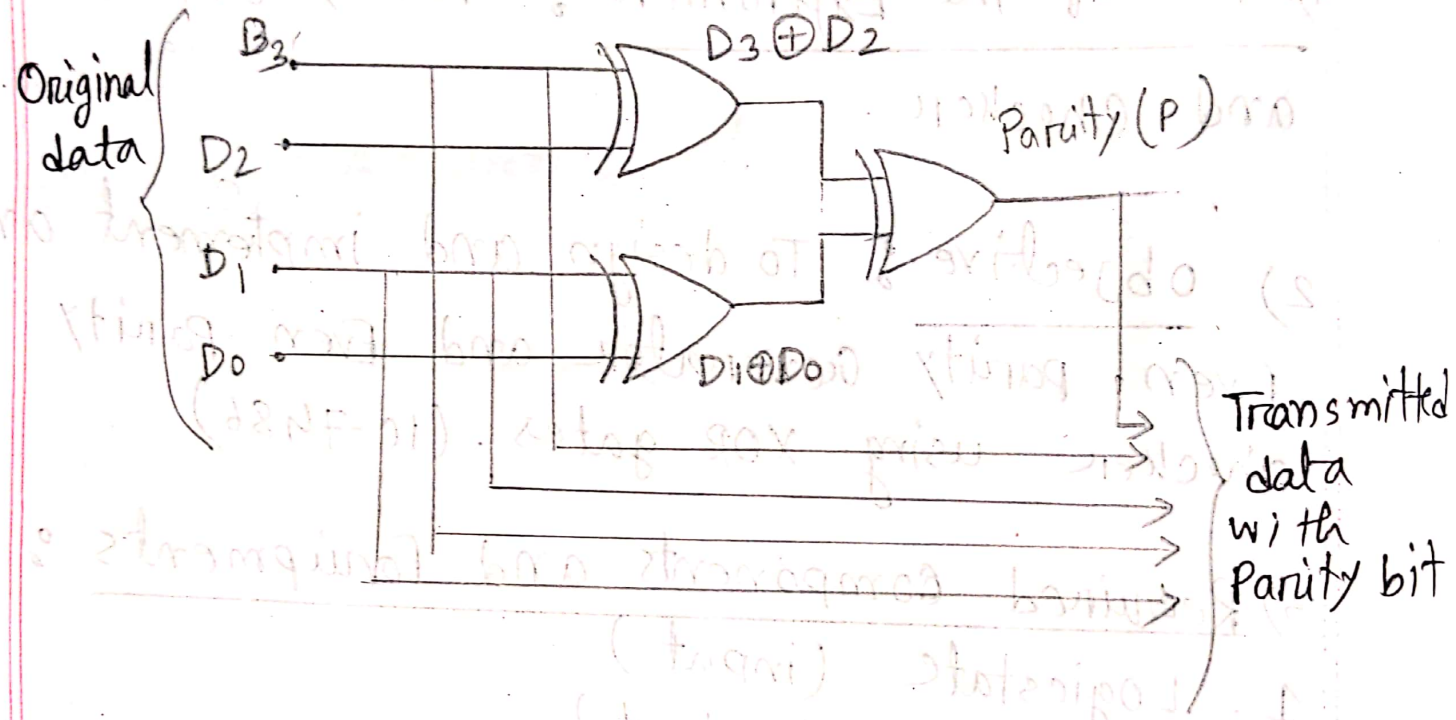
2) Objective: To design and implement an Even parity Generator and Even Parity checker using XOR gates. (IC-7486)

3) Required Components and Equipments:

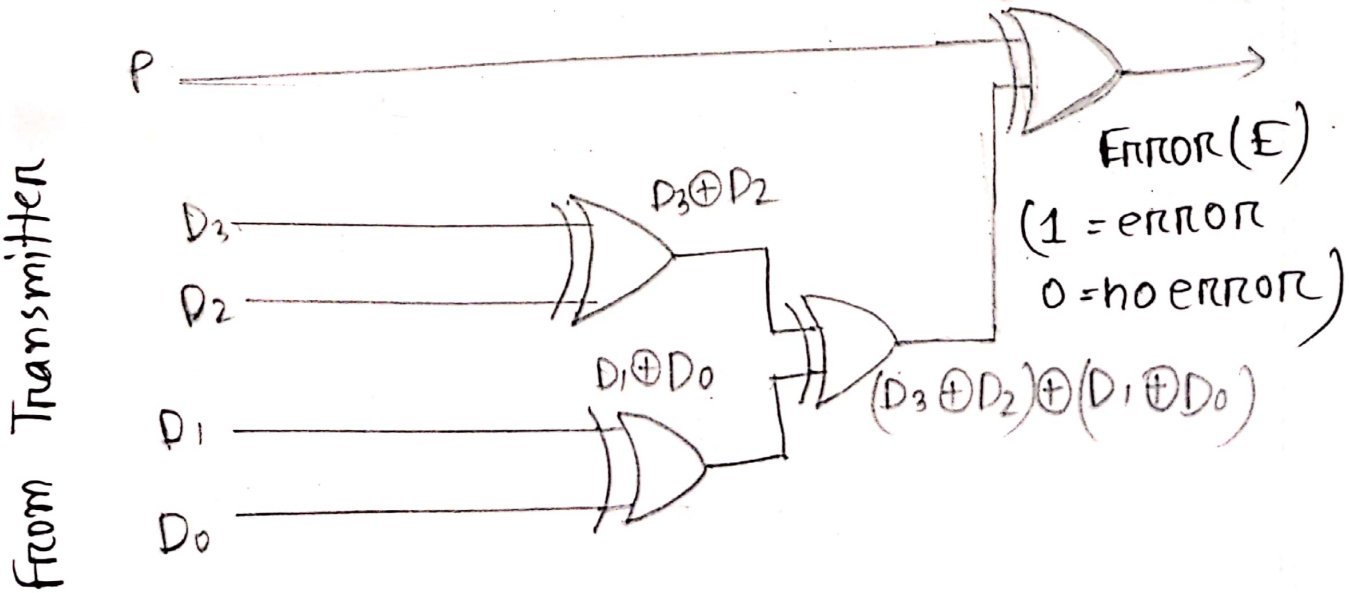
1. Logicstate (input)
2. Logicprobe (output)
3. XOR gate

4) Experimental setup :

Even parity generator :



Even Parity checker :



5. Results in Tabulated form :

1) Parity generators output :-

set	D_3	D_2	D_1	D_0	P
a	0	1	1	1	1
b	1	0	0	1	0
c	0	0	0	0	0
d	0	1	0	0	1

Here, the outputs of P are the results of each of the sets of input data D_3, D_2, D_1, D_0.

2) Parity Checkers output for given sets of data from the transmitter -

P	D_3	D_2	D_1	D_0	output
0	1	0	1	0	0
1	1	1	1	0	0
1	1	1	1	1	1
1	0	0	0	0	1

6. Disscussions : In a parity bit generator if the number of 1 is of even number, it gives zero. Again if number of 1 is of odd number, it gives 1 as output. For this reason in our parity generators output, we found 1 in first and last set of inputs as there are uneven numbers of 1 and received 0 as output in second and third set of inputs as there are even numbers of 1. In the parity checker, if the output is zero, it means the inputs for a parity remain unchanged which shows no error. Again if output is 1, it stand for an error.