Q: Are all of these enough to get full marks in the exam?

A: NO. This is a practice sheet. Meaning, you can practice all you want using the questions from this sheet. However, doing well in exams depends upon your ability to understand a question, formulate an answer, and express it correctly. You see, these are humane skills which cannot be guaranteed from completing a practice sheet only. But yeah, Best of luck anyways.

Chapter 1 (Computer Abstractions and Technology)

Question - 1:

Assume a 19 cm diameter wafer, X has a cost of 20, contains 89 dies, and has 0.023 defects/cm^2.Assume another 20 cm diameter wafer, Y has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2

A

A. What do you understand by yield?
B. Dies per wafer ≈ Wafer area / Die Area - Explain why there is “≈” not “=”
C. Find the yield for both wafers.
D. Find the cost per die for both wafers.

Question - 2:

Suppose gaming consoles PlayStation 5 and Xbox Series X use different implementations of AMD's Zen 2 architecture. The instructions they support can be divided into four classes according to their CPI (class A, B, C, and D). PlayStation has a clock rate of 2.7 GHz and the instruction classes have CPIs of 7, 2, 3, and 6 respectively whereas Xbox has a clock rate of 3.0 GHz and the instruction classes have CPIs of 5, 4, 2, and 1 respectively. Now suppose, a program has an instruction count of 1.0 * 10^6, and the instructions are divided into classes as follows:

30% class A,
50% class B,
10% class C, and
10% class D.

Now answer the following questions:
1. Calculate how many more clock cycles per instruction on average does the PlayStation take compared to the Xbox?
2. Calculate the difference between the execution time in these two consoles in milliseconds

3. If the program runs on a reference PC with an execution time of 120 ms, calculate the SPECRatio for the PlayStation

Question - 3:

Consider three different processors P1, P2, and P3 executing the exact same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
Now answer the following questions:

a. Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the execution time by 30%, but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Question - 4:

Consider a computer running a program that requires 250s, with 70s spent executing add instructions, 85s executed sub instructions, and 40s spent executing left-shift instructions.

a. By how much is the total time reduced if the time for add operations is reduced by 20%?
b. Can the total time can be reduced by 20% by reducing only the time for left-shift instructions?

Question - 5:

Processor, P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. Processor,P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions.

a. We consider the processor with the largest MIPS has the largest performance. See if this is true for Processor P1 and P2.

Question - 6:

Explain the power trend equation. If a new system has 14.3% less capacitive load and uses only 81.3% of the voltage and frequency of the old system, what percentage of power utilization can be reduced in the new system compared to the old system?

Question - 7

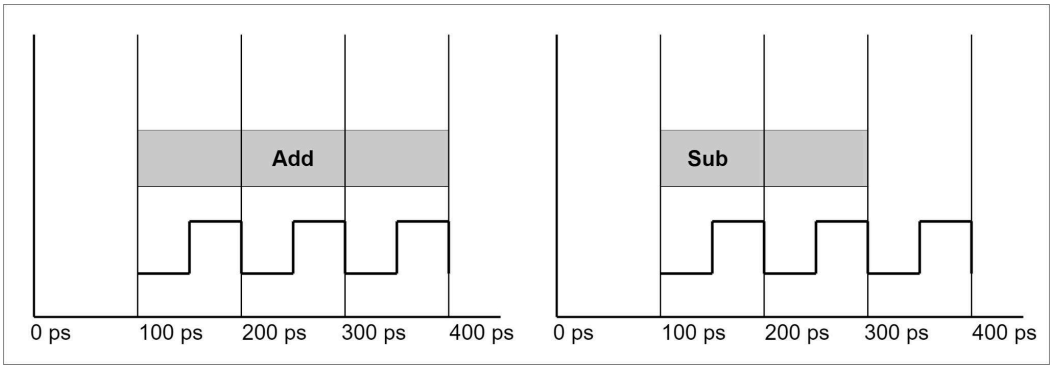

Figure 1: Represents 1 add instruction

Figure 2: Represents 1 sub instruction

Program **A** is divided into two classes according to their **CPI** (Add and Sub). The **instruction counts** are 21 and 3 respectively. Reference for **program A** is 1080ps.

Now, answer the following questions,

a) What is the Clock period? **Hint**: follow any of the figures
b) What is the frequency?
c) What is the CPI for Add and Sub ?
d) What is the Avg. CPI?

e) Find out the execution time of the program?

f) Find the SPEC ratio?

g) If you want to improve the performance by 1.2 times, what improvement do you need to include in the program's add operation?

Chapter 2 (Instructions: Language of the Computer)

Question - 1:

Construct the equivalent RISC-V code of the following C code. Once you have the RISC-V code, identify type of each instruction and encode them accordingly.

```
A[7] = A[2] + A[B[8]] + 10;
B[i] = A[3] - 8;
```

Base addresses of array A and B are in register X_{20} and X_{21} and i is in register X_{22}

Question - 2:

Construct the equivalent RISC-V code of the following C code.

```
for (i = 8; i > 0 ; i--) {
  if ( A[i] == i){
     A[2] = A [B[3]] ;
  }
}
```

Base addresses of array A and B are in register X_{20} and X_{21} . Also consider i is in register X_{22}.

Question - 3:

Construct the equivalent RISC-V code of the following C code.

```
if ( A[i] < i){
     A[2] = A [B[3]] ;
}
```

Base addresses of array A and B are in register X_{20} and X_{21} . Also consider i is in register X_{22}.

Question - 4:

Construct the equivalent RISC-V code of the following C code.

```
if ( A[3] != A[6]){
    if (A[3] == 0) {
        A[3] = A[3] + 2;
    }else{
         A[6] = A[6] / 16;
    }
}else{
    A[6] = A[6] * 8
}
```

Base addresses of array A and B are in register X_{20} and X_{21} .

Question - 5:

Translate the following code written in C programming language into instructions sequence written in RISC-V Assembly. The values in the variables a, b, and c inside the add function are stored in the argument registers $\$X_{10}$, $\$X_{15}$, and $\$X_{12}$ respectively. Also, the values in the variables x and y inside the are stored in the argument registers $\$X_{13}$ and $\$X_{14}$ respectively. The return value is stored in the return register $\$X_{11}$ for both functions.

```
int max(int x, int y) {
  if(x > y)
        return x;
  else
    return y;
}
```

```
int calc(int a, int b, int c) {
  return a + max(b,c)
}
```

Question - 6:

Construct the equivalent RISC-V code of the following C code.

```
Main () {
    int x = 0;
    int y = 9;
    int z = addition(x, y);
}

int addition (int a, int b) {
    int c = a + b;
    return c;
}
```

Variables x, y, z are stored in X_{20}, X_{21} and X_{22} registers. Argument x, y are passed using register X_{13}, X_{14}
Variable c from the addition function also uses register X_{21}

Question - 7:

Write RISC-V assembly code that checks if the number stored in register $\mathbf{X_{25}}$ is **even** or not. If **even** then store **1** in register $\mathbf{X_{26}}$ otherwise store **0**.

Question - 8:

ADD X_{25} , X_{25} , X_0 . Can you make this instruction faster? If yes, Write the updated instruction?

Question - 9:

Memory Location	Code	Line Number	Machine Code
	ADDI $\mathbf{X_5}$, $X_{\mathbf{0}}$, 5	1	
	ADDI $\mathbf{X_6}$, $X_{\mathbf{0}}$, 1	2	
	ADDI $\mathbf{X_{25}}$, $X_{\mathbf{0}}$, 0	3	

	Loop: BLT $\mathbf{X}_5$, $\mathbf{X}_6$, loopBreak	4	_____________________XXX______XXXXXXX
	ADDI X_{25} , X_{25} , 1	5	
#7080	ADDI X_5 , X_5 , -1	6	
	BEQ $\mathbf{X}_0$, $\mathbf{X}_0$, Loop	7	_____________________XXX______XXXXXXX
	loopBreak:	8	

a) What is the value of **PC** while executing line2? Answer: ______________

b) Fill up the machine codes corresponding to line4 and line7 in the table above.

Question - 10:

Memory Location	Code	Line Number
	Loop:	1
	SLLI $\mathbf{X}_{10}$, X_{22} , 3	2
	ADD $\mathbf{X}_{10}$, X_{10} , X_{25}	3
	LD $\mathbf{X}_9$, 0(X_{10})	4
	BNE $\mathbf{X}_9$, $\mathbf{X}_{24}$, Exit	5
#80016	ADDI X_{22} , X_{22} , 1	6
	BEQ $\mathbf{X}_0$, $\mathbf{X}_0$, Loop	7
	Exit:	8

a. Fill up the memory locations.

b. Find the SB-type instructions from the above code and encode them accordingly.
Given,
I. opcode = $(103)_{10}$, funct3 = $(000)_2$ opcode for BEQ
II. opcode = $(103)_{10}$, funct3 = $(001)_2$ opcode for BNE

Construct the equivalent RISC-V code of the following C code.

```
Main () {
  addition(10, 7, 12);
}

int addition (int a, int b, int c) {
    int c = 5;
    int d = max(a, c) + b;
    int e = c + d;
    return e;
}

int max (int a, int b) {
   if(a > b)
         return a;
   else
         return b;
}
```

Arguments for **addition** are passed using register X10, X13, X14. Variables c, d, e are stored in X20, X21, X22 registers. Return value for addition should be stored in X10.

Arguments for **max** are passed using register X10, X13. Return value for **max** should be stored in X10.

Question - 11:

Write necessary RISC-V instructions to store the value (1111 1111 0000 1111 11)2 in X20 register.

Question - 12:

Show how the value 0xabcdef12 would be arranged in memory in RISC-V machine.

Question - 13:

For the RISC-V assembly instructions below, what is the corresponding C/high level statement?

```
slli x30, x5, 3
add x30, x10, x30
slli x31, x6, 3
add x31, x11, x31
ld x5, 0(x30)
addi x12, x30, 8
ld x30, 0(x12)
```

Assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the

add x30, x30, x5 sd x30, 0(x31)	Arrays A and B are in registers x10 and x11, respectively.