Fall 23

CSE341

Final Exam

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sec: 6

1B5C0 1B5C1

set B

Ans to qr no 1

A) size of IVT of intel 8086 = 256 x 4
= 1024 byte
= 1 kB

B) INT 33 = 33 x 4 = 132 = 00084 H
In IVT:
ISR's, IP lower byte - 84 H (value = A0h)
IP Higher byte address = 85 H (value = 15h)
CS lower byte address = 86 H (value = 02h)
CS Higher byte address = 87 H (value = 1Ah)

CS = 1A02 H , IP = 15A0 H

ISR address = 1A02 x 10 + 15A0
= 1B5C0 h

∴ 2 byte hex instruction fetched = 6E5Bh

(c)

Actions taken by 8086 when it gets a request in INTR pin:

1. It sends two INTA acknowledgement pulses on $\overline{INTA}$ pin with the first pulse asking for interrupt vector number and second pulse for getting it.
2. Then it calculates the IVT address for ISR and gets the ISR address.
3. It pushes the flag register in stack clearing IF and TF flag.
4. Pushes the segment address and then pushes the IP address.
5. Then loads the ISR address in IP and executes the interrupt.
6. After interrupt execution, it pops the IP, CS, flags and restores to main programme.

Ans to Q2 (A)

i) length of 1 instruction cycle = 160 ns.

ii) Since it takes 16 bit data from unaligned word, it'll need 2 bus cycles to complete one instruction cycle.

∴ 160 ns = 2 bus cycle

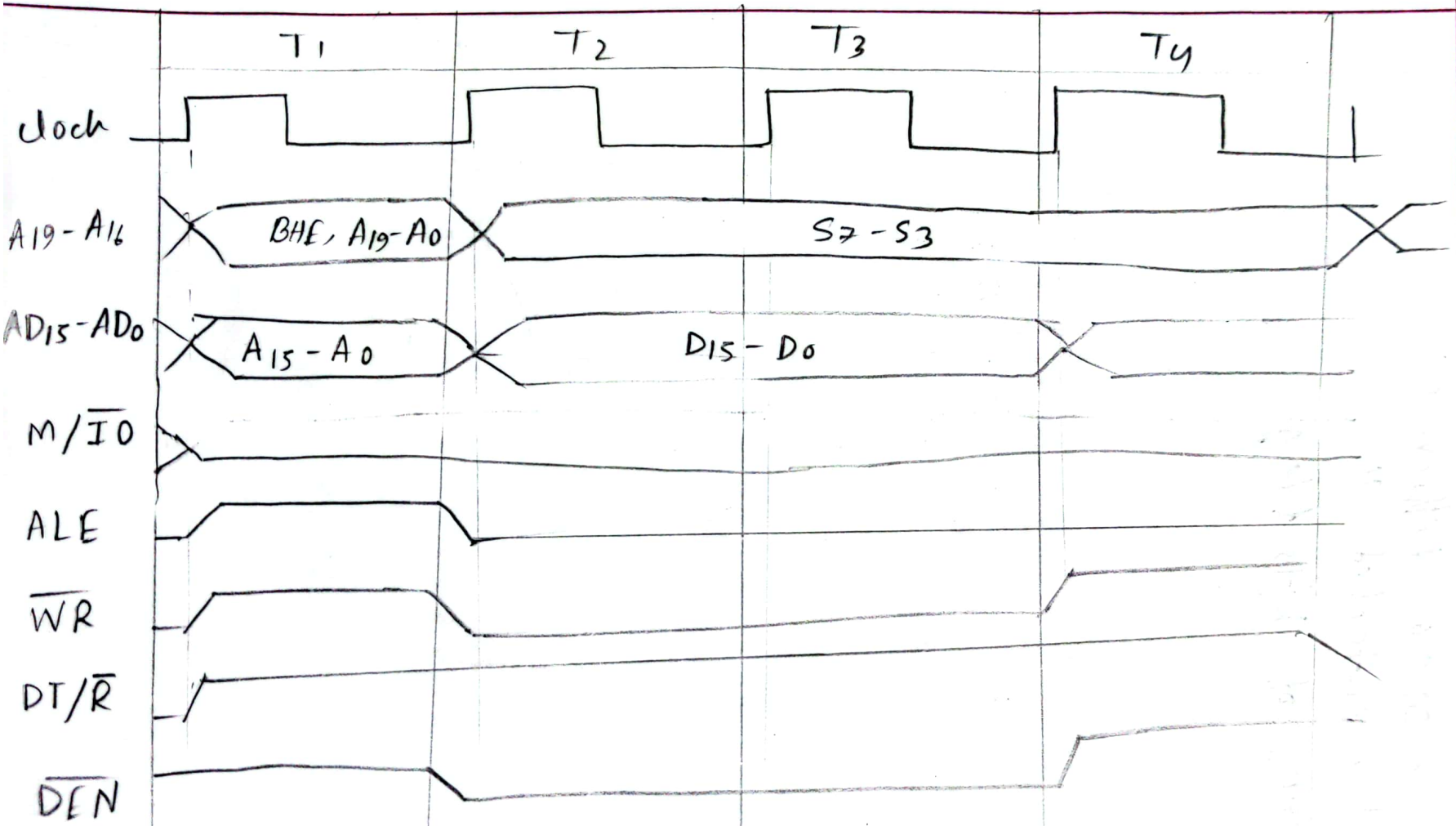
∴ 1 bus cycle = 80 ns.

iii) $f_{max} = \frac{1}{80ns} = \frac{1}{80 \times 10^{-9} s} = 12.5\ MHz$

iv) Duty cycle = 20%.

T_{on} = 20% of 80 = 16 ns

T_{off} = 80 − 16 = 64 ns


T1
T2
T3
Ty
clock
A19 - A16
BHE, A19 - A0
S7 - S3
AD15 - AD0
A15 - A0
D15 - D0
M/IO
ALE
WR
DT/R
DEN

Ans to Q 2 (B)

Ans to Q 2(C)

EM means Emulate processor extension flag. ~~If~~ it's set to one a wp can test results of extended cores without having to change anything in hardware levels.

MP means monitor processor extension. If it's set to 1, it'll mean that wp allows WAIT instruction to develop a sync or extended processor meaning that it can simultaneously process more programmes by extending cores.

Ans to Qr 3

(A) (i) OUT 1234h, AX is invalid.

Reason: As this is a fixed address, it can support upto 8 bits in port address. However the address given is greater than 255. Hence, it cannot by accessed.

(B) I/O addressing technique showed in the ii) OUT DX, AX is a variable addressing technique for only I/O mapped I/O. Here, a word data is being written in DX. Here, DX represents a port for the I/O device.

Again in the 3rd instruction MOV [1234h], AX, the [1234h] represents an address in memory and not port. This can be used in memory mapped I/O process. Here the value of AX register (16 bit) is being stored in memory. 1239h and 1235h

HRQ, HLDA, DREQ, DACK, IOR', IOW', MEMR', MEMW'

Ans to or 3 (c)

① Firstly CPU will set read / write command to I/O devices to start the process.

② When the I/O devices are ready, it will send a DMA request through DREQ pin and connected DREQ will be 1. ③ Then DMA controller will send a Hold Request through HRQ pin to gain control of system bus. Hence, HRQ = 1.

④ CPU will give the DMA bus control by setting the HLDA pin = 1. This is the hold acknowledgement.

⑤ DMA will send DMA acknodgement to I/O devices by setting corresponding DACK pin to 1.

⑥ Now data transfer will start. DMA will read data from memory and

write data in I/O devices.

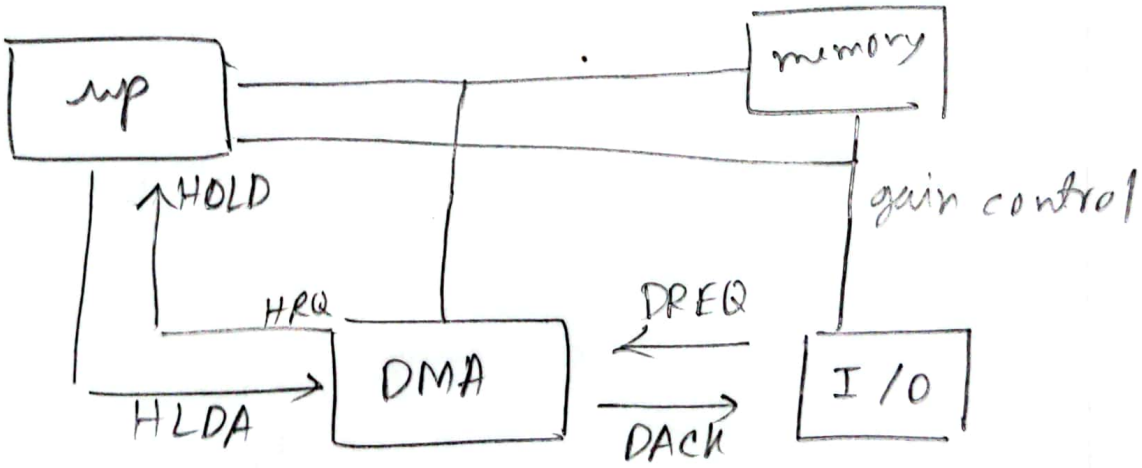
Hence, $\overline{IOR}$ = High (1)

$\overline{IOW}$ = Low (0)

$\overline{MEMW}$ = High (1)

$\overline{MEMR}$ = Low (0)

⑦ After data transfer DMA sends interrupt signal to CPU and DACK is set to 0, CPU disables the HOLD acknowledgement by setting HLDA = 0 and gains system bus control.



Ans to Q 4 (A)

		D	Left
T = 10 ns,	IR6	(7)	43
T = 17 ns,	IR5	(10)	(10)
T = 27 ns,	IR0	(37)	

$T = 10 + 7 + 10 + 37 + 10 + 43$ ns

$= 117$ ns

∴ When IR6 is served $T = 117$ ns

Ans to Q4(B)

When a PIC 8259 gets a high signal in the IR pins, it follows some procedures:

① PIC sends Interrupt to µp through INT pin to µp's INTR pin.

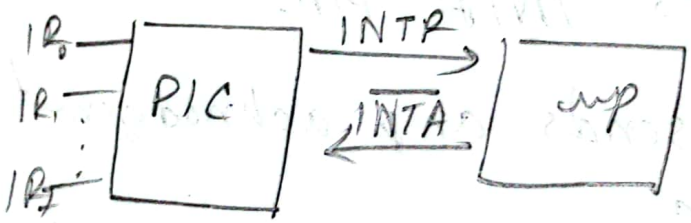
② Then µP sends an acknodgement through $\overline{INTA}$ to PIC.

③ After getting the $\overline{INTA}$, PIC starts to resolve priority using IMR, IRR and ISR register.

④ After resolving priority it updates ISR's value to set the interrupt that will be executed.

⑤ It sends the vector number of the current interrupt to µp and gets disconnected from µp for it to execute the interrupt and resets.

(c) However, if the interrupt is served, a programmer has to set EOP command to let PIC know that ISR has ended so that it can set the bit of ISR to 0. Otherwise new interrupts will not be executed.



Ans to 4(c)

Min PIC required to get 50 interrupt requests at a time = 1 + 4 + 12 = 17