Group Assessment

BRAC University

Semester: Fall 2022
Course No: CSE251 Course Title: Electronic Devices and Circuits

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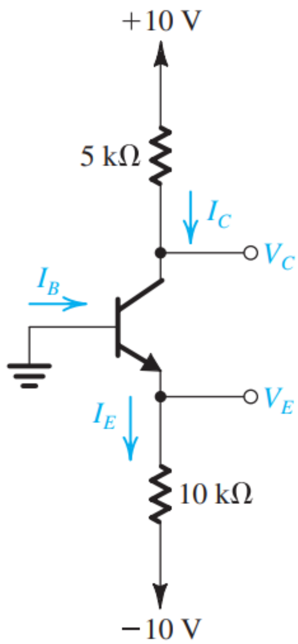
Student IDs:

Set-1

(i)

In the circuit shown in Fig. the voltage at the emitter was measured and found to be –0.7 V. If $\beta = 50$, find I_E, I_B, I_C, and V_C.



Solution:

Let, the BJT is in **active** mode.

Given, $V_E = -0.7V$

$$I_E = \frac{-0.7-(-10)}{10} = 0.93 \, mA$$

$$I_C = \alpha I_E = \frac{\beta}{\beta+1} I_E = \frac{50}{51} \times 0.93$$

$$= 0.92 \, mA$$

$$\therefore I_B = I_E - I_C = 0.01 \, mA$$

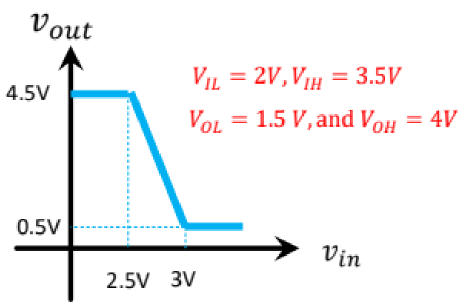
$$\text{now, } I_C = \frac{10 - V_c}{5} = 0.92$$

$$\Rightarrow V_c = 10 - 5 \times 0.92$$

$$\approx 5.45 \, V$$

Here, $V_{CE}=V_C-V_E=5.45-(-0.7) > 0.2V$

(ii) Consider the circuit shown below. Does it follow the Static Discipline? Calculate the noise margins NM_0 and NM_1.



Solution: See the slides on MOSFET.

Set-2

Consider an NMOS transistor fabricated with L = 0.18 μm and W = 2 μm. The process technology is specified to have **k_n'=387 μA/V^2**, and **V_T = 0.5 V**. Find **V_{GS}** and **V_{DS}** that result in the MOSFET operating at the edge of the saturation region with I_{DS} = 100 μA. **If V_{GS} is kept constant, find V_{DS} that results in I_D = 50 μA.**

For MOSFET

$$\boxed{k = k'_n \frac{W}{L}}$$

$$I_D = 0, \text{ if } V_{GS} < V_T$$

$$I_D = k\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right], \text{ if } V_{GS} \geq V_T \text{ and } V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{1}{2}k(V_{GS} - V_T)^2, \text{ if } V_{GS} \geq V_T \text{ and } V_{DS} \geq (V_{GS} - V_T)$$

Solution:

the transistor transconductance parameter k_n,

$$k_n = k'_n\left(\frac{W}{L}\right)$$

$$= 387\left(\frac{2}{0.18}\right) = 4.3 \text{ mA/V}^2$$

With the transistor operating in saturation,

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$I_D = k_n\left[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$50 = 4.3 \times 10^3\left[0.22V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06 \text{ V}$$

Set-3

(i) Draw the I-V graph of a **MOSFET**. Identify all the regions. [You have to draw for at least three V_{GS} values and mark V_{ov} on the graph.]
(ii) Draw the I-V graph of a **BJT**. Identify all the regions. [You have to draw for at least three I_B values on the graph.]
(iii) Draw DTL and RTL inverter circuits. Why do we need these circuits? Explain.

Solution: See the class lecture.

Set-4

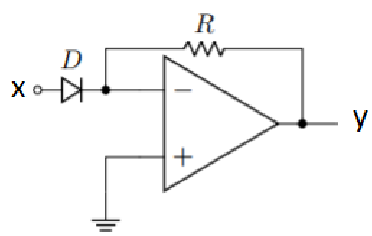


Fig. 1

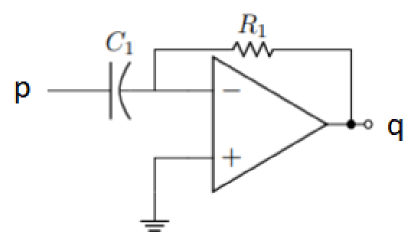


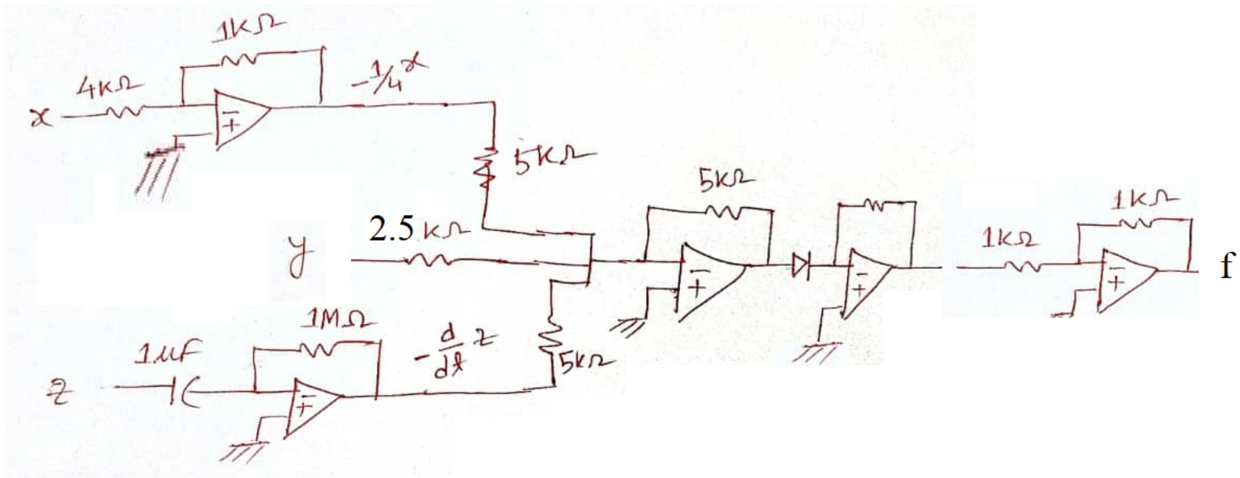
Fig. 2

(i) **Derive** the expressions for y and q (separately).
(ii) Consider y and p nodes to be shorted together. Now **find** the expression for q.
(iii) Design a circuit using Op-Amp to implement the expression:

$$f = \exp\left(\frac{1}{4}x - 2y + \frac{d}{dt}z\right)$$

Solution:
(i) See the class lecture (exponent and differentiator, respectively)
$y = -I_s R \exp(x/V_T)$, $q = -RC\,(dp/dt)$
(ii) $q = -RC\, dy/dt = -RC\, d(-I_s R \exp(x/V_T))/dt$

(iii)



1kΩ
4kΩ
x
$-\frac{1}{4}x$
5kΩ
5kΩ
1kΩ
y
2.5 kΩ
f
1kΩ
1MΩ
1μf
z
$-\frac{d}{dt}z$
5kΩ