CSE 260

Lab Report 8

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Sec : 1

1. Experiment Name : Design and Implementation of the following circuit: four 2 bit numbers A, B, C, D and two selection variables S_1 and S_2 are available. S_1 will select either A or B and S_2 will select either C or D. Depending on the two selection variables, the circuit will work in the following way.

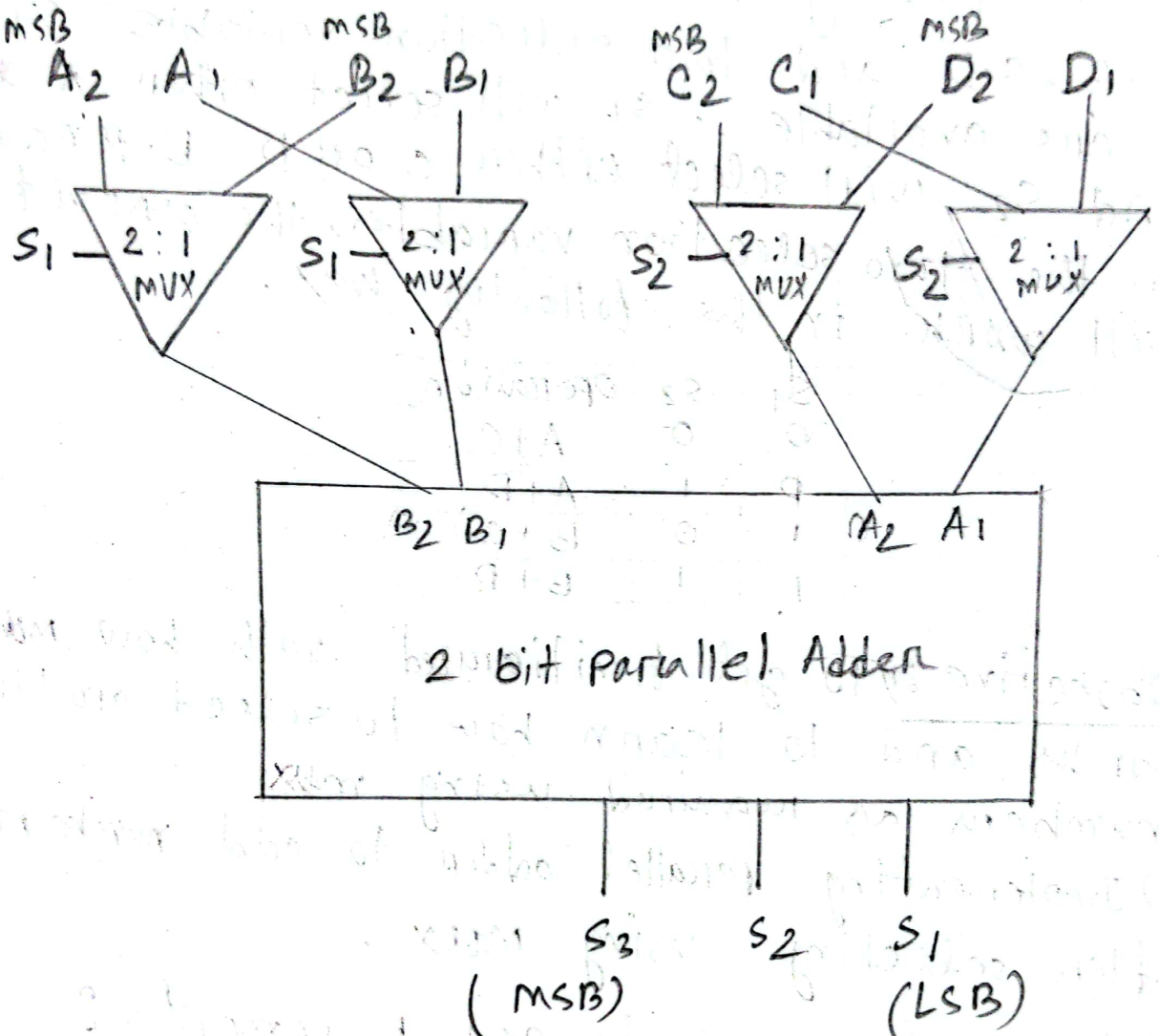
S_1	S_2	Operation
0	0	A+C
0	1	A+D
1	0	B+C
1	1	B+D

2. Objective : i) To get fimiliarized with how mux works and to learn how to select cretain numbers as required using mux.
ii) Implementing parallel adder to add numbers after selecting using mux.

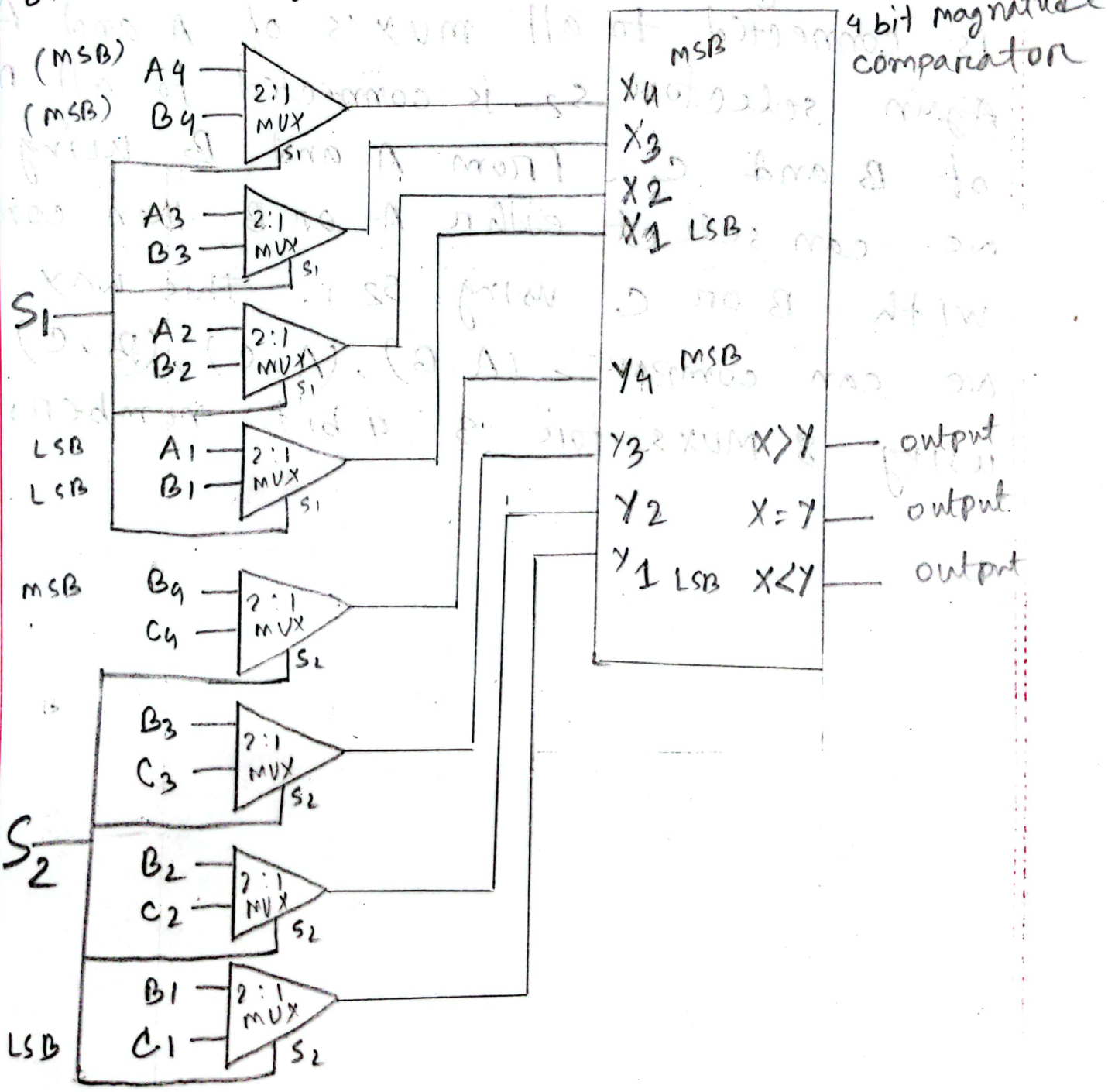
3. Required components and Equipments :

i) LOGICSTATE (input)
ii) LED - Green (output)
iii) IC - MUX (74153)
iv) Parallel Adder IC - 7483

4. Experimental setup :



5. Results and Discussions: A circuit diagram which will compare three 4 bit numbers, using a magnatidue comparator and 2:1 MUXs as given below:



On this circuit $A = A_4 A_3 A_2 A_1$, $B = B_4 B_3 B_2 B_1$, $C = C_4 C_3 C_2 C_1$. The input bits of this circuit are connected through 2:1 MUX then passed to a magnetude comparator. The selector S_1 is connected to all mux's of A and B. Again selector S_2 is connected to all mux of B and C. From A and B using MUX we can select either A or B then compare with B or C using S_2. This way we can compare (A, B), (A, C), (B, C) using 8 MUXs for 3 4 bit numbers.