CSE 260 LAB Report

Experiment Name : Implementation of 4 bit Magnitude Comparator

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1. Name of the Experiment: Implementation of 4 bit Magnitude comparator.

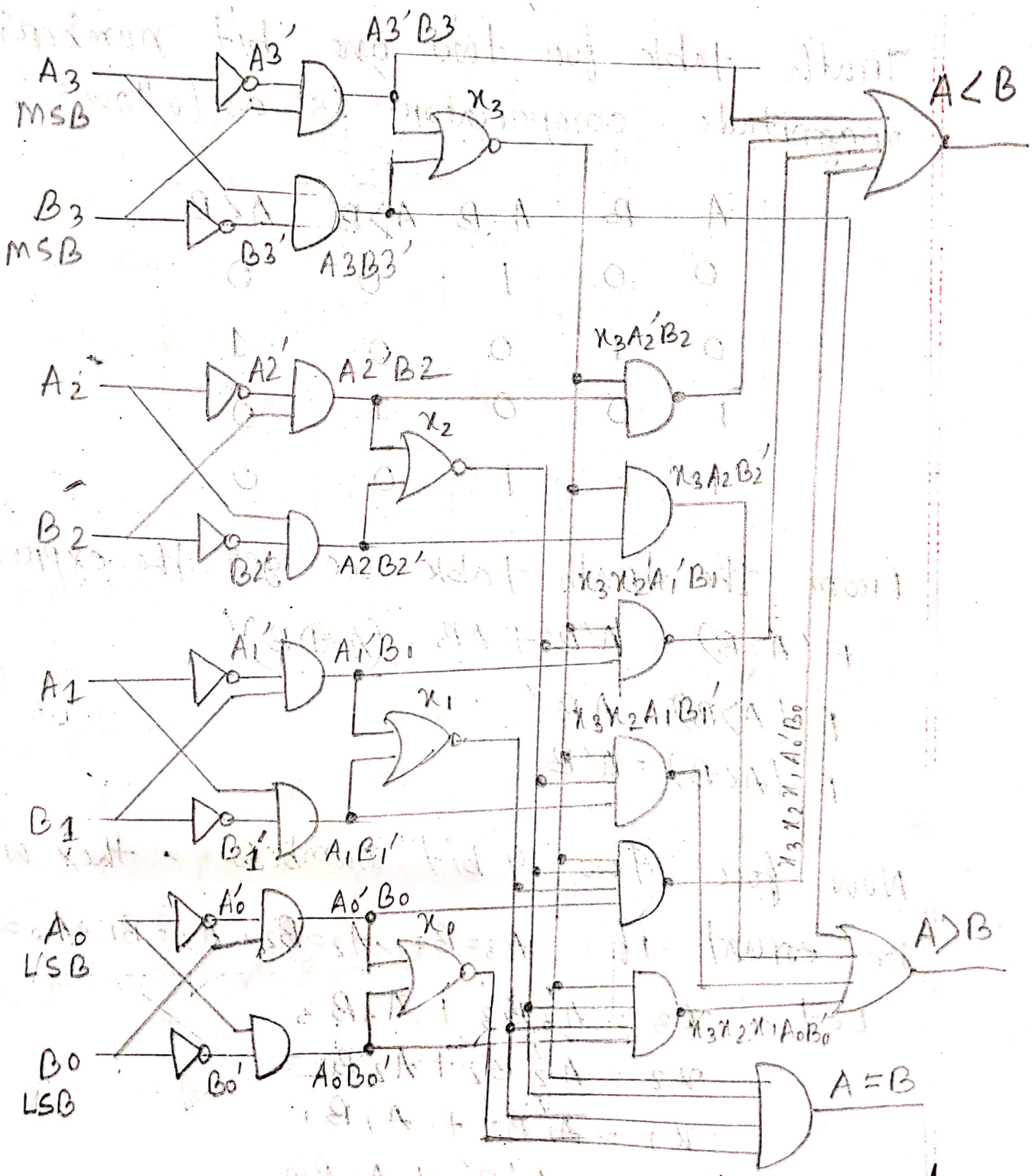
2. Objective: 1. To draw the circuit that will act as a Magnitude comparator and be able to compare two 4 bits number.

2. ~~For~~ To implement the circuit for 4 bit numbers.

3. Required Components and Equipments:

i) AND Gate
ii) AND-3 Gate
iii) AND-4 Gate
iv) NOT Gate
v) OR Gate
vi) OR-4 Gate
vii) LED-Green (output)
viii) LOGICSTATE (input)

4. Experimental setup :



setup: Implementation of 4 bit Magnitude comparator.

Here, In the output of our 4 bit magnitude comparator setup diagram :-

i) $(A = B) = x_3 x_2 x_1 x_0$

$+ A_3B_3 + A_3'B_3' + A_2B_2 + A_2'B_2' + A_1B_1 + A_1'B_1'$

$+ A_0B_0 + A_0'B_0'$

ii) $(A < B) = A_3'B_3 + x_3A_2'B_2 + x_3x_2A_1'B_1 + x_3x_2x_1 A_0'B_0$

(iii) $(A > B) = A_3B_3' + x_3A_2B_2' + x_3x_2A_1B_1' + x_3x_2x_1 A_0B_0'$

These expressions represent the output for each of their objectives which helps compare the di numbers.

Here, in the diagram, $x_i = A_iB_i + A_i'B_i'$

where $i = 0, 1, 2, 3$.

5. Results and Discussions:

Truth table for two one bit numbers magnitude comparator is as follows:

A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

From the truth table we get the expressions:

$$F(A=B) = A'B' + AB = (A \oplus B)'$$

$$F(A>B) = AB'$$

$$F(A<B) = A'B$$

Now for two 4 bit numbers, they will be equal if $A_3=B_3, A_2=B_2, A_1=B_1, A_0=B_0$

Let, $x_3 = A_3'B_3' + A_3B_3$

$x_2 = A_2'B_2' + A_2B_2$

$x_1 = A_1'B_1' + A_1B_1$

$x_0 = A_0'B_0' + A_0B_0$

$\therefore A(A=B) = x_0 x_1 x_2 x_3$

In case of $A > B$, A will be greater than B. if any digit from MSB is greater than the same digit of B.

condition:

$$f(A>B) = (A_3 \geq B_3) + (A_3=B_3)(A_2>B_2) + (A_3=B_3)(A_2=B_2)(A_1>B_1) + (A_3=B_3)(A_2=B_2)(A_1=B_1)(A_0>B_0)$$

$$\therefore F(A>B) = A_3B_3' + x_3A_2B_2' + x_3x_2A_1B_1' + x_3x_2x_1A_0B_0'$$

In terms of finding $A<B$, A will be less than B if any digit from MSB is less than B's.

$$f(A<B) = (A_3<B_3) + (A_3=B_3)(A_2<B_2) + (A_3=B_3)(A_2=B_2)(A_1<B_1) + (A_3=B_3)(A_2=B_2)(A_1=B_1)(A_0<B_0)$$

$$\therefore F(A<B) = A_3'B_3 + x_3A_2'B_2 + x_3x_2A_1'B_1 + x_3x_2x_1A_0'B_0$$

a) To implement the circuit of 4 bit magnitude comparator after taking A_i and B_i inputs for the two 4 bit numbers where $i = 0, 1, 2, 3$, we take the i^{th} digit of inpnt of one number with another numbers compliment through AND crate and ~~get~~ again take the second number's i^{th} digit with first one's i^{th} digits compliment and get $A_i' B_i$, $A_i B_i'$. Then running these through NOR crate we get $(A_i' B_i + A_i B_i')'$ which gives us;

$$(A_i' B_i + A_i B_i')' = (A_i' B_i)' \cdot (A_i B_i')'$$

$$= (A_i'' + B_i)(A_i' + B_i'') \quad \text{[Demorgan's law]}$$

$$= (A_i + B_i')(A_i' + B_i)$$

$$= A_i A_i' + A_i B_i + A_i' B_i' + B_i B_i'$$

$$= A_i B_i + A_i' B_i'$$

$$= x_i$$

After getting x_i where $i = 0, 1, 2, 3$, we run all four of these outputs in an AND_4 gate which gives us $F(A=B) = x_3 x_2 x_1 x_0$.

b) To get the output for $A > B$, we will need 3 And gates AND, AND-3, AND-4 where we will plug x_3, A_2B_2' in AND gate; x_3, x_2, A_1B_1' in AND-3; x_3, x_2, x_1, A_0B_0' in AND-4 gate. Then by running the outputs of these three AND gates along will A_3B_3' through an OR gate we will get the expression

$F(A>B) = A_3B_3' + x_3A_2B_2' + x_3x_2x_1A_1B_1' + x_3x_2x_1A_0B_0'$

c) In order to get the expression for $A < B$, will will again need same three AND gates where we will plug values for $x_3, A_2'B_2$ in AND; $x_3, x_2A_1'B_1$ in AND-3 and $x_3, x_2, x_1, A_0'B_0$ in AND-4. Then if we

Sum these output with $A_3' B_3$ in an OR gate we will get the expression

$$F(A<B) = A_3' B_3 + x_3 A_2' B_2 + x_3 x_2 A_1' B_1 + x_3 x_2 x_1 A_0' B_0$$

We can achieve 4 bit Magnitude Comparator in circuit in the following way.