BRAC UNIVERSITY

Inspiring Excellence

CSE251

Electronic Devices and Circuits

Semester: Fall 22

Exp -05: Study of I-V Characteristics of BJT and Implementation of CE Amplifier Using BJT

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Date of performance: 31/10/22

Date of Submission: 21/11/22

2. Circuit Diagrams:

<u>Diagram 1:</u>

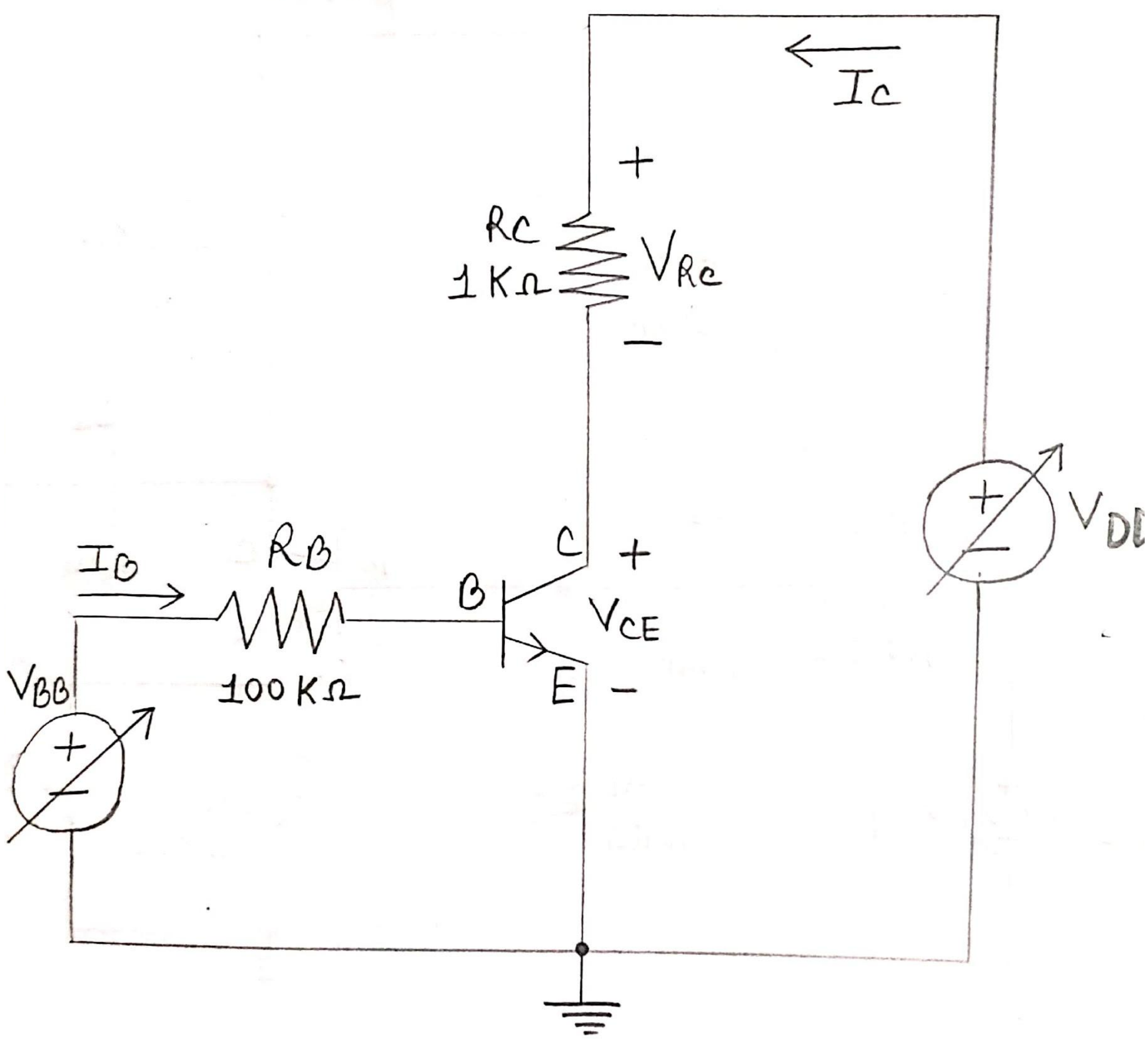


Figure: Circuit for determining the IV charecteristic (I_C vs. V_{CE}) of BJT

Diagram 2:

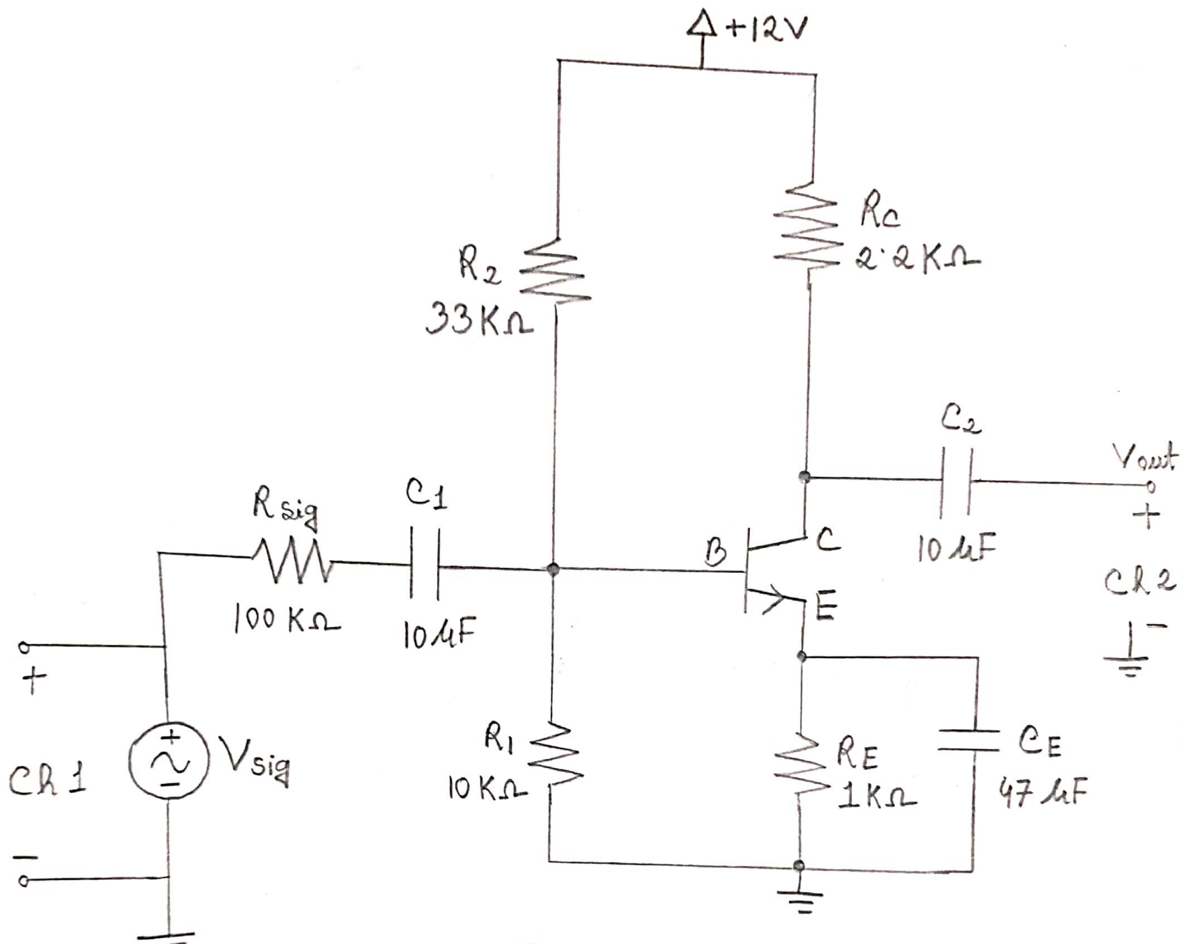


Figure : BJT CE Amplifier Circuit

3. Signed Data Sheets and Calculations:

DATA TABLE 1: OUTPUT I–V CHARACTERISTICS

Actual value of R_B = 97.5kΩ **and R_C =** 0.983kΩ **(using multimeter)**

1. V_{BB} = 2 V

V_{DD} (V)	$I_B = \frac{V_{BB}-0.7}{R_B\,[k\Omega]} \times 10^3$ (µA)	V_{CE} (V)	V_{RC} (V)	$I_C = \frac{V_{RC}}{R_C\,[k\Omega]}$ (mA)	$\beta = \frac{I_C}{I_B}$
0.0	13.334µA	0.0148	0.0053	0.005392	0.4054
0.1		0.0226	0.0297	0.0302	2.2707
0.2	$=13.33\times10^{-3}$ mA	0.0467	0.1126	0.1146	8.6165
0.3		0.051	0.1792	0.1823	13.7067
0.4		0.0596	0.2555	0.2599	19.5413
0.5	= 0.0133 mA	0.0658	0.359	0.3652	27.4586
0.6		0.0746	0.440	0.4476	33.6541
0.7		0.0787	0.565	0.5748	43.2181
0.8		0.0835	0.664	0.6755	50.7895
0.9		0.0869	0.754	0.7670	57.6692
1.0		0.0902	0.857	0.8718	65.5489
2.0		0.1204	1.835	1.8667	140.3534
3.0		0.146	2.783	2.8311	212.8647
4.0		0.181	3.75	3.8149	286.8346
5.0		0.497	4.55	4.6287	348.0225
6.0		1.412	4.60	4.6800	351.8797
7.0		2.298	4.68	4.7609	357.9624
8.0		3.264	4.73	4.8118	361.7895
9.0		4.29	4.78V	4.8627	365.6165
10.0		5.14	4.80V	4.8830	367.1428

2.556V

2. $V_{BB} = 2.5$ V

V_{DD} (V)	$I_B = \frac{V_{BB}-0.7}{R_B\,[k\Omega]} \times 10^3$ (μA)	V_{CE} (V)	V_{RC} (V)	$I_C = \frac{V_{RC}}{R_C\,[k\Omega]}$ (mA)	$\beta = \frac{I_C}{I_B}$
0.2	= 19.0359 μA	0.0288	0.0858	0.0873	4.586
0.5		0.0543	0.3169	0.3224	16.9364
1.0		0.0822	0.885	0.9003	47.2948
2.0	$= 19.0359 \times 10^{-3}$	0.1086	1.842	1.8739	98.4403
3.0	mA	0.13	2.819	2.8678	150.652
4.0		0.1523	3.81	3.8759	203.61
5.0		0.1821	4.81	4.8932	257.051
6.0		0.265	5.71	5.8087	305.144
7.0		0.976	5.98	6.0834	319.5751
8.0		1.865	6.04	6.1444	322.7796
9.0		2.812	6.13	6.2360	327.5915
10.0		3.698	6.26	6.3683	334.5416
11.0		4.730	6.30	6.4089	336.6744
12.0		5.650	6.36	6.4699	339.8788
13.0		6.640	6.41	6.5208	342.5527
14.0		7.560	6.47	6.5819	345.7625

31.10.22

DATA TABLE 2: COMMON EMITTER AMPLIFIER

Measured values of resistances (Using multimeter)				
R_{sig} (kΩ)	R_1 (kΩ)	R_2 (kΩ)	R_C (kΩ)	R_E (kΩ)
97.5	9.98	32.77	2.178	0.989

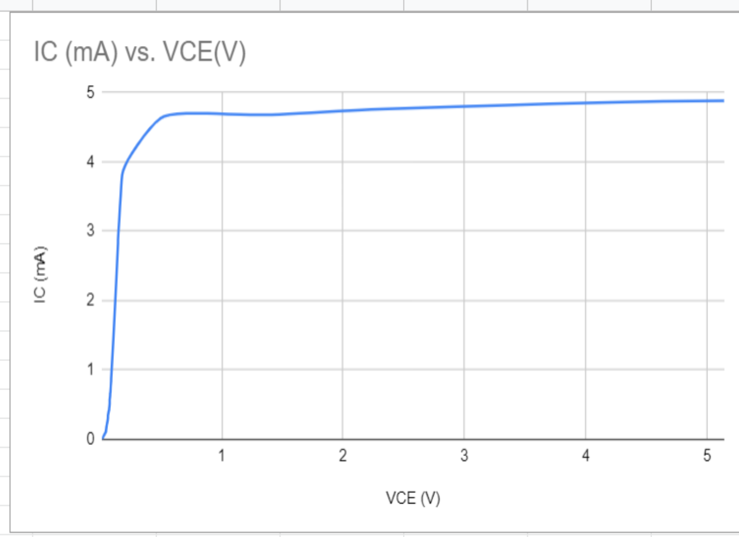
Amplitude of the input signal, v_{sig} (from signal generator) (mV)	Amplitude of the output signal, v_{out} (from oscilloscope) (V)	Gain = $\frac{\lvert v_{sig} \rvert}{\lvert v_{out} \rvert}$ $\frac{v_{out}}{v_{sig}}$
~~244.0 mV~~ 96.8	468 mV	4.83

21.10.22

4. Graphs of IC vs Vce:

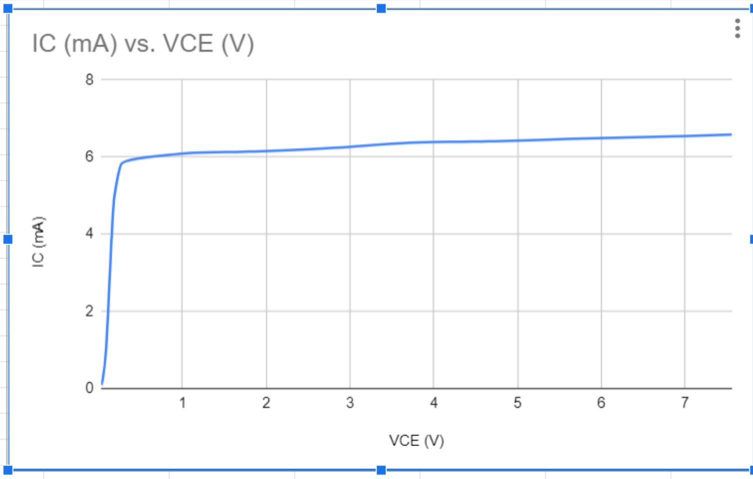
<u>For Vbb= 2v:</u>

VDD (V)	VCE(V)	VRC (V)	IC (mA)
0	0.0148	0.0053	0.005392
0.1	0.0226	0.0297	0.0302
0.2	0.0467	0.1126	0.1146
0.3	0.051	0.1792	0.1823
0.4	0.0596	0.2555	0.2599
0.5	0.0658	0.359	0.3652
0.6	0.0746	0.44	0.4476
0.7	0.0787	0.565	0.5748
0.8	0.0835	0.664	0.6755
0.9	0.0869	0.754	0.767
1	0.0902	0.857	0.8718
2	0.1204	1.835	1.8667
3	0.146	2.783	2.8311
4	0.181	3.75	3.8149
5	0.497	4.55	4.6287
6	1.412	4.6	4.68
7	2.298	4.68	4.7609
8	3.264	4.73	4.8118
9	4.29	4.78	4.8627
10	5.14	4.8	4.883



For Vbb= 2.5v:

VDD (V)	VCE (V)	VRC(V)	IC (mA)
0.1	0.0288	0.0858	0.0873
0.5	0.0543	0.3169	0.3224
1	0.0822	0.885	0.9003
2	0.1086	1.842	1.8739
3	0.13	2.819	2.8678
4	0.1523	3.81	3.8759
5	0.1821	4.81	4.8932
6	0.265	5.71	5.8087
7	0.976	5.98	6.0834
8	1.865	6.04	6.1444
9	2.812	6.13	6.236
10	3.698	6.26	6.3683
11	4.73	6.3	6.4089
12	5.65	6.36	6.4699
13	6.64	6.41	6.5208
14	7.56	6.47	6.5819



5. LT spice Circuit Diagrams:

Diagram 1:

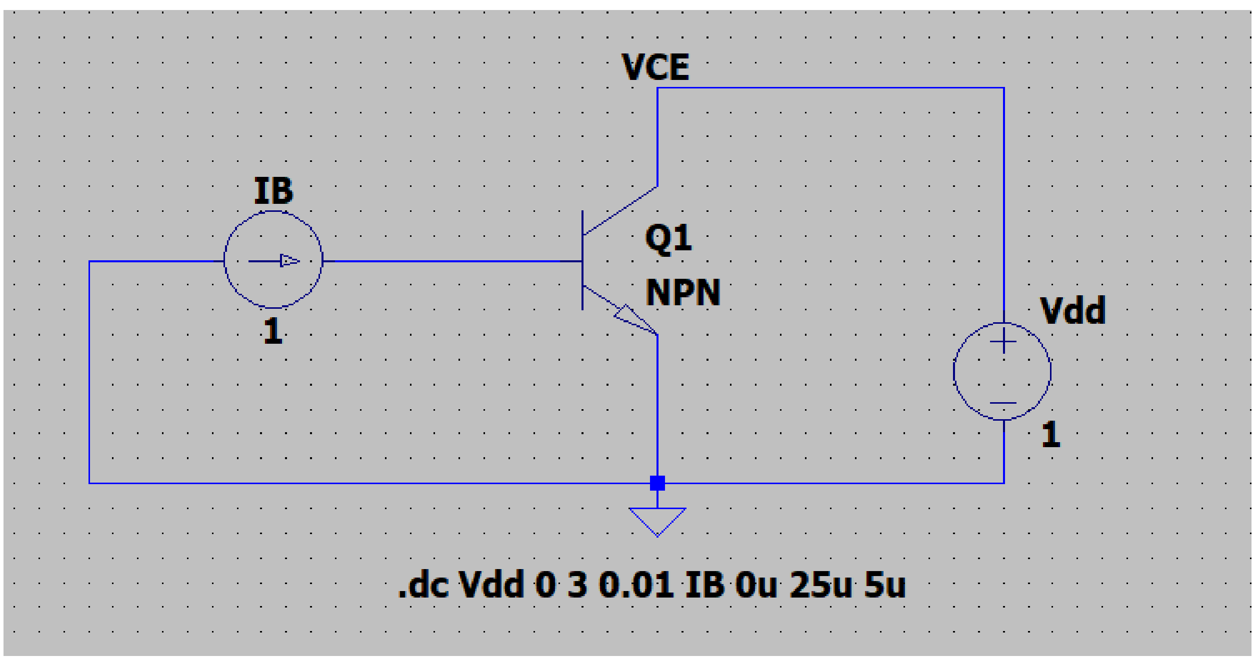
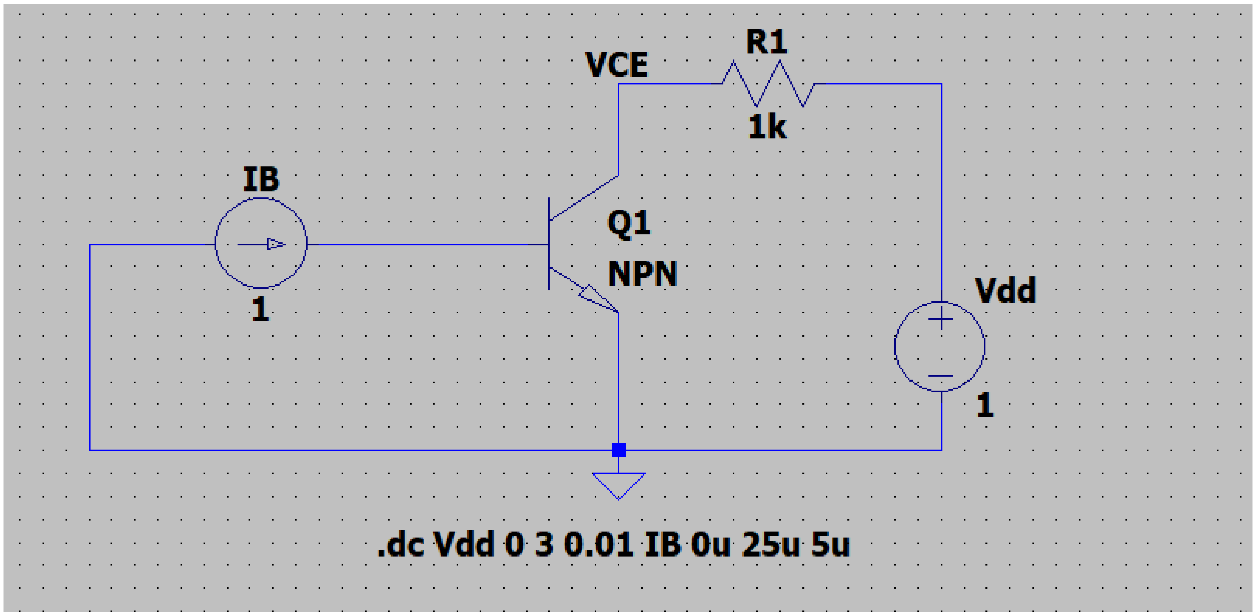
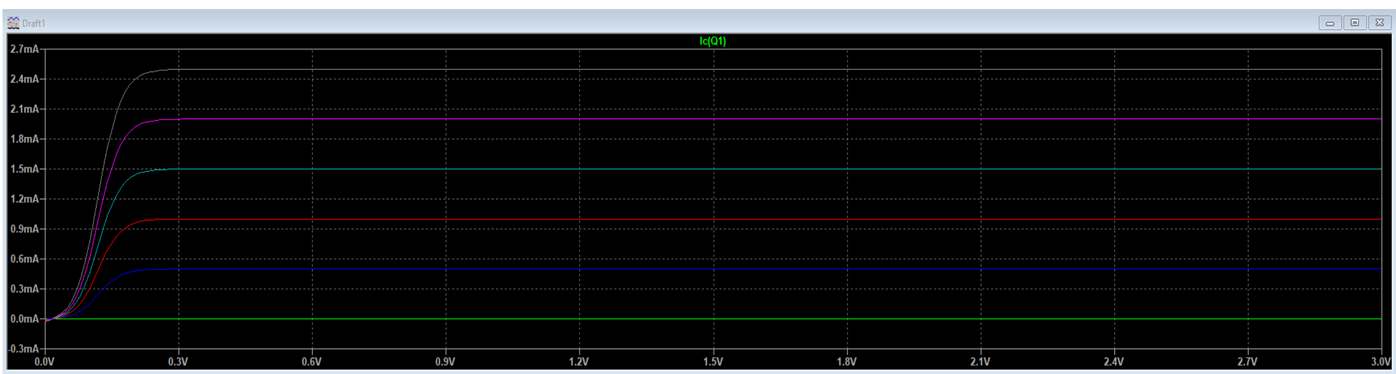


Diagram 2:

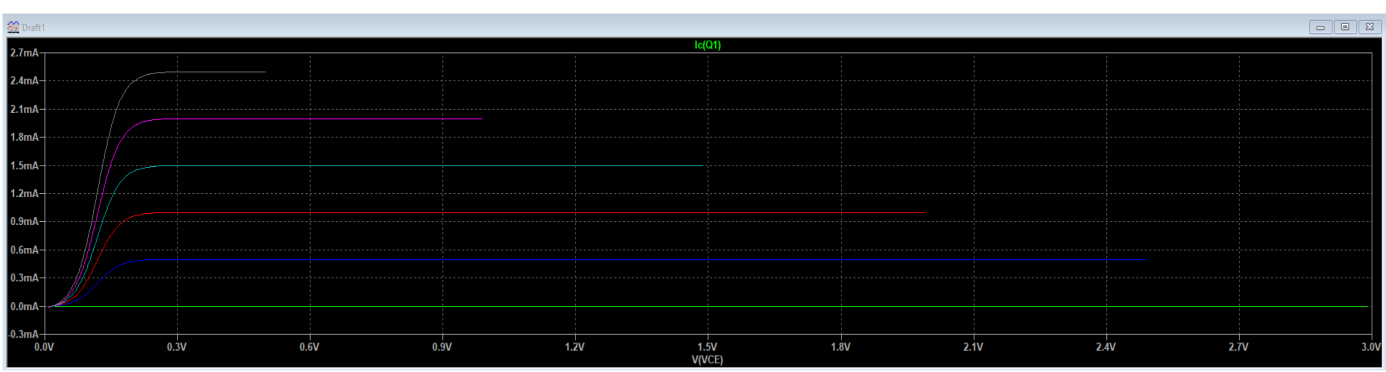


6. Plots Generated in LT spice simulation:

Plot 01:



Plot 2:



7. Discussion:

IC varies with changes in Vce while IB is held constant, as seen by the I-V characteristics produced from the datasets of the hardware experiment of circuit 1. We can observe from the graph that it was created that the collector current starts off rapidly increasing until becoming almost constant. Three regions can be identified on this graph: When Vce is increased by a specific amount and the output current stays the same, this region is known as the active region. Second, the saturation region, where IC rapidly increases from 0 to the active region. Third is the Cut-off Region, where there is almost no current. The output I-V characteristics show that, in the active region, IC increases with an increase in IB if VCE is maintained constant. In fact, the relationship between IC and IB in active mode is linear, and the following equation can be used to illustrate it: $IC = \beta IB$.

In the second plot of the Lt spice diagrams, we could notice that the Ic (collector current) was not reaching the end of Vce in the plot. We know that, Vce= Vdd - Ic*Rc. Hence, when Ib is increased Ic also increases as Ib initially passes through the BJT to provide collector current. Hence, Vce decreases due to more Ic. In the same way, when Ib is decreased, Ic is also decreased. Hence, in that case, Vce is increased. However, after a time we cannot reach our collector current for a higher Vce as it keeps decreasing.

We noticed some of the discrepancies in the hardware experiment such as some values we measured were not theoretically accurate. For some of the inputs, we measured Vce and Vrc which were not theoretically accurate. Although our final graph generated after smoothing out looked correct yet some of the data were faulty due to the human and hardware errors we usually see in hardware experiments. As per precautions, we were careful about how much voltage we were giving as input so that no device gets harmed in the process.