CSE460 Handout (Summary 2024)

Exam schedule (tentative)

Exam	Time	Date	Syllabus*	COs
Quiz 1	3rd Week	[TBA]	Lecture 1-3	*CO1*
Quiz 2	4th Week		Lecture 5-6	*CO1*
Quiz 3	6th Week		Lecture 8-10	*CO2*
Midterm	***7th Week***		***Lecture 1-10***	*CO1, CO2*
Quiz 4	10th or 11th Week	[TBA]	Lecture 13-16	*CO4*
Quiz 5	12th or 13th Week		Lecture 17- 20	*CO1*
Final	***14th Week***	***May 02, 2024***	***Lecture 11-20***	*CO1, CO3, CO4*

*Follow course timeline

Marks distribution

Theory/Lab	Assessment	Percentage	Total number of assessments	Number of assessment to be graded
Theory (75%)	Attendance	**-**	-	70% (90%+ for lab) or more to be eligible for Final Exam
	Assignment	**10%**	4	Best 3 (n-1)
	Quiz*	**15%**	5 (n)	Best 4 (n-1)
	Midterm	**20%**	1	1
	Final	**30%**	1	1
Lab (25%)	Lab Report	**5%**	1-2	All
	Lab Performance	**10%**	6-7 (n)	Best 5-6 (n-1)
	Lab-test	**10%**	2	2

*The last quiz (n^{th} quiz) will be considered as make-up for any missed quiz (maximum of 1), whatever the reason. **No other make-up quizzes will be taken.**
Make-Up Lab Policy: No make-up of lab will be considered without **valid reason.**

Theory Class Schedule

Section	Faculty	Day	Schedule	Room
1	PMD	SAT, THU	08:00 AM-09:20 AM	12F-32L
2	KFP	SAT, THU	09:30 AM-10:50 AM	12F-32L
3	PMD	SAT, THU	11:00 AM-12:20 PM	12F-31L
4	KFP	SAT, THU	12:30 PM-01:50 PM	12F-32L
6	YAR	SAT, THU	03:30 PM-04:50 PM	09B-10L
7	HAD	SUN, TUE	03:30 PM-04:50 PM	12F-31L
8	AGS	MON, WED	08:00 AM-09:20 AM	12F-31L

Lab Schedule and Status

Section	Faculty	Day	Schedule	Room	Lab Executed
1	ABY, HAD	SUN	08:00 AM-10:50 AM	12F-32L	LAB1 (DSCH2)
2	ABY, AGS	SUN	11:00 AM-01:50 PM	12F-32L	LAB1 (DSCH2)
3	KFP, ABY	MON	11:00 AM-01:50 PM	12F-31L	**LAB1 (DSCH2)**
4	BRH, PMD	TUE	11:00 AM-01:50 PM	12F-32L	LAB1 (DSCH2)
6	PMD, BRH	WED	02:00 PM-04:50 PM	09B-10L	**LAB1 (DSCH2)**
7	PMD, BRH	THU	02:00 PM-04:50 PM	12F-31L	**LAB1 (DSCH2)**
8	YAR, ABY	SAT	08:00 AM-10:50 AM	12F-31L	**LAB1 (DSCH2)**

Theory Faculties

Initial	Name	BRACU Email
HAD	Shadman Shahid	ext.shadman.shahid@bracu.ac.bd
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Lab Faculties

Initial	Name	BRACU Email
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BRH	Beig Rajibul Hasan	rajib.hasan@bracu.ac.bd

Lab softwares

- **dsch2**
  Download link:
  https://drive.google.com/drive/folders/1xwzh8gbnfAvQBYRBd9xDs20lFbyK6SlJ?usp=sharing (For experiments: 1)
- **Quartus**
  Download link:
  https://drive.google.com/drive/folders/1VVXijpn4d9LY4PS-Q_dAKXCU8q9xoESm?usp=sharing (For experiments: 2, 3,4,5)
- **Microwind**
  Download link:
  https://drive.google.com/drive/folders/11xGLeyzWkfMV4nPgUqLjLi4eXAZVs7WM?usp=sharing (For experiments: 6)
- Jupyter Notebook / Google Colab (For experiments: 7)

Communication platform

CSE460 Summer '24 Official Discord Server: https://discord.gg/SKWWkFet

Textbooks

- **[Weste&Harris]** CMOS VLSI Design A Circuit and Systems Perspective 4e - Weste, Harris: http://library.lol/main/51BD9C7E9E62DF12B1122C9B874DBFAC
  [*Solution manual is also available online*]
- **[Brown&Vranesic]** Fundamentals of Digital Logic with Verilog Design 3e - Stephen Brown, Zvonko Vranesic:
  http://library.lol/main/7084609A715D3C56A468C66D66DD1019
  [*Solution manual is also available online*]
- **[Andrew,Jens,Igor&Jin]** VLSI Physical Design: From Graph Partitioning to Timing Closure 1e - Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu:
  https://theswissbay.ch/pdf/Gentoomen%20Library/Misc/Summerer%20-%20VLSI%20Physical%20Design.pdf
- [Naveed A. Sherwani] Algorithms for VLSI Physical Design automation (third edition)
  https://drive.google.com/file/d/1zN8dcQeKMQdQj-ejm17JCRlWwx58VpfZ/view?usp=share_link
- ***Chapter wise topic lists from the Books-***
  https://drive.google.com/file/d/1nVr_EWHiICuEubedRChEcz0Y9VqXNJEx/view?usp=share_link

Practice problems sheet

After watching/attending the lectures and reading the corresponding texts, try to solve the following problems:

Week-wise Practice Problems:CSE460: VLSI Design Practice Problems for Exam (Fall 2023)
Solution Manual for Practice Problems: [Answer_Sheet]

**[*The problems are compiled from the corresponding reading sections' solved example problems or exercises.*]
****The final questions in the exam will be conceptual & analytical (theoretical and problem-solving).**

Course timeline

Week	Event	Details/Syllabus	Reference	Slide	BuX Video Link
1 [May 28 - May 30]	Theory(1): Week 1 Lecture 1	Introduction to VLSI	[Weste&Harris] Chapter 1 1.1 A Brief History	CSE4…	1. Course Content 2. The transistor concept 3.History and basic transistor 4.MOSFETs: A closer look 5.Moore's Law 6.Design abstraction and methodologies
2 [June 1 - June 6]	**Lab:** Experiment 1	CMOS Schematic Circuit Design in DSCH2	CSE 460 Expe…		1.CSE 460 Experiment 4 Part 1 : Introduction to DSCH2 2.CSE 460 Experiment 4 Part 2 : DSCH2 Example - CMOS Inverter 3.CSE 460 Experiment 4 Part 3 : DSCH2 Example - F= AB+CD 4.CSE 460 Experiment 4 Part 4 : DSCH2 Example - NAND gate 5.DSCH2 Example - D latch 6.DSCH2 Example D Flip Flop
	Theory(2): Week 2 Lecture 1	- Review of digital electronics - Logic gates in CMOS	[Brown&Vranesic] Chapters 2, 4, 5 2.4 Logic Gates and Networks [Full, up to Functionally Equivalent Networks] 2.3 Boolean Algebra: Axioms of Boolean Algebra, Examples: 2.3, 2.4 4.1 Multiplexers [up to example 4.1(included)] 5.3 Gated D Latch [Full, 5.3.1 will be covered in future] 5.4.1 Master-Slave D	CSE4…	1.Review of logic gates 2.Logic function synthesis (SOP, POS, K-maps) 3.Review of MUX 4.Review of Mux, Decoder and Encoder (optional) 5.Review of D latch 6.Review of D flip-flop 7.Level triggered vs. Edge triggered

			Flip-flop [Full]		
	Theory(3): Week 2 Lecture 2	Implementation of logic blocks and sequential elements in CMOS technology	[Weste&Harris] Chapter 1 1.3 MOS Transistors (full) 1.4 CMOS Logic (1.4.1-1.4.5)	CSE4…	1. 460 L3 P1 2. nMOS and pMOS operation 3. CMOS logic gate general structure: part 1 4.CMOS logic gate general structure: part 2 5.Example 1 6.Example 2 7.Example 3
3 [Jun 8 - Jun 13]	**Lab**: Experiment 2	Introduction to Verilog; Verilog Design Part 1 (combinational logic)	Altera Quartus … CSE 460 Expe…	CSE4…	
	Theory(4): Week 3 Lecture 1	CMOS Implementation	[Weste&Harris] Chapter 1 1.4 CMOS Logic (1.4.6-1.4.9)	CSE4…	1.nMOS and pMOS as pass transistors 2.CMOS Transmission gates 3.CMOS Tristate buffers and inverters 4.CMOS Multiplexers 5.CMOS D Latch 6.CMOS D Flip-flop
	Theory(5): Week 3 Lecture 2	CMOS transistor theory	[Weste&Harris] Chapter 2 2.1 Introduction 2.2 Long-channel I-V Characteristics	CSE4…	1.MOS Operating modes 2.nMOS Regions of operation 3.nMOS I-V Characteristics derivation: part 1 4.nMOS I-V Characteristics derivation: part 2 5.MOSFET I-V Characteristics Summary
4 [Jun 22 - Jun 27]	**Lab**: Experiment 3	Verilog Design Part 2 (sequential logic)	CSE 460 Expe…	CSE4…	

	Theory(6): Week 4 Lecture 1	CMOS transistor theory	[Weste&Harris] Chapter 2 2.2 Long-channel I-V characteristics Example 2.1 2.3.1 Simple MOS capacitance models + mathematical problem solving	CSE4… CSE4…	1.nMOS & pMOS I-V Characteristics Summary 2.Example 1 3.Example 2 4.Example 3 5.Gate and diffusion capacitance
	Theory(7): Week 4 Lecture 2	DC response of CMOS inverter	[Weste&Harris] Chapter 2 2.5 DC Transfer Characteristics 2.5.1 Static CMOS Inverter DC Characteristics 2.5.2 Beta Ratio Effects 2.5.4 Pass Transistor DC Characteristic	CSE4…	1.DC Response 2.CMOS Inverter DC Response Derivation 3.DC Response Practical Considerations 4.
5 [Jun 29 - Jul 4]	**Lab Test**	Experiment 1 - Experiment 3 CSE 460 Experiment 4 (Verilog 3) Fall22 [AHB]… CSE460 Lab-4 FSM.pptx			
	Theory(8): Week 5 Lecture 1	Introduction to system design using finite state machines	[Brown&Vranesic] Chapter 6 6.1 Basic Design Steps [Brown&Vranesic] Chapter 6 Example 6.1 [full]	CSE4… CSE4…	
	Theory(9): Week 5 Lecture 2	System design using moore and mealy type finite state machines (FSM1)	[Brown&Vranesic] Chapter 6 Section 6.2, 6.2.1 [Full], 6.3 Mealy State Model [full] Example 6.2, 6.4	CSE4…	
6 [Jul 6 - Jul 11]	**Lab**: Experiment 4	Verilog Design Part 3 (FSMs)		CSE4…	
	Theory(10): Week 6 Lecture 1	System design using moore and mealy type finite state machines (FSM2)	[Brown&Vranesic] Chapter 6 Section 6.2, 6.2.1 [Full], 6.3 Mealy State Model [full] Example 6.2, 6.4	CSE4…	
	Theory(11)	Reserved			

7	**Midterm exam**	**Lecture 1 - Lecture 10**			
8 [Jul 22 - Jul 25]	**Lab**: Experiment 5	Verilog Design Part 4 (FSMs)		CSE4…	
	Theory(12): Week 8 Lecture 1	Fabrication of CMOS devices	[Weste&Harris] Chapter 1 1.5 CMOS Fabrication and Layout (1.5.1-1.5.3)	CSE4…	
9 [Jul 22 - Jul 25]	**Lab**: Experiment 6	CMOS Layout Design in Microwind	CSE 460 Expe…		
	Theory(13): Week 9 Lecture 1	Layouts and stick diagrams	[Weste&Harris] Chapter 1 1.5.5 Stick Diagrams (Full + Example 3)	CSE4… CSE4…	
	Theory(14): Week 9 Lecture 2	1. Physical Design	https://nmsu.zoom.us/rec/share/wO2p7vq3qyfhb1mMELK3d3pliaasuQRWnf649-ric_qXzLSd2Ci1GjXtZio8Kze7.DihKIAL49_UpAWnr	CSE4…	
10 [Jul 27 - Jul 31]	**Lab**: Experiment 7	Algorithm implementation using Python	TBA		
	Theory(15): Week 10 Lecture 1	Physical Design (algorithm 1)	Video URL: https://nmsu.zoom.us/rec/share/wO2p7vq3qyfhb1mMELK3d3pliaasuQRWnf649-ric_qXzLSd2Ci1GjXtZio8Kze7.DihKIAL49_UpAWnr	CSE4…	
	Theory(16): Week 10 Lecture 2	Physical Design (algorithm 2)	Lecture note	CSE4…	
11 [Aug 3 - Aug 8]	**Lab: No lab**				
	Theory(17): Week 11 Lecture 1	Delay in CMOS circuits(Part1)	[Weste&Harris] Chapter 4 4.2 Transient Response 4.3 RC Delay Model	CSE4…	

			4.3.1 Effective Resistance 4.3.2 Gate and Diffusion Capacitance 4.3.3 Equivalent RC Circuits		
	Theory(18): Week 11 Lecture 2	Delay in CMOS circuits(Part2)	[Weste&Harris] Chapter 4 4.3.5 Elmore Delay Example 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9	CSE4…	
12 [Aug 10 - Aug 14]	**Lab**: Presentation	Paper presentation			
	Theory(19): Week 12 Lecture 1	Power in CMOS circuits	[Weste&Harris] Chapter 5 5.1.1 Definitions 5.1.2 Examples 5.1.3 Sources of Power Dissipation Example 5.1	CSE4… CSE4…	
	Theory(20): Week 12 Lecture 2	Power in CMOS circuits (Continued)		CSE4…	
13 [Aug 17 - Aug 22]	Lab	Reserved			
	Theory(21)	Reserved			
14 [Aug 24 - Aug 29]	Lab	Reserved			
	Theory(22)	Reserved			
14	**Final exam**	**Lecture 11 - Lecture 20**			

Course contents

Detailed List of Topics

1. **Week 1**
   - Introduction to VLSI, history, timeline. Moore's law.
   - Review of digital logic design. Complete VLSI flow (top down / bottom up)

2. **Week 2**
   - Logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs.
   - Combinational logic circuit design using CMOS. Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates.
   - Multiplexers, encoder, latch, flip-flops using CMOS

3. **Week 3**
   - CMOS transistor theory

4. **Week 4**
   - DC Response of CMOS gates. Pass transistors. Logic levels and noise margins. DC transfer characteristics.
   - FSM Introduction
   - FSM moore and mealy type machines
   -

5. **Week 5**
   - System design using moore and mealy type finite state machines
   - Different hardware implementation techniques
6. **Week 6**
   - CMOS Transistor theory: modes of operation. Derivation of I-V characteristics. MOS Capacitance.

7. **Week 7**
   - Midterm week

8. **Week 8**
   - CMOS Fabrication: Inverter cross-section and layout analysis.
   - Layout
   - Masks. Stick diagrams and area estimation. (Eulerian path. Complex examples)

9. **Week 9, 10**
   - Physical design: floorplanning, partitioning, routing, clock tree synthesis.
   - KL algorithm for partitioning.
   - Lee's maze algorithm for global routing

10. **Week 11**
    - Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance. MOS Capacitance.
    - Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons
11. **Week 12**
    - CMOS Power: Instantaneous and Average power, Energy. Power in circuit elements analysis (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling.