① Inverter E

$$E_{source} = C V_{DD}^{2}$$

② Capacitor

$$E_{charge} = \frac{1}{2} C V_{DD}^{2}$$

$$E_{discharge} = -\frac{1}{2} C V_{DD}^{2}$$

③ Activity factor

$$\alpha = \frac{F_{sw}}{F_{clock}}$$

④ Power of inv switching

$$P_{switch} = \frac{E}{}$$

T_{sw}

$$P_{sw} = \alpha F_{clock} C V_{DD}^2$$

⑤ Metrics:

$1\,MHz = 10^6\,Hz$

$1\,GHz = 10^9\,Hz$

$1\,nF = 10^{-9}\,F$

$1\,fF = 10^{-15}\,F$

$1\,pF = 10^{-12}\,F$

$1B = 10^9$, $1T = 10^{12}$

$1M = 10^6$

$1\,nm = 10^{-9}\,m$

$1\,um = 10^{-6}\,m$

VLSI Algo

(1) PPA — Power Performance Area

(2) Physical Design:

(i) Partitioning (create blocks)

(ii) floorplan : block place

- 2's sum = 1's other

(iii) placement : gates

a) Global

b) Detailed

(IV) signal routing : wire

a) golal (b) Detailed

(V) Clock tree synthesis CTS
- add delay to match gates

(VI) Timing closure : wait

(VII) Partioning terminology :
- node - gate
- module block

Lees Algo

(1) routing region → where route

② sequential routing → one by one

③ concurrent routing → all

④ rule of thumb → no bend

Power formula prove

① $P = VI$ ② $E = Pt$

$= VIt$

Now,

$$dE = P\,dt$$

$$E = \int_0^{V_{DD}} VI\,dt$$

$$= \int_0^{V_{DD}} V \cdot C\frac{dV}{dt}\,dt$$

$$= C\int_0^{V_{DD}} V\,dV$$

$$= \frac{1}{2} C V^2$$

Now,

$$E_{source} = CV \int_0^{V_{DD}} 1 \, dV$$

$$= CV^2$$

Now,

$$P_{sw} = \frac{E}{T_{sw}} = f_{sw} E$$

$$= f_{sw} C V_{DD}^2$$

$$= \alpha F C V_{DD}^2$$

$$\alpha = \frac{f_{sw}}{f_c}$$

$$\Rightarrow f_{sw} = \alpha f_c$$