Advanced Computer-Aided VLSI System Design
Homework 4 Report

Due Tuesday, May 27, 13:59

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Student Name:

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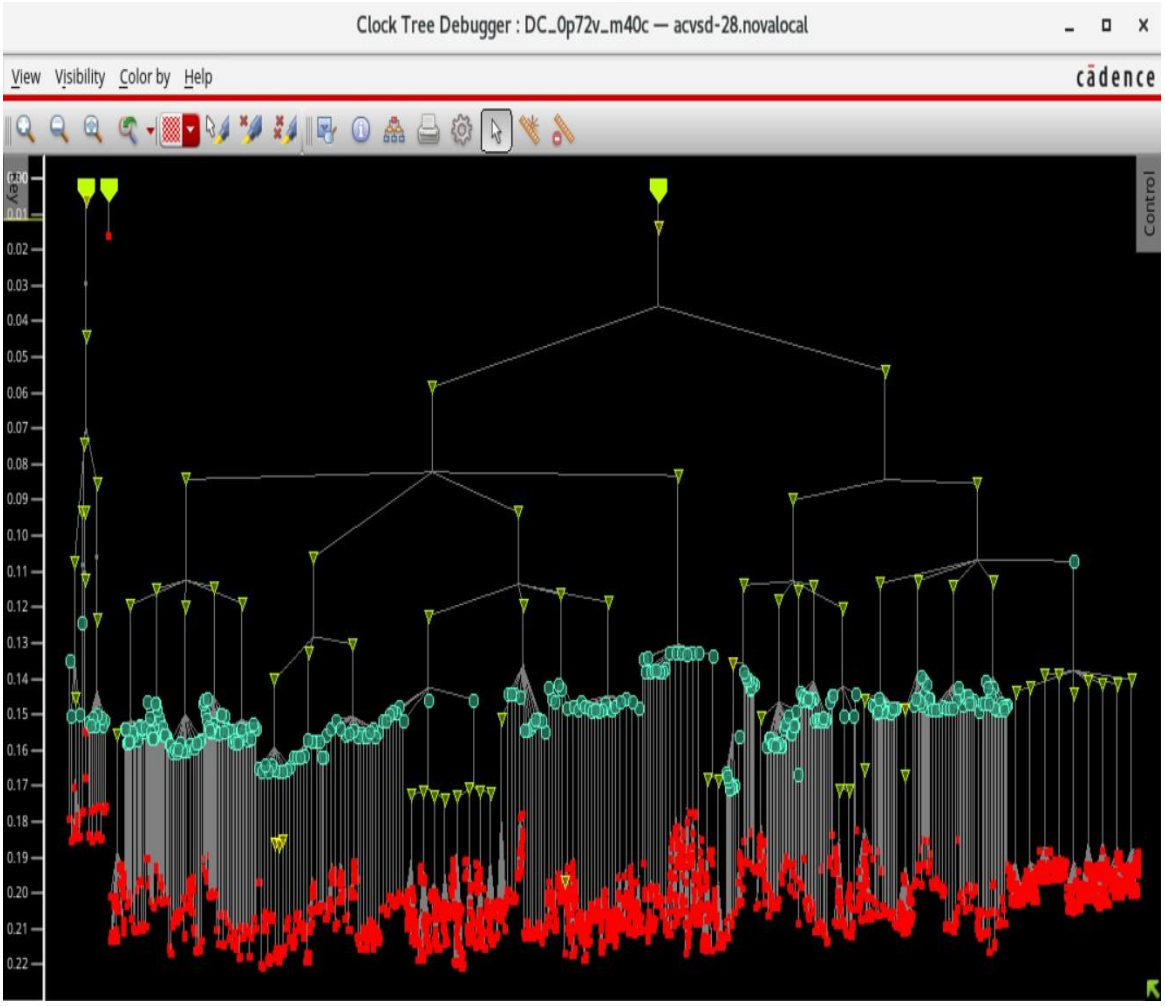
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	174650.27
	Core Area (um^2)	66505.02

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 2598.0) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.072 0.000 28.344 28.272} 1 of 484
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {28.344 0.000 56.616 28.272} 2 of 484
 VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {56.616 0.000 84.888 28.272} 3 of 484
 VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {84.888 0.000 113.160 28.272} 4 of 484
 VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {113.160 0.000 141.432 28.272} 5 of 484
 VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {141.432 0.000 169.704 28.272} 6 of 484
 VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {169.704 0.000 197.976 28.272} 7 of 484
 VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {197.976 0.000 226.248 28.272} 8 of 484
 VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {226.248 0.000 254.520 28.272} 9 of 484
 VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
```

```
VERIFY DRC ..... Sub-Area: {197.976 593.712 226.248 613.632} 470 of 484
VERIFY DRC ..... Sub-Area : 470 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {226.248 593.712 254.520 613.632} 471 of 484
VERIFY DRC ..... Sub-Area : 471 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {254.520 593.712 282.792 613.632} 472 of 484
VERIFY DRC ..... Sub-Area : 472 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {282.792 593.712 311.064 613.632} 473 of 484
VERIFY DRC ..... Sub-Area : 473 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {311.064 593.712 339.336 613.632} 474 of 484
VERIFY DRC ..... Sub-Area : 474 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {339.336 593.712 367.608 613.632} 475 of 484
VERIFY DRC ..... Sub-Area : 475 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {367.608 593.712 395.880 613.632} 476 of 484
VERIFY DRC ..... Sub-Area : 476 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {395.880 593.712 424.152 613.632} 477 of 484
VERIFY DRC ..... Sub-Area : 477 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {424.152 593.712 452.424 613.632} 478 of 484
VERIFY DRC ..... Sub-Area : 478 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {452.424 593.712 480.696 613.632} 479 of 484
VERIFY DRC ..... Sub-Area : 479 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {480.696 593.712 508.968 613.632} 480 of 484
VERIFY DRC ..... Sub-Area : 480 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {508.968 593.712 537.240 613.632} 481 of 484
VERIFY DRC ..... Sub-Area : 481 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {537.240 593.712 565.512 613.632} 482 of 484
VERIFY DRC ..... Sub-Area : 482 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {565.512 593.712 593.784 613.632} 483 of 484
VERIFY DRC ..... Sub-Area : 483 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {593.784 593.712 614.322 613.632} 484 of 484
VERIFY DRC ..... Sub-Area : 484 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:04:03  ELAPSED TIME: 243.00  MEM: 93.0M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue May  6 11:53:58 2025

Design Name: CHIP
Database Units: 2000
Design Boundary: (0.0720, 0.0000) (614.3220, 613.6320)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 11:53:58 **** Processed 5000 nets.
**** 11:53:58 **** Processed 10000 nets.
**** 11:53:58 **** Processed 15000 nets.
**** 11:53:58 **** Processed 20000 nets.
**** 11:53:58 **** Processed 25000 nets.
*** 11:53:58 *** Building data for Net VDD
*** 11:54:00 *** Building data for Net VSS

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue May  6 11:54:01 2025
Time Elapsed: 0:00:03.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:03.2  MEM: 283.836M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------------

Setup views included:
 AV_func_0p72v_m40c AV_func_0p72v_125c

+--------------------+---------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg |reg2cgate| in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.000  |  0.002  |  0.002  |  0.004  |  0.000  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  7583   |  6003   |  1431   |   189   |   56    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 51.293%
Total number of glitch violations: 0
------------------------------------------------------------------
```

```
------------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------------

Hold views included:
 AV_func_0p88v_m40c AV_scan_0p88v_m40c AV_scan_0p88v_125c

+--------------------+---------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg |reg2cgate| in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.001  |  0.001  |  0.002  |  0.001  |  0.135  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  13649  |  12070  |  1431   |   188   |   56    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+---------+

Density: 51.293%
------------------------------------------------------------------
```

4. Show the critical path after post-route optimization. What is the path type? (5%)

   Through command：**`report_timing -max_path 1`**

   (The slack of the critical path should match the smallest slack in the timing report)

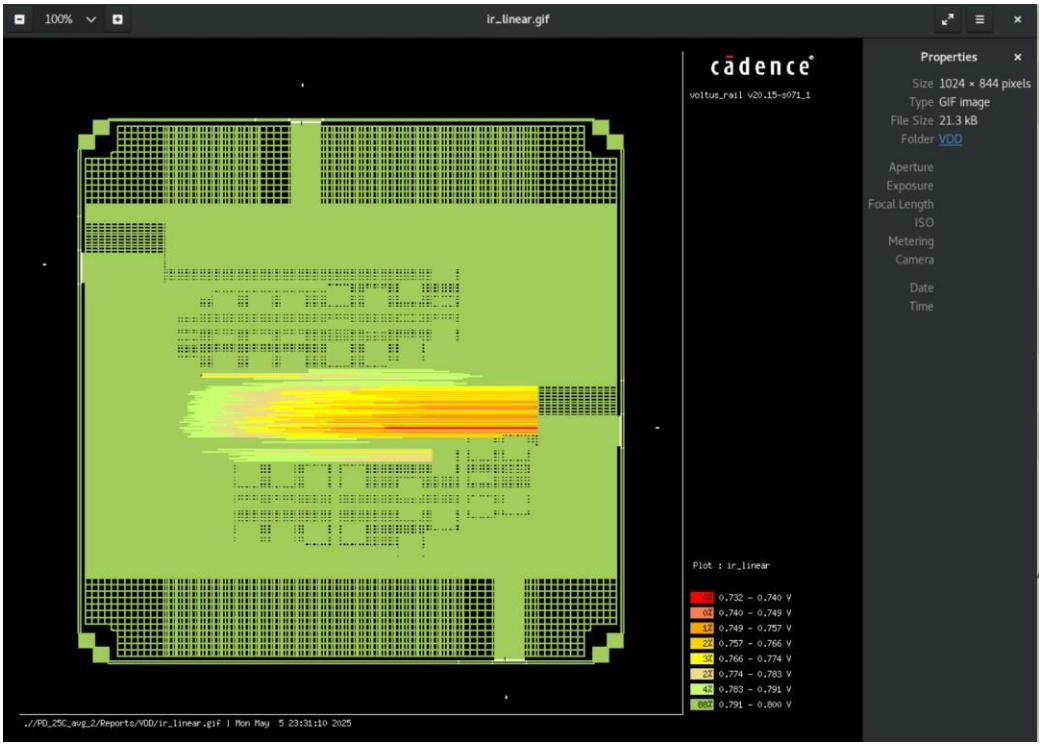
```
Path 1: MET Late External Delay Assertion
Endpoint:   awaddr[11]                      (v) checked with  leading edge of
'clk_ram'
Beginpoint: AW_FIFO/U1/U2/count_int_reg_0_/Q (^) triggered by  leading edge of
'clk_ram'
Path Groups: {reg2out}
Analysis View: AV_func_0p72v_125c
Other End Arrival Time          0.000
- External Delay                0.000
+ Phase Shift                   0.500
+ CPPR Adjustment               0.000
- Uncertainty                   0.100
= Required Time                 0.400
- Arrival Time                  0.400
= Slack Time                    0.000
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.180
     = Beginpoint Arrival Time       0.180
     +-------------------------------------------------------------------------------------------------------+
     |              Instance              |     Arc      |        Cell         | Delay | Arrival | Required |
     |                                    |              |                     |       |  Time   |   Time   |
     |------------------------------------+--------------+---------------------+-------+---------+----------|
     | AW_FIFO/U1/U2/count_int_reg_0_     | CP ^         |                     |       |   0.180 |    0.180 |
     | AW_FIFO/U1/U2/count_int_reg_0_     | CP ^ -> Q ^  | SDFCNQD2BWP20P90LVT | 0.049 |   0.229 |    0.229 |
     | AW_FIFO/U1/U2/FE_OCPC713_rd_addr_0 | I ^ -> Z ^   | BUFFD12BWP16P90LVT  | 0.016 |   0.245 |    0.245 |
     | AW_FIFO/U2/FE_OCPC714_rd_addr_0    | I ^ -> Z ^   | BUFFD2BWP16P90LVT   | 0.022 |   0.267 |    0.267 |
     | AW_FIFO/U2/U7                      | B1 ^ -> ZN v | INR2D8BWP16P90LVT   | 0.007 |   0.274 |    0.274 |
     | AW_FIFO/U2/FE_OFC671_n124          | I v -> Z v   | BUFFD4BWP16P90LVT   | 0.030 |   0.305 |    0.305 |
     | AW_FIFO/U2/U64                     | A2 v -> ZN ^ | AOI22D1BWP16P90LVT  | 0.018 |   0.323 |    0.323 |
     | AW_FIFO/U2/U26                     | A3 ^ -> ZN v | ND4D1BWP16P90LVT    | 0.025 |   0.348 |    0.348 |
     | FE_OFC668_awaddr_11                | I v -> Z v   | BUFFD4BWP16P90LVT   | 0.030 |   0.377 |    0.377 |
     |                                    | awaddr[11] v |                     | 0.023 |   0.400 |    0.400 |
     +-------------------------------------------------------------------------------------------------------+
```

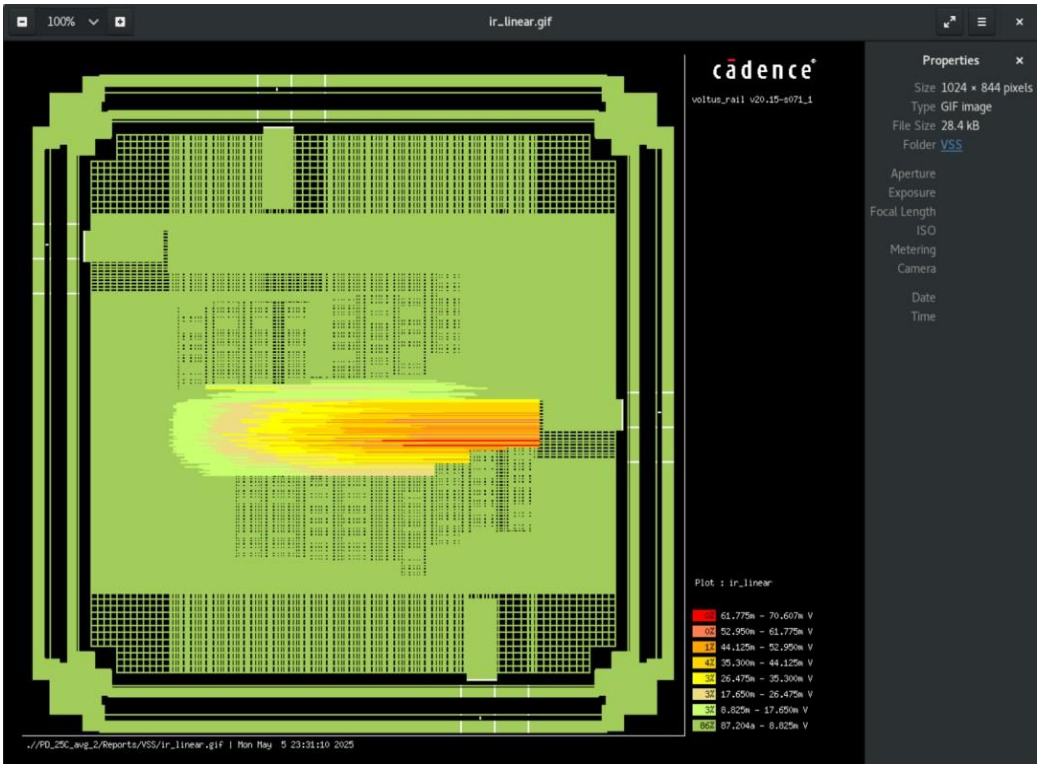
5. Attach the snapshot of GDS stream out messages. (5%)

```
Scanning GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds to register cell name ......
Scanning GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/GDS/N16ADFP_StdIO.gds to register cell name ......
Scanning GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/bondpad/N16ADFP_BondPad/GDS/N16ADFP_BondPad.gds to register cell name ......
Scanning GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/GDS/N16ADFP_SRAM_100a.gds to register cell name ......
Merging GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds ......
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds has version number: 600.
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds has units: 1000 per micron.
       ****** unit scaling factor = 1 ******
Merging GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/GDS/N16ADFP_StdIO.gds ......
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/GDS/N16ADFP_StdIO.gds has version number: 5.
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/GDS/N16ADFP_StdIO.gds has units: 1000 per micron.
       ****** unit scaling factor = 1 ******
Merging GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/bondpad/N16ADFP_BondPad/GDS/N16ADFP_BondPad.gds ......
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/bondpad/N16ADFP_BondPad/GDS/N16ADFP_BondPad.gds has version number: 5.
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/bondpad/N16ADFP_BondPad/GDS/N16ADFP_BondPad.gds has units: 1000 per micron.
       ****** unit scaling factor = 1 ******
Merging GDS file /share1/tech/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/GDS/N16ADFP_SRAM_100a.gds ......
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/GDS/N16ADFP_SRAM_100a.gds has version number: 5.
       ****** Merge file: /share1/tech/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/GDS/N16ADFP_SRAM_100a.gds has units: 1000 per micron.
       ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of IR drop result. (**Make sure IR drop < 8%**) (5%)
   Open **ir_linear.gif** under the path …/PD_25C_avg_x/VDD and VSS. Take the snapshot.

VDD / VSS

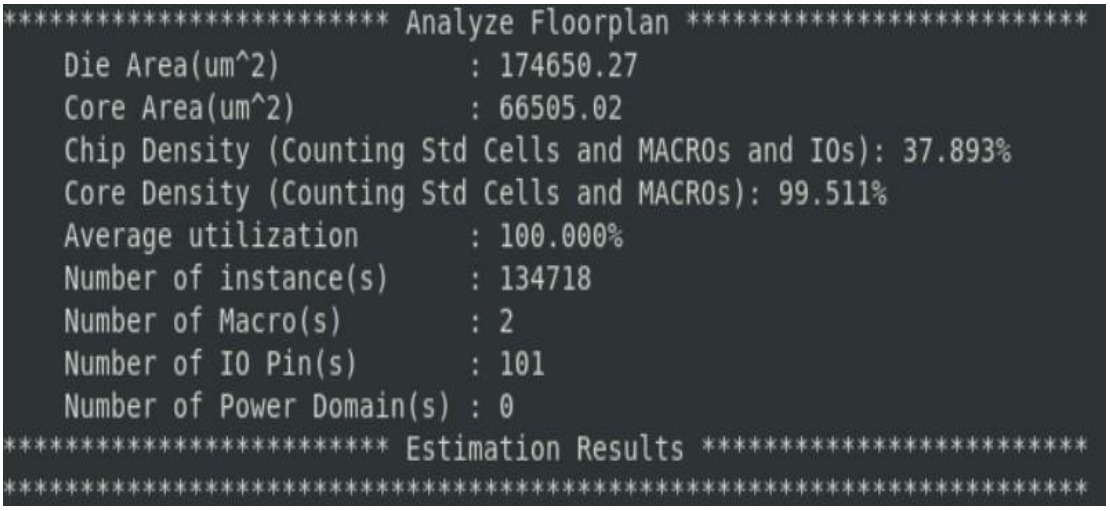




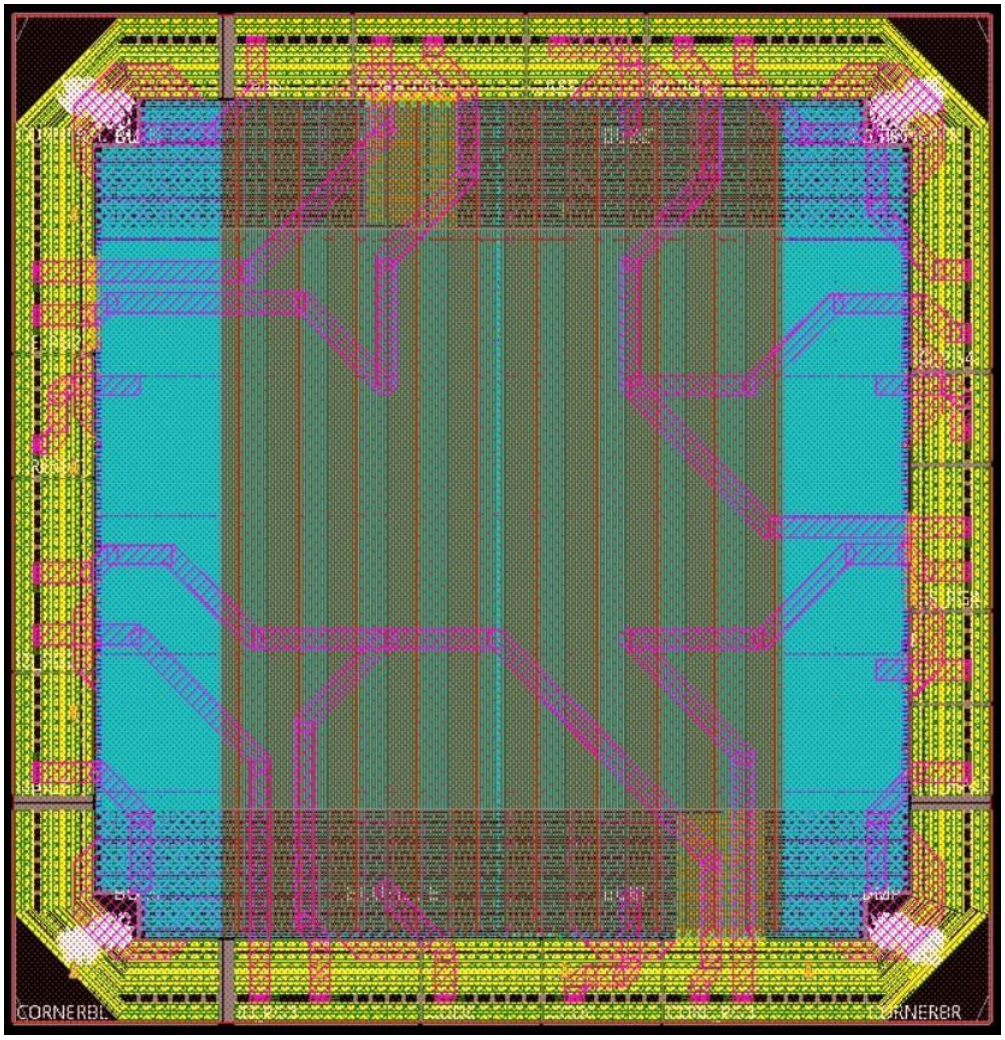
7. Attach the snapshot of the final area result. (5%)

   Through command：**`analyzeFloorplan`**

   (analyzeFloorplan destroys the design. Remember to save your design files first!!)



8. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (5%)



9. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   手動放在旁邊，繞線馬上繞過去，不佔用中間大面積繞線資源