Advanced Computer-Aided VLSI System Design
Homework 4: APR

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Data Preparation

1. Get the 1132_hw4.tar.gz with following command

```
cp /nfshome/acvsd010/1132_hw4.tar.gz .
```

2. Decompress 1132_hw4.tar.gz with following command

```
tar -zxvf 1132_hw4.tar.gz
```

Folder	File	Description
00_TESTBED	testfixture.v	Testbench for simulation w/o pad
00_TESTBED/ test_patterns	p*i*.dat	Input data (*i* = 0, 1, 2, 3, 4, 5)
00_TESTBED/ test_patterns	p*i*_golden.dat	Output golden (*i* = 0, 1, 2, 3, 4, 5)
00_TESTBED/axi	axi_ram.v	External memory
02_SYN/Netlist	top_syn.v	Synthesis netlist
02_SYN/Netlist	top_syn.sdc	Constraint for synthesis
02_SYN/Netlist	top-scan.def	Scan definition file
02_SYN/Netlist	top_syn.sdf	Timing info. from synthesis
03_GATE_PAD	03_run	Gate level simulation bash file
03_GATE_PAD	filelist.f	File list for gate level simulation
05_APR/lab_script	*.tcl	Scripts from APR Lab
05_APR/library/lef	*.tlef/*.lef	Technology/Physical Libraries
05_APR/library/lib	*.lib	Timing Libraries
05_APR/library/sram	*.lef/*.lib/*.gds	SRAM Libraries
06_POST	06_run	Post simulation bash file
06_POST	post_filelist.f	File list for post simulation

Introduction

In this homework, you should use Innovus to do P&R using the design in **Midterm with scan chain**. And try to add pad cell into netlist. You should modify the .sdc file and lab_scripts by yourself.

Pad Specifications

1. Pad cell name: PDCDG_V
2. You can refer to CHIP_syn.v in APR Lab to see how to add.
3. After adding pads, remember to modify the top module in testbench because the input/output ports are changed.
4. Make sure the modified Netlist pass every test pattern.

APR Specifications

1. Top module name: **top**
2. Follow mmmc.view from APR Lab to create the correct mmmc.view for this design
3. Add below command into top_syn.sdc to disable scan chain (port: test_se) for top_func.sdc and enable scan chain for top_scan.sdc

```
set_case_analysis...
```

   You can refer to CHIP_func.sdc and CHIP_scan.sdc in APR Lab to complete the command.
4. SRAM power pin name: VDDM, VSS
5. **For block design, Process related to IO Pad can be skip, but still need to create IO file**
6. **For block design, Process related to Power pad can be skip**
7. **For block design, Process related to Bump can be skip**
8. Process related to Early rail analysis can be skip
9. At least one power stripe in your design, but you should make sure IR drop < 8%
10. After finishing the APR, use below command to analyze the area (analyzeFloorplan destroys the design. Remember to save your design files first!!)

```
innovus #> analyzeFloorplan
```

11. Use below command to check the critical path

```
innovus #> report_timing -max_path 1
```

12. Remember to merge sram.gds when stream-out top.gds

13. **Review each script before execution, as some parts may require modification**

Design Description

1. Manually add pad cells into Netlist and rerun the gate level simulation
2. Perform place & route using Innovus.
3. Run simulation after APR
   - Remember to modify the name of .sdf file in your testbench.

Submission

1. Create a folder named **studentID_hw4**, and put all below files into the folder

```
r12943121_hw4
        ├─ 00_TESTBED
        │    └─ testfixture_pad.v (Testbench for modified netlist with pad cells)
        ├─ 03_GATE_PAD
        │    └─ top_syn_pad.v     (modified netlist with pad cells)
        └─ 05_APR
             ├─ top_func.sdc
             ├─ top_scan.sdc
             ├─ top.gds
             ├─ top_pr.v
             ├─ top_ss0p72vm40c.sdf
             ├─ mmmc.View
             ├─ final.enc         (APR design file)
             └─ final.enc.dat/    (APR design file data)
```

Note: Use **lower case** for the letter in your student ID. (Ex. r12943121_hw4)

2. Compress the folder **studentID_hw4** in a **tar file** named **studentID_hw4_v*k*.tar** (***k* is the number of version, *k* =1,2,…)**

```
tar -zcvf studentID_hw4_vk.tar.gz studentID_hw4
```

- TA will only check the last version of your homework.
- Place the tar.gz file at the root of your ADFP account
- Note: Use **lower case** for the letter in your student ID. (Ex. r12943121_hw4_v1)

3. Submit the report named **studentID_report.pdf** in NTU COOL
- Note: Use **lower case** for the letter in your student ID. (Ex. r12943121_report.pdf)

Grading Policy

1. TA will run your code as the commands in 03_run and 06_run. Make sure to run these commands with no error message for each test pattern.
2. APR report: **50%**
3. Correctness of simulation after adding pads: **10%**
4. Correctness of mmmc.view setting: **5%**
5. Correctness of top_func.sdc and top_scan.sdc setting: **5%**

6. Correctness of simulation after APR: **10%**
7. For Chip-level design with IO pads and bumps: **20%**
8. 5 points minus for any incorrect naming or submission format
9. No late submission, or 0 point for this homework