Computer-Aided VLSI System Design
Homework 5: APR

TA: 吳秉陞 r10943007@ntu.edu.tw **Due Tuesday, Dec. 5, 14:00**

Data Preparation

1. You would need related files below to finish APR
   (You can find all files under **/home/raid7_4/raid1_1/ PnR/SOCE_Lab/library**)
   - **design**
     A. Your core_syn.v from HW3
     B. Your core_syn.sdc from HW3
   - **celtic**
     A. slow.cdB
   - **Capacitance Table**
     A. tsmc013.capTbl
   - **tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **gds**
     A. tsmc13gfsg_fram.gds
     B. sram_*.gds (in sram_lef.zip)
   - **lef**
     A. tsmc13fsg_8lm_cic.lef
     B. antenna_8.lef
     C. sram_*.vclef (in sram_lef.zip)
     D. sram_*_ant.lef (in sram_lef.zip)
   - **lib**
     A. slow.lib
     B. sram_*_slow_syn.lib
   - streamOut.map

Introduction

In this homework, you should use Innovus to do P&R using your design in **HW3**. Note that the .sdc file are not provided to you. You should create them by yourself.

Specifications

1. Top module name: **core**
2. Only use worst case library for APR.
   - **AV_func_mode_max** for both **Setup Analysis View** and **Hold Analysis View**
3. Generate core_syn.sdc from synthesis stage by below command:

```
write_sdc Netlist/core_syn.sdc -version 1.8
```

4. Process related to IO Pad can be skip.
5. Process related to scan chain can be skip
6. At least one power stripe in your design.
7. Use below command to analyze the area
   (analyzeFloorplan destroys the design. Remember to save your design files first!!)

```
innovus #> analyzeFloorplan
```

8. Use below command to check the critical path

```
innovus #> report_timing -max_path 1
```

9. Remember to merge sram.gds when stream-out core.gds

Design Description

1. Perform place & route using Innovus.
2. Run simulation after APR
   - Remember to modify the name of .sdf file in your testbench.

Submission

1. Create a folder named **studentID_hw5**, and put all below files into the folder
   - **core_cts.sdc** (sdc file for clock tree synthesis)
   - **core.gds**
   - **core_pr.v**
   - **core_pr.sdf**
   - **mmmc.view**
   - **design.txt**
   - **report.pdf**

   Note: Use **lower case** for the letter in your student ID. (Ex. r07943001_hw1)

2. Compress the folder **studentID_hw5** in a **tar file** named **studentID_hw5_v*k*.tar** (***k* is the number of version, *k* =1,2,…)**

```
tar -cvf studentID_hw5_vk.tar StudentID_hw5
```

TA will only check the last version of your homework.

Note: Use **lower case** for the letter in your student ID. (Ex. d06943027_hw5_v1)

3. Submit to NTU COOL

Grading Policy

1. TA will run your code with following command. Make sure to run this command with no error message. (sram.v refers to sram applied in your design)

```
vcs testbench.v core_pr.v tsmc13_neg.v sram.v -full64 -R \
-debug_access+all +v2k +maxdelays -negdelay +neg_tchk +define+SDF+tb0
```

2. APR report: **60%**
3. Correctness of file submission: **10%**
4. Correctness of mmmc.view setting: **10%**
5. Correctness of simulation after APR: **20%**