Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 5, 14:00

Student ID:b09901081

Student Name:施伯儒

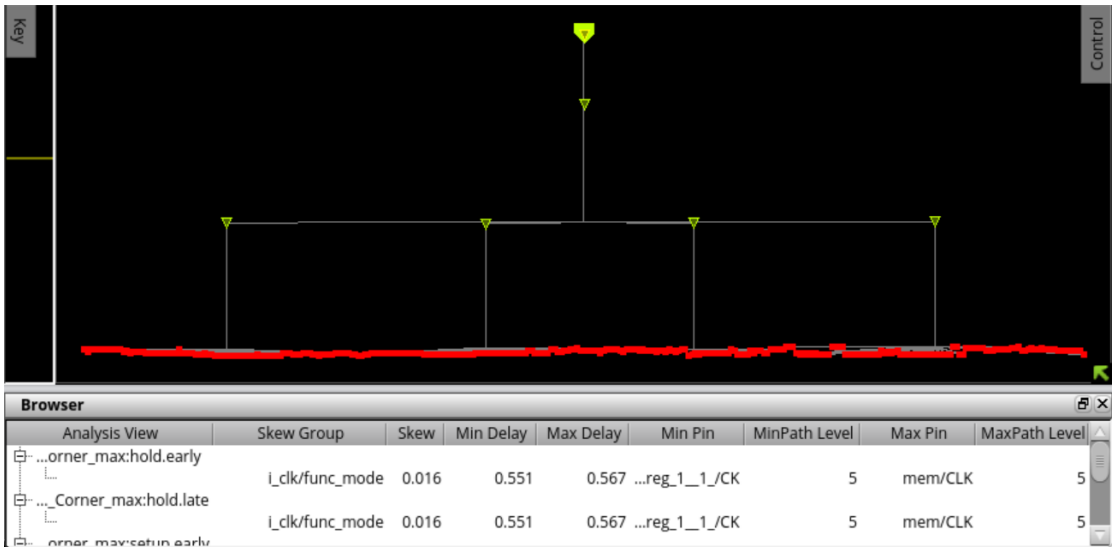
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	489062.43
	Core Area (um^2)	290445.51
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	5.00ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		From TA

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
  VERIFY DRC ..... Sub-Area: {530.400 0.000 699.200 176.800} 4 of 16
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 176.800 176.800 353.600} 5 of 16
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 176.800 353.600 353.600} 6 of 16
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 176.800 530.400 353.600} 7 of 16
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 176.800 699.200 353.600} 8 of 16
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 353.600 176.800 530.400} 9 of 16
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 353.600 353.600 530.400} 10 of 16
  VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 353.600 530.400 530.400} 11 of 16
  VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 353.600 699.200 530.400} 12 of 16
  VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 530.400 176.800 699.460} 13 of 16
  VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 530.400 353.600 699.460} 14 of 16
  VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 530.400 530.400 699.460} 15 of 16
  VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 530.400 699.200 699.460} 16 of 16
  VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

  Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.4  ELAPSED TIME: 1.00  MEM: 1.0M) ***
```

```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.4  MEM: 0.250M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no

timing violation (post-route). (5%)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.069  |  0.069  |  0.252  |  1.351  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.526  |  0.526  |  2.348  |  3.182  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 36.015%
```

4. Show the critical path after post-route optimization. What is the path type? (10%) (The slack of the critical path should match the smallest slack in the timing report)

   Path type: reg to reg

```
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.488
- Setup                         0.181
+ Phase Shift                   5.000
+ CPPR Adjustment               0.000
= Required Time                 5.306
- Arrival Time                  5.289
= Slack Time                    0.017
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.499
     = Beginpoint Arrival Time           0.499
     +-------------------------------------------------------------------------------+
     |    Instance     |       Arc       |    Cell     | Delay | Arrival | Required |
     |                 |                 |             |       |  Time   |   Time   |
     |-----------------+-----------------+-------------+-------+---------+----------|
     | mem             | CLK ^           |             |       |   0.499 |    0.516 |
     | mem             | CLK ^ -> Q[5] v | sram_4096x8 | 2.680 |   3.178 |    3.196 |
     | U4262           | A v -> Y ^      | NAND2X6     | 0.145 |   3.324 |    3.341 |
     | FE_DBTC65_n4684 | A ^ -> Y v      | INVX6       | 0.141 |   3.465 |    3.482 |
     | U2305           | B v -> Y v      | AND2X2      | 0.196 |   3.661 |    3.678 |
     | U4026           | A0 v -> Y v     | AO22X1      | 0.331 |   3.991 |    4.009 |
     | U3788           | AN v -> Y v     | NAND2BX2    | 0.180 |   4.171 |    4.189 |
     | U4171           | A v -> Y v      | AND3X2      | 0.185 |   4.357 |    4.374 |
     | U4824           | A1 v -> Y v     | OA21X4      | 0.238 |   4.595 |    4.612 |
     | U3611           | D v -> Y v      | AND4X1      | 0.264 |   4.859 |    4.876 |
     | U4064           | A0 v -> Y ^     | OAI32X1     | 0.187 |   5.046 |    5.063 |
     | U3827           | B ^ -> Y ^      | OR2X2       | 0.169 |   5.215 |    5.232 |
     | U3829           | B ^ -> Y v      | NAND3X1     | 0.074 |   5.289 |    5.306 |
     | psum_r_reg_17_  | D v             | DFFRX1      | 0.000 |   5.289 |    5.306 |
     +-------------------------------------------------------------------------------+
```

5. Attach the snapshot of GDS stream out messages. (10%)

```
Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file sram_lef/sram_4096x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file sram_lef/sram_4096x8.gds ......
        ****** Merge file: sram_lef/sram_4096x8.gds has version number: 5.
        ****** Merge file: sram_lef/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
Start to collect the design information.
Build netlist information for Cell core.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 81320 sites (138033 um^2) / alloc_area 81320 sites (138033 um^2).
Pin Density = 0.09721.
            = total # of pins 16633 / total area 171112.
************************** Analyze Floorplan **************************
    Die Area(um^2)              : 489062.43
    Core Area(um^2)             : 290445.51
    Chip Density (Counting Std Cells and MACROs and IOs): 53.654%
    Core Density (Counting Std Cells and MACROs): 90.345%
    Average utilization         : 100.000%
    Number of instance(s)       : 13963
    Number of Macro(s)          : 1
    Number of IO Pin(s)         : 33
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
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```
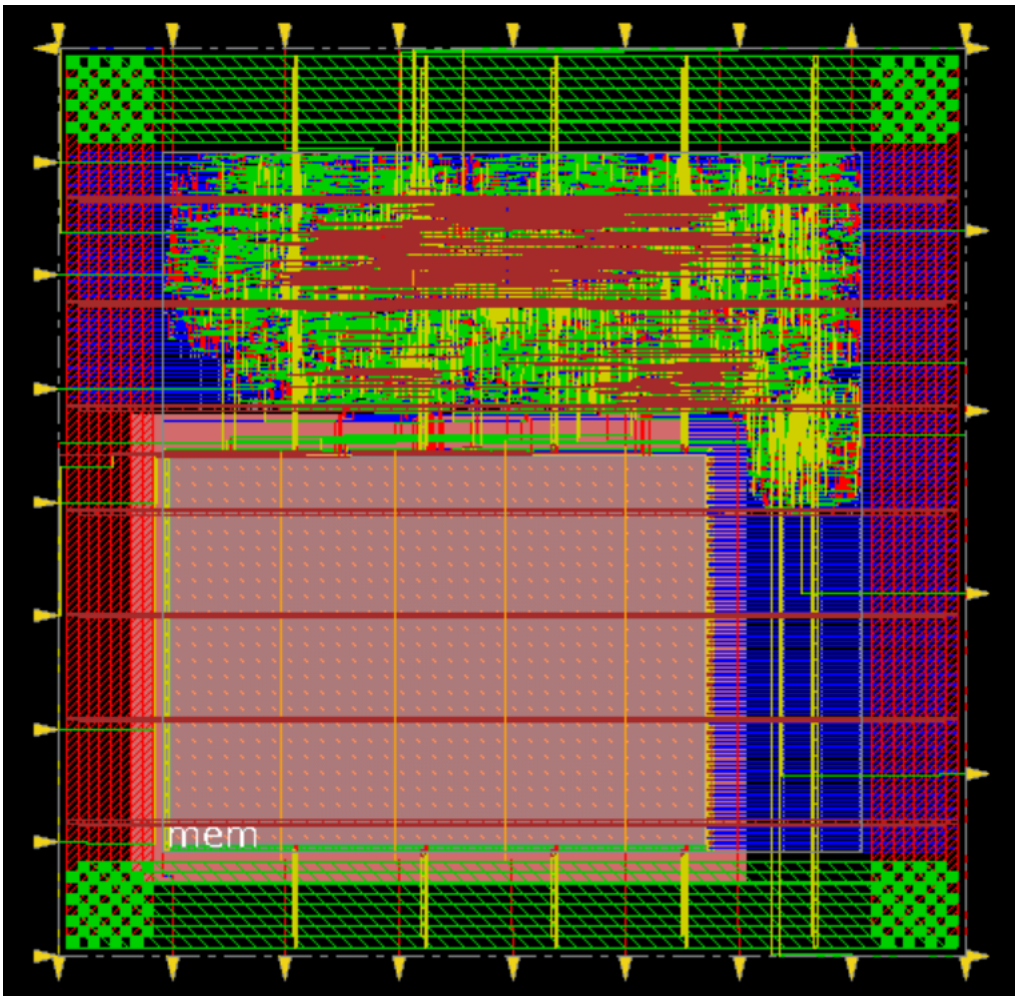

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to

switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)
   盡量靠邊邊放，且 io 接口盡可能朝中心，為了方便後續繞線不會繞一大圈，而且也能預留一大塊完整空間。