

# team05\_lab\_bonus\_report

### 層級架構:

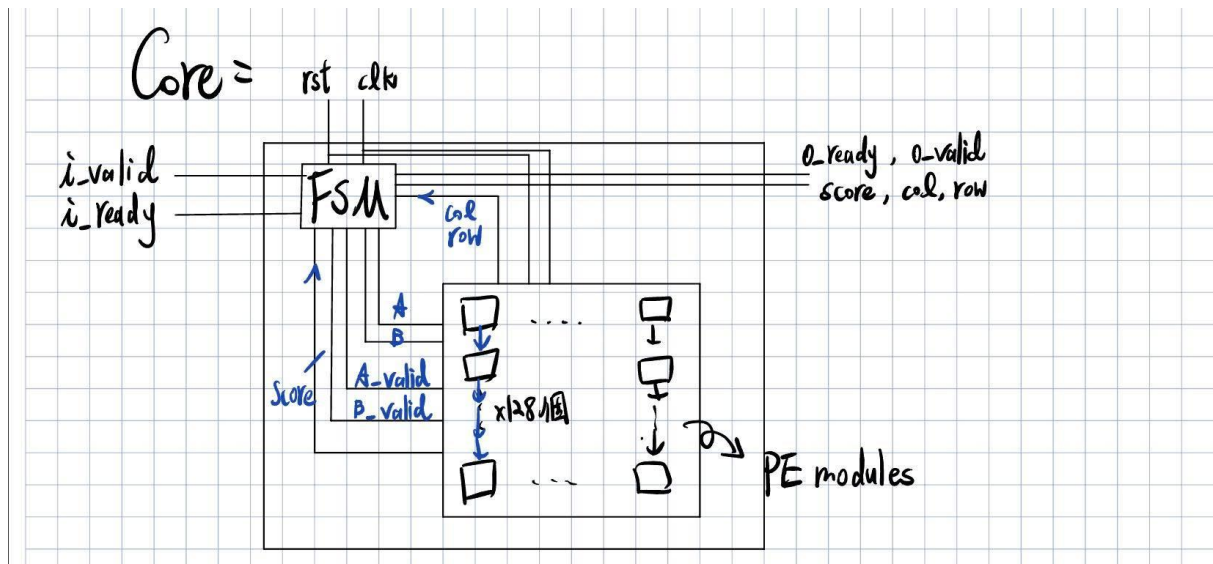
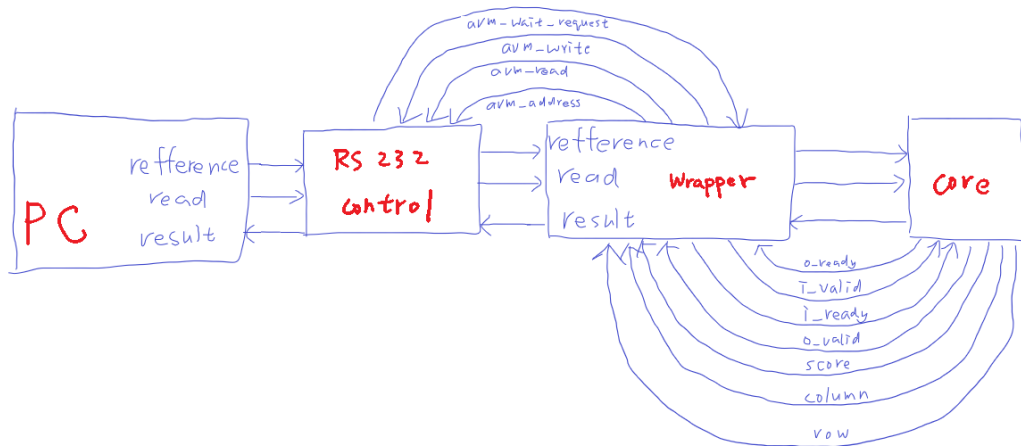
**DE2\_1115.sv**

**sw\_qsys.sv**

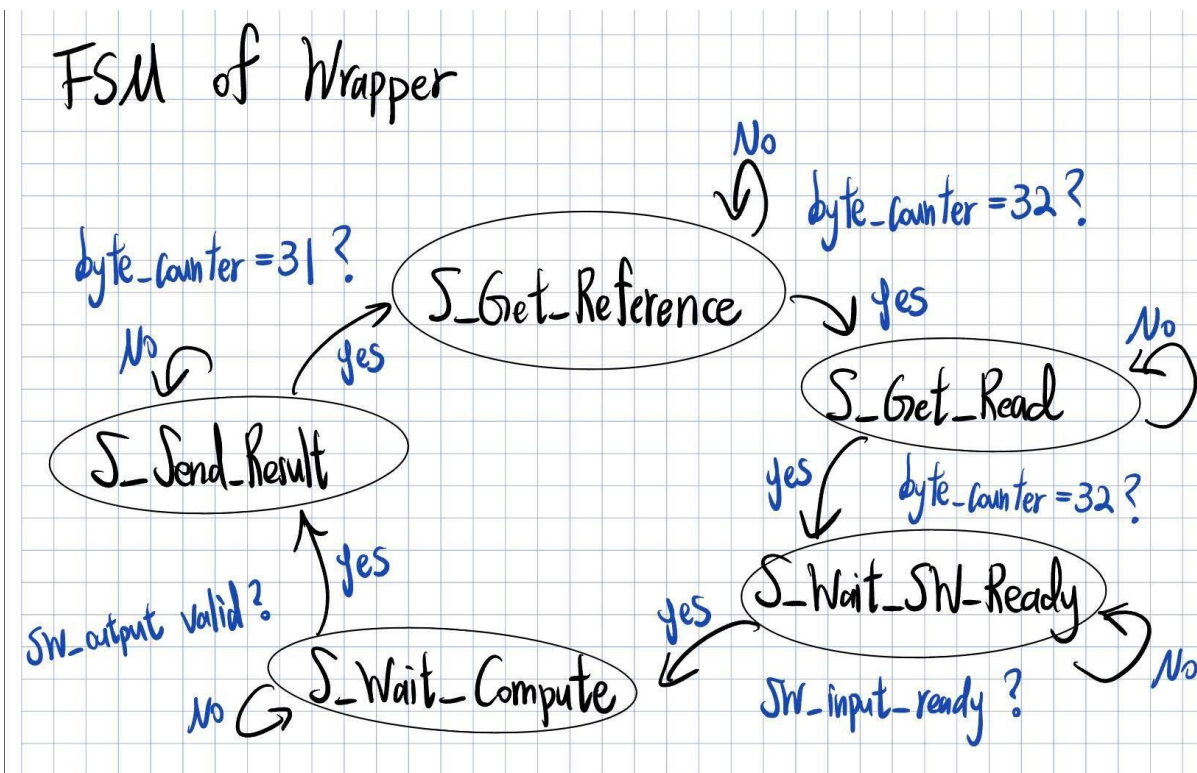
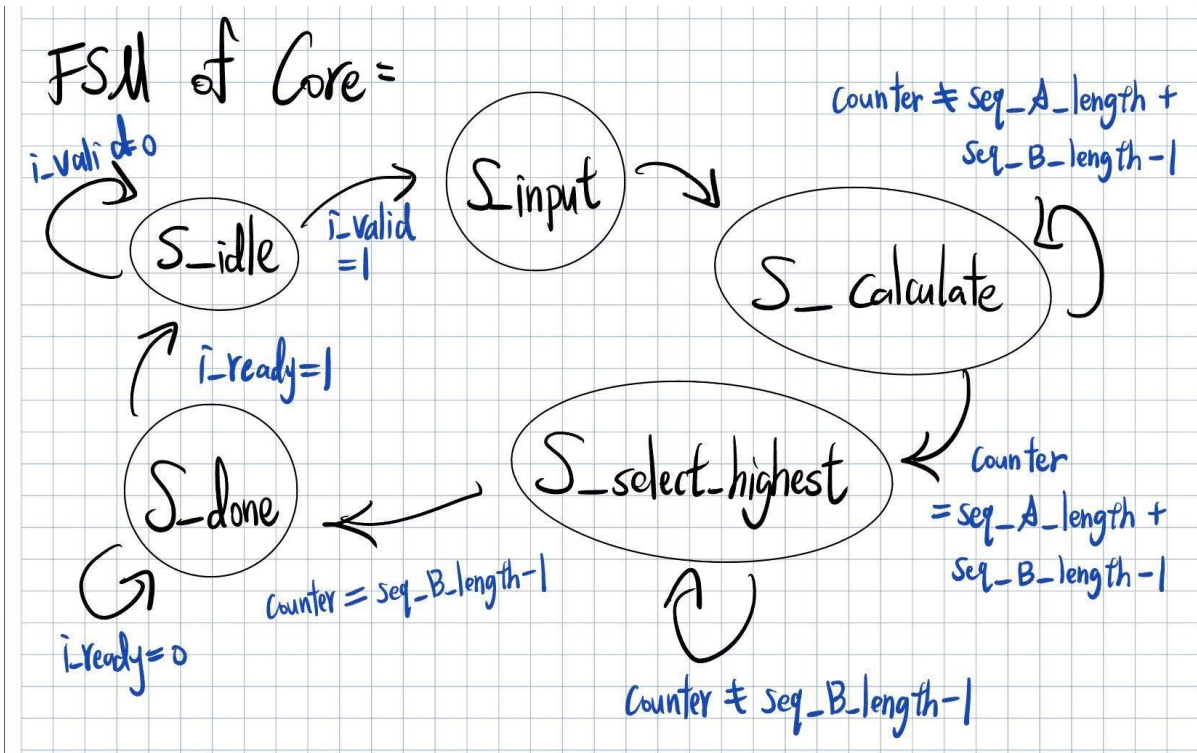
***SW\_Wrapper.sv***

SW\_core.sv

**Block diagram:**



## FSM:



Fitter summary & timing analyzer:

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<ul style="list-style-type: none"> <li>Flow Summary</li> <li>Flow Settings</li> <li>Flow Non-Default Global Settings</li> <li>Flow Elapsed Time</li> <li>Flow OS Summary</li> <li>Flow Log</li> <li>Analysis &amp; Synthesis <ul style="list-style-type: none"> <li>Fitter <ul style="list-style-type: none"> <li><b>Summary</b></li> <li>Settings</li> <li>Parallel Compilation</li> <li>I/O Assignment Warnings</li> <li>Ignored Assignments</li> <li>Incremental Compilation Summary</li> <li>Pin-Out File</li> <li>Resource Section</li> <li>I/O Rules Section</li> <li>Device Options</li> <li>Operating Settings and Constraints</li> <li>Messages</li> <li>Suppressed Messages</li> <li>Flow Messages</li> <li>Flow Suppressed Messages</li> </ul> </li> <li>Assembler</li> <li>TimeQuest Timing Analyzer</li> </ul> </li> </ul>	<table> <tr> <td>Fitter Status</td><td>Successful - Tue Nov 29 01:46:54 2022</td></tr> <tr> <td>Quartus II 64-Bit Version</td><td>15.0.0 Build 145 04/22/2015 SJ Full Version</td></tr> <tr> <td>Revision Name</td><td>DE2_115</td></tr> <tr> <td>Top-level Entity Name</td><td>DE2_115</td></tr> <tr> <td>Family</td><td>Cyclone IV E</td></tr> <tr> <td>Device</td><td>EP4CE115F29C7</td></tr> <tr> <td>Timing Models</td><td>Final</td></tr> <tr> <td>Total logic elements</td><td>47,278 / 114,480 ( 41 % )</td></tr> <tr> <td>    Total combinational functions</td><td>46,251 / 114,480 ( 40 % )</td></tr> <tr> <td>    Dedicated logic resources</td><td>1,027 / 114,480 ( 1 % )</td></tr> <tr> <td>Total registers</td><td>12113</td></tr> <tr> <td>Total pins</td><td>480 / 529 ( 91 % )</td></tr> <tr> <td>Total virtual pins</td><td>0</td></tr> <tr> <td>Total memory bits</td><td>0 / 3,981,312 ( 0 % )</td></tr> <tr> <td>Embedded Multiplier 9-bit elements</td><td>0 / 532 ( 0 % )</td></tr> <tr> <td>Total PLLs</td><td>1 / 4 ( 25 % )</td></tr> </table>	Fitter Status	Successful - Tue Nov 29 01:46:54 2022	Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version	Revision Name	DE2_115	Top-level Entity Name	DE2_115	Family	Cyclone IV E	Device	EP4CE115F29C7	Timing Models	Final	Total logic elements	47,278 / 114,480 ( 41 % )	Total combinational functions	46,251 / 114,480 ( 40 % )	Dedicated logic resources	1,027 / 114,480 ( 1 % )	Total registers	12113	Total pins	480 / 529 ( 91 % )	Total virtual pins	0	Total memory bits	0 / 3,981,312 ( 0 % )	Embedded Multiplier 9-bit elements	0 / 532 ( 0 % )	Total PLLs	1 / 4 ( 25 % )
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6	Unconstrained Output Port Paths	1	1

## Q&A:

### 1. Short-read mapping 的流程為何？

**Ans:** 把short read切成好幾個seed, 去找出在reference內完全相同的位置, 再拓展回去原本的長度,此時short read對應到好幾組candidate,再對各組candidate使用SW, 分數最高的即是最相似sequence。

### 2. 以軟體實現 SW 演算法的挑戰是什麼？

### 3. 以硬體實現的優勢是甚麼？

**Ans(2&3):** 在軟體上實現SW, 當reference sequence和short read sequence長度變為n倍時, 會花 $n^2$ 倍去完成, 但是用硬體的話可以多使用n倍PE module去計算使得時間降低為n倍。軟體的挑戰是時間複雜度, 但是硬體可以用多使用運算資源去降低時間複雜度。