Verilog Simulation & Debugging Tools

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Outline

- NC-Verilog
- nWave
- Verdi

NC-Verilog

Introduction to NC-Verilog

- The Cadence® NC-Verilog® simulator is a Verilog digital logic simulator.
- We can use NC-Verilog to
  - Compiles the Verilog source files.
  - Elaborates the design and generates a simulation snapshot.
  - Simulates the snapshot.

Before Using NC-Verilog

- Source the environment settings of CAD tools.

  > source /usr/cadence/cshrc

- If you try entering the command "ncverilog" but it turns out "command not found," it means there's something wrong with the "*.cshrc" file or the software license is out of date.

Running Verilog (1/2)

- Run the Verilog simulation:

```
ncverilog Lab0_alu_tb.v Lab0_alu.v +access+rw
```

- Another choice of running Verilog simulation:

```
ncverilog -f Lab0_alu_file.f +access+rw
```

In Lab0_alu_file.f

```
Lab0_alu_tb.v
Lab0_alu.v
~
~
```

Running Verilog (2/2)

- "+access+rw" is added to enable waveform file dumping.

Waveform dumping example for testbench

```
initial begin
    $fsdbDumpfile("exp2_rsa.fsdb");
    $fsdbDumpvars;
end
```

or

```
initial begin
    $dumpfile("exp2_rsa.vcd");
    $dumpvars;
end
```

- *.fsdb has smaller file size than *.vcd. But $fsdbDumpfile cannot work without sourcing verdi.cshrc.

Simulation Results

- Check the simulation result to see if the Verilog design is finished correctly.

```
ncverilog: 10.20-s114: (c) Copyright 1995-2012 Cadence Design Systems, Inc.
Loading snapshot worklib.testbench:v ..................... Done
*Novas* Loading libsscore_ius102.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
Novas FSDB Dumper for IUS, Release 2012.04, Linux, 04/10/2012
Copyright (C) 1996 - 2012 by SpringSoft, Inc.
*Novas* : Create FSDB file 'exp2_rsa.fsdb'
*Novas* : Begin traversing the scopes, layer (0).
*Novas* : End of traversing.
----------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 100046010 NS + 0
./testbench.v:177         $finish;
ncsim> exit
```

nWave

Introduction to nWave

- nWave is one of the best waveform (*.vcd or *.fsdb) viewer.
- We can debug easily by checking the waveform file dumped during simulation.

Before Using nWave

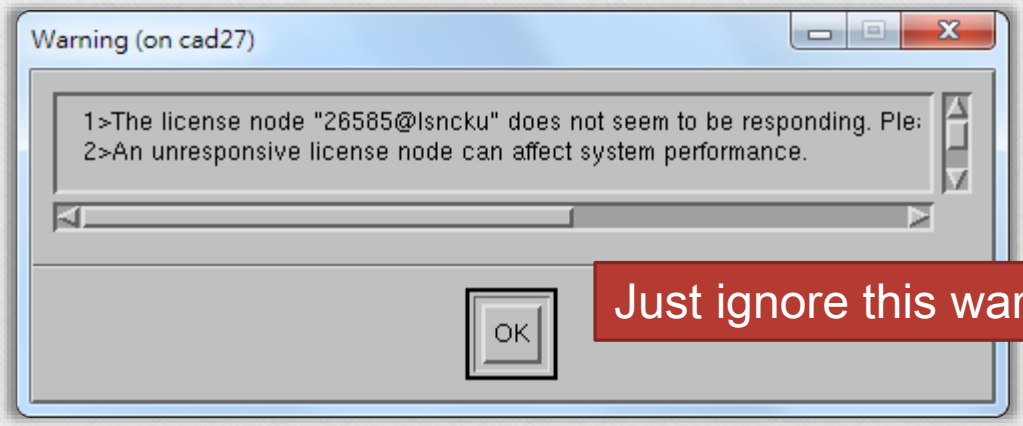
- Source the environment settings of CAD tools.
  - > source /usr/cad/synopsys/CIC/license.csh
  - > source /usr/spring_soft/CIC/verdi.cshrc

Start nWave

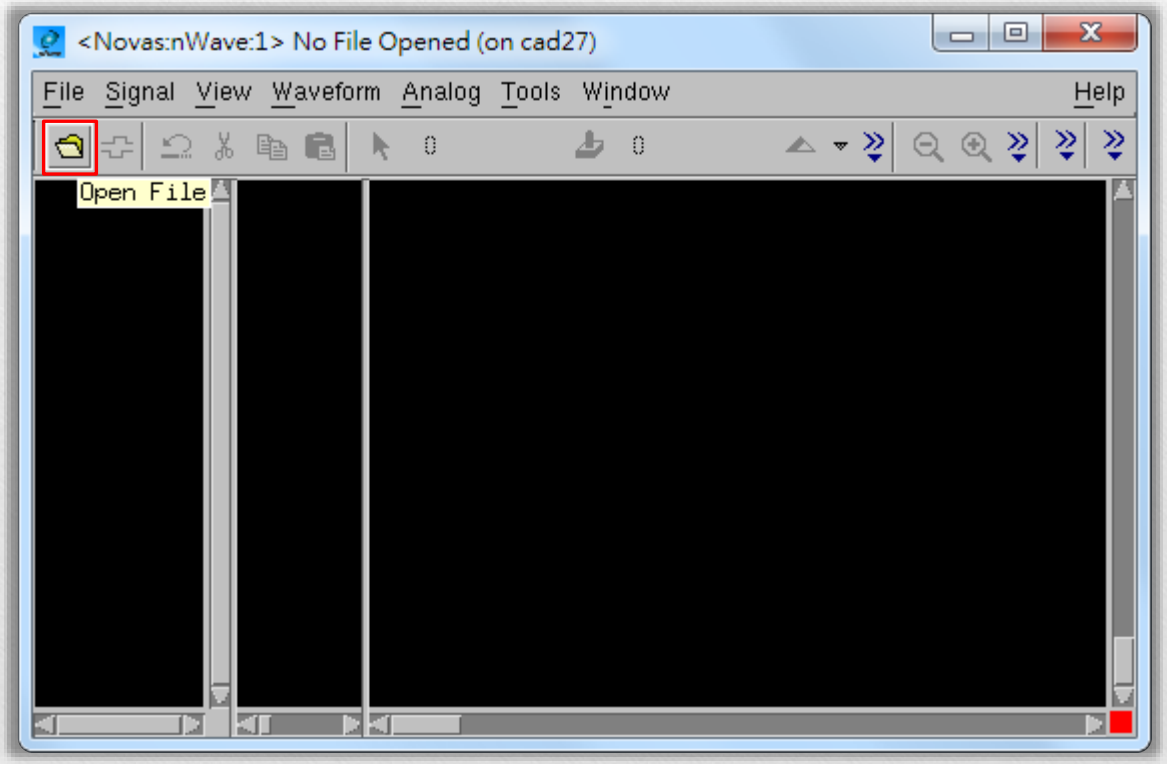
- Type the following command:

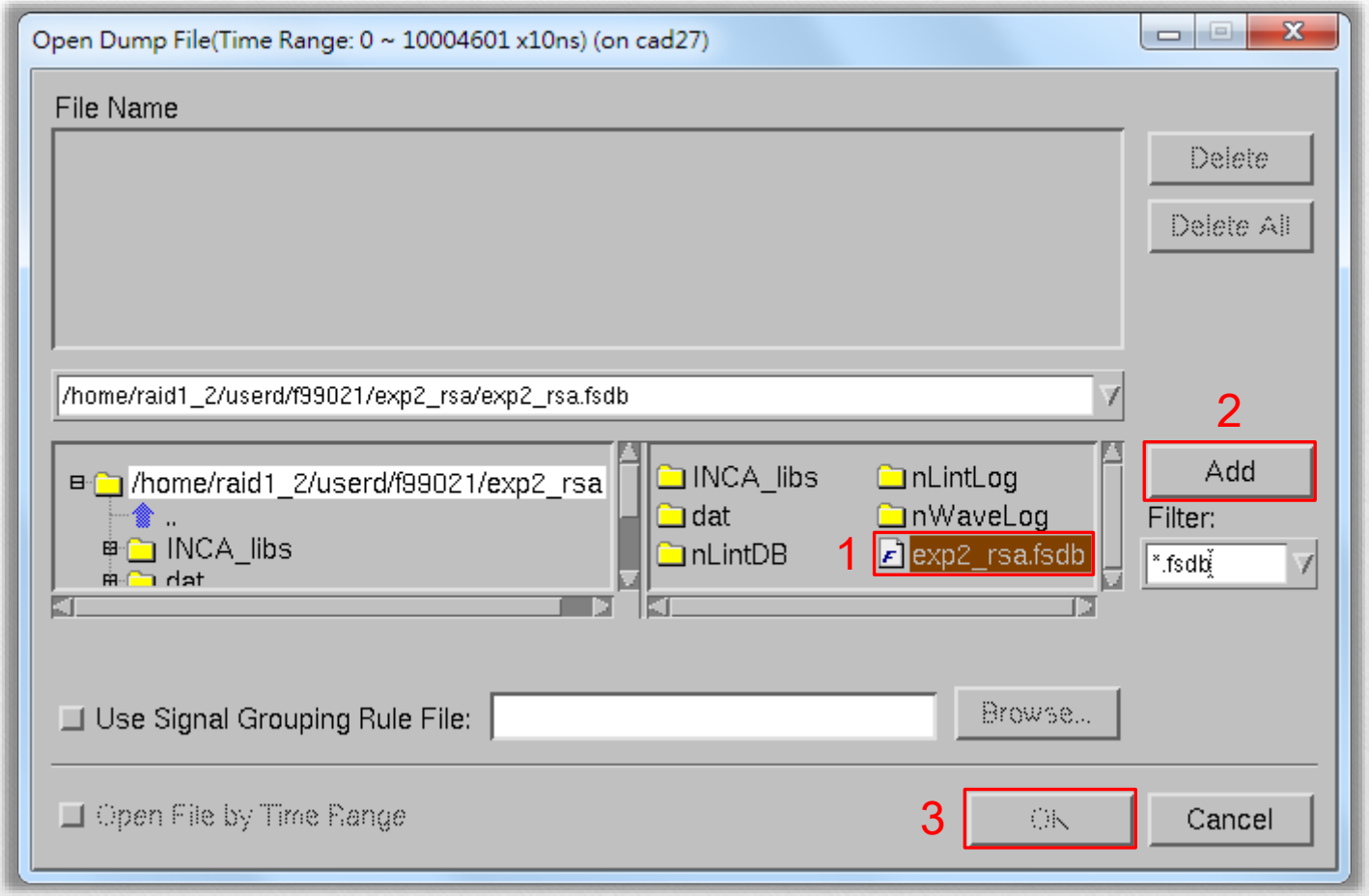
```
nWave &
```

  - Also, the token "&" enable you to use the terminal while Verdi is running in the background.

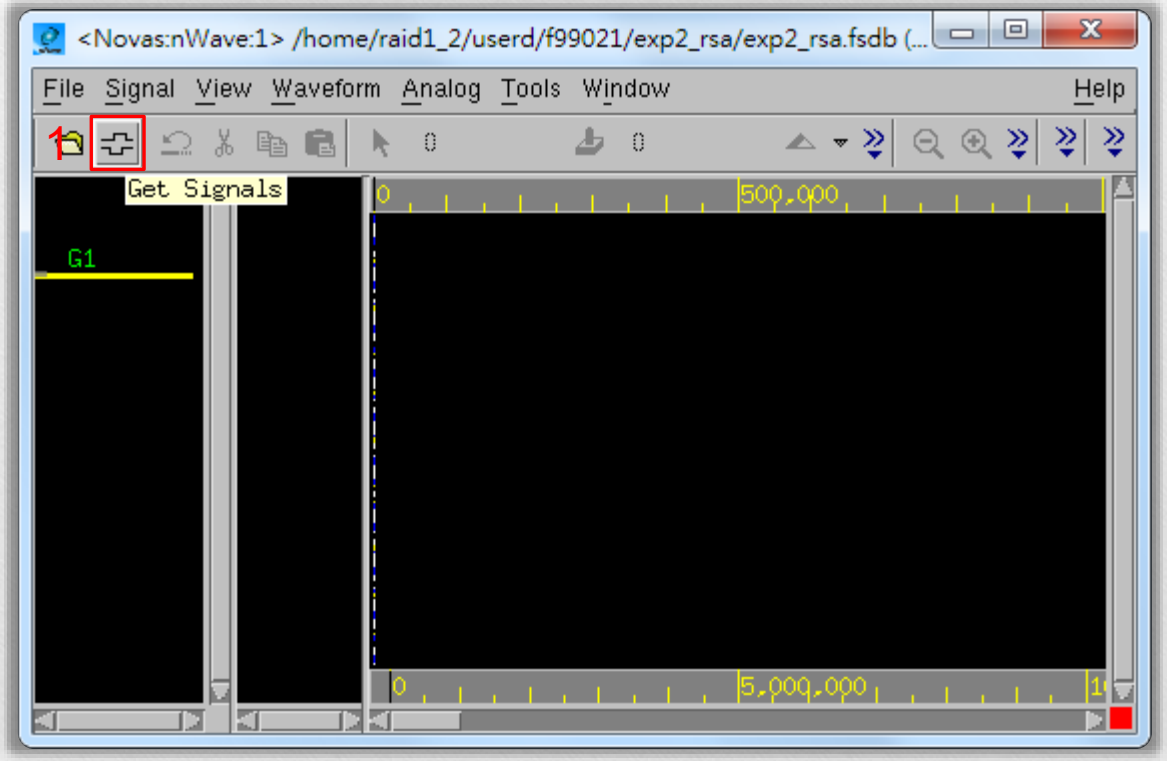


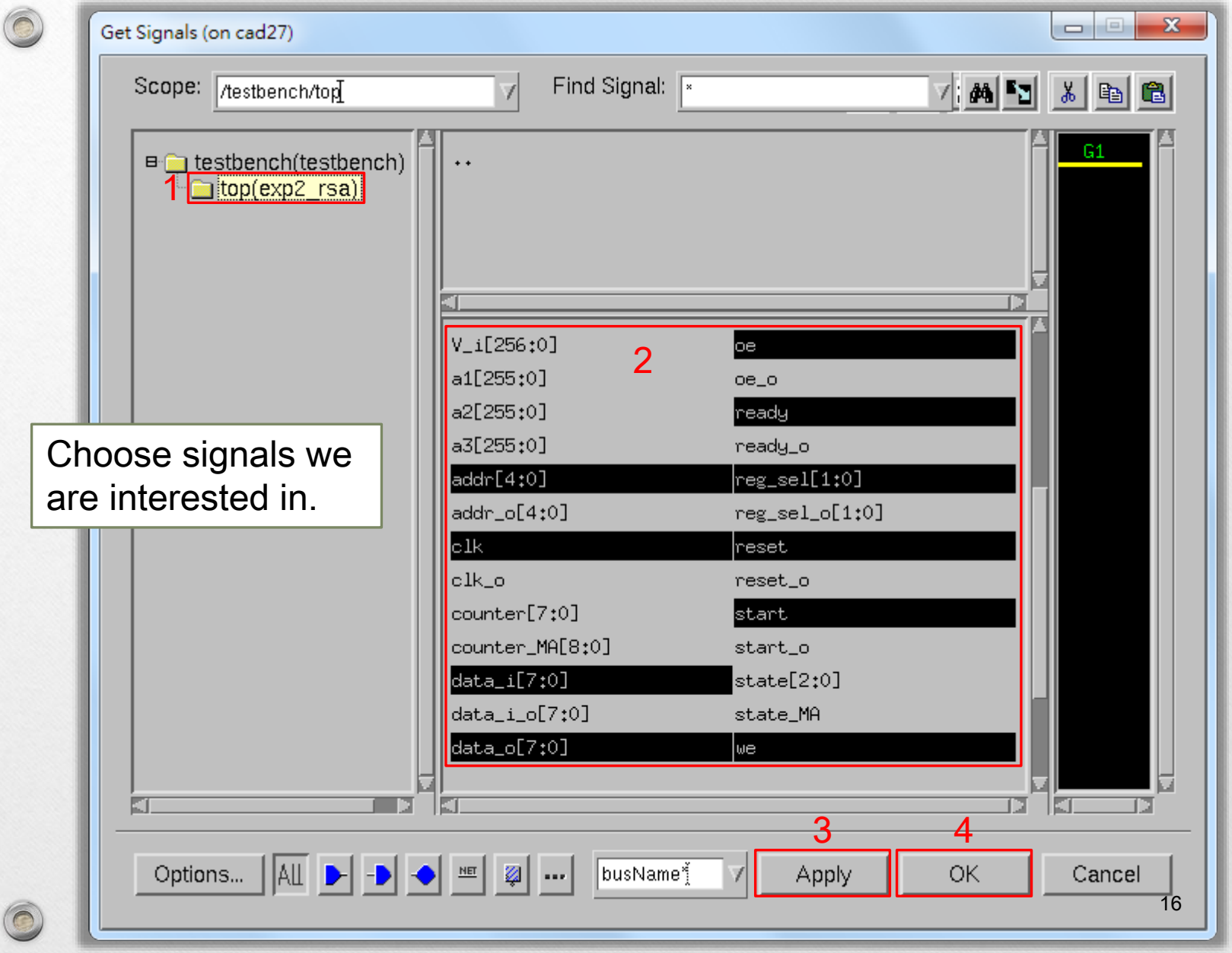
Open the FSDB File




Open Dump File(Time Range: 0 ~ 10004601 x10ns) (on cad27)
File Name
Delete
Delete All
/home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb
2
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
dat
INCA_libs
dat
nLintDB
nLintLog
nWaveLog
1
exp2_rsa.fsdb
Add
Filter:
*.fsdb
Use Signal Grouping Rule File:
Browse...
Open File by Time Range
3
OK
Cancel

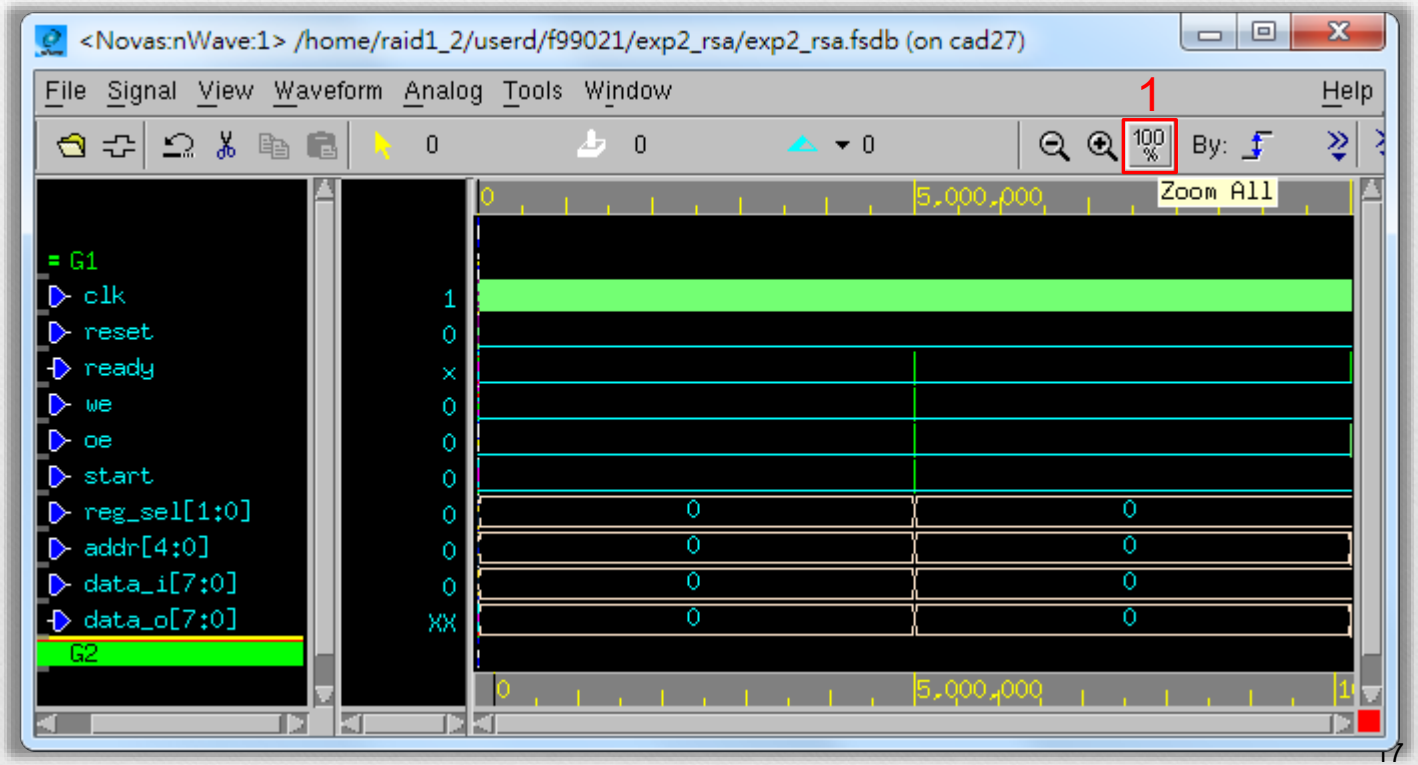
Choose Signals



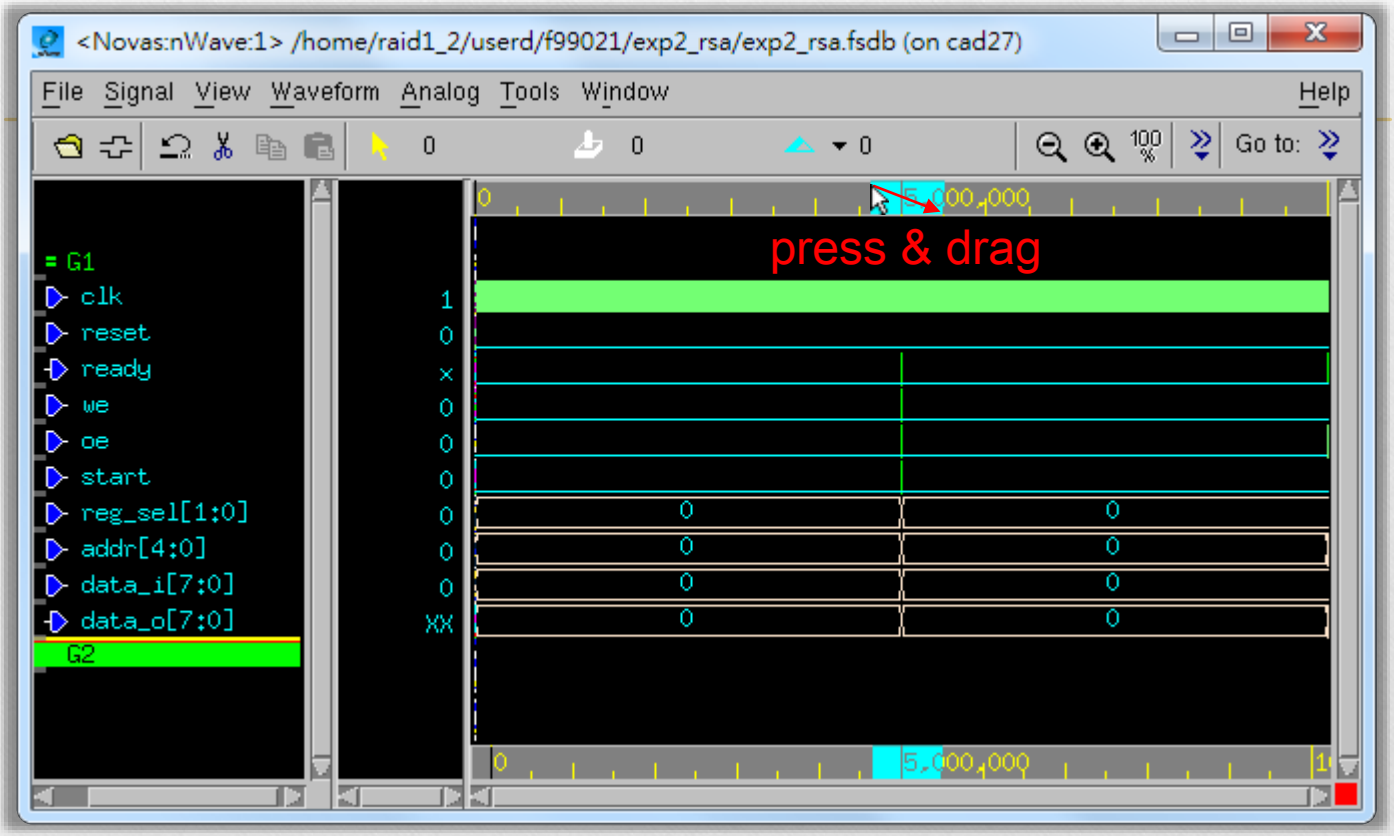


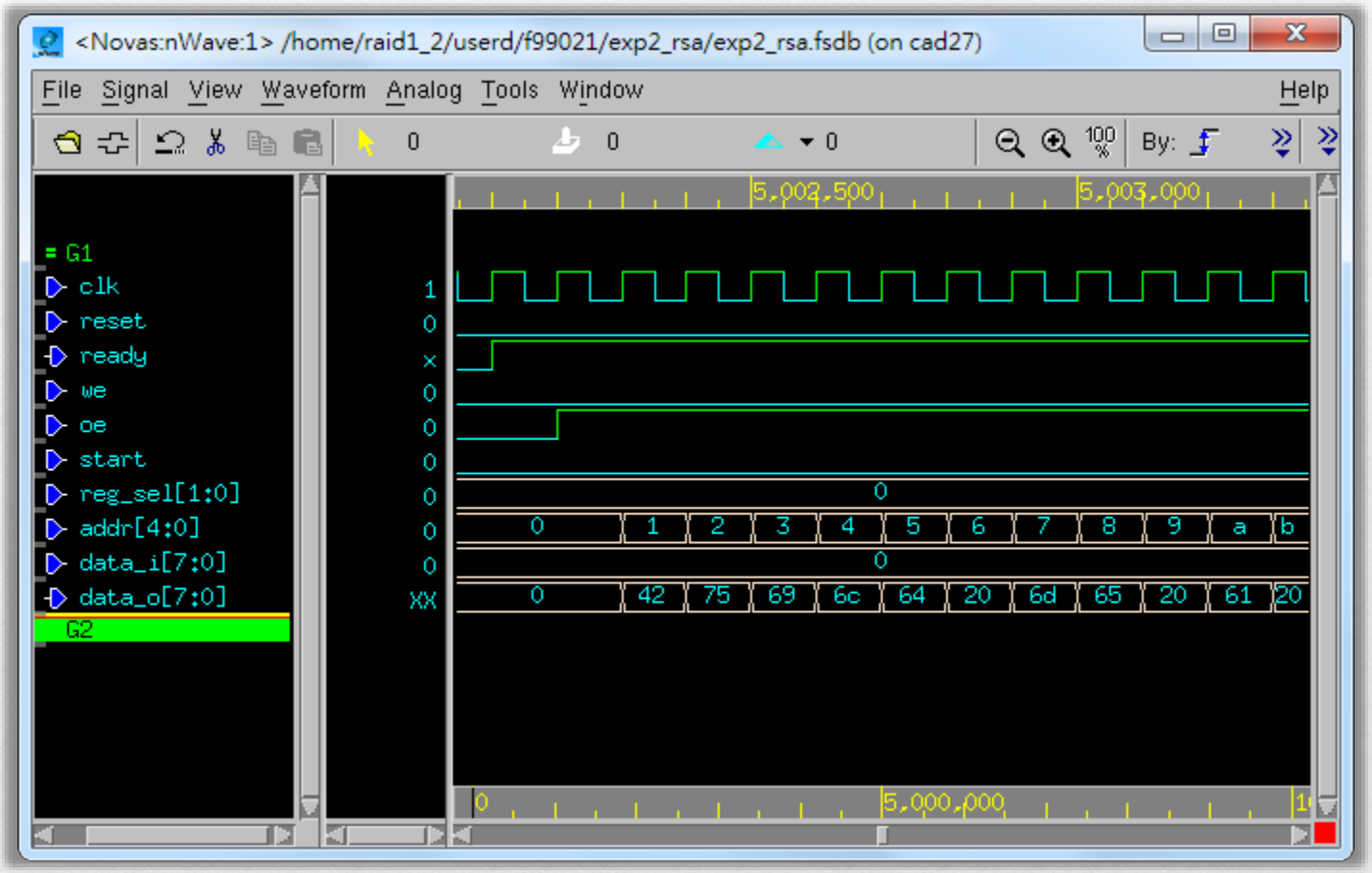
Choose signals we are interested in.

Browse the Whole Waveform

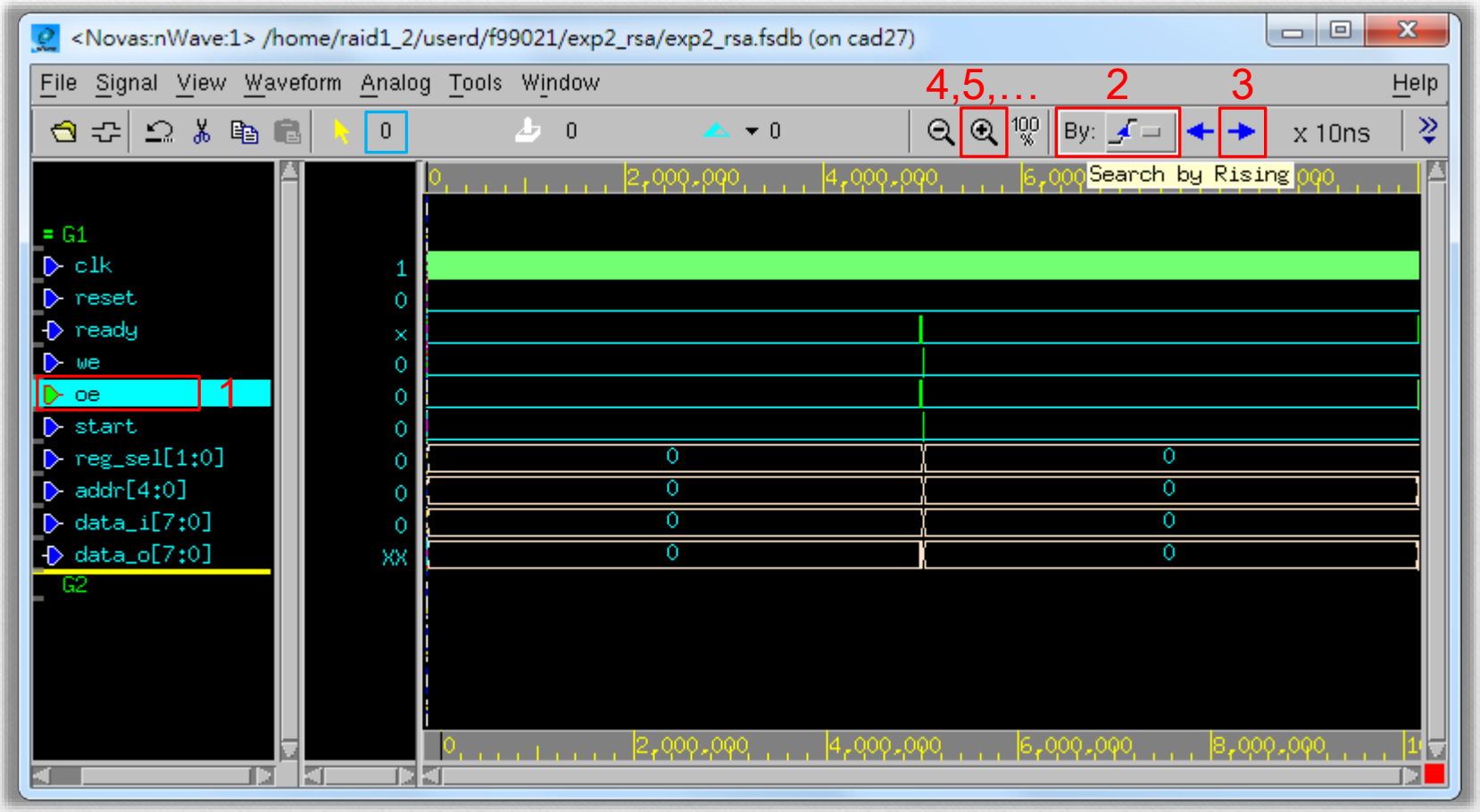


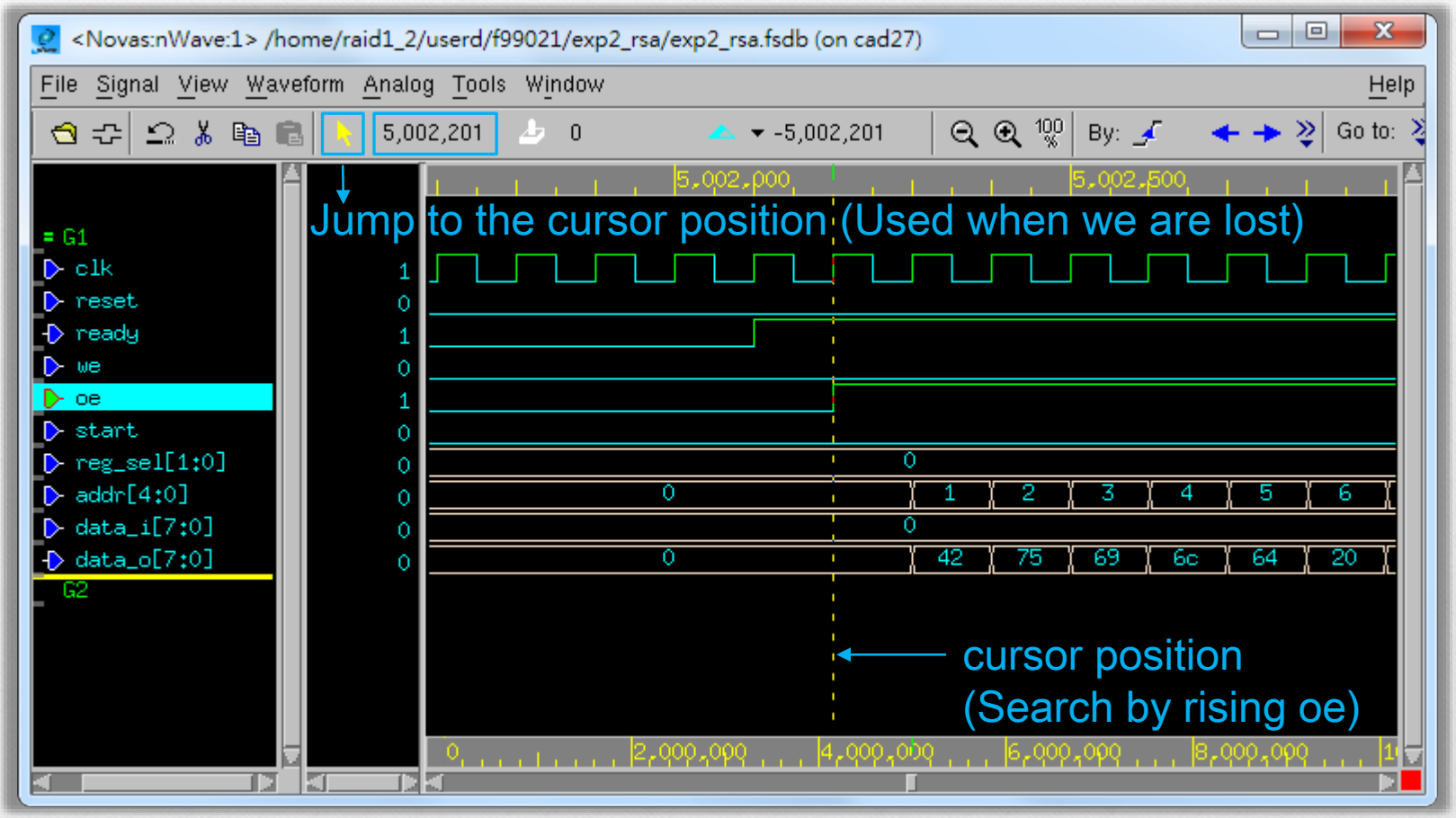
Browse the Specified Interval



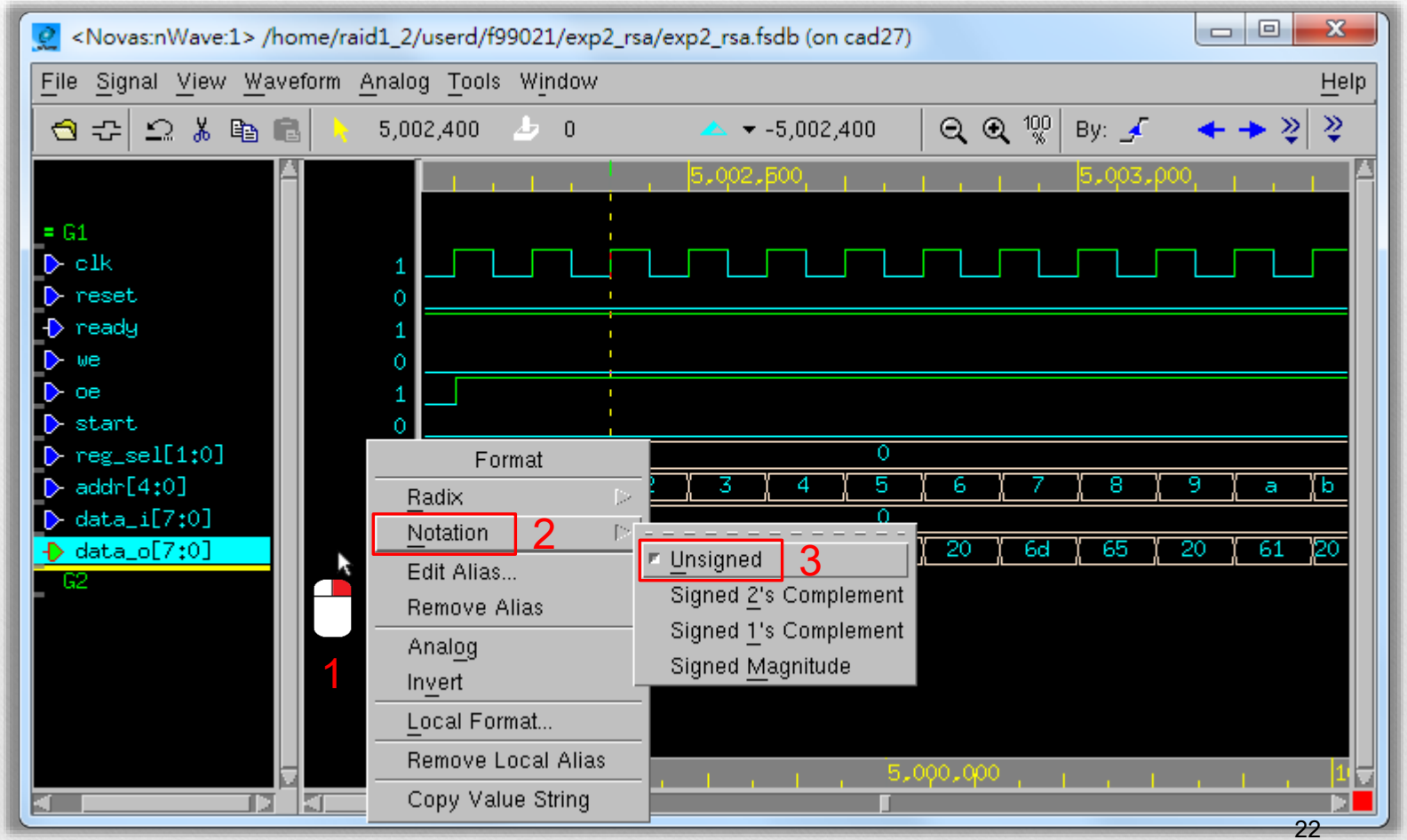

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
By:
5,002,500
5,003,000
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
x
0
0
0
0
0
0
XX
0 1 2 3 4 5 6 7 8 9 a b
0 42 75 69 6c 64 20 6d 65 20 61 20
0
5,000,000

Search for Specified Signal

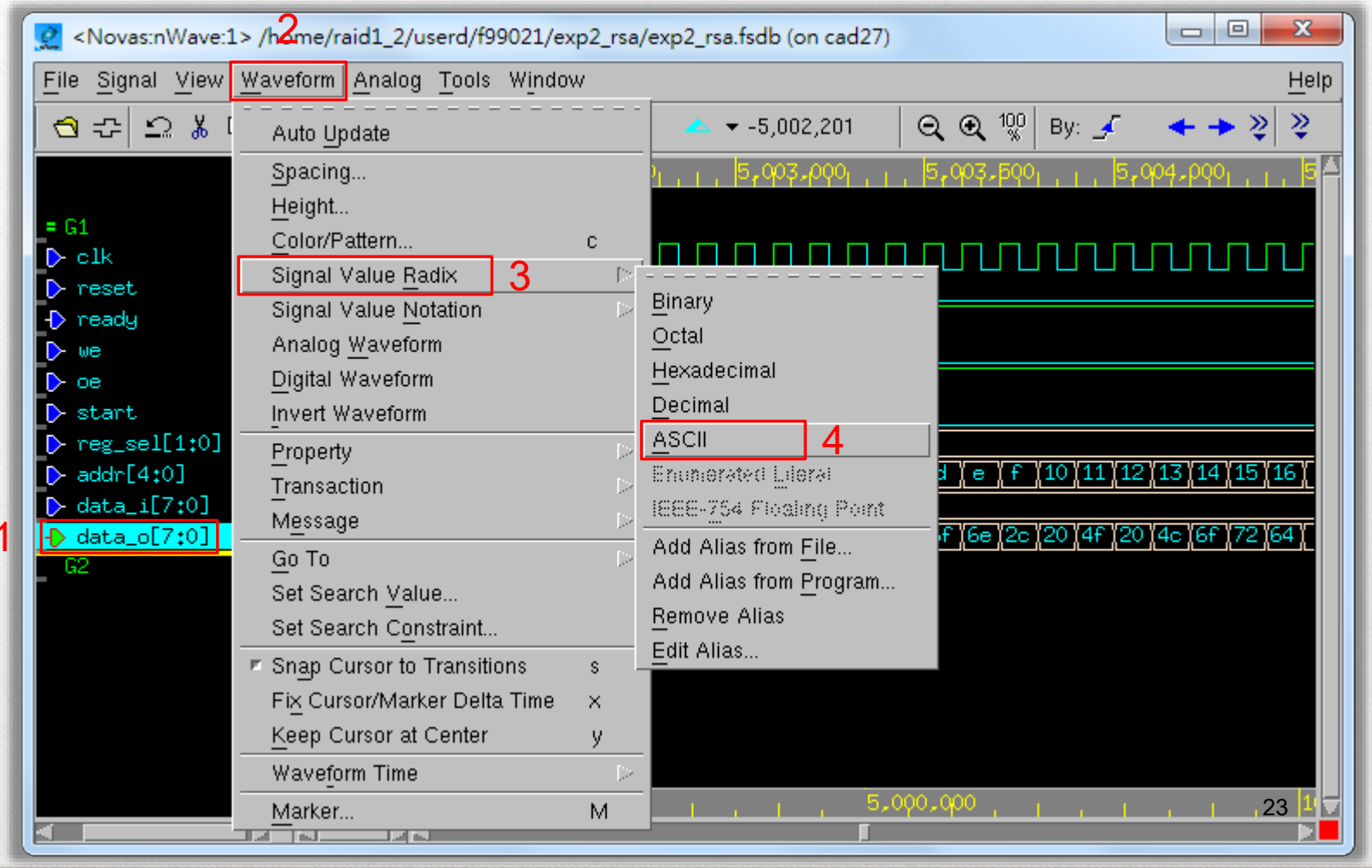


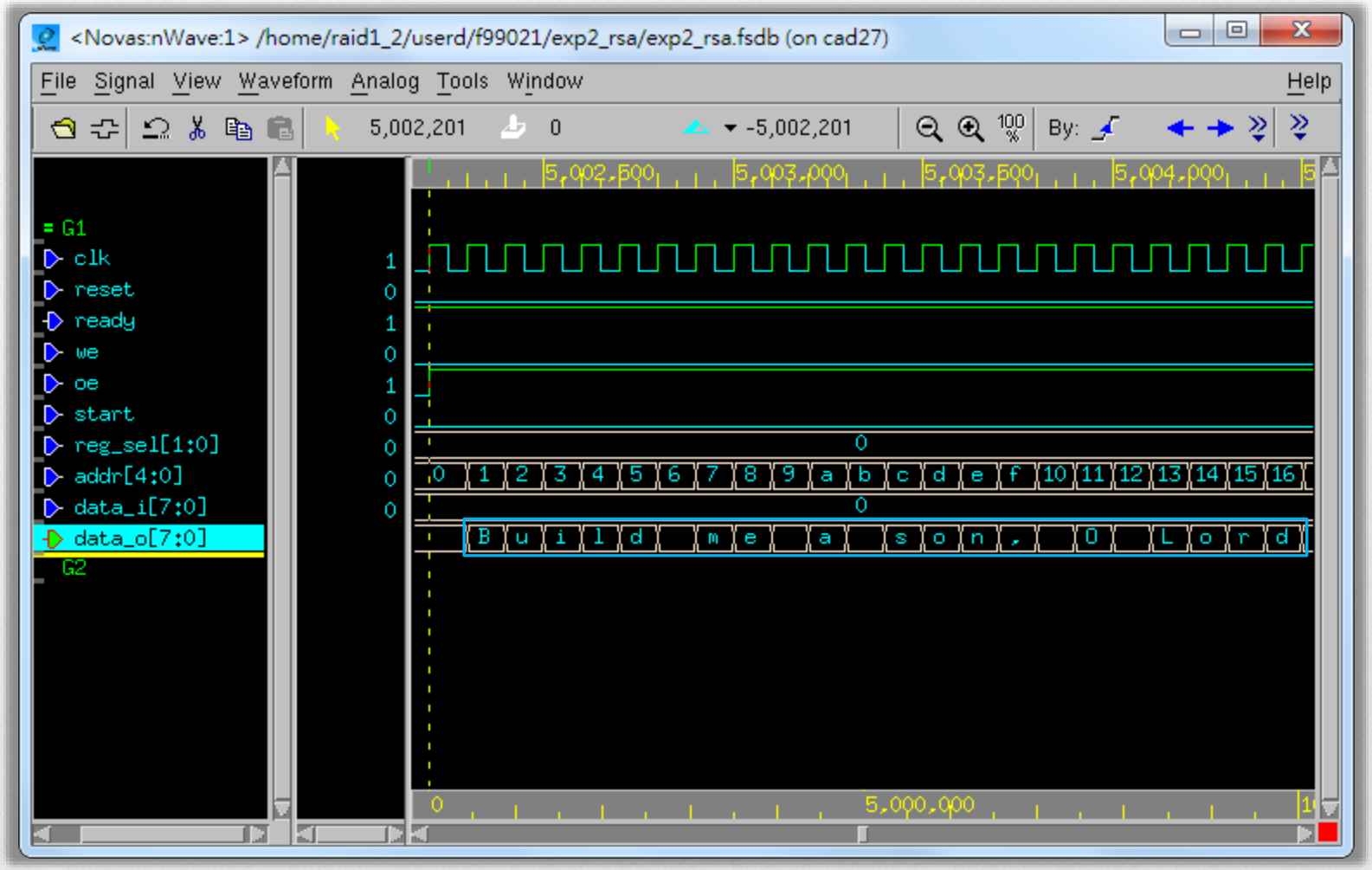

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
5,002,201
0
-5,002,201
By:
Go to:
Jump to the cursor position (Used when we are lost)
5,002,000
5,002,500
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
1
0
1
0
0
0
0
0
0
1
2
3
4
5
6
42
75
69
6c
64
20
cursor position
(Search by rising oe)
0
2,000,000
4,000,000
6,000,000
8,000,000

Change Sign Representation

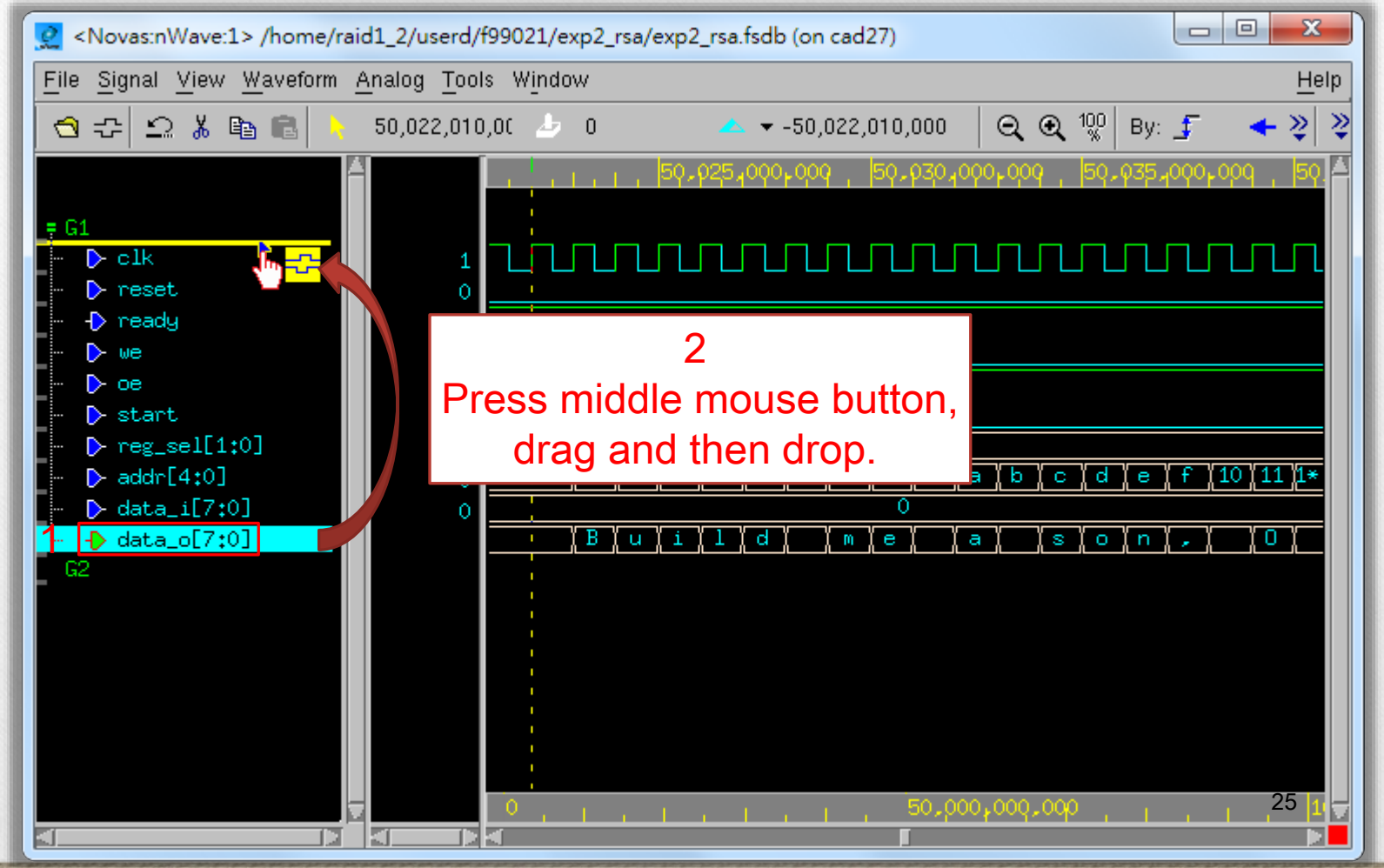


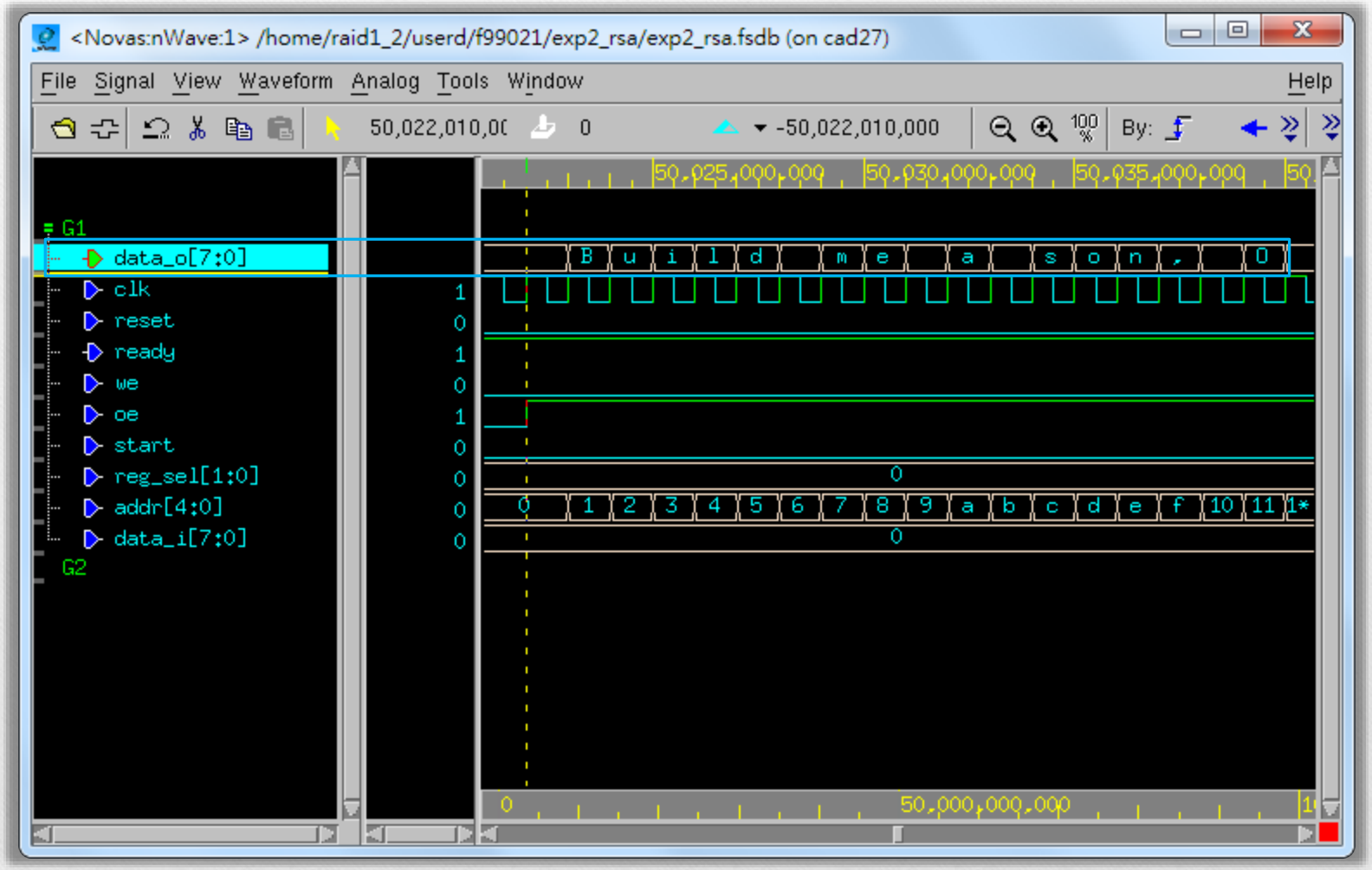
Change Radix Representation



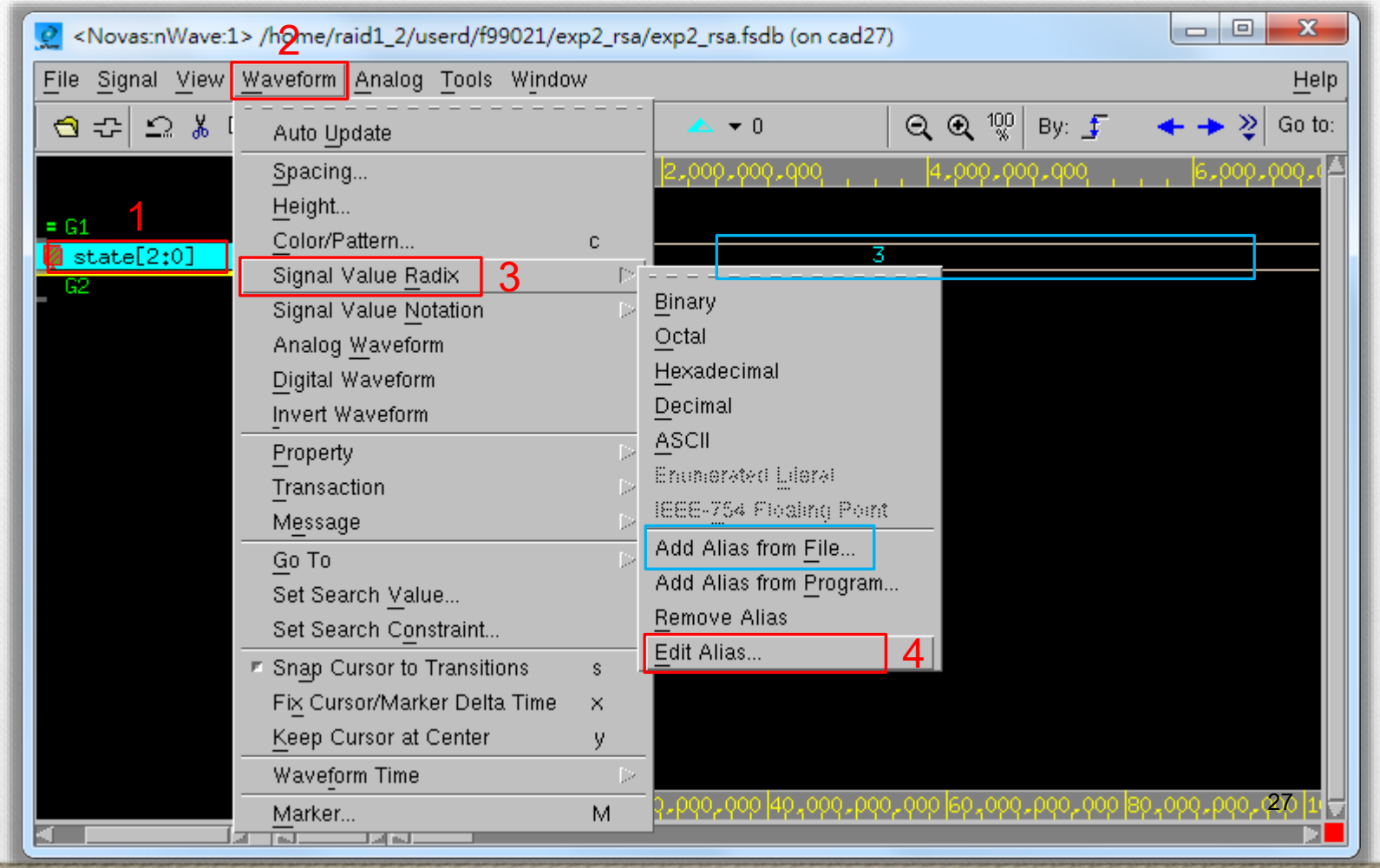

<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
5,002,201
0
-5,002,201
By:
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
1
0
1
0
0
0
0
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 12 13 14 15 16
B u i l d m e a s o n , 0 L o r d
5,000,000

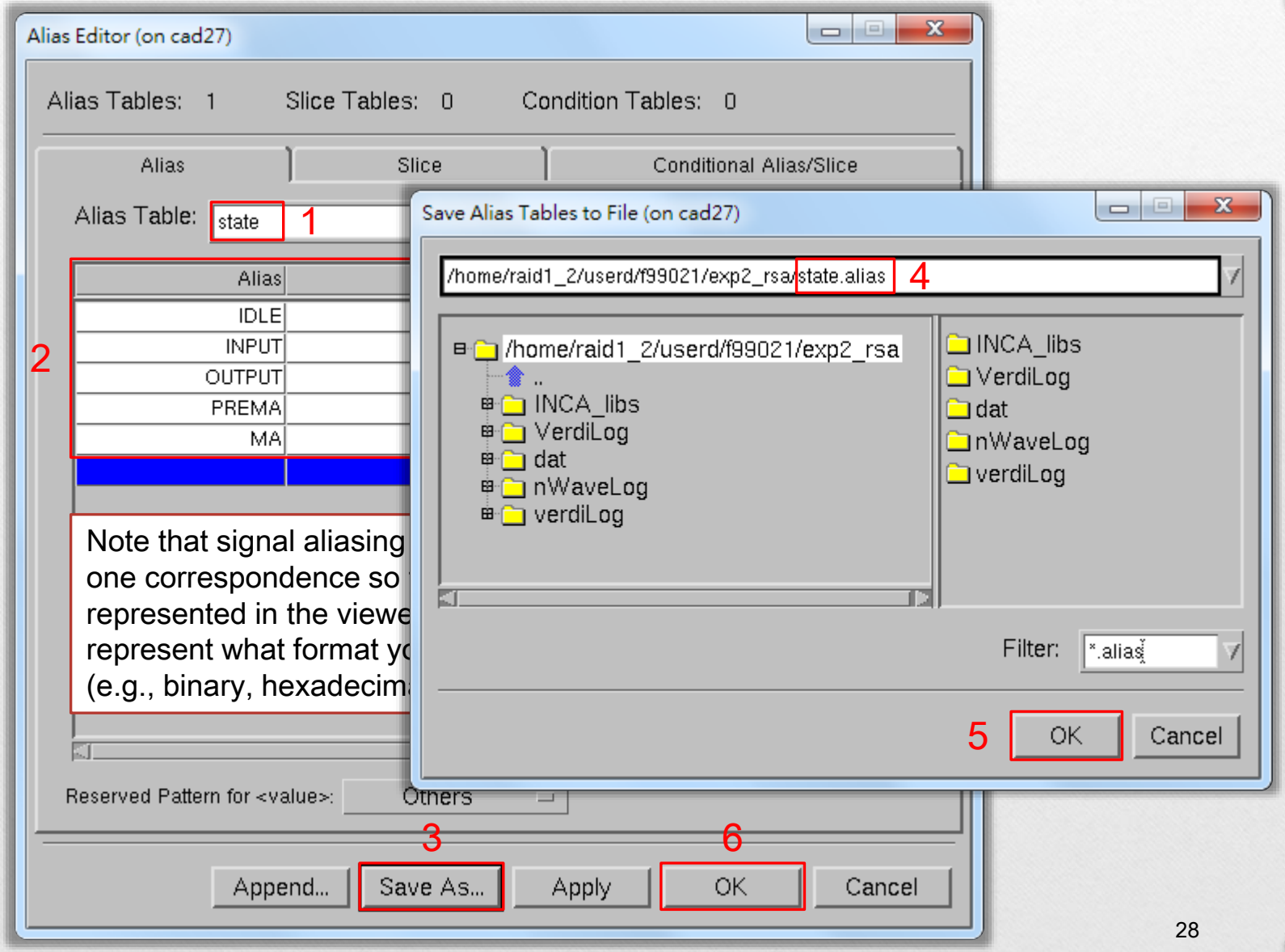
Change Signal Position

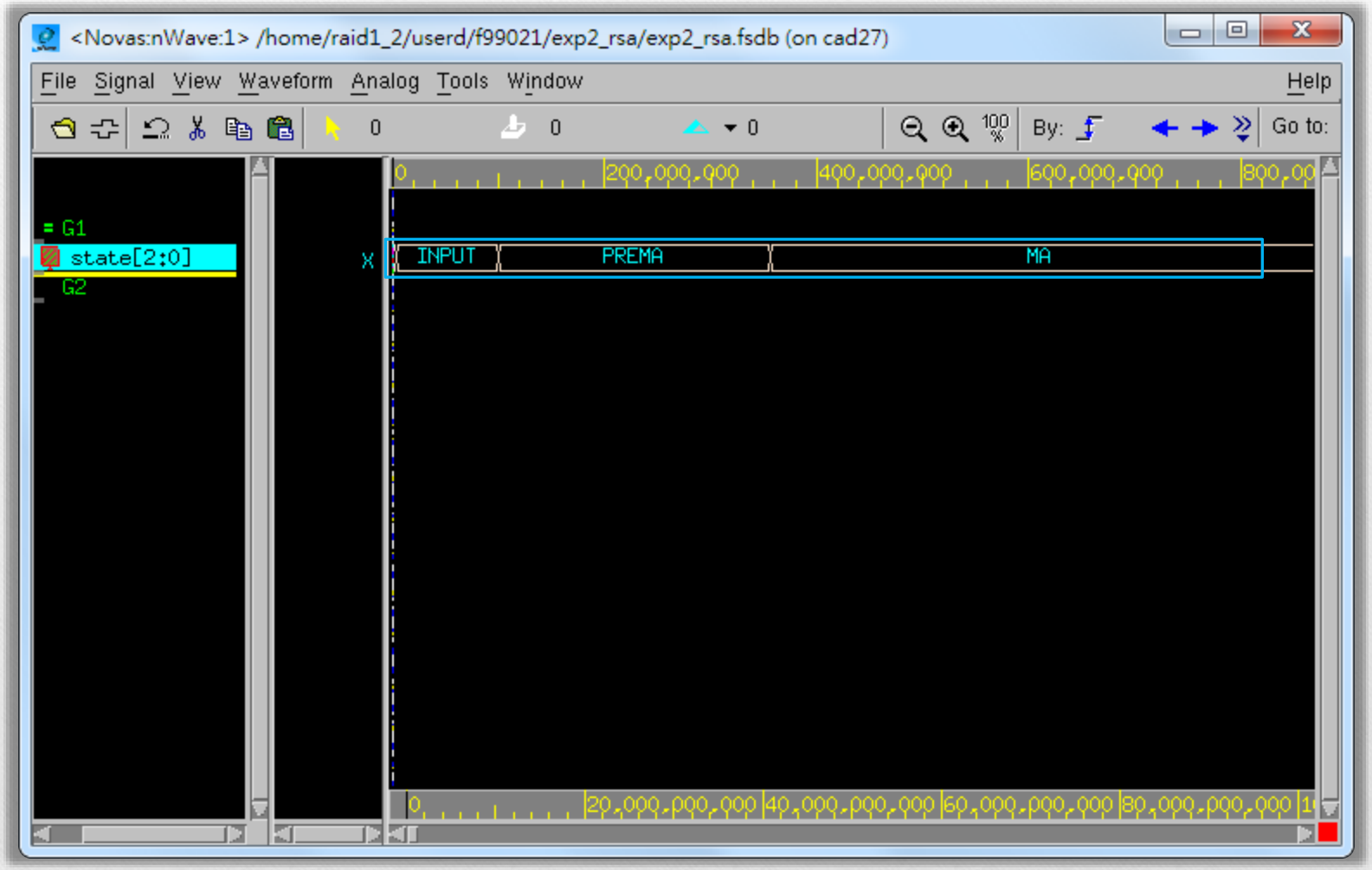



<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
50,022,010,0(
0
-50,022,010,000
By:
50,025,000,000
50,030,000,000
50,035,000,000
G1
data_o[7:0]
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
G2
B u i l d m e a s o n , 0
1
0
1
0
1
0
0
0
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 1*
0
0
50,000,000,000

Signal Aliasing

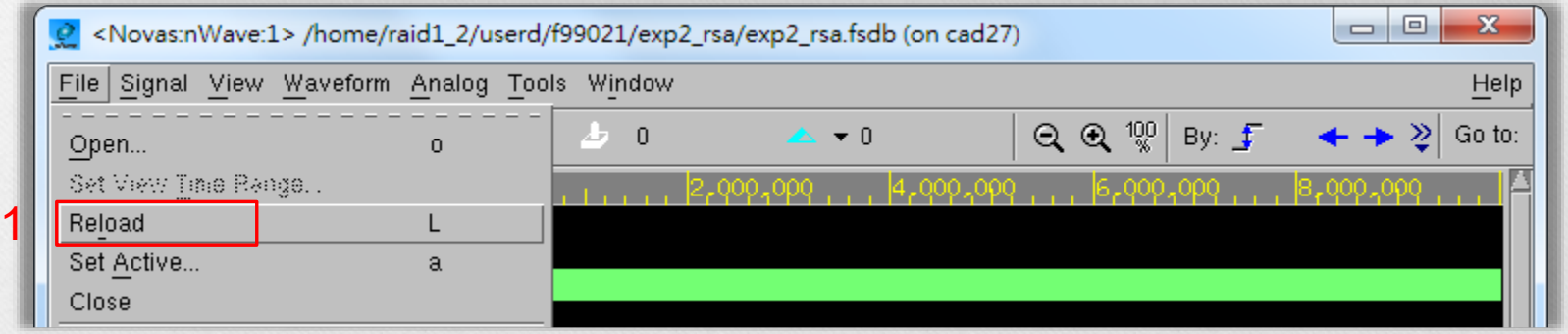



Alias Editor (on cad27)
Alias Tables: 1
Slice Tables: 0
Condition Tables: 0
Alias
Slice
Conditional Alias/Slice
Alias Table: state
1
Alias
IDLE
INPUT
OUTPUT
PREMA
MA
2
Note that signal aliasing
one correspondence so
represented in the viewe
represent what format yc
(e.g., binary, hexadecim
Reserved Pattern for <value>:
Others
3
Append...
Save As...
Apply
6
OK
Cancel
Save Alias Tables to File (on cad27)
/home/raid1_2/userd/f99021/exp2_rsa/state.alias
4
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
VerdiLog
dat
nWaveLog
verdiLog
INCA_libs
VerdiLog
dat
nWaveLog
verdiLog
Filter:
*.alias
5
OK
Cancel


<Novas:nWave:1> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad27)
File Signal View Waveform Analog Tools Window Help
Go to:
G1
state[2:0]
G2
INPUT
PREMA
MA

Reload the Waveform

- Remember to reload the waveform whenever finishing another Verilog simulation.



Verdi

Introduction to Verdi

- The Verdi Automated Debug System is an advanced open platform for debugging digital designs with powerful technology that helps you:
  1. Comprehend complex and unfamiliar design behavior.
  2. Automate difficult and tedious debug processes.
  3. Unify diverse and complicated design environments.

Basic Function (1/2)

- nTrace
  - A source code viewer and analyzer that operates on the knowledge database (KDB) to display the design hierarchy and source code (Verilog, VHDL, SysmVerilog, SystemC, PSL, OVA, mixed) for selected design blocks.
  - The main window of Verdi.

Basic Function (2/2)

- nWave
  - A state-of-the-art graphical waveform viewer and analyzer that is fully integrated with Verdi's source code, schematic, and flow views.
- nSchema
  - A schematic viewer and analyzer that generates interactive debug-specific logic diagrams showing the structure of selected portions of a design.

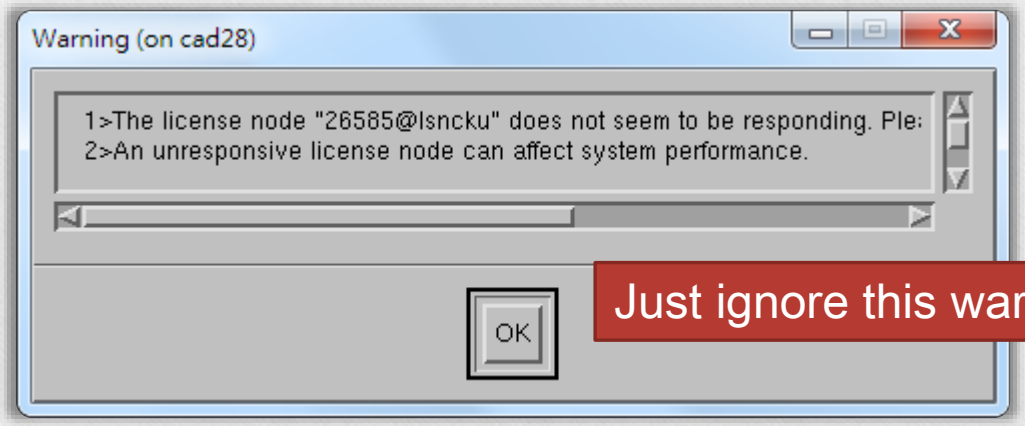
These two tools can be opened through nTrace.

Start Verdi

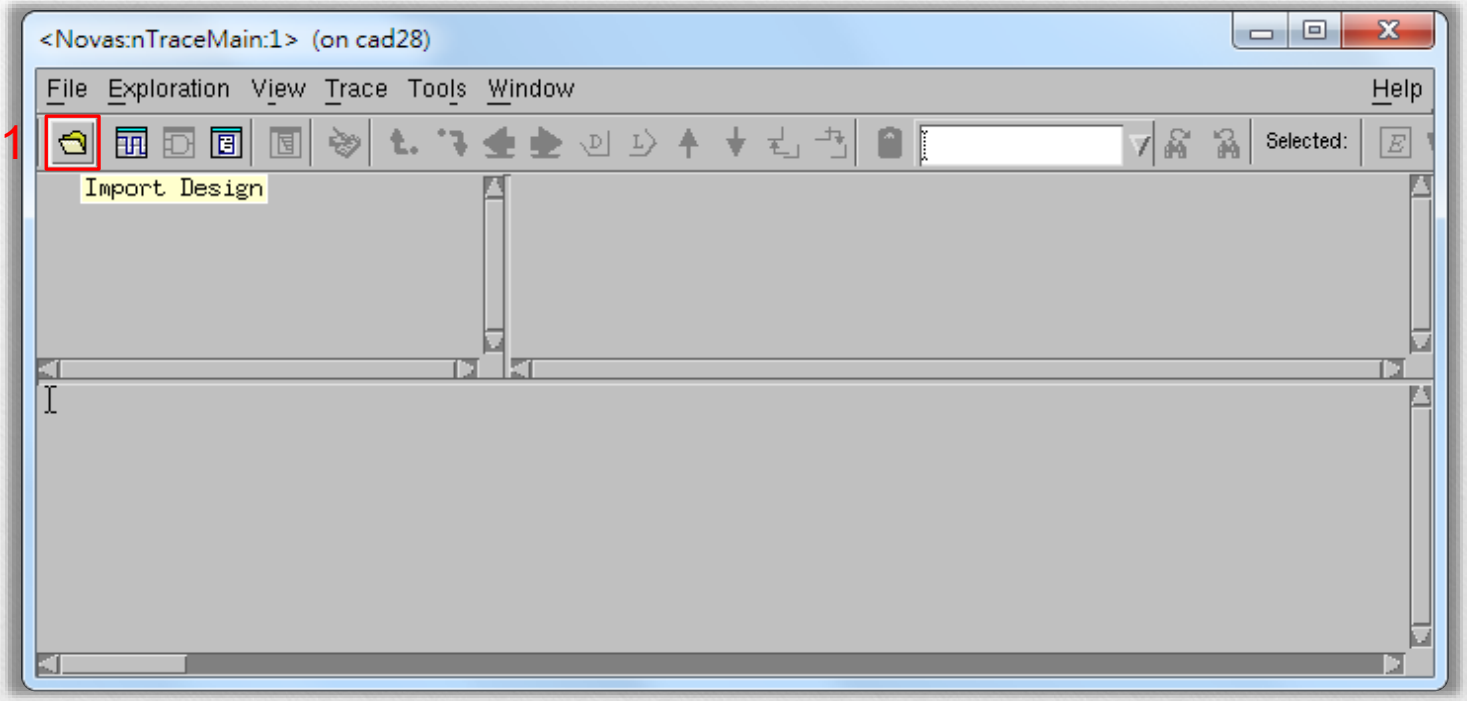
- Type the following command:

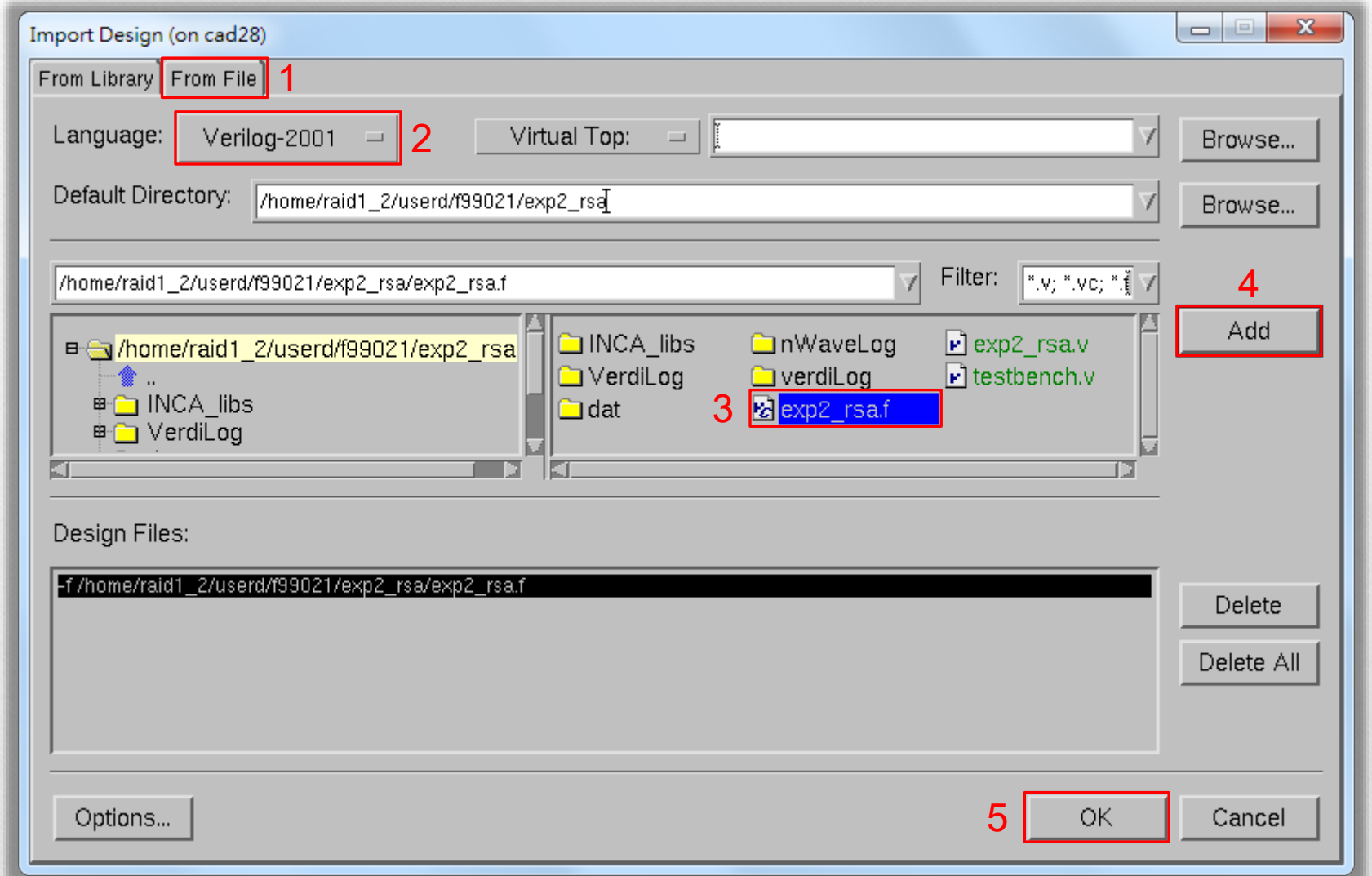
```
verdi &
```

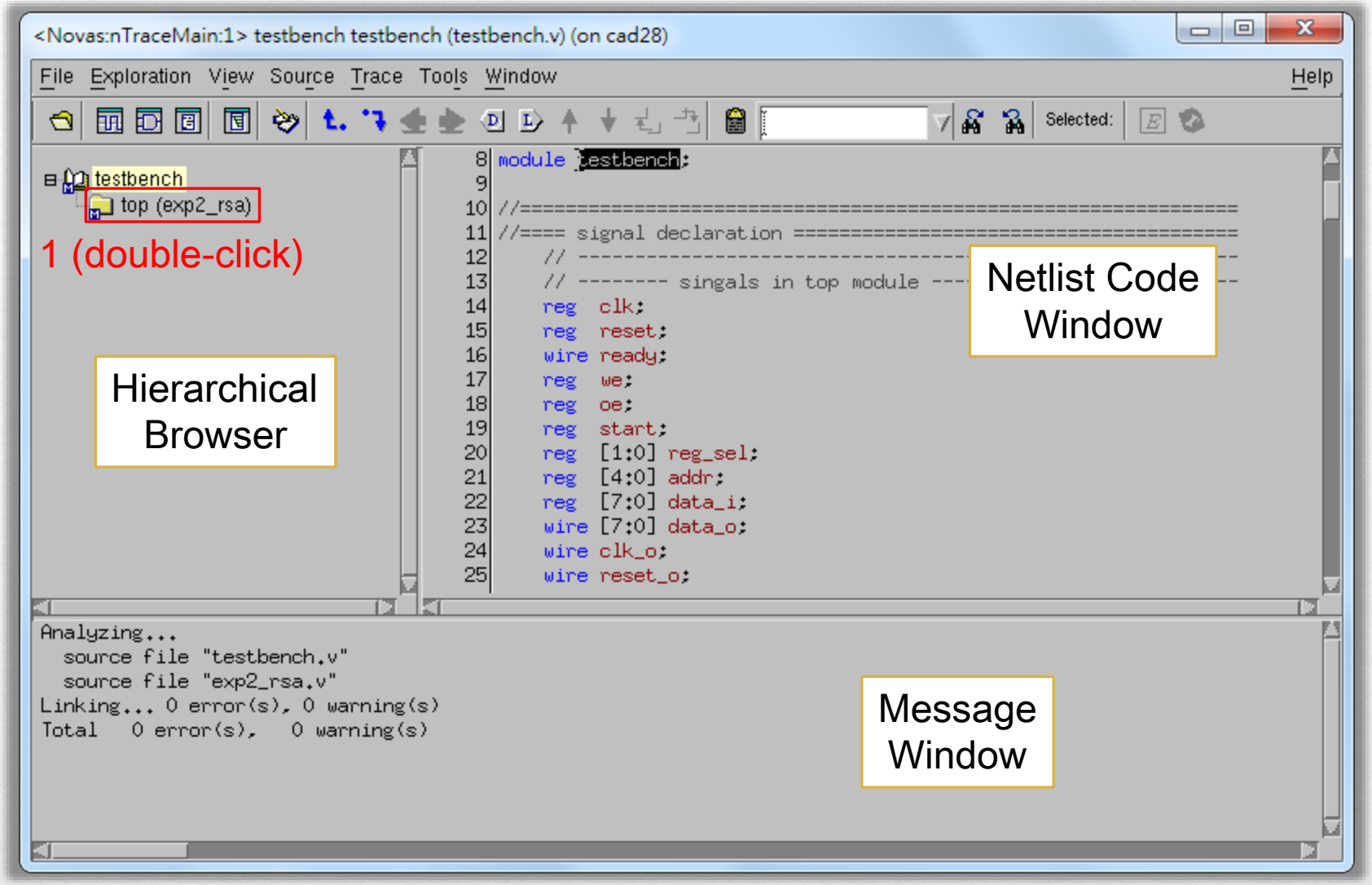
  - Also, the token "&" enable you to use the terminal while Verdi is running in the background.

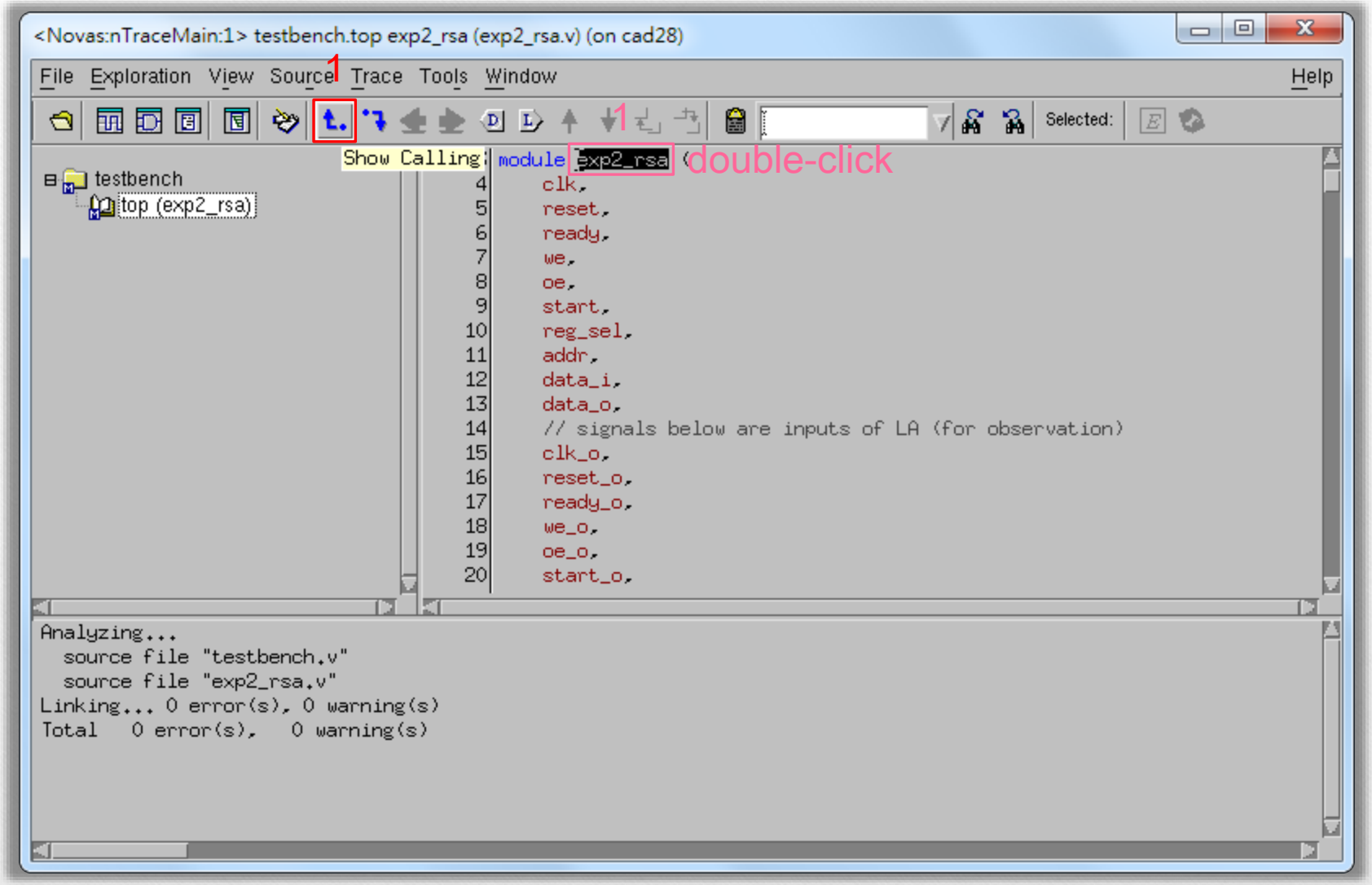


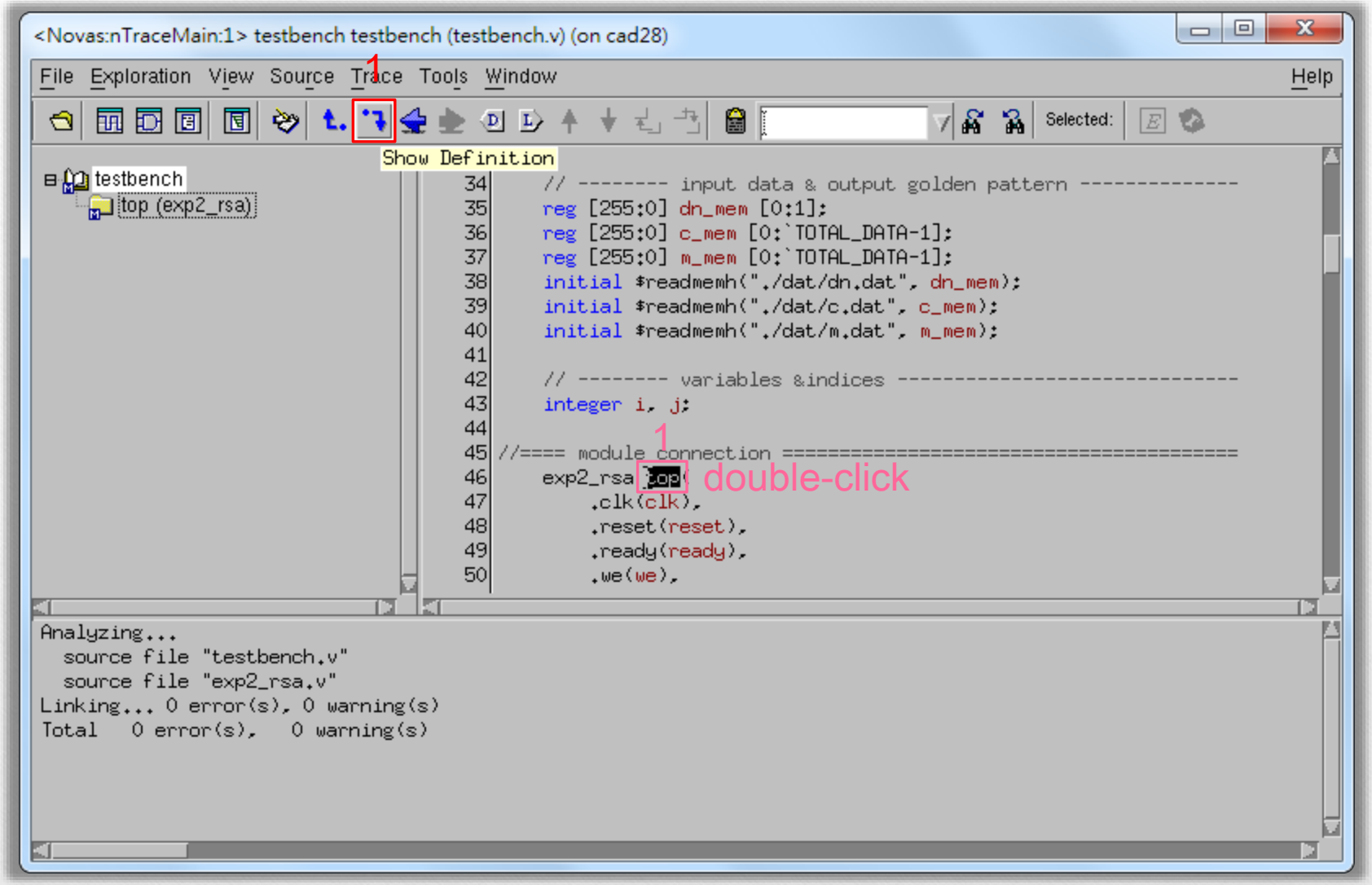
nTrace

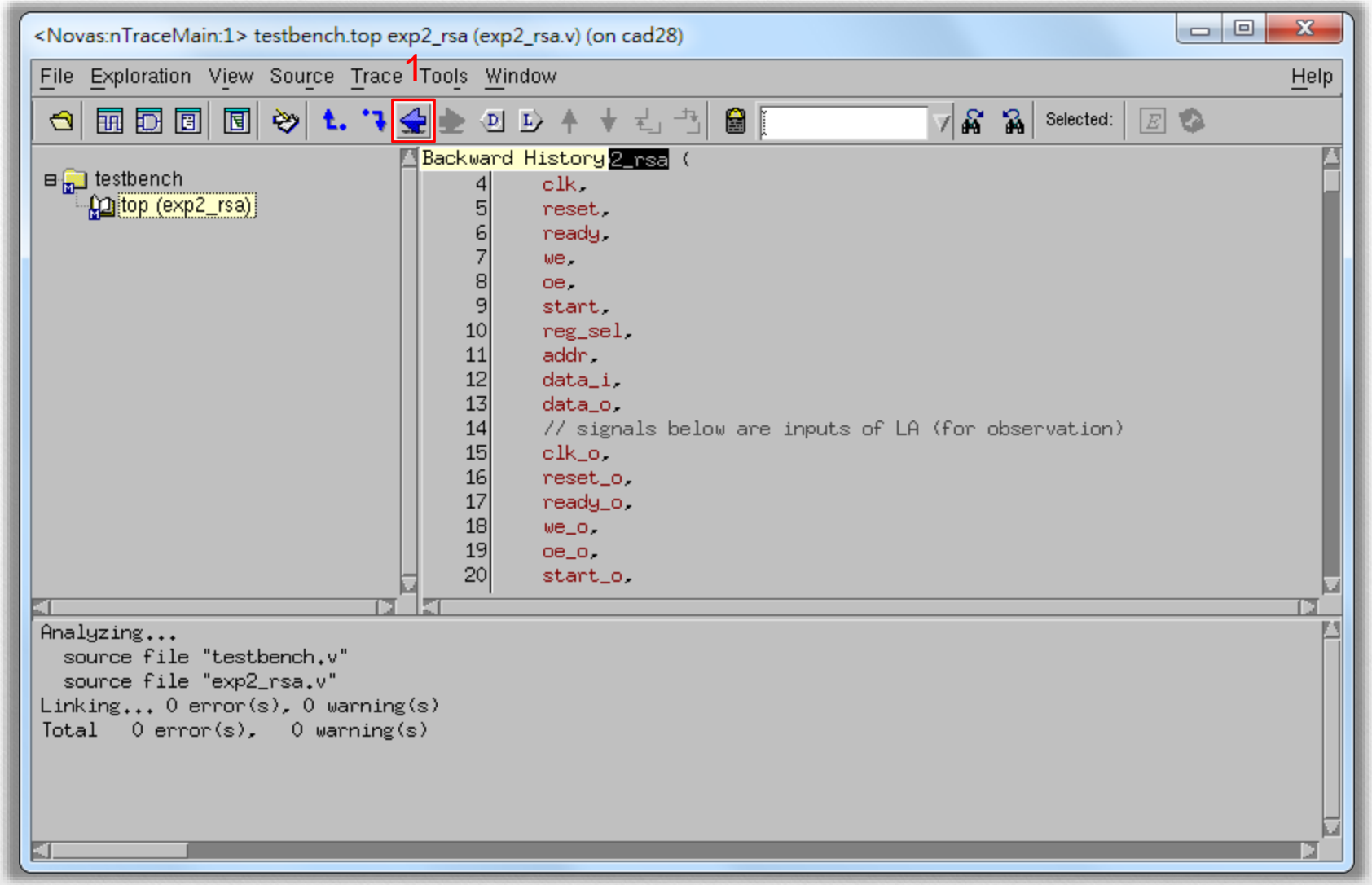

<Novas:nTraceMain:1> (on cad28)
File Exploration View Trace Tools Window Help
1
Selected:
Import Design

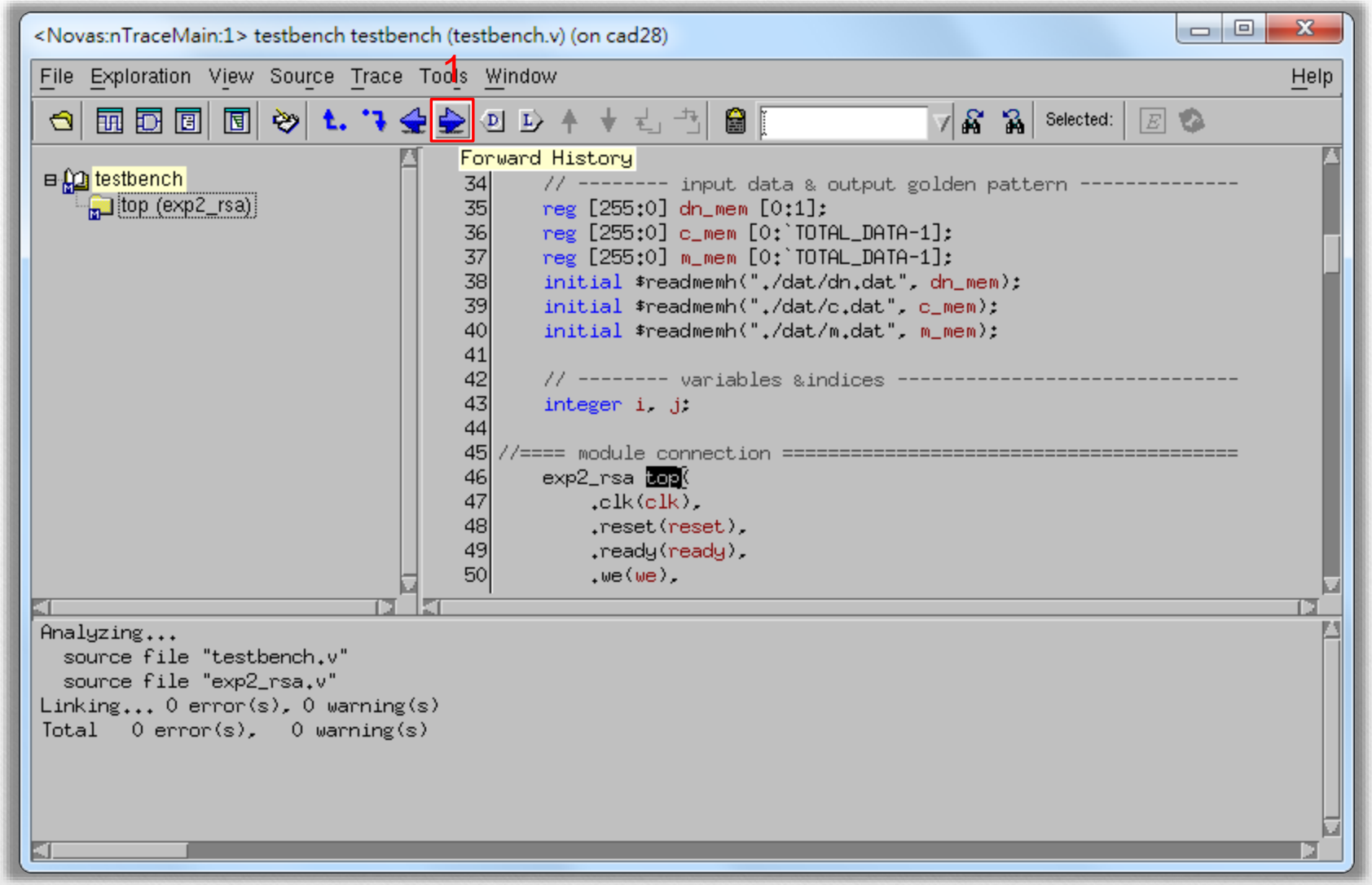

Import Design (on cad28)
From Library
From File
1
Language:
Verilog-2001
2
Virtual Top:
Browse...
Default Directory:
/home/raid1_2/userd/f99021/exp2_rsa
Browse...
/home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.f
Filter:
*.v; *.vc; *.f
4
Add
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
VerdiLog
INCA_libs
VerdiLog
dat
nWaveLog
verdiLog
3
exp2_rsa.f
exp2_rsa.v
testbench.v
Design Files:
-f /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.f
Delete
Delete All
Options...
5
OK
Cancel

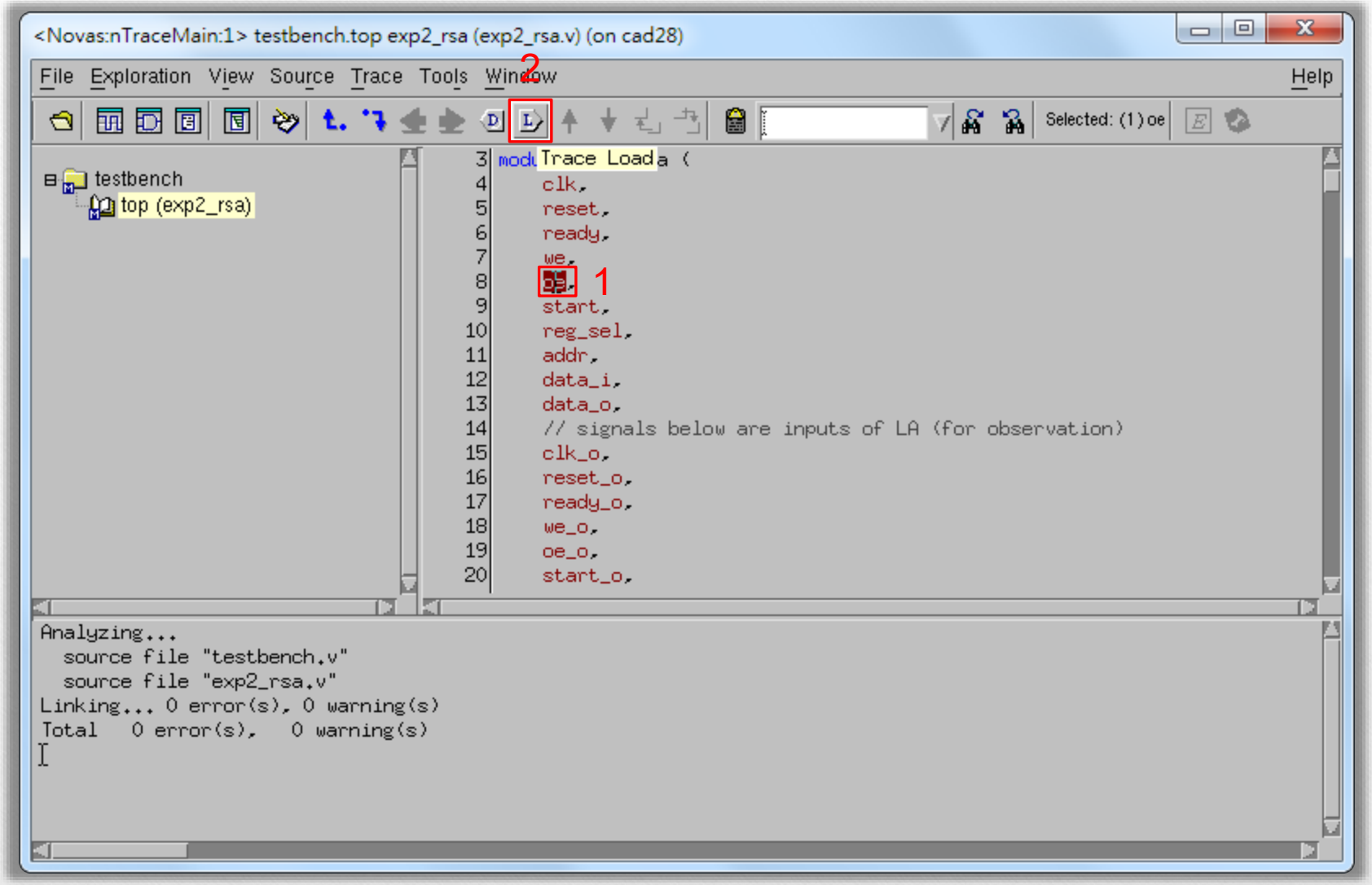

<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
Selected:
testbench
top (exp2_rsa)
1 (double-click)
Hierarchical Browser
8 module testbench;
9
10 //===
11 //==== signal declaration ======================================
12 // ----------
13 // -------- singals in top module ----
14 reg clk;
15 reg reset;
16 wire ready;
17 reg we;
18 reg oe;
19 reg start;
20 reg [1:0] reg_sel;
21 reg [4:0] addr;
22 reg [7:0] data_i;
23 wire [7:0] data_o;
24 wire clk_o;
25 wire reset_o;
Netlist Code Window
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)
Message Window

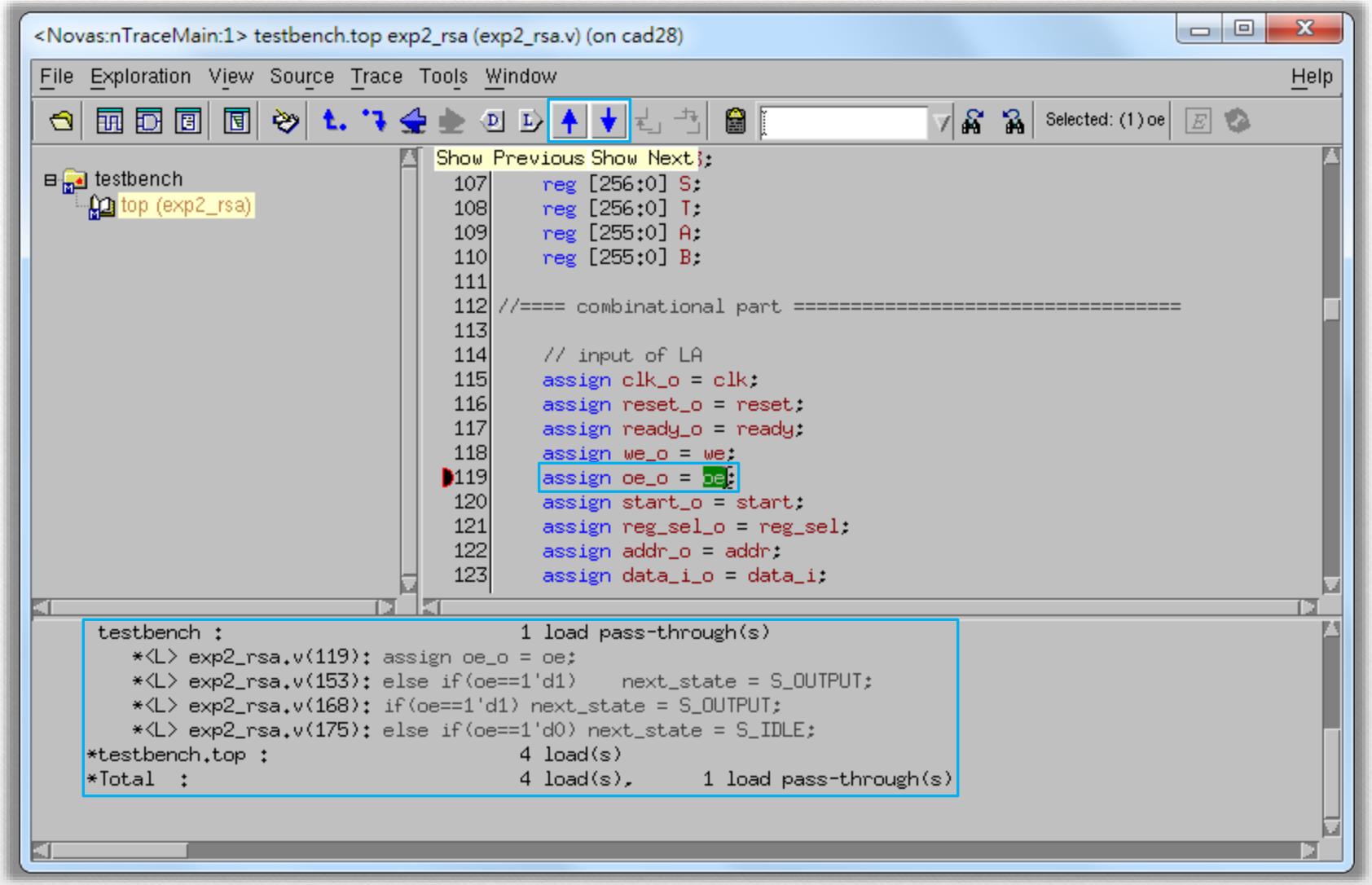

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
1
1
Selected:
Show Calling
testbench
top (exp2_rsa)
module exp2_rsa (
double-click
clk,
reset,
ready,
we,
oe,
start,
reg_sel,
addr,
data_i,
data_o,
// signals below are inputs of LA (for observation)
clk_o,
reset_o,
ready_o,
we_o,
oe_o,
start_o,
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

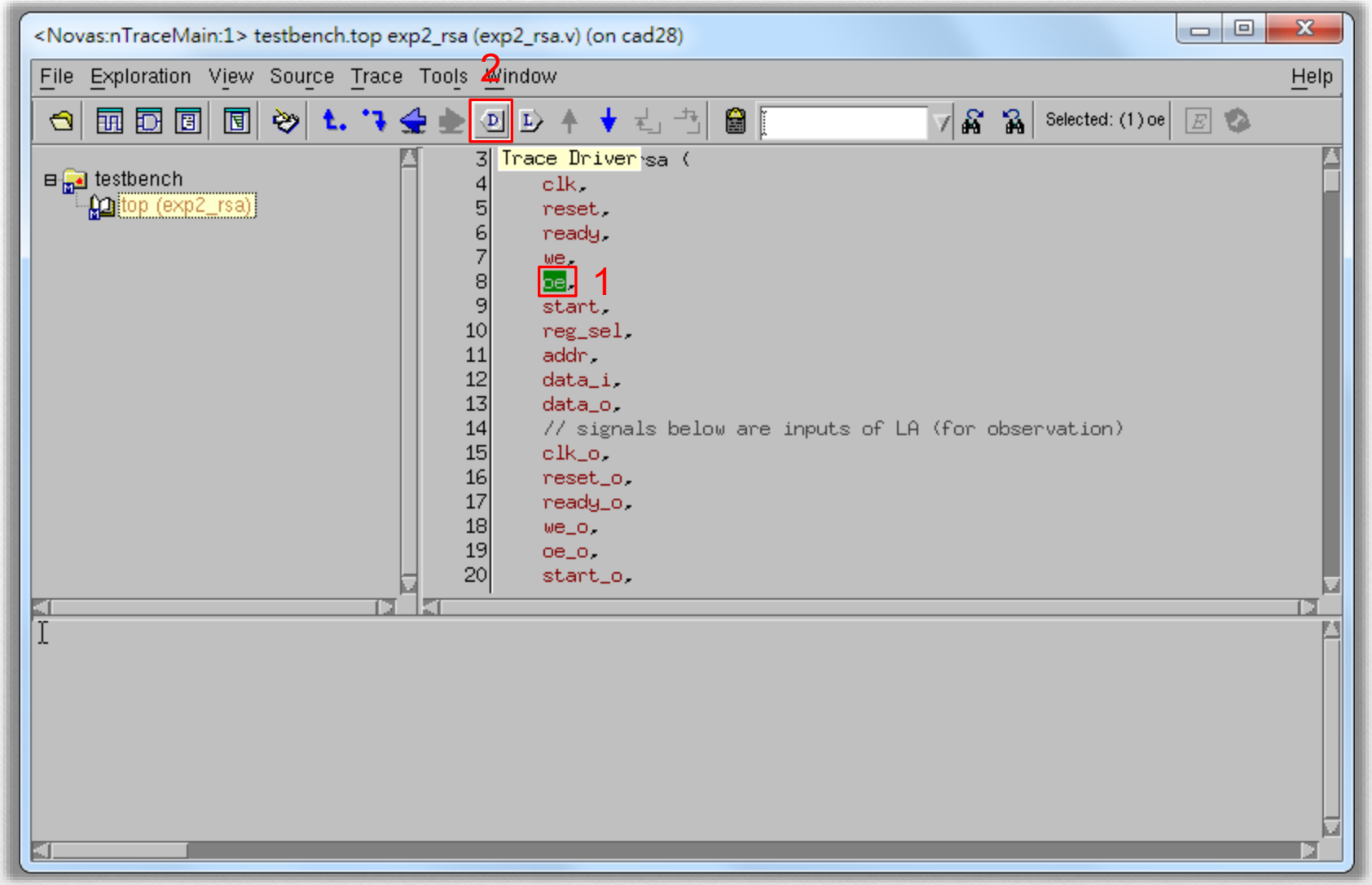

<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
1
Show Definition
Selected:
testbench
top (exp2_rsa)
34 // -------- input data & output golden pattern --------------
35 reg [255:0] dn_mem [0:1];
36 reg [255:0] c_mem [0:`TOTAL_DATA-1];
37 reg [255:0] m_mem [0:`TOTAL_DATA-1];
38 initial $readmemh("./dat/dn.dat", dn_mem);
39 initial $readmemh("./dat/c.dat", c_mem);
40 initial $readmemh("./dat/m.dat", m_mem);
41
42 // -------- variables &indices ------------------------------
43 integer i, j;
44
45 //==== module connection ======================================
1
46 exp2_rsa top(
double-click
47 .clk(clk),
48 .reset(reset),
49 .ready(ready),
50 .we(we),
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

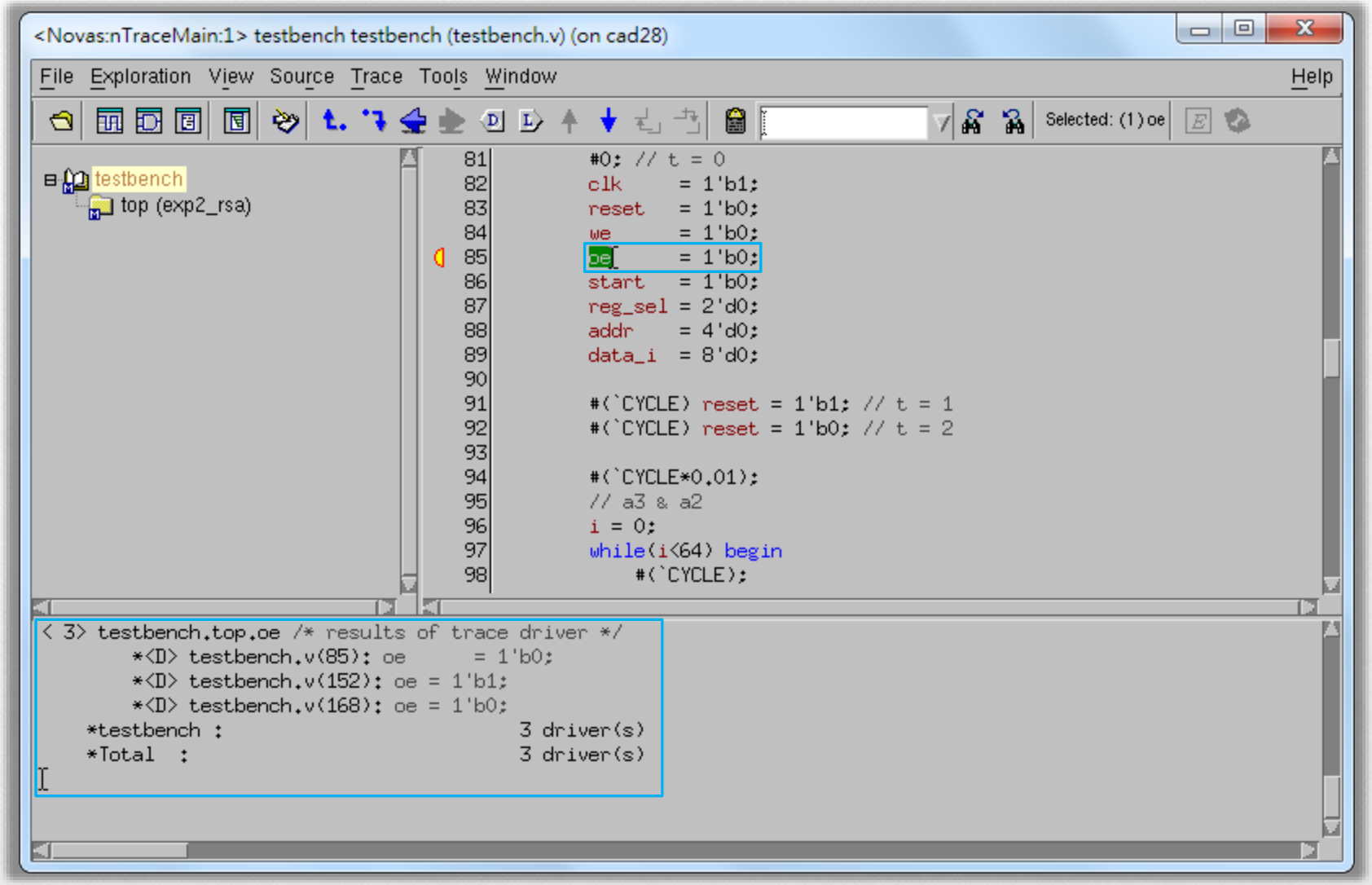

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
1
Selected:
testbench
top (exp2_rsa)
Backward History 2_rsa (
clk,
reset,
ready,
we,
oe,
start,
reg_sel,
addr,
data_i,
data_o,
// signals below are inputs of LA (for observation)
clk_o,
reset_o,
ready_o,
we_o,
oe_o,
start_o,
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)


<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
1
Selected:
Forward History
testbench
top (exp2_rsa)
34 // -------- input data & output golden pattern --------------
35 reg [255:0] dn_mem [0:1];
36 reg [255:0] c_mem [0:`TOTAL_DATA-1];
37 reg [255:0] m_mem [0:`TOTAL_DATA-1];
38 initial $readmemh("./dat/dn.dat", dn_mem);
39 initial $readmemh("./dat/c.dat", c_mem);
40 initial $readmemh("./dat/m.dat", m_mem);
41
42 // -------- variables &indices ------------------------------
43 integer i, j;
44
45 //==== module connection ======================================
46 exp2_rsa top(
47 .clk(clk),
48 .reset(reset),
49 .ready(ready),
50 .we(we),
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

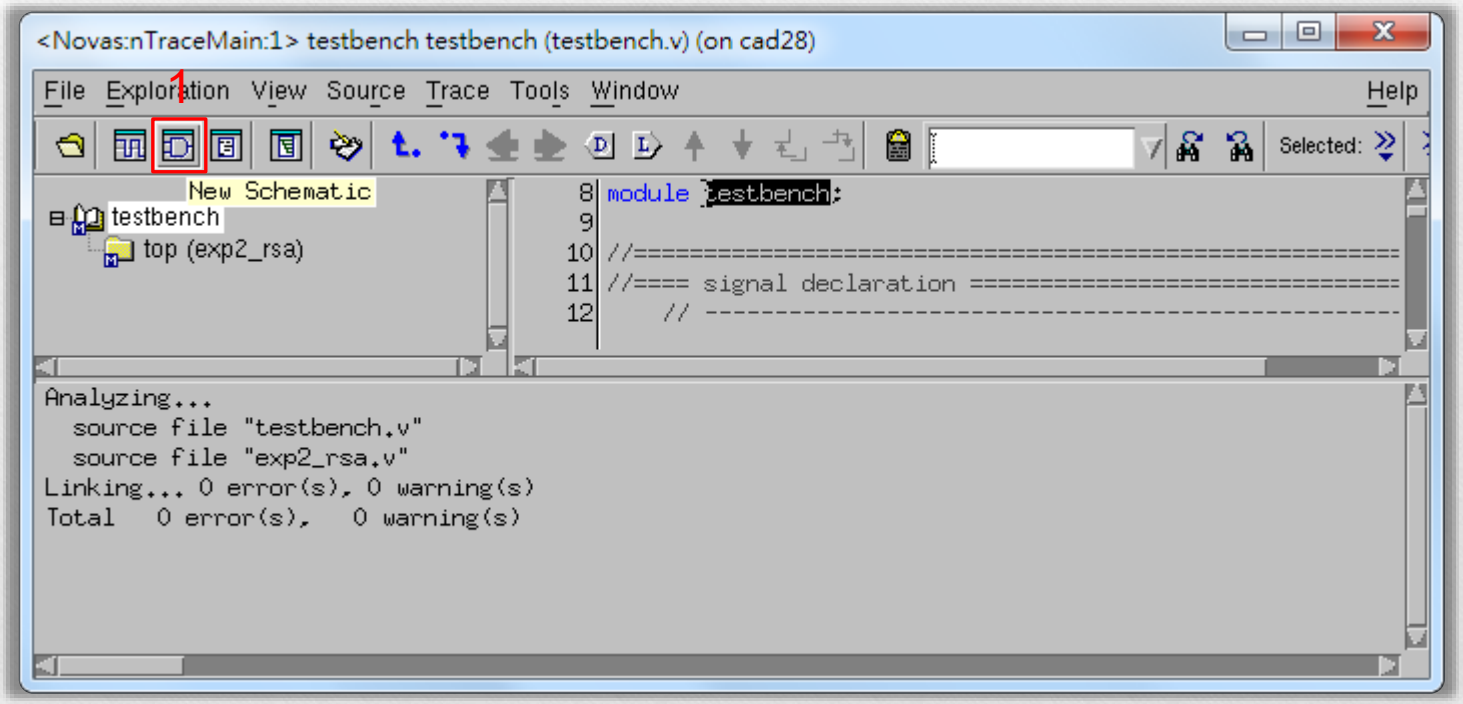

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
2
Selected: (1) oe
testbench
top (exp2_rsa)
3 modu Trace Loada (
4 clk,
5 reset,
6 ready,
7 we,
8
1
9 start,
10 reg_sel,
11 addr,
12 data_i,
13 data_o,
14 // signals below are inputs of LA (for observation)
15 clk_o,
16 reset_o,
17 ready_o,
18 we_o,
19 oe_o,
20 start_o,
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

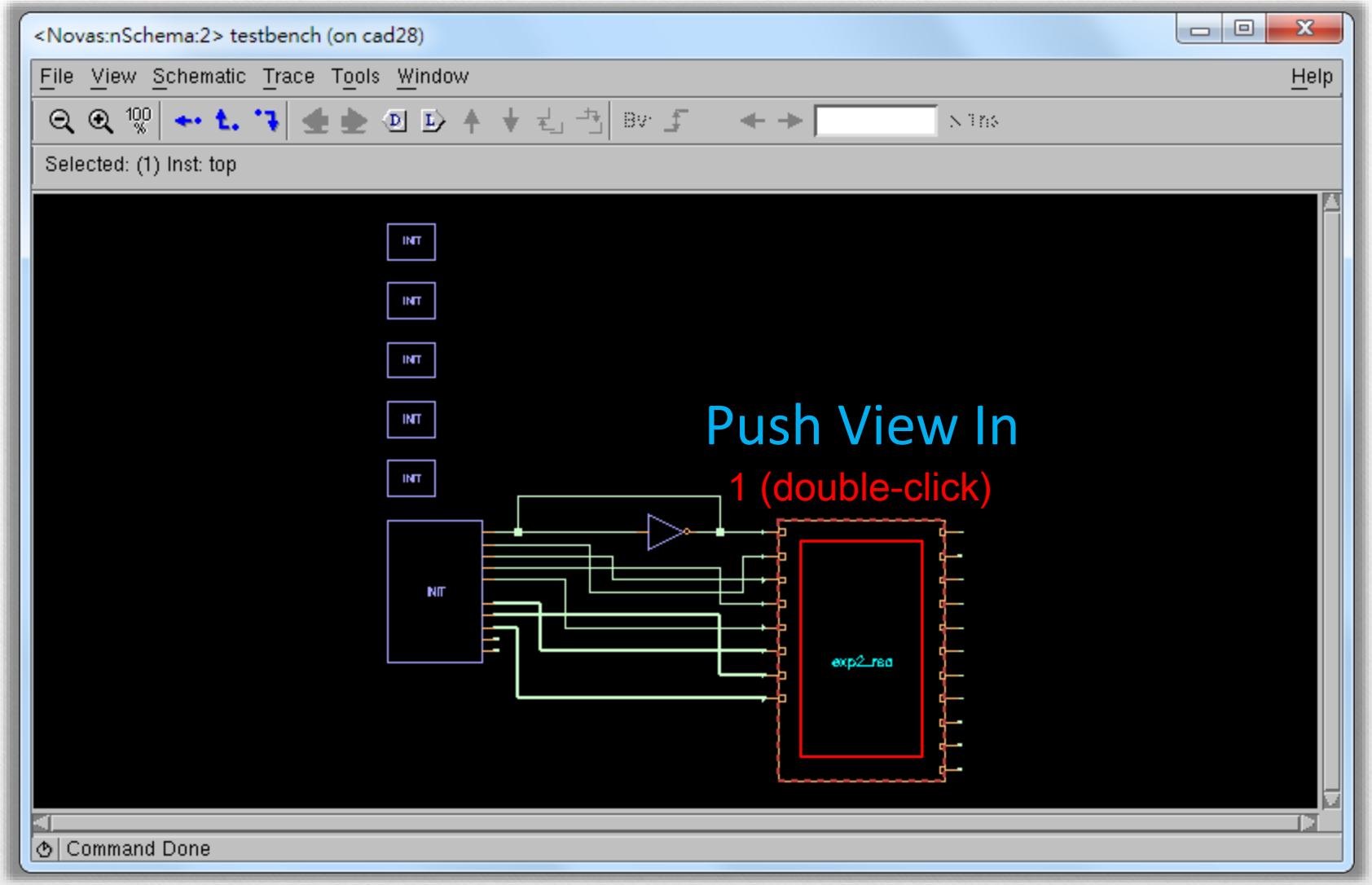

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (1) oe
testbench
top (exp2_rsa)
Show Previous Show Next
107 reg [256:0] S;
108 reg [256:0] T;
109 reg [255:0] A;
110 reg [255:0] B;
111
112 //==== combinational part ================================
113
114 // input of LA
115 assign clk_o = clk;
116 assign reset_o = reset;
117 assign ready_o = ready;
118 assign we_o = we;
119 assign oe_o = oe;
120 assign start_o = start;
121 assign reg_sel_o = reg_sel;
122 assign addr_o = addr;
123 assign data_i_o = data_i;
testbench : 1 load pass-through(s)
*<L> exp2_rsa.v(119): assign oe_o = oe;
*<L> exp2_rsa.v(153): else if(oe==1'd1) next_state = S_OUTPUT;
*<L> exp2_rsa.v(168): if(oe==1'd1) next_state = S_OUTPUT;
*<L> exp2_rsa.v(175): else if(oe==1'd0) next_state = S_IDLE;
*testbench.top : 4 load(s)
*Total : 4 load(s), 1 load pass-through(s)

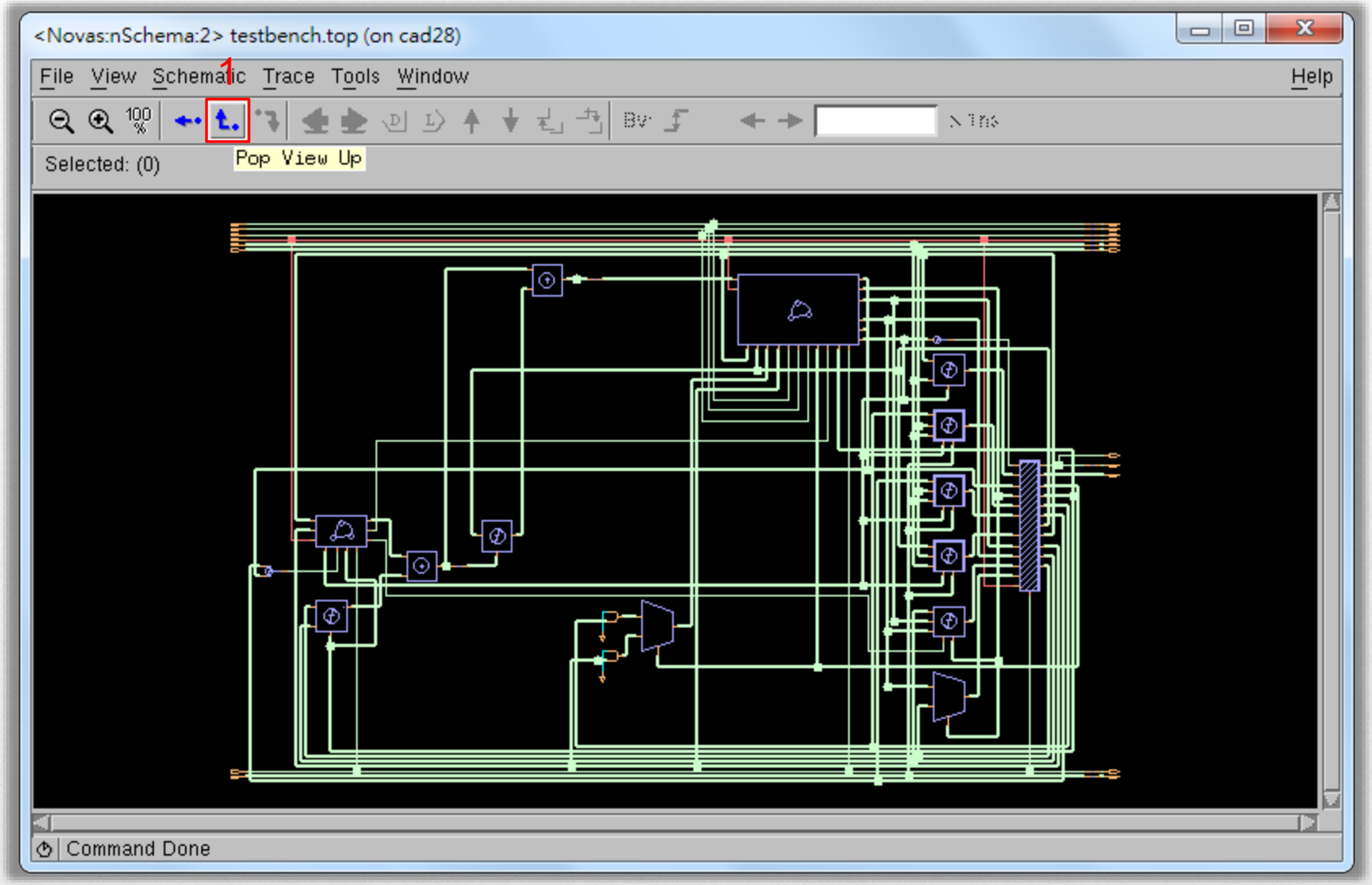

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
2
Selected: (1) oe
testbench
top (exp2_rsa)
Trace Driver sa (
clk,
reset,
ready,
we,
oe,
1
start,
reg_sel,
addr,
data_i,
data_o,
// signals below are inputs of LA (for observation)
clk_o,
reset_o,
ready_o,
we_o,
oe_o,
start_o,

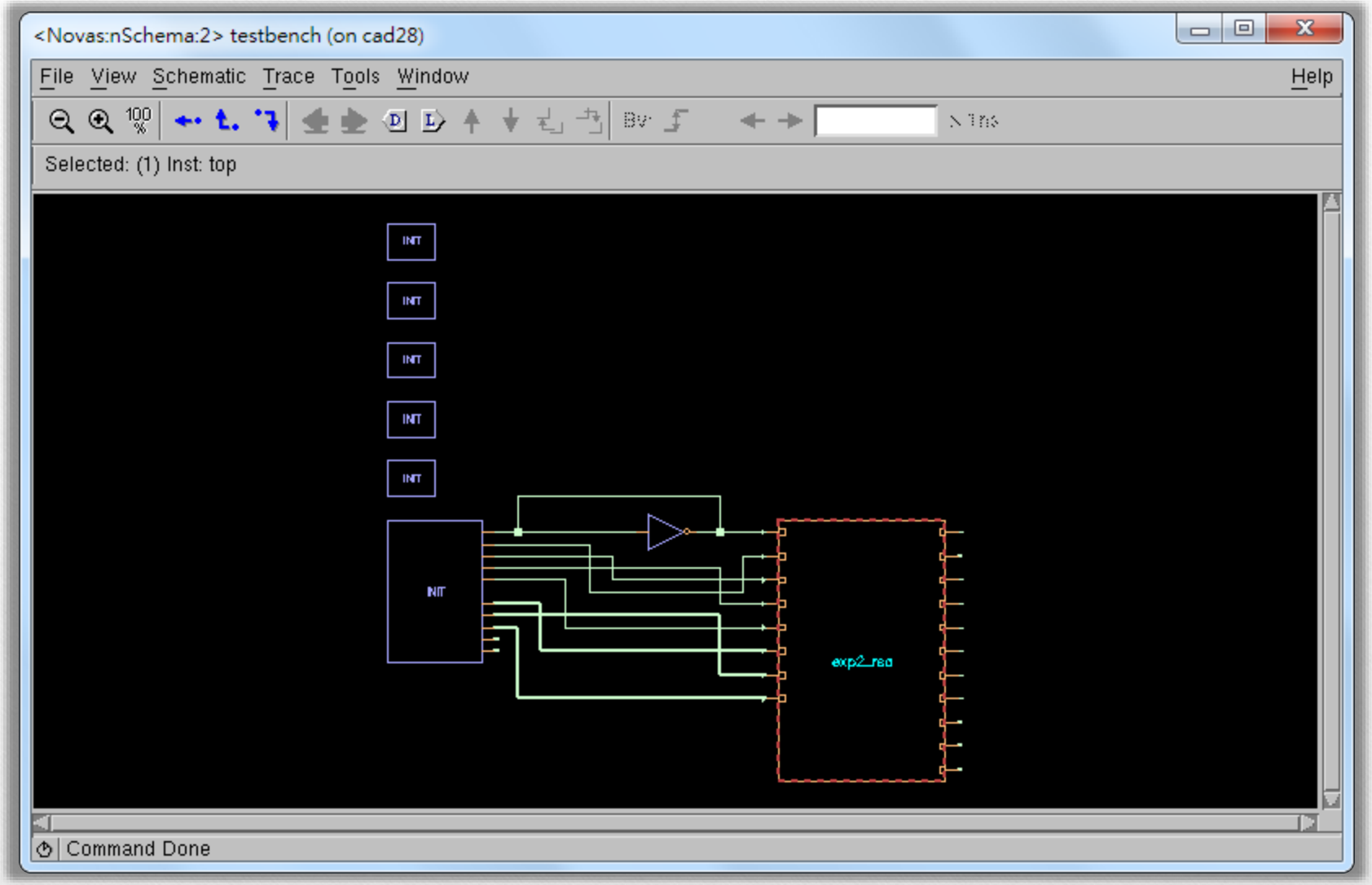

<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (1) oe
testbench
top (exp2_rsa)
81 #0; // t = 0
82 clk = 1'b1;
83 reset = 1'b0;
84 we = 1'b0;
85 oe = 1'b0;
86 start = 1'b0;
87 reg_sel = 2'd0;
88 addr = 4'd0;
89 data_i = 8'd0;
90
91 #(`CYCLE) reset = 1'b1; // t = 1
92 #(`CYCLE) reset = 1'b0; // t = 2
93
94 #(`CYCLE*0.01);
95 // a3 & a2
96 i = 0;
97 while(i<64) begin
98 #(`CYCLE);
< 3> testbench.top.oe /* results of trace driver */
*<D> testbench.v(85): oe = 1'b0;
*<D> testbench.v(152): oe = 1'b1;
*<D> testbench.v(168): oe = 1'b0;
*testbench : 3 driver(s)
*Total : 3 driver(s)

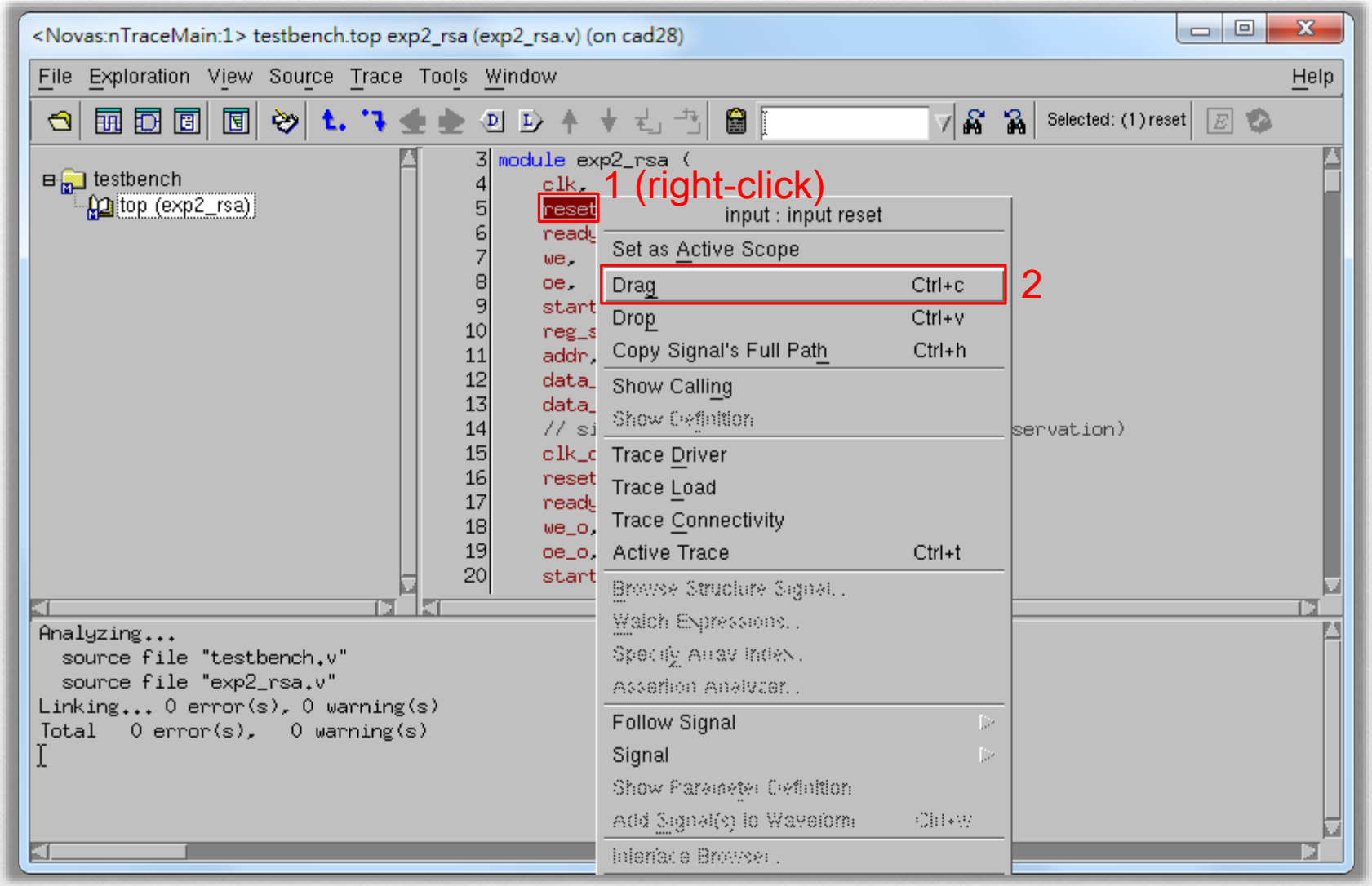
nSchema

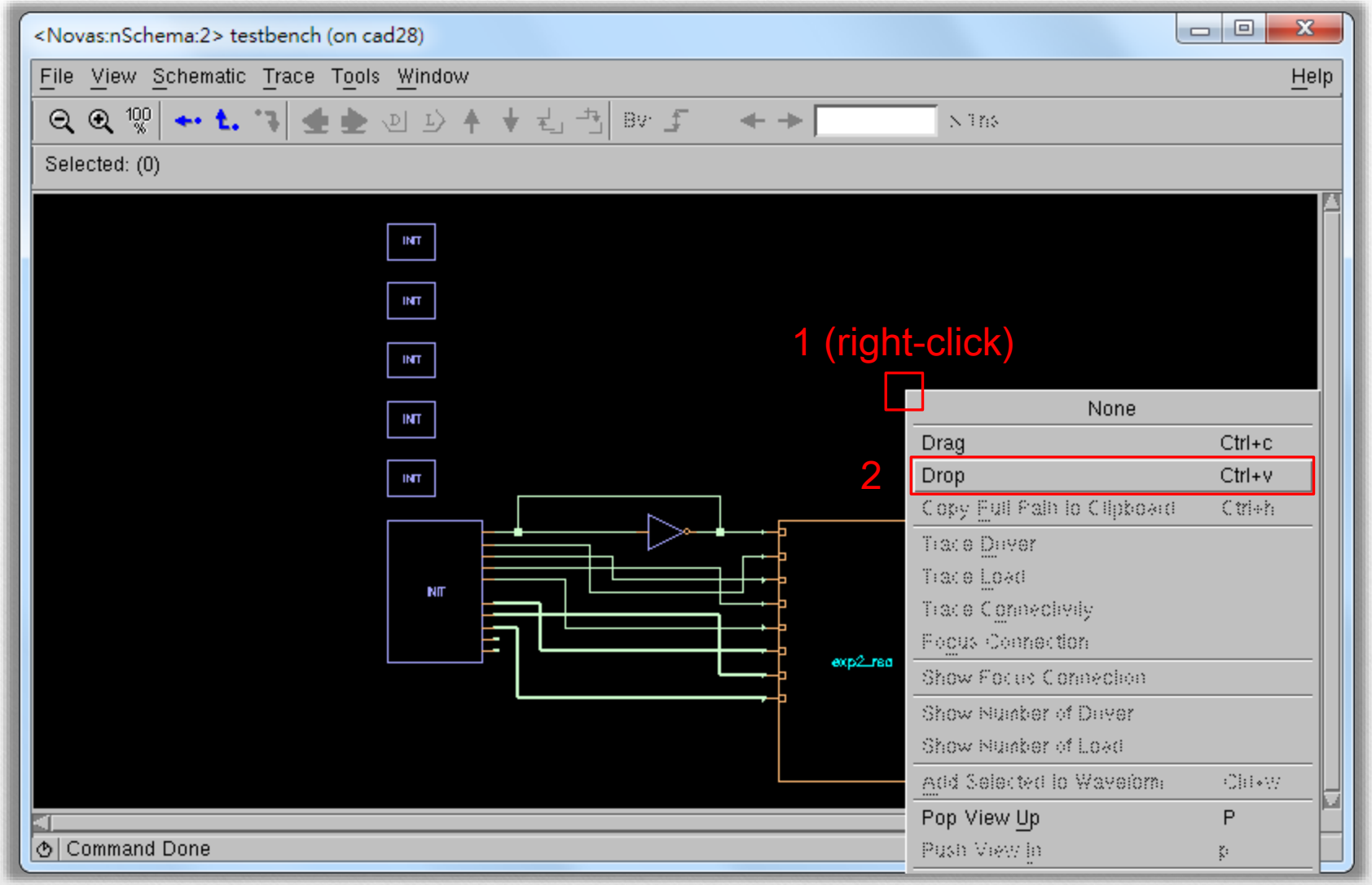

<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
1
New Schematic
Selected:
testbench
top (exp2_rsa)
8 module testbench;
9
10 //===
11 //==== signal declaration ====================================
12 // ---
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

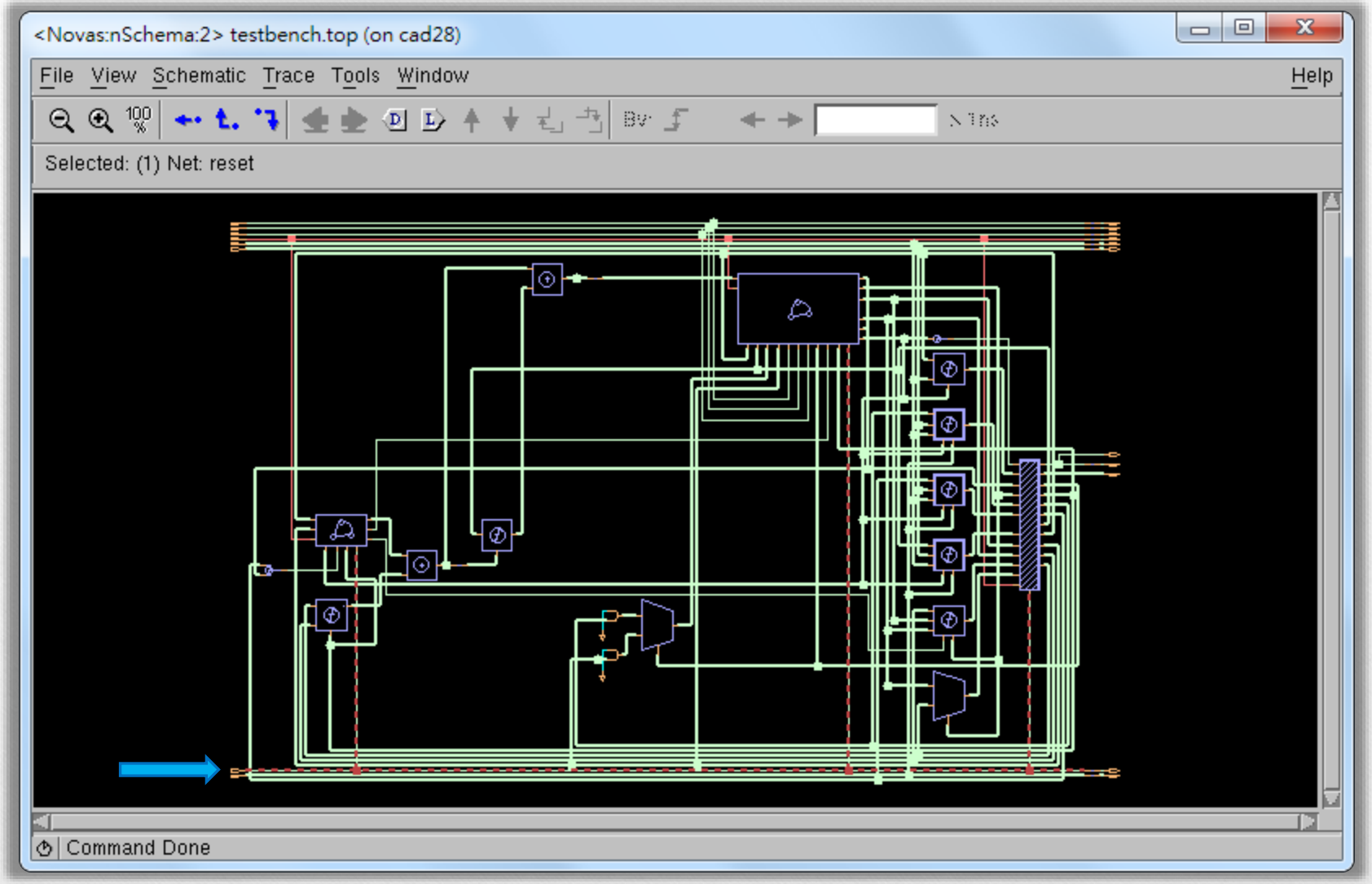

<Novas:nSchema:2> testbench (on cad28)
File View Schematic Trace Tools Window Help
Selected: (1) Inst: top
INT
INT
INT
INT
INT
INT
exp2_rea
Push View In
1 (double-click)
Command Done


<Novas:nSchema:2> testbench.top (on cad28)
File View Schematic Trace Tools Window Help
1
Pop View Up
Selected: (0)
Command Done

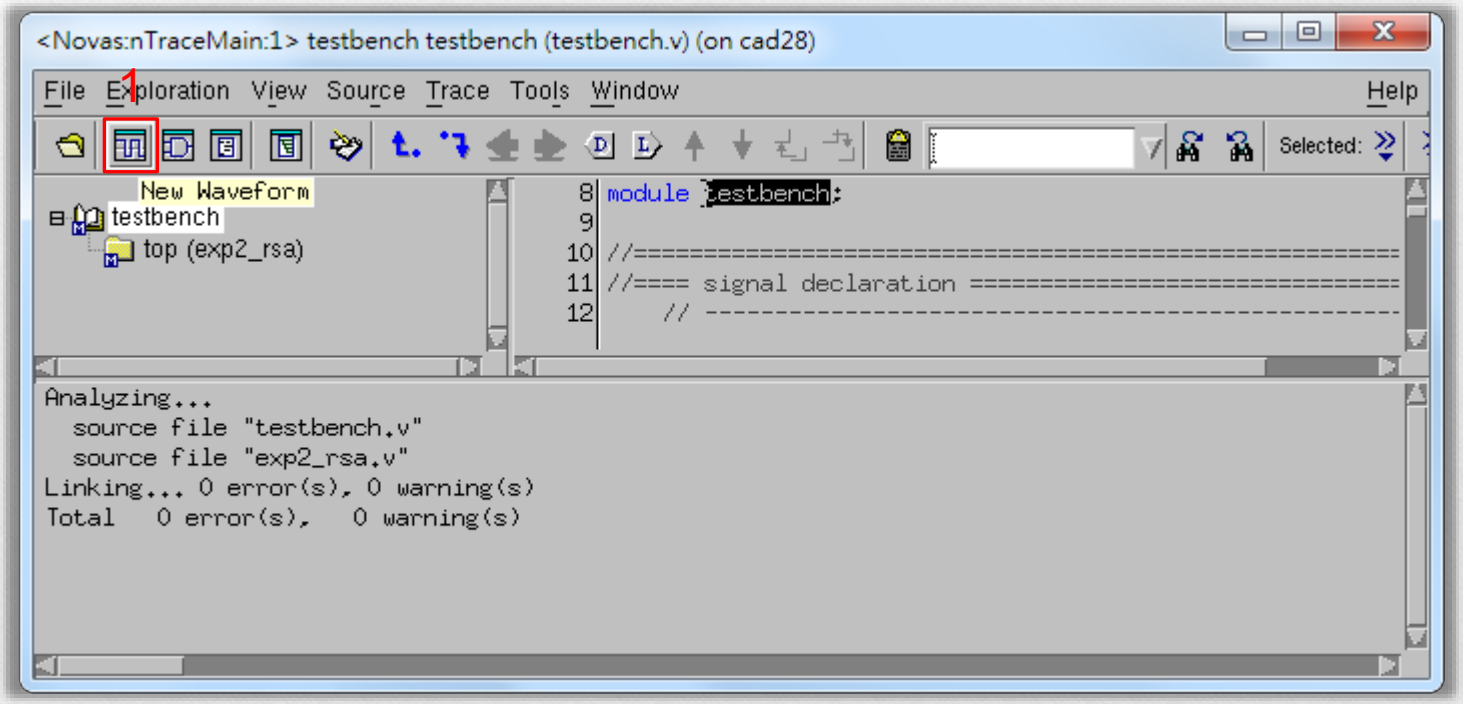

<Novas:nSchema:2> testbench (on cad28)
File View Schematic Trace Tools Window Help
Selected: (1) Inst: top
INT
INT
INT
INT
INT
INIT
exp2_rea
Command Done

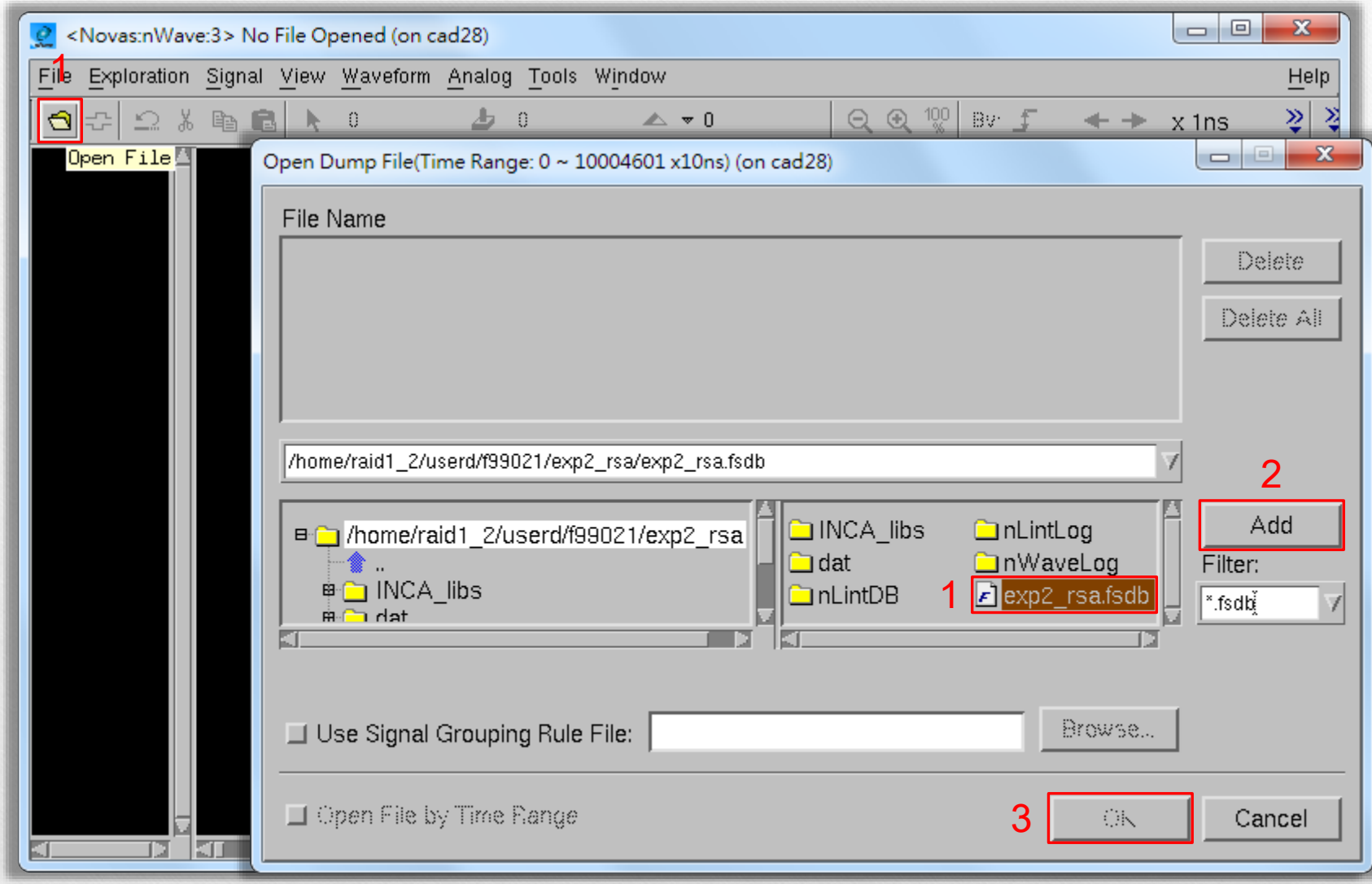

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (1) reset
testbench
top (exp2_rsa)
module exp2_rsa (
clk,
reset
ready
we,
oe,
start
reg_s
addr,
data_
data_
// si
clk_c
reset
ready
we_o,
oe_o,
start
1 (right-click)
input : input reset
Set as Active Scope
Drag Ctrl+c
Drop Ctrl+v
Copy Signal's Full Path Ctrl+h
Show Calling
Show Definition
Trace Driver
Trace Load
Trace Connectivity
Active Trace Ctrl+t
Browse Structure Signal...
Watch Expressions...
Specify Array Index...
Assertion Analyzer...
Follow Signal
Signal
Show Parameter Definition
Add Signal(s) to Waveform Ctrl+w
Interface Browser...
2
servation)
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

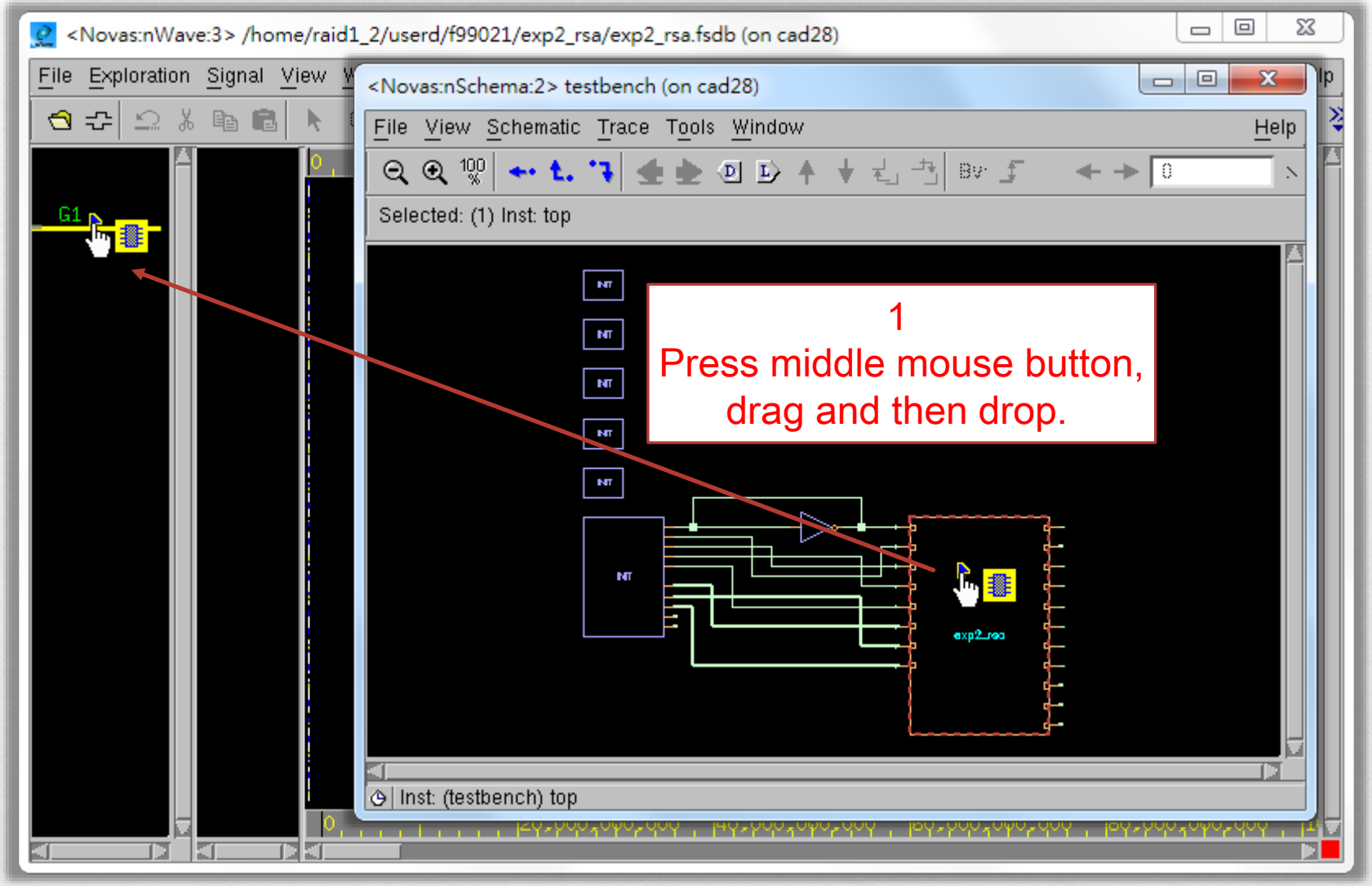

<Novas:nSchema:2> testbench (on cad28)
File View Schematic Trace Tools Window Help
Selected: (0)
INT
INT
INT
INT
INT
INIT
exp2_reg
1 (right-click)
2
None
Drag Ctrl+c
Drop Ctrl+v
Copy Full Path to Clipboard Ctrl+h
Trace Driver
Trace Load
Trace Connectivity
Focus Connection
Show Focus Connection
Show Number of Driver
Show Number of Load
Add Selected to Waveform Ctrl+w
Pop View Up P
Push View In p
Command Done

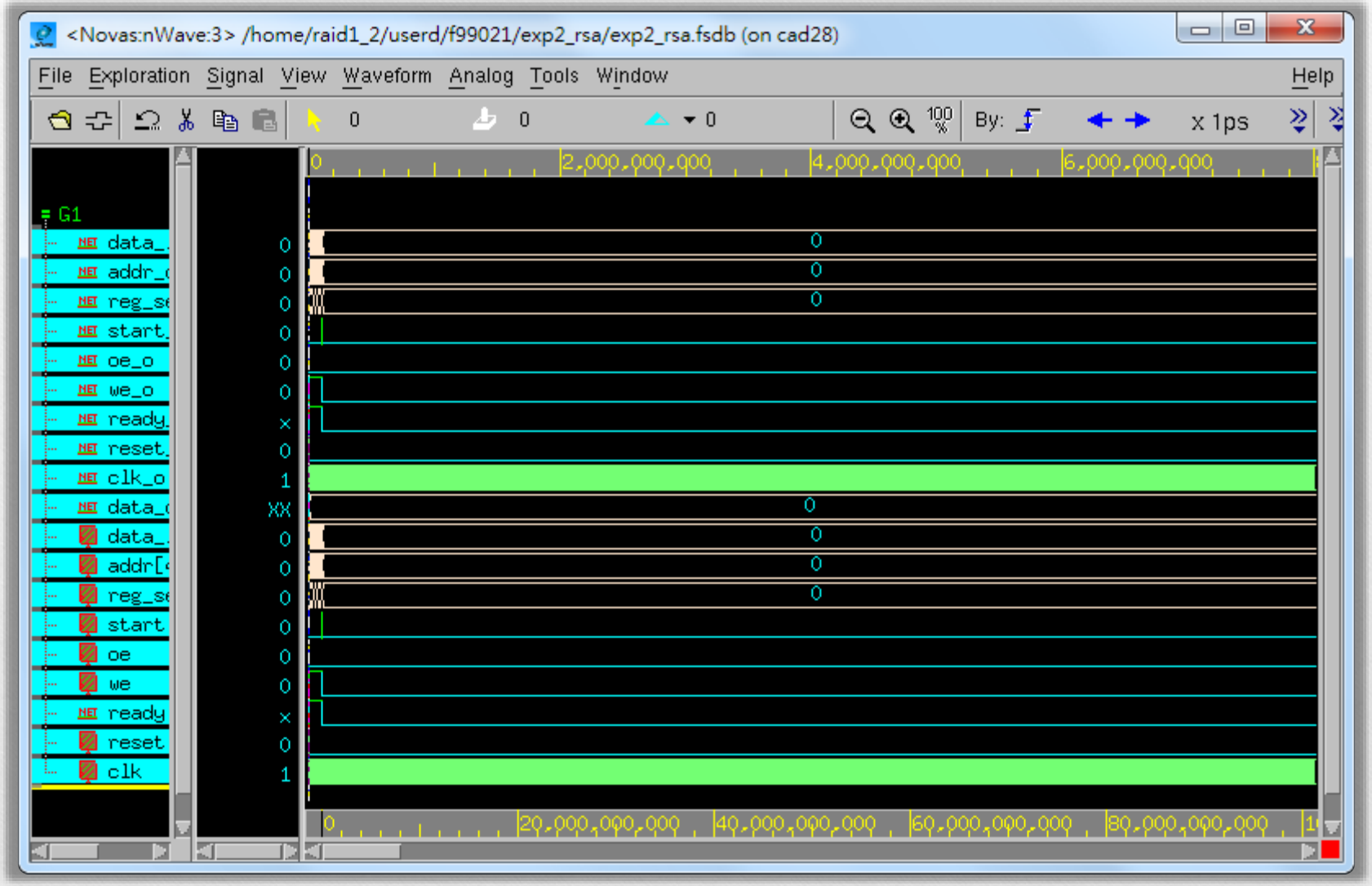

<Novas:nSchema:2> testbench.top (on cad28)
File View Schematic Trace Tools Window Help
Selected: (1) Net: reset
Command Done

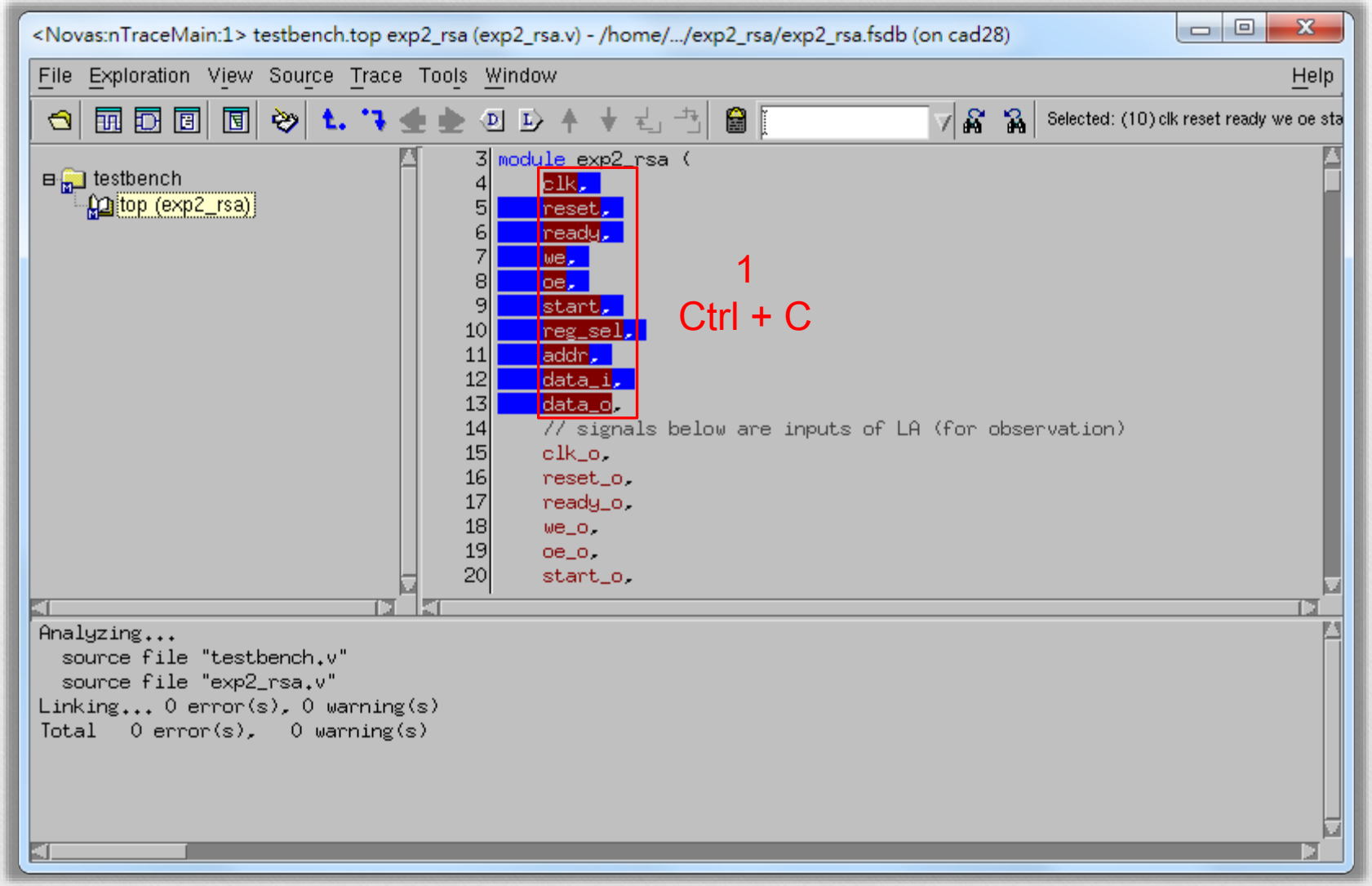
nWave

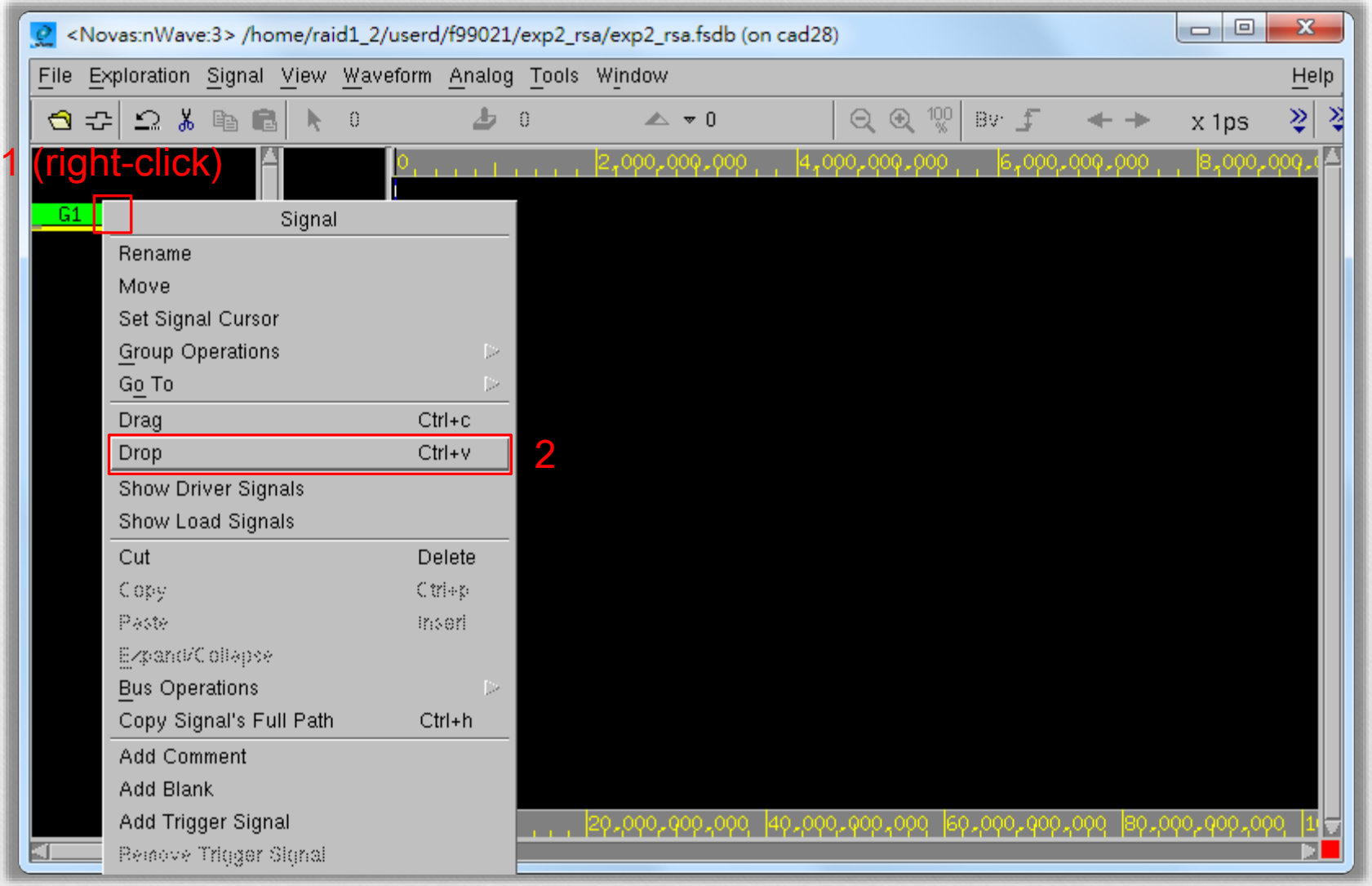

<Novas:nTraceMain:1> testbench testbench (testbench.v) (on cad28)
File Exploration View Source Trace Tools Window Help
Selected:
New Waveform
testbench
top (exp2_rsa)
8 module testbench;
9
10 //=====
11 //==== signal declaration =====
12 // -----
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

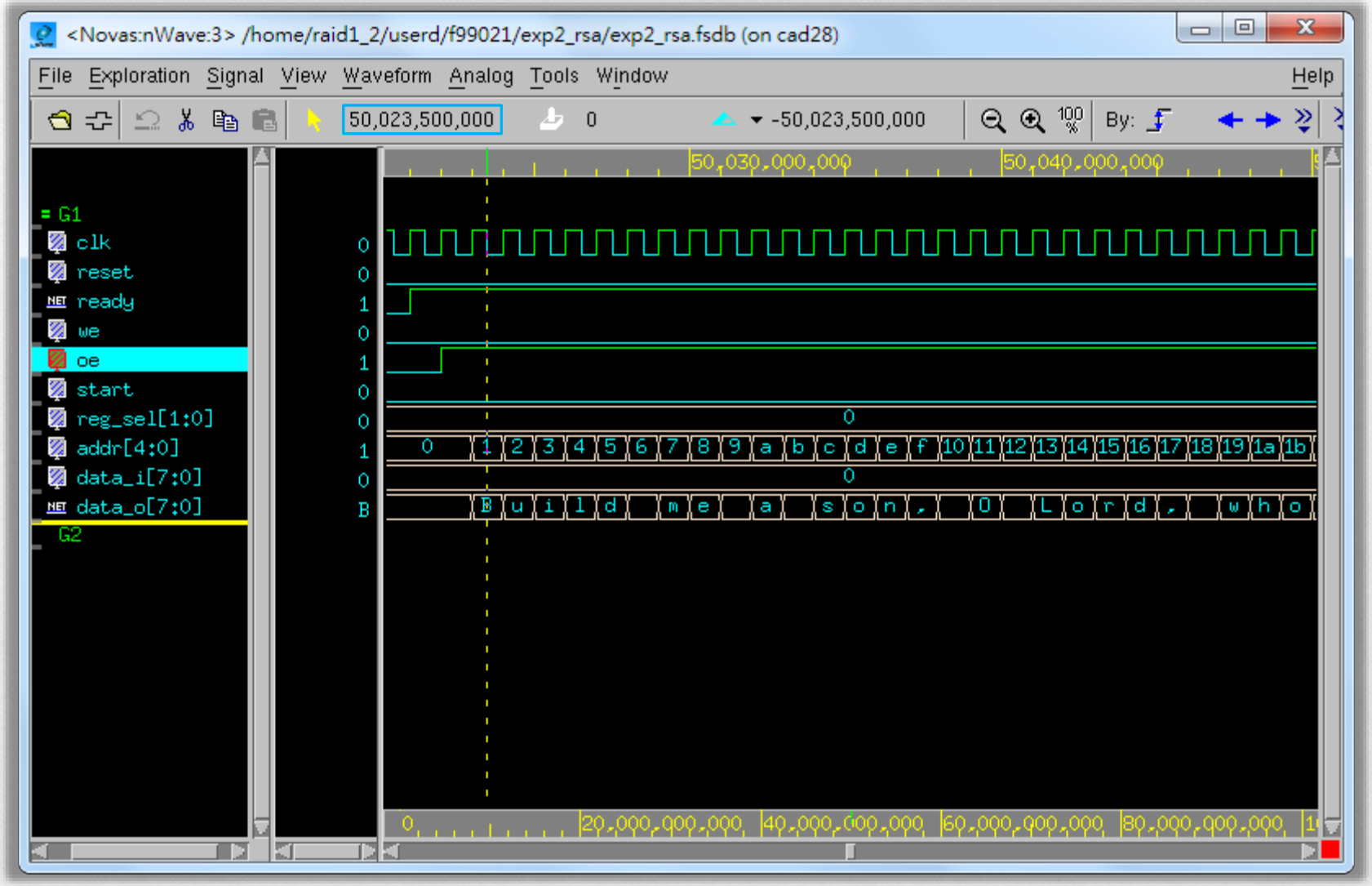

<Novas:nWave:3> No File Opened (on cad28)
File Exploration Signal View Waveform Analog Tools Window Help
1
Open File
Open Dump File(Time Range: 0 ~ 10004601 x10ns) (on cad28)
File Name
Delete
Delete All
/home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb
2
Add
/home/raid1_2/userd/f99021/exp2_rsa
..
INCA_libs
dat
INCA_libs
dat
nLintDB
nLintLog
nWaveLog
1
exp2_rsa.fsdb
Filter:
*.fsdb
Use Signal Grouping Rule File:
Browse...
Open File by Time Range
3
OK
Cancel

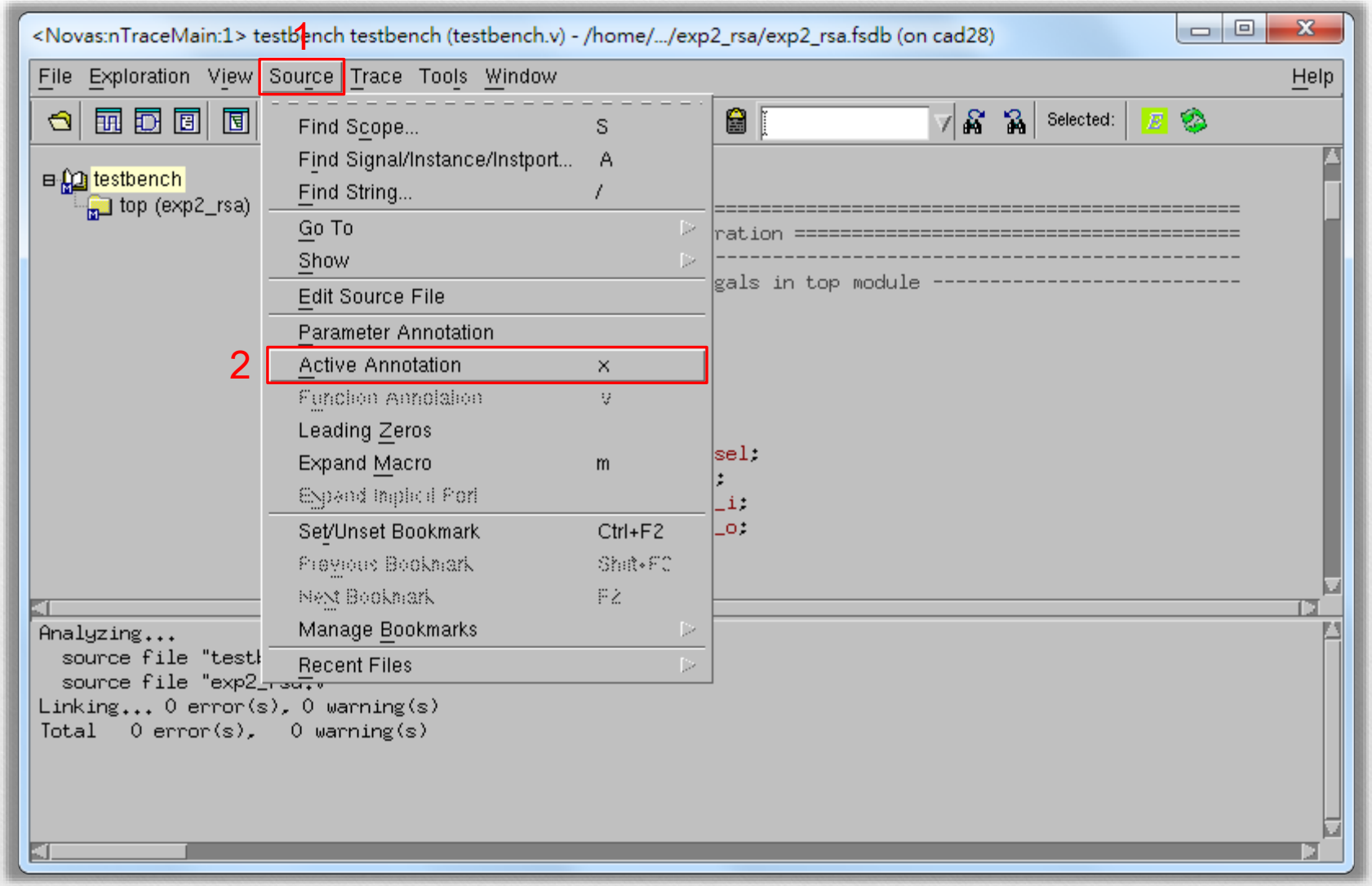

<Novas:nWave:3> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration Signal View
G1
<Novas:nSchema:2> testbench (on cad28)
File View Schematic Trace Tools Window Help
Selected: (1) Inst: top
INT
INT
INT
INT
INT
INT
exp2_rsa
Inst: (testbench) top
1
Press middle mouse button, drag and then drop.

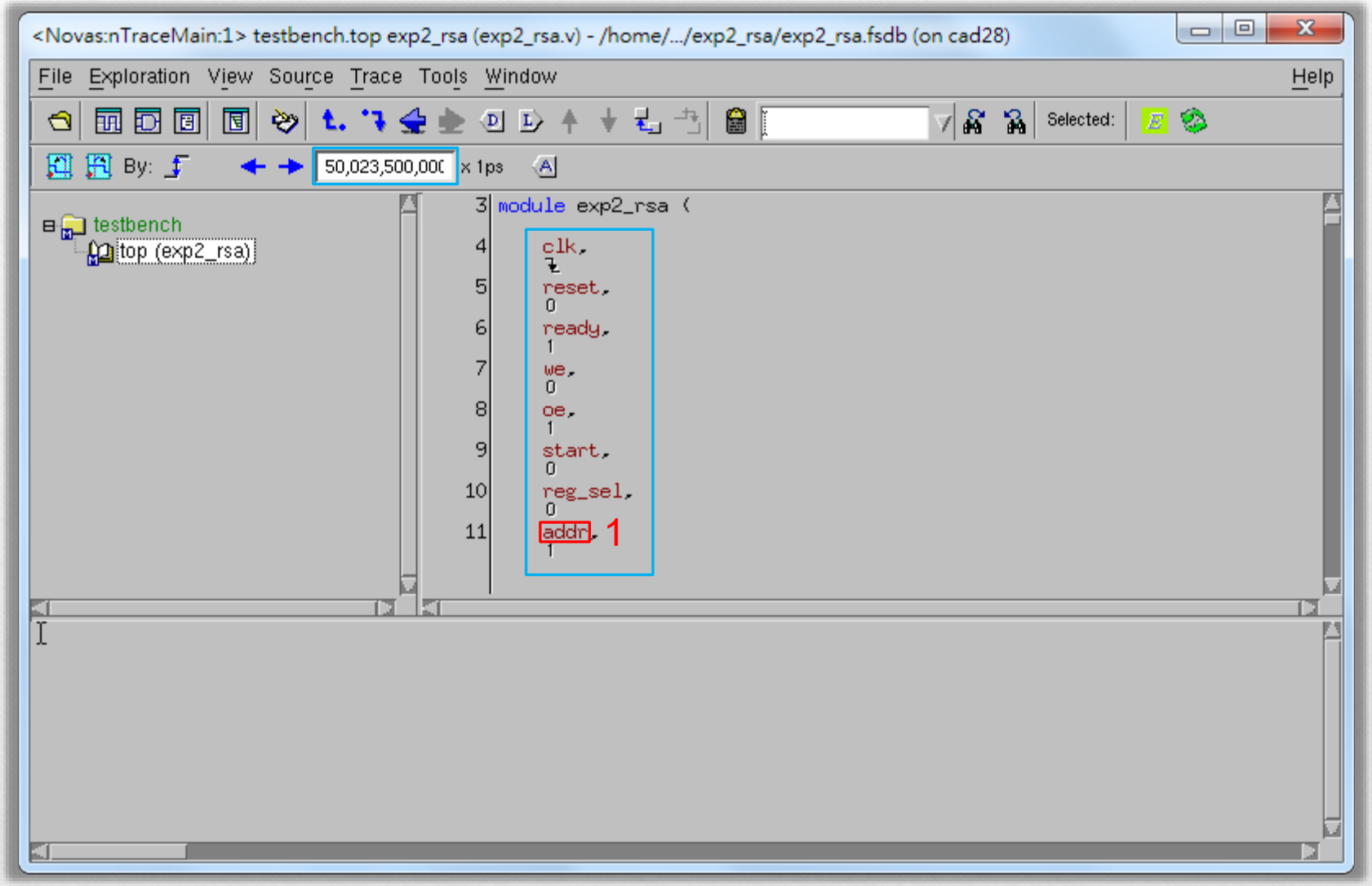

<Novas:nWave:3> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration Signal View Waveform Analog Tools Window Help
By:
x 1ps
G1
data_
addr_
reg_s
start_
oe_o
we_o
ready_
reset_
clk_o
data_
data_
addr[
reg_s
start
oe
we
ready
reset
clk
2,000,000,000
4,000,000,000
6,000,000,000
20,000,000,000
40,000,000,000
60,000,000,000
80,000,000,000

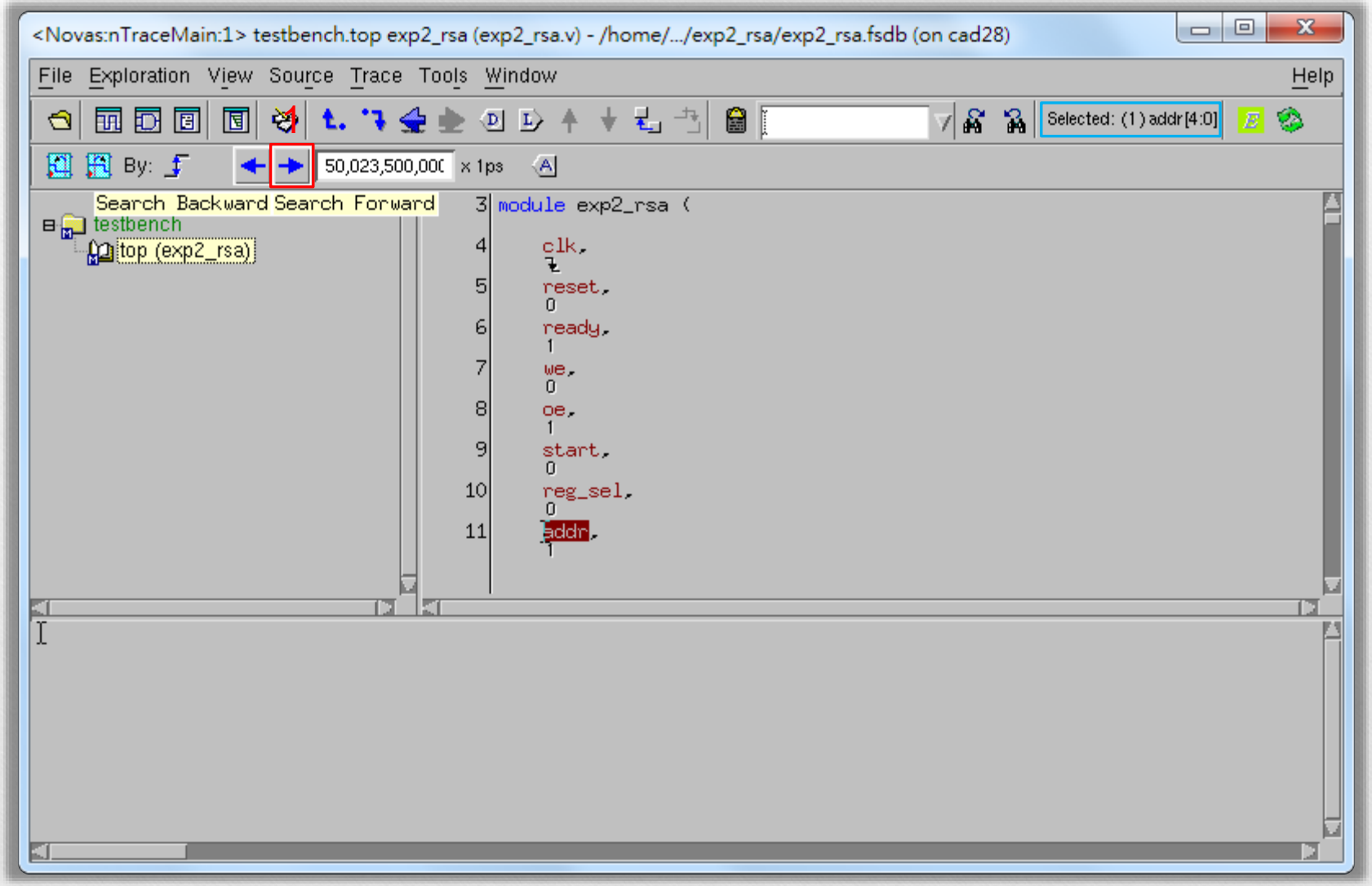

<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) - /home/.../exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (10) clk reset ready we oe sta
testbench
top (exp2_rsa)
3 module exp2_rsa (
4 clk,
5 reset,
6 ready,
7 we,
8 oe,
9 start,
10 reg_sel,
11 addr,
12 data_i,
13 data_o,
14 // signals below are inputs of LA (for observation)
15 clk_o,
16 reset_o,
17 ready_o,
18 we_o,
19 oe_o,
20 start_o,
1
Ctrl + C
Analyzing...
source file "testbench.v"
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)

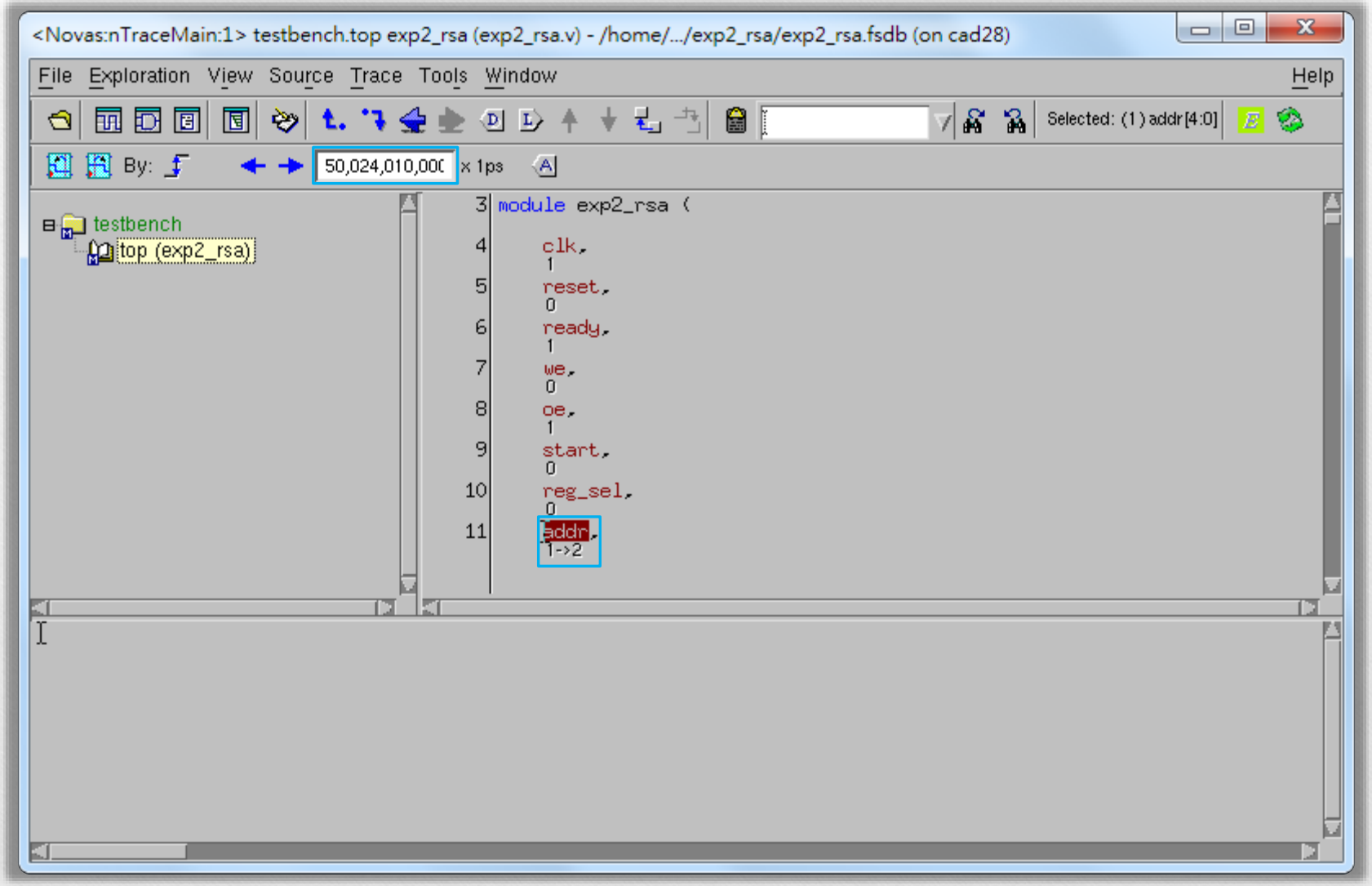

<Novas:nWave:3> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration Signal View Waveform Analog Tools Window Help
x 1ps
1 (right-click)
G1
Signal
Rename
Move
Set Signal Cursor
Group Operations
Go To
Drag Ctrl+c
Drop Ctrl+v
2
Show Driver Signals
Show Load Signals
Cut Delete
Copy Ctrl+p
Paste Insert
Expand/Collapse
Bus Operations
Copy Signal's Full Path Ctrl+h
Add Comment
Add Blank
Add Trigger Signal
Remove Trigger Signal

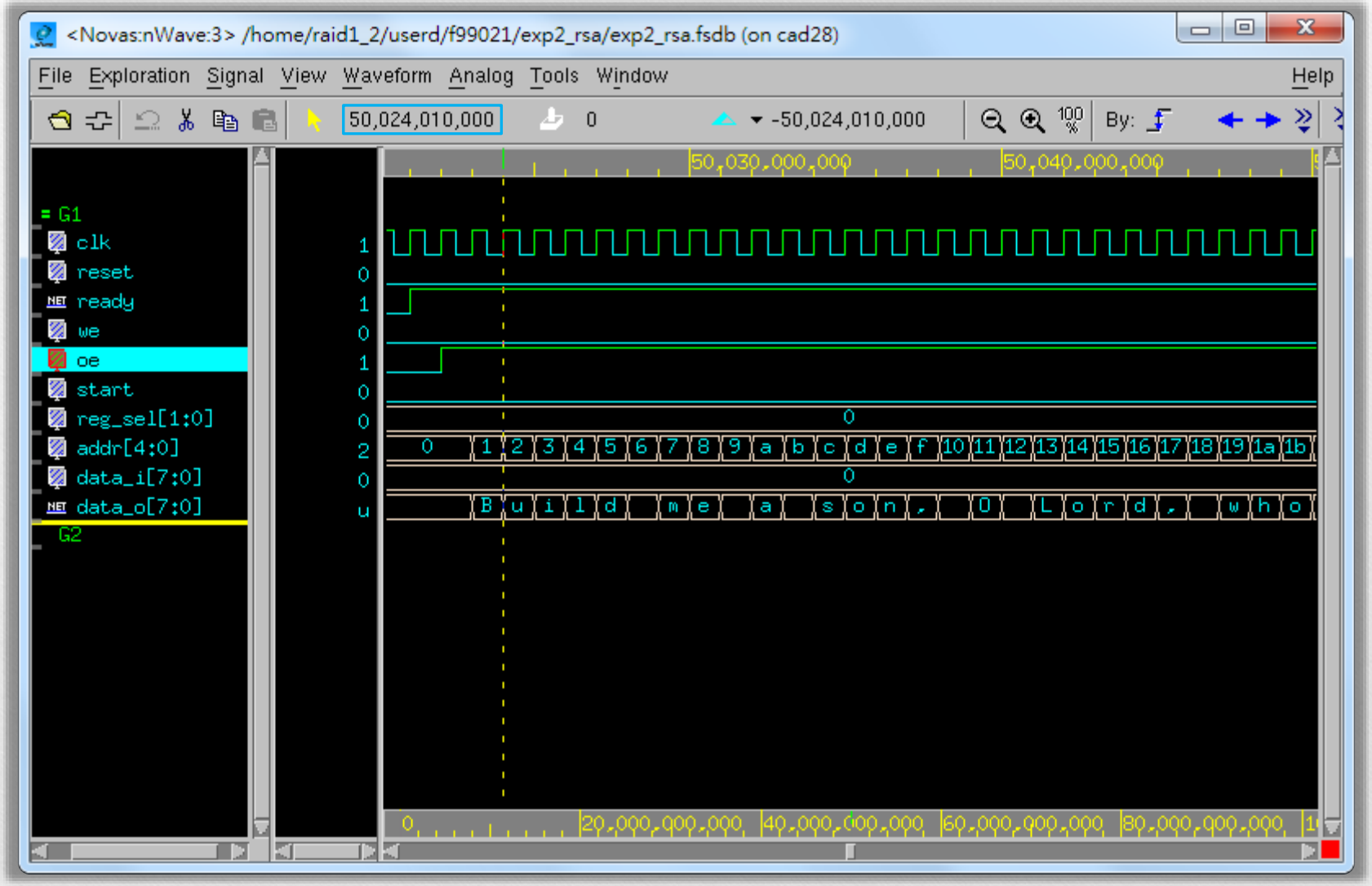

<Novas:nWave:3> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration Signal View Waveform Analog Tools Window Help
50,023,500,000
0
-50,023,500,000
By:
50,030,000,000
50,040,000,000
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
0
0
1
0
1
0
0
1
0
B
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 12 13 14 15 16 17 18 19 1a 1b
0
B u i l d m e a s o n , 0 L o r d , w h o
0
20,000,000,000
40,000,000,000
60,000,000,000
80,000,000,000


1
2
<Novas:nTraceMain:1> testbench testbench (testbench.v) - /home/.../exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration View Source Trace Tools Window Help
Selected:
testbench
top (exp2_rsa)
Find Scope... S
Find Signal/Instance/Instport... A
Find String... /
Go To
Show
Edit Source File
Parameter Annotation
Active Annotation x
Function Annotation v
Leading Zeros
Expand Macro m
Expand Implicit Port
Set/Unset Bookmark Ctrl+F2
Previous Bookmark Shift+F2
Next Bookmark F2
Manage Bookmarks
Recent Files
ration
gals in top module
sel;
_i;
_o;
Analyzing...
source file "testb
source file "exp2_rsa.v"
Linking... 0 error(s), 0 warning(s)
Total 0 error(s), 0 warning(s)


<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) - /home/.../exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration View Source Trace Tools Window Help
Selected:
By:
50,023,500,000
x 1ps
testbench
top (exp2_rsa)
3 module exp2_rsa (
4 clk,
5 reset,
6 ready,
7 we,
8 oe,
9 start,
10 reg_sel,
11 addr,
1


<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) - /home/.../exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (1) addr[4:0]
By:
50,023,500,000
x 1ps
Search Backward Search Forward
testbench
top (exp2_rsa)
3 module exp2_rsa (
4 clk,
5 reset,
6 ready,
7 we,
8 oe,
9 start,
10 reg_sel,
11 addr,


<Novas:nTraceMain:1> testbench.top exp2_rsa (exp2_rsa.v) - /home/.../exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration View Source Trace Tools Window Help
Selected: (1) addr[4:0]
By:
50,024,010,000
x 1ps
testbench
top (exp2_rsa)
3 module exp2_rsa (
4 clk,
1
5 reset,
0
6 ready,
1
7 we,
0
8 oe,
1
9 start,
0
10 reg_sel,
0
11 addr,
1->2


<Novas:nWave:3> /home/raid1_2/userd/f99021/exp2_rsa/exp2_rsa.fsdb (on cad28)
File Exploration Signal View Waveform Analog Tools Window Help
50,024,010,000
0
-50,024,010,000
By:
50,030,000,000
50,040,000,000
G1
clk
reset
ready
we
oe
start
reg_sel[1:0]
addr[4:0]
data_i[7:0]
data_o[7:0]
G2
1
0
1
0
1
0
0
2
0
u
0
0 1 2 3 4 5 6 7 8 9 a b c d e f 10 11 12 13 14 15 16 17 18 19 1a 1b
0
B u i l d m e a s o n , 0 L o r d , w h o
0
20,000,000,000
40,000,000,000
60,000,000,000
80,000,000,000

The End.

Any question?

Reference

1. "Cadence NC-Verilog Simulator Tutorial“ by Cadence
2. "Introduction to Verdi" by Abel Hu
3. "Verdi^3 datasheet" by Synopsys