Qsys on Quartus 15.0 Tutorial for lab_bonus_SW

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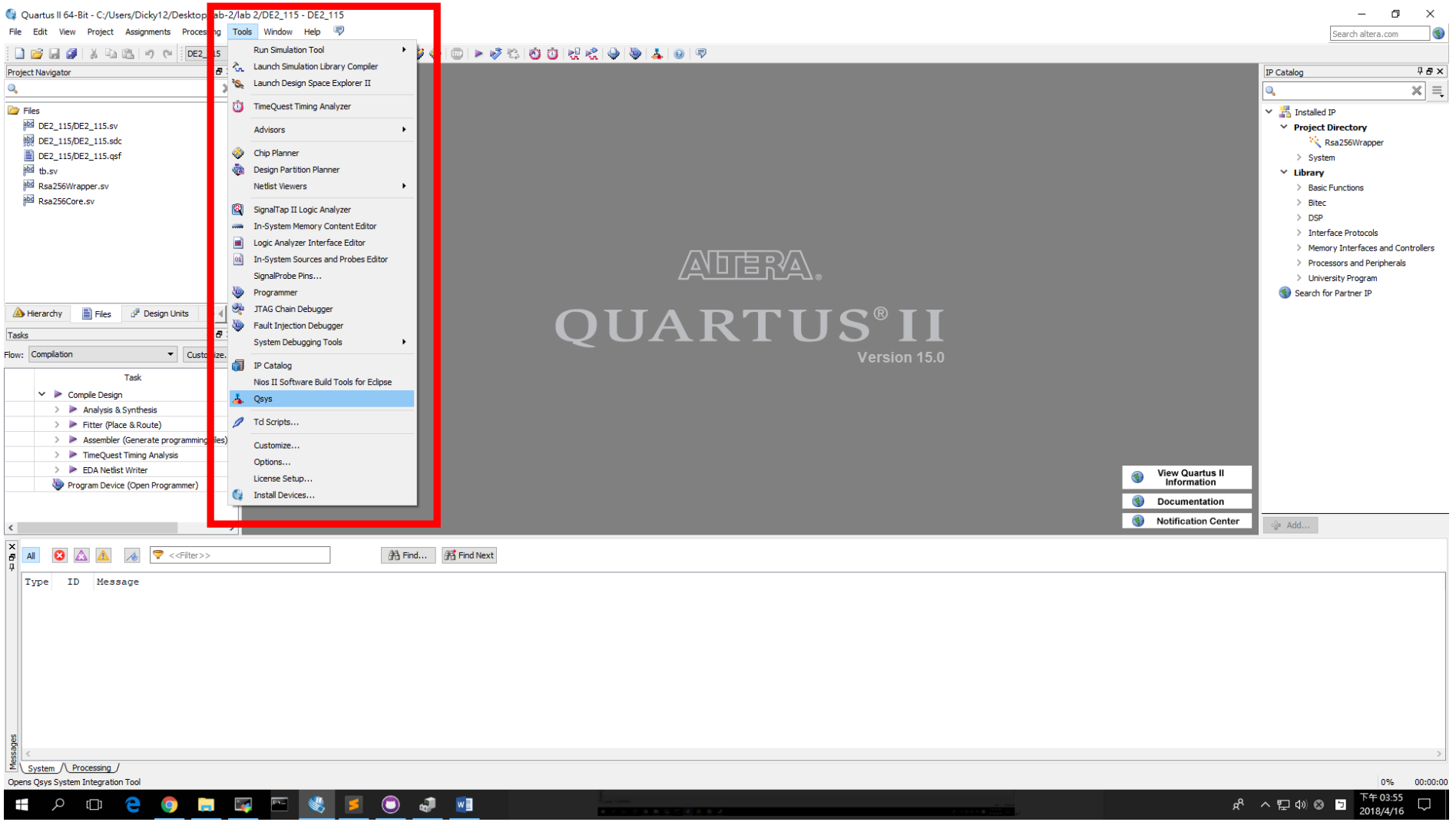
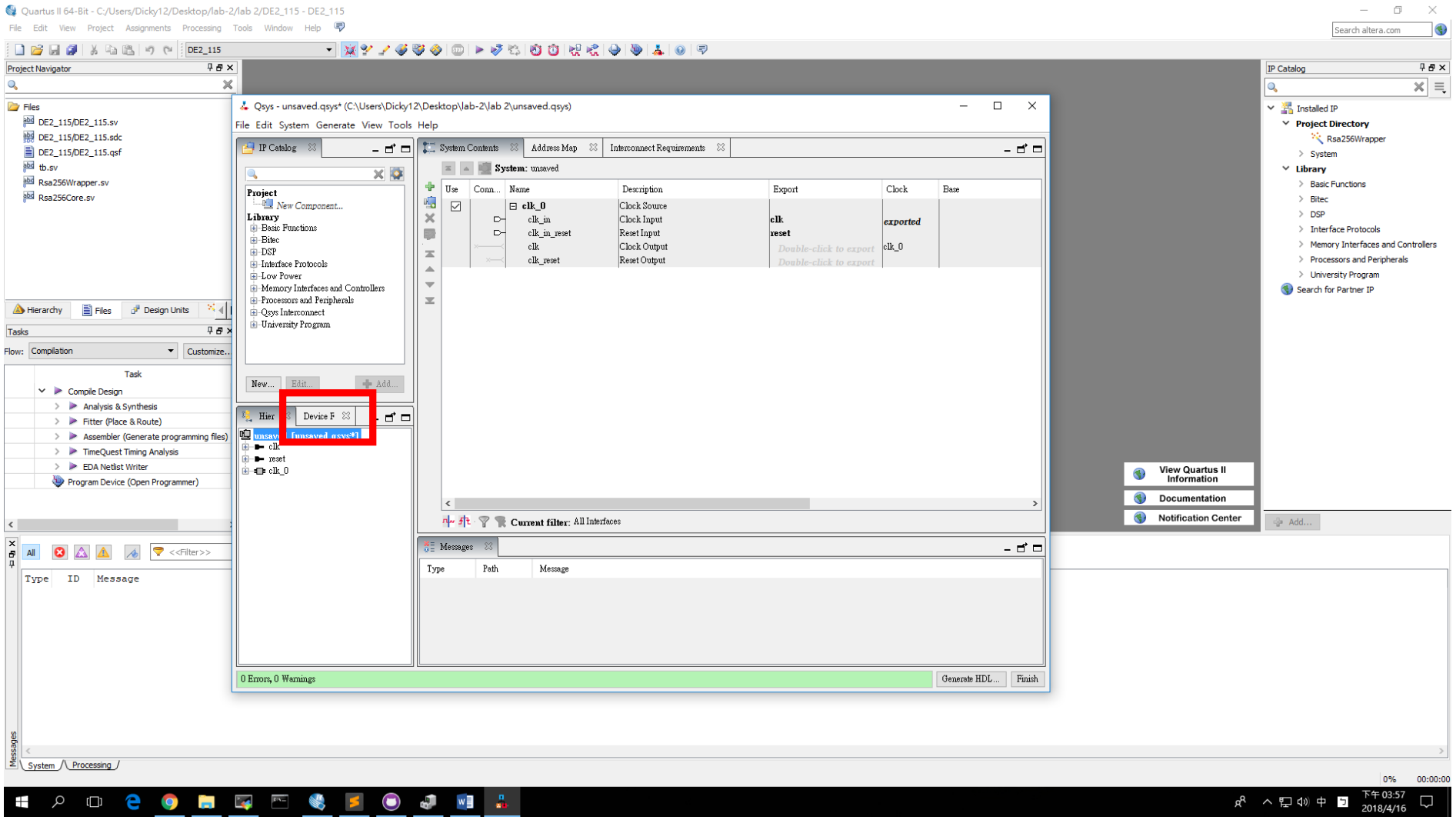
整理：鍾杰、楊仲萱

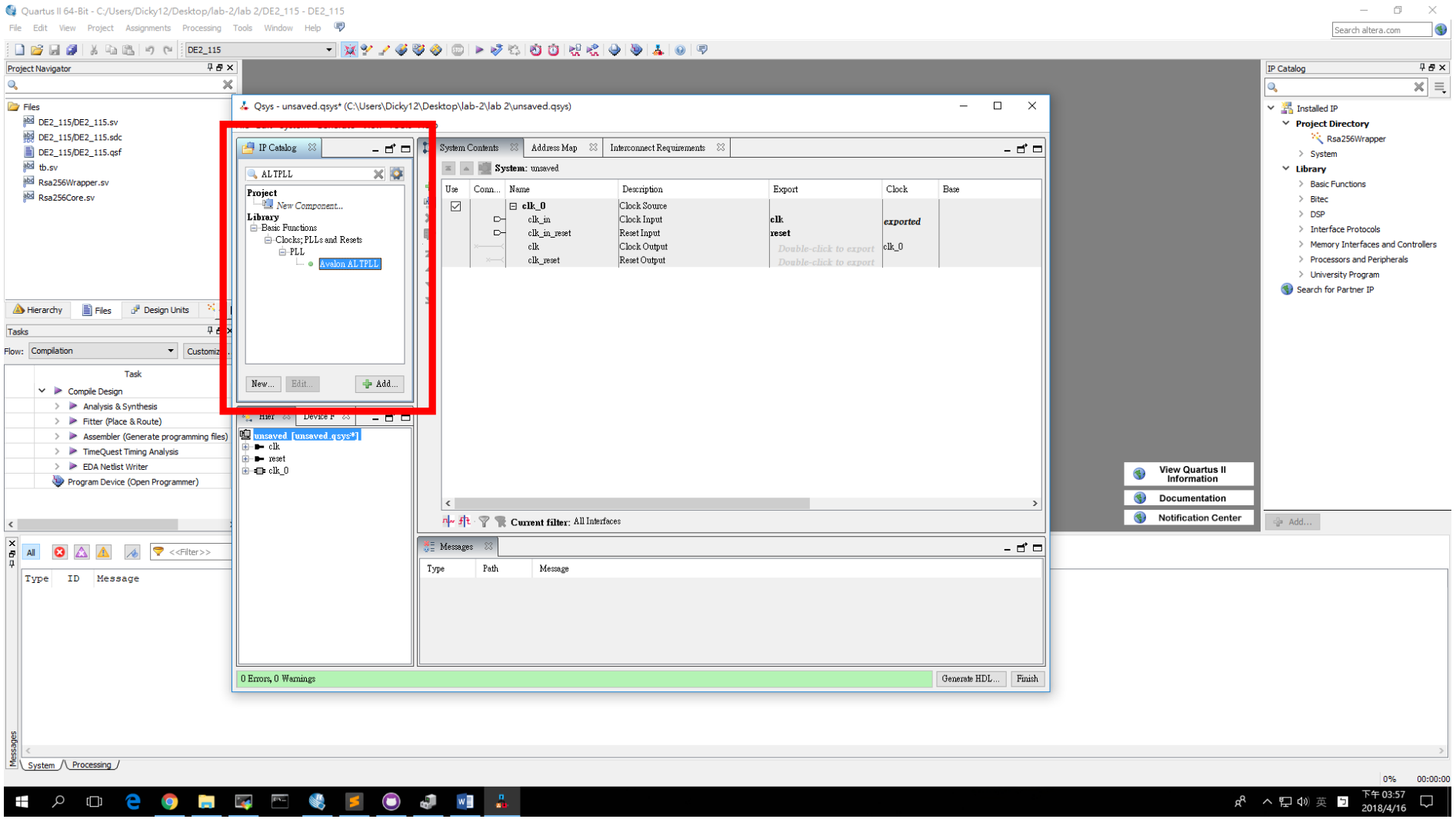
打開Qsys (Tool → Qsys)



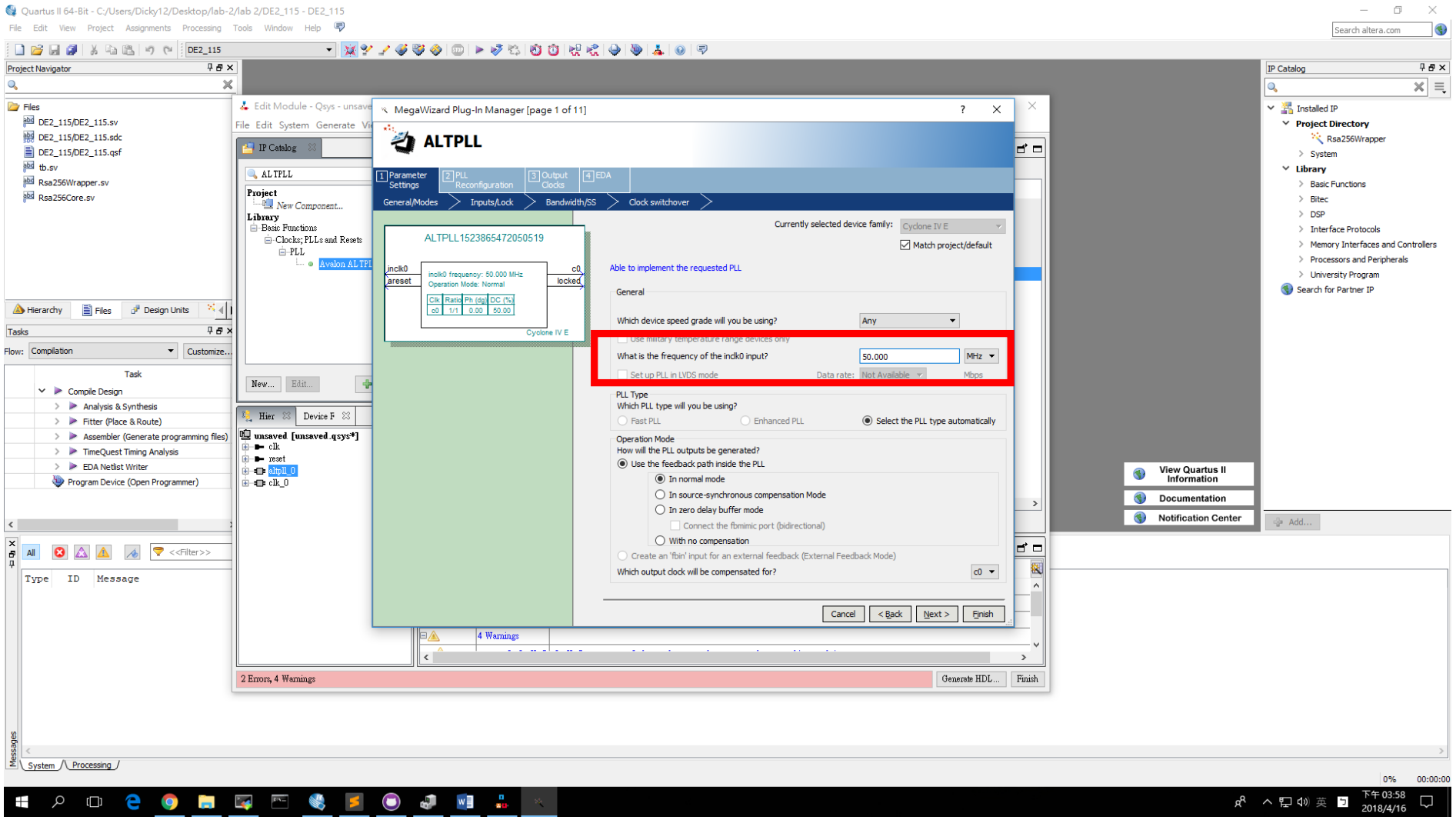
到Device Family選擇Cyclone IV



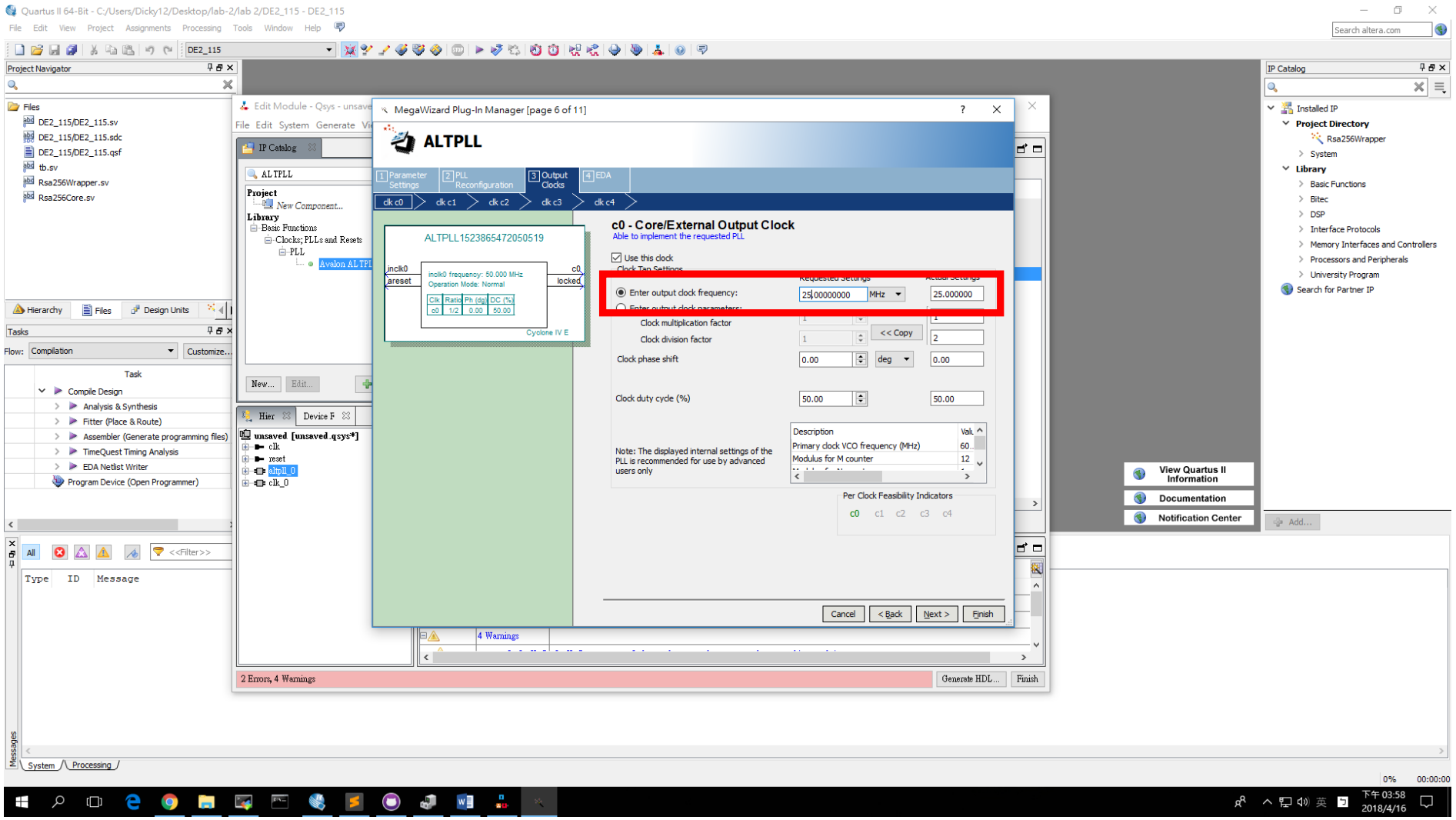
搜尋Avalon ALTPLL，雙擊新增



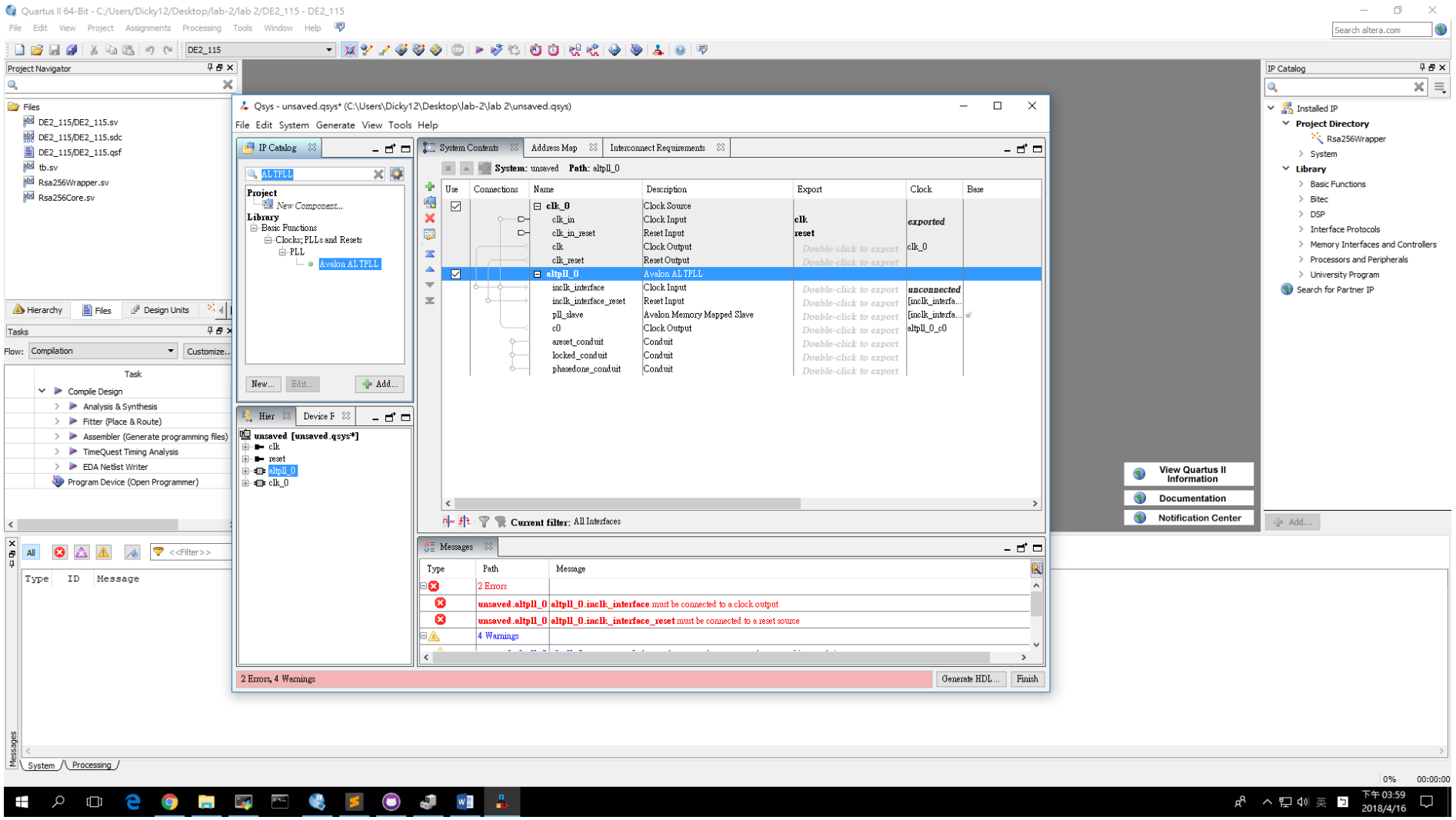
Frequency of inclk0 input = 50MHz



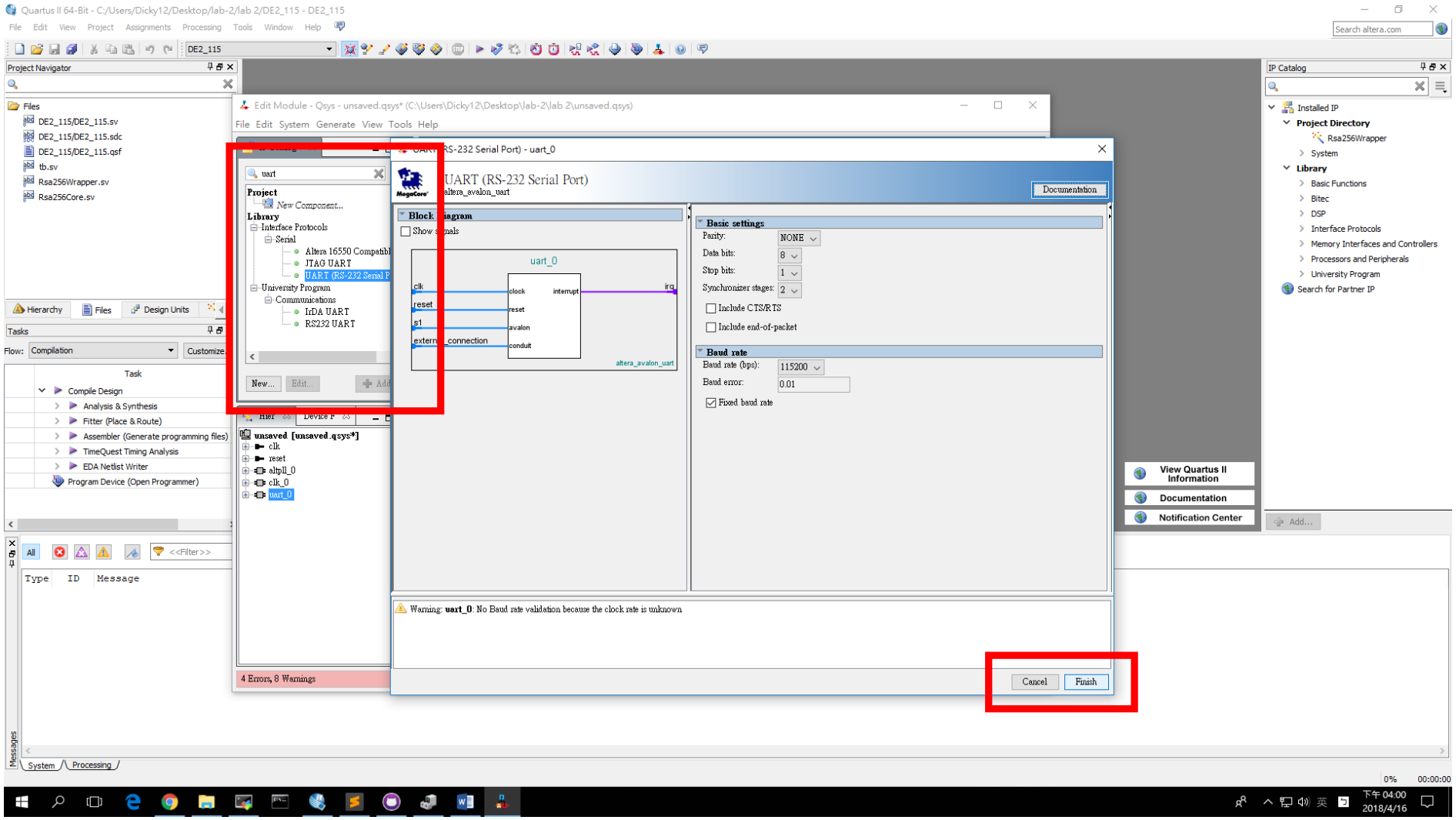
Output clock frequency = 25MHz



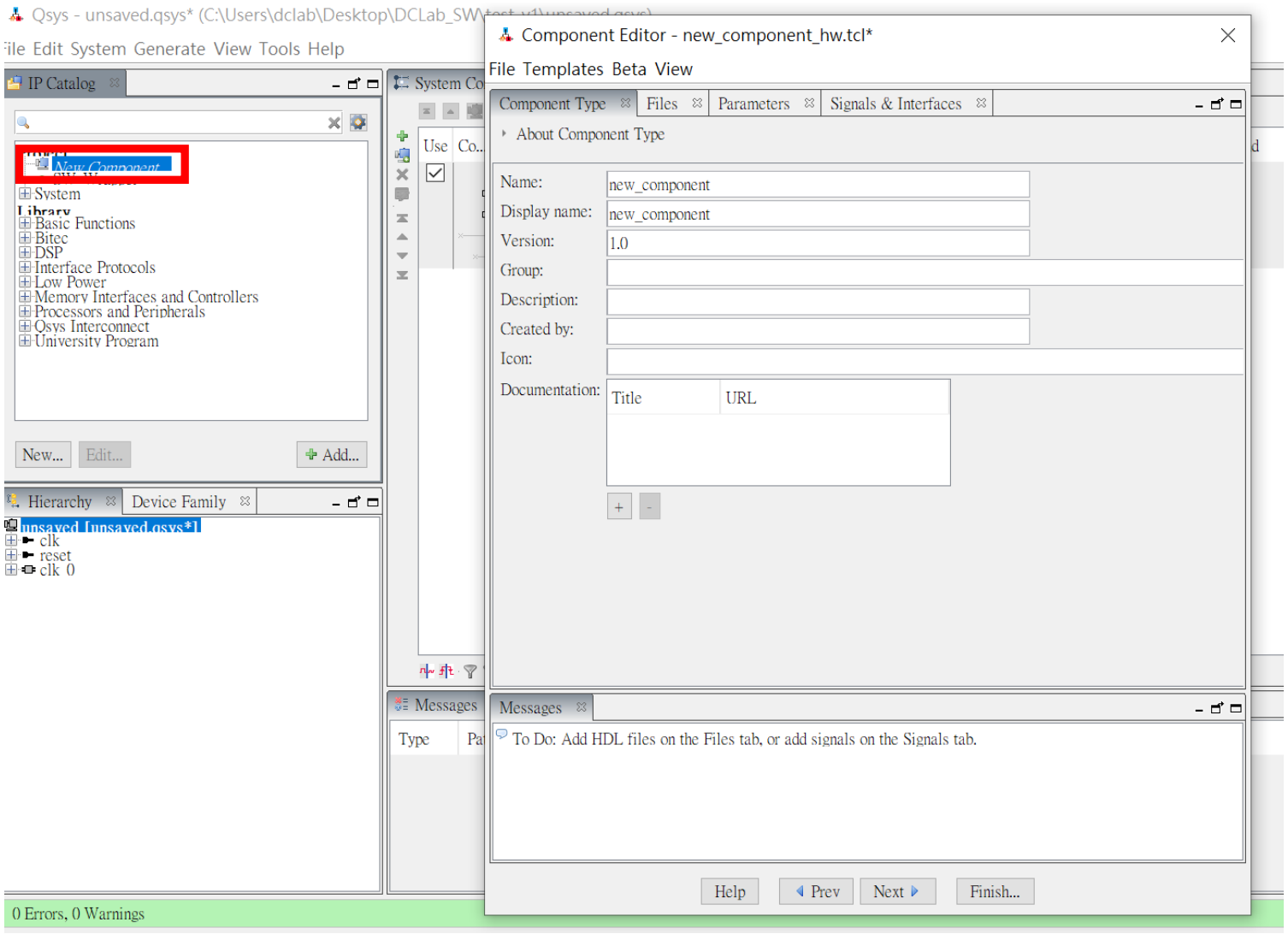
按 Finish 可在右側看到新增的 ALTPLL



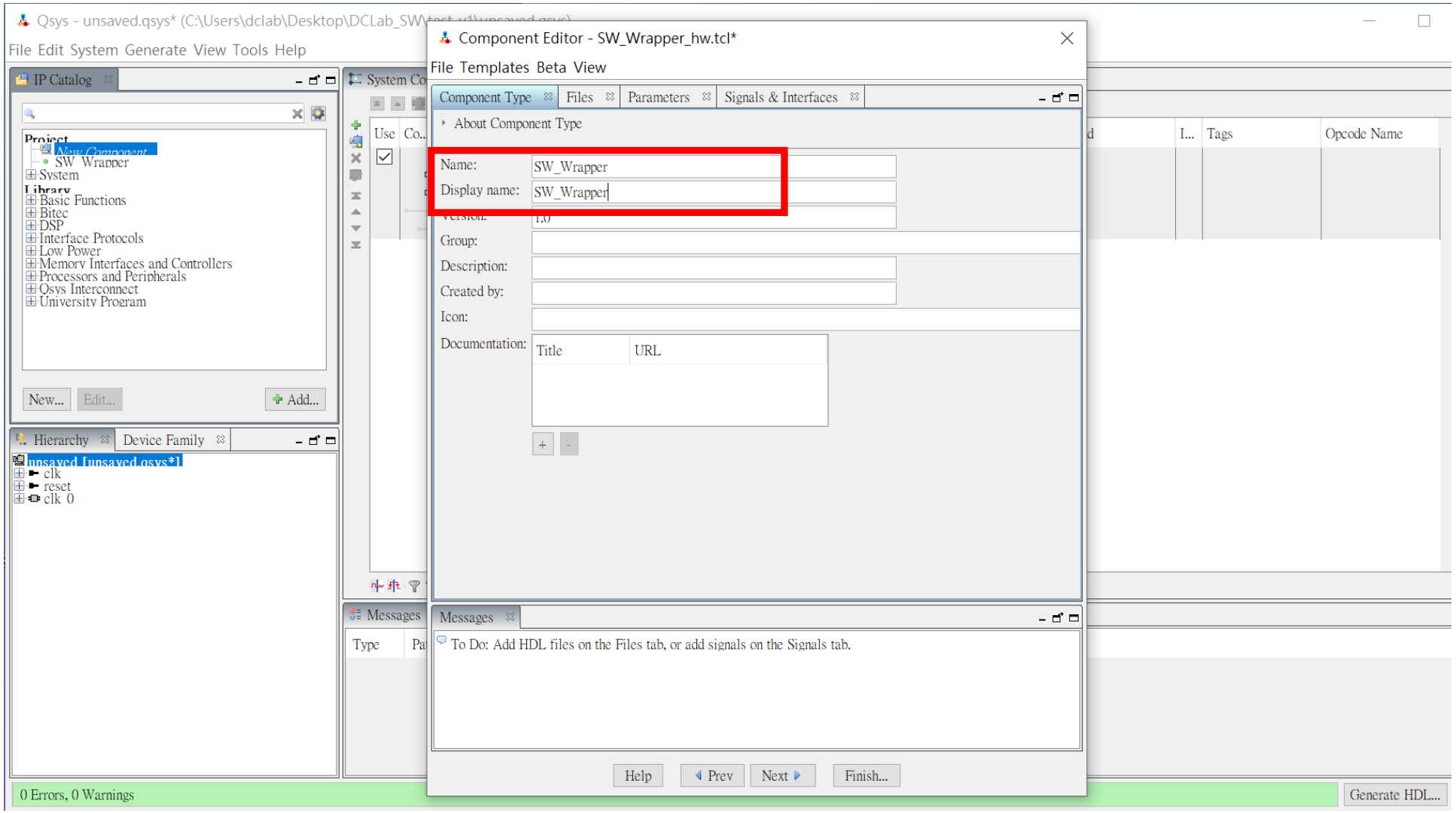
搜尋 UART → UART (RS-232 Serial Port) → Finish



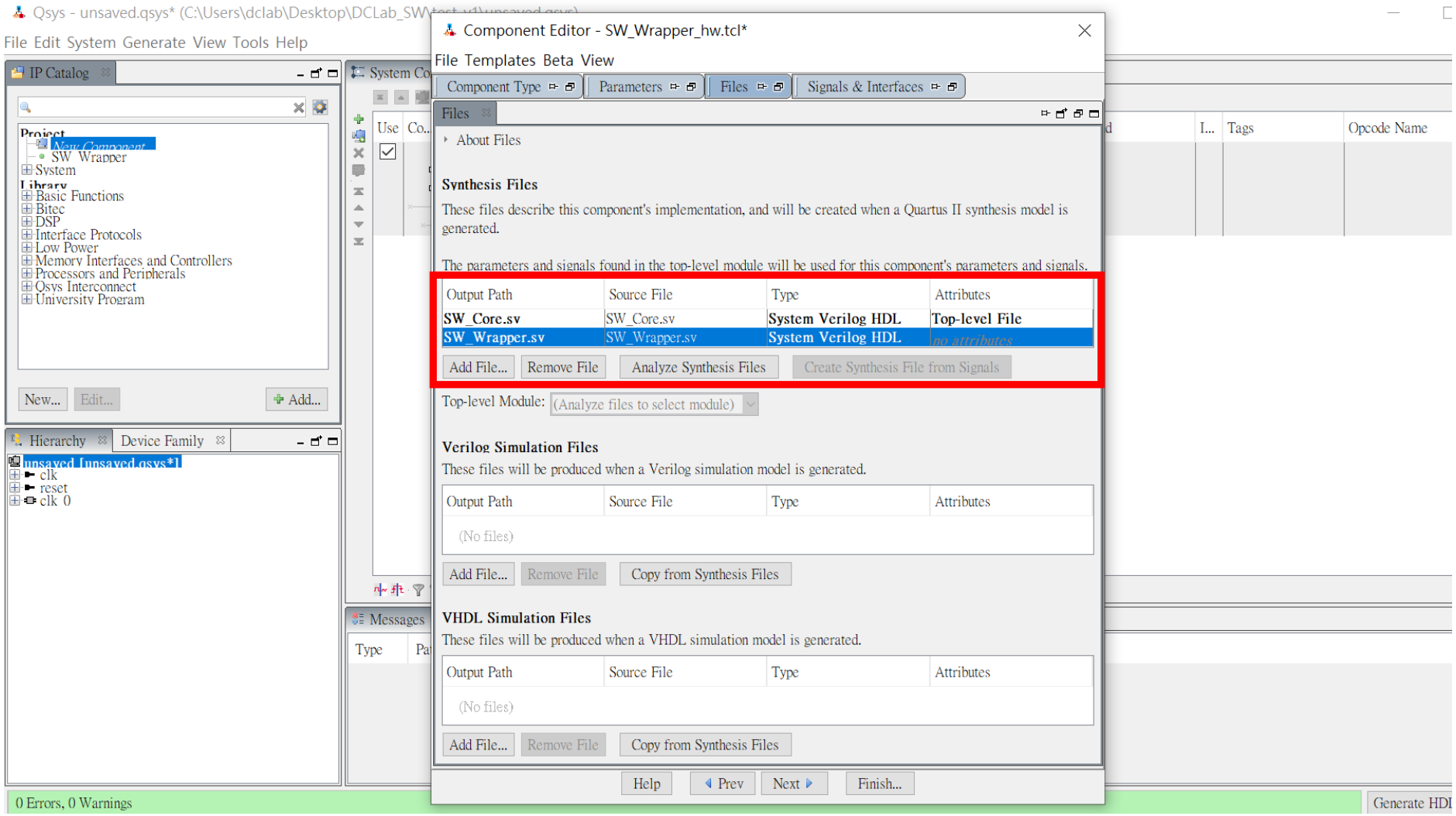
雙擊 New Component



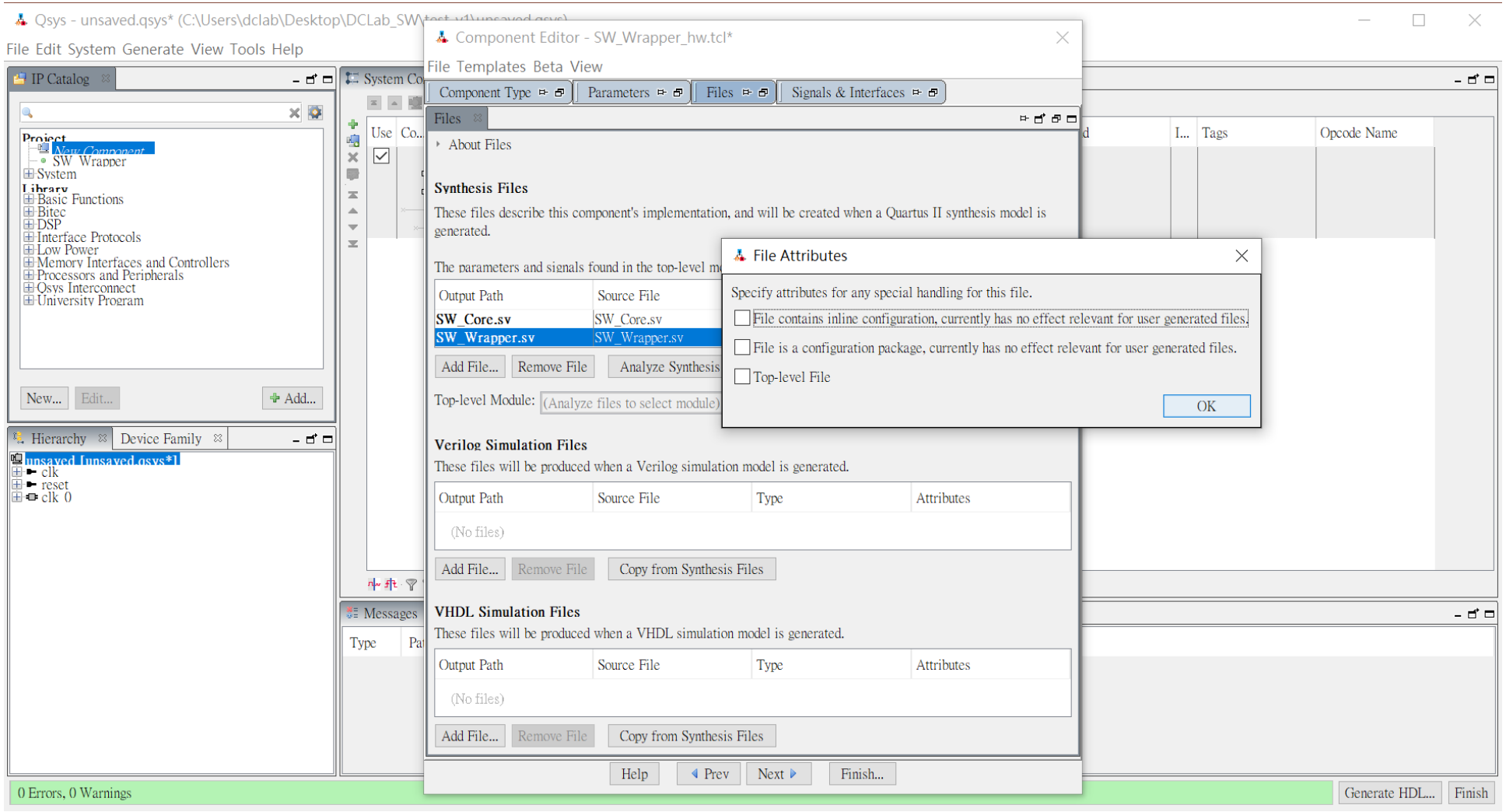
Name = SW_Wrapper
Display Name = SW_Wrapper



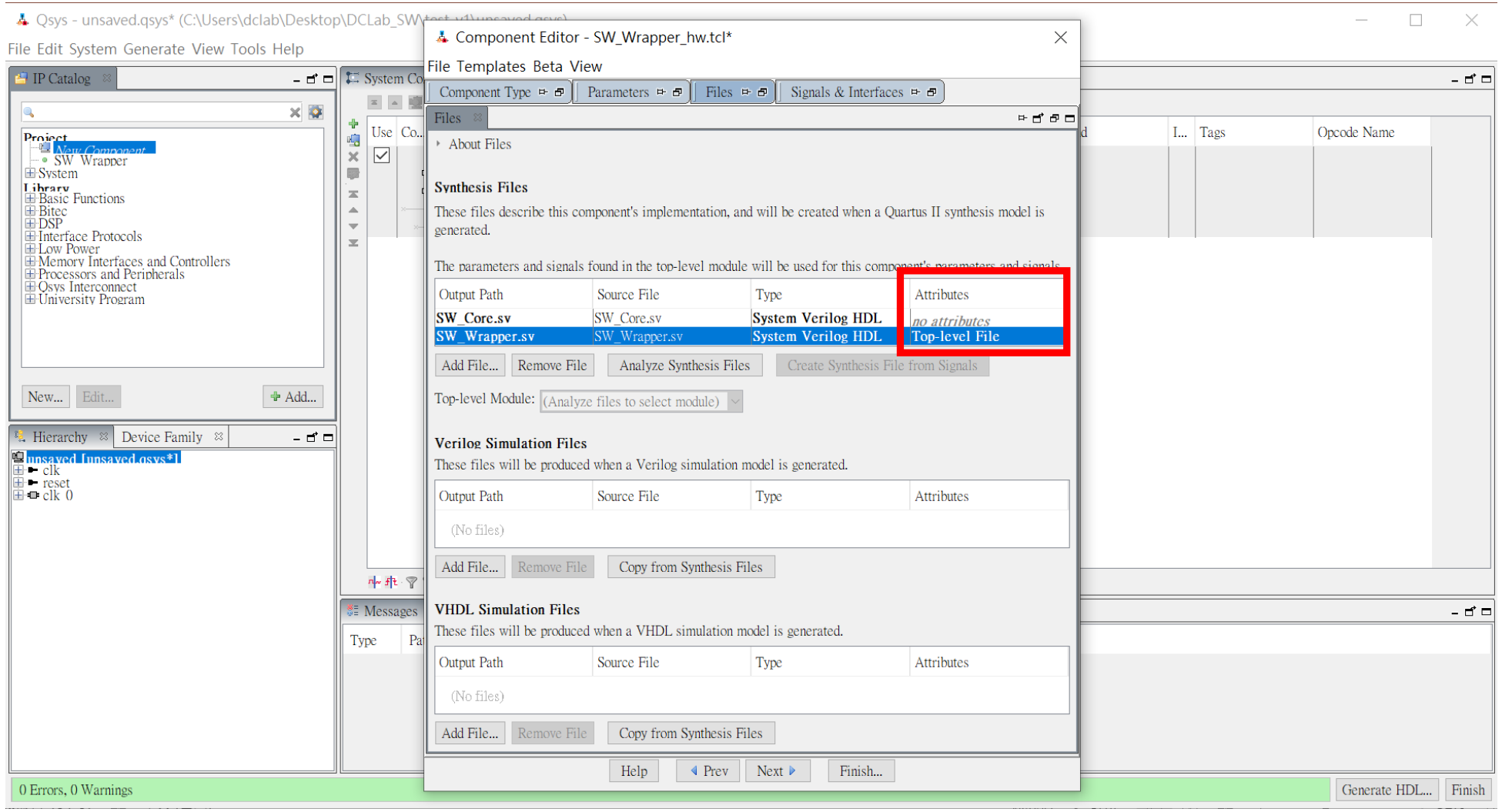
File → Add File
新增 SW_Core.sv 和 SW_Wrapper.sv



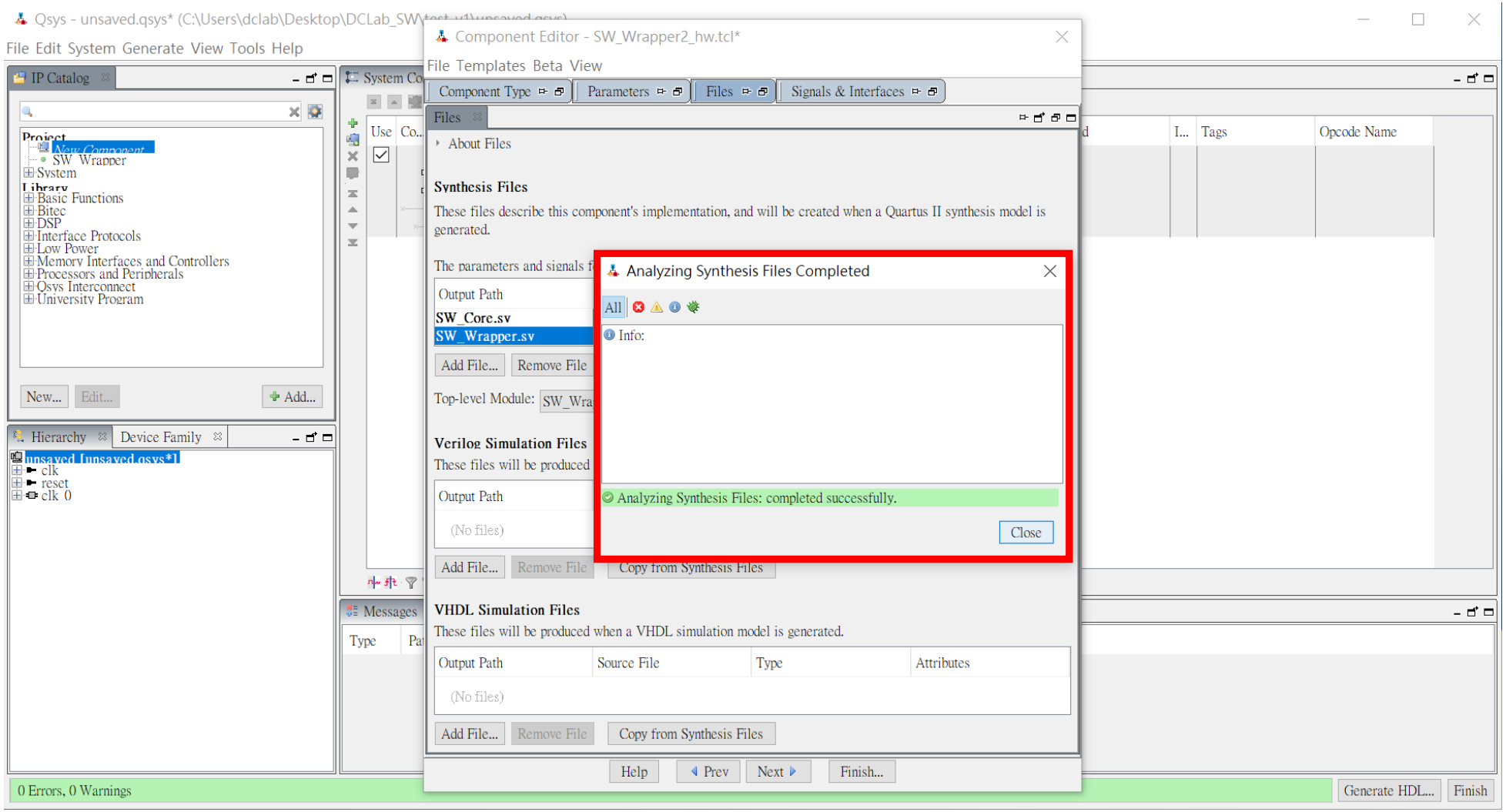
將 SW_Wrapper 改成 Top level file (1/2)



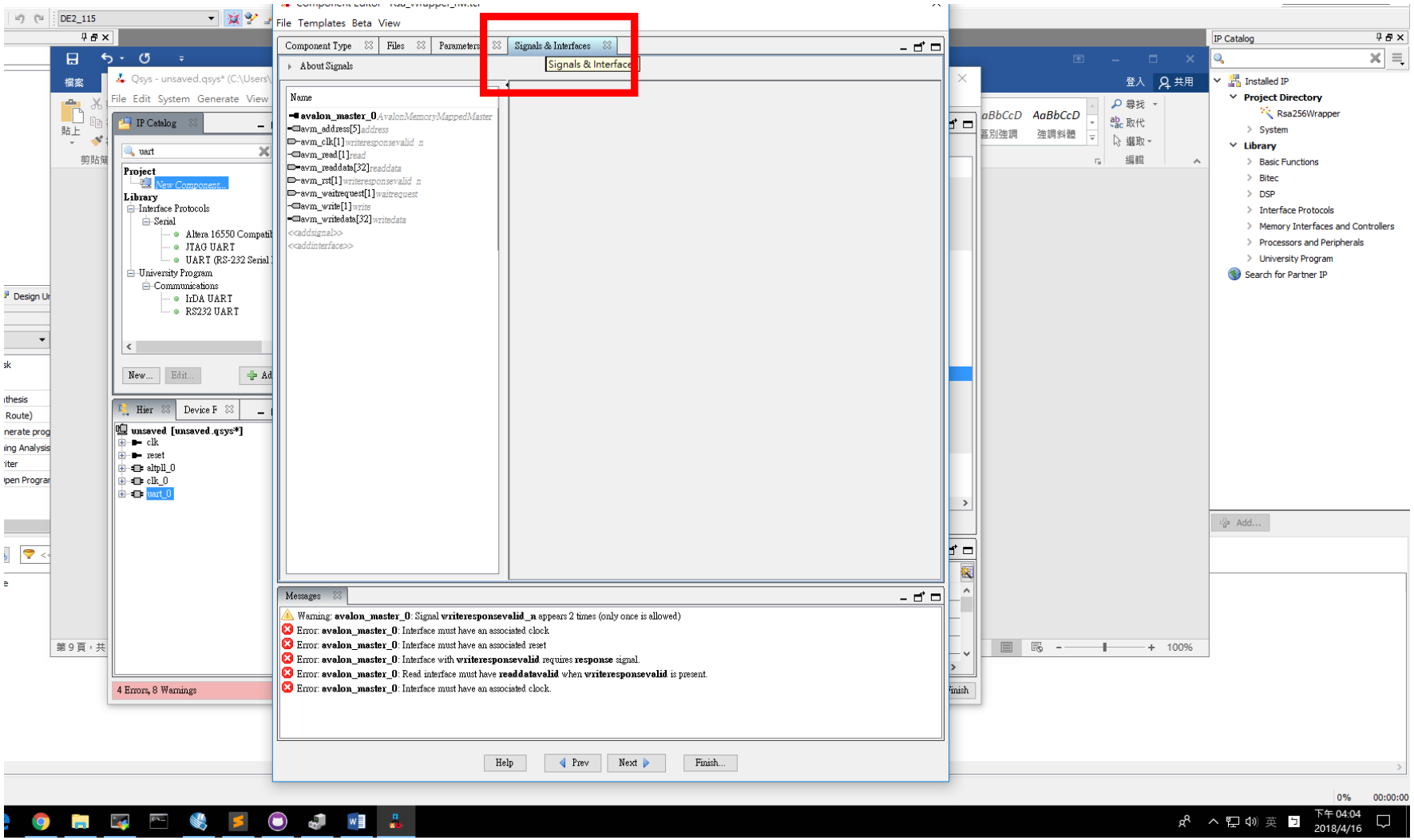
將 SW_Wrapper 改成 Top level file (2/2)



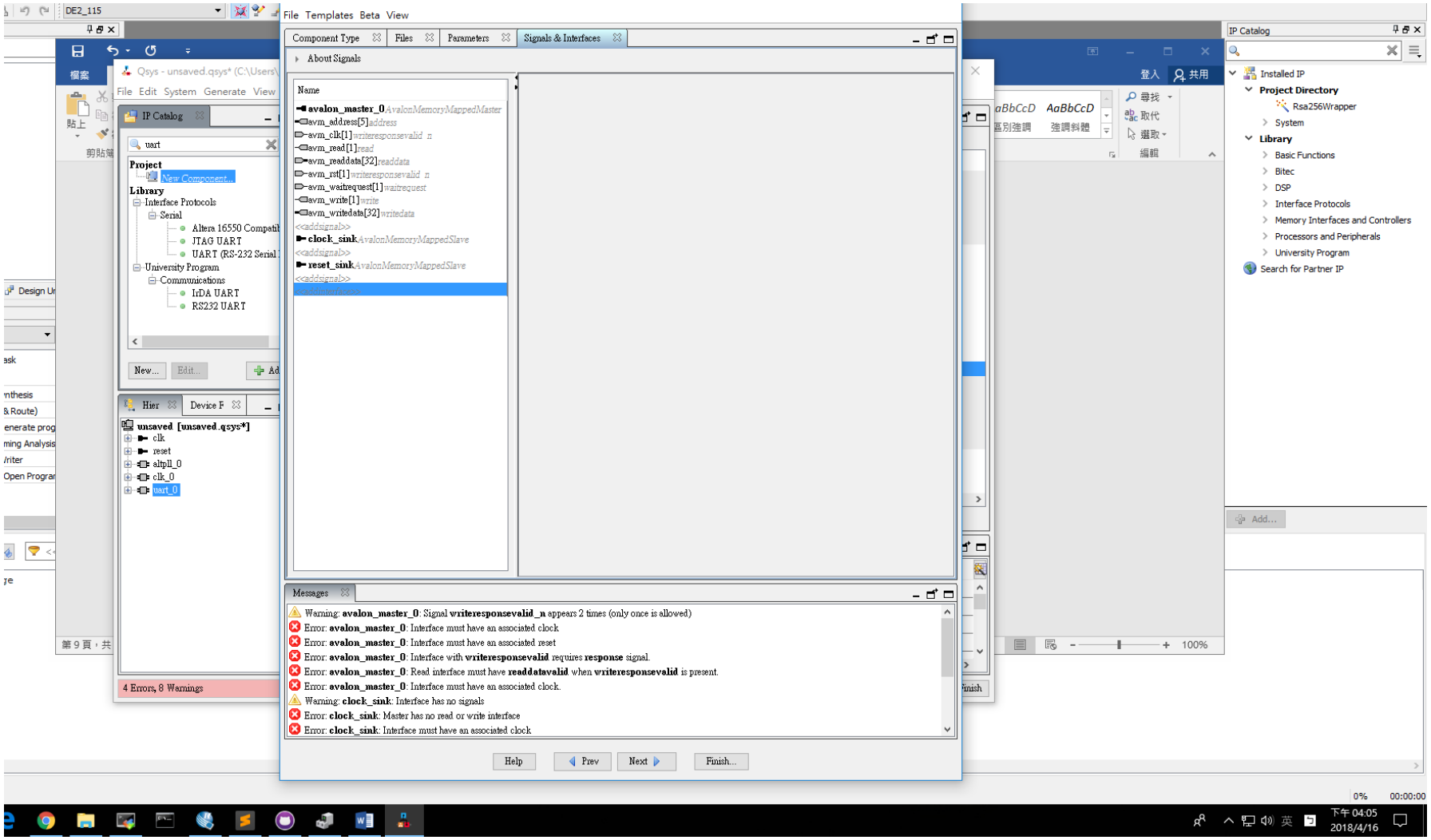
Analyze Synthesis File → Close



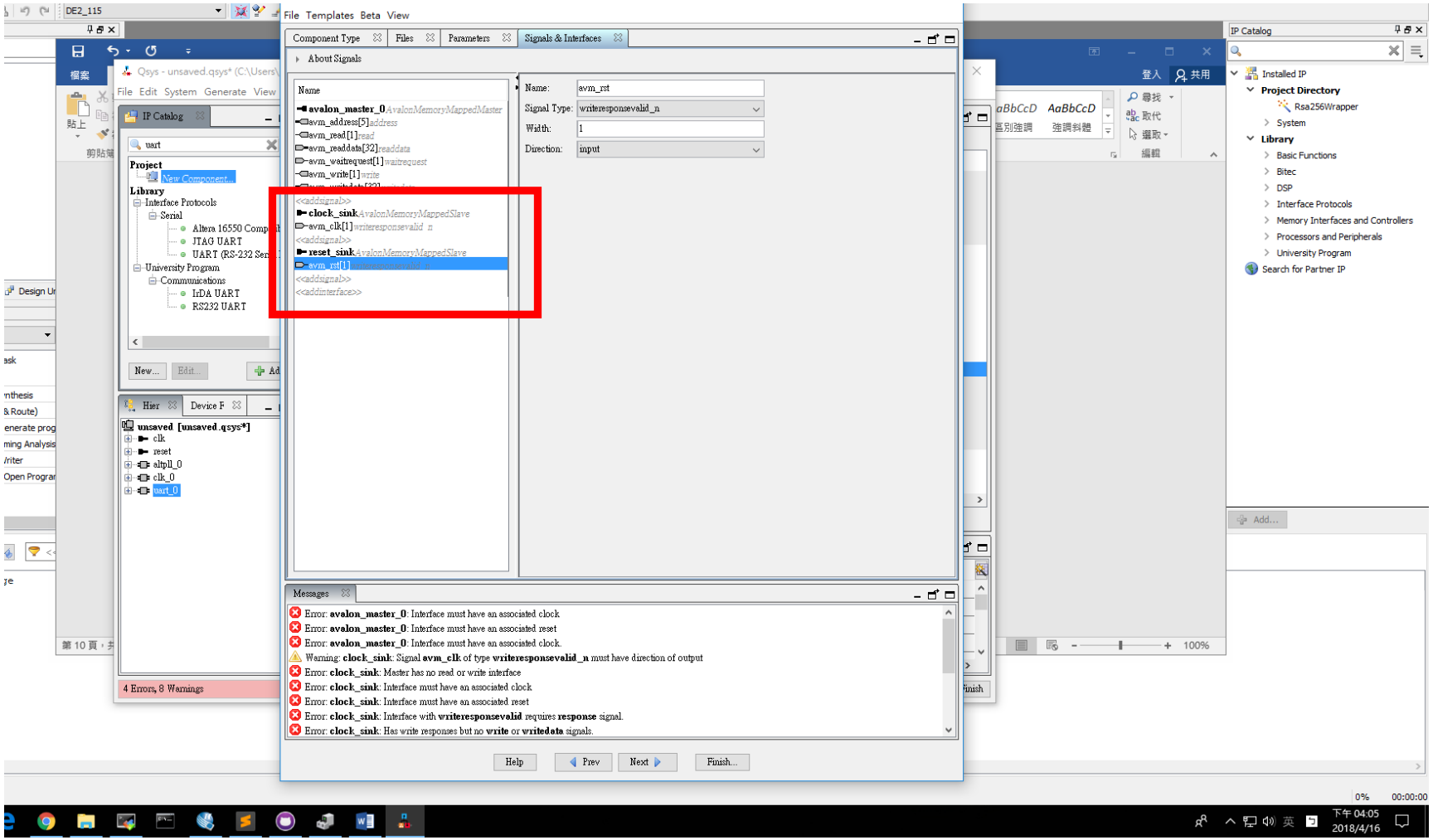
選 Signal Interface



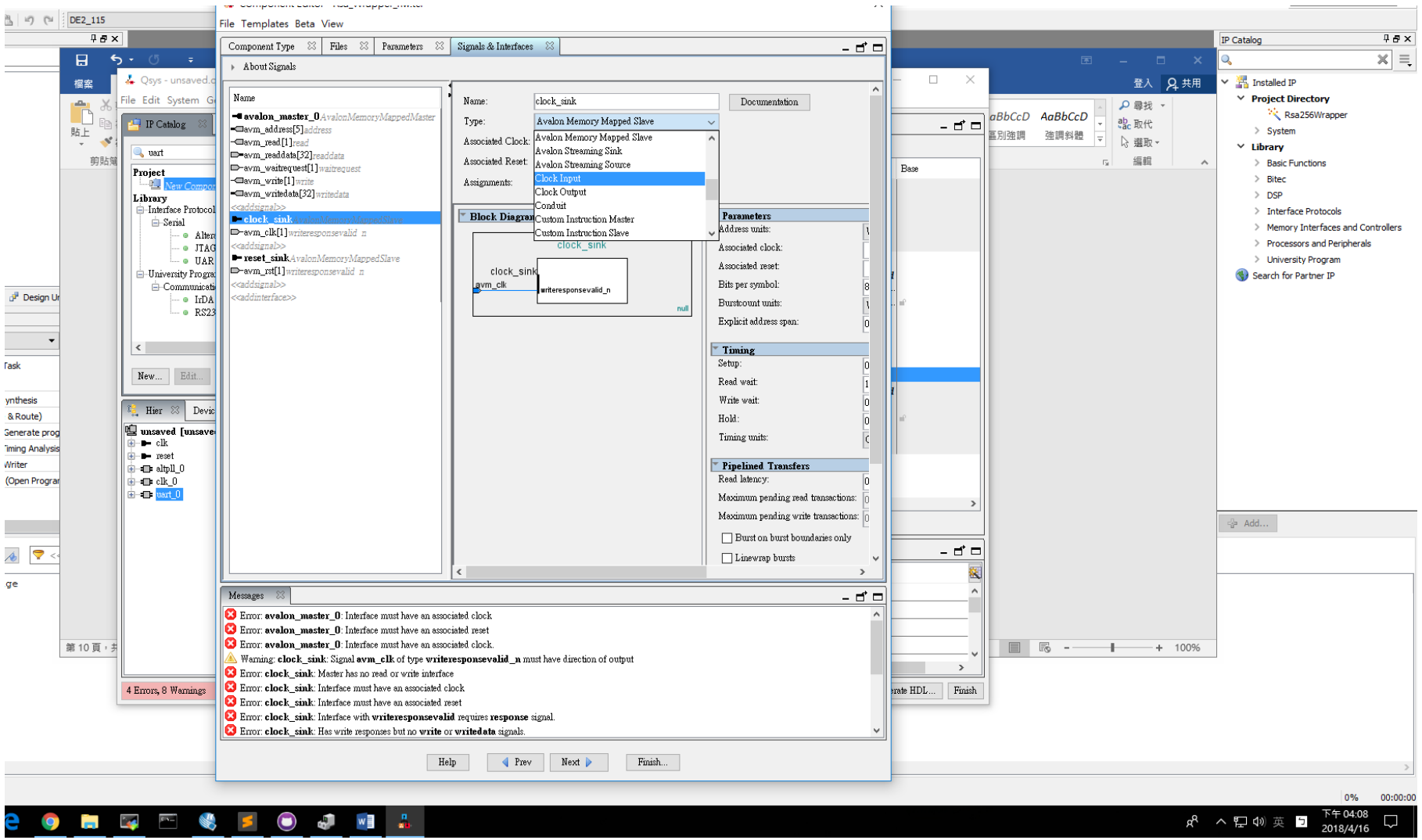
雙擊 Add interface → clock_sink
雙擊 Add interface → reset_sink



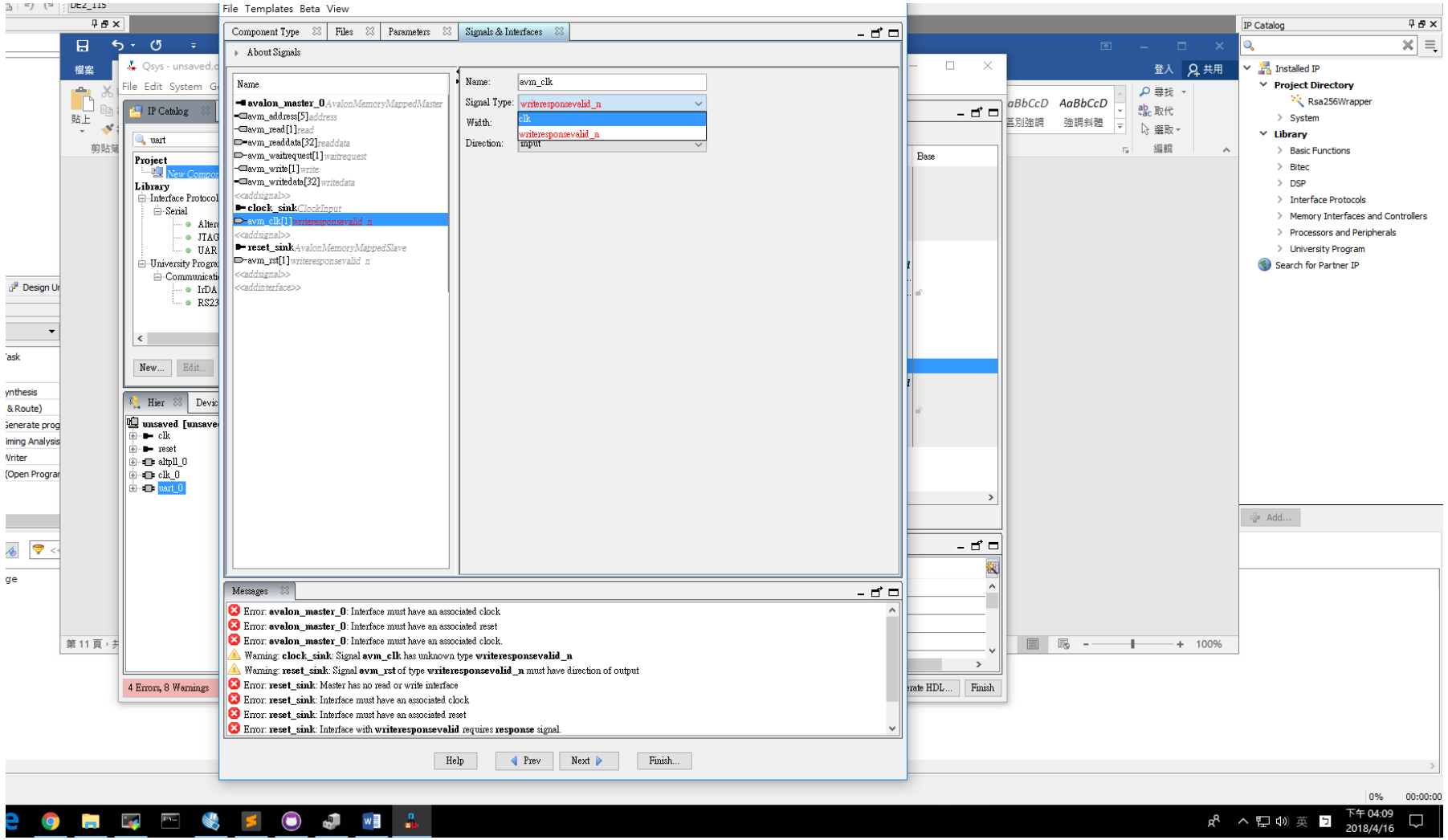
avm_clk 拖曳至 clock_sink下方
avm_rst 拖曳至 reset_sink下方



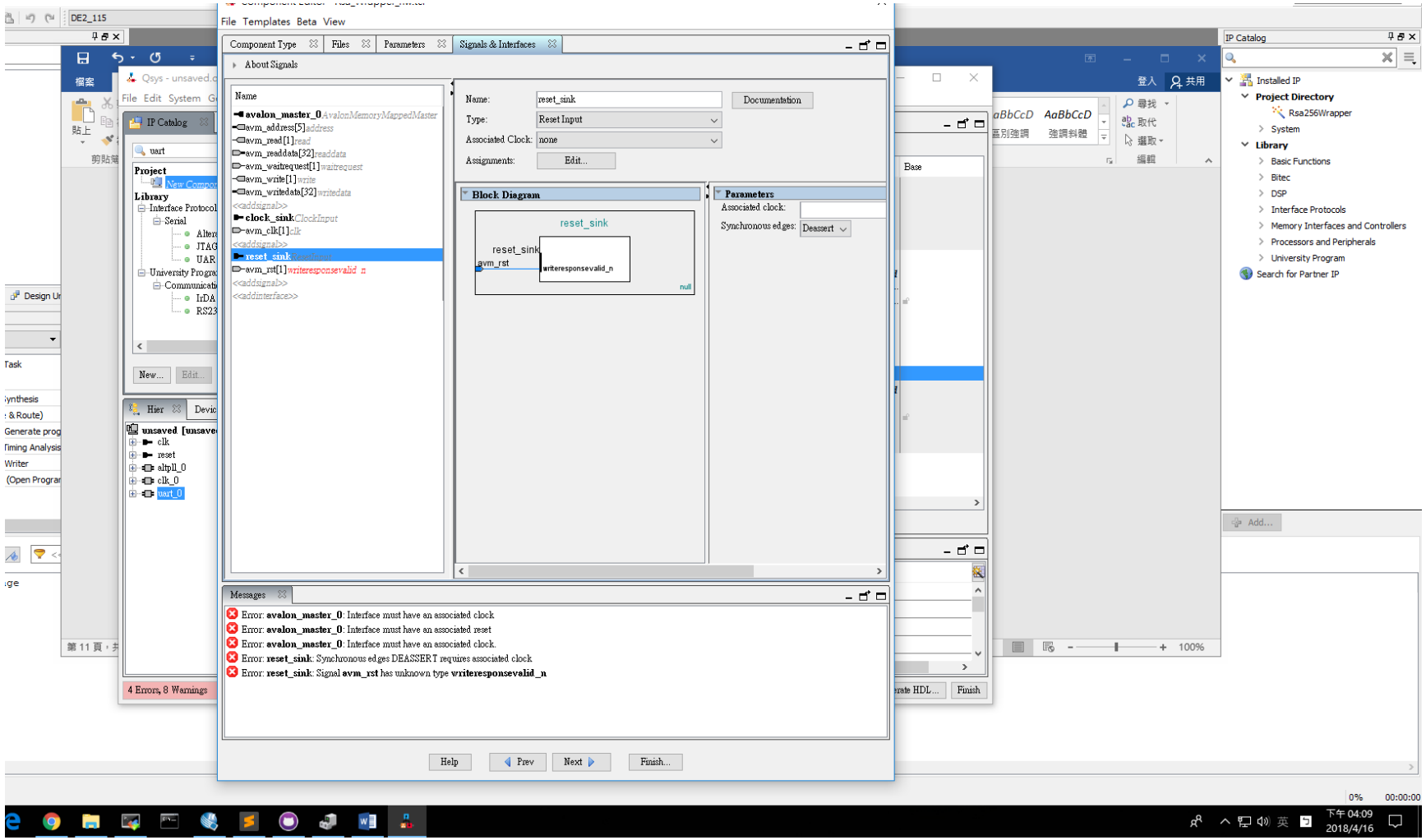
將 clock_sink 的 Type 改成 Clock Input



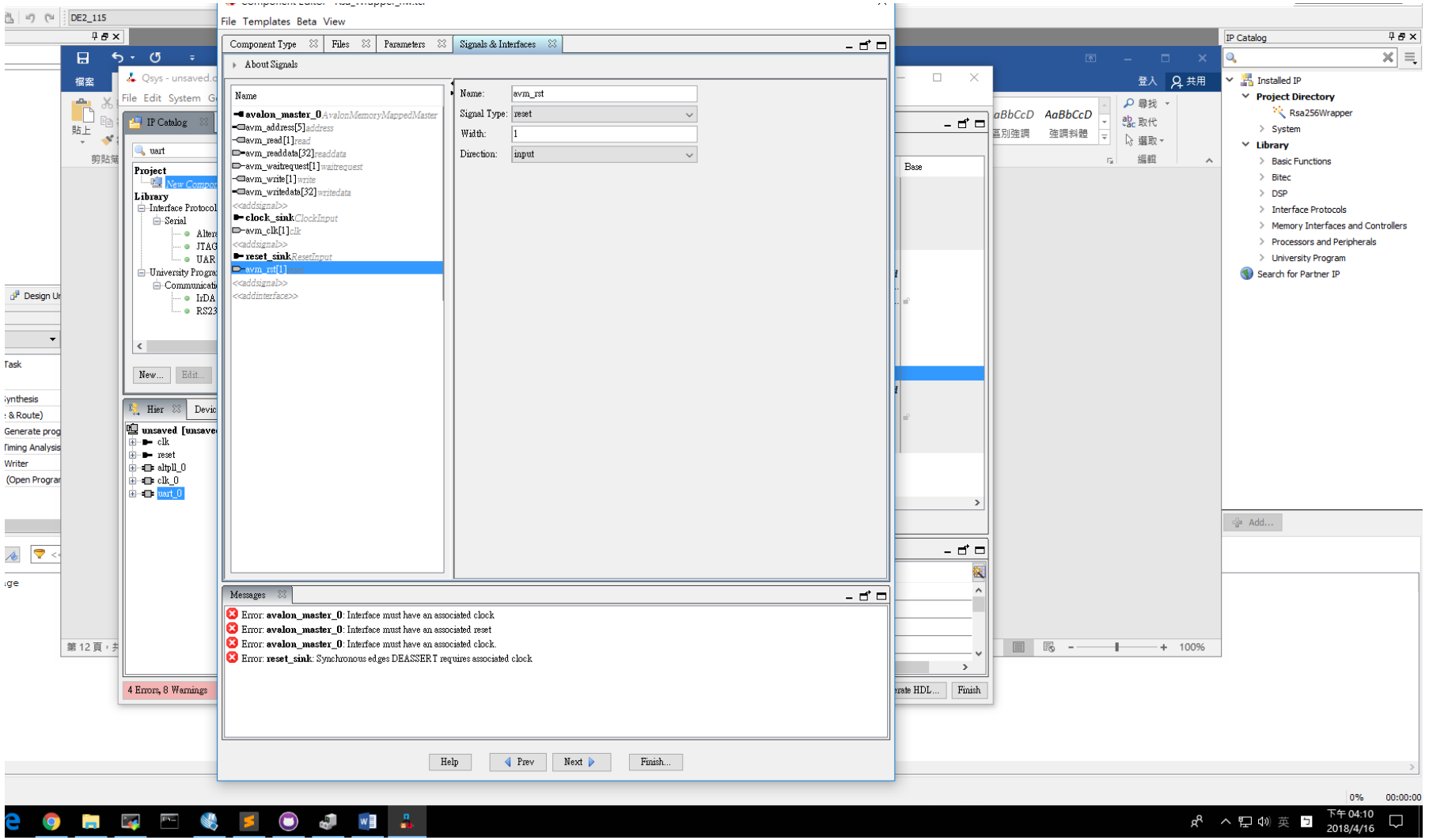
將 avm_clk 的 Signal Type 改成 clk



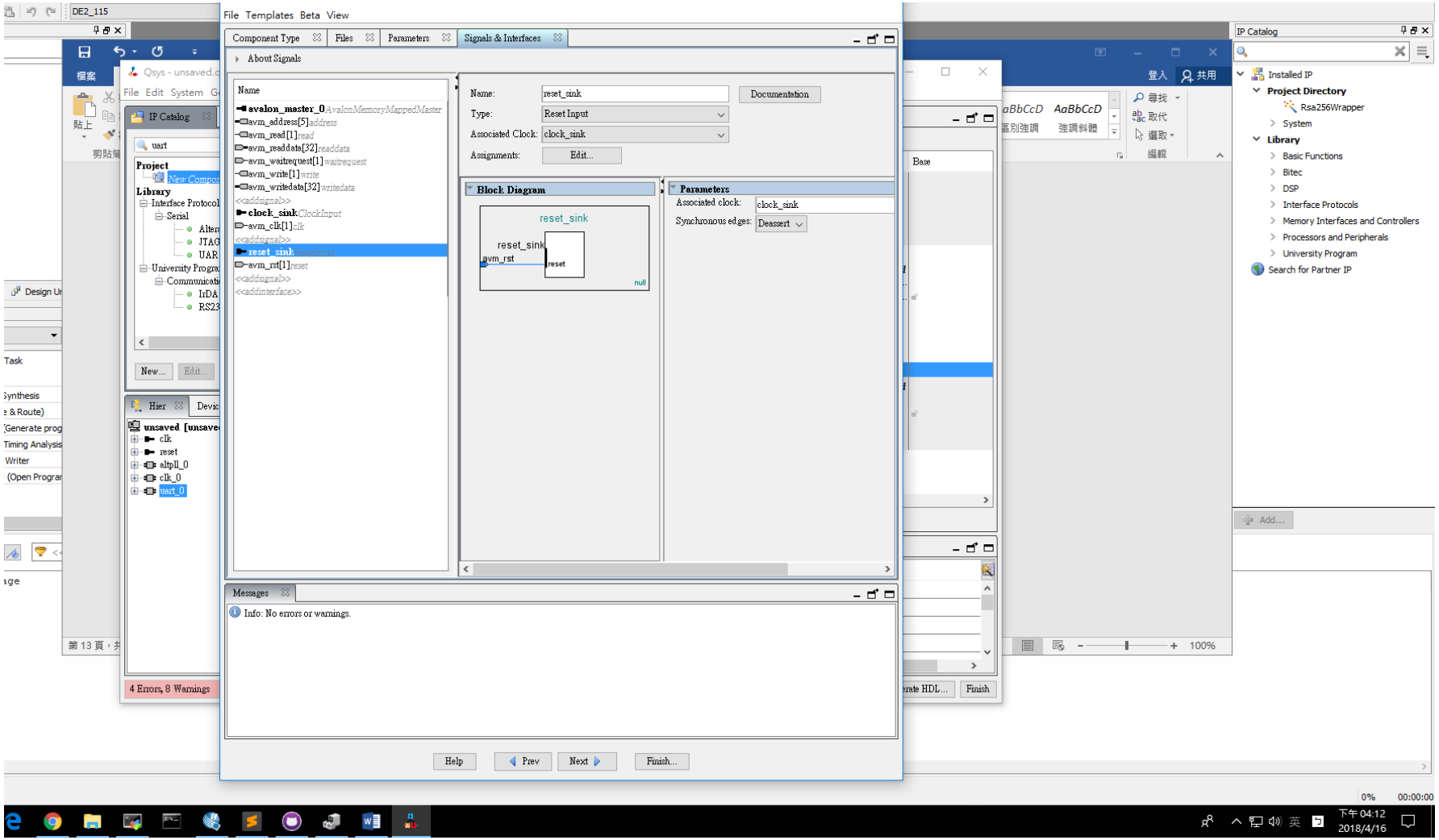
將 reset_sink 的 Type 改成 Reset Input



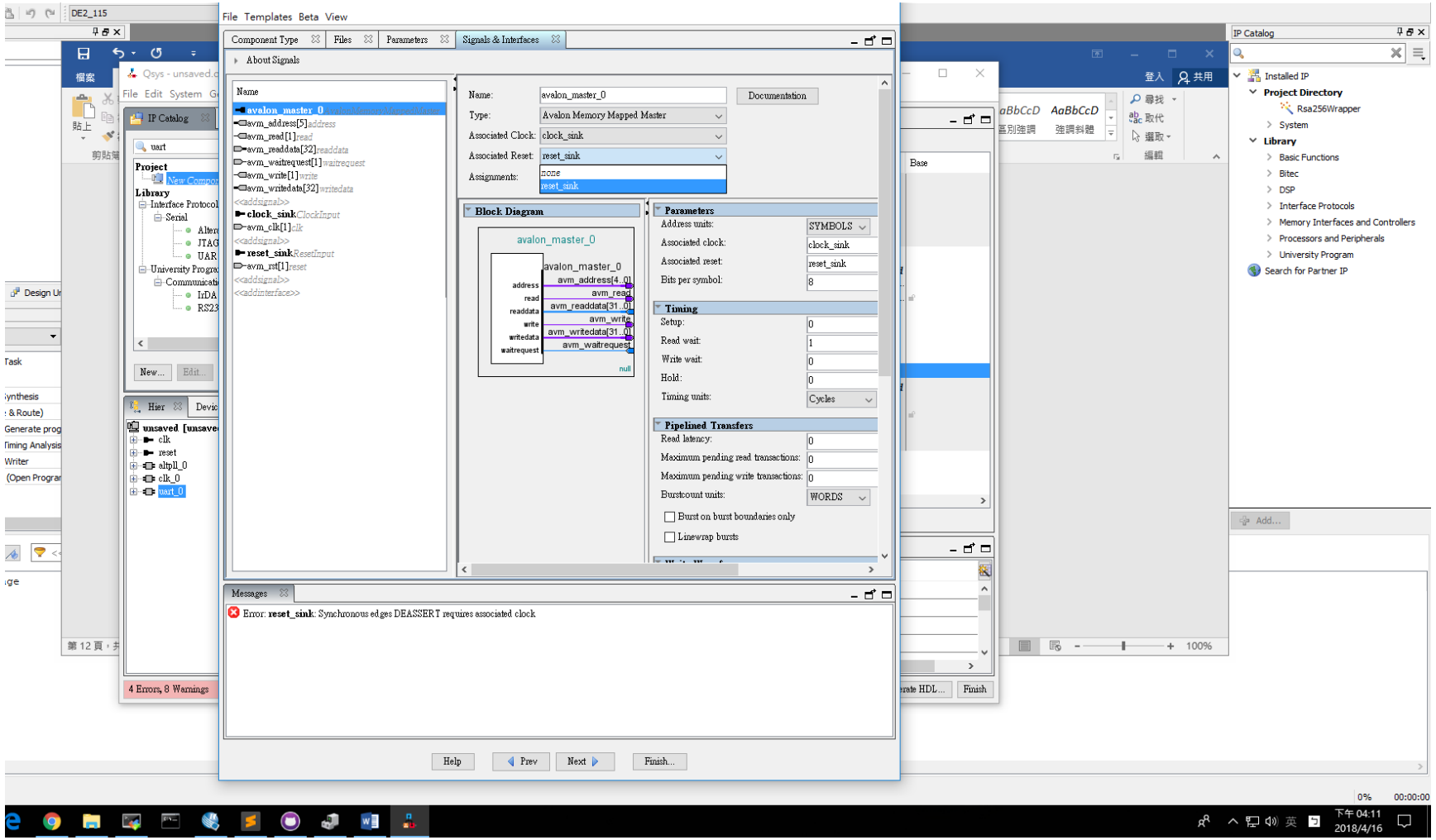
將 avm_rst 的 Signal Type 改成 reset



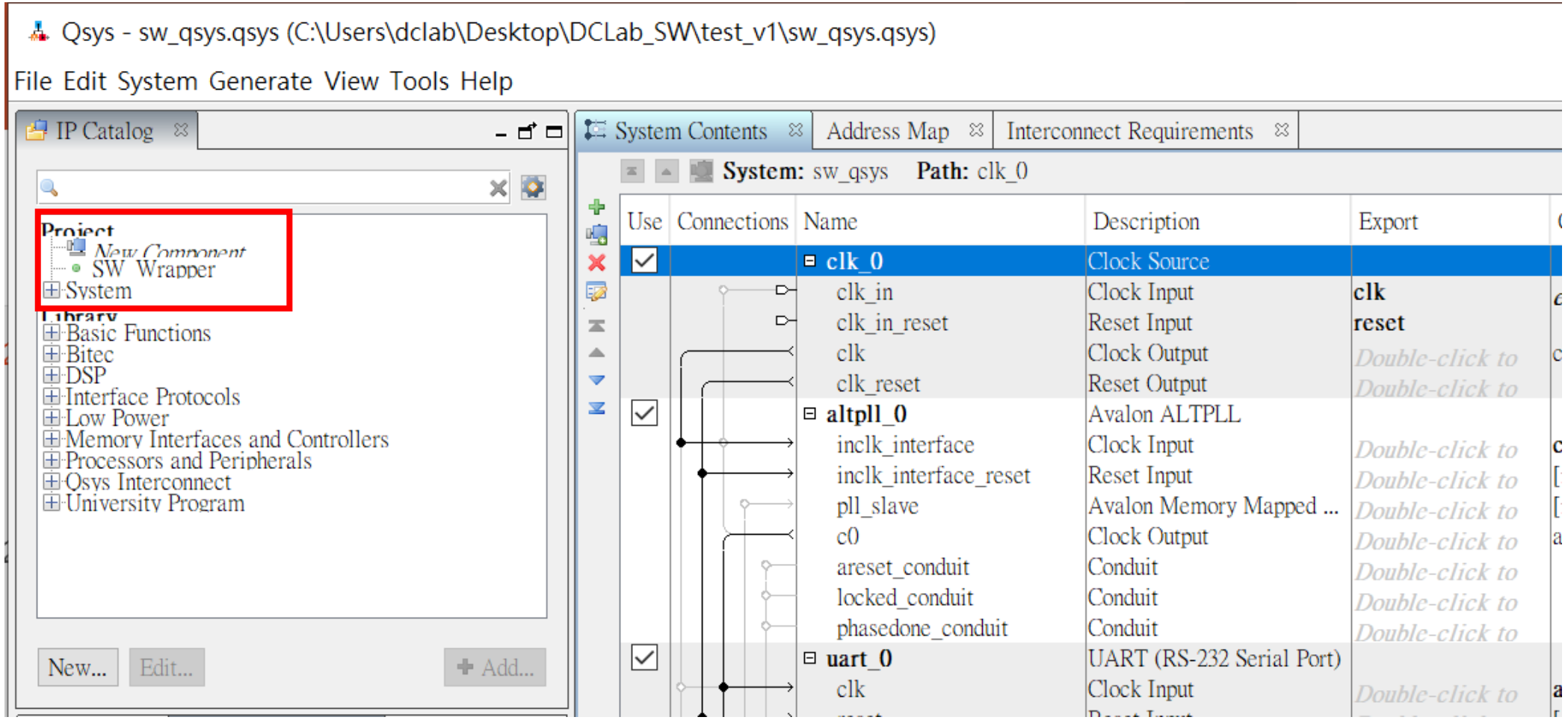
將 reset_sink 的 associate clock 改成 clock_sink



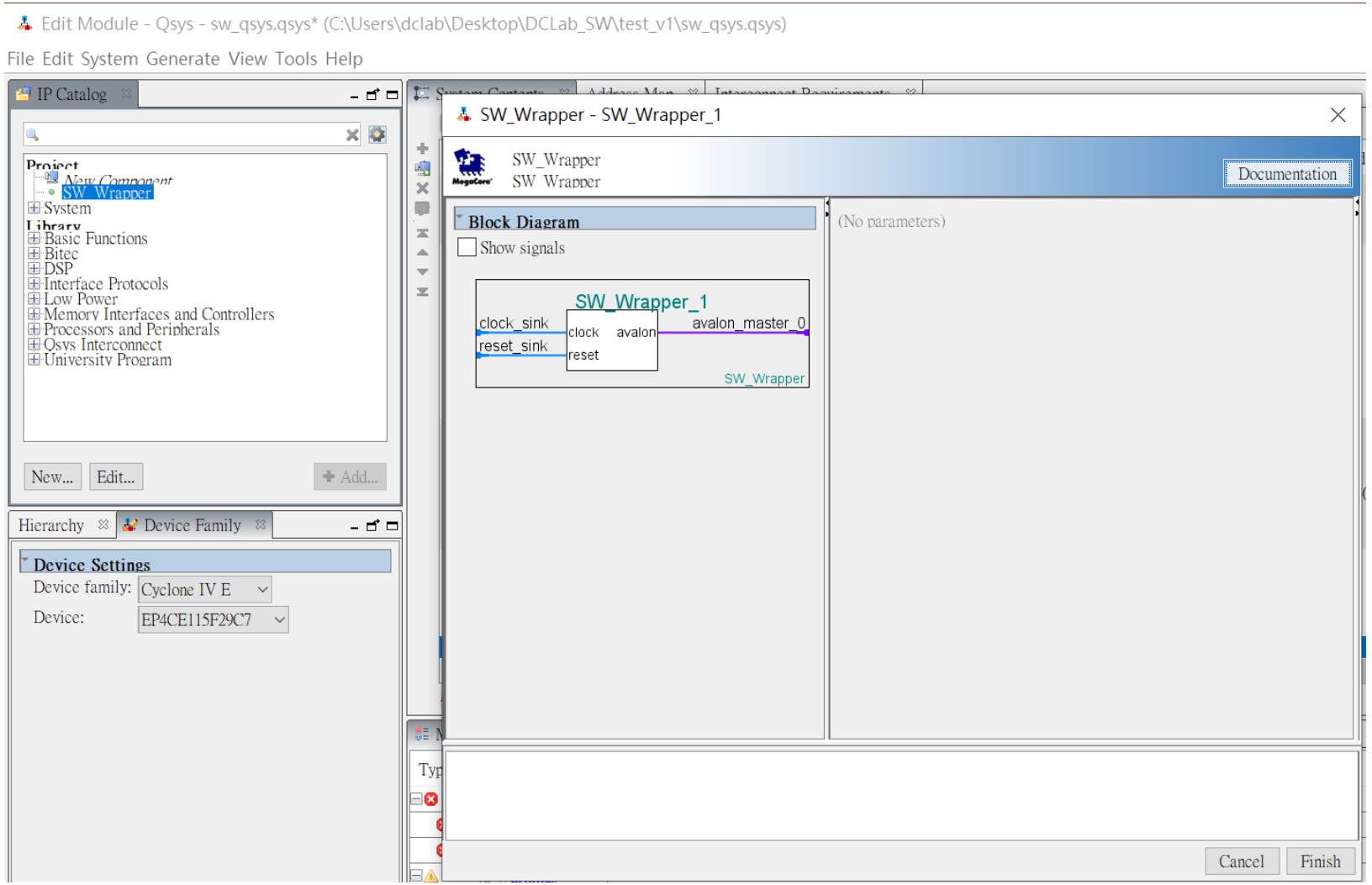
將 avalon_master_0 的 associate clock 改成 clock_sink
將 avalon_master_0 的 associate reset 改成 reset_sink



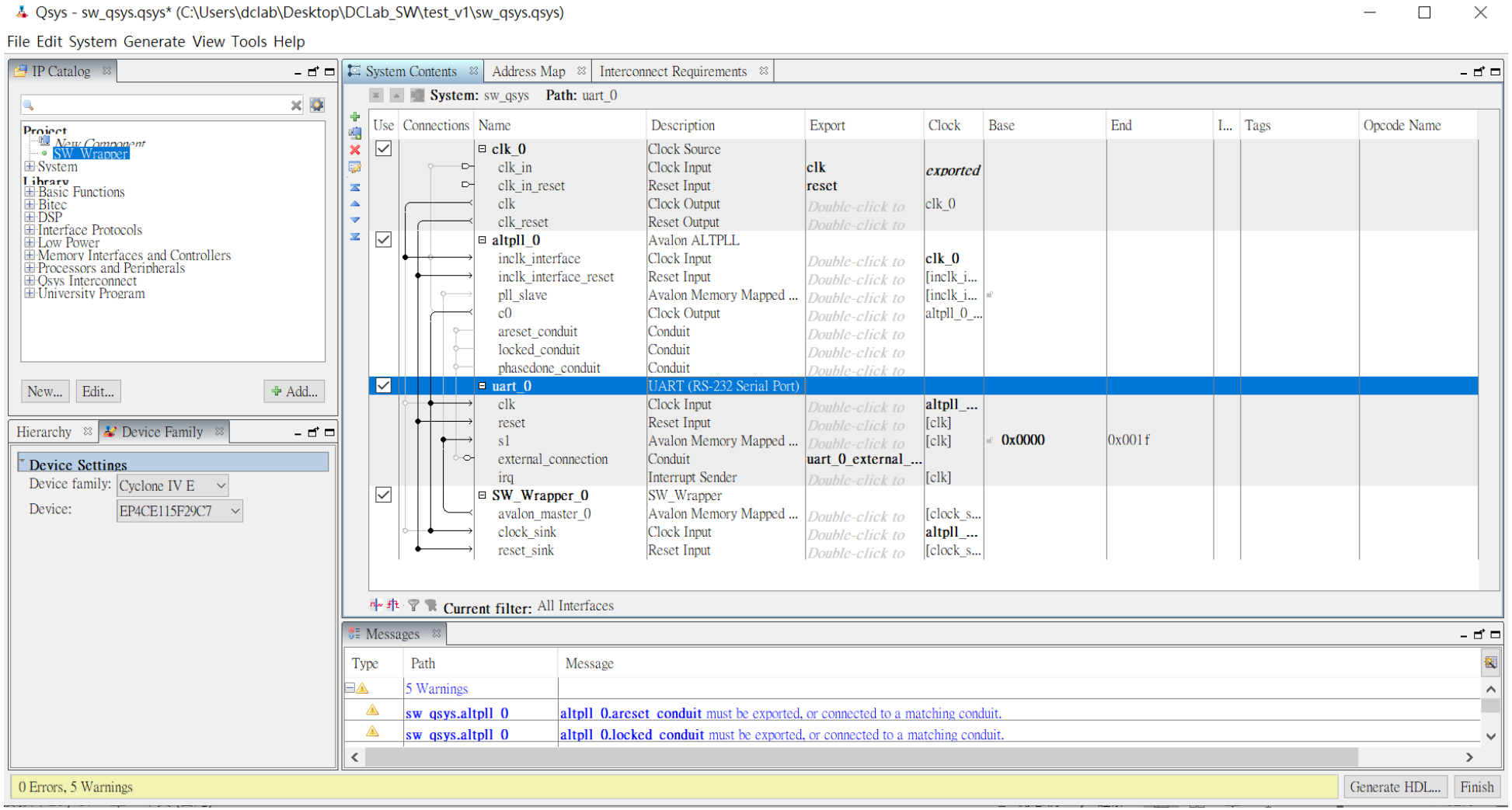
Finish → Yes, save
將搜尋列字串清空可見 SW_Wrapper 在 New Component 底下



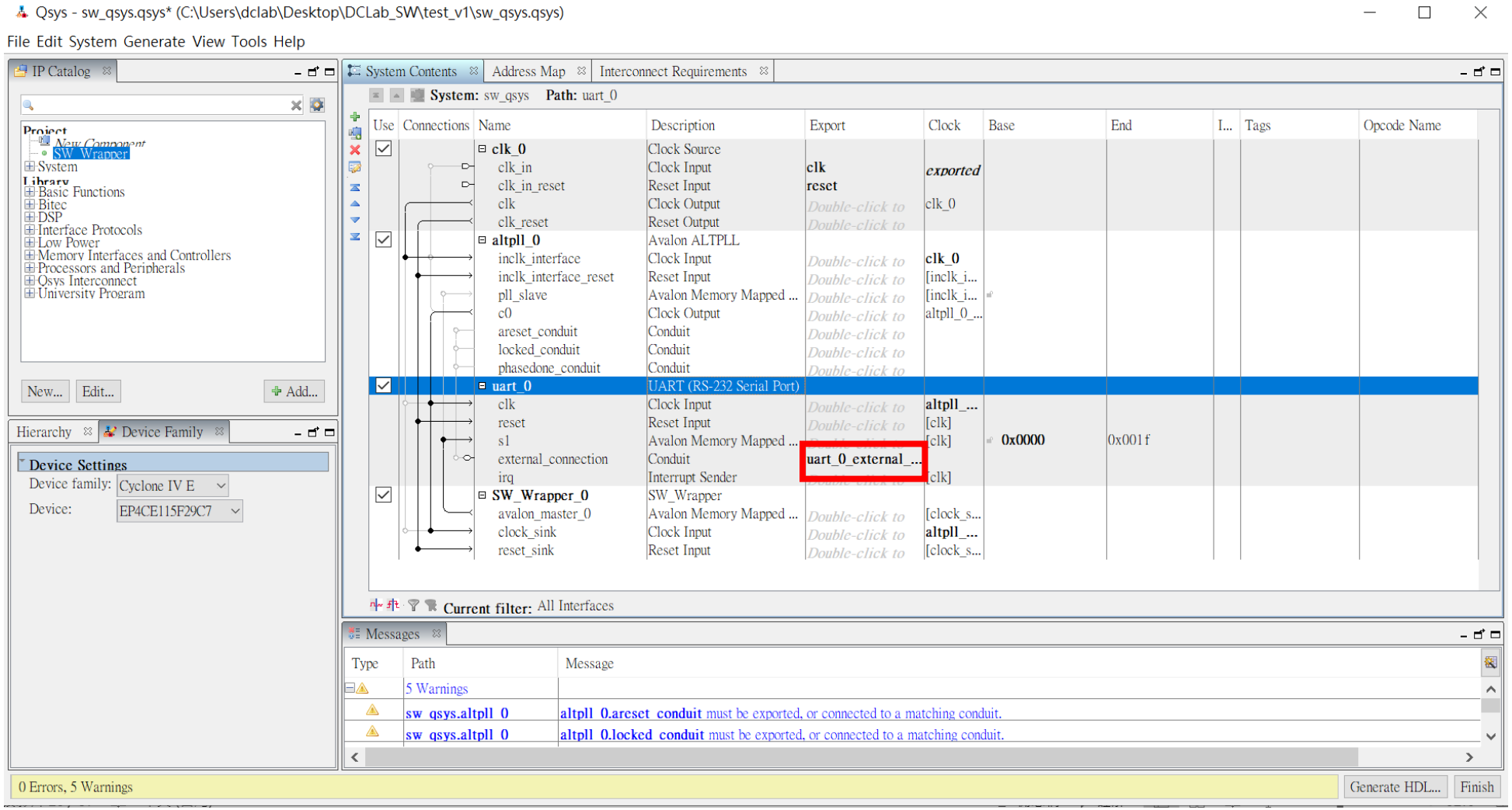
雙擊 SW_Wrapper → Finish



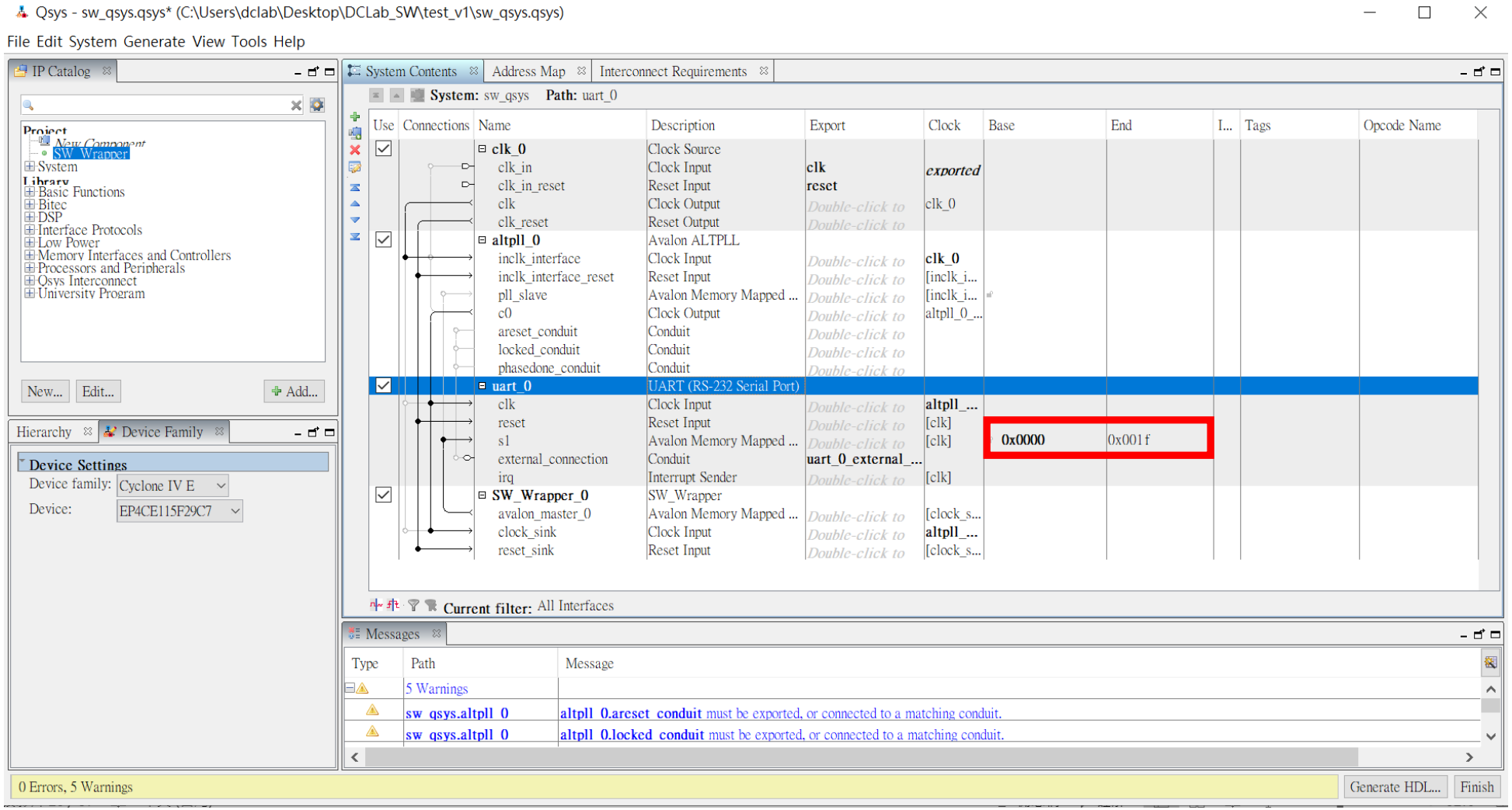
請照圖例接線 (下面 Message 內紅字會不見)



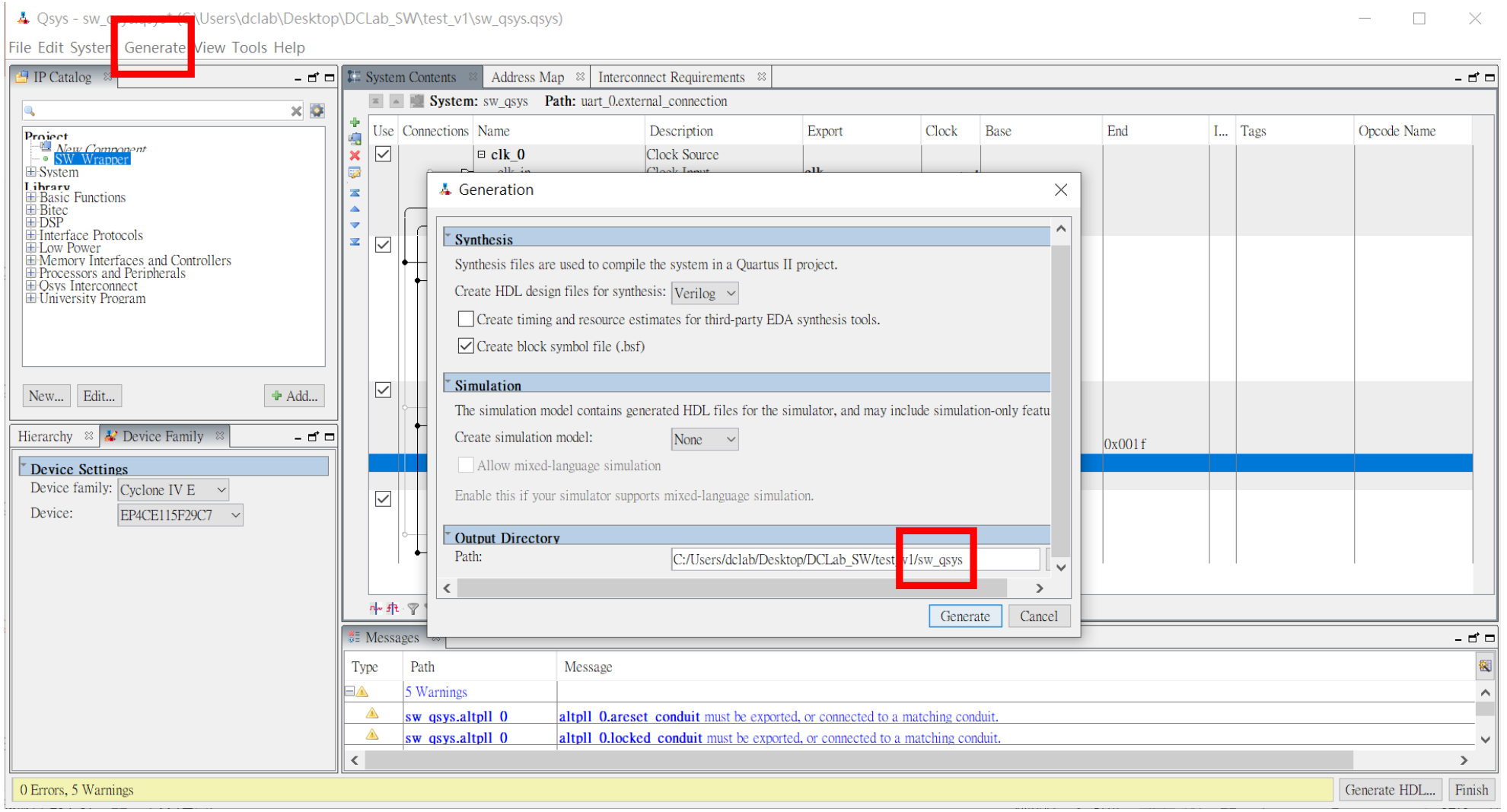
雙擊 external_connection 的 Export 欄位，Enter



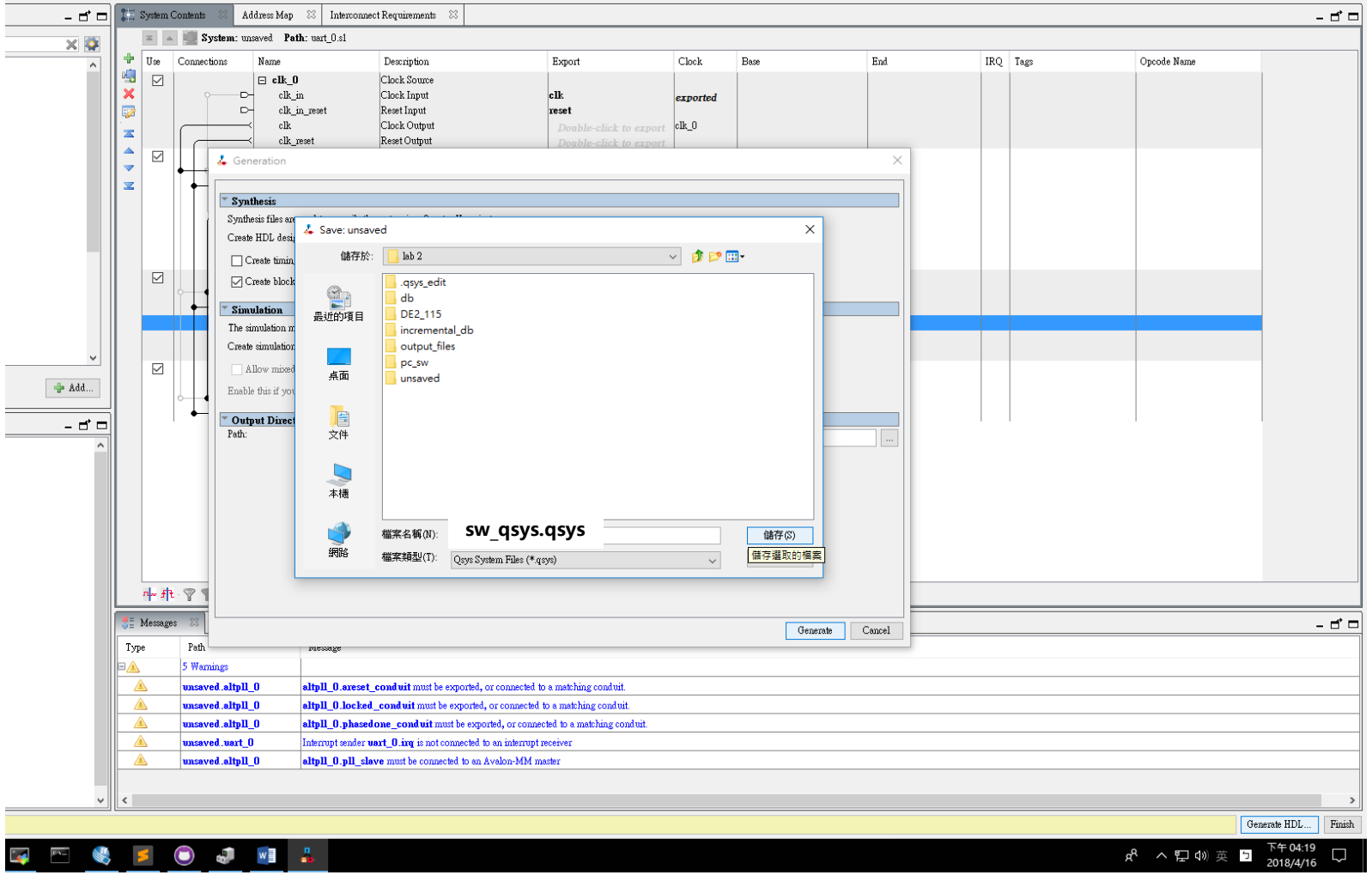
點 s1 的 base 欄位 → s1 被反白選取
System → Assign Base



Generate → Generate… → 將 Output Directory 的最後一層改成 sw_qsys

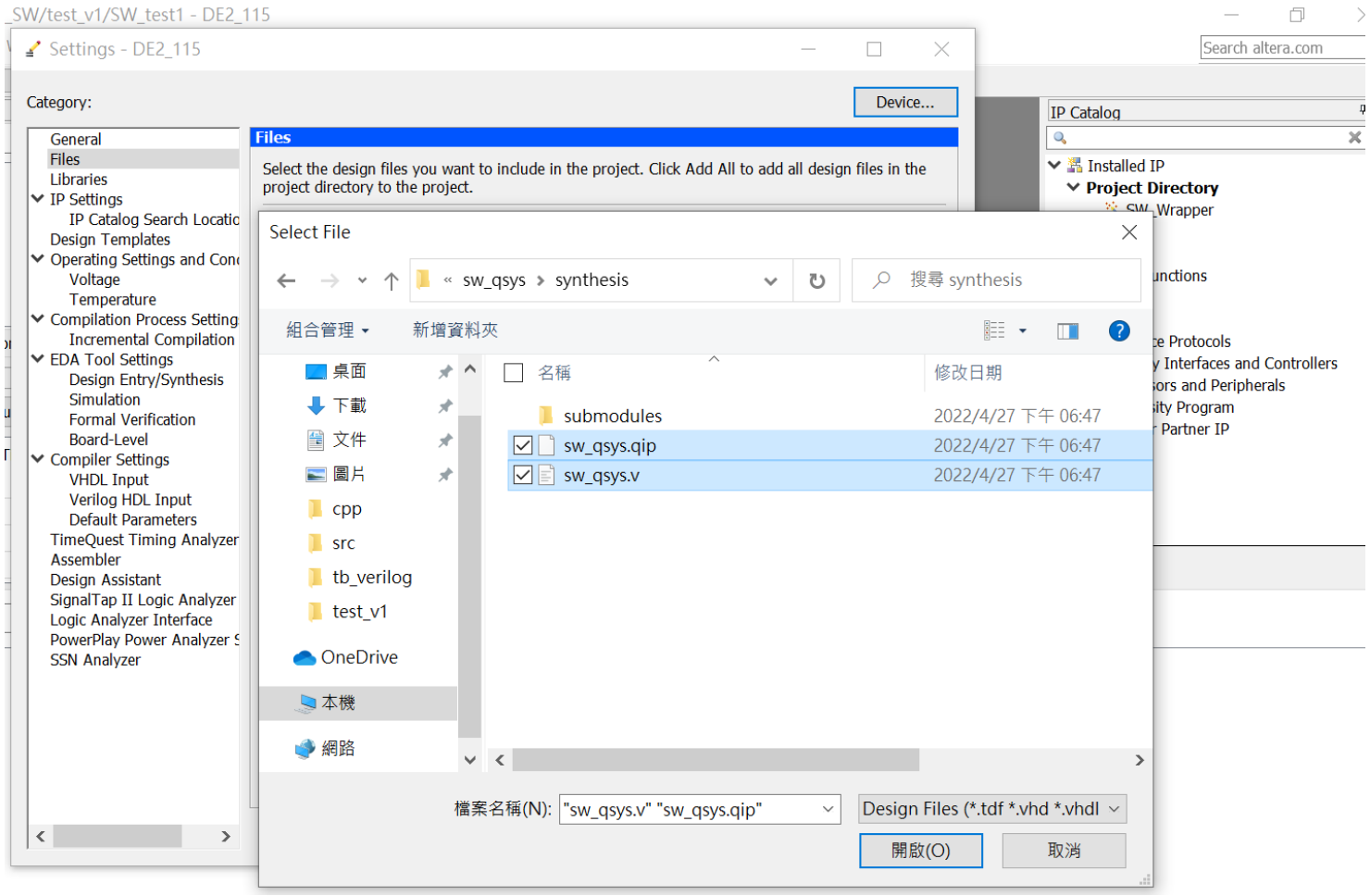


Generate → Save
檔案名稱改成 sw_qsys.qsys，儲存，完畢後按 Close

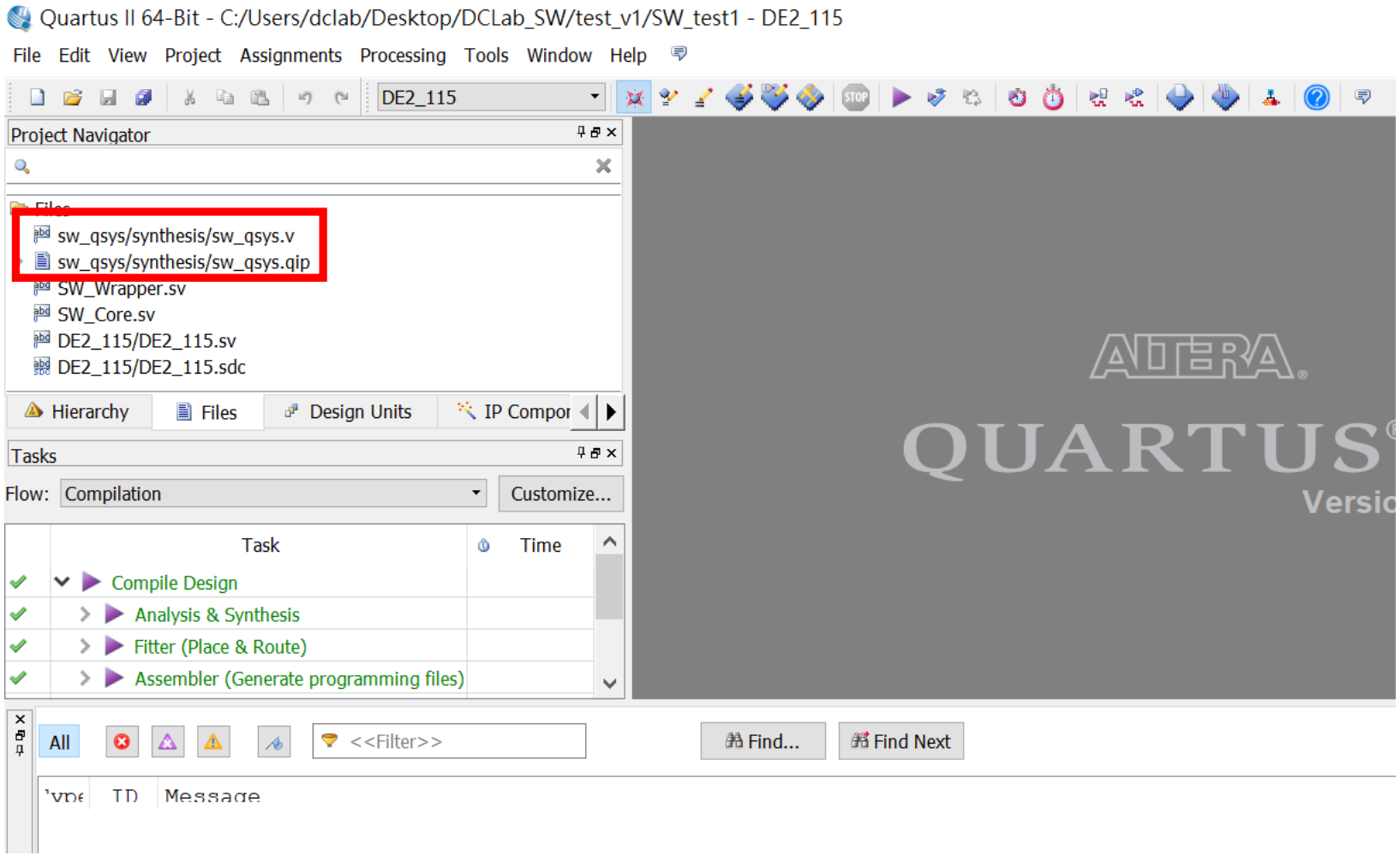


回到 Quartus 視窗 → Assignment → Settings

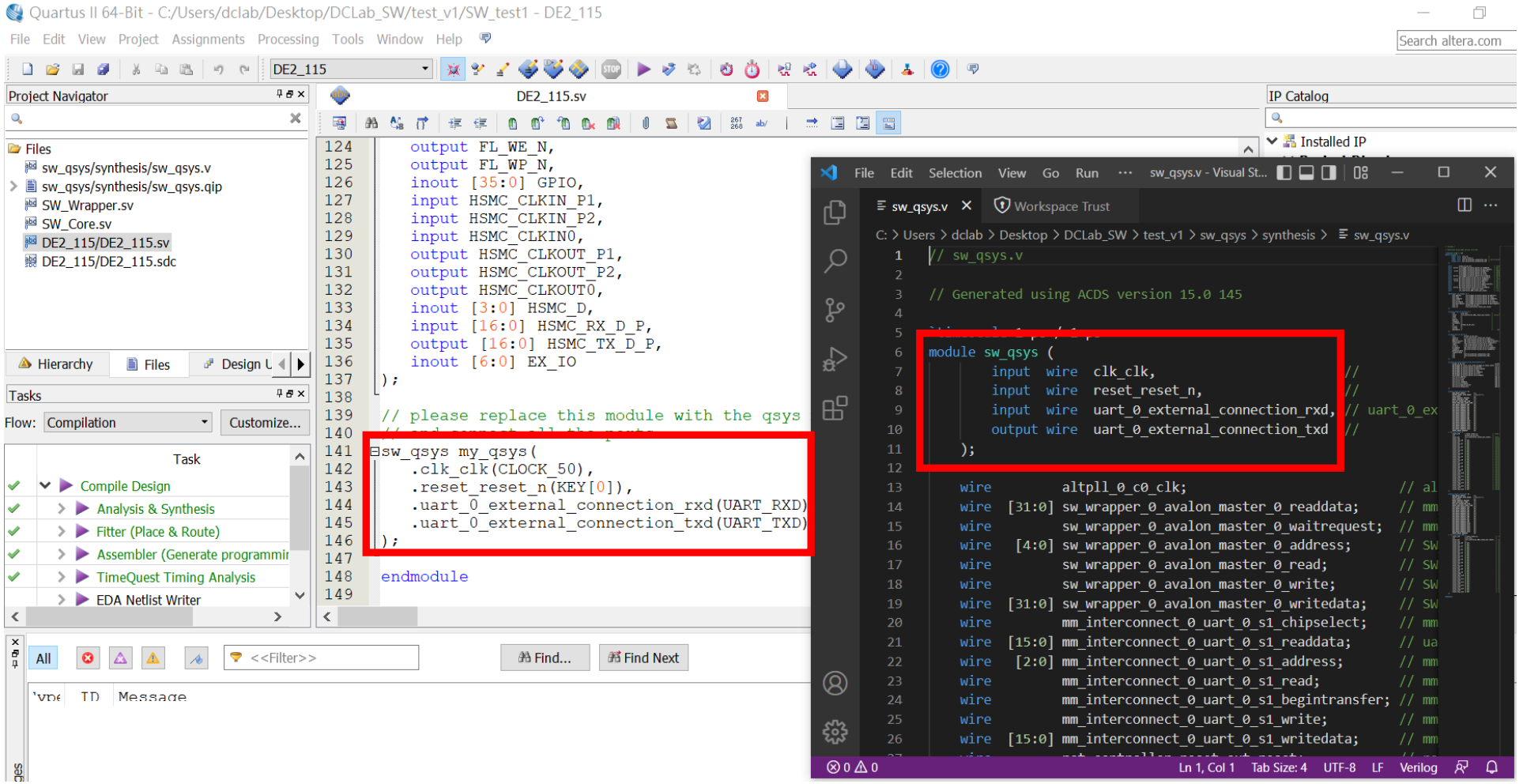
新增 sw_qsys/synethesis 內的 sw_qsys.qip 和 sw_qsys.v → Apply → OK



完成後可以見到 Files 內多出 sw_qsys.v 和 sw_qsys.qip

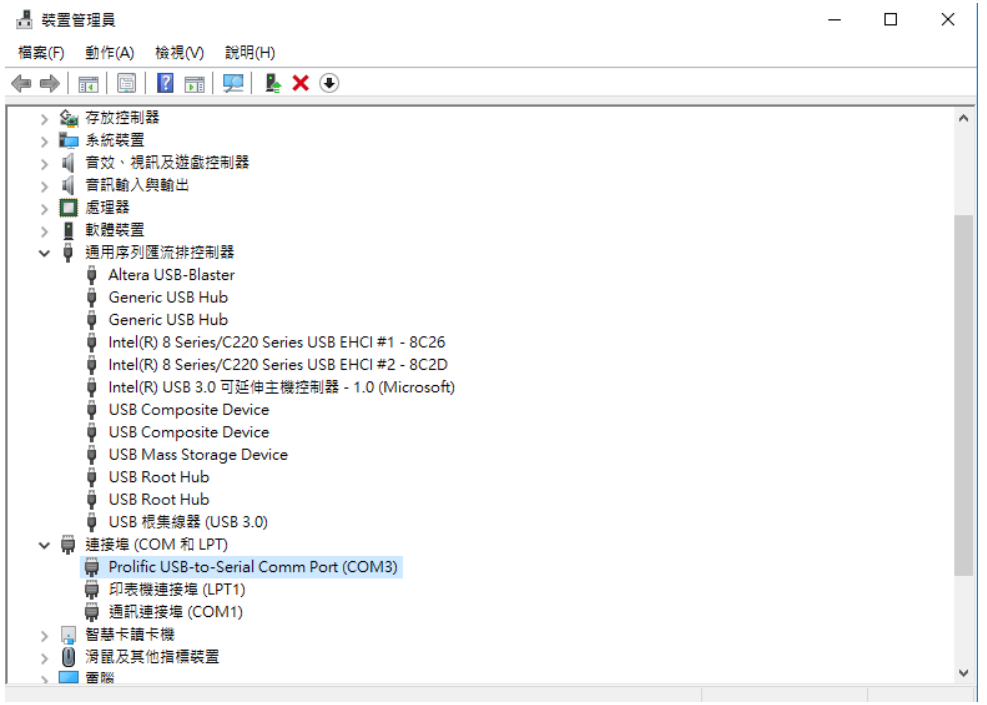


檢查 DE2_115.sv 內使用 sw_qsys 和 sw_qsys.v port 相同



Appendix: Compile (Windows)

1. 裝置管理員→連接埠 (COM和LPT)→Prolific USB-to-Serial Common Port (COM?)
   1) 若沒有發現類似的裝置，則需要安裝對應型號的驅動程式
   2) COM?即為OS指派的port代號



Appendix: Compile (Windows)

2. 按下FPGA上的KEY[0] (做reset)
3. $> python test_rs232.py COM?，?從步驟1.可以得知

Appendix: Compile (Windows)

4. 若要測試不同的testing data檔，則將 test_rs232.py 內的 fp_pat = open() 以及 fp_gold = open() 的檔案路徑改成新生成的檔案路徑
5. 執行後，會顯示有無通過所有測資
6. 經驗法則
    1) Compile時間過短或使用的logic elements數量過少，就算compile successful也可能出錯
    2) 重新 qsys 的話，可以將 qsys 這個資料夾砍掉直接重來
    3) Critical warning: Timing requirement not met代表 qsys 無法滿足timing的要求。有時候可能導致每一次compile的結果不盡相同