

Memory Devices on DE2-115

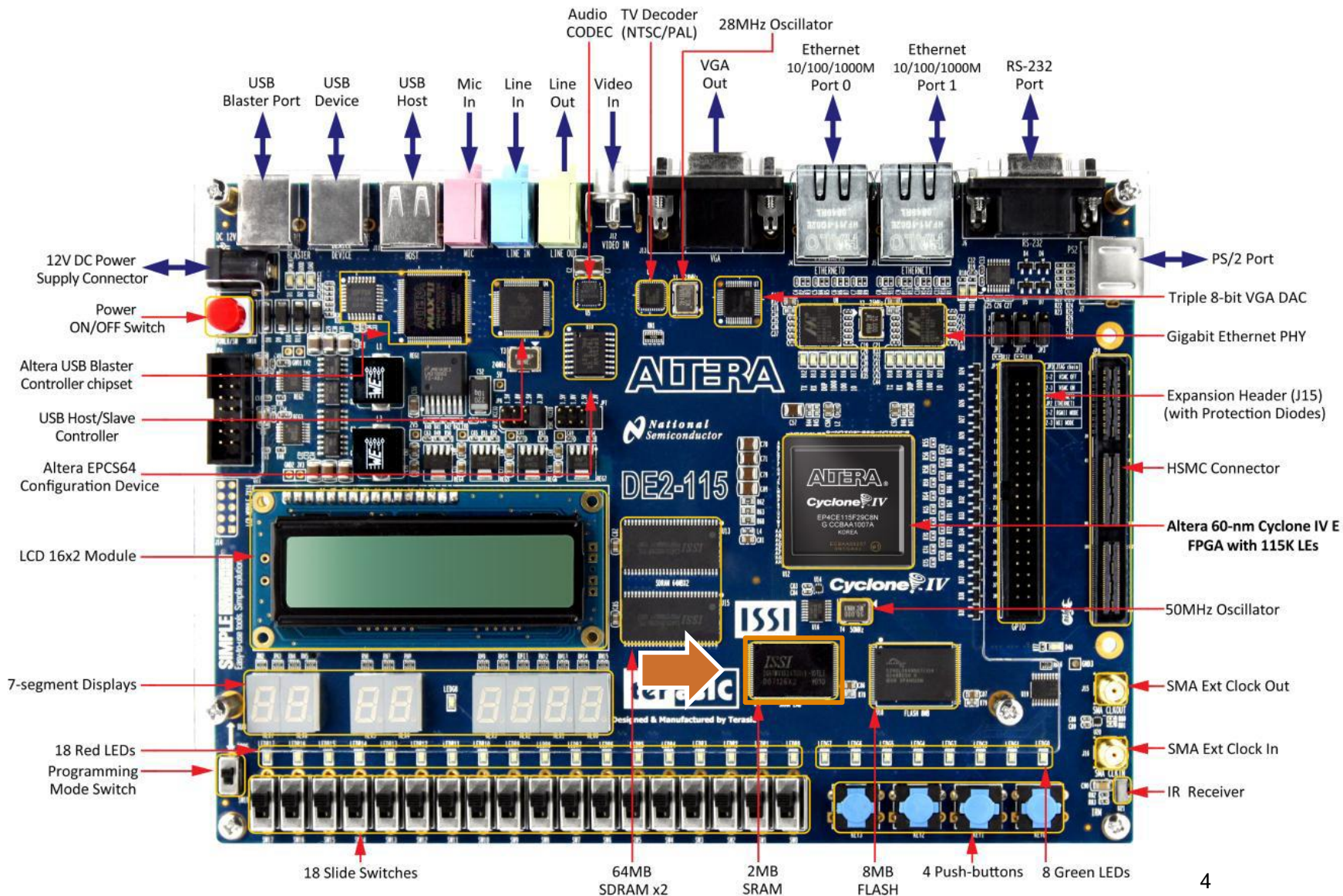
數位電路實驗

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Outline

- SRAM
- SDRAM
- FLASH
- EEPROM
- SD Card

SRAM



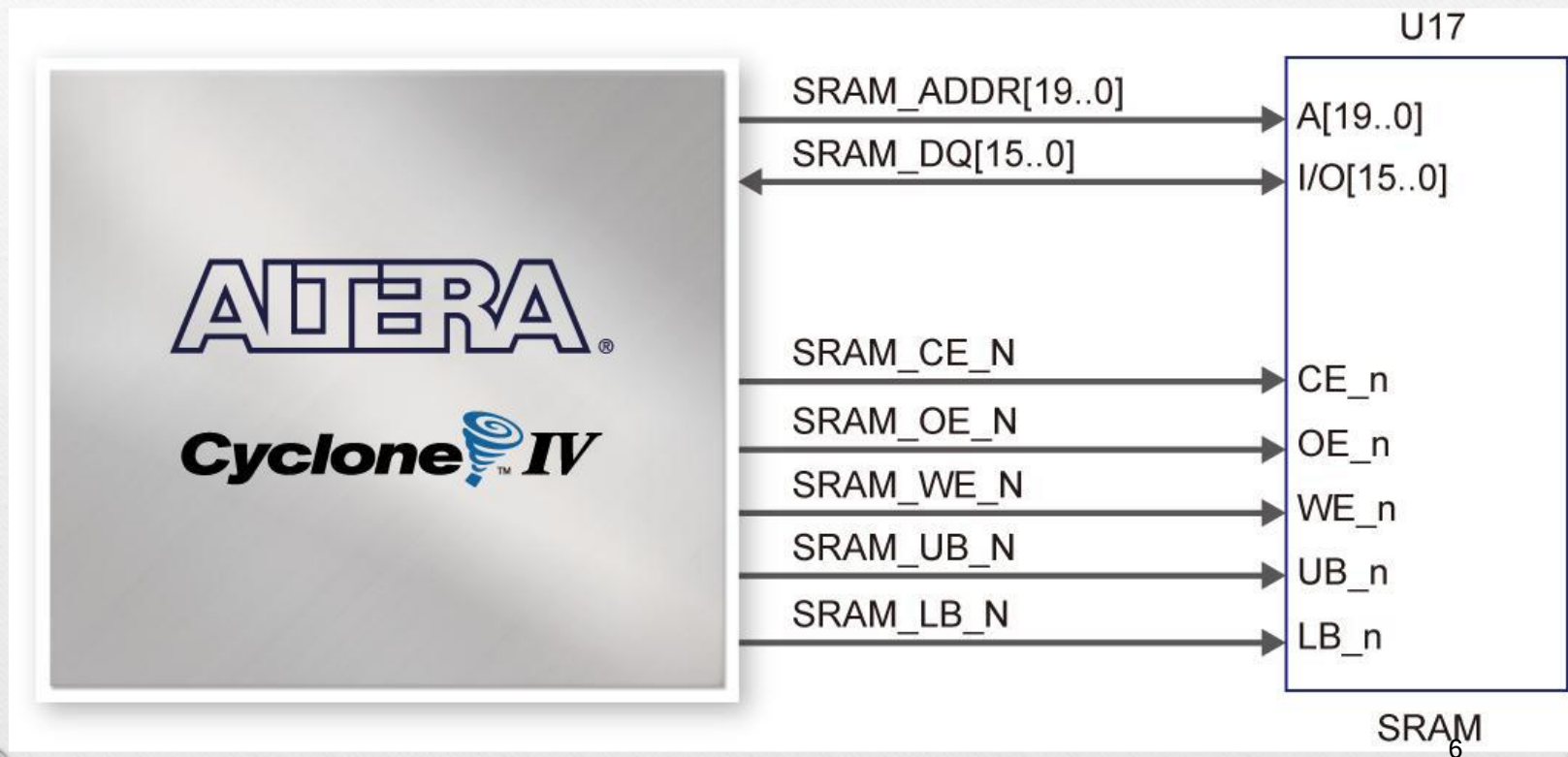
Features

of
addresses

- 16M-bit (2MB) static RAMs organized as 1024K words by 16 bits.
- High-speed access times:
 - speed = 20ns for VDD 1.65V to 2.2V
 - speed = 10ns for VDD 2.4V to 3.6V
 - speed = 8ns for VDD 3.3V + 5%

Maximum performance frequency: 125MHz

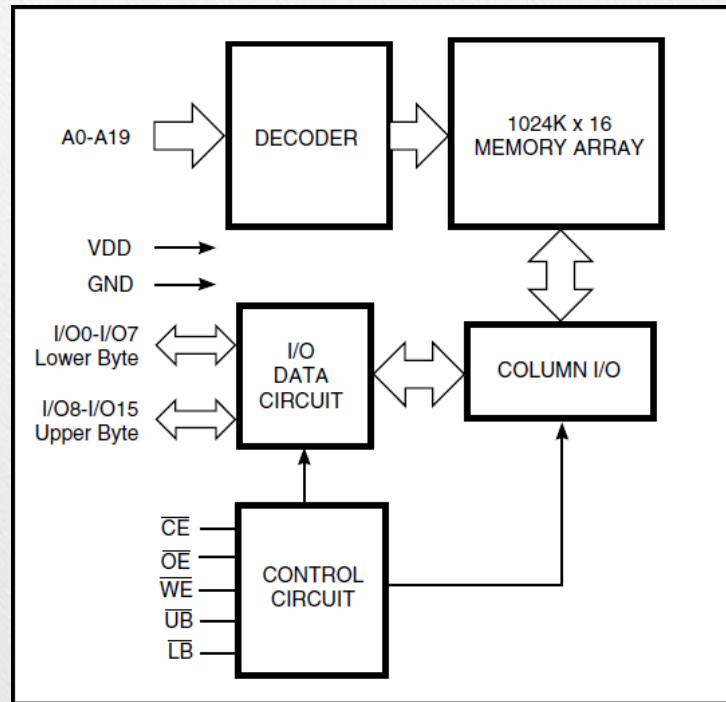
Schematic Diagram



SRAM Pin Assignments

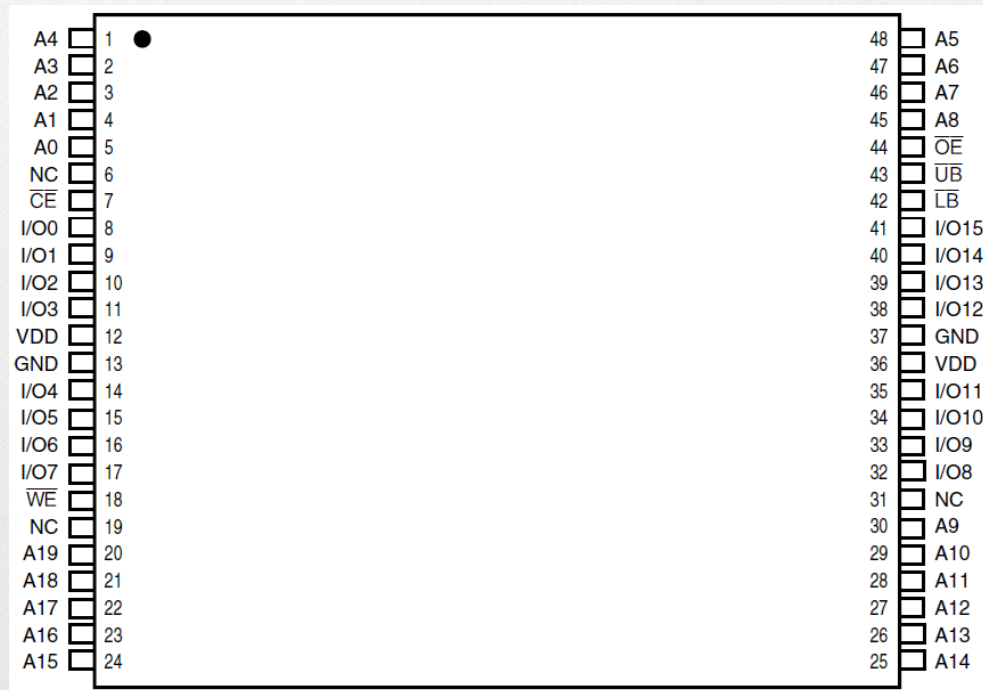
Signal Name	FPGA Pin No.	Description
SRAM_ADDR[0]~	PIN_AB7~	SRAM Address[0]~
SRAM_DQ[0]~	PIN_AH3~	SRAM Data[0]~
SRAM_OE	PIN_AD5	SRAM Output Enable
SRAM_WE	PIN_AE8	SRAM Write Enable
SRAM_CE	PIN_AF8	SRAM Chip Enable
SRAM_LB	PIN_AD4	SRAM Lower Byte Control
SRAM_UB	PIN_AC4	SRAM Upper Byte Control

SRAM Block Diagram



SRAM Pin Configuration

- 48-pin TSOP-1 (12mm x 20mm)

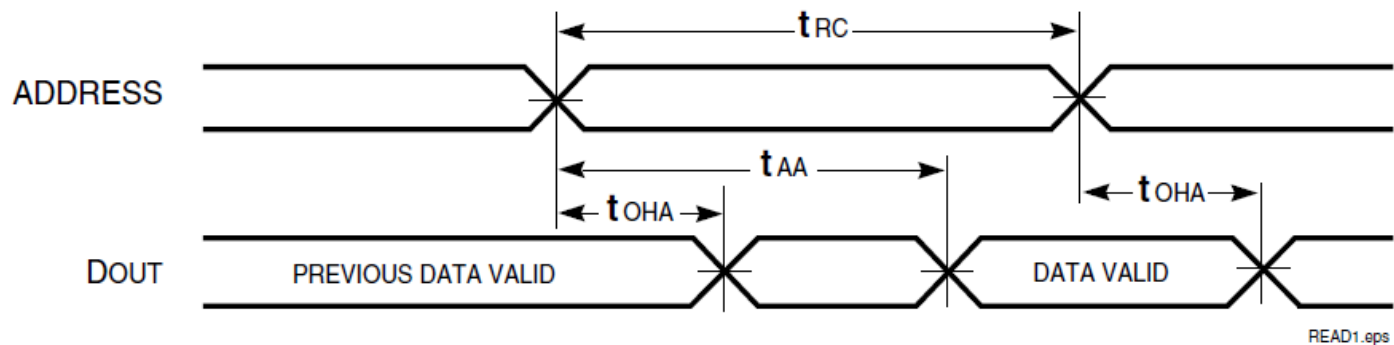


Truth Table

Mode	\overline{WE}	\overline{OE}	\overline{OE}	\overline{LB}	\overline{UB}	I/O PIN		V_{DD} Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	DOUT	High-Z	I_{CC}
	H	L	L	H	L	High-Z	DOUT	
	H	L	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	I_{CC}
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

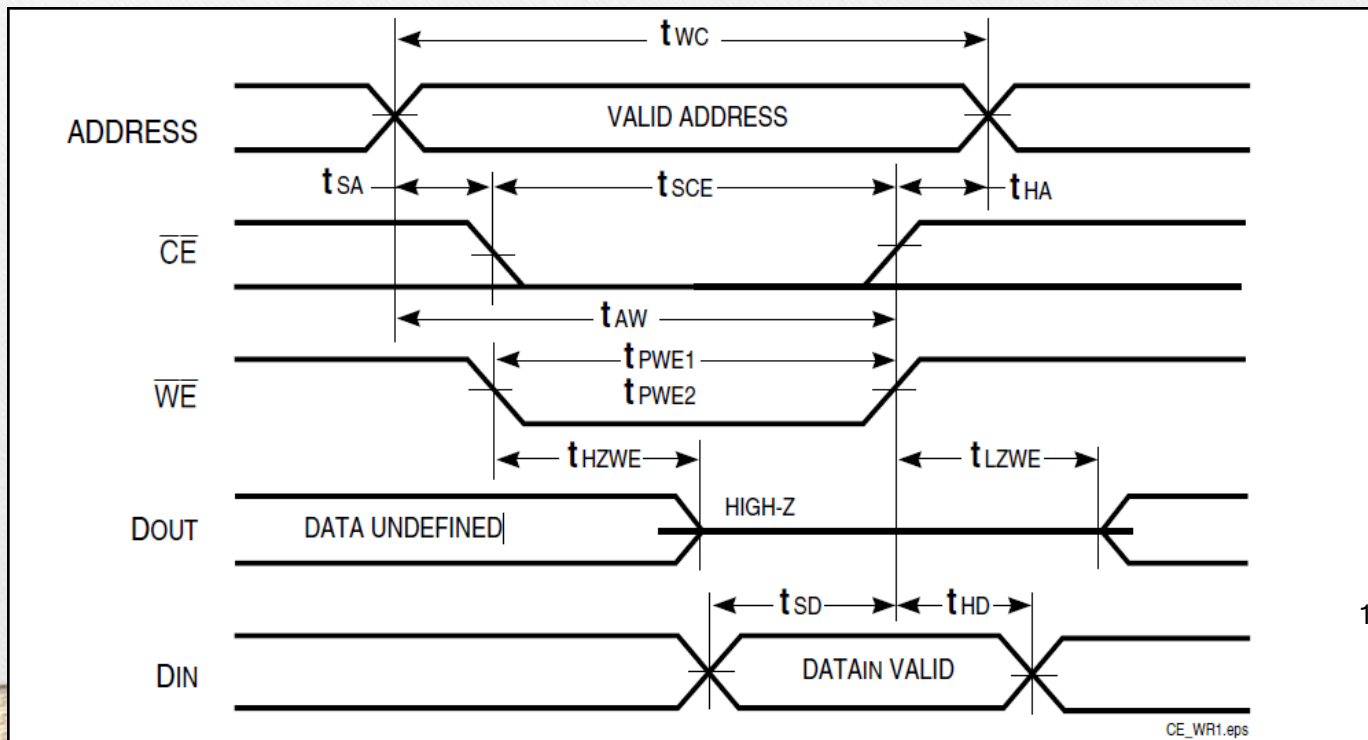
Read Cycle

- Min. read cycle time $t_{RC} = 8\text{ns}$



Write Cycle

- Min. write cycle time $t_{WC} = 8ns$



The End.

Any question?

Reference

1. "DE2-115 User Manual" by Terasic.
2. "DE2-115_MB.pdf" by Terasic.
3. "61WV102416ALL(ISSI_1M x 16_SRAM).pdf" by ISSI.