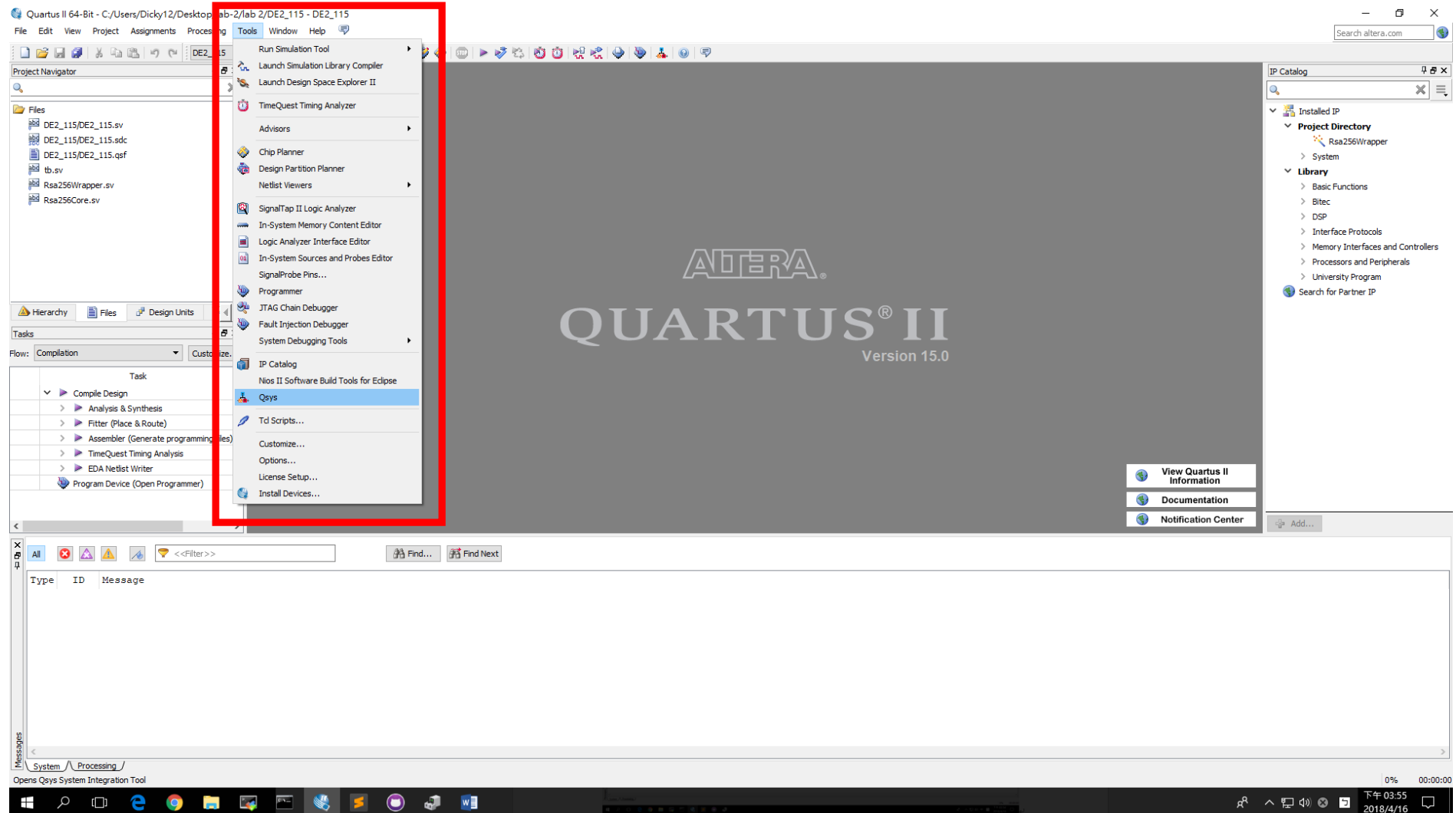


Qsys on Quartus 15.0 Tutorial for lab_bonus_SW

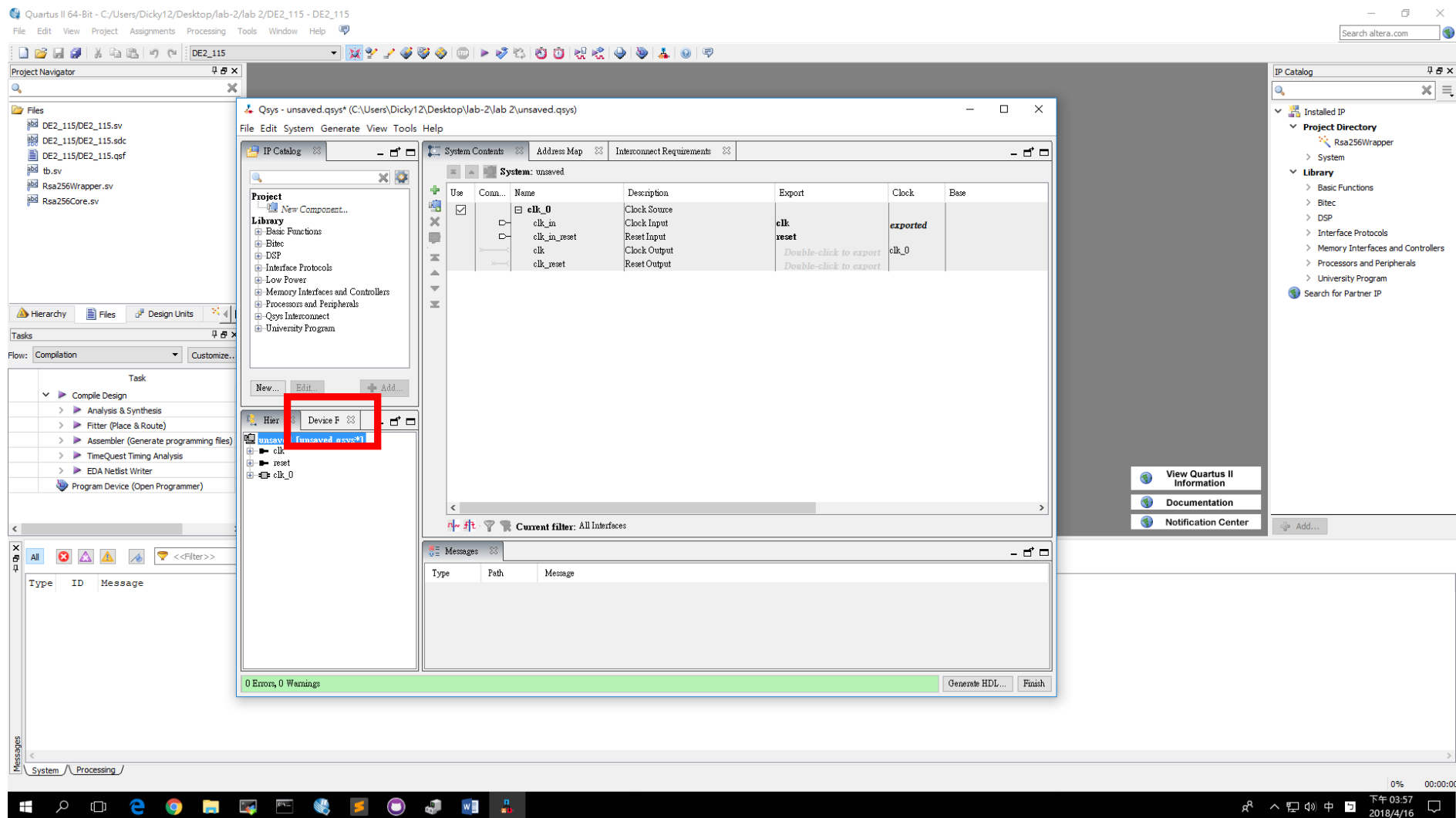
提供：董子維、楊其昇

整理：鍾杰、楊仲萱

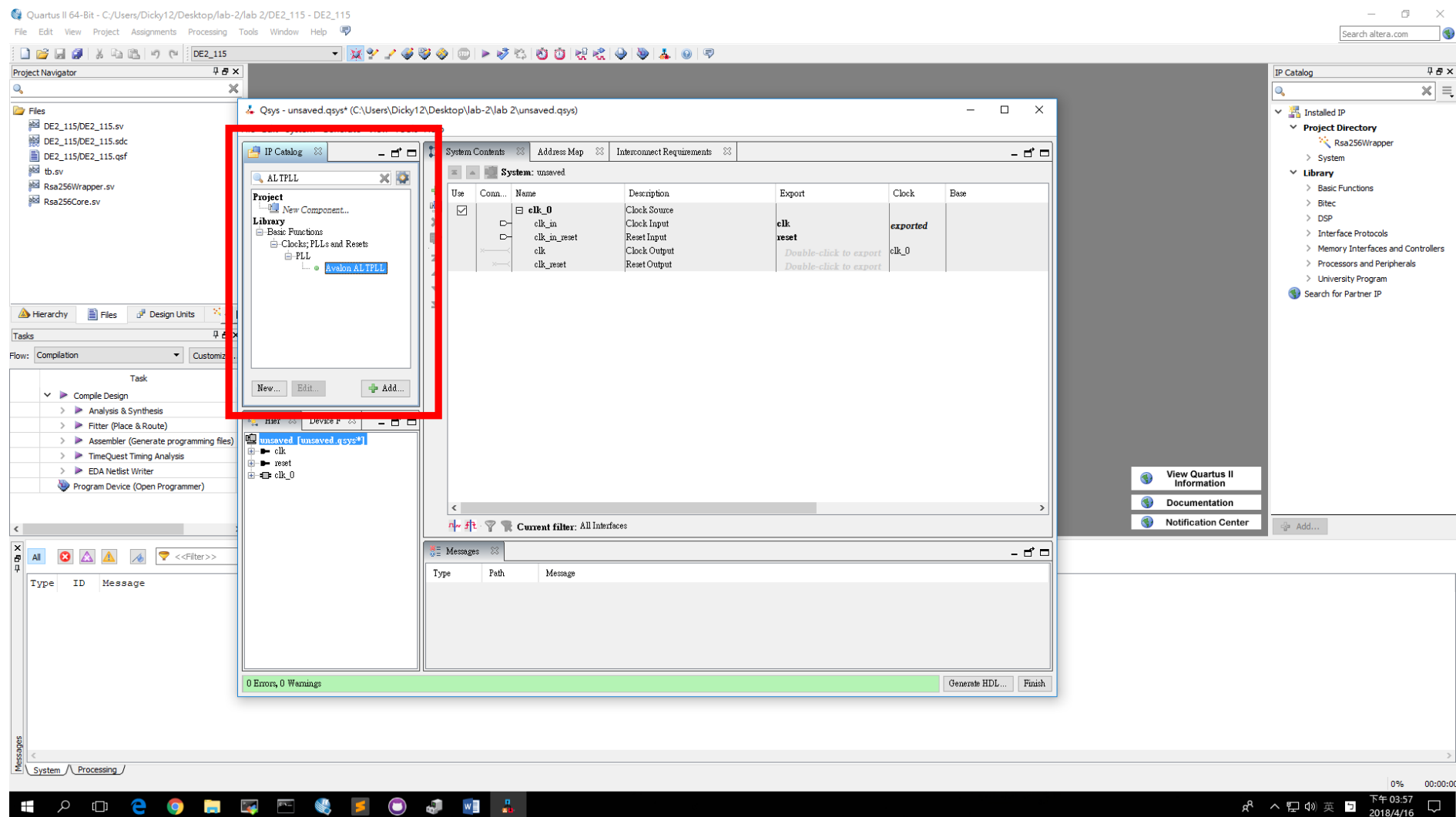
打開Qsys (Tool → Qsys)



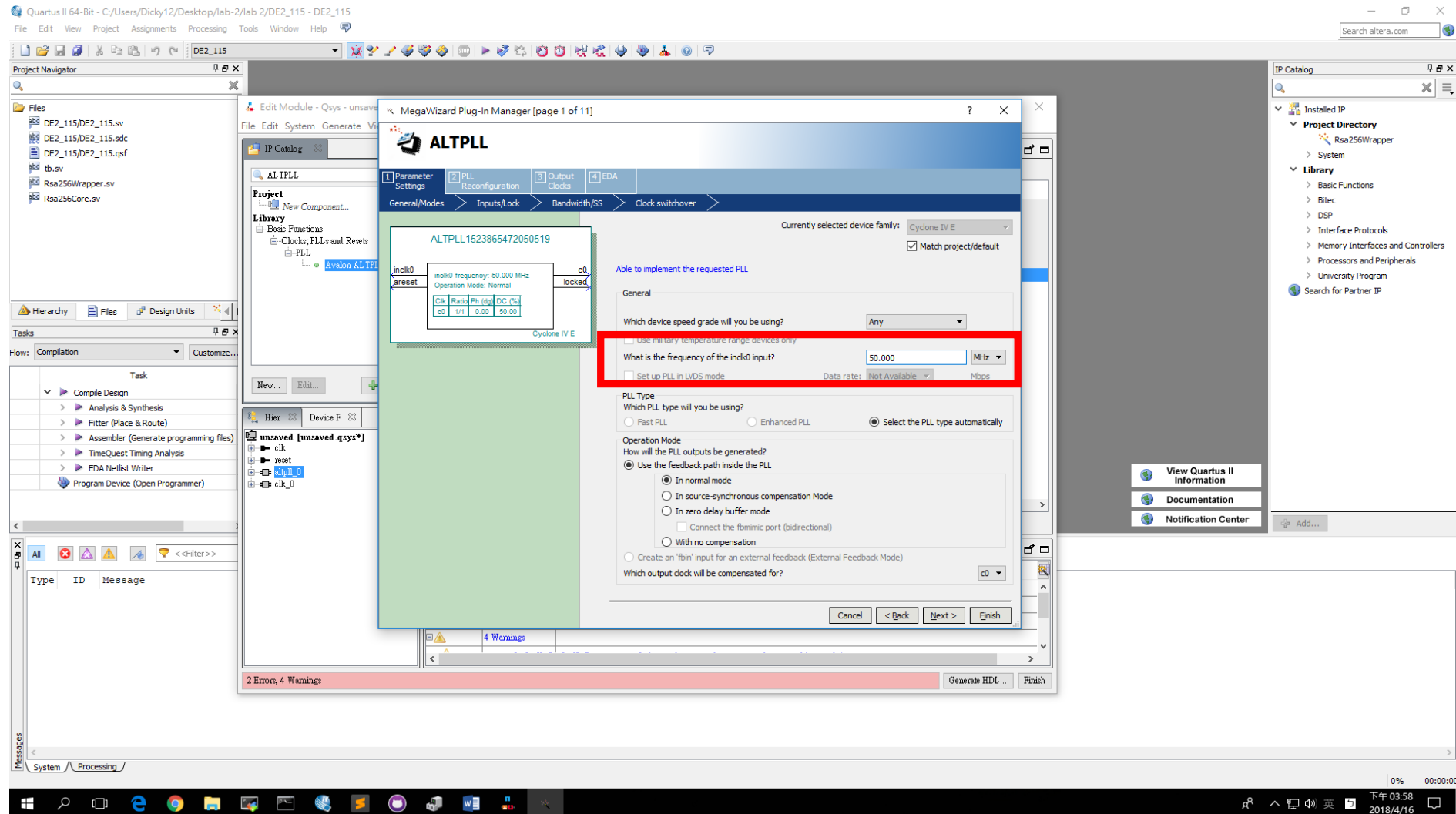
到Device Family選擇Cyclone IV



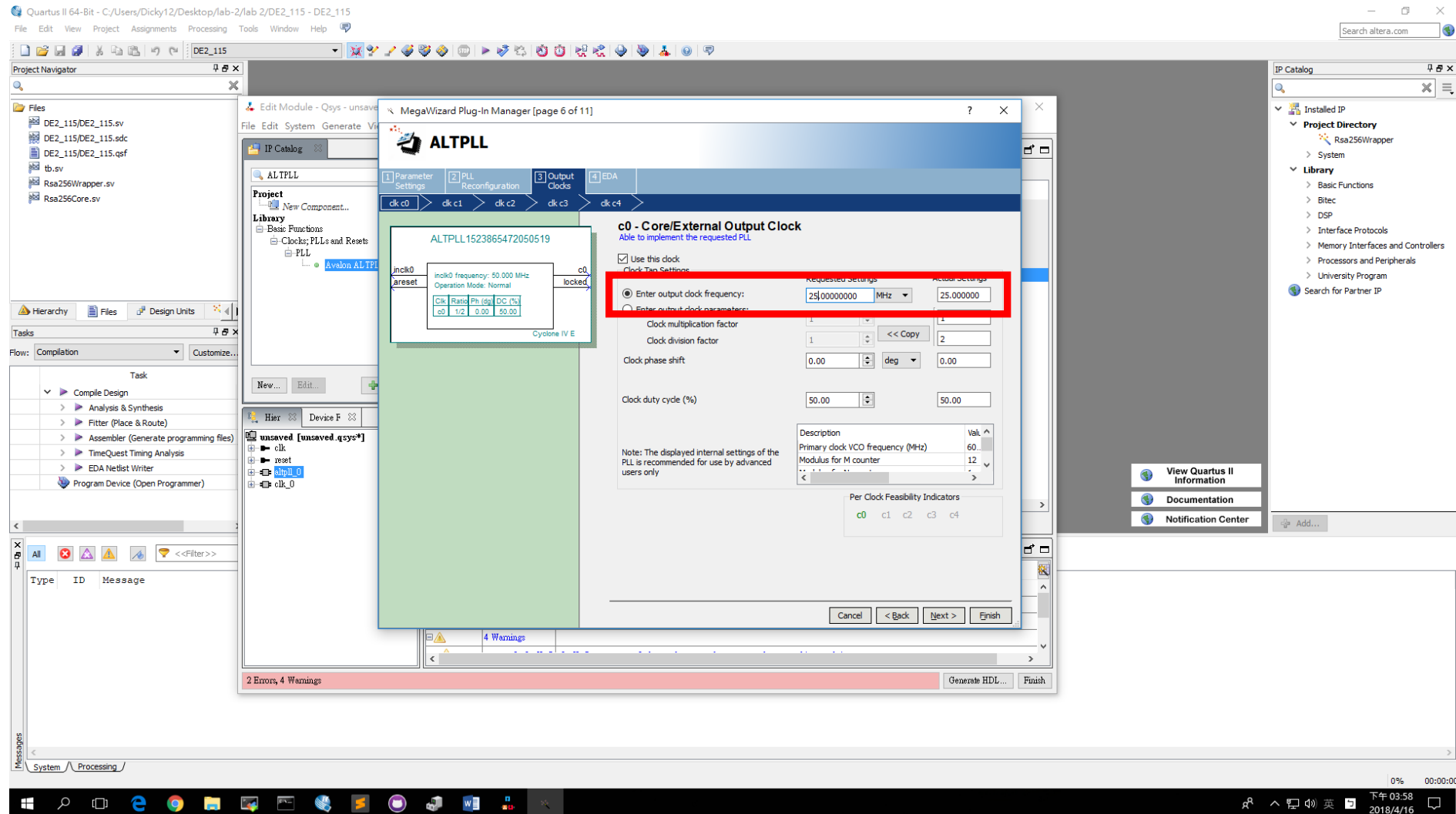
搜尋Avalon ALTPLL, 雙擊新增



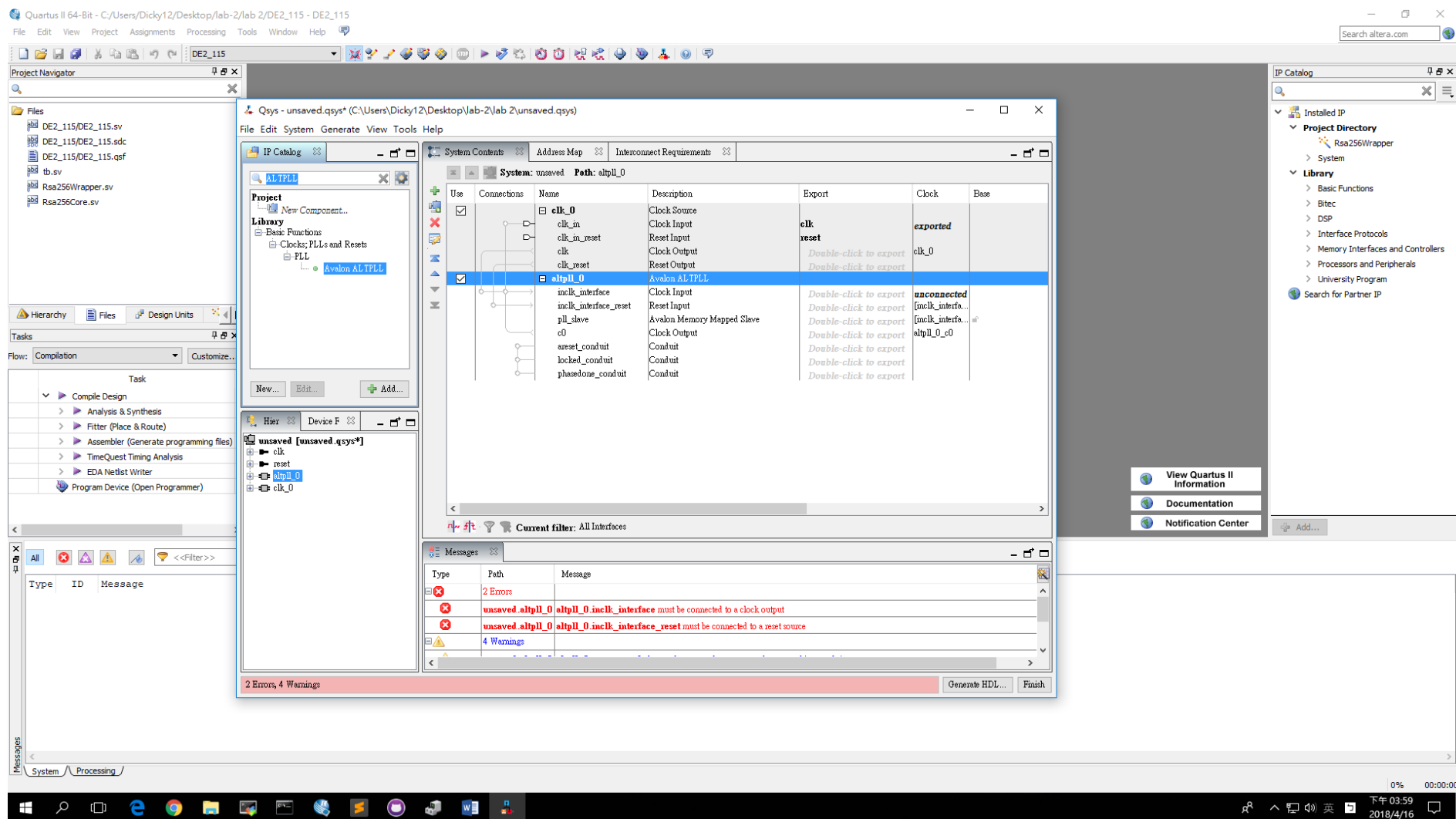
Frequency of inclk0 input = 50MHz



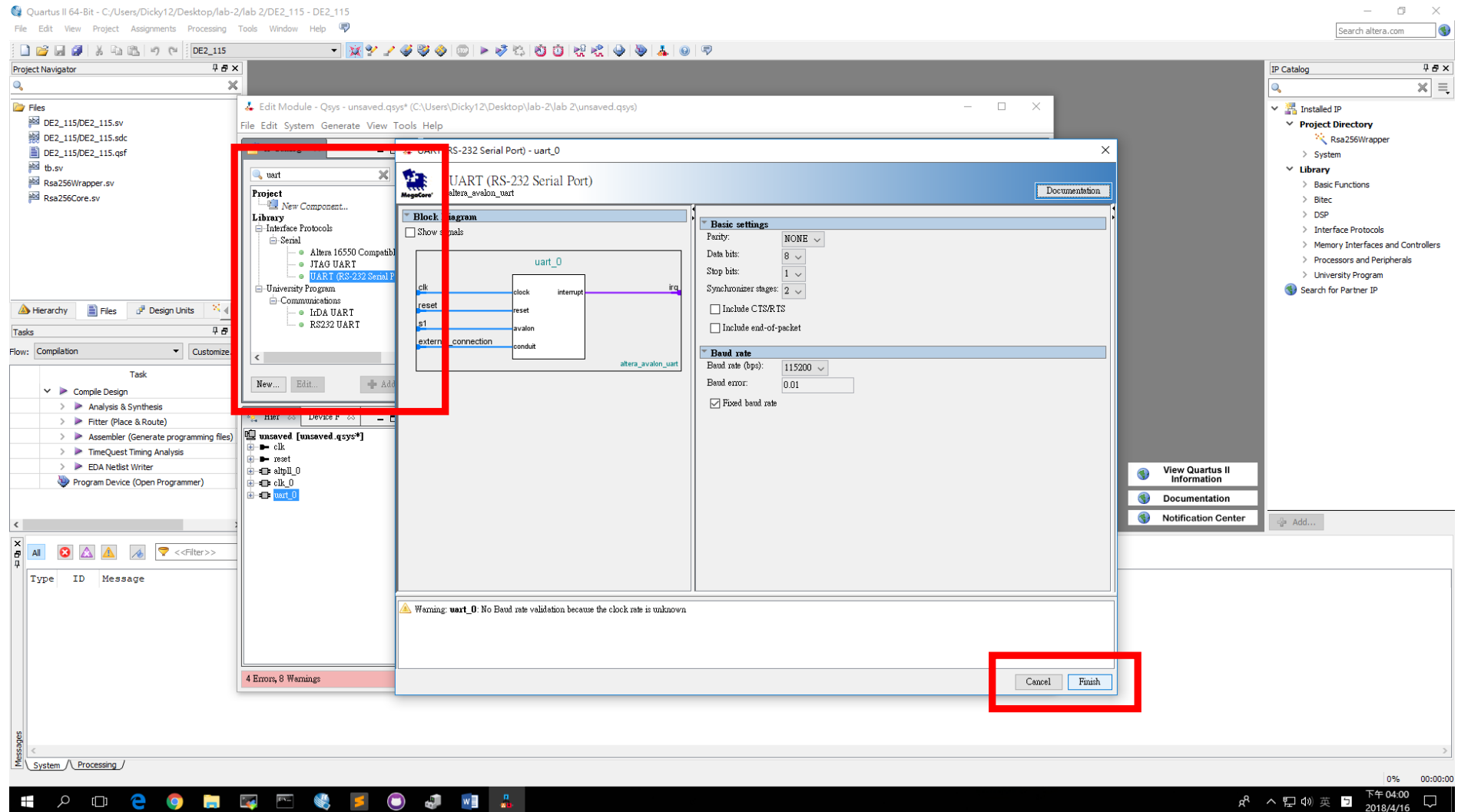
Output clock frequency = 25MHz



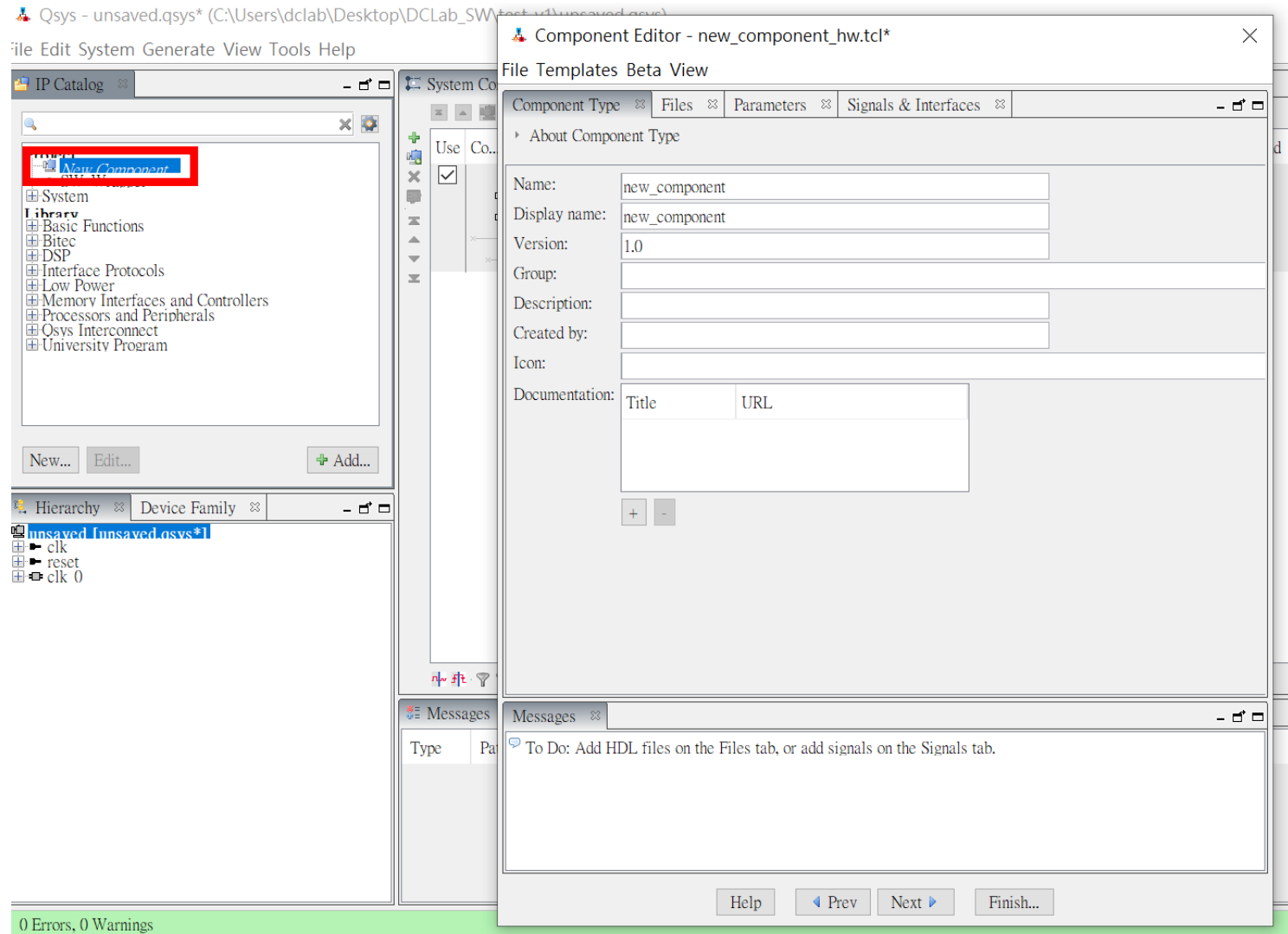
按 Finish 可在右側看到新增的 ALTPLL



搜尋 UART → UART (RS-232 Serial Port) → Finish

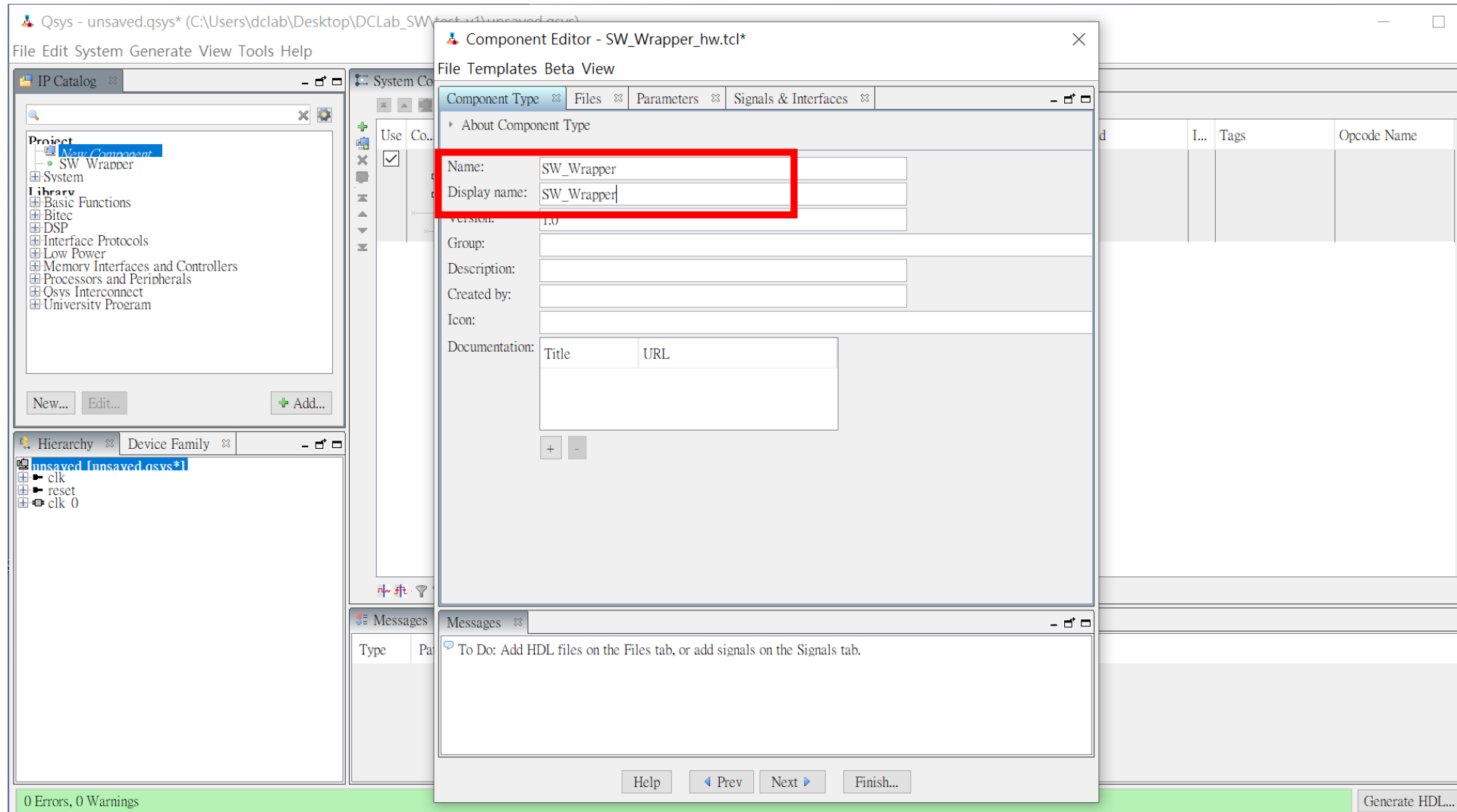


雙擊 New Component



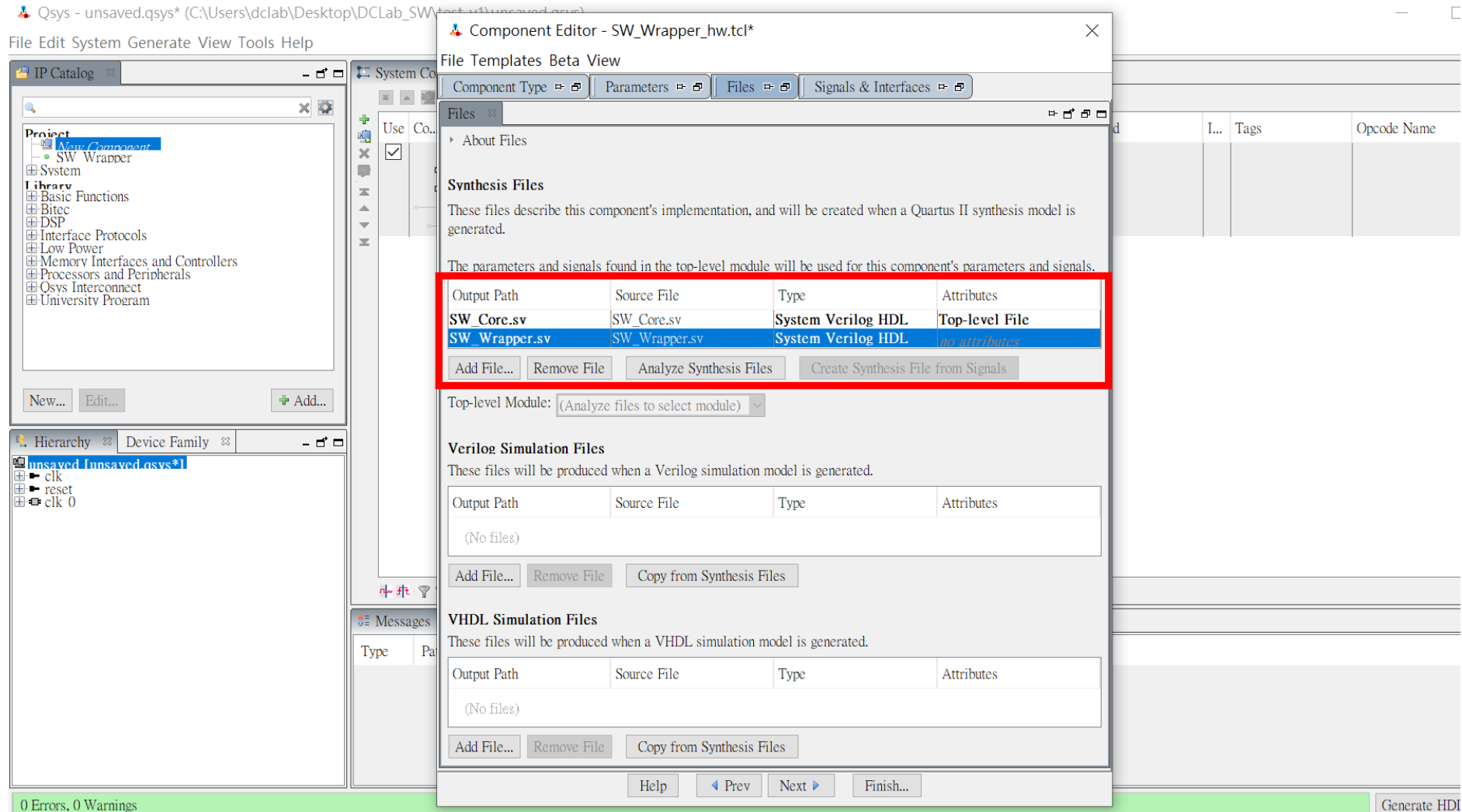
Name = SW_Wrapper

Display Name = SW_Wrapper

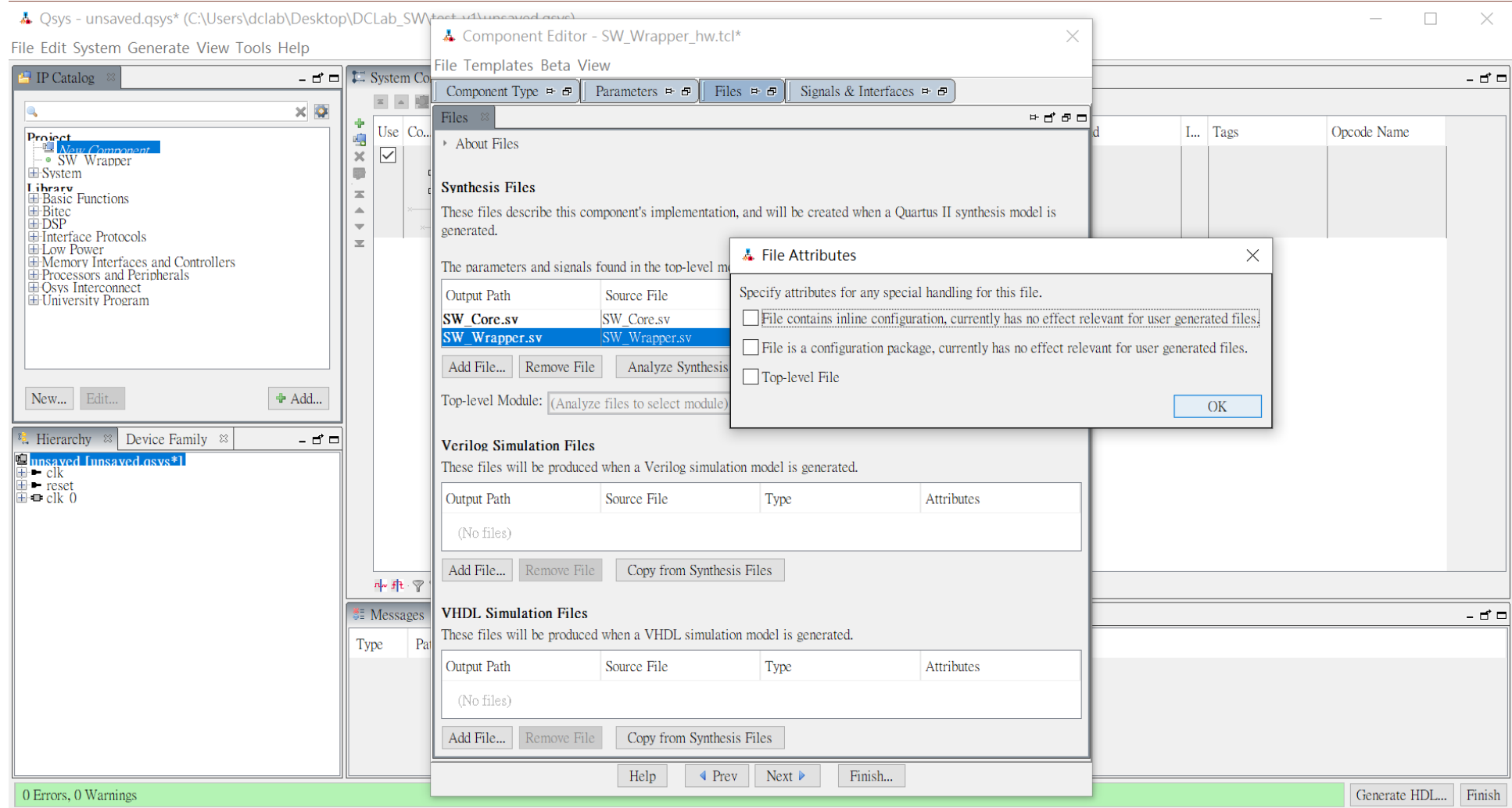


File → Add File

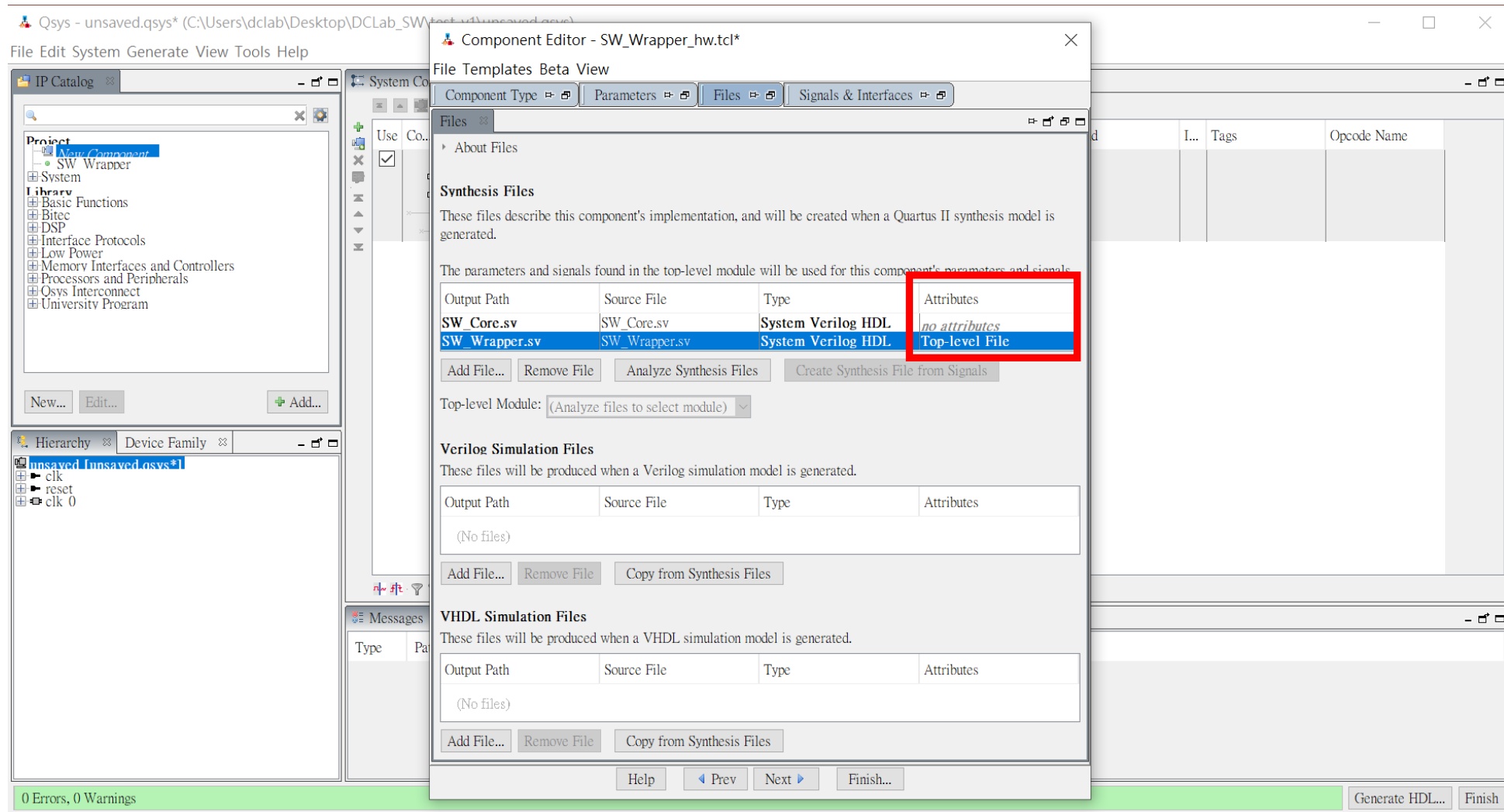
新增 SW_Core.sv 和 SW_Wrapper.sv



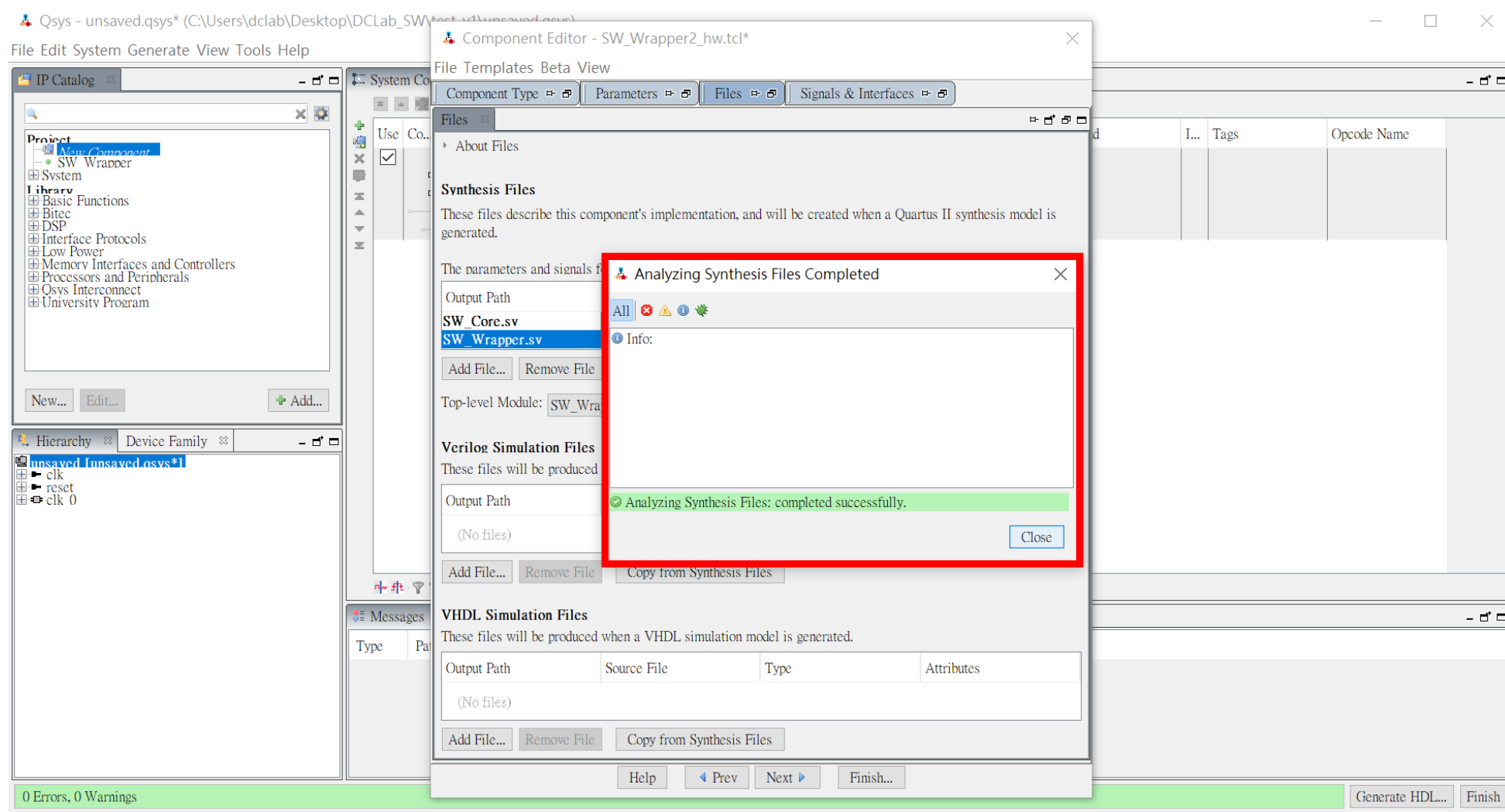
將 SW_Wrapper 改成 Top level file (1/2)



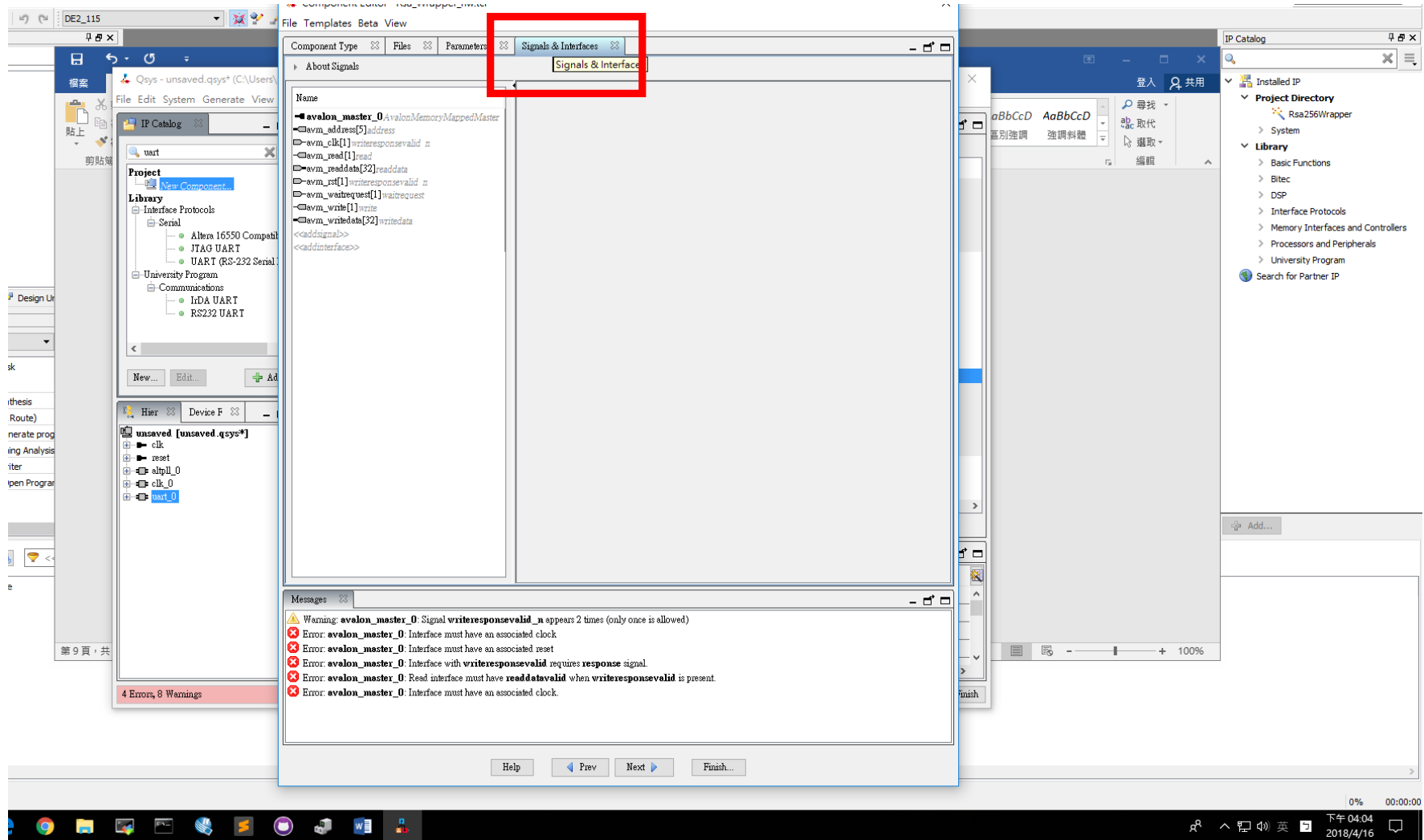
將 SW_Wrapper 改成 Top level file (2/2)



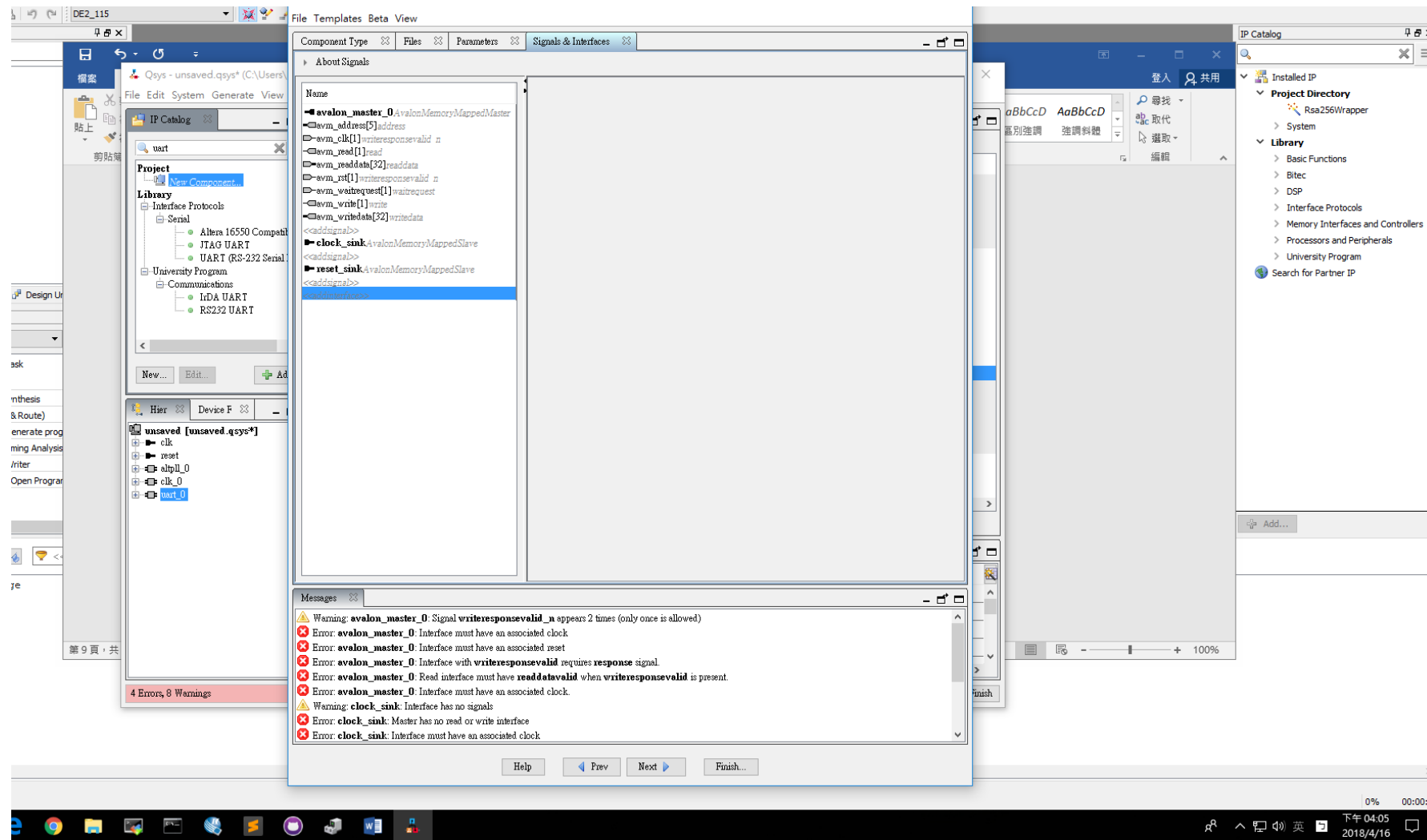
Analyze Synthesis File → Close



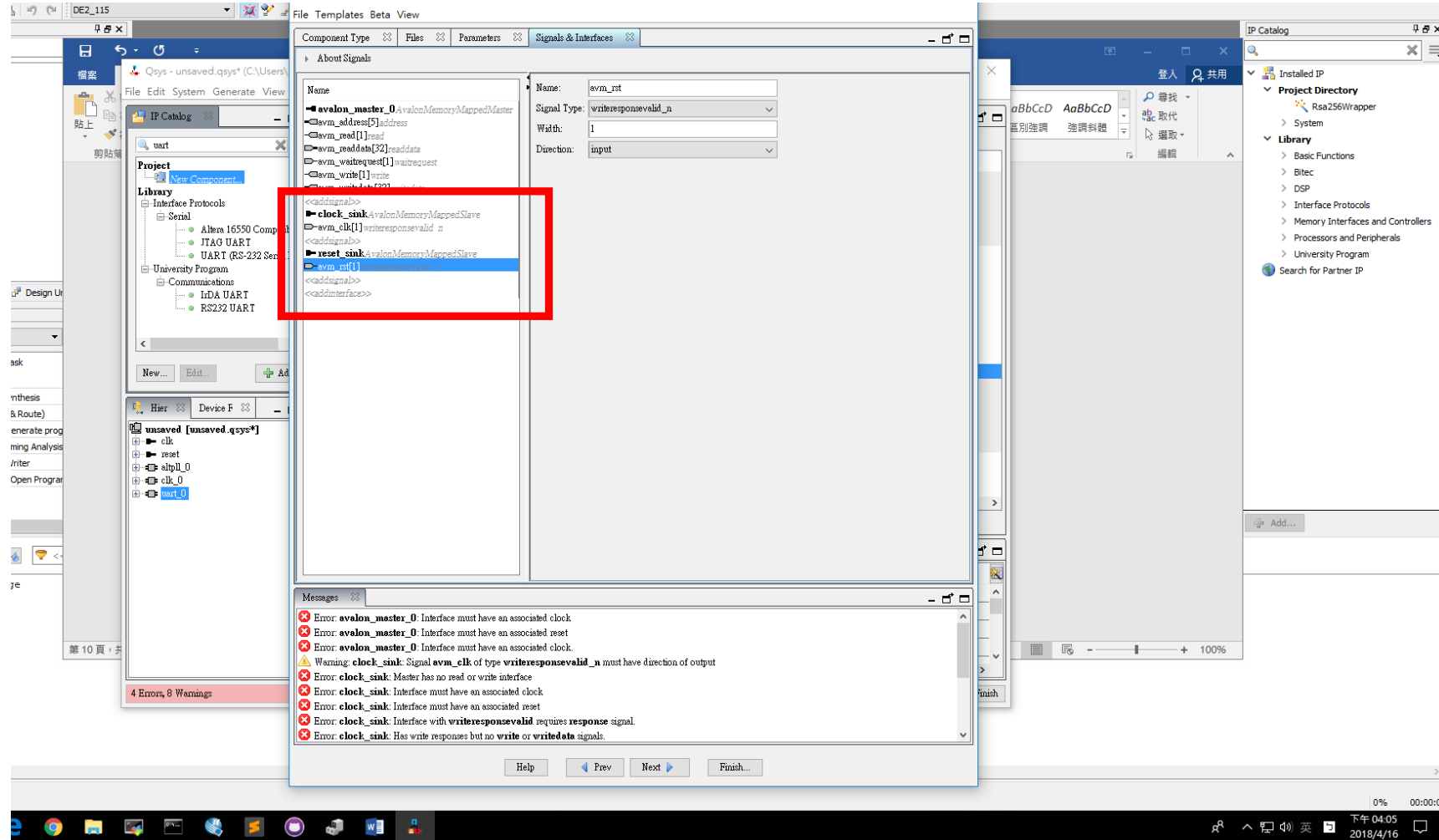
選 Signal Interface



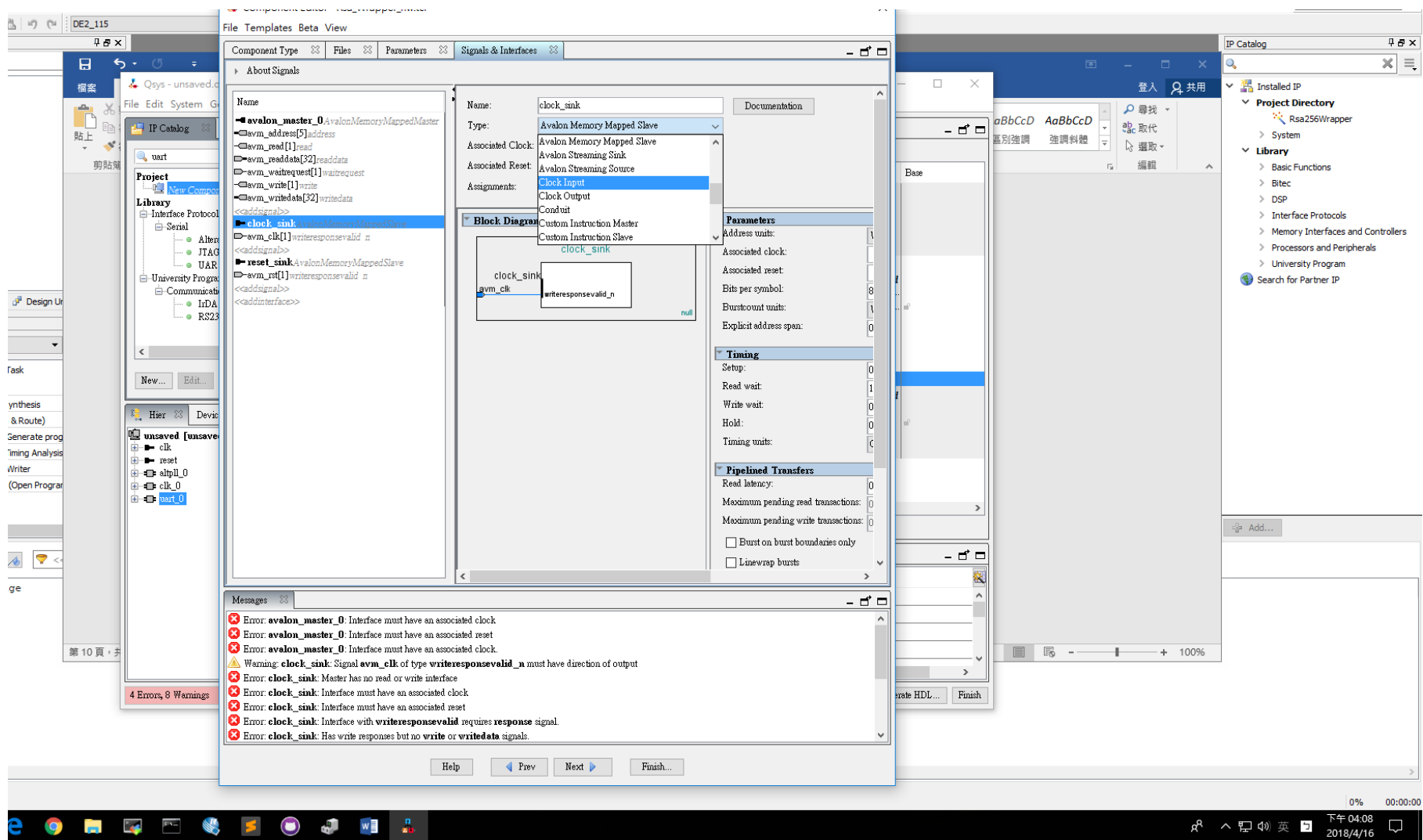
雙擊 Add interface → clock_sink
雙擊 Add interface → reset_sink



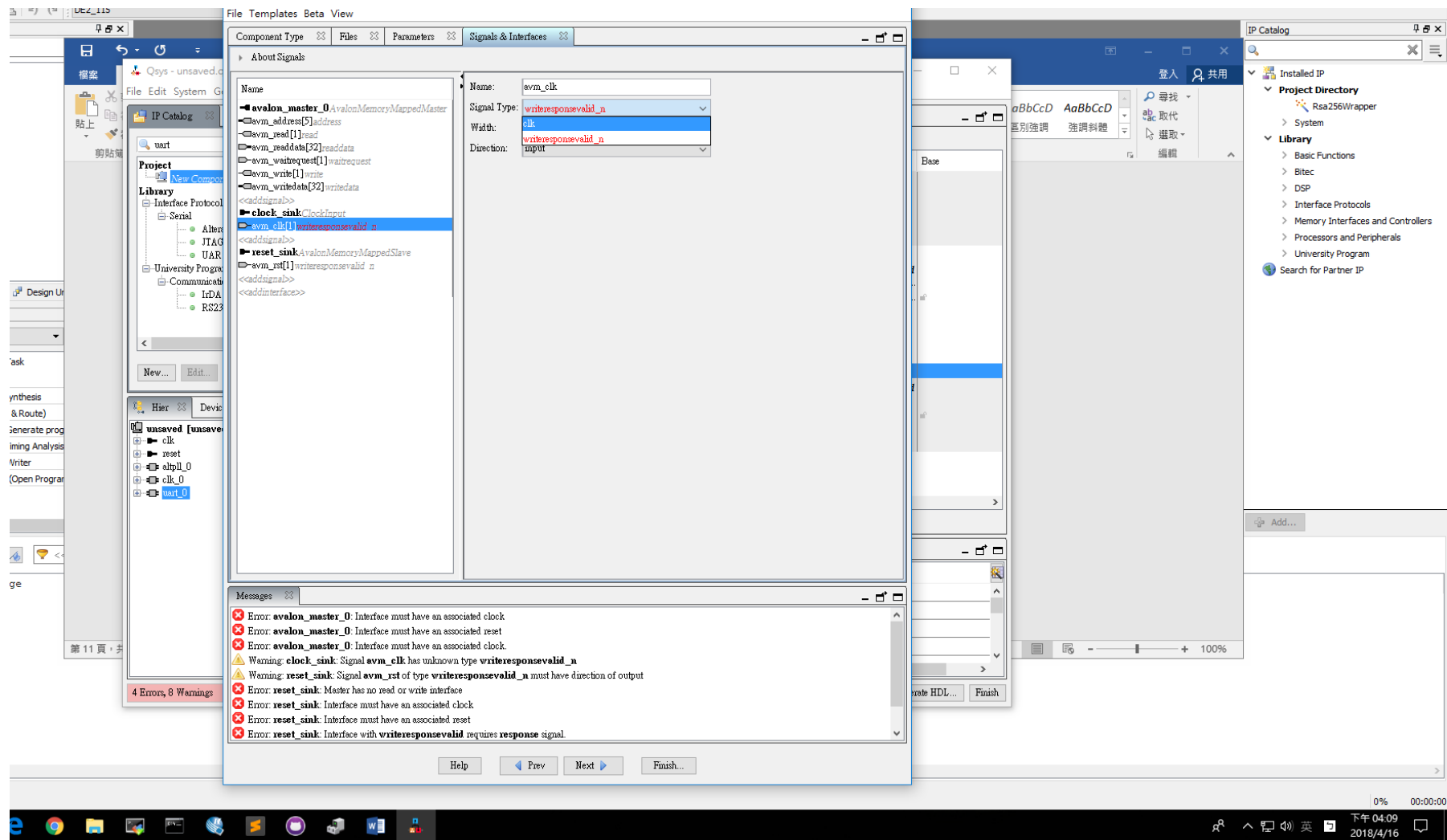
avm_clk 拖曳至 clock_sink 下方
avm_rst 拖曳至 reset_sink 下方



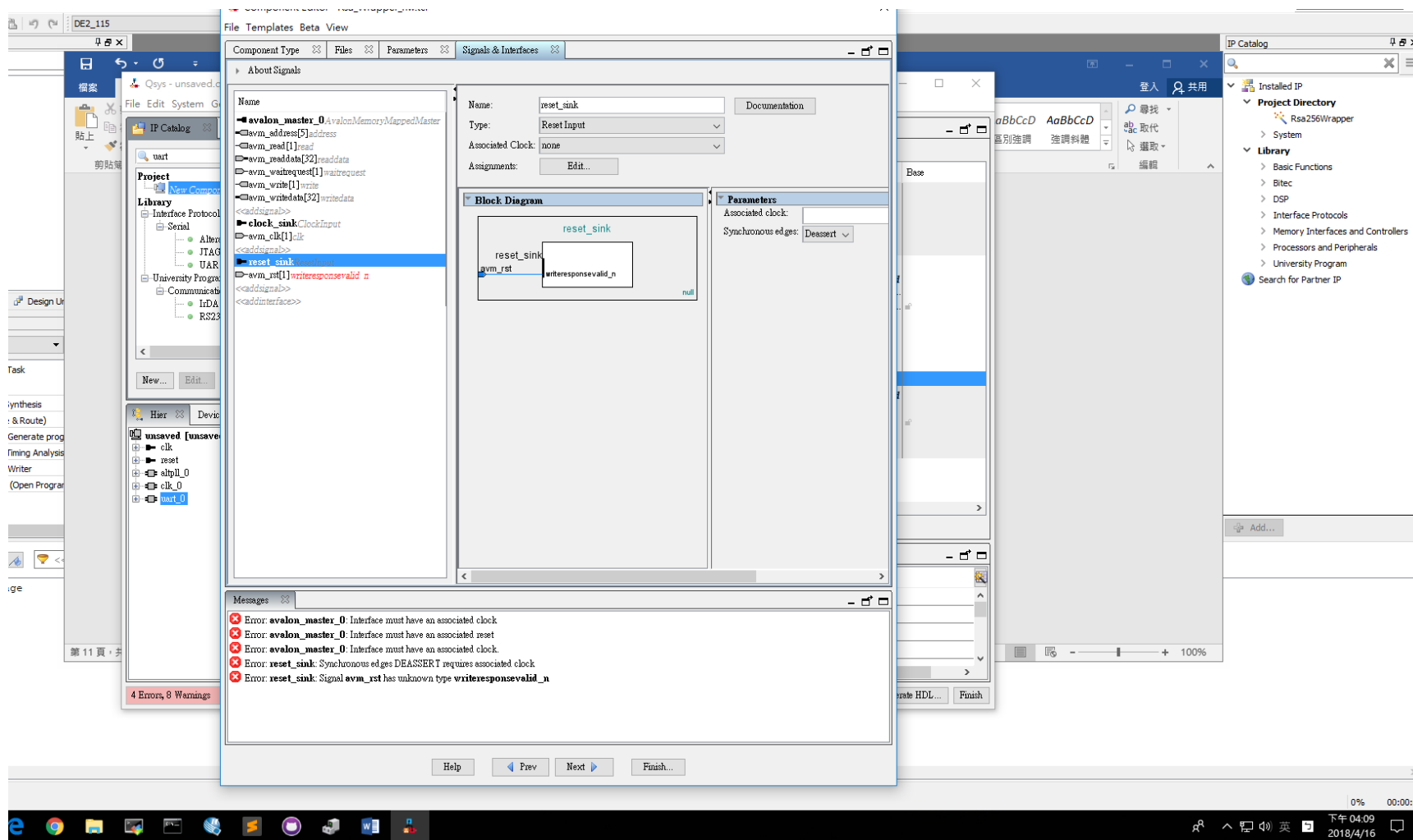
將 clock_sink 的 Type 改成 Clock Input



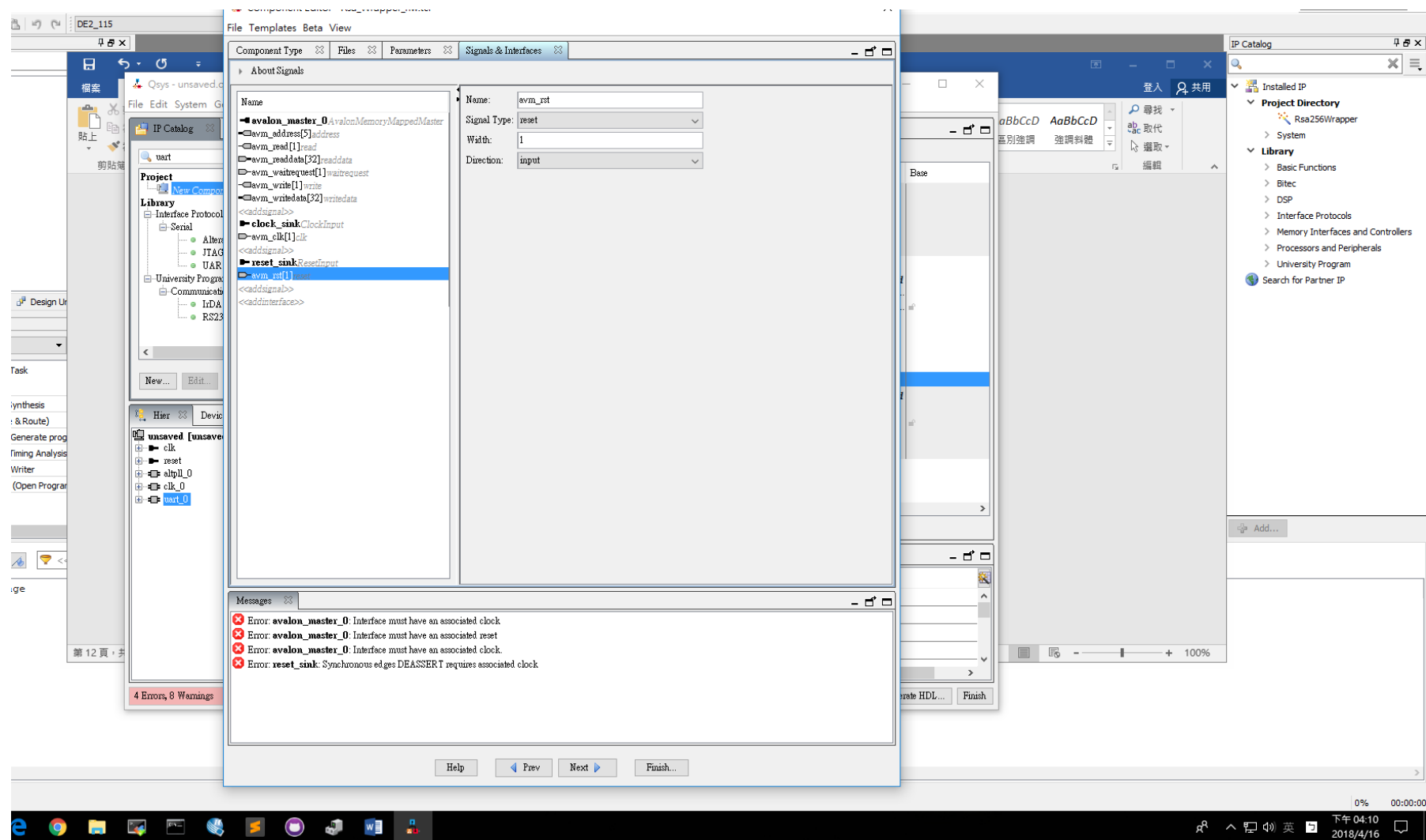
將 avm_clk 的 Signal Type 改成 clk



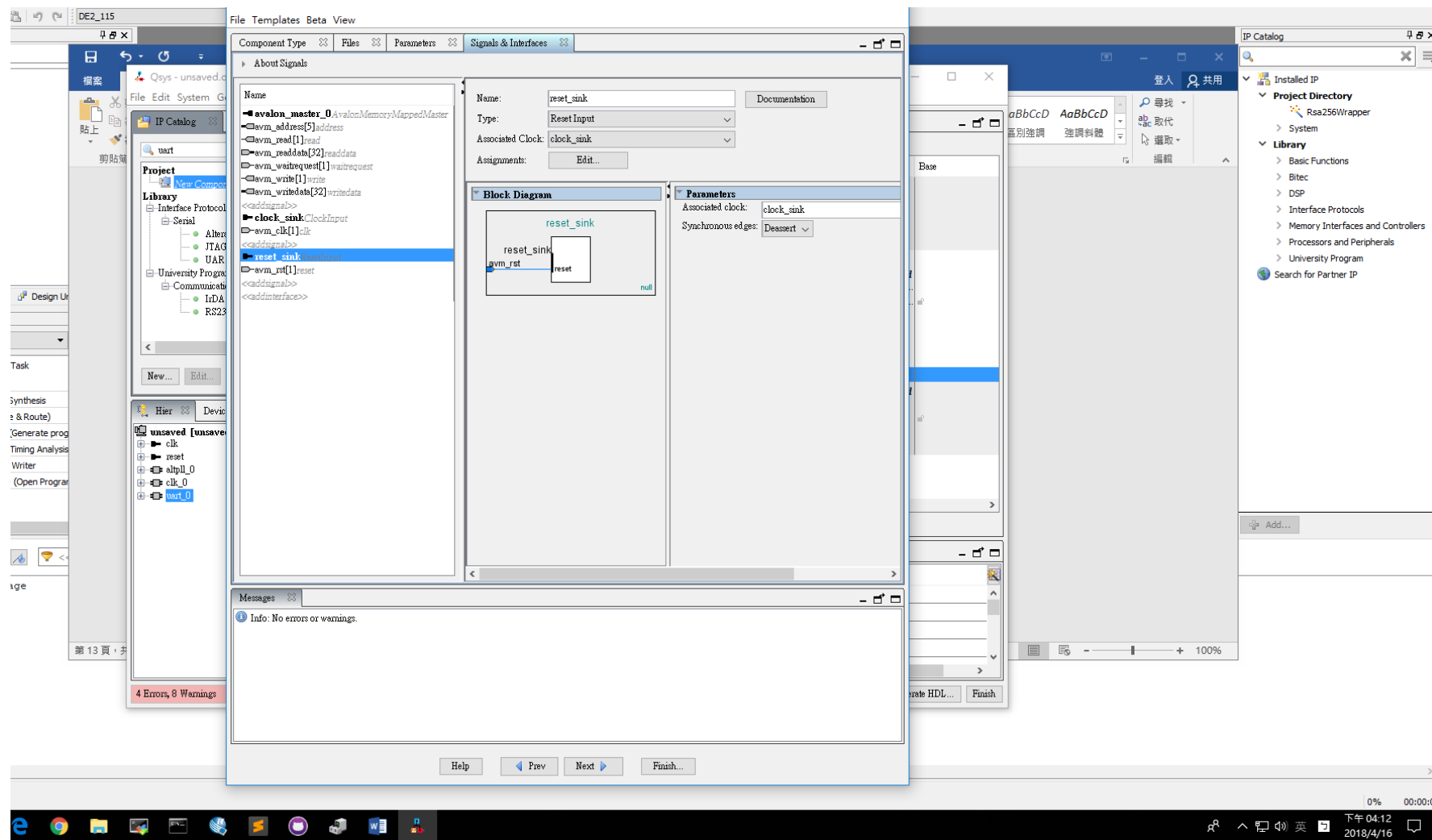
將 reset_sink 的 Type 改成 Reset Input



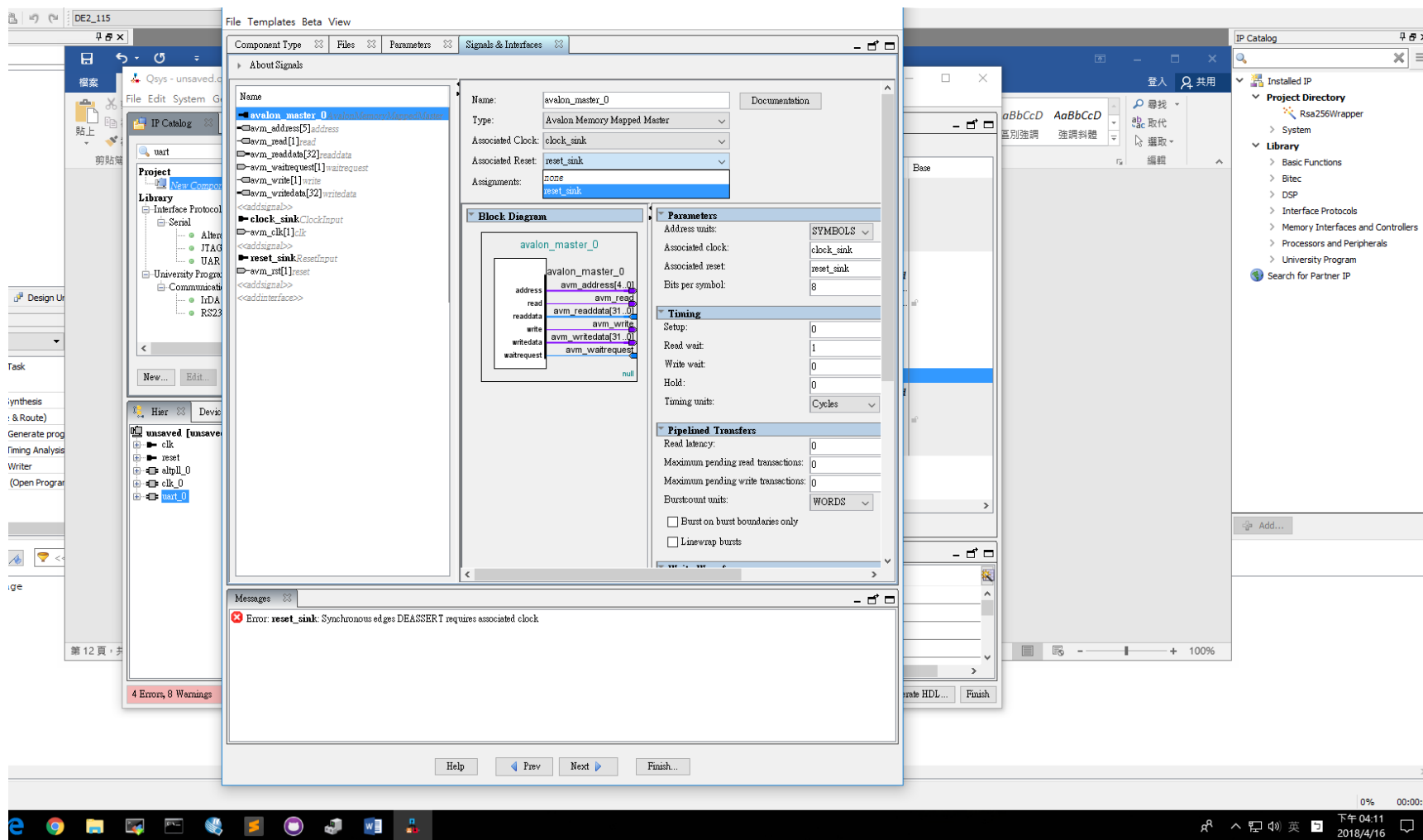
將 avm_rst 的 Signal Type 改成 reset



將 reset_sink 的 associate clock 改成 clock_sink



將 avalon_master_0 的 associate clock 改成 clock_sink
將 avalon_master_0 的 associate reset 改成 reset_sink



Finish → Yes, save
將搜尋列字串清空可見 SW_Wrapper 在 New Component 底下

Qsys - sw_qsys.qsys (C:\Users\dclab\Desktop\DCLab_SW\test_v1\sw_qsys.qsys)

File Edit System Generate View Tools Help

IP Catalog

Project

- New Component
- SW Wrapper
- System

Library

- Basic Functions
- Bitec
- DSP
- Interface Protocols
- Low Power
- Memory Interfaces and Controllers
- Processors and Peripherals
- Qsys Interconnect
- University Program

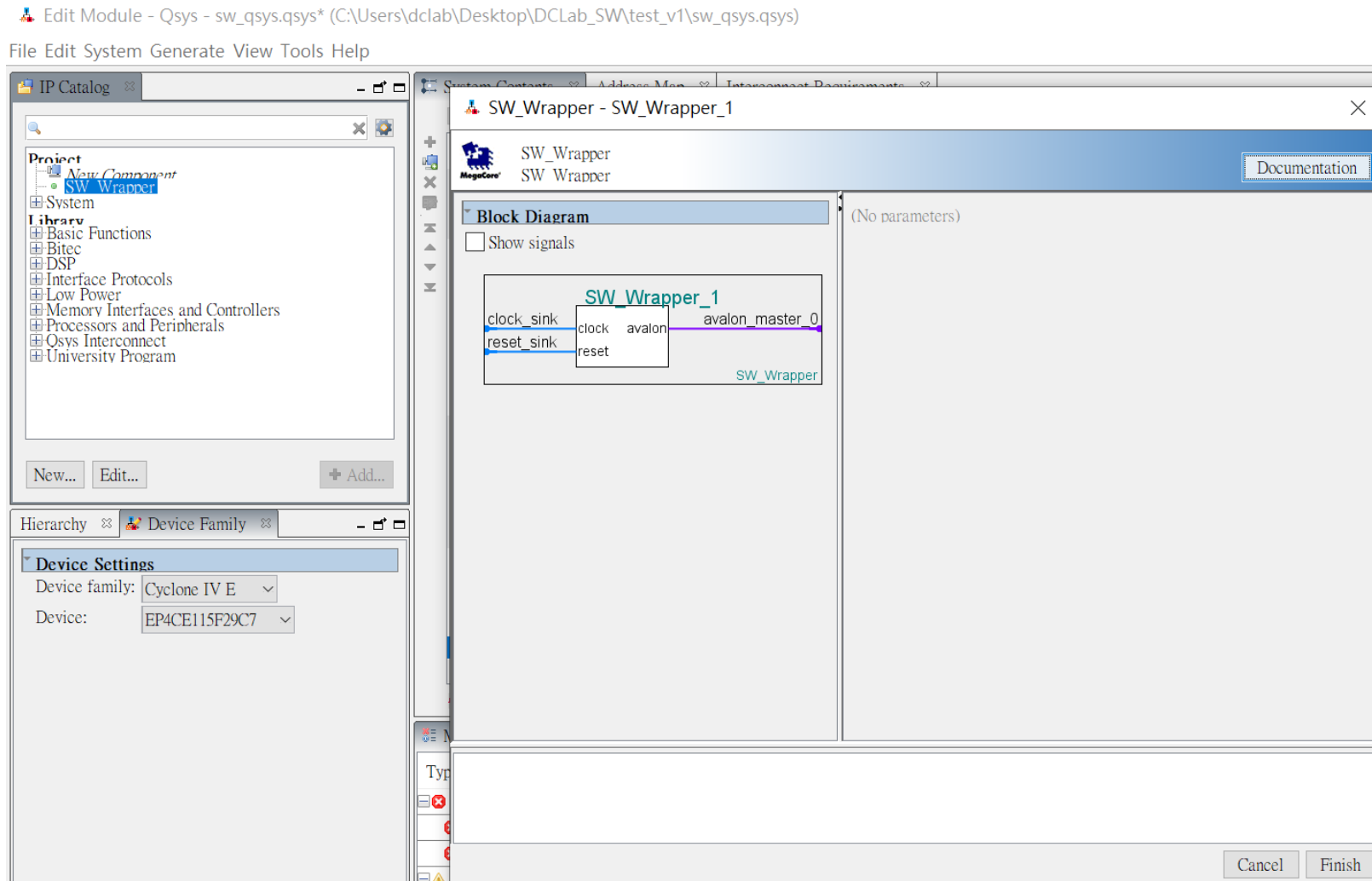
New... Edit... + Add...

System Contents Address Map Interconnect Requirements

System: sw_qsys Path: clk_0

Use	Connections	Name	Description	Export
<input checked="" type="checkbox"/>		clk_0	Clock Source	
		clk_in	Clock Input	clk
		clk_in_reset	Reset Input	reset
		clk	Clock Output	Double-click to
		clk_reset	Reset Output	Double-click to
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL	
		inclk_interface	Clock Input	Double-click to
		inclk_interface_reset	Reset Input	Double-click to
		pll_slave	Avalon Memory Mapped ...	Double-click to
		c0	Clock Output	Double-click to
		areset_conduit	Conduit	Double-click to
		locked_conduit	Conduit	Double-click to
		phasedone_conduit	Conduit	Double-click to
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)	
		clk	Clock Input	Double-click to

雙擊 SW_Wrapper → Finish



請照圖例接線 (下面 Message 內紅字會不見)

Qsys - sw_qsys.qsys* (C:\Users\dclab\Desktop\DCLab_SW\test_v1\sw_qsys.qsys)

File Edit System Generate View Tools Help

IP Catalog

Project: New Component, SW Wrapper

Library: Basic Functions, Biterc, DSP, Interface Protocols, Low Power, Memory Interfaces and Controllers, Processors and Peripherals, Qsys Interconnect, University Program

Hierarchy: Device Family: Cyclone IV E, Device: EP4CE115F29C7

Device Settings

System Contents

System: sw_qsys Path: uart_0

Use	Connections	Name	Description	Export	Clock	Base	End	I...	Tags	Opcode Name
<input checked="" type="checkbox"/>		clk_0	Clock Source	clk						
		clk_in	Clock Input							
		clk_in_reset	Reset Input							
		clk	Clock Output							
		clk_reset	Reset Output							
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL							
		inclk_interface	Clock Input							
		inclk_interface_reset	Reset Input							
		pll_slave	Avalon Memory Mapped ...							
		c0	Clock Output							
		areset_conduit	Conduit							
		locked_conduit	Conduit							
		phasedone_conduit	Conduit							
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)							
		clk	Clock Input							
		reset	Reset Input							
		s1	Avalon Memory Mapped ...							
		external_connection	Conduit							
		irq	Interrupt Sender							
<input checked="" type="checkbox"/>		SW_Wrapper_0	SW_Wrapper							
		avalon_master_0	Avalon Memory Mapped ...							
		clock_sink	Clock Input							
		reset_sink	Reset Input							

Current filter: All Interfaces

Messages

Type	Path	Message
5 Warnings		
Warning	sw_qsys.altpll_0	altpll_0.areset_conduit must be exported, or connected to a matching conduit.
Warning	sw_qsys.altpll_0	altpll_0.locked_conduit must be exported, or connected to a matching conduit.

0 Errors, 5 Warnings

Generate HDL... Finish

雙擊 external_connection 的 Export 欄位, Enter

Qsys - sw_qsys.qsys* (C:\Users\dclab\Desktop\DCLab_SW\test_v1\sw_qsys.qsys)

File Edit System Generate View Tools Help

IP Catalog

Project: New Component, SW Wrapper, System

Library: Basic Functions, Biterc, DSP, Interface Protocols, Low Power, Memory Interfaces and Controllers, Processors and Peripherals, Qsys Interconnect, University Program

Hierarchy: Device Family: Cyclone IV E, Device: EP4CE115F29C7

Device Settings

System Contents

System: sw_qsys Path: uart_0

Use	Connections	Name	Description	Export	Clock	Base	End	I...	Tags	Opcode Name
<input checked="" type="checkbox"/>		clk_0	Clock Source	clk	exported					
<input checked="" type="checkbox"/>		clk_in	Clock Input	reset						
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input	Double-click to						
<input checked="" type="checkbox"/>		clk	Clock Output	Double-click to	clk_0					
<input checked="" type="checkbox"/>		clk_reset	Reset Output	Double-click to						
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL	Double-click to						
<input checked="" type="checkbox"/>		inclk_interface	Clock Input	Double-click to	clk_0					
<input checked="" type="checkbox"/>		inclk_interface_reset	Reset Input	Double-click to	[inclk_i...					
<input checked="" type="checkbox"/>		pll_slave	Avalon Memory Mapped ...	Double-click to	[inclk_i...					
<input checked="" type="checkbox"/>		c0	Clock Output	Double-click to	altpll_0...					
<input checked="" type="checkbox"/>		areset_conduit	Conduit	Double-click to						
<input checked="" type="checkbox"/>		locked_conduit	Conduit	Double-click to						
<input checked="" type="checkbox"/>		phasedone_conduit	Conduit	Double-click to						
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)	Double-click to						
<input checked="" type="checkbox"/>		clk	Clock Input	Double-click to	altpll_...					
<input checked="" type="checkbox"/>		reset	Reset Input	Double-click to	[clk]					
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped ...	Double-click to	[clk]	0x0000	0x001f			
<input checked="" type="checkbox"/>		external_connection	Conduit	uart_0_external_...	[clk]					
<input checked="" type="checkbox"/>		irq	Interrupt Sender	Double-click to						
<input checked="" type="checkbox"/>		SW_Wrapper_0	SW_Wrapper	Double-click to						
<input checked="" type="checkbox"/>		avalon_master_0	Avalon Memory Mapped ...	Double-click to	[clock_s...					
<input checked="" type="checkbox"/>		clock_sink	Clock Input	Double-click to	altpll_...					
<input checked="" type="checkbox"/>		reset_sink	Reset Input	Double-click to	[clock_s...					

Current filter: All Interfaces

Messages

Type	Path	Message
5 Warnings		
Warning	sw_qsys.altpll_0	altpll_0.areset_conduit must be exported, or connected to a matching conduit.
Warning	sw_qsys.altpll_0	altpll_0.locked_conduit must be exported, or connected to a matching conduit.

0 Errors, 5 Warnings

Generate HDL... Finish

點 s1 的 base 欄位 → s1 被反白選取 System → Assign Base

Qsys - sw_qsys.qsys* (C:\Users\dclab\Desktop\DCLab_SW\test_v1\sw_qsys.qsys)

File Edit System Generate View Tools Help

The screenshot displays the Qsys software interface. The 'System Contents' pane shows a list of components and their connections. The 'uart_0' component is selected, and its 'Base' field is highlighted with a red box, showing the values '0x0000' and '0x001f'. The 'Messages' pane at the bottom shows 5 warnings.

Use	Connections	Name	Description	Export	Clock	Base	End	I...	Tags	Opcode Name
<input checked="" type="checkbox"/>		clk_0	Clock Source	clk	<i>exported</i>					
		clk_in	Clock Input							
		clk_in_reset	Reset Input	reset						
		clk	Clock Output	<i>Double-click to</i>	clk_0					
		clk_reset	Reset Output	<i>Double-click to</i>						
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL							
		inclk_interface	Clock Input	<i>Double-click to</i>	clk_0					
		inclk_interface_reset	Reset Input	<i>Double-click to</i>	[inclk_i...					
		pll_slave	Avalon Memory Mapped ...	<i>Double-click to</i>	[inclk_i...					
		c0	Clock Output	<i>Double-click to</i>	altpll_0...					
		areset_conduit	Conduit	<i>Double-click to</i>						
		locked_conduit	Conduit	<i>Double-click to</i>						
		phasedone_conduit	Conduit	<i>Double-click to</i>						
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)							
		clk	Clock Input	<i>Double-click to</i>	altpll_...					
		reset	Reset Input	<i>Double-click to</i>	[clk]					
		s1	Avalon Memory Mapped ...	<i>Double-click to</i>	[clk]	0x0000	0x001f			
		external_connection	Conduit	<i>Double-click to</i>	uart_0_external_...					
		irq	Interrupt Sender	<i>Double-click to</i>	[clk]					
<input checked="" type="checkbox"/>		SW_Wrapper_0	SW_Wrapper							
		avalon_master_0	Avalon Memory Mapped ...	<i>Double-click to</i>	[clock_s...					
		clock_sink	Clock Input	<i>Double-click to</i>	altpll_...					
		reset_sink	Reset Input	<i>Double-click to</i>	[clock_s...					

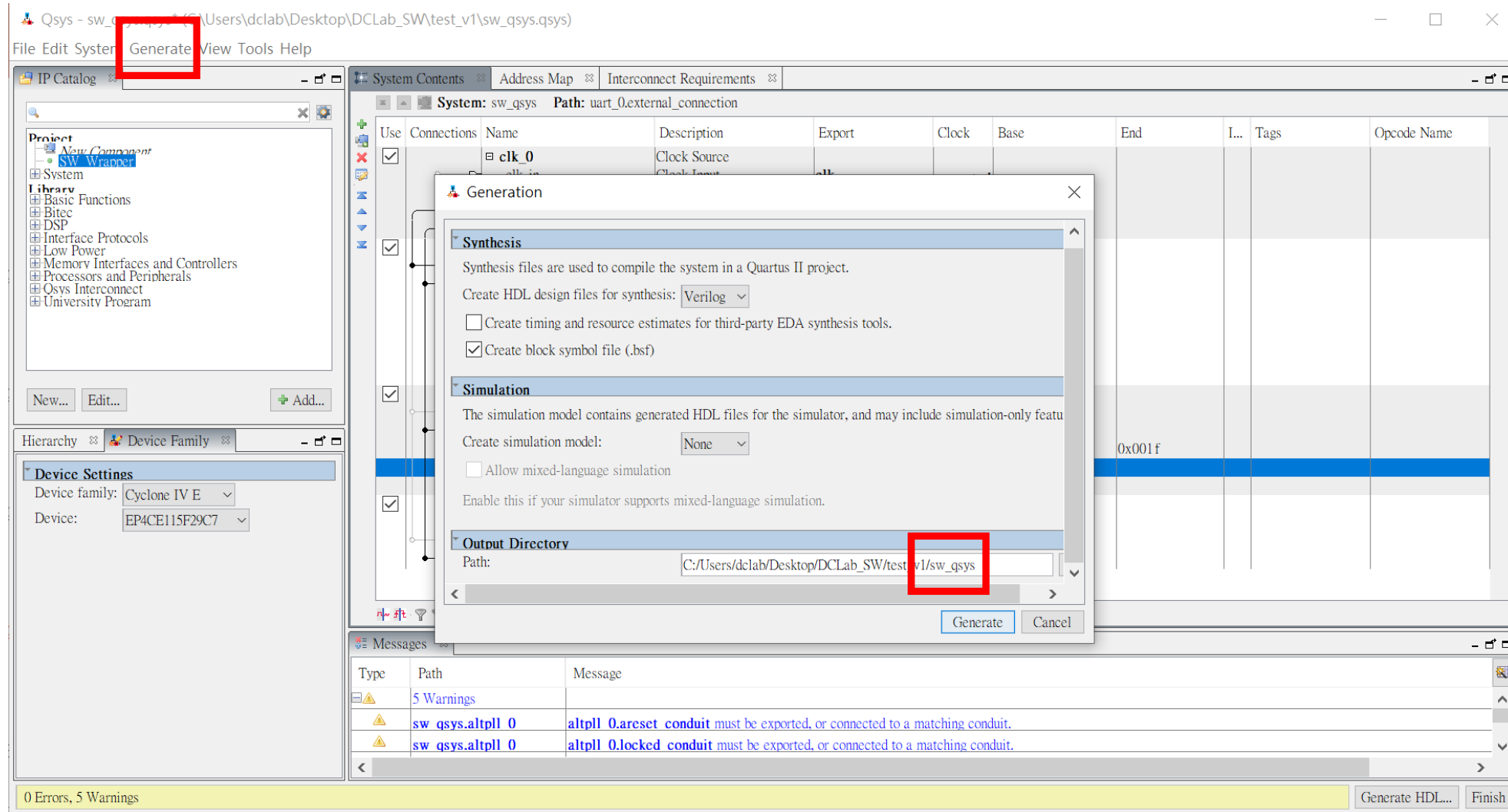
Current filter: All Interfaces

Type	Path	Message
5 Warnings		
Warning	sw_qsys.altpll_0	altpll_0.areset_conduit must be exported, or connected to a matching conduit.
Warning	sw_qsys.altpll_0	altpll_0.locked_conduit must be exported, or connected to a matching conduit.

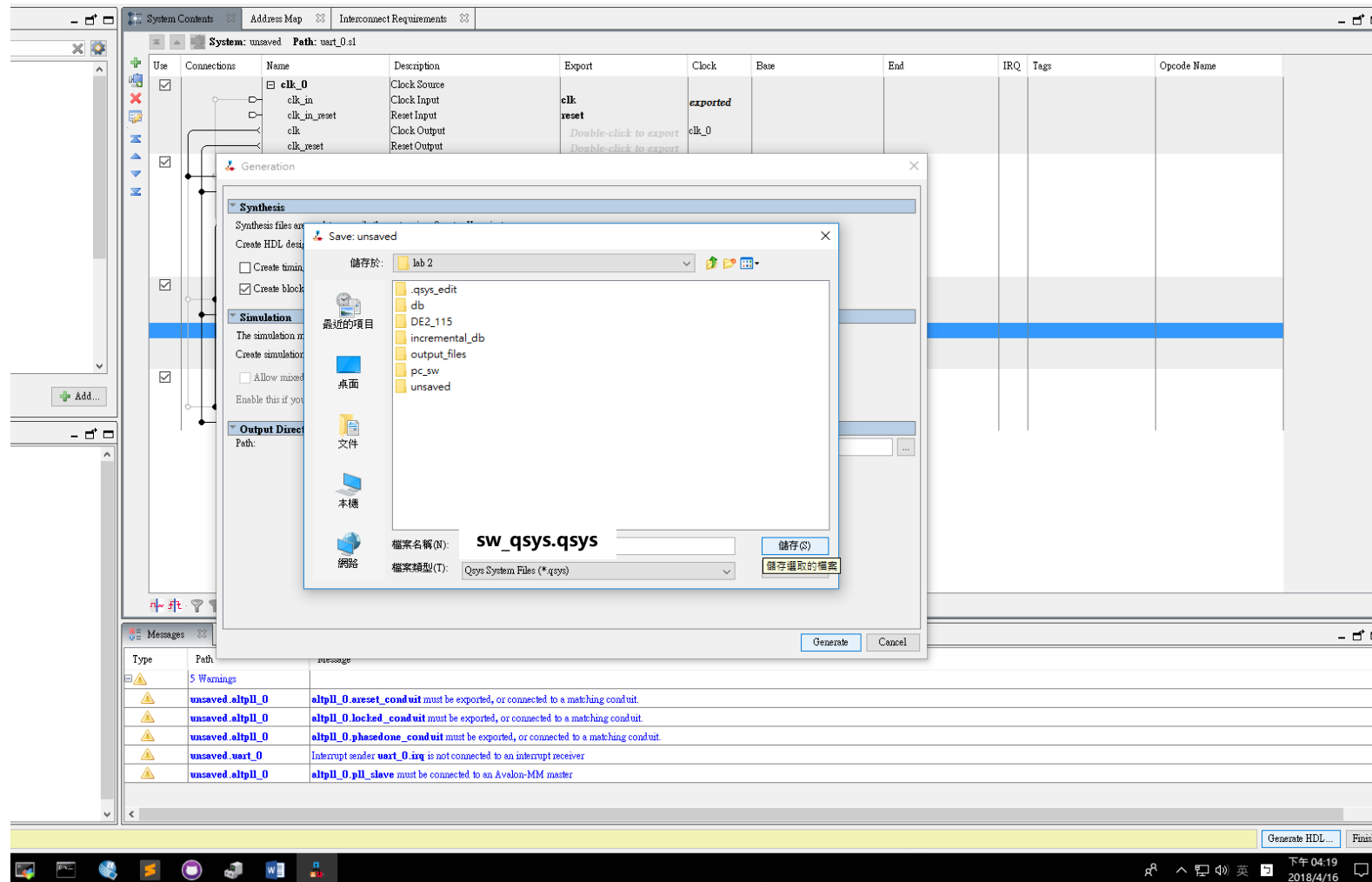
0 Errors, 5 Warnings

Generate HDL... Finish

Generate → Generate... → 將 Output Directory 的最後一層改成 sw_qsys



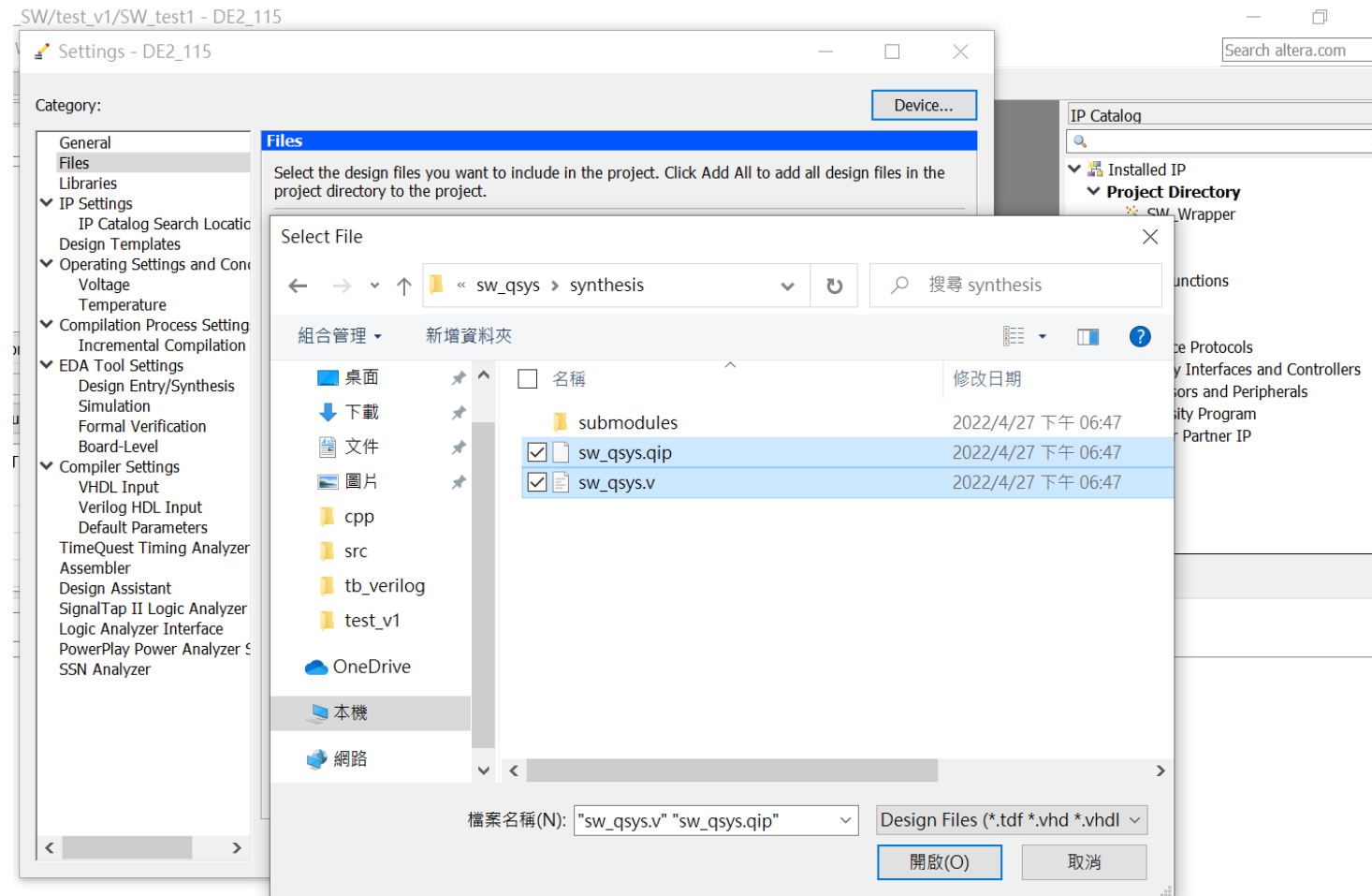
Generate → Save
檔案名稱改成 sw_qsys.qsys, 儲存, 完畢後按 Close



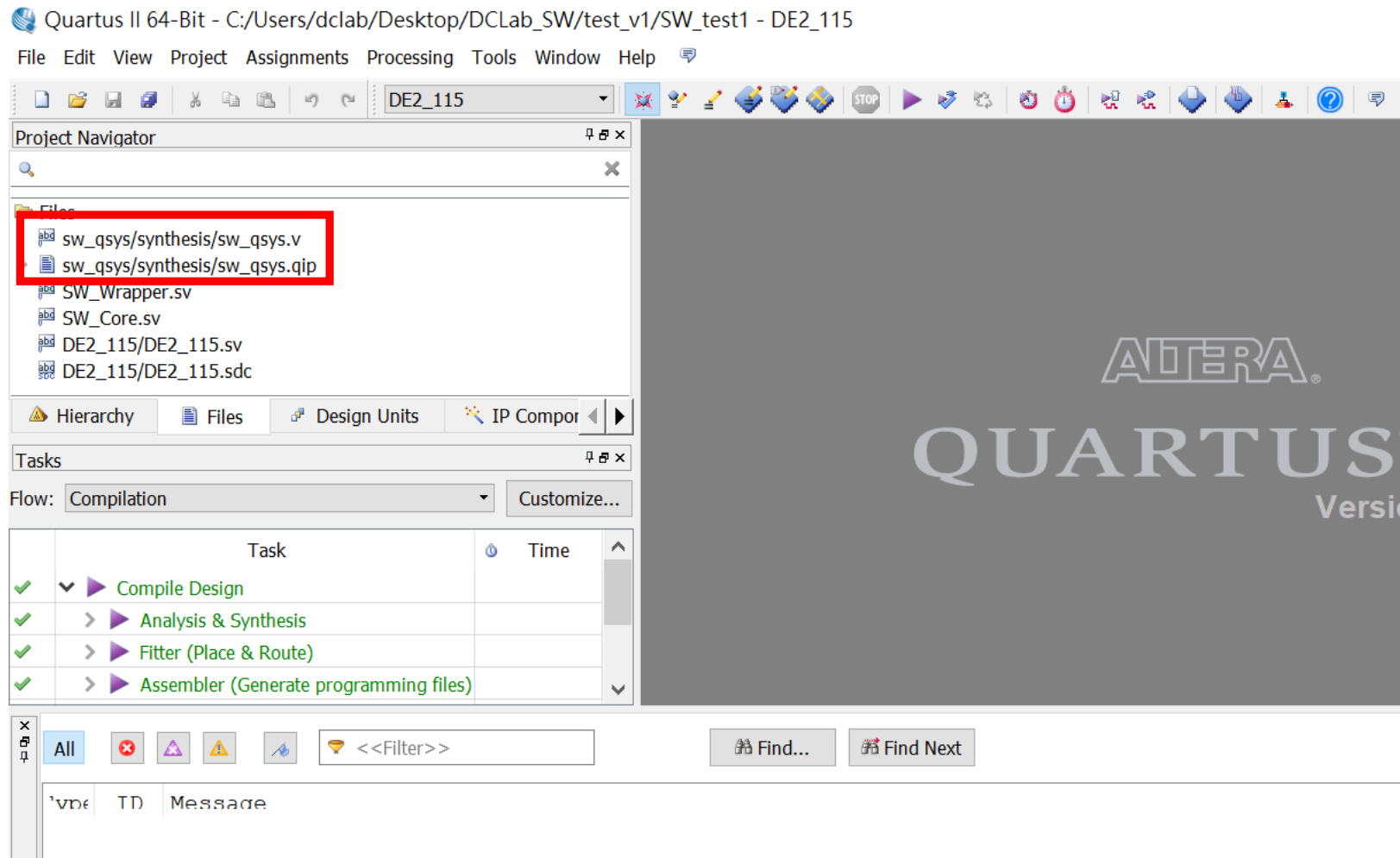
回到 Quartus 視窗 → Assignment → Settings



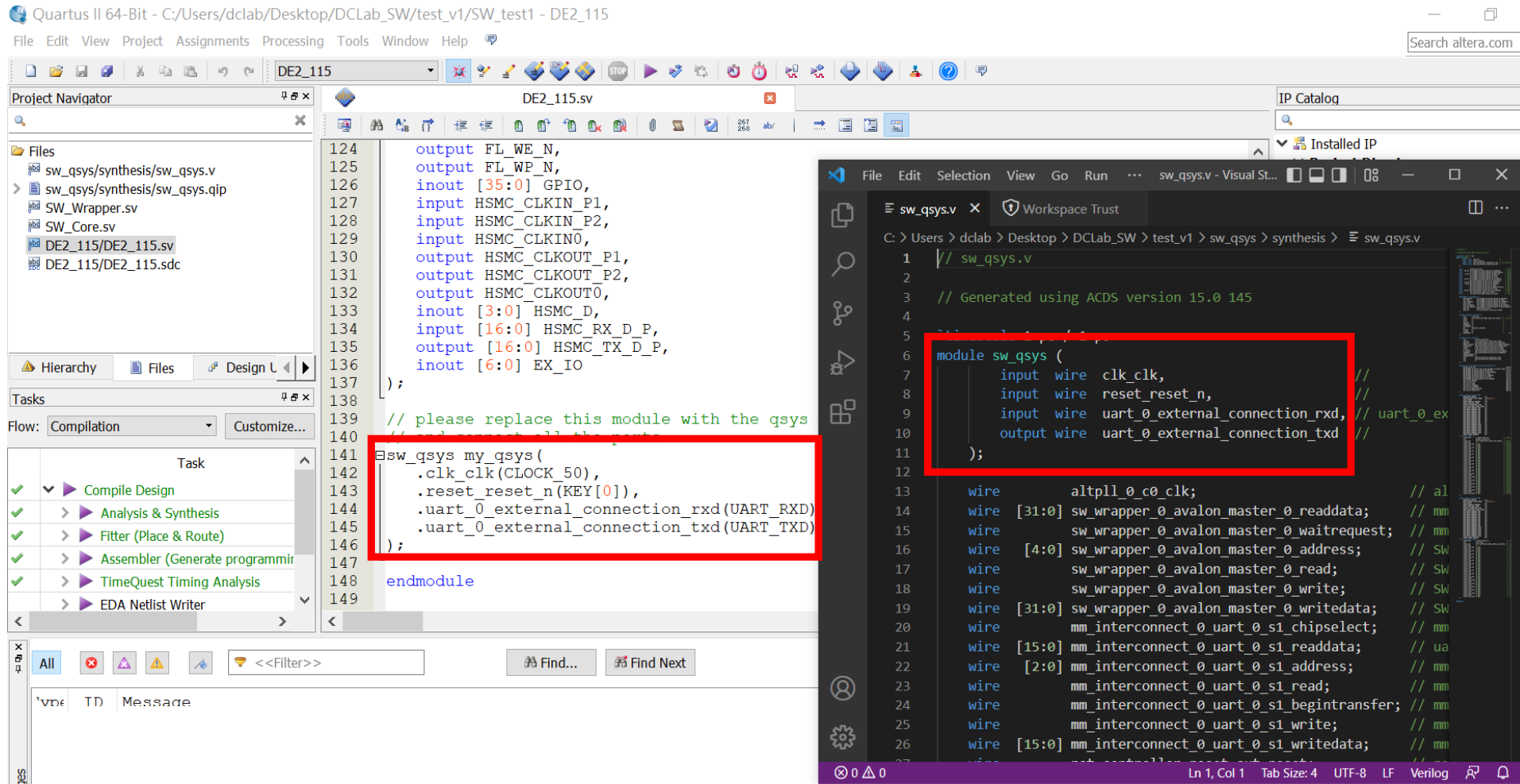
新增 sw_qsys/synethesis 內的 sw_qsys.qip 和
sw_qsys.v → Apply → OK



完成後可以見到 Files 內多出 sw_qsys.v 和 sw_qsys.qip

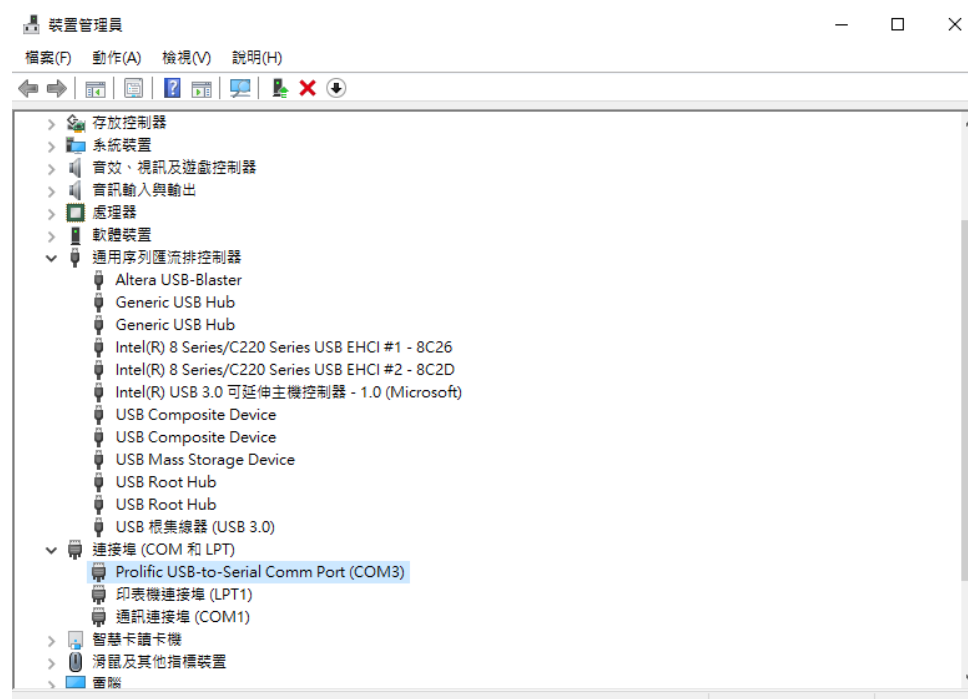


檢查 DE2_115.sv 內使用 sw_qsys 和 sw_qsys.v port 相同




Appendix: Compile (Windows)

1. 裝置管理員→連接埠 (COM和LPT)→Prolific USB-to-Serial Common Port (COM?)
 - 1) 若沒有發現類似的裝置，則需要安裝對應型號的驅動程式
 - 2) COM?即為OS指派的port代號



Appendix: Compile (Windows)

2. 按下FPGA上的KEY[0] (做reset)
3. `$> python test_rs232.py COM?`, ?從步驟1.可以得知



```
命令提示字元
Microsoft Windows [版本 10.0.19044.1645]
(c) Microsoft Corporation. 著作權所有，並保留一切權利。
C:\Users\dclab>cd C:\Users\dclab\Desktop\DCLab_SW\test_v1\pc_python
C:\Users\dclab\Desktop\DCLab_SW\test_v1\pc_python>python test_rs232.py COM3
```

Appendix: Compile (Windows)

4. 若要測試不同的testing data檔，則將 test_rs232.py 內的 fp_pat = open() 以及 fp_gold = open() 的檔案路徑改成新生成的檔案路徑
5. 執行後，會顯示有無通過所有測資
6. 經驗法則
 - 1) Compile時間過短或使用的logic elements數量過少，就算compile successful也可能出錯
 - 2) 重新 qsys 的話，可以將 qsys 這個資料夾砍掉直接重來
 - 3) Critical warning: Timing requirement not met代表 qsys 無法滿足timing的要求。有時候可能導致每一次compile的結果不盡相同