DSD HW2 B09901081 施伯儒

1. Cycle: 3.8ns

2. Area:

```
Number of ports:                          836
Number of nets:                          6891
Number of cells:                         6204
Number of combinational cells:           5164
Number of sequential cells:              1024
Number of macros/black boxes:               0
Number of buf/inv:                        982
Number of references:                     131

Combinational area:                59594.016076
Buf/Inv area:                       9695.548827
Noncombinational area:             29974.387074
Macro/Black Box area:                  0.000000
Net Interconnect area:            740043.746429

Total cell area:                   89568.403150
Total area:                       829612.149579
```

3. AT: 89568.403150*3.8 = 340359.932

4. No latch:

```
Inferred memory devices in process
        in routine CHIP line 168 in file
                '/home/raid7_2/userb09/b09081/NTUEE_DSD/DSD_HW2/verilog/CHIP.v'.
===========================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================================
|     addr_r_reg      | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===========================================================================================
Warning:  /home/raid7_2/userb09/b09081/NTUEE_DSD/DSD_HW2/verilog/CHIP.v:202: sign
rs. (VER-318)

Inferred memory devices in process
        in routine reg_file line 205 in file
                '/home/raid7_2/userb09/b09081/NTUEE_DSD/DSD_HW2/verilog/CHIP.v'.
===========================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================================
|       mem_reg       | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
===========================================================================================
Statistics for MUX_OPs
=======================================================
| block name/line  | Inputs | Outputs | # sel inputs |
=======================================================
|   reg_file/197   |   32   |   32    |      5       |
|   reg_file/198   |   32   |   32    |      5       |
-------------------------------------------------------
```

```
Inferred memory devices in process
        in routine CHIP line 168 in file
                '/home/raid7_2/userb09/b09081/NTUEE_DSD/DSD_HW2/verilog/CHIP.v'.
===========================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================================
|     addr_r_reg      | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===========================================================================================
```