

#### **DSD** Exercise

## **Gauss-Seidel Iteration Machine**

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## **Background**

- Large linear system of equations is required to be solved in many engineering simulations and scientific computing applications
- Several iterative methods is used to accelerate the computing due to their simplicity, such as Jacobi method, Gauss-Seidel iteration model (GSIM), Conjugate gradient...

$$\begin{bmatrix} a_{11} & \cdots & a_{1N} \\ \vdots & \ddots & \vdots \\ a_{N1} & \cdots & a_{NN} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_N \end{bmatrix} = \begin{bmatrix} b_1 \\ \vdots \\ b_N \end{bmatrix}$$

$$\vdots$$

$$a_{11}x_1 + a_{12}x_2 + \cdots + a_{1N}x_N = b_1$$

$$\vdots$$

$$a_{21}x_1 + a_{22}x_2 + \cdots + a_{2N}x_N = b_2$$

$$\vdots$$

$$a_{N1}x_1 + a_{N2}x_2 + \cdots + a_{NN}x_N = b_N$$

Expand eq (1)



# Gauss-Seidel Iteration Model (GSIM)

Iterative method to solve a linear system of equations

$$x_3^0 \text{: initial value of } x_3 \\ x_1^1 = \frac{1}{a_{11}} (b_1 - a_{12} x_2^0 - \dots - a_{1N} x_N^0) \\ a_{21} x_1 + a_{22} x_2 + \dots + a_{2N} x_N = b_2 \\ \vdots \\ a_{N1} x_1 + a_{N2} x_2 + \dots + a_{NN} x_N = b_N$$
 
$$x_1^1 = \frac{1}{a_{11}} (b_1 - a_{12} x_2^0 - \dots - a_{1N} x_N^0) \\ x_2^1 \text{: first iteration result of } x_2 \\ x_2^2 \text{: first iteration result of } x_2 \\ x_2^2 \text{: first iteration result of } x_2 \\ x_2^2 \text{: first it$$

Change the order

Final equation



## **Project Problem**

- Given a fixed matrix A
- Input Different matrix b
- After k iterations (define by yourself!), output final results x

At most 7 non-zero terms one time

#### By the previous equation:

$$\begin{split} x_1^1 &= \frac{1}{20} [b_1 + 13 \left( x_2^0 + 0 \right) - 6 \left( x_3^0 + 0 \right) + \left( x_4^0 + 0 \right) ] \\ x_2^1 &= \frac{1}{20} [b_2 + 13 \left( x_3^0 + x_1^1 \right) - 6 \left( x_4^0 + 0 \right) + \left( x_5^0 + 0 \right) ] \\ x_3^1 &= \frac{1}{20} [b_3 + 13 \left( x_4^0 + x_2^1 \right) - 6 \left( x_5^0 + x_1^1 \right) + \left( x_6^0 + 0 \right) ] \\ x_4^1 &= \frac{1}{20} [b_4 + 13 \left( x_5^0 + x_3^1 \right) - 6 \left( x_6^0 + x_2^1 \right) + \left( x_7^0 + x_1^1 \right) ] \\ &\vdots \\ x_{16}^1 &= \frac{1}{20} [b_{16} + 13 \left( 0 + x_{15}^1 \right) - 6 \left( 0 + x_{14}^1 \right) + \left( 0 + x_{13}^1 \right) ] \end{split}$$

Only divide 20



## **Score Criteria**

- ❖ 評分一: Error rate E<sup>2</sup>

A 級:		$E^2$	< 0.000001
B級:	$0.000001 \le$	$E^2$	< 0.000005
C級:	$0.000005 \le$	$E^2$	< 0.000010
D級:	$0.000010 \leq$	$E^2$	< 0.000050
E級:	$0.000050 \le$	$E^2$	< 0.000100
F級:	$0.000100 \le$	$E^2$	< 0.001000
G級:	$0.001000 \le$	$E^2$	< 0.005000
H級:	$0.005000 \le$	$E^2$	< 0.010000
I級:	$0.010000 \le$	$E^2$	< 0.100000
J級:	$0.100000 \le$	$E^2$	< 0.300000
K級:	$0.300000 \le$	$E^2$	

- ❖ 評分二:AT score
  - $AT = area \times total timing$
  - Area: synthesis cell area
  - Timing: total execution time (tb1+tb2+...+tb5)

```
Your Score Level: A

Congratulations! GSIM's Function Successfully!

PASS-----

Simulation complete via $finish(1) at time 3734500 PS + 0

/testfixture5.v:213 #(`CYCLE/2); $finish;
ncsim> exit
```

Combinational area: 3875.164193
Buf/Inv area: 434.534396
Noncombinational area: 1147.442383
Macro/Black Box area: 0.000000
Net Interconnect area: 48580.242432

 Total cell area:
 5022.606576

 Total area:
 53602.849008



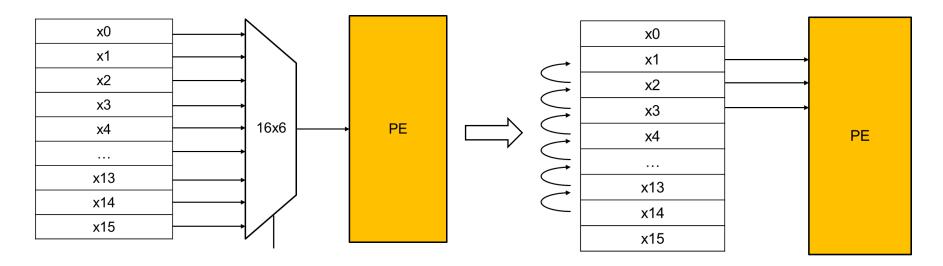
## **Design Guidelines**

- Architecture level
  - Data path scheduling
  - Parallel processing (unfolding)
  - Pipelining
- Computation unit level
  - Constant multiplier, constant divider
  - Decimal analysis



# **Architecture Level Optimization (1/3)**

- Reading data
  - ❖ Arbitrary reading: Using several MUXs to load data
  - Structural reading: Similar computation dataflow

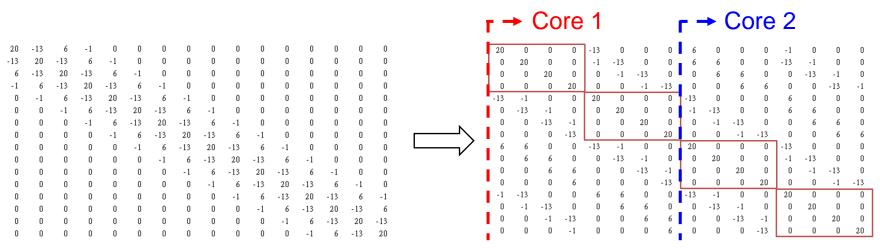


Scheduling by removing 6 MUXs



# **Architecture Level Optimization (2/3)**

- Parallel processing (unfolding)
  - Using multi-core to compute
  - Necessity: No data dependancy
- Reordering computation
  - ❖ Processing elements: 1, 5, 9, 13, ...

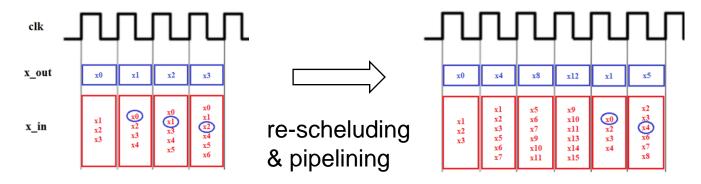


rescheduling

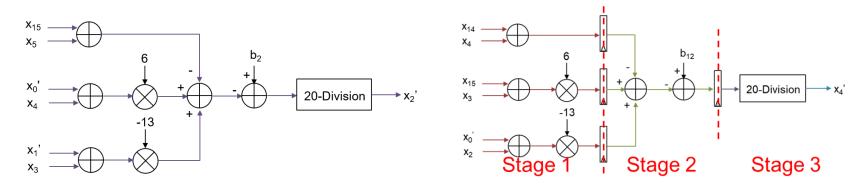


## **Architecture Level Optimization (3/3)**

- Pipelining
  - Divide computation into several cycles



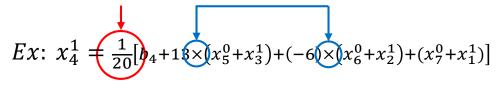
#### e.g. 3-stages pipeling





# **Computation Unit Level (1/2)**

#### 1 Division 2 Multiplication



# Computation flow $x_5^0$ $x_3^1$ $x_6^0$ $x_2^0$ $x_1^0$ Divider $x_7^0$ $x_1^1$ $x_1^0$ $x_2^0$ $x_2$

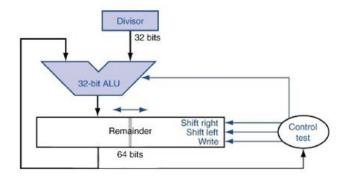
Division and multiplication is complicated.
It need large area and long computation time.





# **Computation Unit Level (2/2)**

- Multiplier
  - Power-of-two method (e.g.  $6 = 110_2$ ,  $13 = 1101_2$ )
- Divider
  - Conventional (for arbitrary input): requires 32 cycles
  - Constant divider: requires 3 cycles
    - Canonic Signed Digit (CSD) code
    - For each odd integer d, there exists an odd integer m such that  $d \times m = 2^n 1$



Need: 1 Adder, 1 shifter

Time: 32 cycles

$$\frac{1}{d} = \frac{m}{2^{n} - 1} = \frac{m}{2^{n} (1 - 2^{-n})}$$
$$= \frac{m}{2^{n}} (1 + 2^{-n}) (1 + 2^{-2n}) (1 + 2^{-4n}) \dots$$

Need: 1 Adder, 1 shifter

Time: 3 cycles



## Simulation & Synthesis

- Check "doc.pdf"
- 3 Major Things
  - RTL coding & Simulation
  - Synthesizable coding & Logic Synthesis
  - Gate-level simulation & Debugging/refinement
- Files needed for simulation
  - RTL code: GSIM.v
  - Gate-level code: GSIM \_syn.v,
  - Timing info (SDF file): GSIM \_syn.sdf,
  - Design library (DDC file): GSIM \_syn.ddc



## **Notice**

- Do not fit the given test pattern, there will be hidden cases!
- Latches are not allowed in gate level code after synthesis, use Flipflop instead.
- Negative Slack and Timing Violations are not allowed after synthesis.
- The tsmc13\_neg.v file is not allowed to be downloaded! Or you may offend the copyright protected by NTU & TSRI!



## **Grading Policy**

- \* RTL (40%): Function correctness, Rank A
- Synthesis (40%): Pass baseline AT score:  $1.0 \times 10^{10}$
- Ranking (15%): AT ranking
- Report (5%)
- For each team, you need to submit 4 files + 1 report
  - \* RTL code: GSIM.v
  - Synthesis:

GSIM\_syn.v,
GSIM\_syn.sdf,
GSIM\_syn.ddc

❖ Report: report.pdf



## Report

#### 1. Simulated cycle time (ns)

Gate-level simulation clock cycle (i.e. The cycle you passed testbench after synthesis)

#### 2. Area (um^2)

report\_area

#### 3. AT score

 $AT = area \times timing$ 

Area: total cell area

❖ Timing: total execution time (tb1 + tb2 + ... + tb5)

#### 4. Screenshot

Inferred memory devices in process (\*No latch should be inferred!) 

 Combinational area:
 3875.164193

 Buf/Inv area:
 434.534396

 Noncombinational area:
 1147.442383

 Macro/Black Box area:
 0.000000

 Net Interconnect area:
 48580.242432

Total cell area: 5022.606576
Total area: 53602.849008



### **Submission**

```
❖ DSD_Exercise_學號/
GSIM.v
GSIM_syn.v
GSIM_syn.sdf
GSIM_syn.ddc
report.pdf
```

- Compress all the files into one ZIP file
  - ❖ File name: DSD\_ Exercise \_學號.zip
  - ❖ EX: DSD\_ Exercise \_b09901001.zip
- Upload the file to NTUCOOL
- Deadline: 2023/05/01 23:59 XLate submission is not allowed