



# DSD HW3

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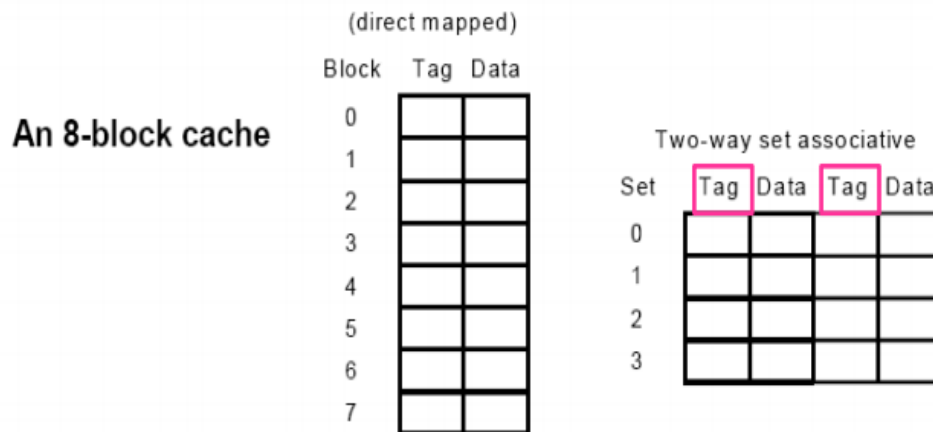
Speaker: Daniel

Date: 2023/05/02



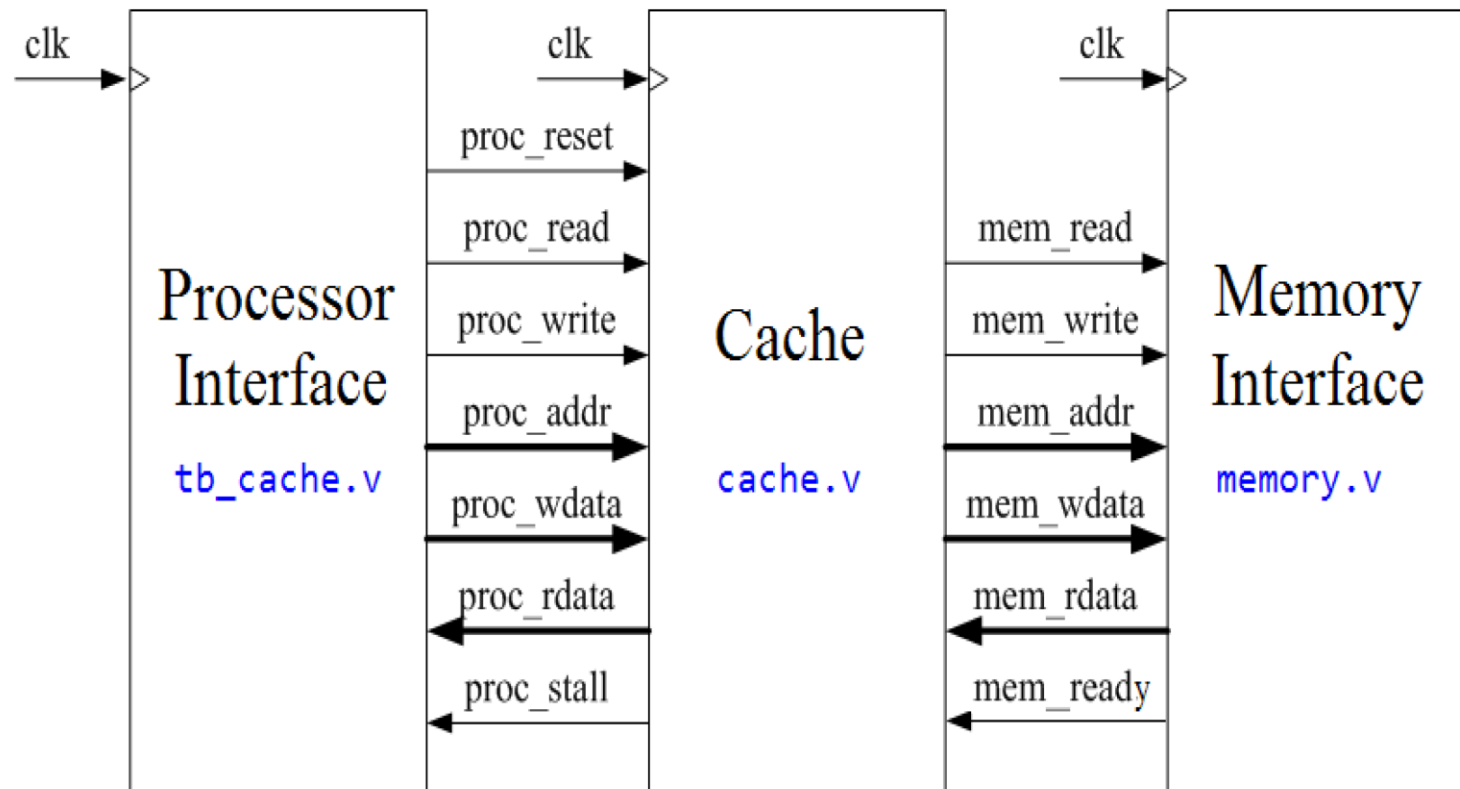
# Cache Specification

- ❖ Implement two architectures
  - ❖ Direct-mapped
  - ❖ Two-way associative
- ❖ 8 blocks with 4 words in each block
- ❖ Write-through & write back are both available write policies
- ❖ Least Recently Used (LRU) & Least Frequently Used (LFU) are both available placement policies





# I/O Interface of The Cache Unit





# I/O Specification of The Processor Interface

Name	I/O	Width	Description
clk	I	1	positive edge trigger clock
proc_reset	I	1	synchronous active-high reset signal
proc_read	I	1	synchronous active-high read enable signal
proc_write	I	1	synchronous active-high write enable signal
proc_addr	I	30	address bus ( <i>word address</i> )
proc_wdata	I	32	data bus for writing to cache
proc_rdata	O	32	data bus for reading from cache
proc_stall	O	1	active-high control signal that asks processor to wait (cache is busy)

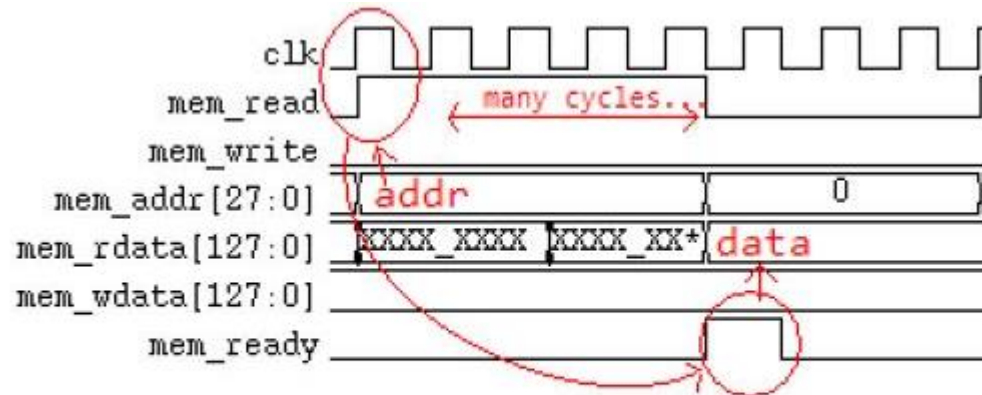


# I/O Specification of The Memory Interface

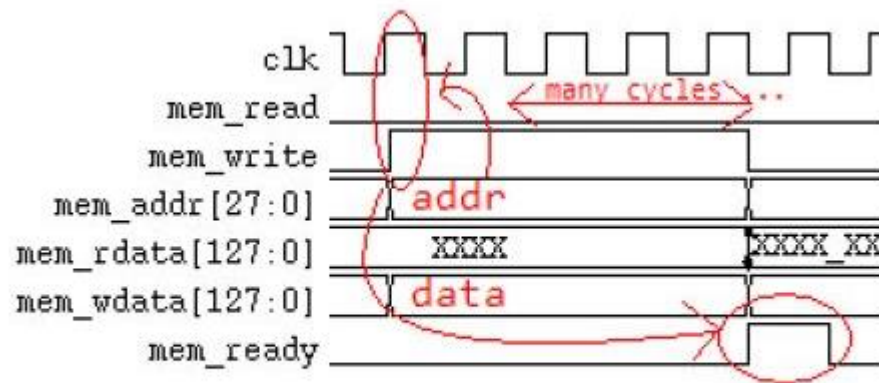
Name	I/O	Width	Description
mem_read	O	1	synchronous active-high read enable signal
mem_write	O	1	synchronous active-high write enable signal
mem_addr	O	28	address bus ( <i>4-word address</i> )
mem_wdata	O	128	data bus for writing to slow memory
mem_rdata	I	128	data bus for reading from slow memory
mem_ready	I	1	asynchronous active-high one-cycle signal that indicates data arrives from memory / data is done written to memory



# Timing Diagram of The Memory Interface



(a) Read operation.



(b) Write operation.



# Stall

- ❖ When the cache needs to access data from the memory and then wait for several cycles, the *proc\_stall* signal should be set high to stall the processor.
- ❖ Two possible cases where a stall is necessary
  - ❖ **Read miss** in both write-through and write-back caches
  - ❖ **Write hit** in only write through caches



# Cache Design (35% Each)

- ❖ **Evaluation is only based on the given testbench “tb\_cache.v”**
- ❖ **RTL Simulation (20%)**
- ❖ **Synthesis**
  - ❖ No latches
  - ❖ No negative endpoint slack
  - ❖ No timing violations
- ❖ **Gate-level Simulation (15%)**
  - ❖ 10% partial points if you pass the gate-level simulation with timing violations or negative endpoint slacks
  - ❖ Still need to pass the RTL simulation and no inferred latches
- ❖ **Performance is not part of the grading criteria**
  - ❖ Specify your cycle time in the report
  - ❖ Still encouraged to optimize it for your final project





## Bonus (Up to 10%)

- ❖ If your cache units are implemented with other skills that enhance the performance significantly
- ❖ Describe your methods or architectures in detail in the report
- ❖ Regulations
  - ❖ direct-mapped & two-way associative
  - ❖ 8 blocks with 4 words each



# Report (30%)

- ❖ **Cycle time to pass the post-synthesis simulation**
  - ❖ cache\_syn.sdc
  - ❖ tb\_cache.v
- ❖ **General Specification**
  - ❖ Write policy
  - ❖ Placement Policy
- ❖ **Finite State Machine**
- ❖ **Performance**
  - ❖ Read/Write miss rate
  - ❖ Execution cycles
  - ❖ Stalled cycles
- ❖ **Comparison of the two architectures and their results**



# Submission

## ❖ DSD\_HW3\_學號/

report.pdf

rtl/

cache\_dm.v

cache\_2way.v

syn/

cache\_dm\_syn.v

cache\_2way\_syn.v

cache\_dm\_syn.sdf

cache\_2way\_syn.sdf

cache\_dm\_syn.ddc

cache\_2way\_syn.ddc

## ❖ Compress all the files into one **ZIP** file

❖ File name: DSD\_ HW3 \_學號.zip

❖ Deadline: **2023/05/15 23:59**

❖ Late submission penalty: 20% off per day