IC Design

Homework #1

Due on 10/06/2022, 9:20 AM in class,
10% penalty for each day of delay

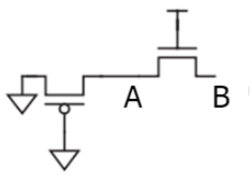
1. (20%) Please answer the following questions. Your answer should contain pictures and texts for a better explanation. A single page of A4 is recommended.
   (a) Gallium oxide is expected to drive future growth in next-generation power conversion devices. Explain what gallium oxide is, how it works, why it is superior to other materials, and where it can be used. (學號尾數為單號者回答此題)

   (b) Using TSMC's wafer-to-wafer 3D integration technology, Graphcore, a UK-based AI computer company, significantly improved its AI processor. Explain briefly what 3D integration technology is, how it works, and what difficulties it has overcome. (學號尾數為雙號者回答此題)

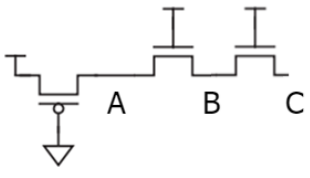
2. (15%) Please draw the compound gate using only NAND, NOR, and INV gates for the following function
   (a) $Y = \overline{(A \cdot \bar{B})} + \overline{(B \cdot C)}$
   (b) $Y = \overline{(A \oplus B)} \cdot \overline{(C \oplus D)}$
   (c) $Y = \overline{(A \cdot (B \oplus C)) \oplus (D \cdot E)}$

3. (20%) Please express **all the node voltages** in the pass transistor networks shown below (neglect the body effect).
   (You can use **V_{DD}, GND, $|V_{tp}|$, or V_{tn}** to express your answer.)
   (Assume that every NMOS has the same threshold voltage, and so does the PMOS.)

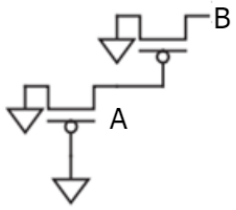
(a)



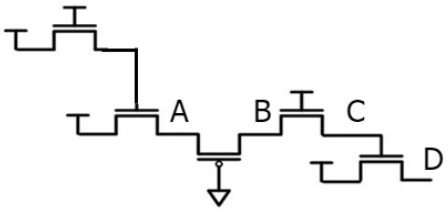
(b)



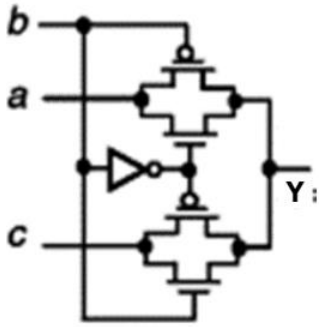
(c)



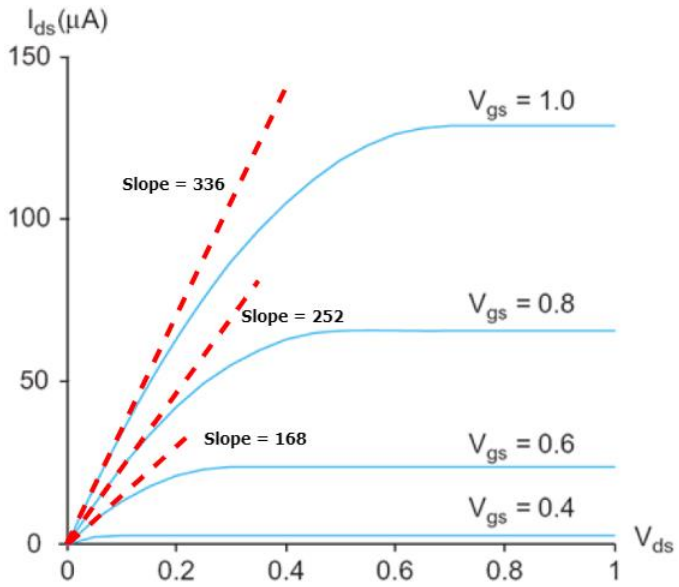
(d)



4. (20%) For the following transmission-gate circuit,
   (a) (10%) Please show the function of this circuit.
   Hint: You can use the truth table method to find the function of Y.
   (b) (10%) Is there any bad-zero or bad-one problem in this circuit? **Explain why.** (Bad-one means the voltage of logic-1 is only VDD-V_{tn}; bad-zero means the voltage of logic-0 is $|V_{tp}|$)



5. (10%) For the following I-V curves of an NMOS transistor, given the slope at 0 for the top three curves, estimate a precise value of V_t (小數點以下兩位). Explain how you find this value from the three slopes.



6. (15%) A 3-input majority gate returns output "**1**" if more than two of the inputs are "**1**".
   (a) (5%)Sketch a transistor-level circuit diagram for a 3-input majority gate using a single stage of CMOS static logic. Please use the least number of transistors. Note that all three inputs and their complements are available for this circuit.
   (b) (10%)Design a 3-input majority gate using CMOS **NANDs**, **NORs,** and **inverters**. Compare the numbers of transistors required in (a) and (b).

TA：黃名善，EE2-329

TA email: r10943003@ntu.edu.tw

HW1 Office hours: Wednesday 14:00-16:00 @電二 329 室

If you have no time during office hours, you can email TA to discuss another time for an appointment.