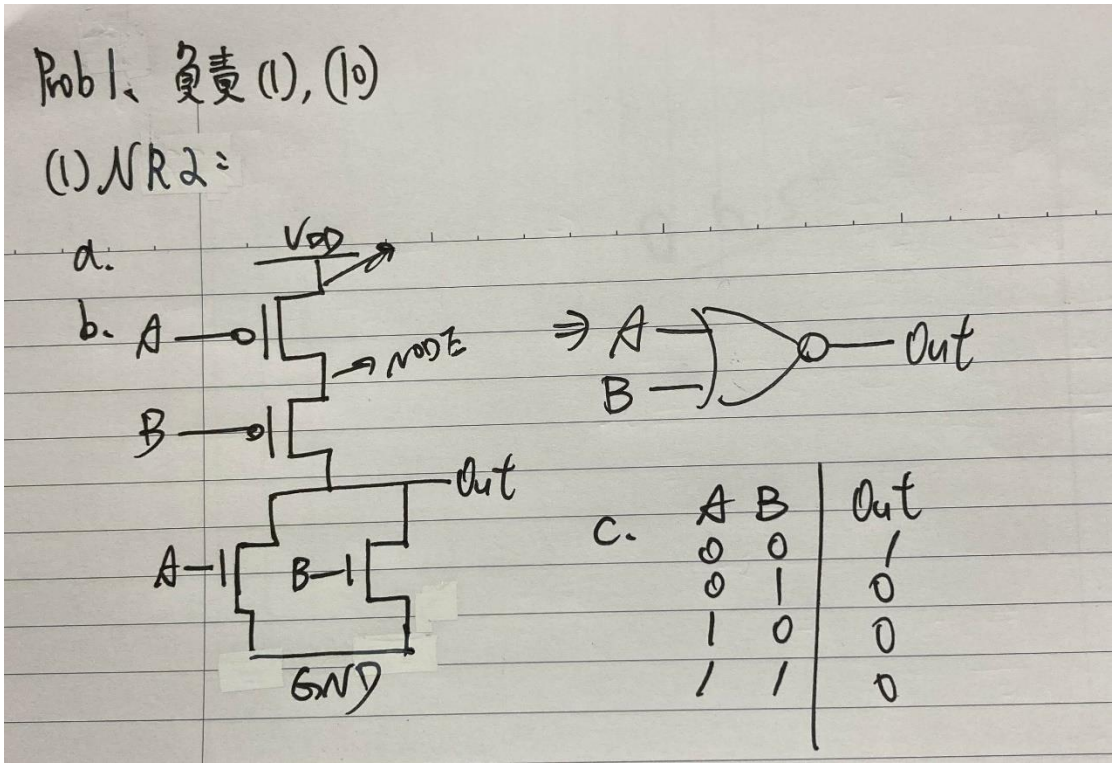
積體電路設計 hw2 B09901081 施伯儒

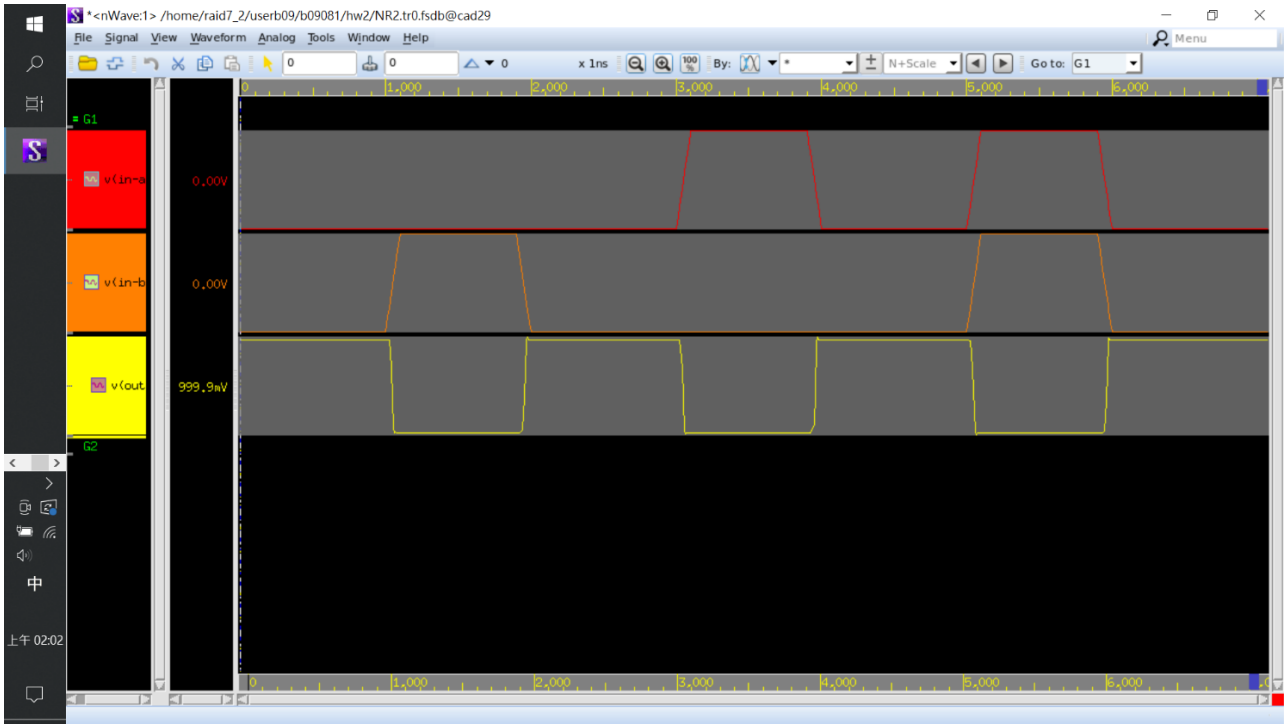
第一題:

(1) NR2: INPUT:A,B OUTPUT:OUT

a~c:



d~e:

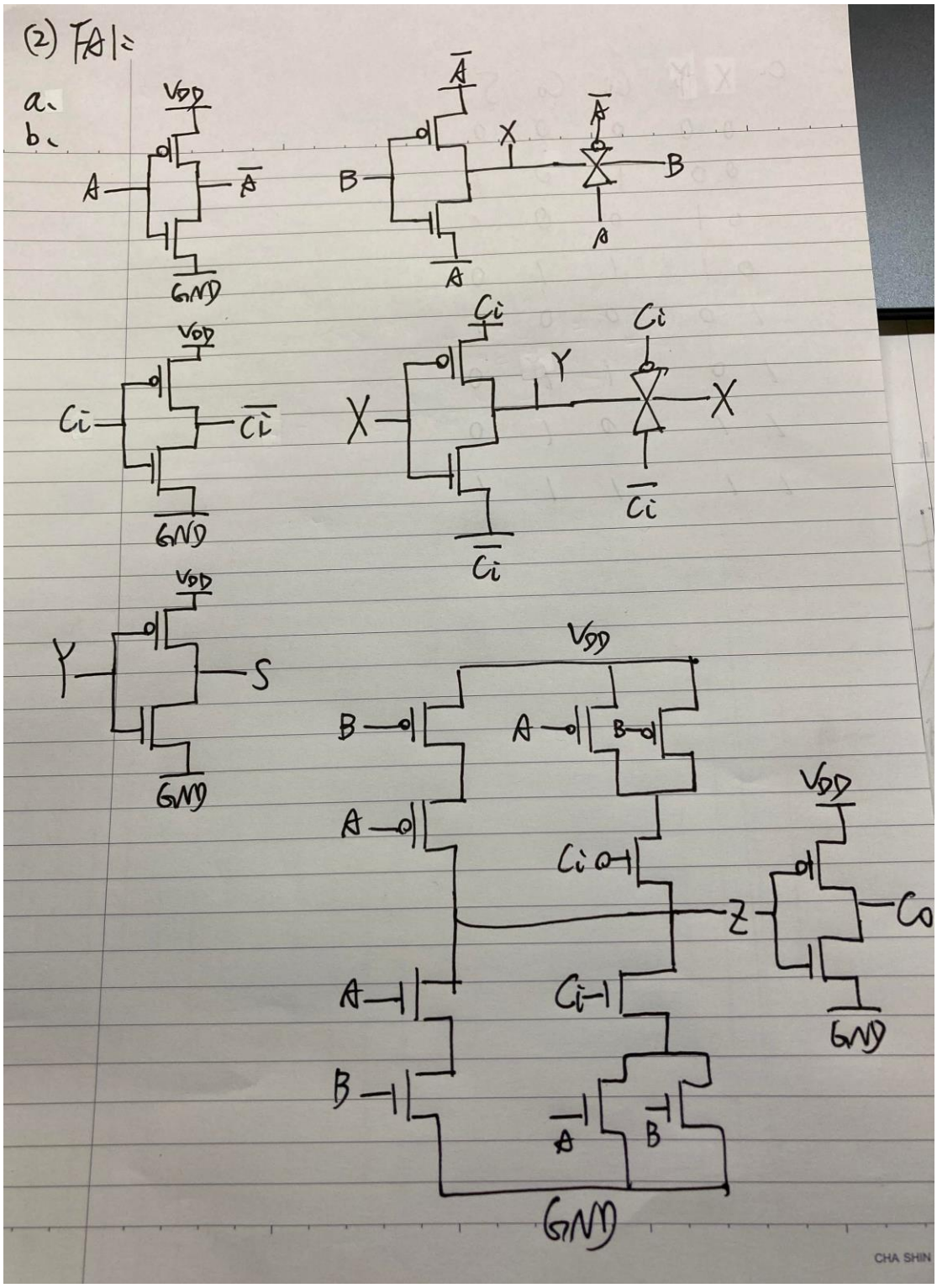


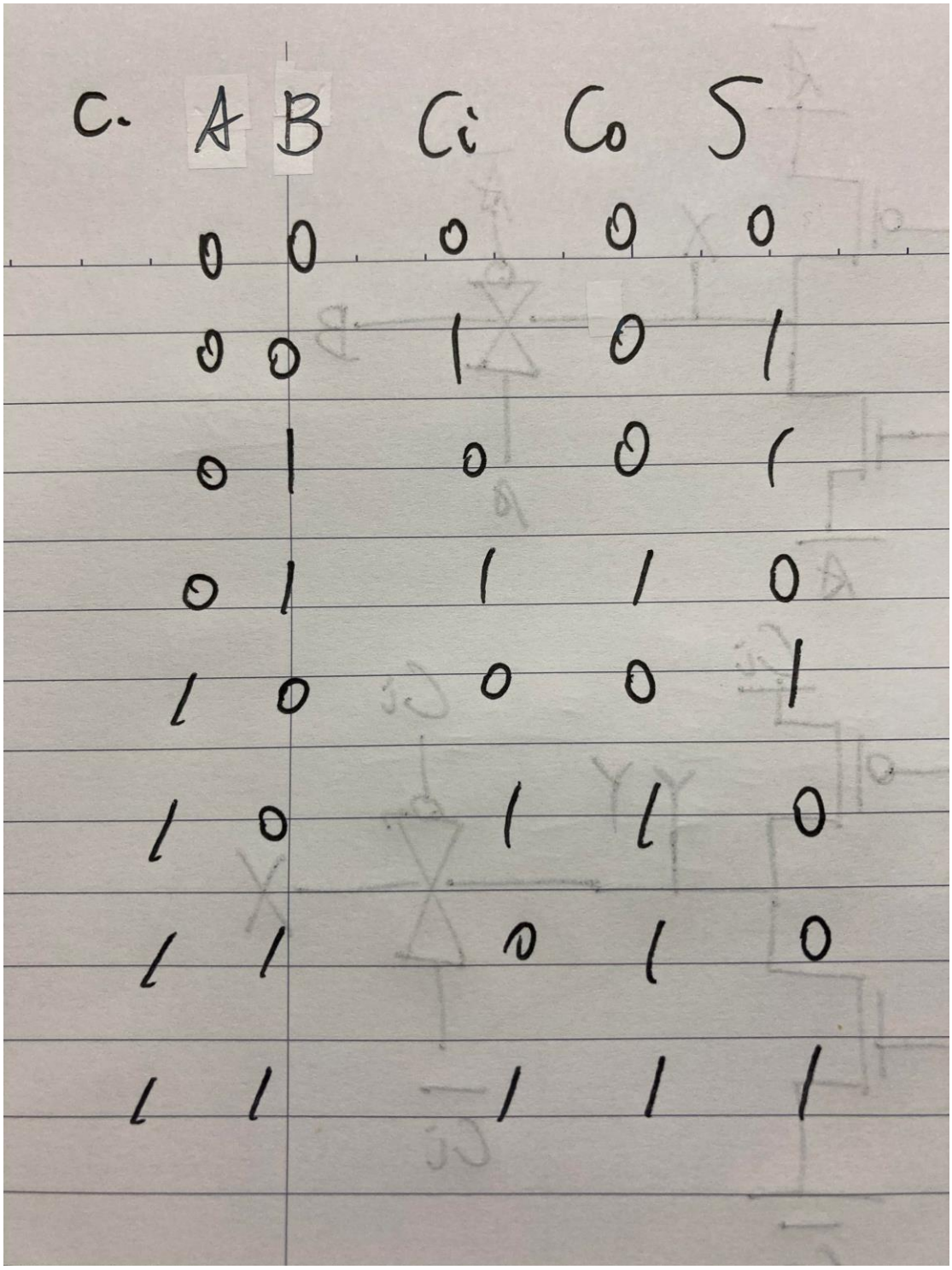

```
*********************************************
.inc '90nm_bulk.l'
.SUBCKT NR2 DVDD GND In-A In-B Out
*.PININFO   DVDD:I GND:I In-A:I In-B:I Out:O
MMA_N Out  In-A GND  GND   NMOS l=0.1u w=0.25u  m=1
MMB_N Out  In-B GND  GND   NMOS l=0.1u w=0.25u  m=1
MMA_P NODE In-A DVDD DVDD  PMOS l=0.1u w=0.5u   m=1
MMB_P Out  In-B NODE DVDD  PMOS l=0.1u w=0.5u   m=1
.ENDS
*********************************************

Vdd DVDD    0   1
Vss GND     0   0

Vin In-A    0   pulse (0 1 0 100n 100n 800n 2u)
Vin In-B    0   pulse (0 1 0 100n 100n 800n 4u)

x1  DVDD    GND In-A In-B Out    NR2

.tran 10n 7u
.op
.option post
.end
```

f:沒有遇到問題。

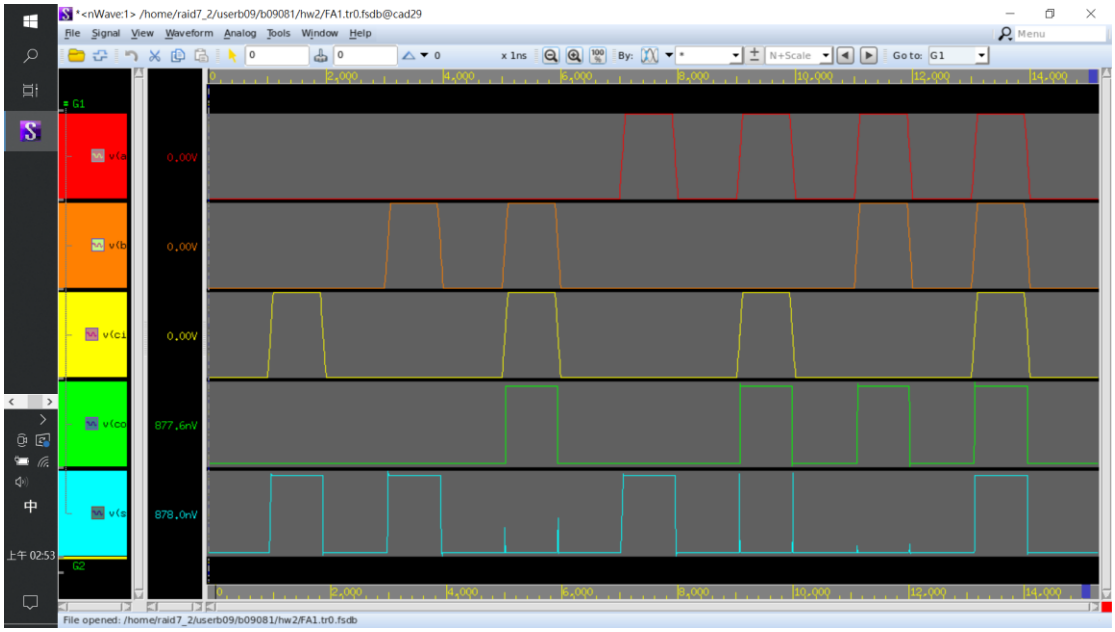
(2):FA2 INPUT:A,B,Ci OUTPUT:Co,S

a~c:





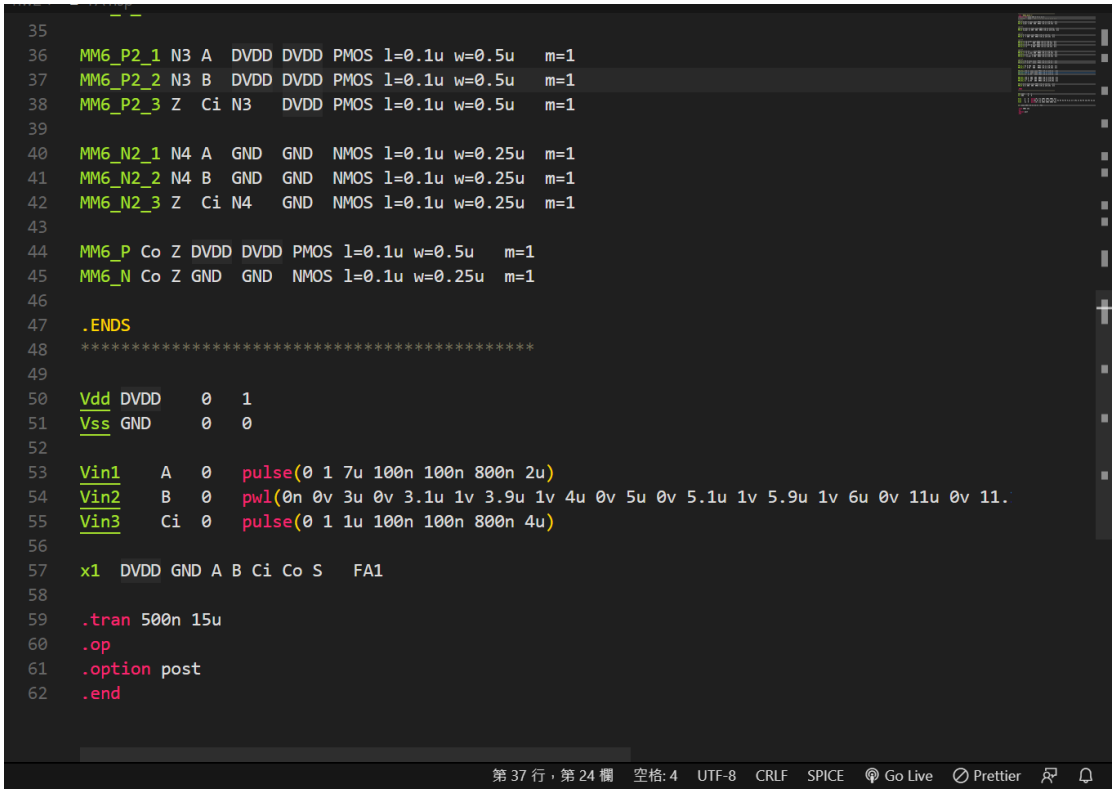
d~e:



hw2 > FA1.sp

```
*part1
MM1_P A_bar A DVDD DVDD PMOS l=0.1u w=0.5u   m=1
MM1_N A_bar A GND  GND  NMOS l=0.1u w=0.25u  m=1

*part2
MM2_P Ci_bar Ci DVDD DVDD PMOS l=0.1u w=0.5u   m=1
MM2_N Ci_bar Ci GND  GND  NMOS l=0.1u w=0.25u  m=1

*part3
MM3_P S  Y DVDD DVDD PMOS l=0.1u w=0.5u   m=1
MM3_N S  Y GND  GND  NMOS l=0.1u w=0.25u  m=1

*part4
MM4_P_1 X B A_bar DVDD PMOS l=0.1u w=0.5u   m=1
MM4_N_1 X B A     GND  NMOS l=0.1u w=0.25u  m=1
MM4_P_2 X A_bar B DVDD PMOS l=0.1u w=0.5u   m=1
MM4_N_2 X A     B GND  NMOS l=0.1u w=0.25u  m=1

*part5
MM5_P_1 Y X Ci     DVDD PMOS l=0.1u w=0.5u   m=1
MM5_N_1 Y X Ci_bar GND  NMOS l=0.1u w=0.25u  m=1
MM5_P_2 Y Ci     X DVDD PMOS l=0.1u w=0.5u   m=1
MM5_N_2 Y Ci_bar X GND  NMOS l=0.1u w=0.25u  m=1

*part6
MM6_P_1 N1 B DVDD DVDD  PMOS l=0.1u w=0.5u   m=1
MM6_P_2 Z  A N1   DVDD  PMOS l=0.1u w=0.5u   m=1

MM6_N_1 N2 B GND  GND   NMOS l=0.1u w=0.25u  m=1
MM6_N_2 Z  A N2   GND   NMOS l=0.1u w=0.25u  m=1
```

第 37 行，第 24 欄　空格: 4　UTF-8　CRLF　SPICE　Go Live　Prettier



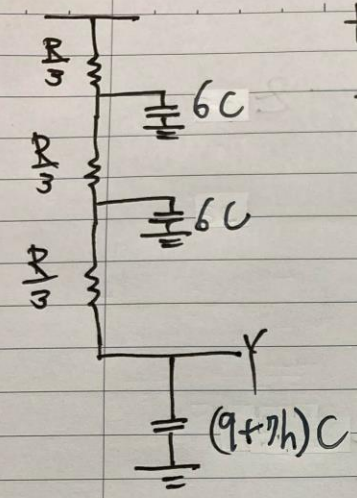
```
35
36  MM6_P2_1 N3 A  DVDD DVDD PMOS l=0.1u w=0.5u   m=1
37  MM6_P2_2 N3 B  DVDD DVDD PMOS l=0.1u w=0.5u   m=1
38  MM6_P2_3 Z  Ci N3   DVDD PMOS l=0.1u w=0.5u   m=1
39
40  MM6_N2_1 N4 A  GND  GND  NMOS l=0.1u w=0.25u  m=1
41  MM6_N2_2 N4 B  GND  GND  NMOS l=0.1u w=0.25u  m=1
42  MM6_N2_3 Z  Ci N4   GND  NMOS l=0.1u w=0.25u  m=1
43
44  MM6_P Co Z DVDD DVDD PMOS l=0.1u w=0.5u   m=1
45  MM6_N Co Z GND  GND  NMOS l=0.1u w=0.25u  m=1
46
47  .ENDS
48  ********************************************
49
50  Vdd DVDD    0   1
51  Vss GND     0   0
52
53  Vin1    A   0   pulse(0 1 7u 100n 100n 800n 2u)
54  Vin2    B   0   pwl(0n 0v 3u 0v 3.1u 1v 3.9u 1v 4u 0v 5u 0v 5.1u 1v 5.9u 1v 6u 0v 11u 0v 11.
55  Vin3    Ci  0   pulse(0 1 1u 100n 100n 800n 4u)
56
57  x1  DVDD GND A B Ci Co S   FA1
58
59  .tran 500n 15u
60  .op
61  .option post
62  .end
```


f.S 的輸出有 spikes。

第二題:

Prob2.

Rising: PMOS area是 nMOS 6倍



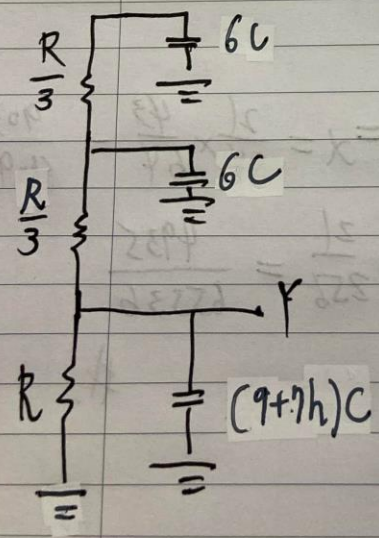
$t_{PLH}=$

$\frac{R}{3}\times 6C+\frac{2R}{3}\times 6C+R(9+7h)C$

$=2RC+4RC+(9+7h)CR$

$=(15+7h)RC$

Falling:



$t_{PHL}=$

$RC(9+7h)+6RC+6RC$

$=RC(9+7h+12)$

$=(21+7h)RC$

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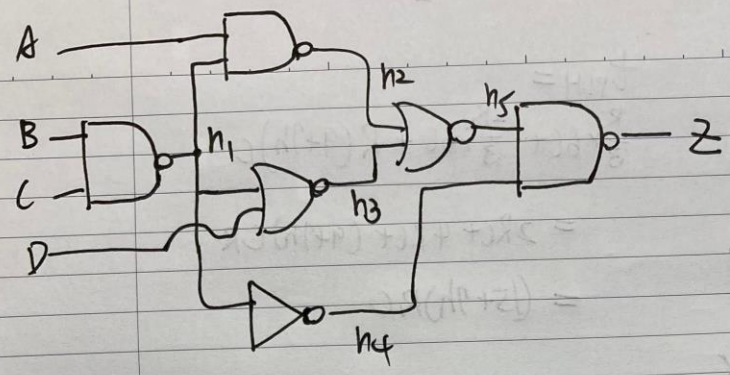
第三題:

Prob3.



$n1: P=\frac{3}{4}, \alpha=\frac{3}{16}$

$n2: 1-\frac{1}{2}\times\frac{3}{4}=\frac{5}{8}=P, \alpha=\frac{5}{8}\times\frac{3}{8}=\frac{15}{64}$

$n3: \frac{1}{2}\times(1-\frac{3}{4})=\frac{1}{8}=P, \alpha=\frac{1}{8}\times\frac{7}{8}=\frac{7}{64}$

$n4 \rightarrow P=\frac{1}{4}, \alpha=\frac{1}{4}\times\frac{3}{4}=\frac{3}{16}$

$n5: (1-\frac{5}{8})(1-\frac{1}{8})=\frac{3}{8}\times\frac{7}{8}=\frac{21}{64}=P, \alpha=\frac{21}{64}\times\frac{43}{64}=\frac{903}{4096}$

$Z: 1-\frac{21}{64}\times\frac{1}{4}=\frac{235}{256}, \alpha=\frac{235}{256}\times\frac{21}{256}=\frac{4935}{65536}$

$\frac{235}{256}=P$

#.