Shih-Ling Shen

+1 (778) 875-0772 | shihling@shihling.com | linkedin.com/in/shih-ling-shen/ | shihling.com

OBJECTIVE

Seeking full-time digital design opportunities after graduation in May 2027

EDUCATION

Bachelor of Applied Science in Electrical Engineering — **Sep 2022 - May 2027**
University of British Columbia — ***Vancouver, BC***

- Courses: Digital System Design, Computer Systems, Data Structures & Algorithms

WORK EXPERIENCE

ASIC Digital Design/Verification Intern — **Jan 2025 - Current**
Synopsys, Inc. — ***Ottawa, ON***

- Designed and verified features within 224G Ethernet PHY IP transmitter and receiver blocks
- Utilized PrimeTime and PrimePower for power estimation and generating power waveforms
- Implemented VC SpyGlass LINT flows to improve RTL quality and identify design issues
- Developed UVM testbenches for generating and verifying ATE test vectors through JTAG and APB

Undergraduate Teaching Assistant I — **Sep 2023 - Dec 2023, Sep 2024 - Dec 2024**
University of British Columbia — ***Vancouver, BC***

- 2024W1 ELEC 202 - Circuit Analysis II
- 2024W1 CPSC 259 - Data Structures and Algorithms for Electrical Engineers
- 2023W1, 2024W1 APSC 160 - Introduction to Computation in Engineering Design

ENGINEERING DESIGN TEAM

Electrical Team Lead — **Sep 2022 - Oct 2024**
UBC Sailbot — ***Vancouver, BC***

- Undergraduate student team focused on creating fully autonomous sailboats capable of sailing in the Pacific Ocean and collecting research data for climate change research
- Led the electrical team consisting of more than 25 students in creating custom PCBs, firmware, motor systems, battery systems, and solar panel solutions

PROJECTS

Waveform Generator and Music Player — **Jun 2024**

- A GUI application running on NIOS II CPU that is written in C, SystemVerilog, and VHDL that serves as a music player and a waveform generator with various modulations at the same time

RC4 Decoder — **Jun 2024**

- Decodes RC4-encrypted 32 byte messages with a 24-bit secret key within 1 second using a 64-core hardware accelerator written with VHDL and SystemVerilog for the DE1-SoC

AWARDS

- **Kenneth George VanSacker Memorial Scholarship** — **Feb 2025**
- **Dean's Honour List** — **May 2023, May 2024**
- **Rogers Communication Inc Scholarship** — **Apr 2024**
- **Outstanding International Student Award** — **Apr 2022**

SKILLS

- **Languages:** SystemVerilog, Python, C/C++, Bash, ARM/8051 Assembly, VHDL
- **Tools:** Synospys Verdi, VCS, VC Spyglass, UVM, PrimeTime, PrimePower, Formality, WaveView, Quartus, ModelSim, MATLAB, SQLite
- **Version Control:** Git, Perforce P4