# **Shih-Ling Shen**

+1 (778) 875-0772 | shihling@shihling.com | linkedin.com/in/shih-ling-shen/ | shihling.com

### **OBJECTIVE**

Apply digital design knowledge in the design and verification of real-world products.

#### **EDUCATION**

### **Bachelor of Applied Science in Electrical Engineering**

Sep 2022 - May 2027

### University of British Columbia

Vancouver, BC

Courses: Digital System Design, Computer Systems, Data Structures & Algorithms

### WORK EXPERIENCE

### **ASIC Digital Design/Verification Intern**

Jan 2025 - Current

Synopsys, Inc.

Ottawa, ON

 Designing and verifying current and next generation Backplane Ethernet, PCIe, SATA, and USB 2/3 SERDES products

# APSC 160 & CPSC 259 & ELEC 202 - Undergraduate Teaching Assistant I

Sep 2024 - Dec 2024 Vancouver, BC

University of British Columbia

- 2024W1 APSC 160 Introduction to Computation in Engineering Design
- 2024W1 CPSC 259 Data Structures and Algorithms for Electrical Engineers
- 2024W1 ELEC 202 Circuit Analysis II

### **APSC 160 - Undergraduate Teaching Assistant I**

Sep 2023 - Dec 2023

University of British Columbia

Vancouver, BC

• 2023W1 APSC 160 - Introduction to Computation in Engineering Design

#### **ENGINEERING DESIGN TEAM**

**Electrical Team Lead** 

Sep 2022 - Oct 2024

**UBC** Sailbot

Vancouver, BC

- Undergraduate student team focused on creating fully autonomous sailboats capable of sailing in the Pacific Ocean and collecting research data for climate change research
- Leading the electrical team consisting of more than 25 students in creating custom PCBs, firmware, motor systems, battery systems, and solar panel solutions

## **PROJECTS**

# **Waveform Generator and Music Player**

Jun 2024

• A GUI application running on NIOS II CPU that is written in C, SystemVerilog, and VHDL that serves as a music player and a waveform generator with various modulations at the same time

RC4 Decoder Jun 2024

• Decodes RC4-encrypted 32 byte messages with a 24-bit secret key within 1 second using a 64-core hardware accelerator written with VHDL and SystemVerilog for the DE1-SoC

#### **AWARDS**

• Dean's Honour List

May 2023, May 2024

• Rogers Communication Inc Scholarship

Apr 2024

• Outstanding International Student Award

Apr 2022

### **SKILLS**

- **Digital Design:** SystemVerilog, VHDL, Quartus, ModelSim, QSys, NIOS II, Picoblaze
- Software: C, Linux, Bash, Assembly, Git, MATLAB, Python, Arduino
- Electrical Design: Altium Designer, KiCAD, Soldering, Perfboard Prototypes
- Communication Protocols: CAN FD, I2C, NMEA 2000
- Languages: English (Native), Mandarin (Native)