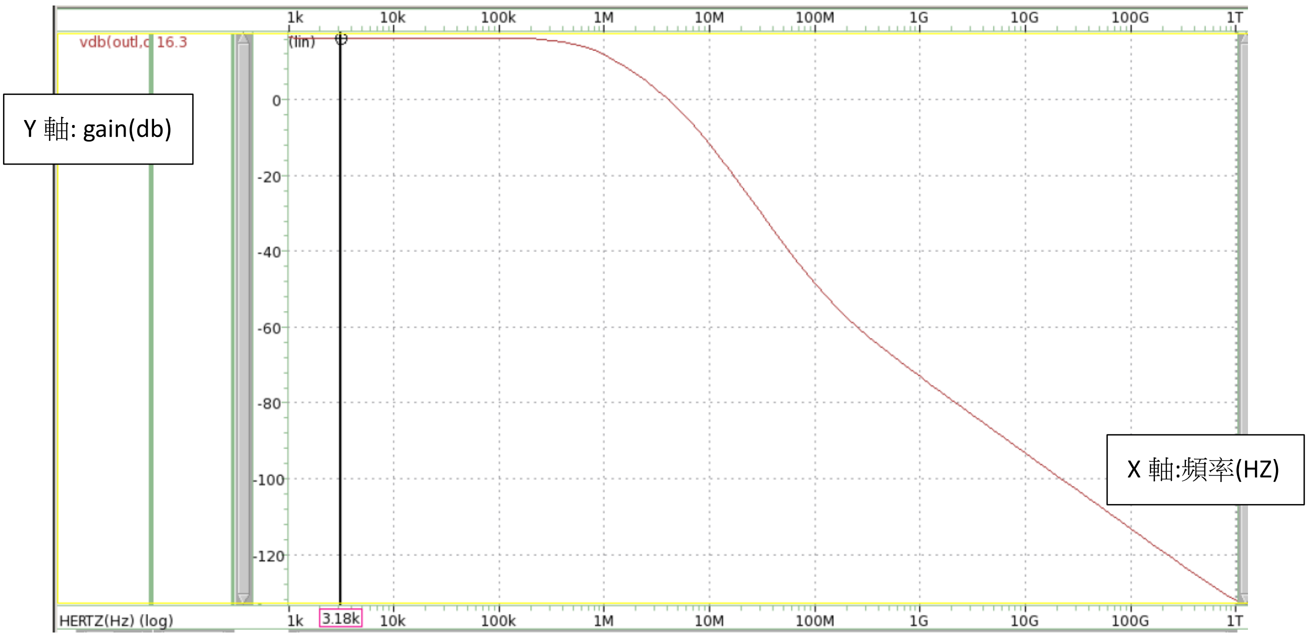
106010006 黃詩瑜 電機 21

Design Items	Specifications	My work
Technology	CIC pseudo 0.18um technology	
Supply voltage	1.8V	
Input common mode	0.9V	
Tail current	< 4uA, as smaller as possible [#1]	3.3548u
Loading	1.5 pF	
Source Impedance	5k ohm	
Simulations		
Gain	> 16 dB, as large as possible	16.3276
Unity-GBW	> 4MHz, as large as possible [#2]	4.0773M
P.M.	> 45°	64.8740
C.M.R.R @ 10kHz	Open for design (dB)	62.2
Linear range	Single-ended input amplitude (mV) [#3]	24
FOM	(#2) x (#3) / (#1)	29.168

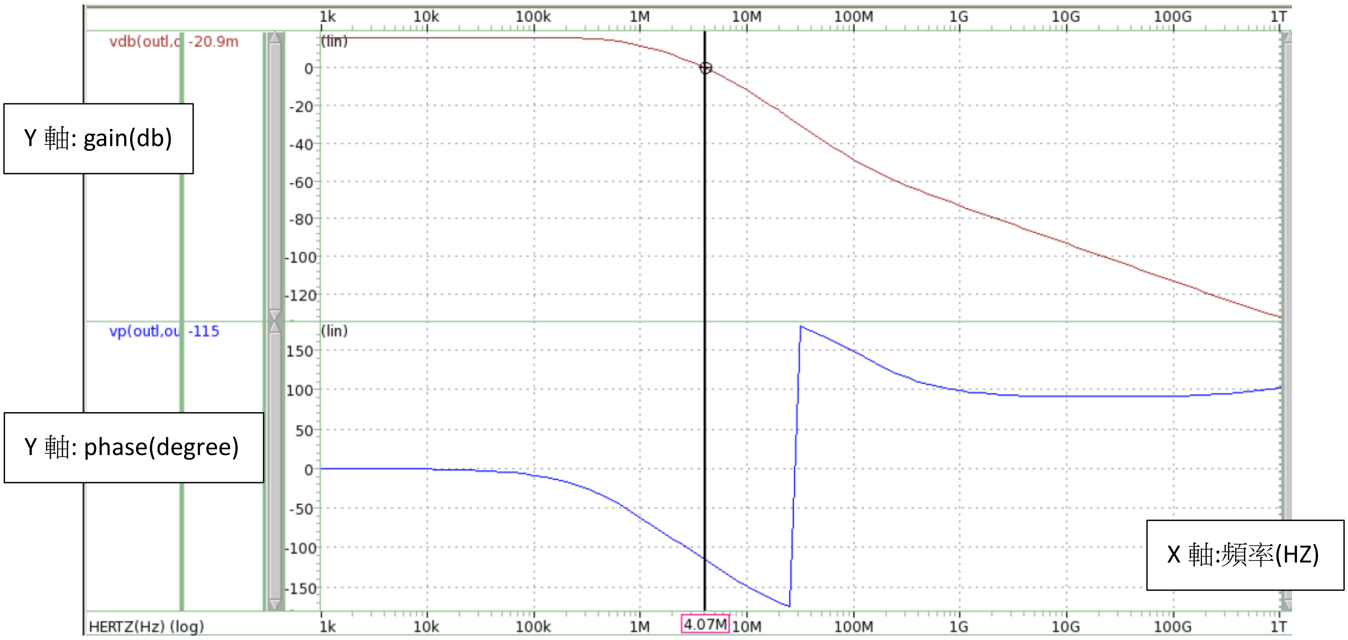
a. Open-loop differential mode AC response

1.

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  16.3276      at=   1.0000k
                 from=   1.0000k      to=   1.0000t
dcgain=   6.5521      at=   1.0000k
                 from=   1.0000k      to=   1.0000t
unity_frequency=   4.0773x
phase=-115.1260
phase_margin=  64.8740
```



DC gain: 16.3 (dB)



unity-gain frequency: 4.07M (Hz)

phase margin: 180-115 = 65 (degree)

2.

subckt					
element	0:mmpl	0:mmpr	0:mmnl	0:mmnr	0:mmnd
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-2.6774u	-2.6774u	2.6774u	2.6774u	3.3548u
ibs	3.252e-22	3.252e-22	-3.0892f	-3.0892f	-8.144e-22
ibd	182.3479a	182.3479a	-4.8725f	-4.8725f	-985.2084a
vgs	-1.0410	-1.0410	418.7905m	418.7905m	520.0000m
vds	-1.0410	-1.0410	277.7997m	277.7997m	481.2095m
vbs	0.	0.	-481.2095m	-481.2095m	0.
vth	-462.7493m	-462.7493m	405.5573m	405.5573m	310.8560m
vdsat	-491.2531m	-491.2531m	65.8156m	65.8156m	183.1267m
vod	-578.2414m	-578.2414m	13.2332m	13.2332m	209.1440m
beta	18.8190u	18.8190u	2.0847m	2.0847m	278.8898u
gam eff	557.0846m	557.0846m	519.4780m	519.4780m	507.4459m
gm	8.4820u	8.4820u	57.3461u	57.3461u	46.6193u
gds	14.1484n	14.1484n	256.2480n	256.2480n	99.7922n
gmb	2.8412u	2.8412u	9.4796u	9.4796u	9.1182u
cdtot	3.7031f	3.7031f	125.3375f	125.3375f	59.0129f
cgtot	190.3110f	190.3110f	5.3176p	5.3176p	5.4551p
cstot	215.5938f	215.5938f	4.7866p	4.7866p	5.6223p
cbtot	67.0441f	67.0441f	1.8427p	1.8427p	1.5171p
cgs	176.8424f	176.8424f	4.3015p	4.3015p	4.9788p
cgd	1.2365f	1.2365f	27.9546f	27.9546f	16.7005f

3.

****** pole/zero analysis

input = 0:v+ output = v(outl,outr)

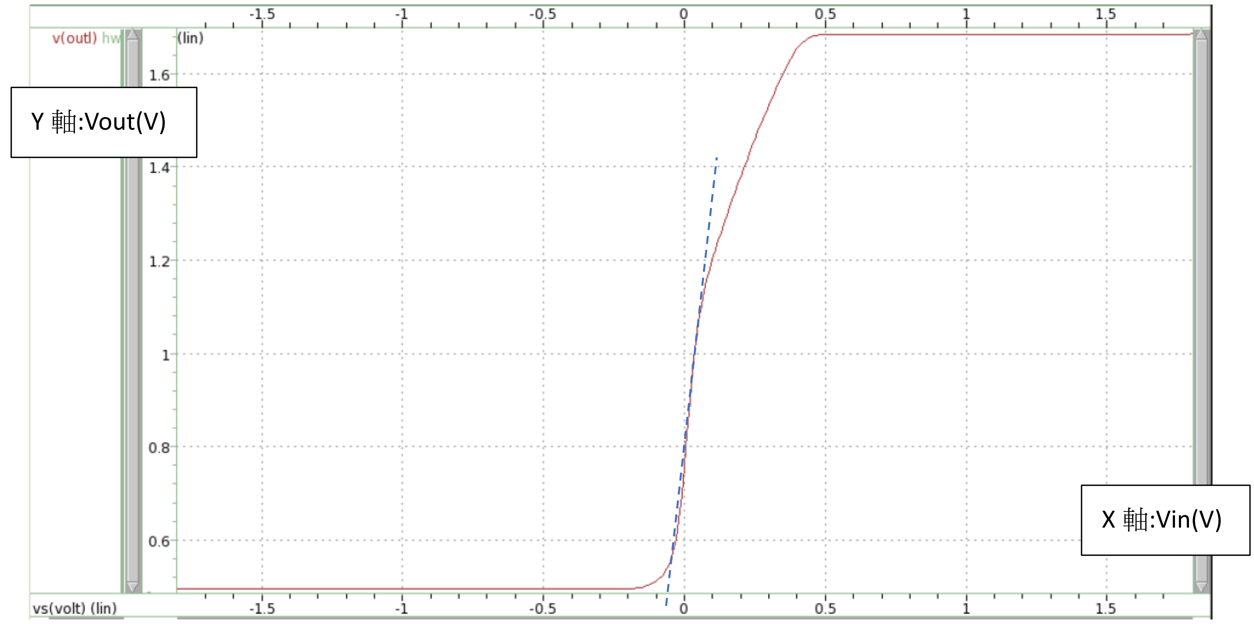
poles (rad/sec) real	imag	poles (hertz) real	imag
-4.66074x	0.	-741.780k	0.
-4.79360x	0.	-762.925k	0.
-14.0920x	0.	-2.24281x	0.
-37.8097x	0.	-6.01760x	0.
-114.168x	0.	-18.1704x	0.

zeros (rad/sec) real	imag	zeros (hertz) real	imag
-4.65964x	0.	-741.604k	0.
-13.8337x	0.	-2.20170x	0.
-97.2915x	0.	-15.4844x	0.
351.501x	0.	55.9431x	0.

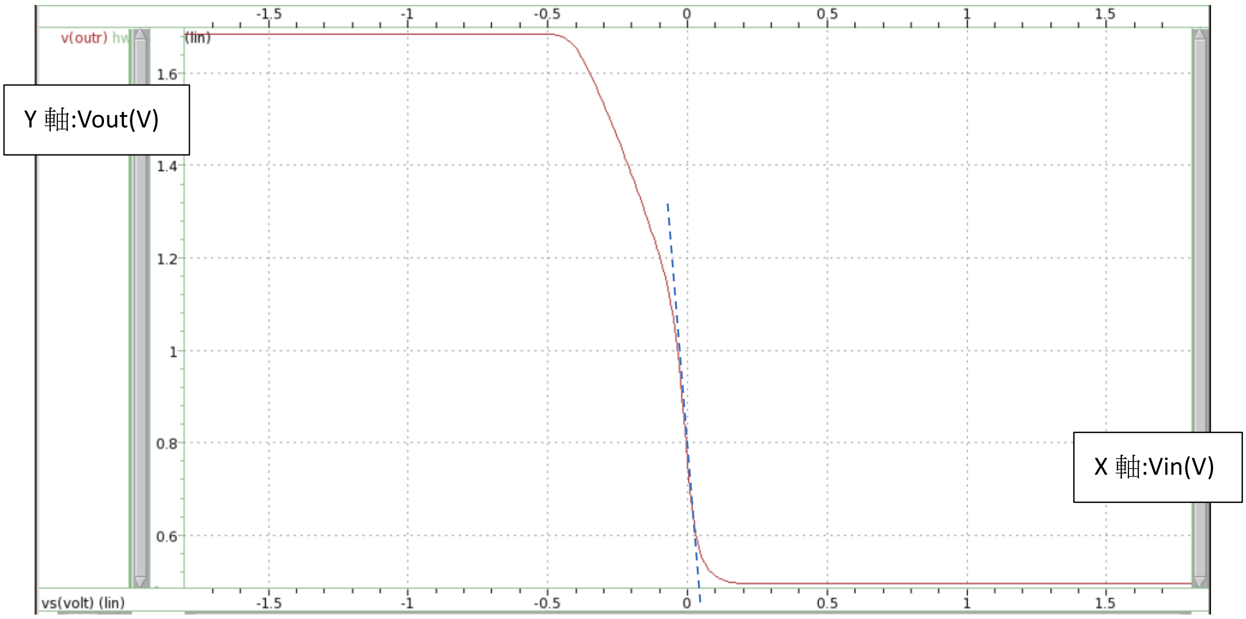
b. Open-loop differential mode DC sweep

single-ended:

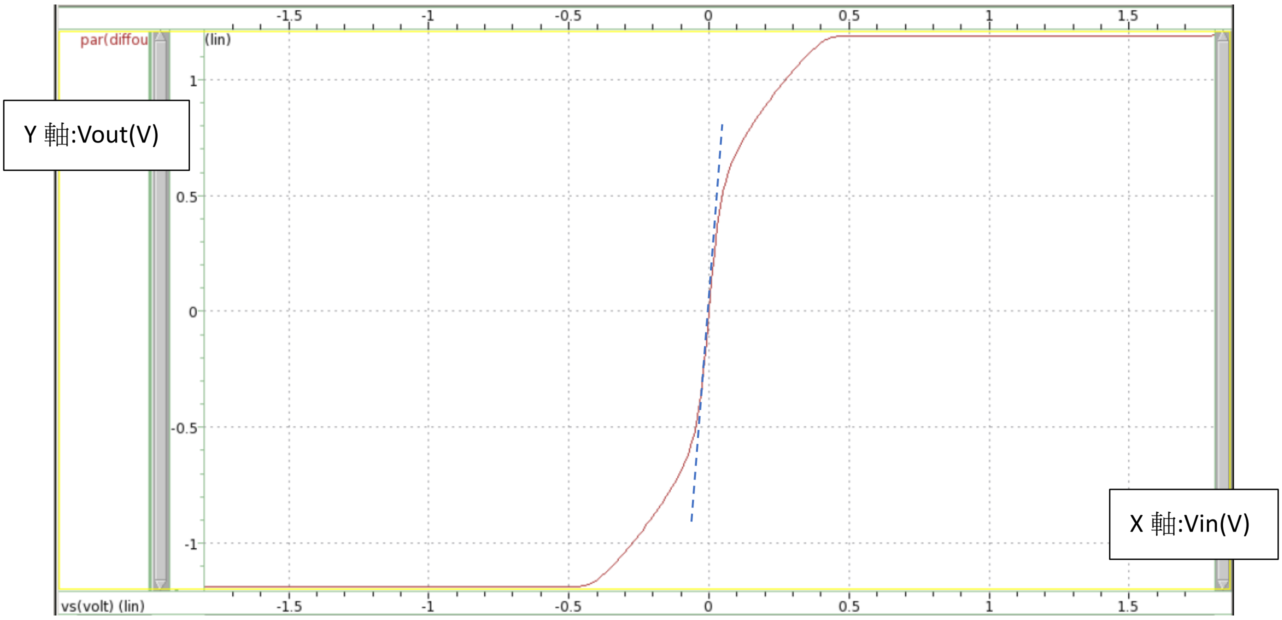
左邊的 output:



右邊的 output:



differential outputs:



Equation

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:hw7b.sw0	slope(v(outl),0)			6.19		
D0:hw7b.sw0	slope(v(outr),0)			-6.81		
D0:hw7b.sw0	slope(par(diffout),0)			13		

斜率:

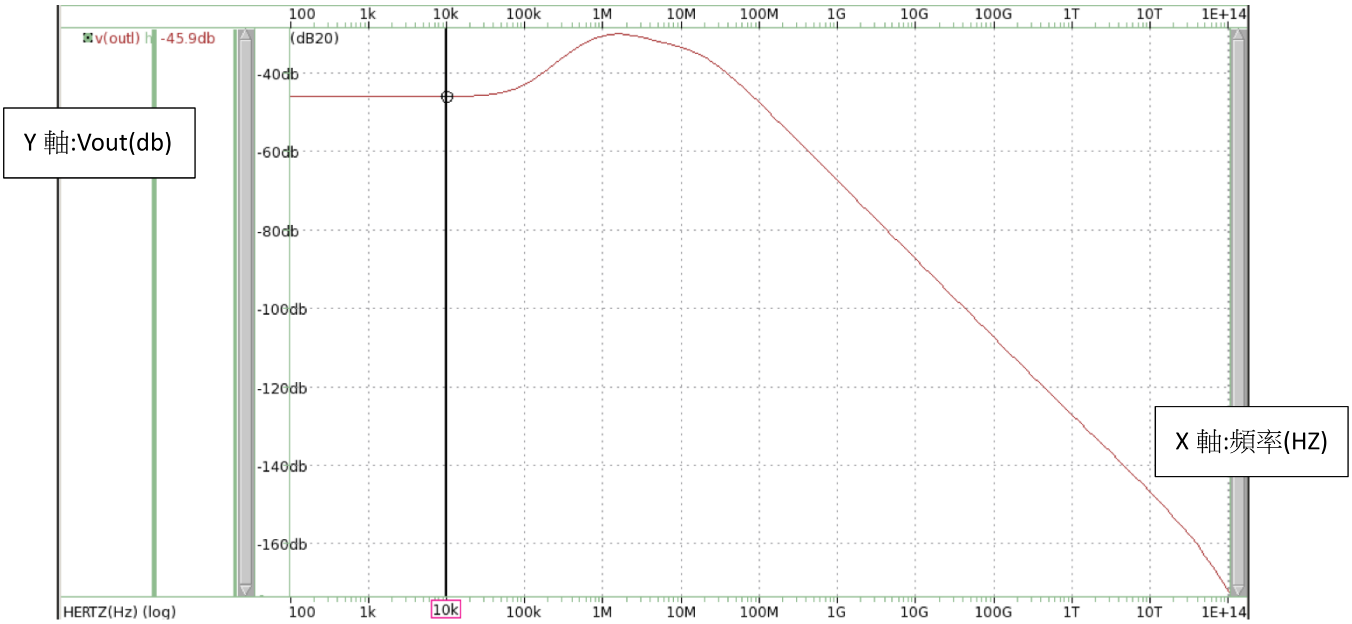
single-ended:

6.19/-6.81

differential outputs:

13

c. Open-loop common mode AC response

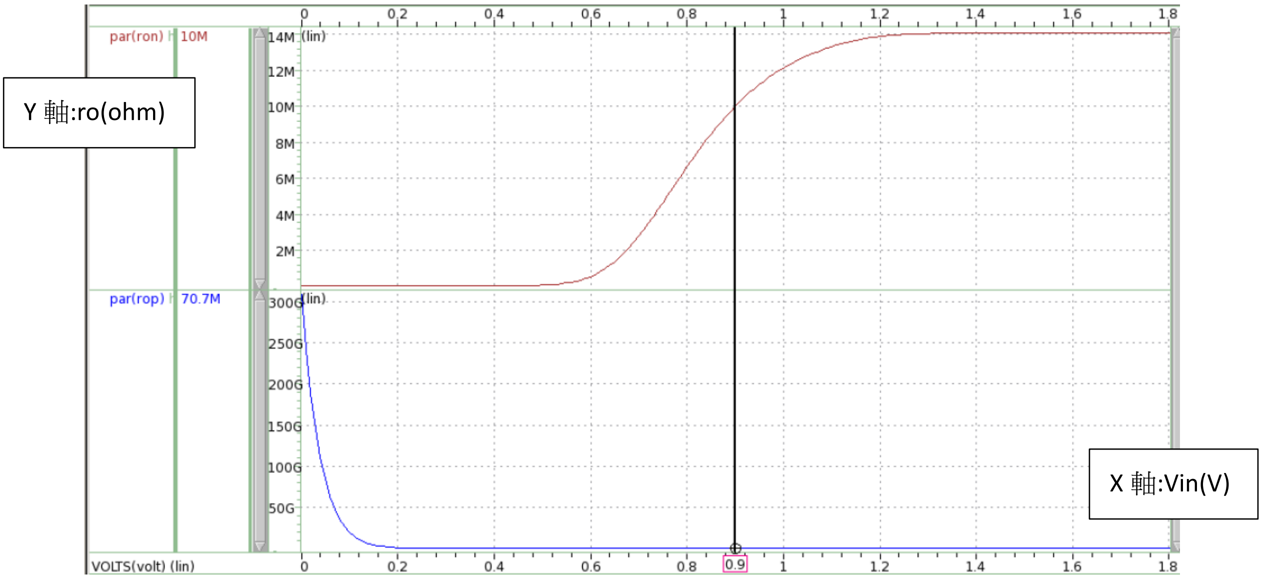


DC gain: -45.9 (dB)

手算 gain:

$$\frac{\Delta Vout}{\Delta Vin}=\frac{-(\frac{1}{g_{mp}}//r_{op})}{2r_{on}+\frac{1}{g_{mn}}}$$

r_{on}為tail current的nmos的，g_{mn}為上方的nmos的



$$\frac{\Delta Vout}{\Delta Vin}=\frac{-(\frac{1}{8.4820u+\frac{1}{70.7M}})}{2X10M+\frac{1}{57.3416u}}=-0.005834(V/V)$$

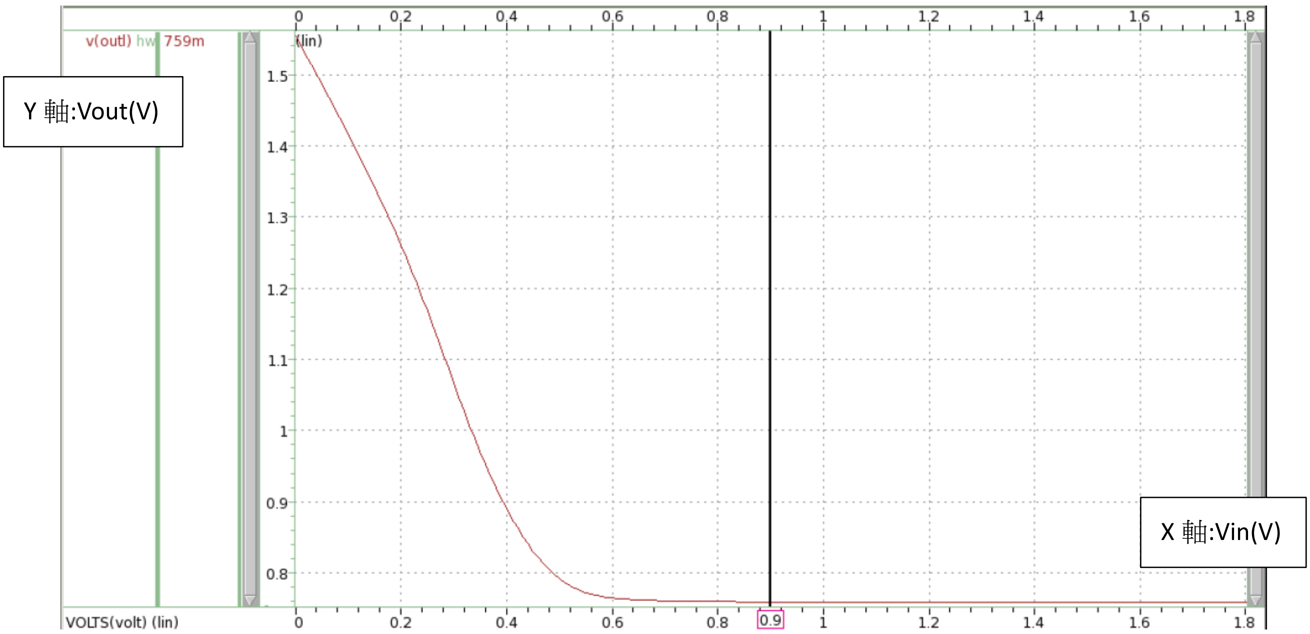
$$-0.005834(\mathrm{V/V})=-44.68(\mathrm{dB})$$

手算與模擬誤差:

$$\frac{-45.9-(-44.68)}{-45.9}X100\%=2.657\%$$

誤差很小，兩值相近

d. Open-loop common mode DC sweep



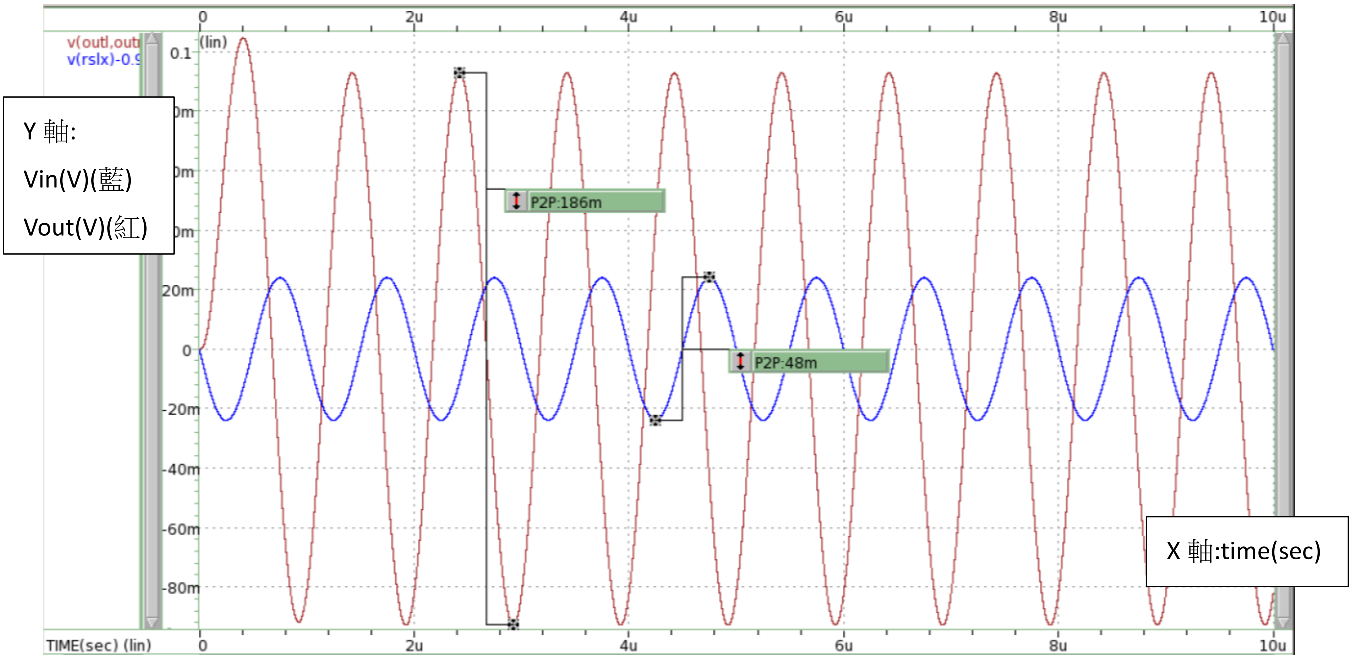
Equation							
File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:hw7d.sw0	slope(v(outl),0.9)			-5.08m		

斜率: 5.08m = -45.882(dB)

與上題求出的 DC gain 值相近

e. Linear range

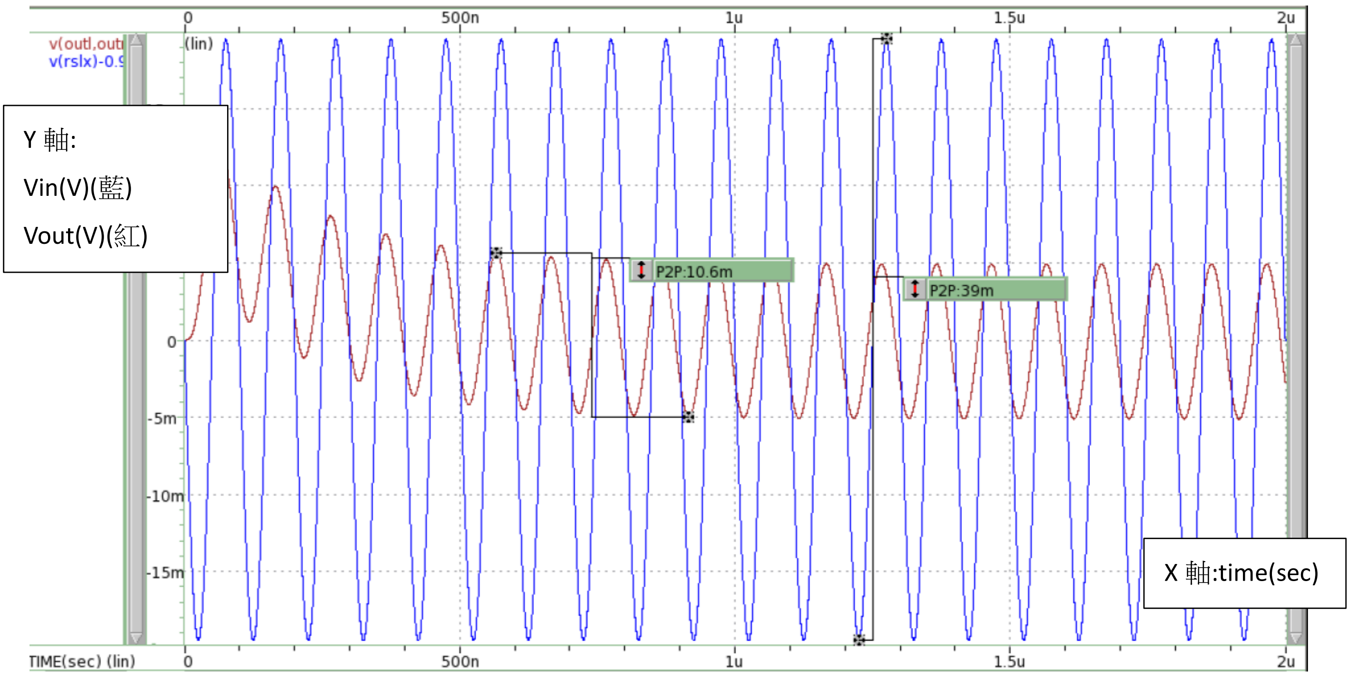
頻率:1M(HZ)　Vin (p-p)=48mV　振幅=24m，Vout (p-p)=186mV　振幅=93mV



harmonic no	frequency (hz)	fourier component	normalized component	phase (deg)	normalized phase (deg)
1	1.0000x	92.9996m	1.0000	-152.4423	0.
2	2.0000x	46.4814u	499.8022u	-4.0339	148.4085
3	3.0000x	149.7049u	1.6097m	135.8793	288.3216
4	4.0000x	1.3128u	14.1159u	-152.4785	-36.1603m
5	5.0000x	405.7097n	4.3625u	3.7222	156.1646
6	6.0000x	7.9173n	85.1327n	-164.0869	-11.6445
7	7.0000x	20.1888n	217.0844n	166.6811	319.1234
8	8.0000x	30.9676n	332.9864n	111.9774	264.4197
9	9.0000x	24.8559n	267.2686n	-119.1485	33.2938

total harmonic distortion =　0.098561　percent

頻率:10M(HZ)　Vin (p-p)=39mV　振幅=19.5mV，Vout (p-p)=10.6mV　振幅=5.3mV



harmonic no	frequency (hz)	fourier component	normalized component	phase (deg)	normalized phase (deg)
1	10.0000x	5.0203m	1.0000	121.3018	0.
2	20.0000x	4.9764u	991.2427u	121.9424	640.5995m
3	30.0000x	119.5380n	23.8107u	-31.8964	-153.1982
4	40.0000x	72.3294n	14.4072u	-62.8508	-184.1527
5	50.0000x	73.5134n	14.6431u	-151.5157	-272.8175
6	60.0000x	41.6647n	8.2992u	-158.2215	-279.5234
7	70.0000x	23.9774n	4.7760u	-2.1103	-123.4121
8	80.0000x	23.2932n	4.6398u	-14.7907	-136.0925
9	90.0000x	26.2448n	5.2277u	-86.8576	-208.1594

total harmonic distortion = 0.0991812 percent

模擬出的 single-ended input amplitude value at 1MHz 為 24mV，手算的 linear range 值為 0.2Vov=0.2X13.2332m=2.64664mV，兩者誤差非常多，推測是為了符合題目的要求，要將電流減少到小於 4u，而 nmos 的狀態與 cutoff 太接近了，所以不能完全符合 current 在 saturation 的公式，且在推導公式的過程中利用了大量的近似，所以誤差才這麼多。

f.

FoM=bandwidth (MHz) x linear range (mV) / tail current (μA)

=4.0773M X 24 / 3.3548u = 29.168

$$\mathrm{Av} = -g_{mn}\left(\frac{1}{g_{mp}}//r_{on}//r_{op}\right) \approx -\frac{g_{mn}}{g_{mp}} = -\sqrt{\frac{\mu_n(\frac{W}{L})_n}{\mu_p(\frac{W}{L})_p}}$$

linear range = Vov

tail current = Id

The diode-connected differential amplifer consume voltage headroom, thus creating a trade-off between:

- the output voltage swings
- the voltage gain

- the input CM range

To achieved higher gain, $\frac{g_{mn}}{gmp}$ must be increased =>> $\frac{\left(\frac{W}{L}\right)_n}{(\frac{W}{L})_p}$ increased =>> $\left(\frac{W}{L}\right)_p$ must be decreased.

I let Gain higher than 16db first.

Problem with this approach:

This increase |Vgsp-Vthp| and lowering the CM level at nodes, since more voltage drop across the PMOS.

So after adjusting, my parameter of pmos:

.param wp=3u

.param lp=10u

my parameter of nmos:

.param wn=90u

.param ln=13u

.sp 檔

```
*hw7a
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.temp 25
.option delmax = 1e-10

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx dc =    vs ac =0.5 0
V- Vx rsrx dc = -vs ac =0.5 180
VD vdd gnd 1.8V


.meas ac dcgain_in_db max vdb(outl,outr)
.meas ac dcgain max vm(outl,outr)

.op
.ac dec 10 1k 1T

.meas ac unity_frequency when vdb(outl,outr)=0
.meas ac phase find vp(outl,outr) at=unity_frequency
.meas ac phase_margin param='180+phase'
.probe V(outl)
.probe V(outr)
.probe diffout = par('V(outl)-V(outr)')

*pole/zero
.pz V(outl,outr) V+
```

```
.END
*******************************************************************************
*hw7b
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.temp 25
.option delmax = 1e-10

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx dc =    vs
V- Vx rsrx dc = -vs
VD vdd gnd 1.8V

.DC Vs -1.8 1.8 0.01
.probe diffout = par('V(outl)-V(outr)')

.END
*******************************************************************************
*hw7c
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.temp 25
.option delmax = 1e-10

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx dc =    vs ac =1 0
V- Vx rsrx dc = -vs ac =1 0
VD vdd gnd 1.8V

.op
```

```
.ac dec 10 0.1k 100T

.meas ac acm_in_db find vdb(outl) at=10k
.end
******************************************************************************
*hw7d
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.temp 25
.option delmax = 1e-10

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx dc =    vs
V- Vx rsrx dc = vs
VD vdd gnd 1.8V

.DC Vcm 0 1.8 0.01
.probe DC
+ rop = par('1/LX8(mmpl)')
+ ron = par('1/LX8(mmnd)')

.END
******************************************************************************
*hw7e1M
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.option delmax = 1e-10
.temp 25

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx sin(0V 0.024V 1x 0ns)
```

```
V- Vx rsrx dc =-vs ac =0
VD vdd gnd 1.8V

.op
.tran 0.1ns 10us
.four 1x v(outl,outr)
.probe AC

.END
******************************************************************************
*hw7e10M
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+runlvl=6
.option delmax = 1e-10
.temp 25

.param wp=3u
.param lp=10u
.param wn=90u
.param ln=13u
.param wnd=28u
.param lnd=30u
.param vbss=0.52
.param vs =0


mmpl outl outl vdd vdd p_18 W=wp L=lp m=1
mmpr outr outr vdd vdd p_18 W=wp L=lp m=1
mmnl outl n1 nd gnd n_18 W=wn L=ln m=1
mmnr outr nr nd gnd n_18 W=wn L=ln m=1
mmnd nd vbs gnd gnd n_18 W=wnd L=lnd m=1

rsl n1 rslx 5k
rsr nr rsrx 5k
cll outl gnd 1.5p
clr outr gnd 1.5p

Vcm Vx GND dc = 0.9V
Vbs Vbs GND dc = vbss
V+ Vx rslx sin(0V 0.0195V 10x 0ns)
V- Vx rsrx dc =-vs ac =0
VD vdd gnd 1.8V

.op
.tran 0.1ns 2us
.four 10x v(outl,outr)
.probe AC

.END
```