

Design Items	Specifications	My Work
Technology	CIC pseudo 0.18um technology	
Supply voltage	1.5V , as small as possible	1.5V
Vicm, Vocm	0.75V / 0.75V	0.75/0.7499
Supply current	< 5mA , as small as possible	0.461m
Loading	5pF / 50KΩ (for each output)	5p/50K
Compensation R, C,	Open for design	10K(ohm)/3p(F)
Open-loop simulation		
DC gain	> 60dB , as large as possible	70.8482
G-BW	> 1MHz , as large as possible	22.1267M
P.M.	> 45 °	58.3983
C.M.R.R. @10KHz	>80dB	80.1
P.S.R.R.+ @10KHz	> 80dB	84.5
P.S.R.R.- @10KHz	> 80dB	97.4
Closed-loop simulation		
Differential swing of 1.2V (step signal)		
S.R.+ (10% ~ 90%)	> 1 V/us	4.92
S.R.- (90% ~ 10%)	> 1 V/us	4.92
Settling+ (to 0.1%)	< 10 us	2.7537u
Settling- (to 0.1%)	< 10 us	2.7537u
FoM		
Small signal	GBW (MHz) x CL (pF) / Power (mW)	133.3255
Large signal +	SR+ (V/us) x CL (pF) / Power (mW)	29.6456978
Large signal -	SR- (V/us) x CL (pF) / Power (mW)	29.6456978

1. Schematic

Fig. 1(a)

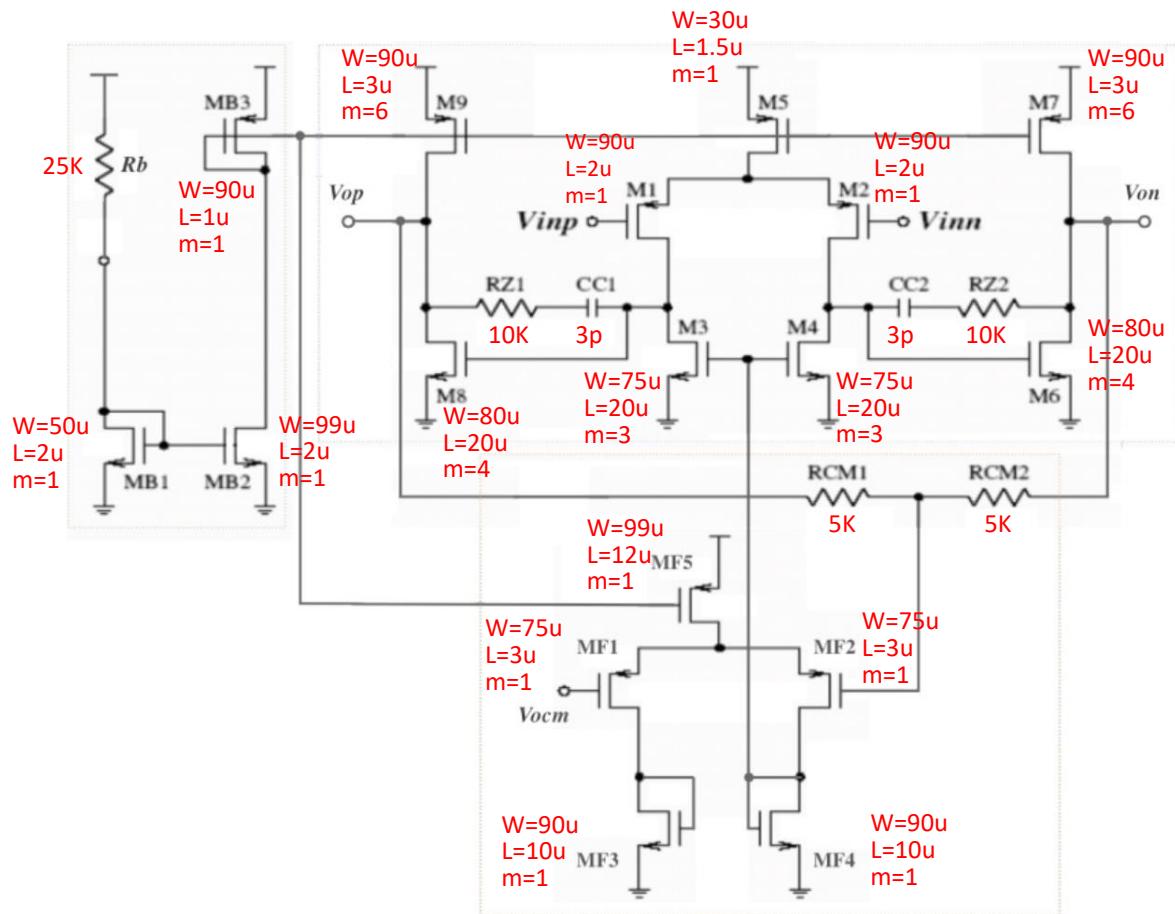
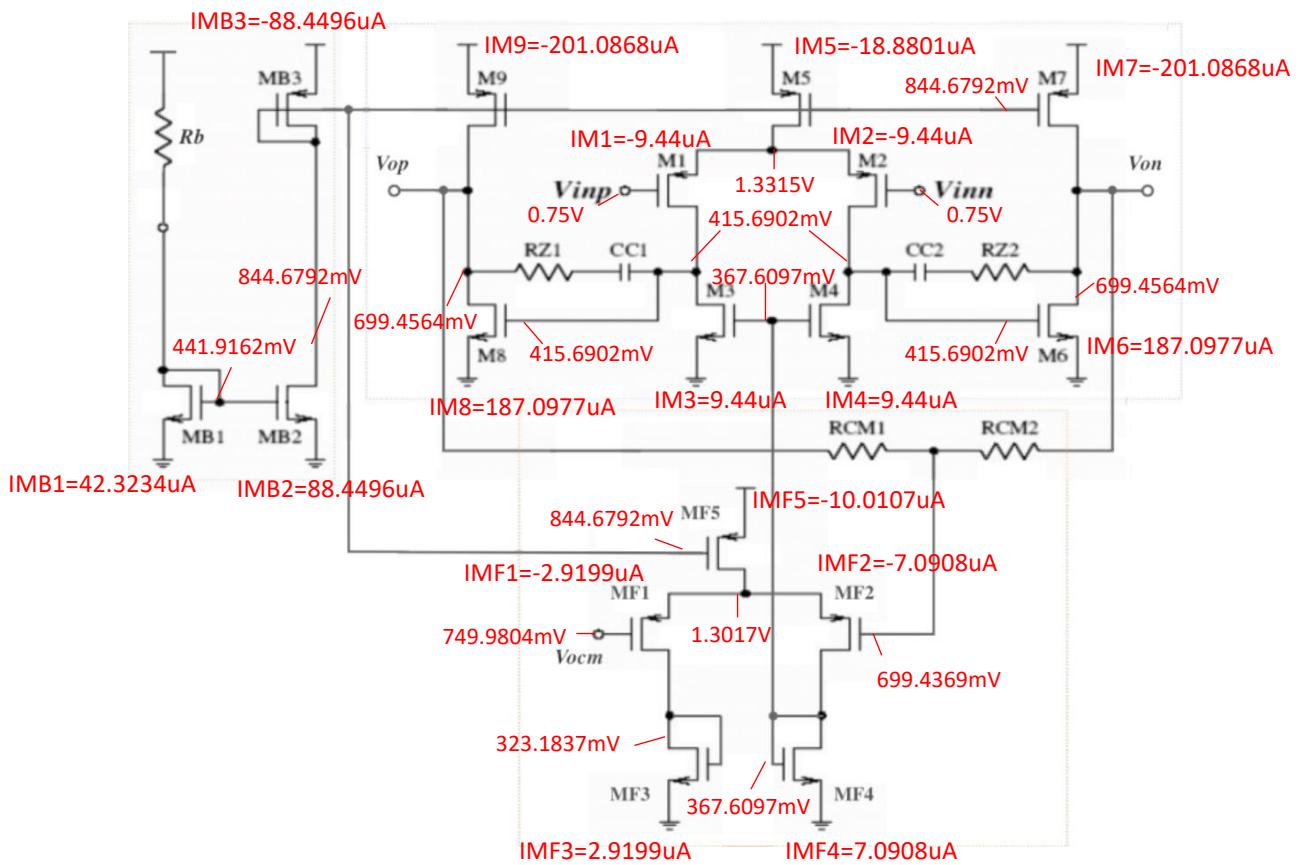


Fig. 1(b)



List. 1

subckt	xop	xop	xop	xop	xop	xop
element	1:mmb2	1:mmbl	1:mmf4	1:mmf3	1:mm6	1:mm8
model	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	88.4496u	42.3234u	7.0908u	2.9199u	187.0977u	187.0977u
ibs	-1.311e-20	-6.336e-21	-1.052e-21	-4.332e-22	-2.780e-20	-2.780e-20
ibd	-5.9586f	-1.5904f	-2.3599f	-2.0747f	-15.9879f	-15.9879f
vgs	441.9162m	441.9162m	367.6097m	323.1837m	415.6902m	415.6902m
vds	844.6792m	441.9162m	367.6097m	323.1837m	699.4564m	699.4564m
vbs	0.	0.	0.	0.	0.	0.
vth	346.3133m	348.4897m	315.9318m	316.0266m	347.0748m	347.0748m
vdsat	110.9965m	109.3885m	80.9108m	60.4261m	94.2430m	94.2430m
vod	95.6029m	93.4265m	51.6780m	7.1571m	68.6155m	68.6155m
beta	15.0589m	7.6056m	2.6760m	2.6699m	48.6160m	48.6160m
gam eff	507.4460m	507.4460m	507.4459m	507.4459m	507.4459m	507.4459m
gm	1.2742m	618.5352u	128.3280u	63.1970u	3.0822m	3.0822m
gds	10.4597u	5.4662u	462.1115n	221.7123n	25.0600u	25.0600u
gmb	257.2522u	125.9700u	26.4510u	13.1959u	629.3650u	629.3650u
cdtot	127.8162f	70.1972f	133.5276f	131.5084f	423.3494f	423.3494f
cgtot	1.2998p	656.3734f	5.3336p	4.0172p	4.0680p	4.0680p
cstot	1.3854p	698.6813f	5.3269p	3.5158p	4.2971p	4.2971p
cbtot	538.3148f	276.9022f	1.7810p	1.7639p	1.7528p	1.7528p
cgs	1.1488p	580.6219f	4.6492p	3.0319p	3.5478p	3.5478p
cgd	34.0732f	17.4997f	29.7877f	31.1768f	110.8665f	110.8665f
subckt	xop	xop	xop	xop	xop	xop
element	1:mm4	1:mm3	1:mm3	1:mm2	1:mmf1	1:mmf5
model	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	9.4400u	9.4400u	-88.4496u	-7.0908u	-2.9199u	-10.0107u
ibs	-1.404e-21	-1.404e-21	8.140e-21	659.4592a	659.4588a	9.204e-22
ibd	-6.6865f	-6.6865f	2.6097f	3.7662f	3.9140f	867.6997a
vgs	367.6097m	367.6097m	-655.3208m	-602.2631m	-551.7196m	-655.3208m
vds	415.6902m	415.6902m	-655.3208m	-934.1099m	-978.5359m	-198.2804m
vbs	0.	0.	0.	198.2804m	198.2804m	0.
vth	311.7750m	311.7750m	-494.5442m	-533.1427m	-533.1427m	-460.8440m
vdsat	82.6100m	82.6100m	-165.3849m	-99.2368m	-72.3808m	-179.9444m
vod	55.8347m	55.8347m	-160.7766m	-69.1204m	-18.5769m	-194.4768m
beta	3.3365m	3.3365m	6.4441m	1.7640m	1.7816m	590.5370u
gam eff	507.4459m	507.4459m	557.0846m	555.7078m	555.7078m	557.0847m
gm	167.8936u	167.8936u	902.5429u	111.7641u	56.4901u	85.2315u
gds	348.1357u	348.1357u	4.6029u	111.0648n	49.5404n	6.7234u
gmb	34.5885u	34.5885u	273.9939u	31.3884u	15.8521u	26.5862u
cdtot	339.0813f	339.0813f	103.3321f	79.8277f	79.2854f	849.1871f
cgtot	26.8595p	26.8595p	585.3235f	1.3300p	1.0769p	7.8750p
cstot	26.8772p	26.8772p	683.3184f	1.4394p	1.0591p	8.4638p
cbtot	8.4645p	8.4645p	330.4776f	546.5008f	537.1426f	2.7957p
cgs	23.5633p	23.5633p	512.5032f	1.1711p	845.6581f	6.9949p
cgd	74.5798f	74.5798f	32.4508f	26.9620f	26.9247f	363.6378f
subckt	xop	xop	xop	xop	xop	xop
element	1:mm7	1:mm9	1:mm2	1:mm5	1:mm1	
model	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1	
region	Saturati	Saturati	Saturati	Saturati	Saturati	
id	-201.0868u	-201.0868u	-9.4400u	-18.8801u	-9.4400u	
ibs	1.851e-20	1.851e-20	670.7132a	1.776e-21	670.7132a	
ibd	19.1280f	19.1280f	4.3180f	228.4969a	4.3180f	
vgs	-655.3208m	-655.3208m	-581.5761m	-655.3208m	-581.5761m	
vds	-800.5436m	-800.5436m	-915.8859m	-168.4239m	-915.8859m	
vbs	0.	0.	168.4239m	0.	168.4239m	
vth	-475.5182m	-475.5182m	-532.0459m	-488.2559m	-532.0459m	
vdsat	-172.2408m	-172.2408m	-88.7556m	-166.8696m	-88.7556m	
vod	-179.8026m	-179.8026m	-49.5303m	-167.0649m	-49.5303m	
beta	12.8343m	12.8343m	3.1983m	1.4206m	3.1983m	
gam eff	557.0847m	557.0847m	555.9068m	557.0846m	555.9068m	
gm	1.9026m	1.9026m	161.6726u	175.1145u	161.6726u	
gds	3.2042u	3.2042u	227.5158n	22.7288u	227.5158n	
gmb	588.5584u	588.5584u	45.7992u	54.1226u	45.7992u	
cdtot	607.1584f	607.1584f	96.3039f	64.8544f	96.3039f	
cgtot	10.3990p	10.3990p	1.0126p	300.0392f	1.0126p	
cstot	11.7486p	11.7486p	1.0836p	331.7614f	1.0836p	
cbtot	4.2957p	4.2957p	481.1134f	148.2432f	481.1134f	
cgs	9.4346p	9.4346p	859.8610f	260.3154f	859.8610f	
cgd	195.8408f	195.8408f	32.3203f	21.8073f	32.3203f	

2. Spice Code

```

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.param vdd=1.5V
.param vss=0V
.param vocm=0.75

*****
* Library Name: final
* Cell Name: final
* View Name: schematic
*****


.SUBCKT op vinp vinn vdd vss vop von vocm
*.PININFO Vinn:I Vinp:I Vocm:0 Von:0 Vop:0
CCc2 net13 net1 3p
CCc1 net7 net11 3p
RRb vdd net063 25K
RRCM2 net095 Von 5K
RRCM1 Vop net095 5K
RRZ2 net1 Von 10K
RRZ1 Vop net7 10K
MMB2 net23 net063 vss vss n_18 W=99u L=2u m=1
MMB1 net063 net063 vss vss n_18 W=50u L=2u m=1
MMF4 net19 net19 vss vss n_18 W=90u L=10u m=1
MMF3 net071 net071 vss vss n_18 W=90u L=10u m=1
MM6 Von net13 vss vss n_18 W=80u L=2u m=4
MM8 Vop net11 vss vss n_18 W=80u L=2u m=4
MM4 net13 net19 vss vss n_18 W=75u L=20u m=3
MM3 net11 net19 vss vss n_18 W=75u L=20u m=3
MMB3 net23 net23 vdd vdd p_18 W=90u L=1u m=1
MMF2 net19 net095 net0100 vdd p_18 W=75u L=3u m=1
MMF1 net071 Vocm net0100 vdd p_18 W=75u L=3u m=1
MMF5 net0100 net23 vdd vdd p_18 W=99u L=12u m=1
MM7 Von net23 vdd vdd p_18 W=90u L=3u m=6
MM9 Vop net23 vdd vdd p_18 W=90u L=3u m=6
MM2 net13 Vinn net32 vdd p_18 W=90u L=2u m=1
MM5 net32 net23 vdd vdd p_18 W=30u L=1.5u m=1
MM1 net11 Vinp net32 vdd p_18 W=90u L=2u m=1
.ENDS

```

3. Simulations

3.1 Open-loop differential mode AC response

Fig. 3.1(a)

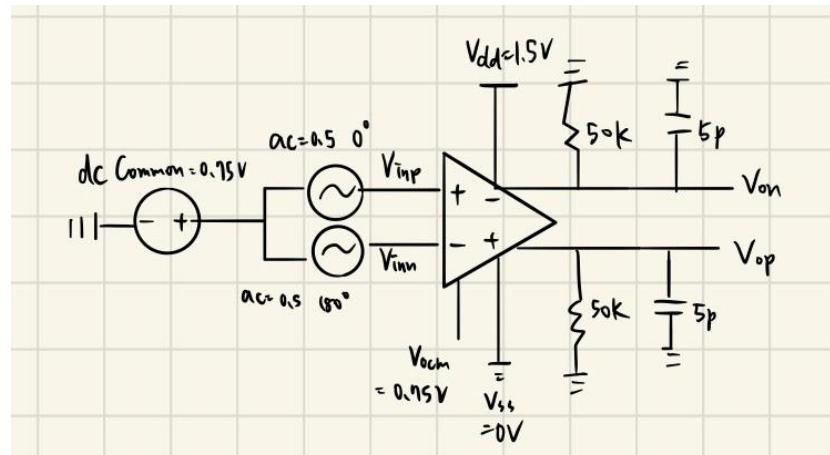
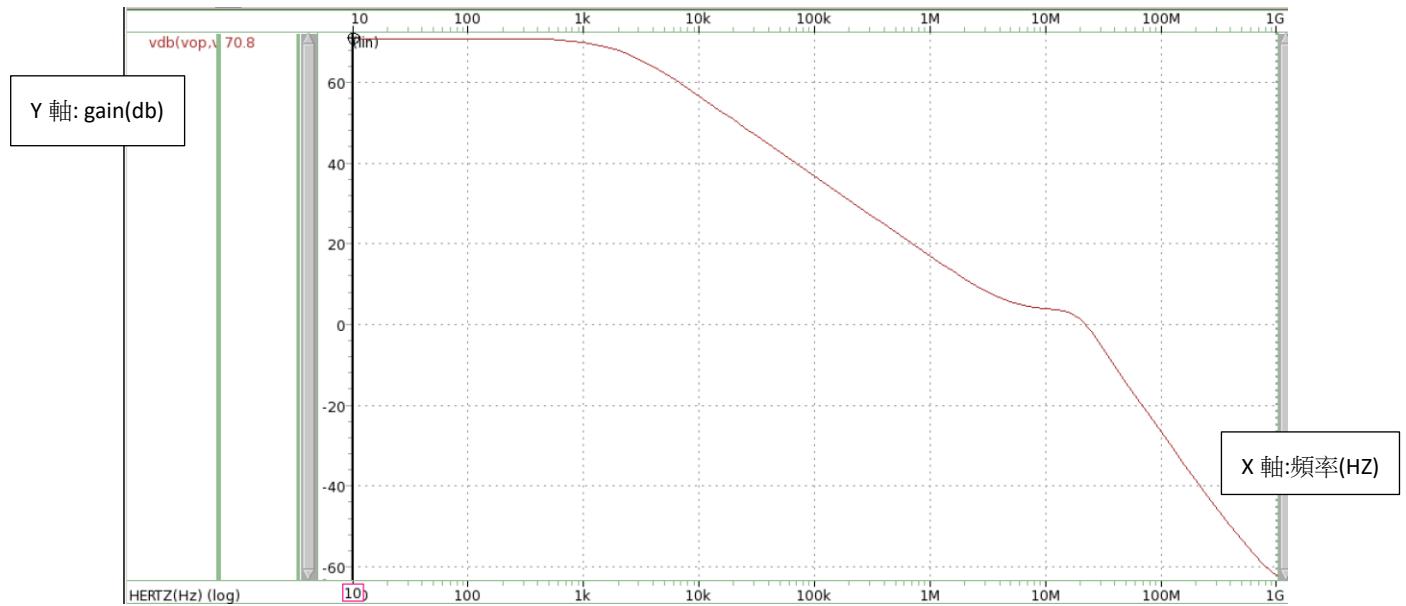
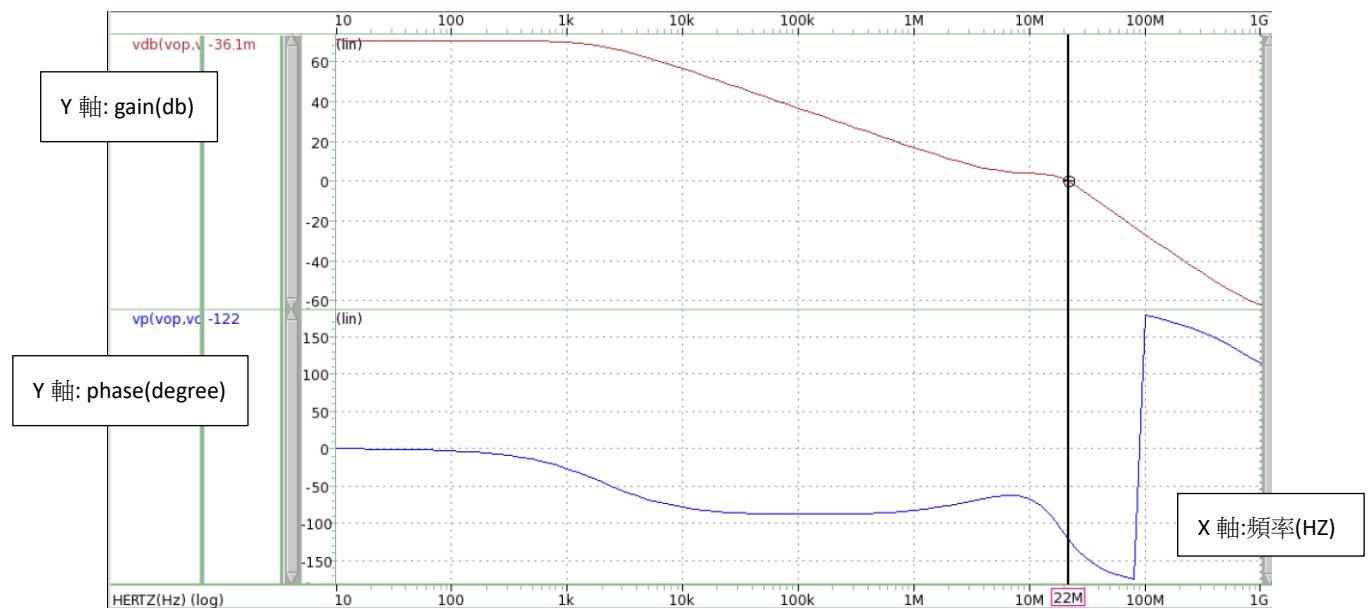


Fig. 3.1(b)

```
***** ac analysis tnom= 25.000 temp= 25.000 *****
dcgain_in_db= 70.8482 at= 10.0000
from= 10.0000 to= 1.0000g
dcgain= 3.4867k at= 10.0000
from= 10.0000 to= 1.0000g
unity_frequency= 22.1267x
phase=-121.6017
phase_margin= 58.3983
```



DC gain: 70.8 (dB)



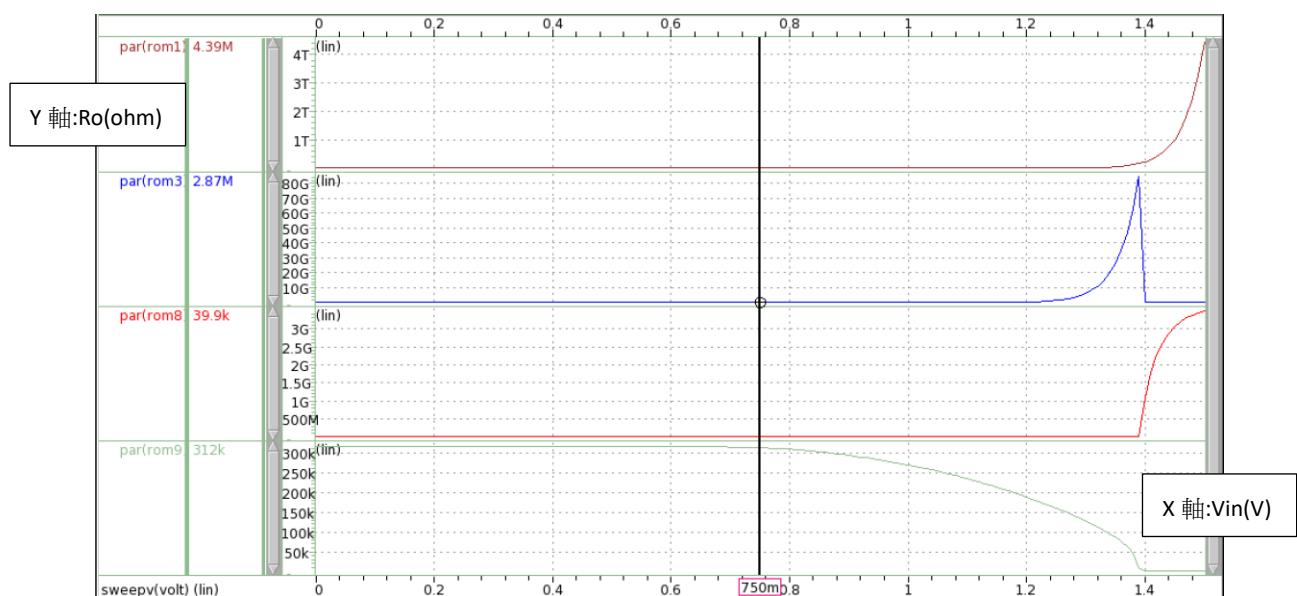
unity-gain frequency: 22M (Hz)
phase margin: 180-122 = 58 (degree)

Fig. 3.1(c)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-12.4715k	0.	-1.98489k	0.
-1.58944x	5.77692x	-252.966k	919.426k
-1.58944x	-5.77692x	-252.966k	-919.426k
-15.3011x	0.	-2.43524x	0.
-29.8741x	0.	-4.75460x	0.
-47.7248x	94.5977x	-7.59564x	15.0557x
-47.7248x	-94.5977x	-7.59564x	-15.0557x
-62.5768x	-100.781x	-9.95941x	-16.0398x
-62.5768x	100.781x	-9.95941x	16.0398x
-70.2542x	0.	-11.1813x	0.
-195.439x	0.	-31.1052x	0.
-334.973x	0.	-53.3127x	0.
-437.064x	0.	-69.5609x	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-1.54172x	-5.66930x	-245.372k	-902.298k
-1.54172x	5.66930x	-245.372k	902.298k
-1.73057x	5.63327x	-275.428k	896.562k
-1.73057x	-5.63327x	-275.428k	-896.562k
-15.3011x	0.	-2.43525x	0.
-29.8346x	5.46095k	-4.74832x	869.138
-29.8346x	-5.46095k	-4.74832x	-869.138
-34.5023x	0.	-5.49121x	0.
-48.2451x	95.4129x	-7.67845x	15.1854x
-48.2451x	-95.4129x	-7.67845x	-15.1854x
-48.3792x	-94.8913x	-7.69979x	-15.1024x
-48.3792x	94.8913x	-7.69979x	15.1024x
-70.3262x	-9.52626k	-11.1928x	-1.51615k
-70.3262x	9.52626k	-11.1928x	1.51615k
-189.925x	5.16862k	-30.2276x	822.612
-189.925x	-5.16862k	-30.2276x	-822.612
-334.969x	0.	-53.3120x	0.
-431.634x	19.3757k	-68.6968x	3.08374k
-431.634x	-19.3757k	-68.6968x	-3.08374k
2.65470g	0.	422.509x	0.
22.2844g	0.	3.54667g	0.

Dis. 3.1(d)



$$ro1=4.39M(\text{ohm}) \quad ro3=2.87M(\text{ohm}) \quad ro8=39.9k(\text{ohm}) \quad ro9=312k$$

$$DC\ gain = gm1(r_o1//r_o3)gm8(r_o8//r_o9//r_{load})$$

$$= 161.6726u \times \left(\frac{1}{\frac{1}{4.39M} + \frac{1}{2.87M}} \right) \times 3.0822m \times \left(\frac{1}{\frac{1}{39.9k} + \frac{1}{312k} + \frac{1}{50K}} \right)$$

$$= 1.7916 \times 10^4 = 85.064db$$

$$\begin{aligned} \text{pole1} &= \frac{1}{2\pi(r_{o1}//r_{o3})g_{m8}(r_{o8}//r_{o9}//R_{load})C_{c1}} \\ &= \frac{1}{2\pi\left(\frac{1}{4.39M} + \frac{1}{2.87M}\right)3.0822m\left(\frac{1}{39.9k} + \frac{1}{312k} + \frac{1}{50K}\right)3p} \\ &= 978.586(HZ) \\ \text{pole2} &= \frac{g_{m8}}{2\pi(C_{c1} + C_{load})} = \frac{3.0822m}{2\pi(3p + 5p)} = 6.132 \times 10^7(Hz) \\ \text{zero} &= \frac{1}{2\pi C_{c1}(\frac{1}{g_{m8}} - R_{z1})} = \frac{1}{2\pi \times 3p(\frac{1}{3.0822m} - 10k)} = 5.305 \times 10^7(Hz) \end{aligned}$$

.lis 檔中測得的 DC gain 為 70.8482db，把.lis 檔中相近的 pole 和 zero 抵銷後，pole1 是 1.98489k(HZ)，pole2 是 11.1813M(HZ)，zero 是 5.49121M(HZ)，與手算結果誤差都蠻大的，原因在於複雜的電路中會產生許多寄生電容，但是手算公式很簡化，無法計算到，且我的電路中有設計到幾個 MOS 有並聯的情況，造成實際上的 r_o 有誤差。測出的 pole 和 zero 有實部與虛部，而手算的部分忽略了虛部，所以 DC gain 與 pole 和 zero 都與手算結果有蠻大的差距。

3.2 Open-loop differential mode DC sweep

Fig. 3.2(a)

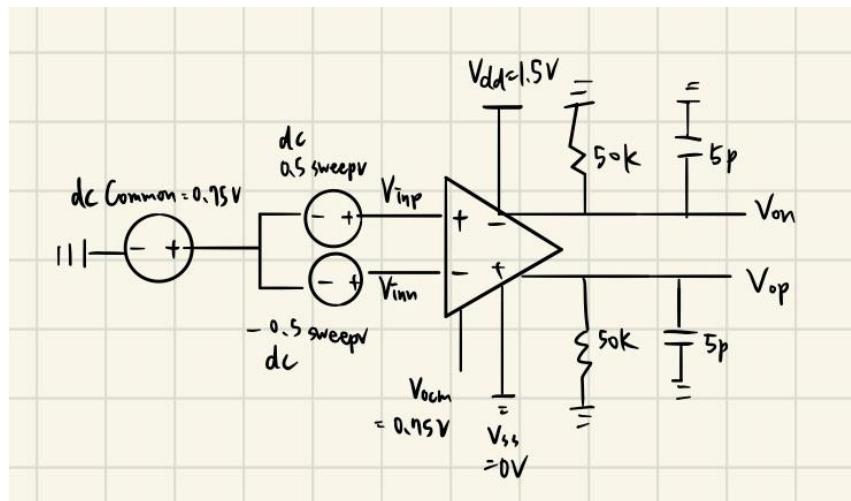
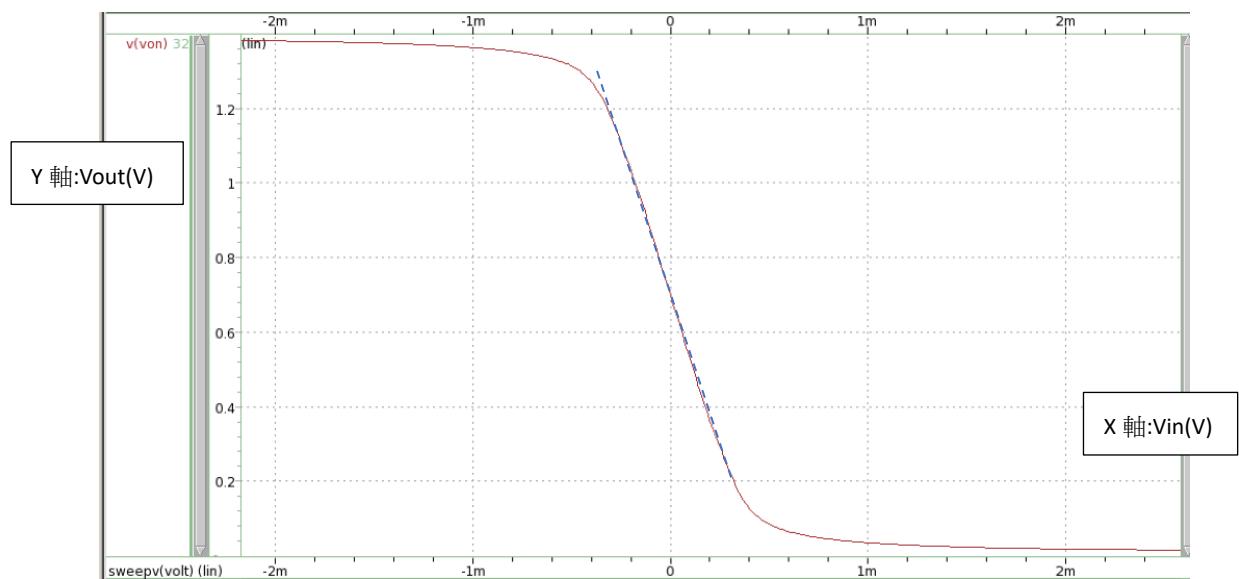
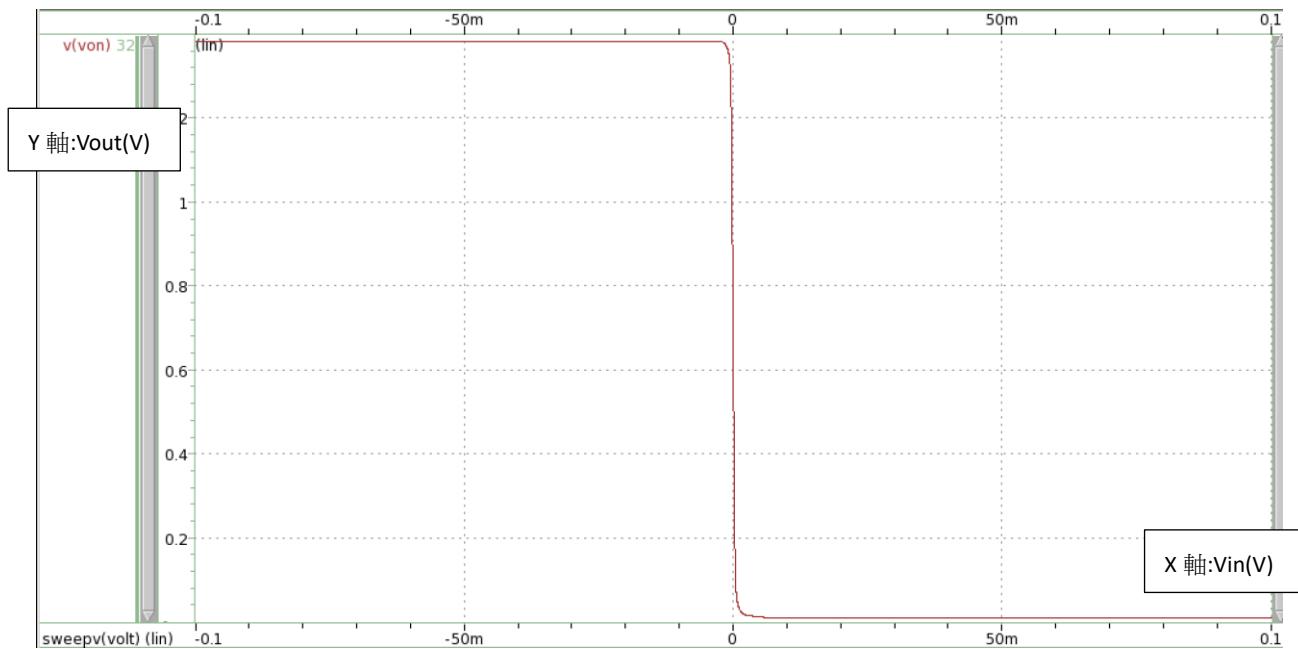


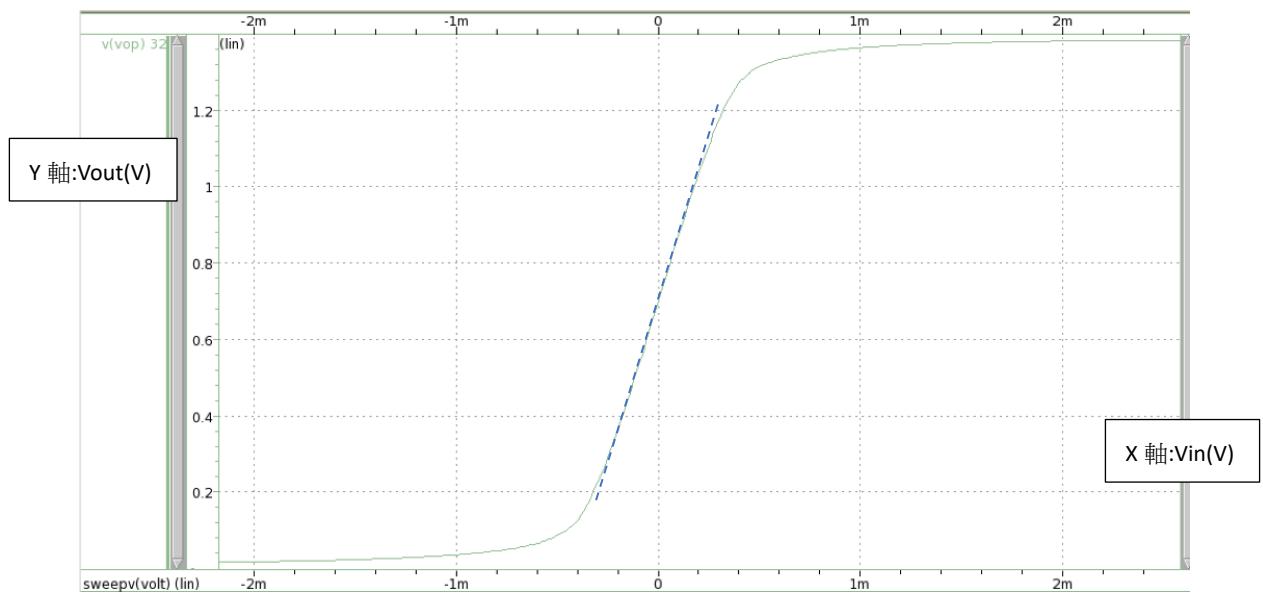
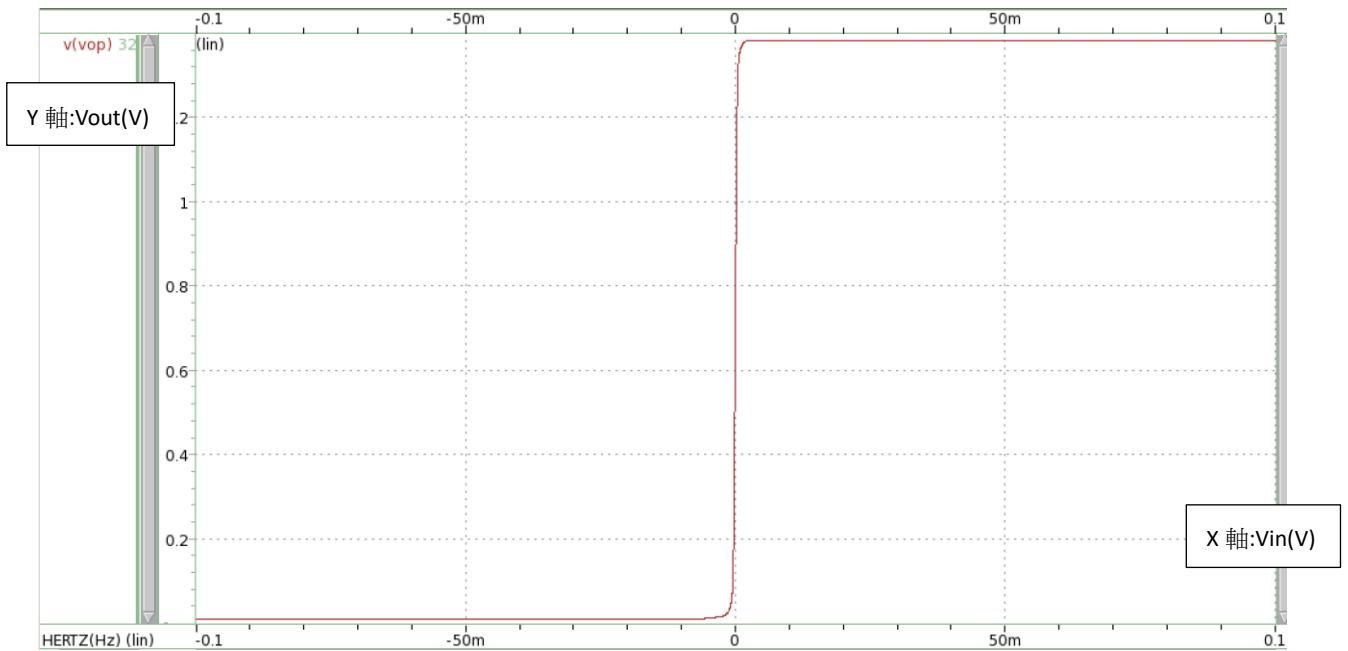
Fig. 3.2(b)

single-ended:

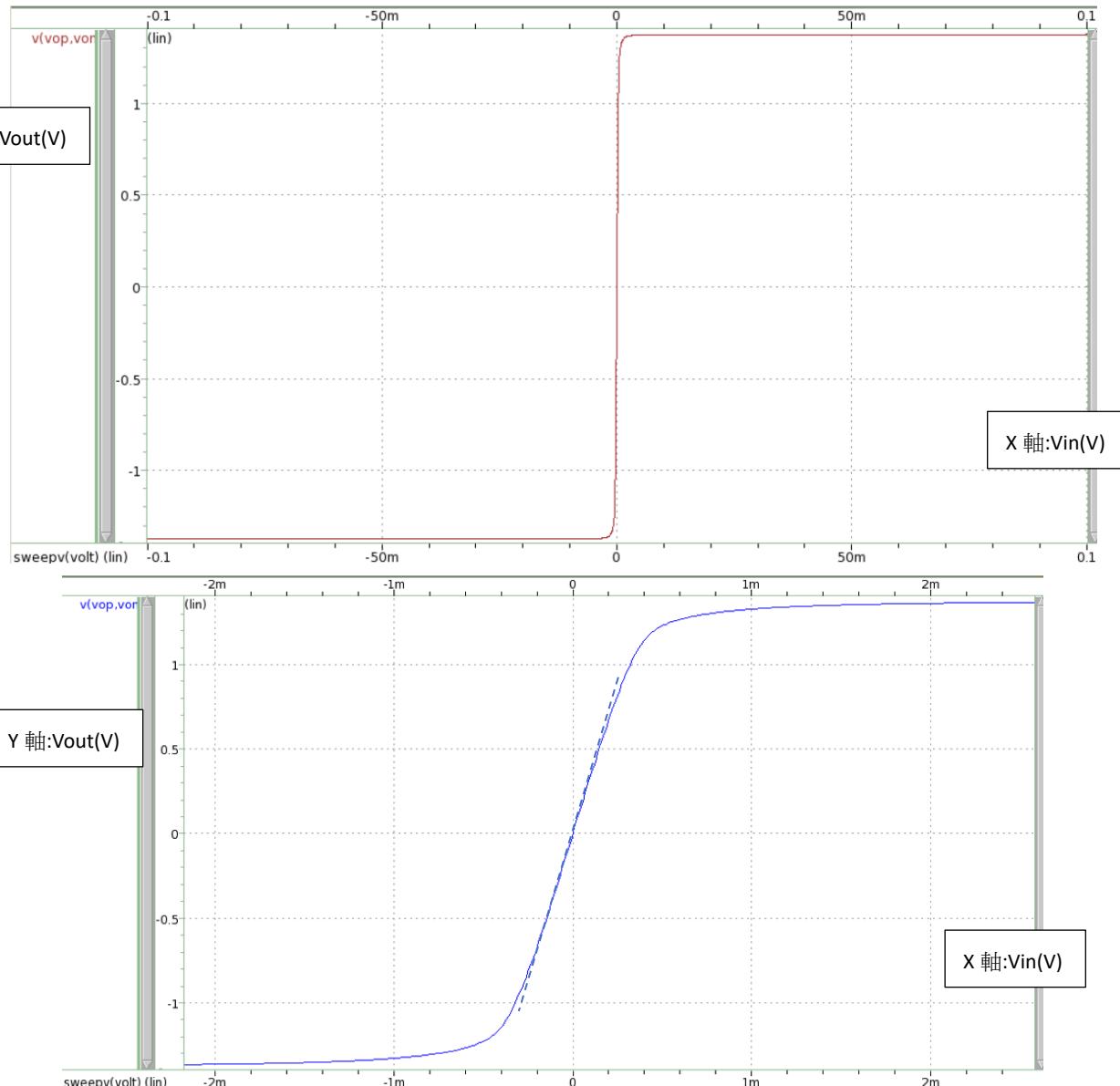
v_{on}:



Vop:



differential outputs:



Equation						Pass/Fail	
File	Equation	Specification		Result			
		Min	Max	Value	Mean		
D0:32_dc-dm_v2.sw0	slope(v(von),0)			-1.74k			
D0:32_dc-dm_v2.sw0	slope(v(vop),0)			1.74k			
D0:32_dc-dm_v2.sw0	slope(v(vop,von),0)			3.49k			

斜率:

single-ended:

-1.74k/1.74k

differential outputs:

3.49k

3.3 Open-loop common mode AC response

Fig. 3.3(a)

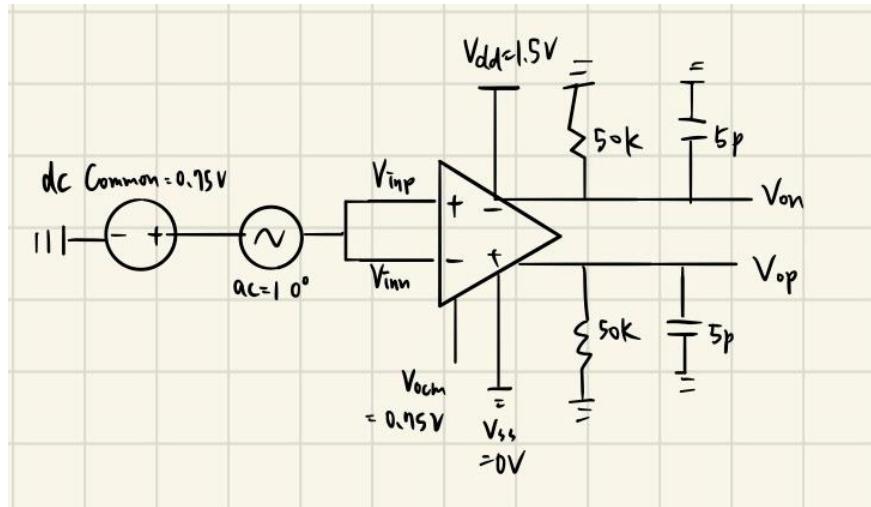
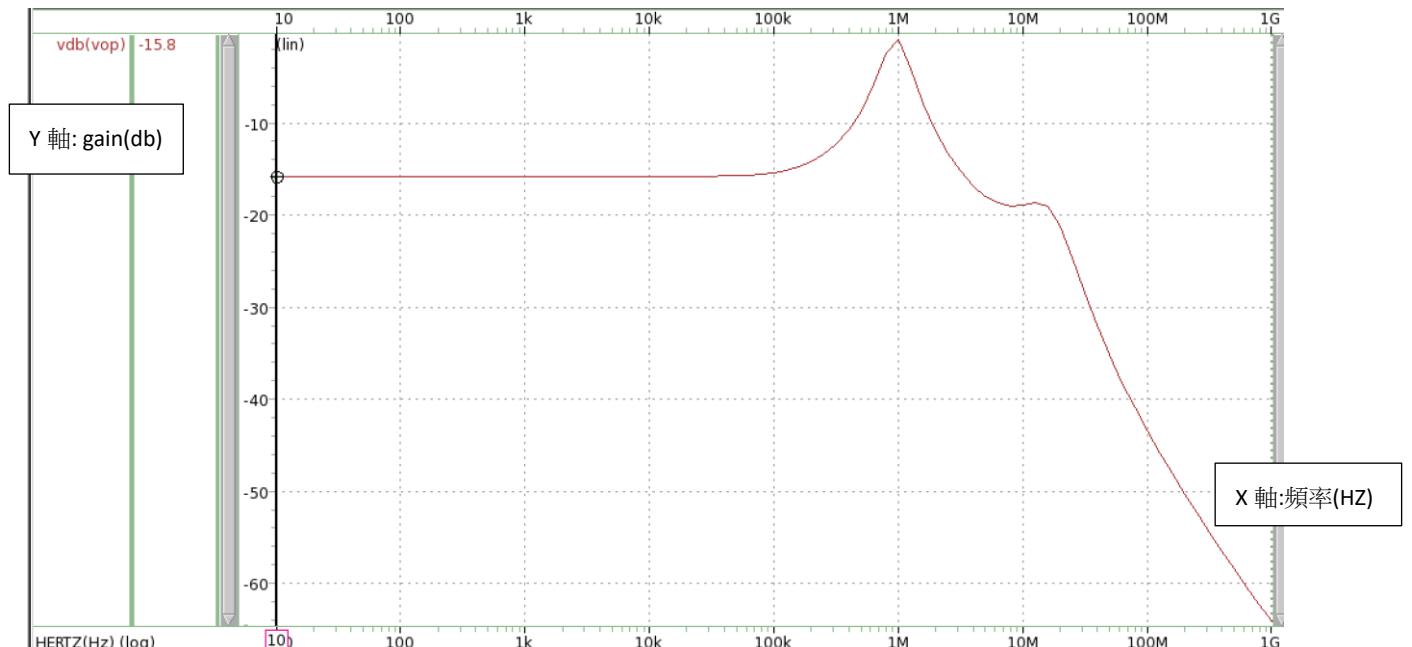
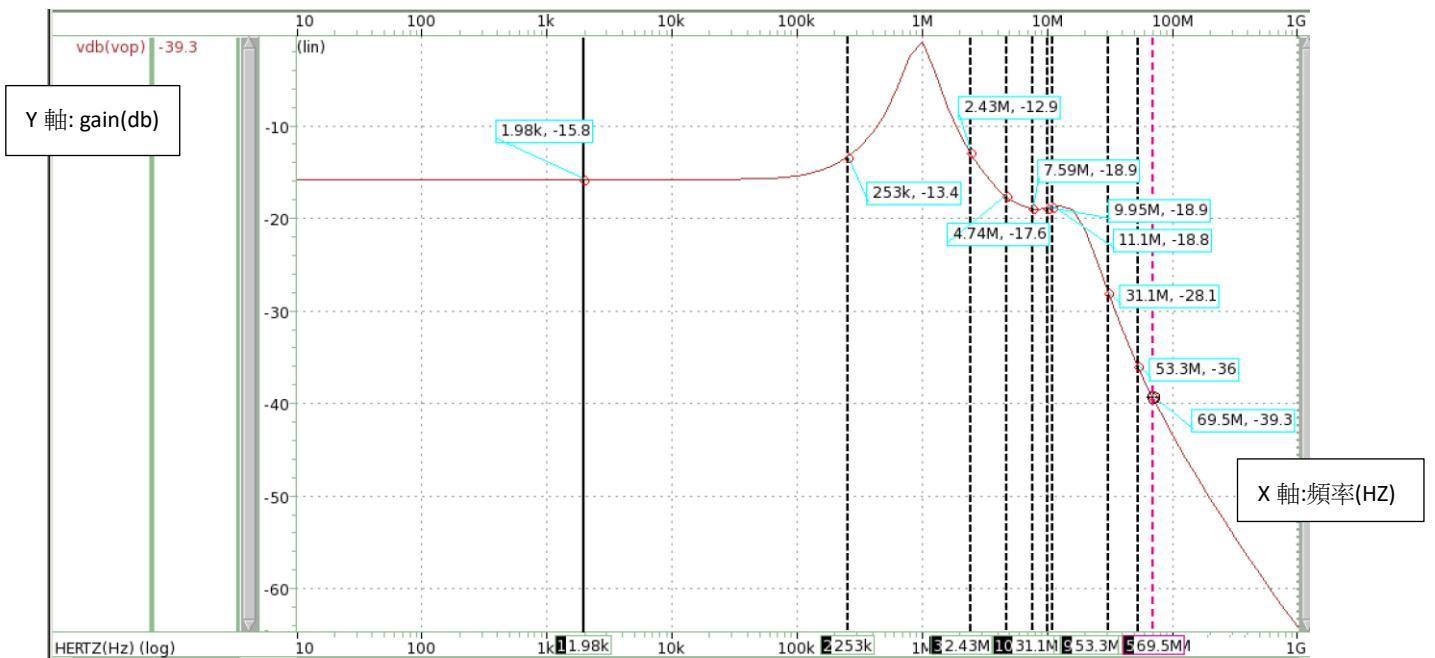


Fig. 3.3(b)



DC gain:-15.8(db)

Poles:



Zeros:

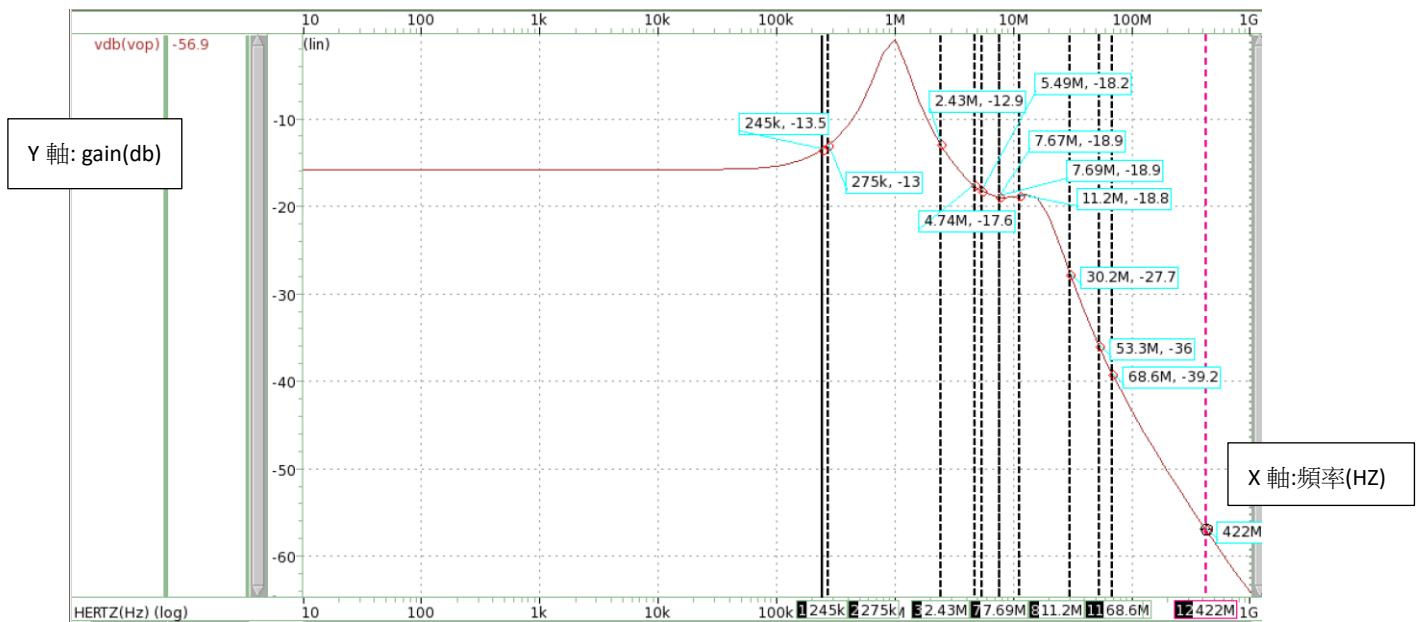


Fig. 3.3(c)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-12.4715k	0.	-1.98489k	0.
-1.58944x	5.77692x	-252.966k	919.426k
-1.58944x	-5.77692x	-252.966k	-919.426k
-15.3011x	0.	-2.43524x	0.
-29.8741x	0.	-4.75460x	0.
-47.7248x	94.5977x	-7.59564x	15.0557x
-47.7248x	-94.5977x	-7.59564x	-15.0557x
-62.5768x	-100.781x	-9.95941x	-16.0398x
-62.5768x	100.781x	-9.95941x	16.0398x
-70.2542x	0.	-11.1813x	0.
-195.439x	0.	-31.1052x	0.
-334.973x	0.	-53.3127x	0.
-437.064x	0.	-69.5609x	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-1.54172x	-5.66930x	-245.372k	-902.298k
-1.54172x	5.66930x	-245.372k	902.298k
-1.73057x	5.63327x	-275.428k	896.562k
-1.73057x	-5.63327x	-275.428k	-896.562k
-15.3011x	0.	-2.43525x	0.
-29.8346x	5.46095k	-4.74832x	869.138
-29.8346x	-5.46095k	-4.74832x	-869.138
-34.5023x	0.	-5.49121x	0.
-48.2451x	95.4129x	-7.67845x	15.1854x
-48.2451x	-95.4129x	-7.67845x	-15.1854x
-48.3792x	-94.8913x	-7.69979x	-15.1024x
-48.3792x	94.8913x	-7.69979x	15.1024x
-70.3262x	-9.52626k	-11.1928x	-1.51615k
-70.3262x	9.52626k	-11.1928x	1.51615k
-189.925x	5.16862k	-30.2276x	822.612
-189.925x	-5.16862k	-30.2276x	-822.612
-334.969x	0.	-53.3120x	0.
-431.634x	19.3757k	-68.6968x	3.08374k
-431.634x	-19.3757k	-68.6968x	-3.08374k
2.65470g	0.	422.509x	0.
22.2844g	0.	3.54667g	0.

Fig. 3.3(d)

Poles 和 zeros 與 3.1(d)測得的和手算公式都一模一樣，

$$ro1=4.39M(\text{ohm}) \quad ro3=2.87M(\text{ohm}) \quad ro8=39.9k(\text{ohm}) \quad ro9=312k$$

$$DC\ gain = gm1(ro1//ro3)gm8(ro8//ro9//rload)$$

$$\begin{aligned}
 &= 161.6726u \times \left(\frac{1}{\frac{1}{4.39M} + \frac{1}{2.87M}} \right) \times 3.0822m \times \left(\frac{1}{\frac{1}{39.9k} + \frac{1}{312k} + \frac{1}{50K}} \right) \\
 &= 1.7916 \times 10^4 = 85.064db
 \end{aligned}$$

$$\begin{aligned}
\text{pole1} &= \frac{1}{2\pi(r_{o1}/r_{o3})g_{m8}(r_{o8}/r_{o9}/R_{load})C_{c1}} \\
&= \frac{1}{2\pi\left(\frac{1}{\frac{1}{4.39M} + \frac{1}{2.87M}}\right)3.0822m\left(\frac{1}{\frac{1}{39.9k} + \frac{1}{312k} + \frac{1}{50K}}\right)^{3p}} \\
&= 978.586(\text{Hz}) \\
\text{pole2} &= \frac{g_{m8}}{2\pi(C_{c1} + C_{load})} = \frac{3.0822m}{2\pi(3p + 5p)} = 6.132 \times 10^7(\text{Hz}) \\
\text{zero} &= \frac{1}{2\pi C_{c1}(\frac{1}{g_{m8}} - R_{z1})} = \frac{1}{2\pi \times 3p(\frac{1}{3.0822m} - 10k)} = 5.305 \times 10^7(\text{Hz})
\end{aligned}$$

.lis 檔中測得的 DC gain 為 70.8482db，把.lis 檔中相近的 pole 和 zero 抵銷後，pole1 是 1.98489k(HZ)，pole2 是 11.1813M(HZ)，zero 是 5.49121M(HZ)，與手算結果誤差都蠻大的，原因在於複雜的電路中會產生許多寄生電容，但是手算公式很簡化，無法計算到，且我的電路中有設計到幾個 MOS 有並聯的情況，造成實際上的 r_o 有誤差。測出的 pole 和 zero 有實部與虛部，而手算的部分忽略了虛部，所以 DC gain 與 pole 和 zero 都與手算結果有蠻大的差距。

3.4 Open-loop common mode DC sweep

Fig. 3.4(a)

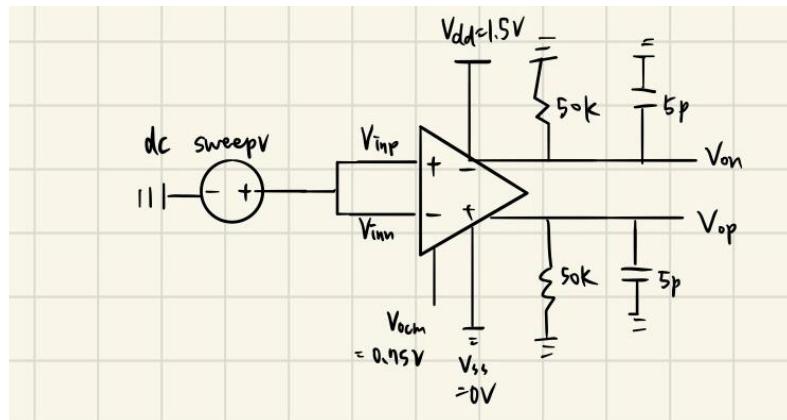
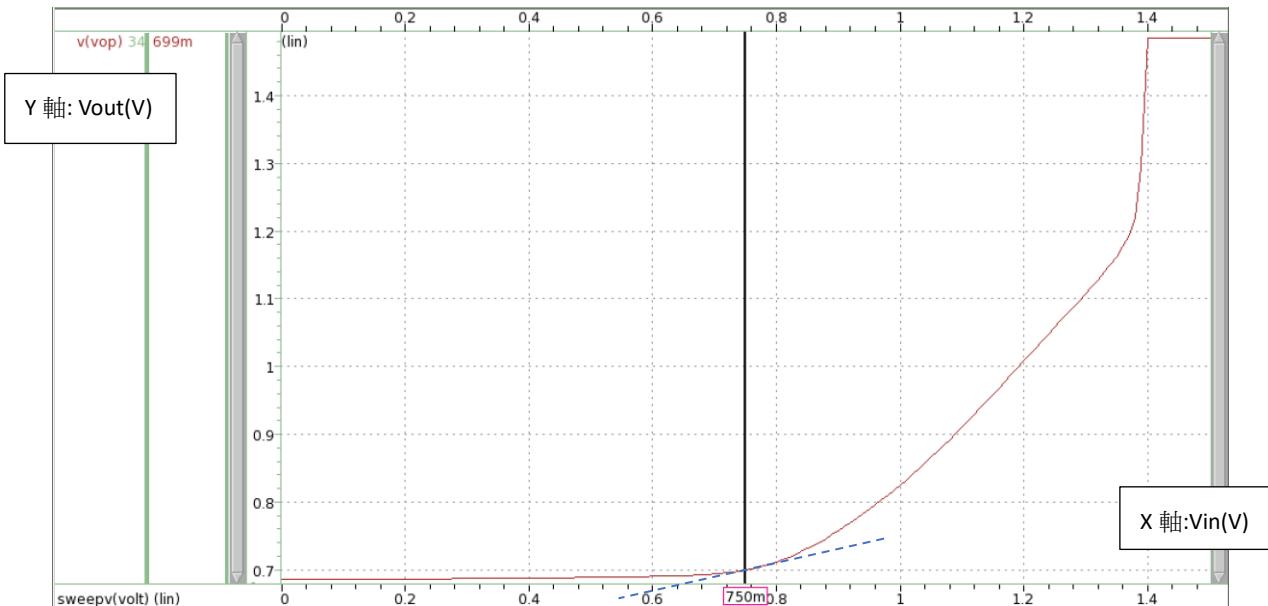


Fig. 3.4(b)



Equation						Pass/Fail	
File	Equation	Specification		Result			
		Min	Max	Value	Mean		
D0:34_dc-cm.sw0	slope(v(vop),0.75)			149m			

在 0.75V 時斜率為 $149\text{m} = -16.5\text{dB}$ ，與 3.3 求得的 DC Gain: -15.8dB ，誤差為

$$\frac{-16.5 - (-15.8)}{-16.5} \times 100\% = 4.2\%$$

兩值相近

3.5 Open-loop power supply+ AC response

Fig. 3.5(a)

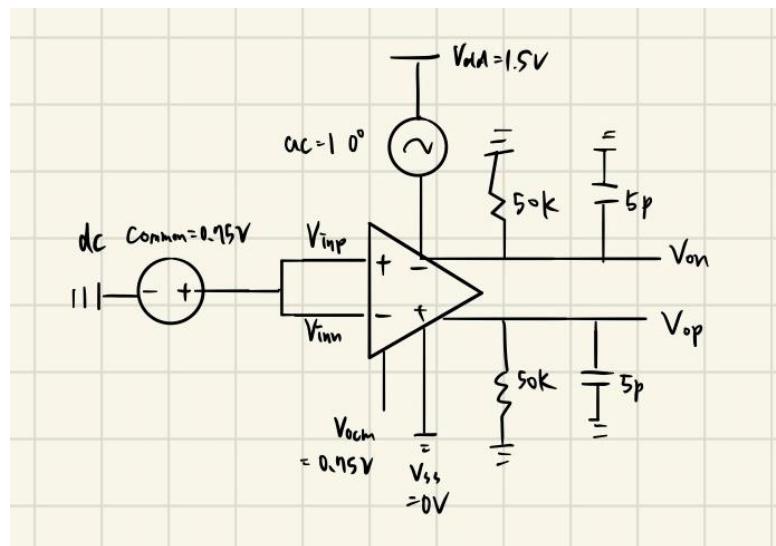
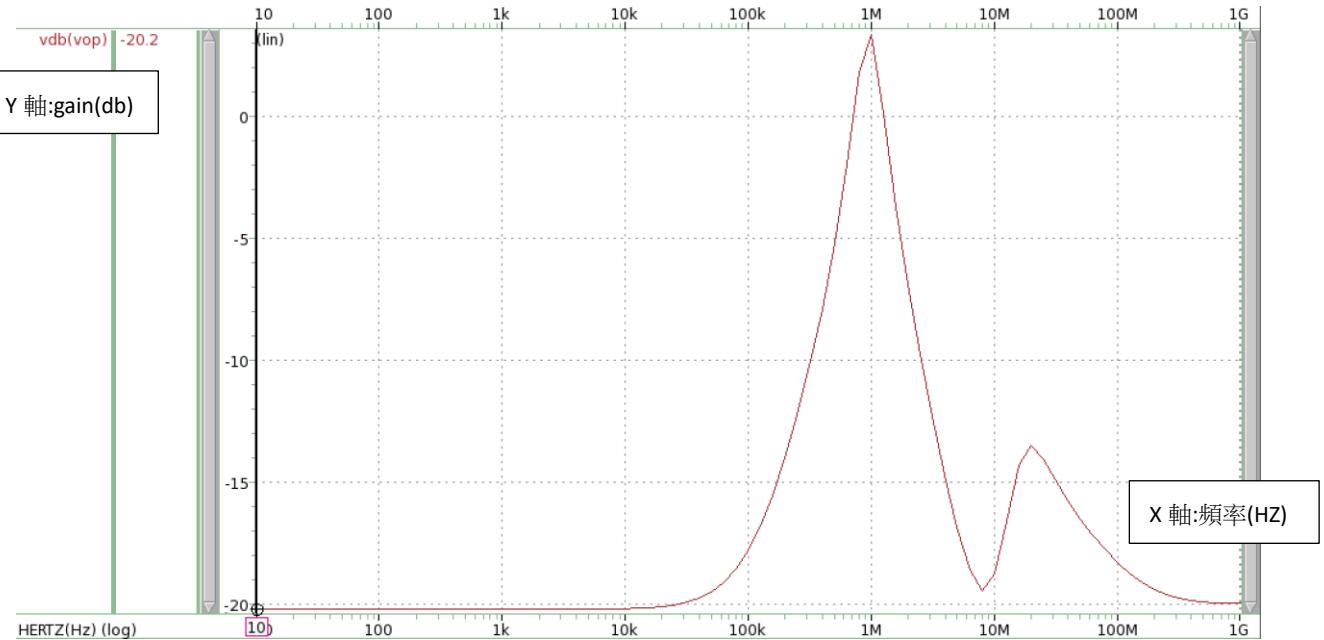


Fig. 3.5(b)



DC gain: -20.2dB

3.6 Open-loop power supply- AC response

Fig. 3.6(a)

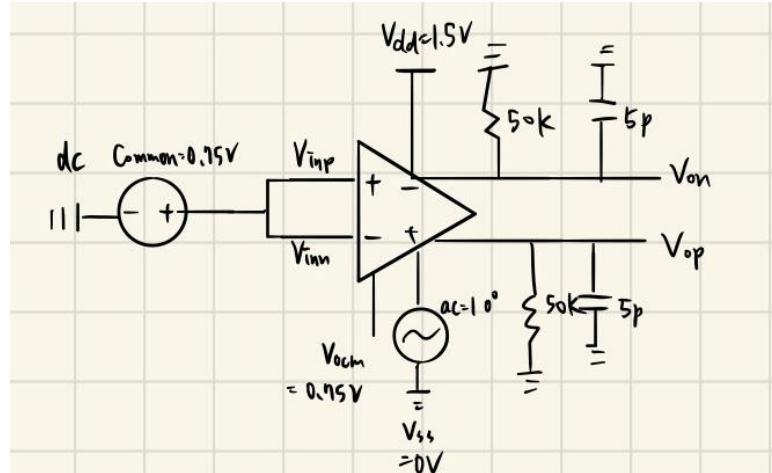
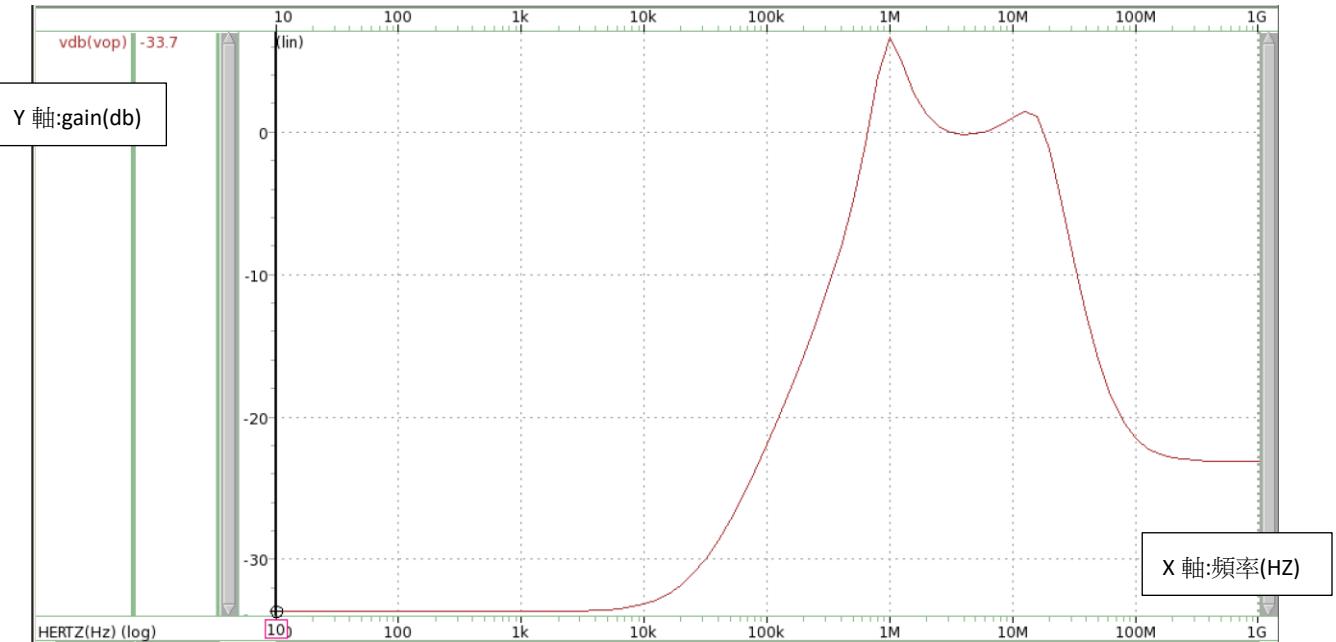
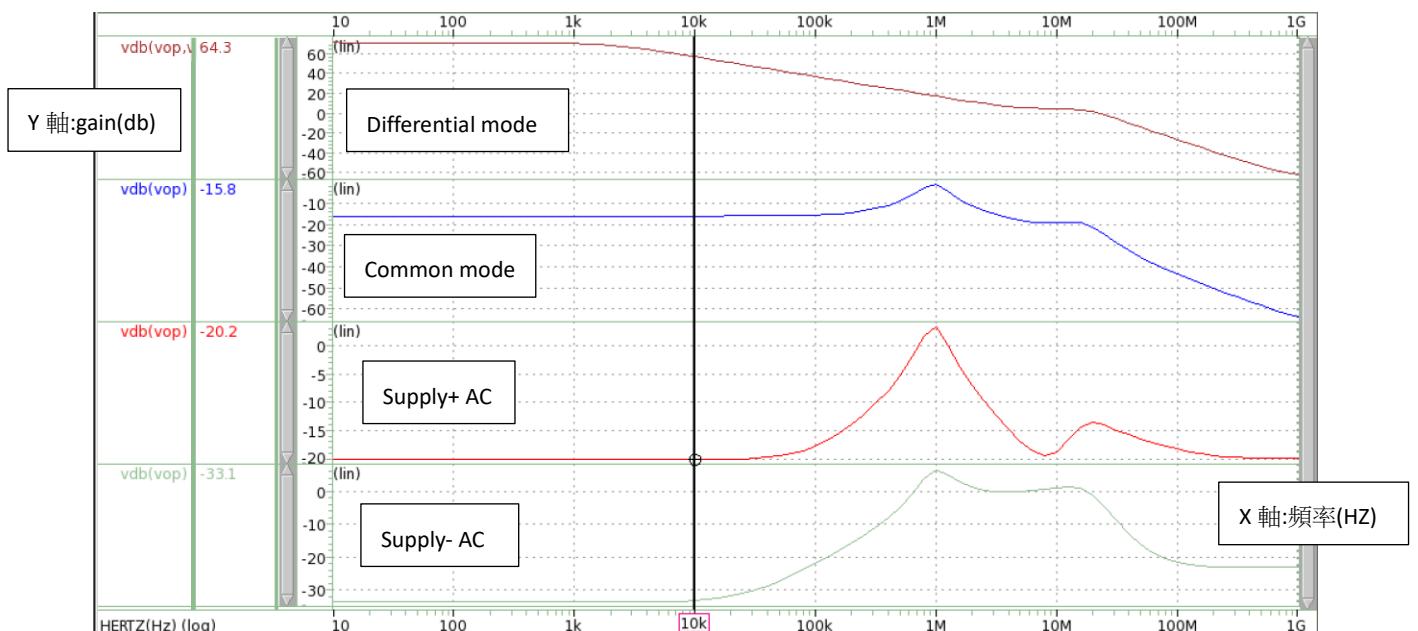


Fig. 3.6(b)



DC gain: -33.7dB

CMRR、PSRR+、PSRR-計算：



$$CMRR = 64.3\text{dB} + 15.8\text{dB} = 80.1\text{dB}$$

$$PSRR_+ = 64.3\text{dB} + 20.2\text{dB} = 84.5\text{dB}$$

$$PSRR_{-} = 64.3\text{dB} + 33.1\text{dB} = 97.4\text{dB}$$

3.7 Closed-loop differential mode AC response

Fig. 3.7(a)

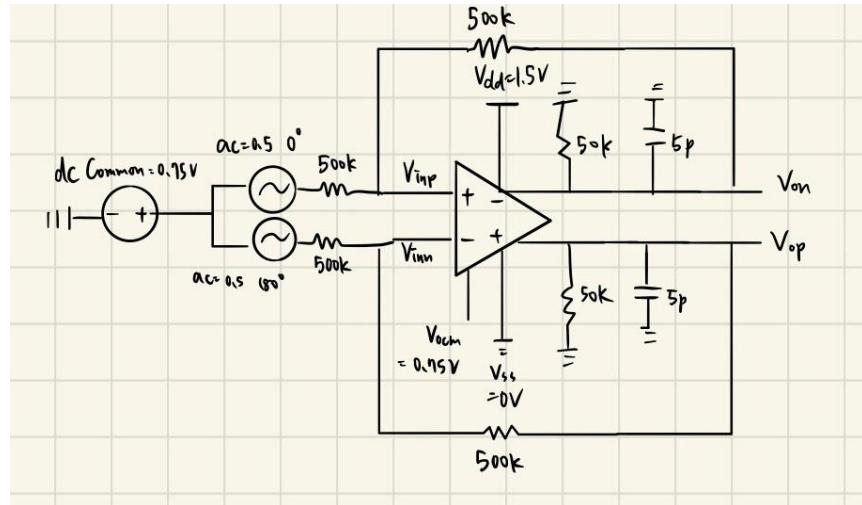
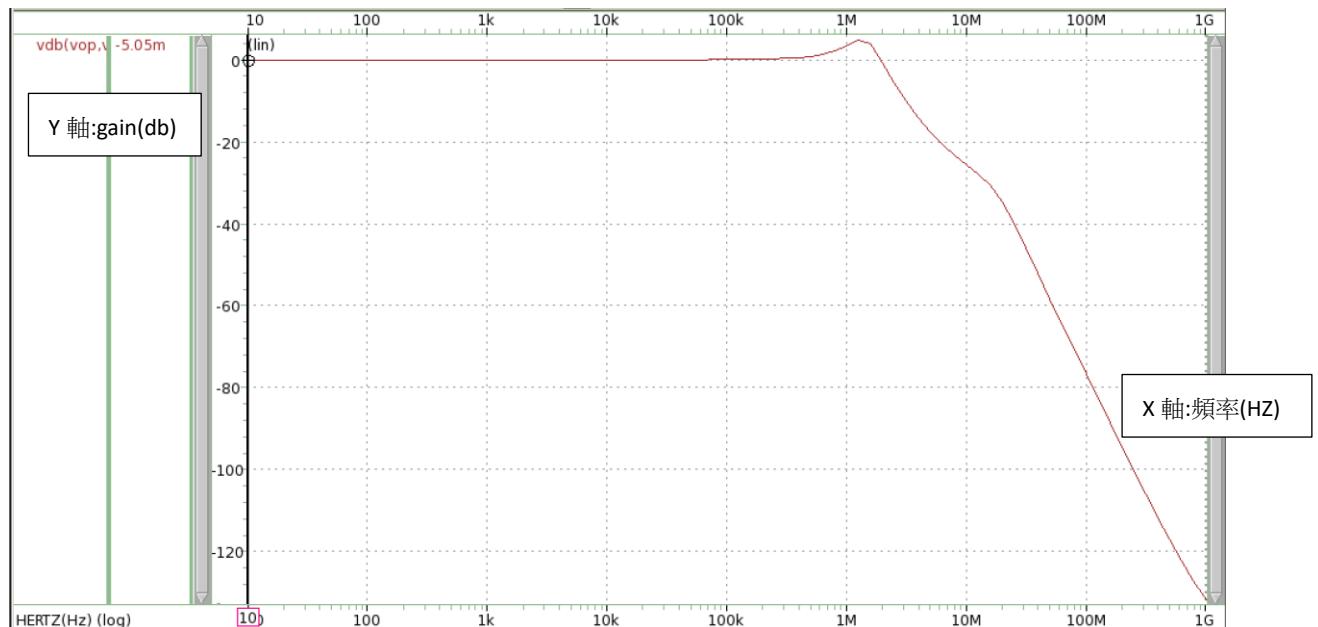
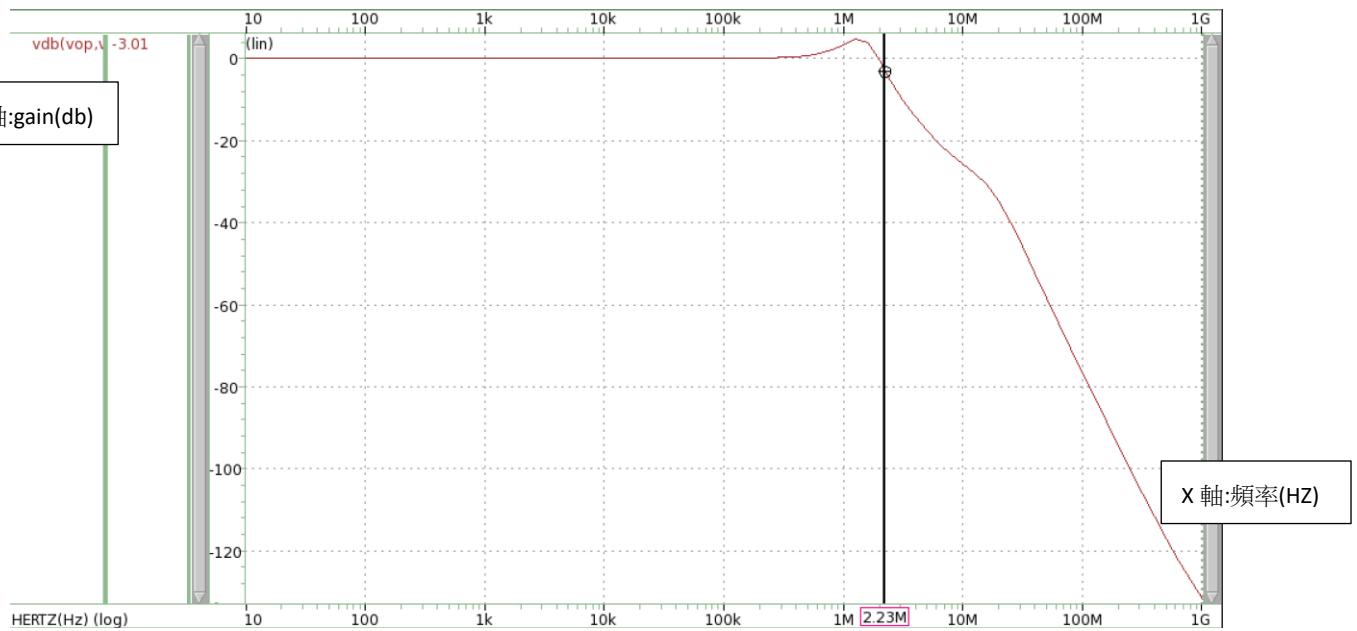


Fig. 3.7(b)



DC gain: -5.05m(dB)



$$-3\text{dB freq} = 2.23\text{M(HZ)}$$

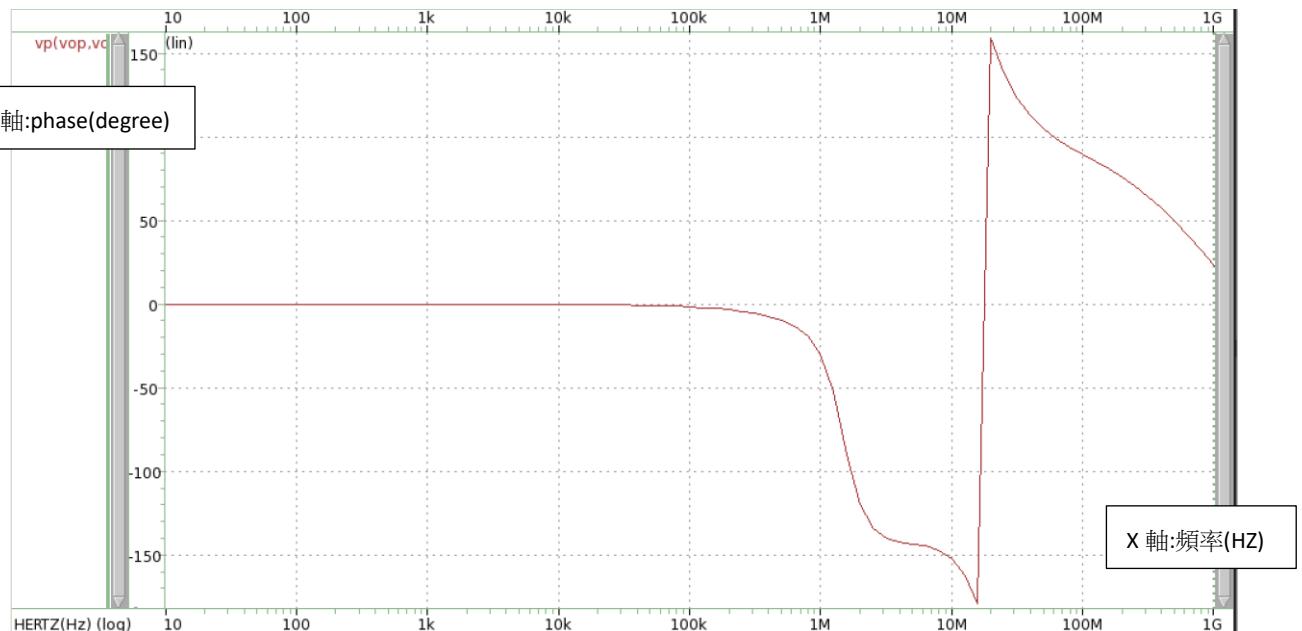


Fig. 3.7(c)

node	=voltage	node	=voltage	node	=voltage
+0:test1	= 750.0000m	0:test2	= 750.0000m	0:vdd	= 1.5000
+0:vinn	= 722.9648m	0:vinp	= 722.9648m	0:vocm	= 750.0000m
+0:von	= 695.9296m	0:vop	= 695.9296m	0:vss	= 0.
+1:net0100	= 1.2999	1:net063	= 441.9162m	1:net071	= 321.1429m
+1:net095	= 695.9296m	1:net1	= 695.9296m	1:net11	= 415.7630m
+1:net13	= 415.7630m	1:net19	= 368.6795m	1:net23	= 844.6792m
+1:net32	= 1.3114	1:net7	= 695.9296m		

$$\frac{von}{vinn} = \frac{vop}{vinp} = \frac{695.9296m}{722.9648m} = 0.962 = -0.33dB$$

b 小題的 DC gain 為 -5.05m(dB) ，兩者都相當接近 0，結果合理。

Fig. 3.7(d)

**** small-signal transfer characteristics

$v(v_{op}, v_{on})/v_{inp}$	=	999.4192m
input resistance at v_{inp}	=	679.0669k
output resistance at $v(v_{op}, v_{on})$	=	4.6417

Fig. 3.7(e)

```
***** ac analysis tnom= 25.000 temp= 25.000 *****
dcgain_in_db= 70.8482 at= 10.0000
from= 10.0000 to= 1.0000g
dcgain= 3.4867k at= 10.0000
from= 10.0000 to= 1.0000g
unity_frequency= 22.1267x
phase=-121.6017
phase_margin= 58.3983
```

$$\text{Feedback 的 } k = \frac{Rcm2}{Rcm1+Rcm2} = \frac{5K}{5k+5K} = 0.5$$

open loop gain: $A=3486.7(V/V)$

$$\text{closed loop gain} = \frac{1-k}{k} \times \frac{1}{1 + \frac{1}{4K}} = \frac{1-0.5}{0.5} \times \frac{1}{1 + \frac{1}{\frac{3486.7 \times 0.5}{10}}} = 0.99943(V/V)$$

與.lis 檔的 gain: 999.4192m(V/V) 非常接近

3.8 Closed-loop differential mode DC sweep

Fig. 3.8(a)

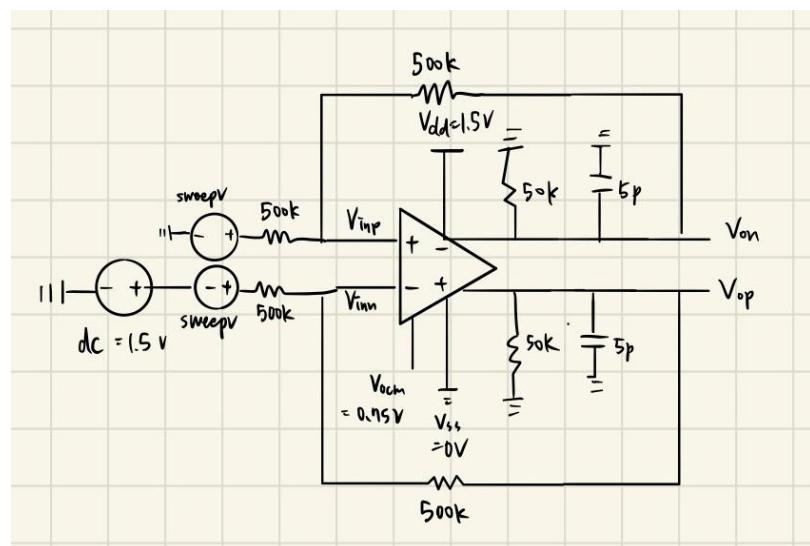
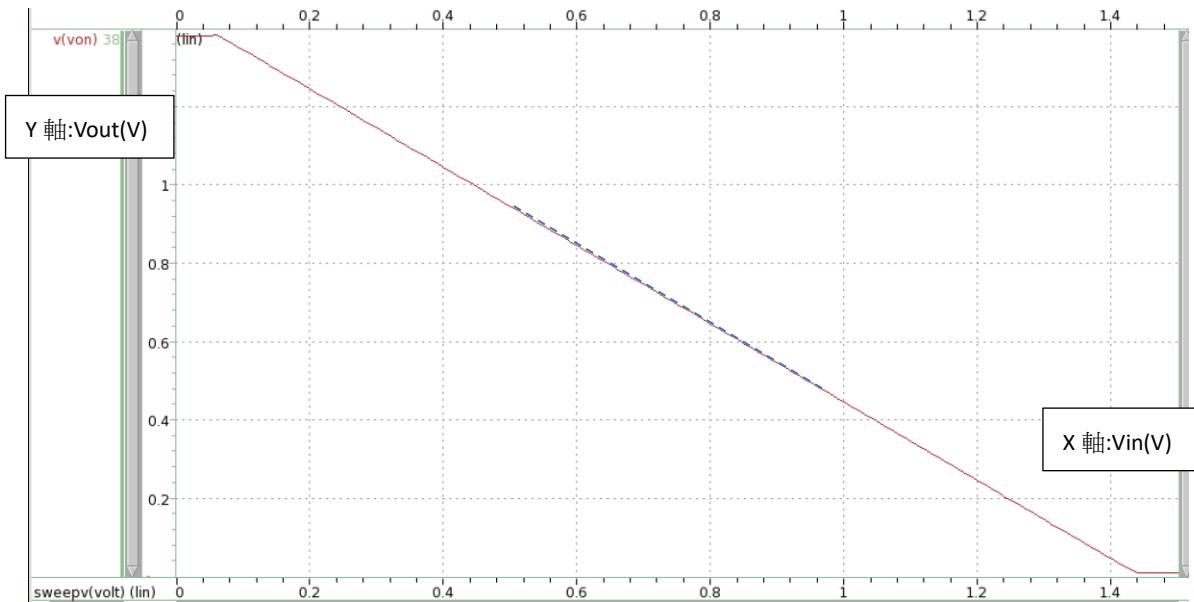


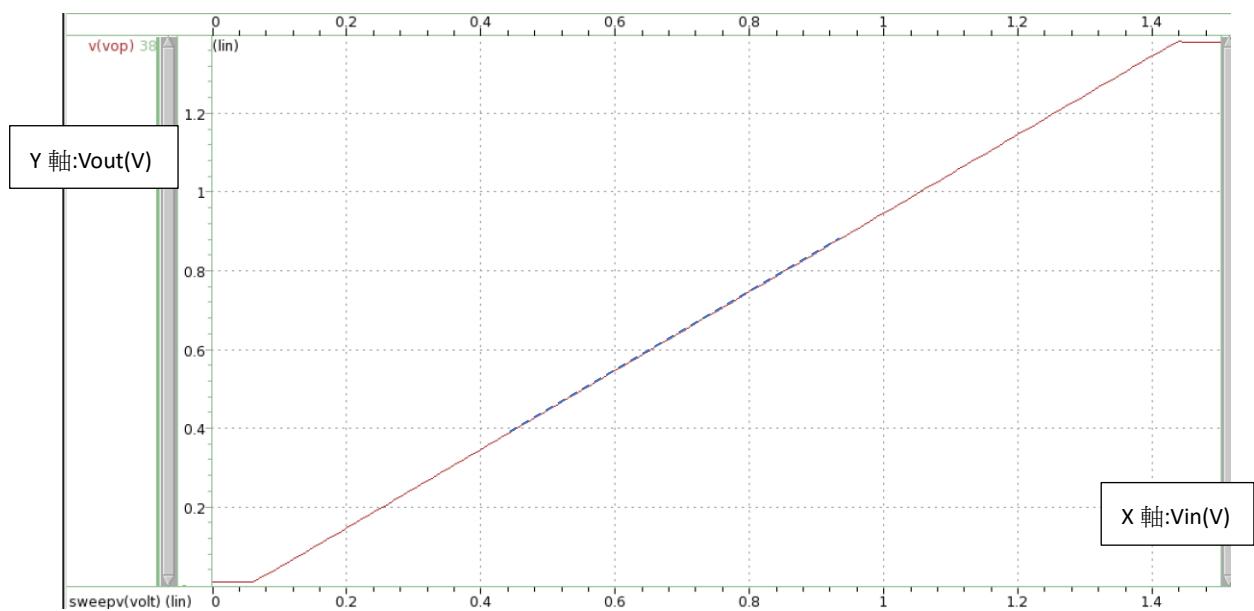
Fig. 3.8(b)

single-ended:

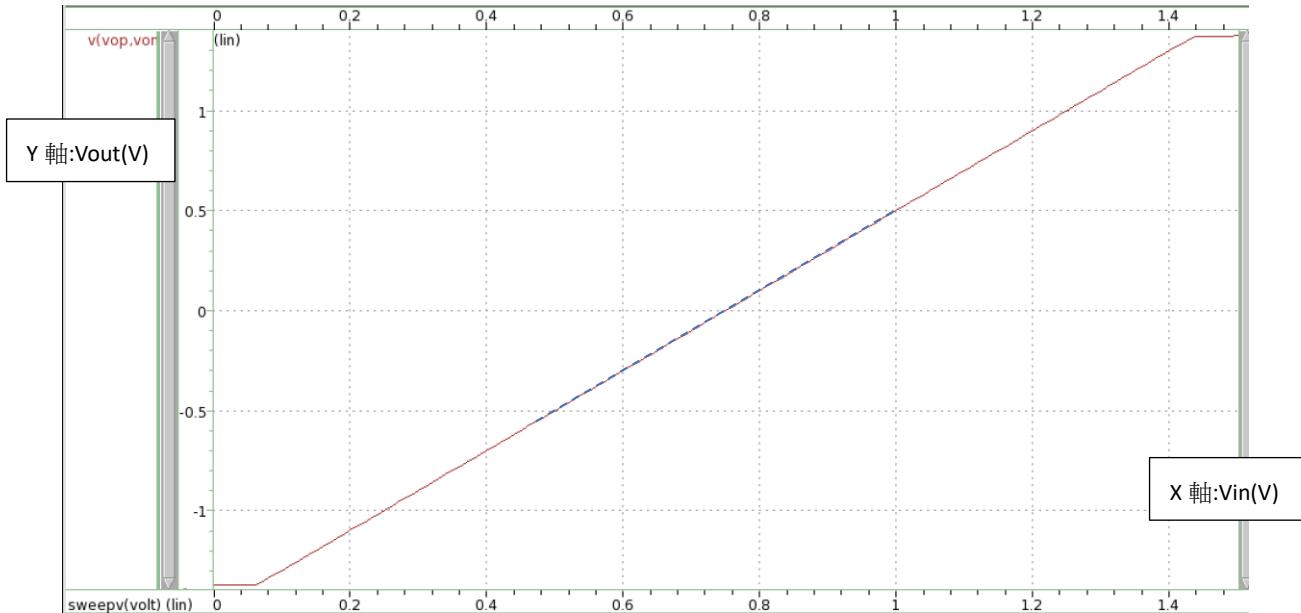
v_{on}:



V_{op} :



differential outputs:



Equation						
File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:38_closed-dc_dm.sw0	slope(v(von),0.75)			-999m		
D0:38_closed-dc_dm.sw0	slope(v(vop),0.75)			999m		
D0:38_closed-dc_dm.sw0	slope(v(vop,von),0.75)			2		

斜率:

single-ended:

-999m/999m

differential outputs:

2

dc response 的 differential outputs 斜率是 2，dc sweep 是一端 input vinp 掃 'supplyn+sweepv'，另一端 vinn 掃 'supplyp-sweepv'，因此 differential outputs 會是由兩倍的 vin 影響，除 2 後就與 ac response 的 dc gain : 1 相同。

3.9 Closed-loop step+ response

Fig. 3.9(a)

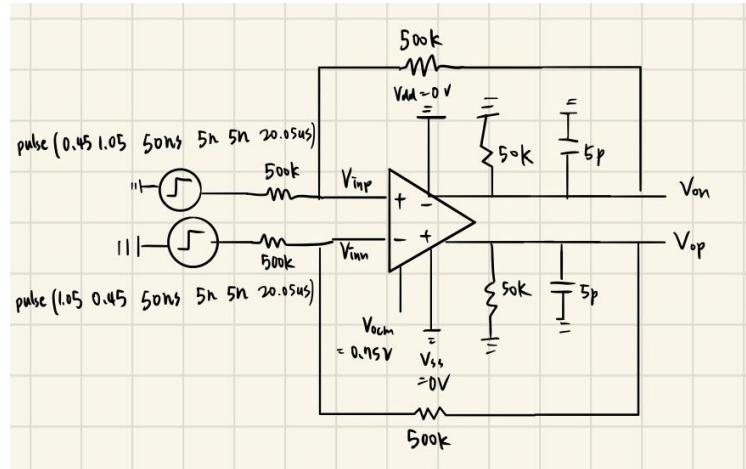
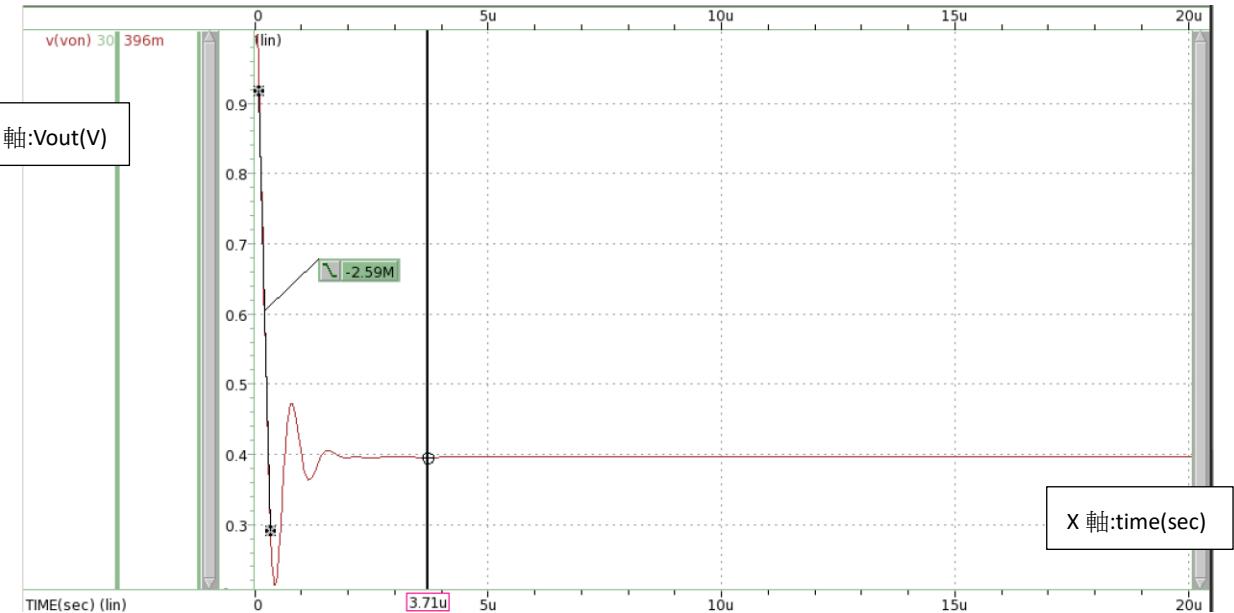


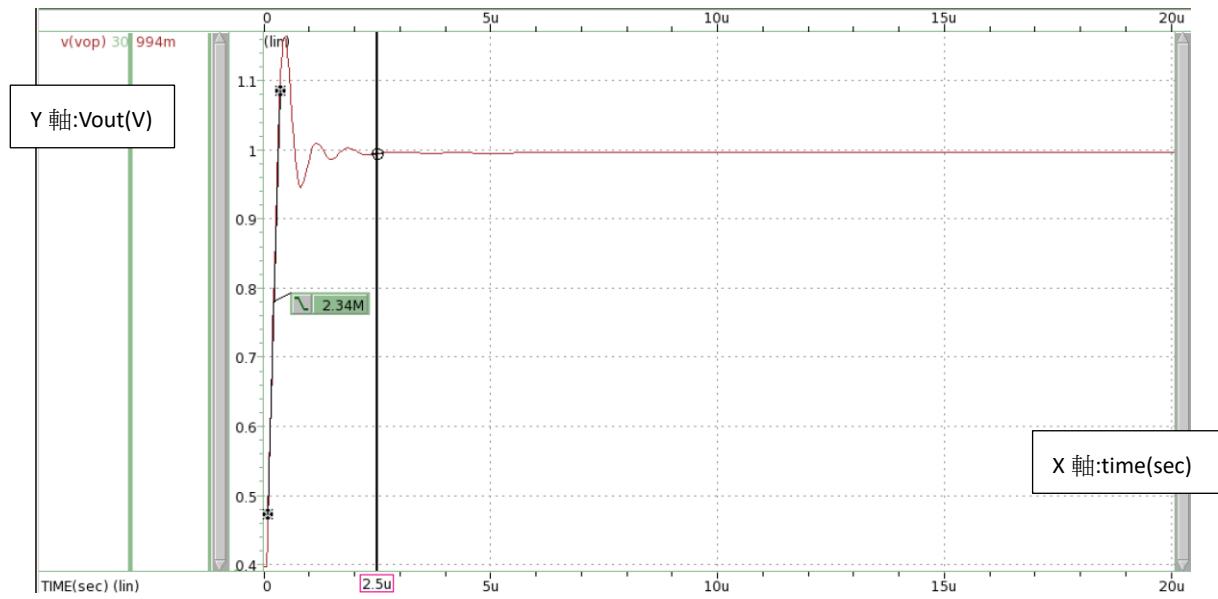
Fig. 3.9(b)

Single-ended:

V_{on} :



vop:



Differential outputs:

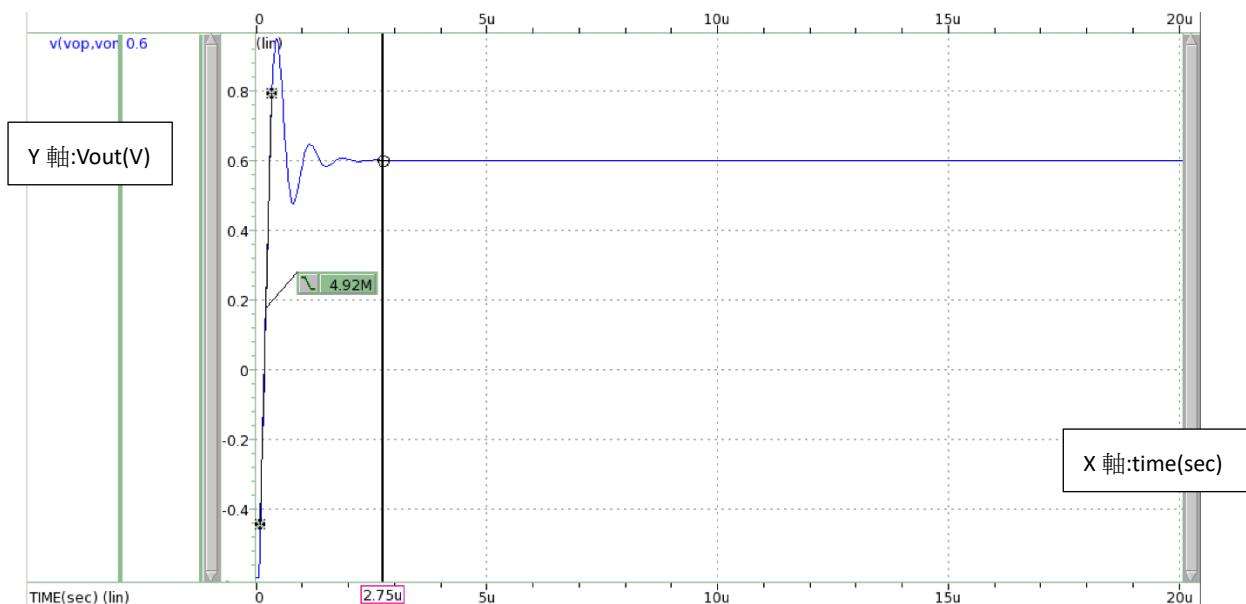
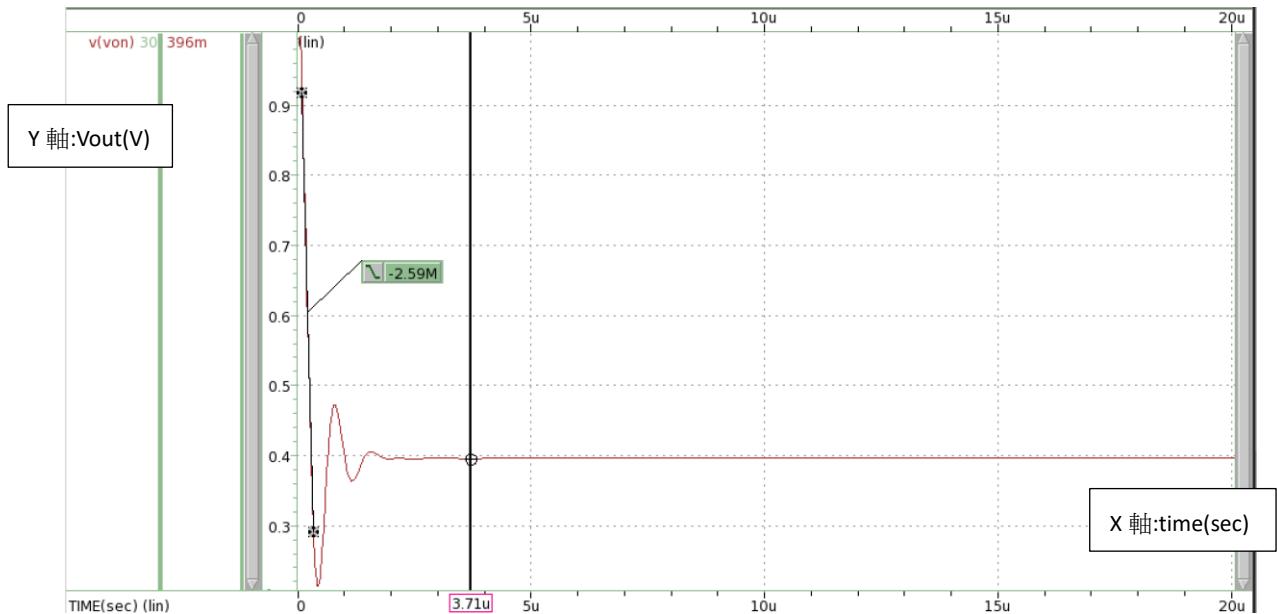


Fig. 3.9(c)

Single-ended:

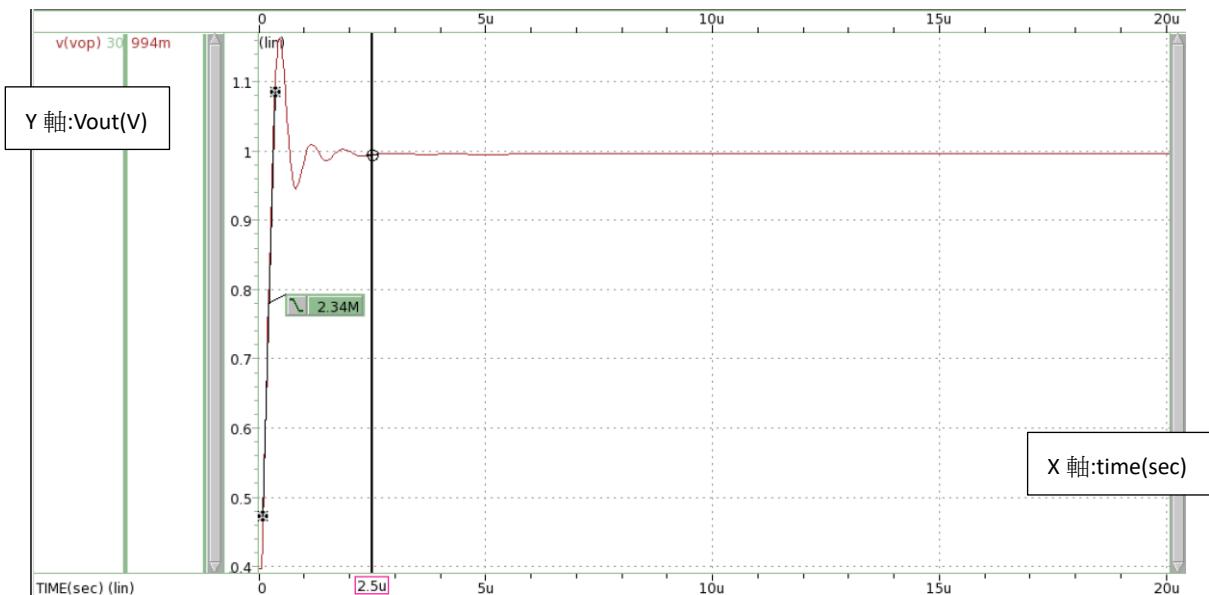
Von:



```
final2= 396.0986m  
hlimit2= 396.4947m  
llimit2= 395.7025m  
htime2= 3.2385u  
ltime2= 3.7622u  
pos_settling2= 3.7122u
```

Slew rate:2.59(V/us) Settling time:3.7122u(s)

vop:



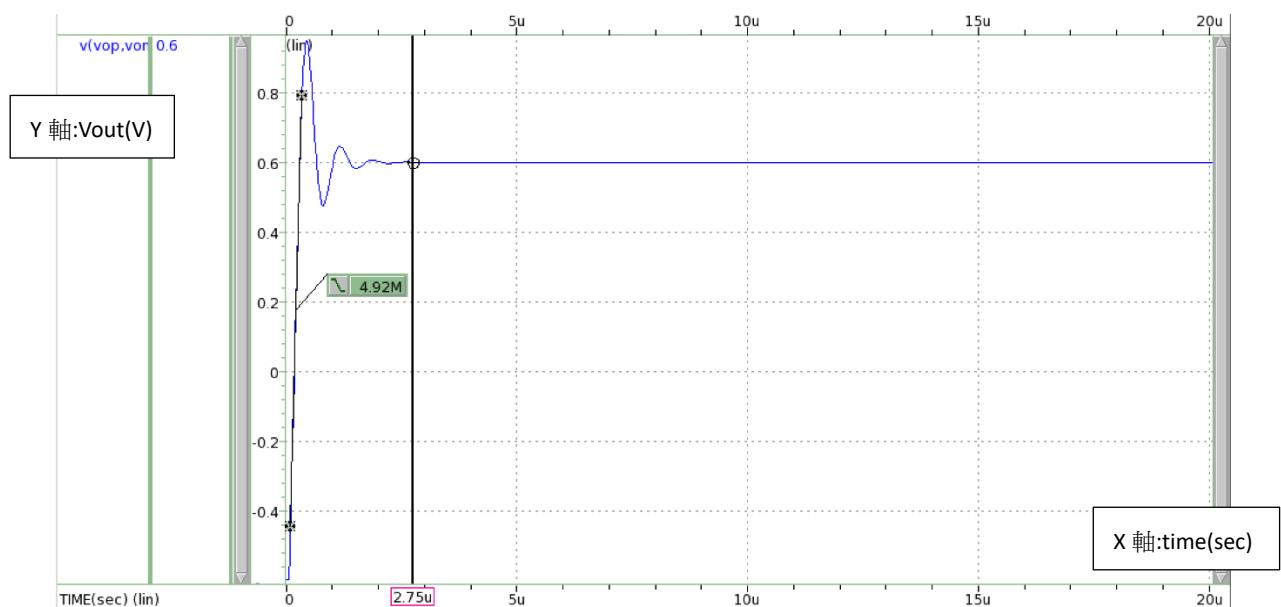
```

final= 995.7372m
hlimit= 996.7329m
llimit= 994.7415m
htime= 2.0897u
ltime= 2.5548u
pos_settling= 2.5048u

```

Slew rate:2.34(V/us) Settling time:2.5048u(s)

Differential outputs:



```

final= 599.6386m
hlimit= 600.2383m
llimit= 599.0390m
htime= 2.8037u
ltime= 2.4530u
pos_settling= 2.7537u

```

Slew rate:4.92(V/us) Settling time:2.7537u(s)

Fig. 3.9(d)

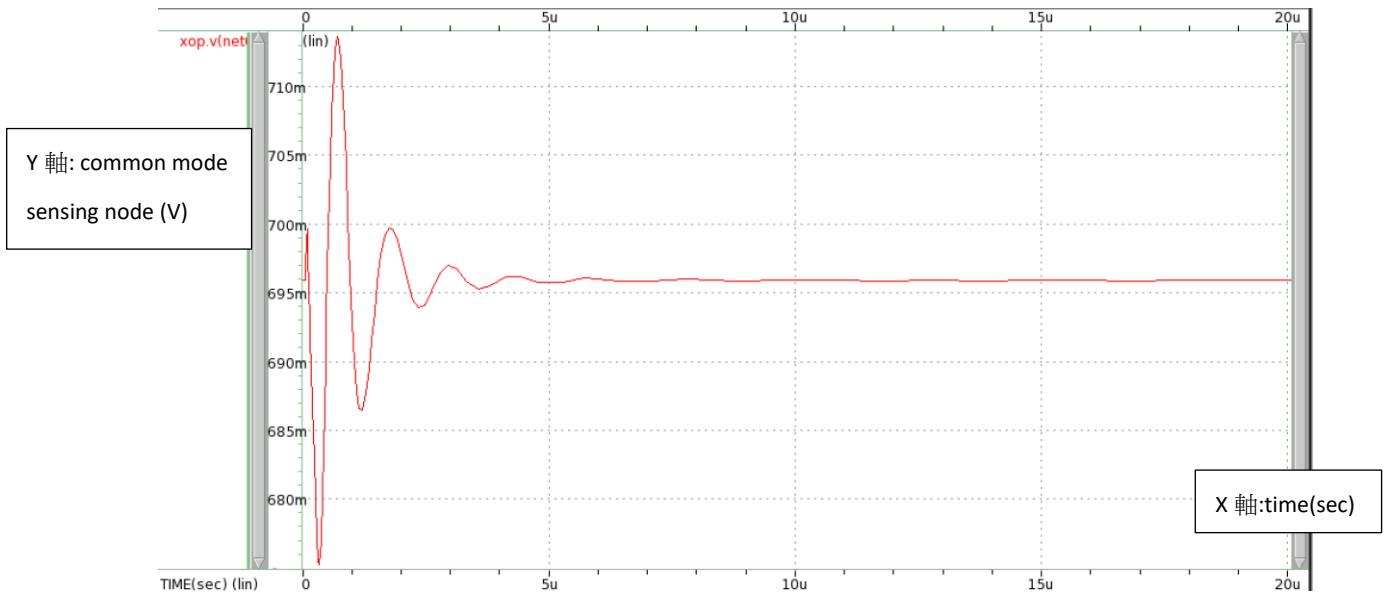


Fig. 3.9(e)

common mode sensing node 接到 MF2 的 gate 上，當此點電壓上升， V_{sg} 下降導致電流減少，MF2 和 MF4 電流必須一致，MF4 的電流也下降，造成它的 V_{ds} 下降，drain 那點接到 M3 和 M4 的 gate，M3 和 M4 的電流下降，M1 和 M2 的電流也下降，M3 和 M4 的 drain 那點電壓下降，此點接到 V_{on} 和 V_{op} ，讓 V_{on} 和 V_{op} 下降，最後 common mode sensing node 就會下降。

所以當 common mode sensing node 下降，經過一系列的 negative feedback，此點又會上升，呈現上圖上下震盪的樣子。

3.10 Closed-loop step- response

Fig. 3.10(a)

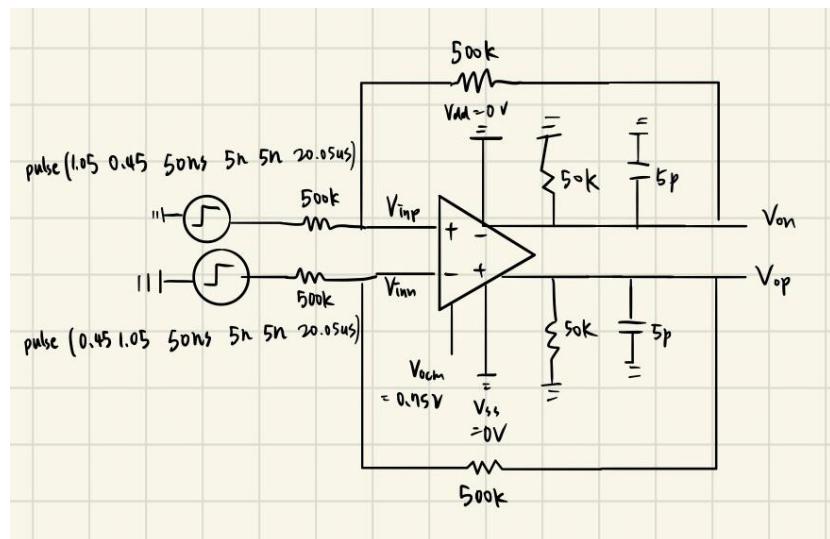


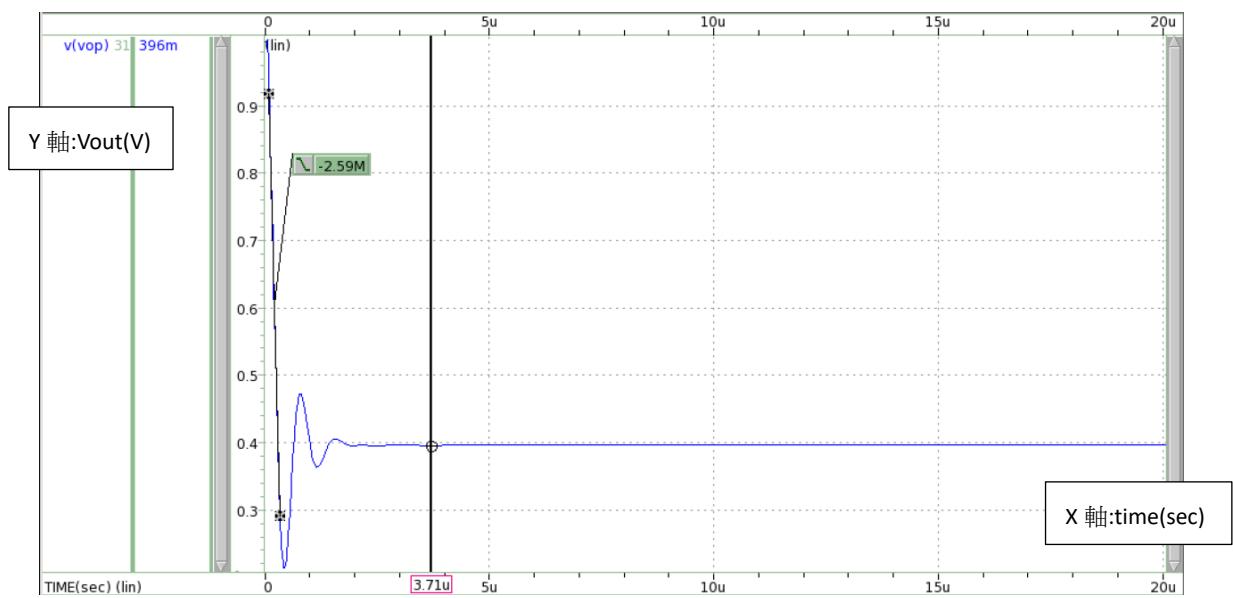
Fig. 3.10(b)

Single-ended:

Von:



Vop:



Differential outputs:

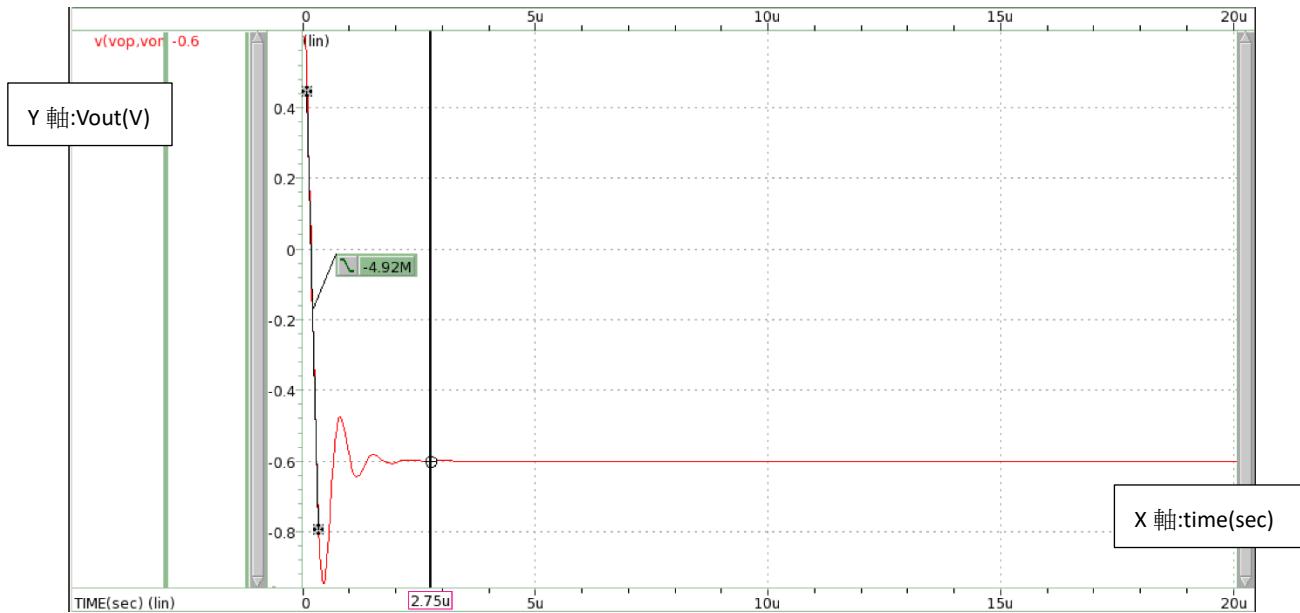
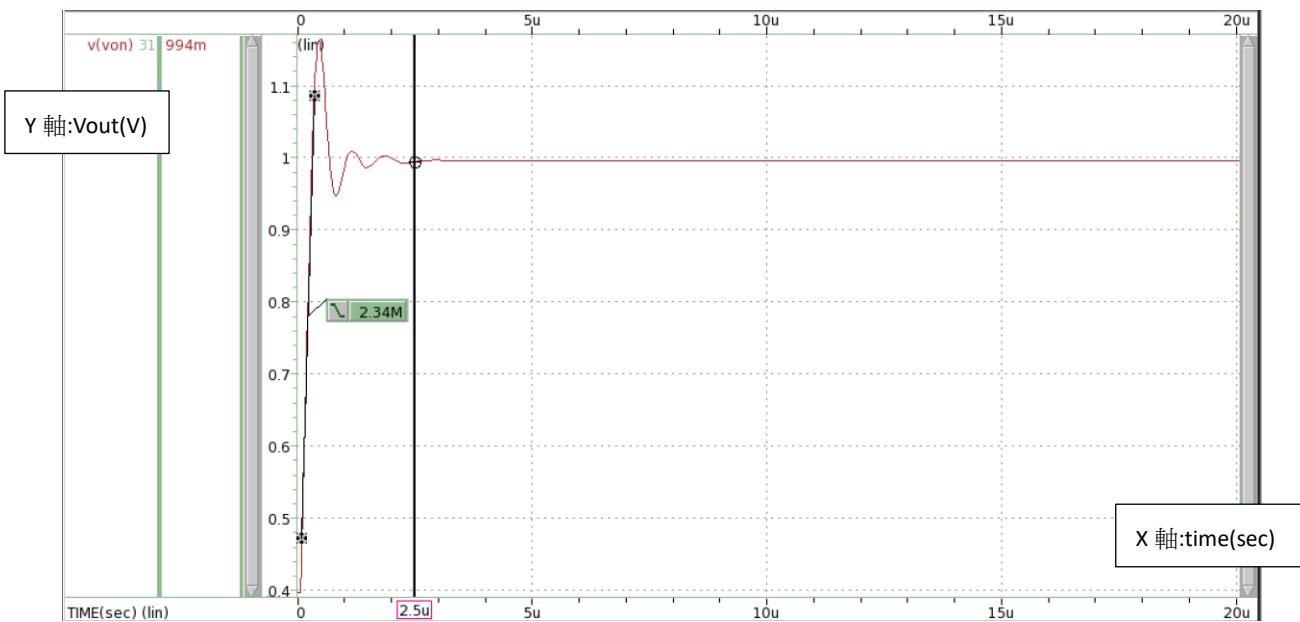


Fig. 3.10(c)

Single-ended:

Von:

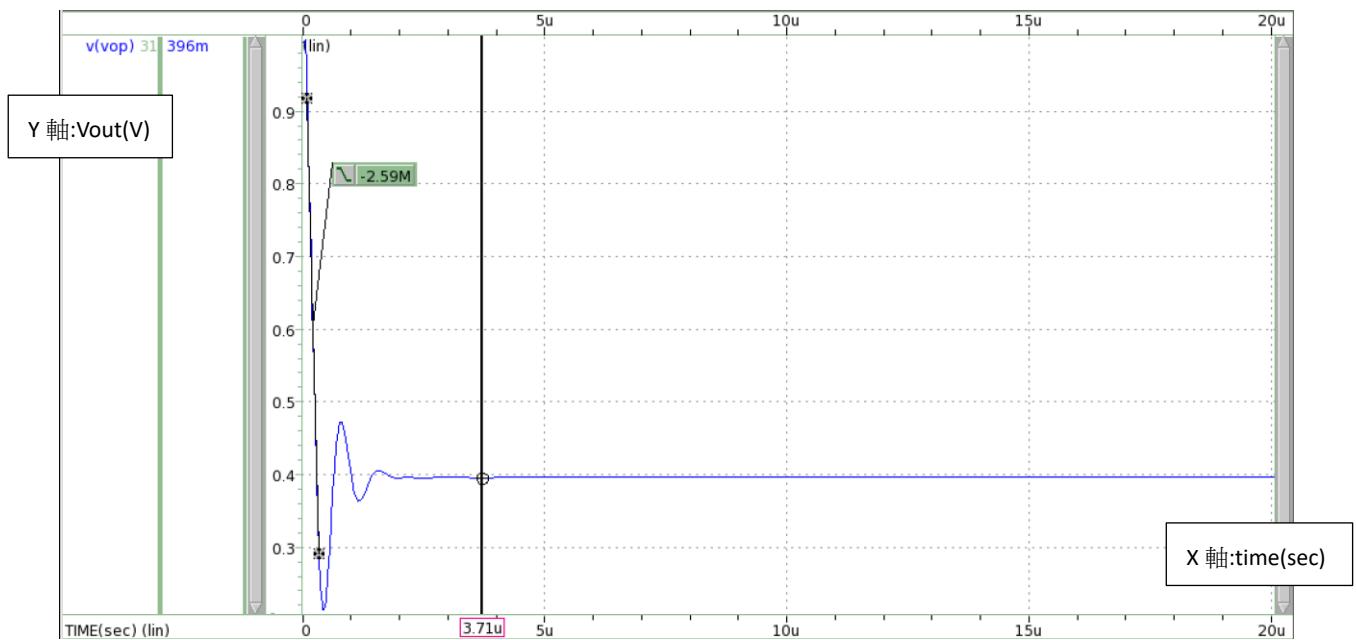


```

final2= 995.7372m
hlimit2= 996.7329m
l1limit2= 994.7415m
htime2= 2.0897u
ltime2= 2.5548u
pos_settling2= 2.5048u
  
```

Slew rate:2.34(V/us) Settling time:2.5048u(s)

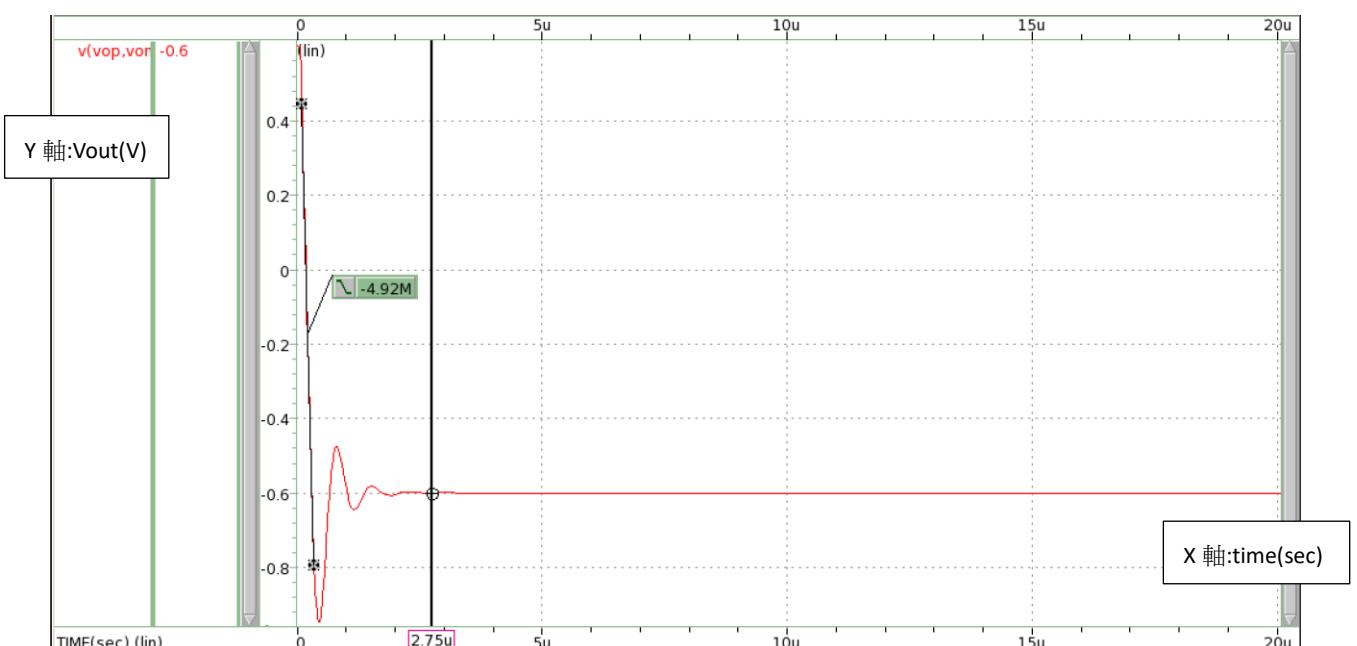
vop:



```
final1= 396.0986m  
hlimit1= 396.4947m  
l1limit1= 395.7025m  
htime1= 3.2385u  
ltime1= 3.7622u  
pos_settling1= 3.7122u
```

Slew rate:2.59(V/us) Settling time:3.7122u(s)

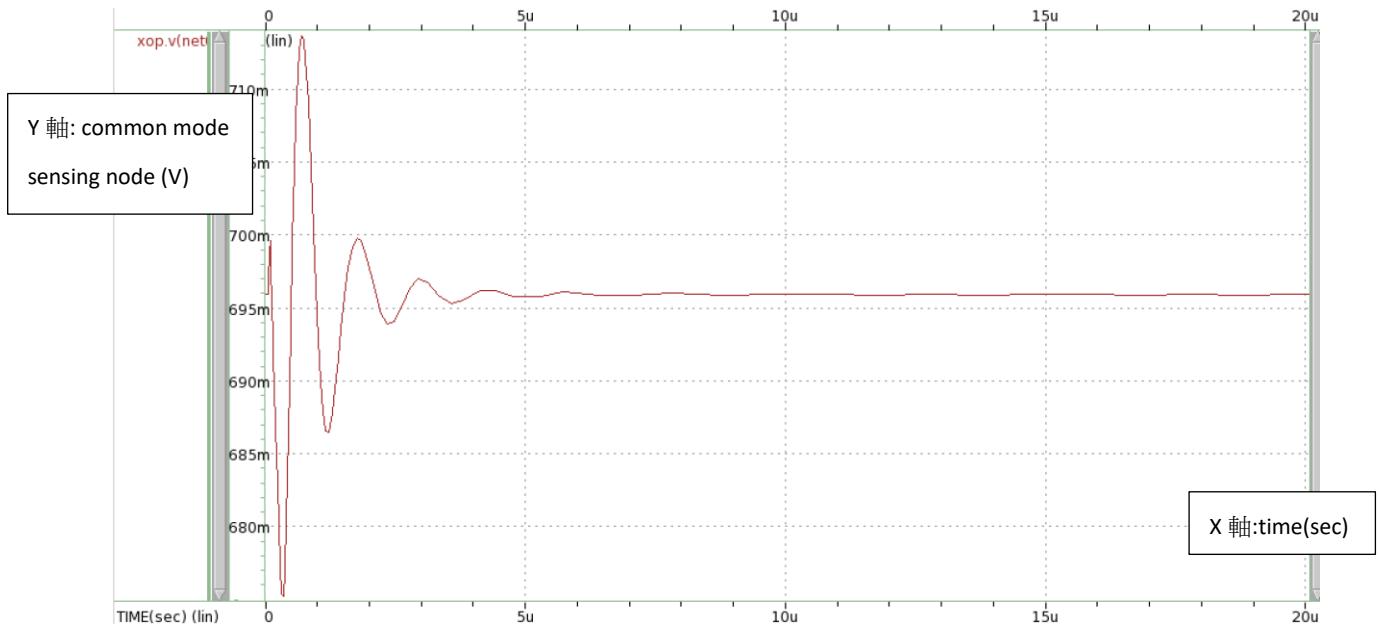
Differential outputs:



```
final=-599.6386m  
hlimit=-600.2383m  
llimit=-599.0390m  
htime= 2.8037u  
ltime= 2.4530u  
pos_settling= 2.7537u
```

Slew rate:4.92(V/us) Settling time:2.7537u(s)

Fig. 3.10(d)



4. Performance Table

Design Items	Specifications	My Work
Technology		
Supply voltage	1.5V, as small as possible	1.5V
Vicm, Vocm	0.75V / 0.75V	0.75/0.7499
Supply current	< 5mA, as small as possible	0.461mA
Loading	5pF / 50KΩ (for each output)	5p/50K
Compensation R, C,	Open for design	10K(ohm)/3p(F)
Open-loop simulation		
DC gain	> 60dB, as large as possible	70.8482
G-BW	> 1MHz, as large as possible	22.1267M
P.M.	> 45 °	58.3983
C.M.R.R. @10KHz	>80dB	80.1
P.S.R.R. @10KHz	> 80dB	84.5
P.S.R.R. @10KHz	> 80dB	97.4
Closed-loop simulation		
Differential swing of 1.2V (step signal)		
S.R.+ (10% ~ 90%)	> 1 V/us	4.92
S.R.- (90% ~ 10%)	> 1 V/us	4.92
Settling+ (to 0.1%)	< 10 us	2.7537u
Settling- (to 0.1%)	< 10 us	2.7537u
FoM		
Small signal	GBW (MHz) x CL (pF) / Power (mW)	133.3255
Large signal +	SR. (V/us) x CL (pF) / Power (mW)	29.6456978
Large signal -	SR- (V/us) x CL (pF) / Power (mW)	29.6456978

5. Design concerns

我調整的想法是先調整第一階段的 amplifier(M1~M5)，給 M3 和 M4 一個 0.55 的 gate 電壓，因為總共的 gain 要大於 60db，所以先設計它的 gain 到達 8db 左右，因為全部的 gain 公式為

$$DC\ gain = gm1(ro1//ro3)gm8(ro8//ro9//rload)$$

第一級的 gain 與 M1 的 gm 有很大的關係，gm 與 W/L 成正比，所以我將 M1/M2 的 W 設 90u，L 設 2u，這樣通過 M1/M2 的電流就會很大，因為 M1+M2 的電流會等於 M5 的電流，所以設計 M5 的 W/L 小一點，這樣會影響 M1/M2 的 Vsd 變小，讓 M1~M5 不在 saturation，所以要再慢慢調整。

之後再加上 M6~M9 和電阻 RZ 與電容 Cc，gain 與 M8 的 gm 有很大的關係，所以我將 M8/M6 的 W/L 比值調大，電容 Cc 越大的話 pole 越小，所以設計 Cc 小一點，電阻 RZ 則是慢慢調整，讓全部的 mos 保持在 saturation。再接上 MB1~MB3 和電阻 Rb，MB3 的 gate 電壓會接到 M5/M7/M9，所以要慢慢調整讓它不要將 M5/M7/M9 的 gate 電壓改變太多，不然剛剛調整的很多東西會受到影響，所以我先隨便設定 MB1 的 W/L，再設定上方的電阻 Rb 讓 MB1 在 saturation，再慢慢調整 MB2 和 MB3，看如何讓 mos 都保持在 saturation，且不要過於影響到 M5/M7/M9 的 gate 電壓，最後加上 MF1~MF5 和電阻 Rcm，MF1~MF5 我先隨便設定 MF1/MF2，再調整 MF3~MF5 讓全部的 mos 保持在 saturation，因為我給 M3 和 M4 一個 0.55 的 gate 電壓，MF4 的 gate 電壓會接到 M3/M4，所以要慢慢調整讓 MF4 的 gate 電壓接近 0.55。

等 gain 大於 60db 後，再檢查其他的要求有沒有過，我將 Rcm1/Rcm2 調大，讓電路保持穩定，settling time 跟題目要求的差蠻多的，所以我先處理，發現降低了某些 mos 的並聯數量後能讓 settling time 降低，再來是 phase margin 的部分，我調整 M7/M9 的 L 下降，讓 phase margin 上升。

6. Discussions

我設計步驟分了三大區塊，每一區塊的 mos 達到 saturation 之後，再接下一區塊，但是好不容易調整好的接到其他區塊後，很多 mos 會跑到 linear 或是 cut off，所以再全部東西都接起來之後，我調整了很久，試了很多組 W/L 和並聯，想辦法控制 mos 的 Vth 來達到 saturation，比較麻煩的是 project 中有很多條件，改了一些 mos 就要去查驗這些 settling time 或是 phase margin 等是怎麼改變的，趨勢是如何，我大概花了四天滿足所有條件後，發現 FoM 都不太理想，所以是試著將 power 減小，也就是電流的部分，我將某些 mos 的 L 調大一些，後來大概只花兩天的時間滿足全部的條件，在做 project 中漸漸熟悉了整個完整電路的運作，跟之前的作業比起來真的複雜許多，翻了很多次上課的講義，花了很多時間與同學討論，最後完成後真的很有成就感。

教授真的是一個很認真的老師，花了好長一段時間複習電子學，雖然這是我們本來就應該要會的東西，感謝教授的複習，如果直接進入類比課的主題，我一定跟不上步調，學習這些電路的運作方式，一些 bandwidth 和 gain 等知識後，讓我打了很好的基礎，在看一些 paper 時有感覺到比較熟悉如何去分析一個電路的架構，feedback 如何操作等，這堂課雖然辛苦但是學習到的知識非常的扎實，作業與 project，讓我們透過實際操作更了解上課的內容。

Sp 檔:

```
*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.param vdd=1.5V
.param vss=0V
.param vocm=0.75

*****
* Library Name: final
* Cell Name:    final
* View Name:   schematic
*****


.SUBCKT op vinp vinn vdd vss vop von vocm
*.PININFO Vinn:1 Vinp:1 Vocm:0 Von:0 Vop:0
CCc2 net13 net1 3p
CCc1 net7 net11 3p
RRb vdd net063 25K
RRCM2 net095 Von 5K
RRCM1 Vop net095 5K
RRZ2 net1 Von 10K
RRZ1 Vop net7 10K
MMB2 net23 net063 vss vss n_18 W=99u L=2u m=1
MMB1 net063 net063 vss vss n_18 W=50u L=2u m=1
MMF4 net19 net19 vss vss n_18 W=90u L=10u m=1
MMF3 net071 net071 vss vss n_18 W=90u L=10u m=1
MM6 Von net13 vss vss n_18 W=80u L=2u m=4
MM8 Vop net11 vss vss n_18 W=80u L=2u m=4
MM4 net13 net19 vss vss n_18 W=75u L=20u m=3
MM3 net11 net19 vss vss n_18 W=75u L=20u m=3
```

```
MMB3 net23 net23 vdd vdd p_18 W=90u L=1u m=1
MMF2 net19 net095 net0100 vdd p_18 W=75u L=3u m=1
MMF1 net071 .Vocom net0100 vdd p_18 W=75u L=3u m=1
MMF5 net0100 net23 vdd vdd p_18 W=99u L=12u m=1
MM7 Von net23 vdd vdd p_18 W=90u L=3u m=6
MM9 Vop net23 vdd vdd p_18 W=90u L=3u m=6
MM2 net13 Vinn net32 vdd p_18 W=90u L=2u m=1
MM5 net32 net23 vdd vdd p_18 W=30u L=1,5u m=1
MM1 net11 .Vinn net32 vdd p_18 W=90u L=2u m=1
.ENDS
```