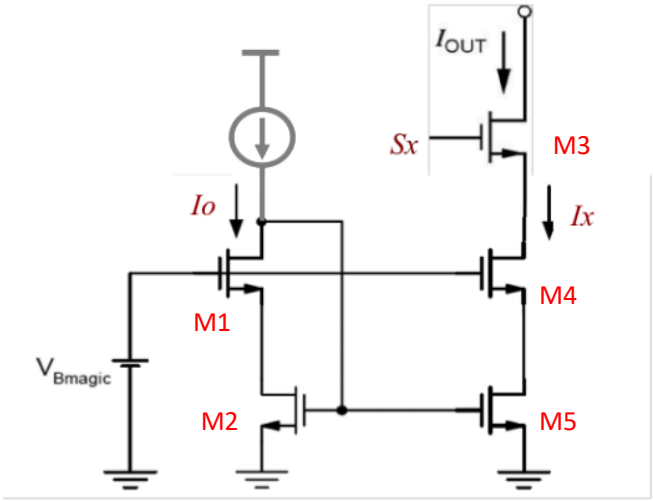
106010006 黃詩瑜 電機 21

Working Item	Simulation result
Vdd	1.5-V
Reference Io	0.0001A
Reference size (W/Lbottom, W/Lcascode)	Bottom: x1 (6.125u/0.735u) Cascode: x1 (6.125u/0.735u)
Output load Rout	0.5 Kohm
DAC unit size (W/Lbottom, W/Lcascode)	I: Bottom: x1 (6.125u/0.735u，m=1) Cascode: x1 (6.125u/0.735u，m=1) 2I: Bottom: x2 (6.125u/0.735u，m=2) Cascode: x2 (6.125u/0.735u，m=2) 4I: Bottom: x4 (6.125u/0.735u，m=4) Cascode: x4 (6.125u/0.735u，m=4) 8I: Bottom: x8 (6.125u/0.735u，m=8) Cascode: x8 (6.125u/0.735u，m=8)
Output voltage range (0.75)	1.5V~0.75107415V

DNL Error (%) [(this level – previous level)- ideal step] / ideal step (0.75V/15)							
I1	I2	I3	I4	I5	I6	I7	I8
0.024	0.028	0.014	-0.01	0.04	-0.004	0.006	-0.074
I9	I10	I11	I12	I13	I14	I15	
0.046	-0.037272	-0.063264	-0.155468	-0.309706	-0.584944	-1.067646	
INL Error (%) this level – ideal level / ideal step (0.75V/15)							
I1	I2	I3	I4	I5	I6	I7	I8
-0.024	-0.052	-0.066	-0.056	-0.096	-0.092	-0.098	-0.024
I9	I10	I11	I12	I13	I14	I15	
-0.07	-0.032728	0.030536	0.186004	0.49571	1.080654	2.1483	

(a)



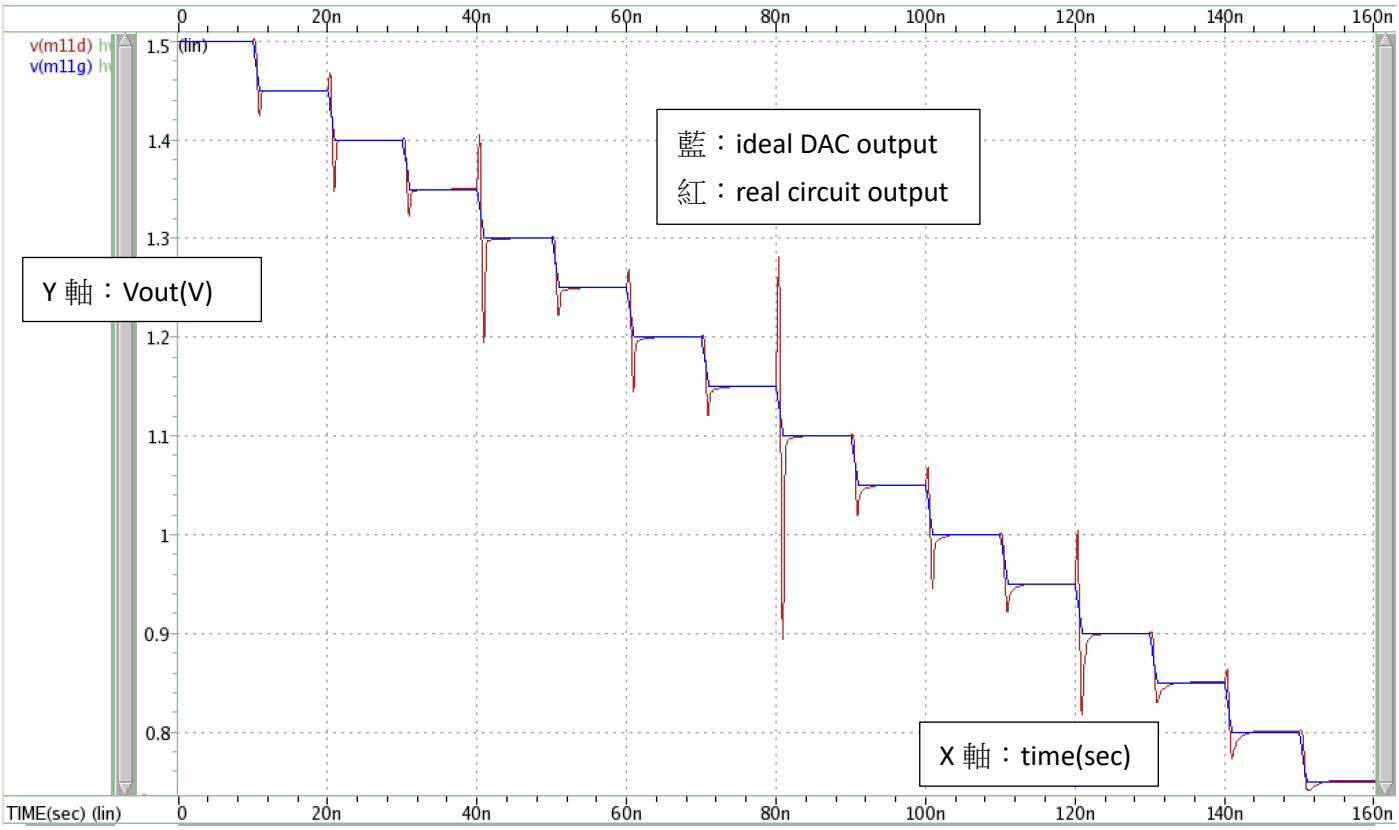
Reference 的 nmos M1: x1 (6.125u/0.735u，m=1)

M2: x1 (6.125u/0.735u，m=1)

DAC unit:

	M3	M4	M5
I	x1 (6.125u/0.735u，m=1)	x1 (6.125u/0.735u，m=1)	x1 (6.125u/0.735u，m=1)
2I	x2 (6.125u/0.735u，m=2)	x2 (6.125u/0.735u，m=2)	x2 (6.125u/0.735u，m=2)
4I	x4 (6.125u/0.735u，m=4)	x4 (6.125u/0.735u，m=4)	x4 (6.125u/0.735u，m=4)
8I	x8 (6.125u/0.735u，m=8)	x8 (6.125u/0.735u，m=8)	x8 (6.125u/0.735u，m=8)

(b)



(c)

每個 step 寬度為 10n，fall time 為 1n

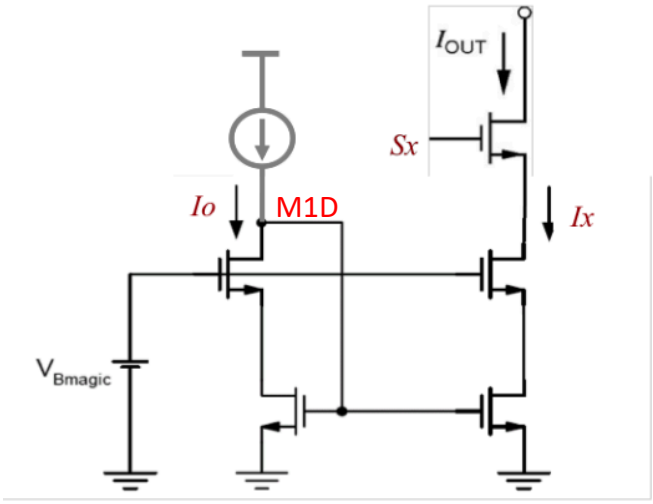
Ideal step=0.05

At time(sec)	模擬 Vout 結果(V)	理想 Vout(V)
5n	vout1= 1.500000	1.5
15n	vout2= 1.449988	1.45
25n	vout3= 1.399974	1.4
35n	vout4= 1.349967	1.35
45n	vout5= 1.299972	1.3
55n	vout6= 1.249952	1.25
65n	vout7= 1.199954	1.2
75n	vout8= 1.149951	1.15
85n	vout9= 1.099988	1.1
95n	vout10= 1.049965	1.05
105n	vout11= 999.983636m	1.0
115n	vout12= 950.015268m	0.95
125n	vout13= 900.093002m	0.9
135n	vout14= 850.247855m	0.85
145n	vout15= 800.540327m	0.8
155n	vout16= 751.074150m	0.75

	DNL error	INL error
I1	(|1.449988-1.5|-0.05)/0.05*100% = 0.024%	(1.449988-1.45)/0.05*100% = -0.024%
I2	(|1.399974-1.449988|-0.05)/0.05*100% = 0.028%	(1.399974-1.4)/0.05*100% = -0.052%
I3	(|1.349967-1.399974|-0.05)/0.05*100% = 0.014%	(1.349967-1.35)/0.05*100% = -0.066%
I4	(|1.299972-1.349967|-0.05)/0.05*100% = -0.01%	(1.299972-1.3)/0.05*100% = -0.056%
I5	(|1.249952-1.299972|-0.05)/0.05*100% = 0.04%	(1.249952-1.25)/0.05*100% = -0.096%
I6	(|1.199954-1.249952|-0.05)/0.05*100% = -0.004%	(1.199954-1.2)/0.05*100% = -0.092%
I7	(|1.149951-1.199954|-0.05)/0.05*100% = 0.006%	(1.149951-1.15)/0.05*100% = -0.098%
I8	(|1.099988-1.149951|-0.05)/0.05*100% = -0.074%	(1.099988-1.1)/0.05*100% = -0.024%
I9	(|1.049965-1.099988|-0.05)/0.05*100% = 0.046%	(1.049965-1.05)/0.05*100% = -0.07%
I10	(|0.999983636-1.049965|-0.05)/0.05*100% = -0.037272%	(0.999983636-1.0)/0.05*100% = -0.032728%
I11	(|0.950015268-0.999983636|-0.05)/0.05*100% = -0.063264%	(0.950015268-0.95)/0.05*100% = 0.030536%
I12	(|0.900093002-0.950015268|-0.05)/0.05*100% = -0.155468%	(0.900093002-0.9)/0.05*100% = 0.186004%
I13	(|0.850247855-0.900093002|-0.05)/0.05*100% = -0.309706%	(0.850247855-0.85)/0.05*100% = 0.49571%
I14	(|0.800540327-0.850247855|-0.05)/0.05*100% = -0.584944%	(0.800540327-0.8)/0.05*100% = 1.080654%
I15	(|0.75107415-0.800540327|-0.05)/0.05*100% = -1.067646%	(0.75107415-0.75)/0.05*100% = 2.1483%

DNL Error (%) [(this level – previous level)- ideal step] / ideal step (0.75V/15)							
I1	I2	I3	I4	I5	I6	I7	I8
0.024	0.028	0.014	-0.01	0.04	-0.004	0.006	-0.074
I9	I10	I11	I12	I13	I14	I15	
0.046	-0.037272	-0.063264	-0.155468	-0.309706	-0.584944	-1.067646	
INL Error (%) this level – ideal level / ideal step (0.75V/15)							
I1	I2	I3	I4	I5	I6	I7	I8
-0.024	-0.052	-0.066	-0.056	-0.096	-0.092	-0.098	-0.024
I9	I10	I11	I12	I13	I14	I15	
-0.07	-0.032728	0.030536	0.186004	0.49571	1.080654	2.1483	

(d)



Voltage range 為 0.75，S1~S4 都接通電流會有 15I，

$$Vdd - 15I * Rl = 0.75$$
$$=\gg 1.5 - 15I * 500 = 0.75$$

，所以 I=0.0001A，每個 nmos 都要是 saturation，

Vds>Vgs-Vth

=>> V(M1D)>V(Bmagic)-Vth

，Vth 大約是 450mv 左右，

$$Id = \frac{1}{2}\mu Cox\frac{W}{L}(Vgs - Vth)^2$$

在 I 的情況，先設 W=6.125u，L=0.735u，μCox約為$266X10^{-6}$

$$0.0001 = \frac{1}{2}X266X10^{-6}X\frac{6.125u}{0.735u}(V(M1D) - 0.45)^2$$

=>> V(M1D)約為 0.75V

=>> V(M1D)>V(Bmagic)-Vth

=>> 0.75> V(Bmagic)-0.45

因此設 V(Bmagic)為 1.1V

在 DAC unit 會流跟 reference 同樣的電流(I=0.0001A)，nmos 的 W/L/Vgs/Vds 等，與 reference 相同，所以也會在 saturation，在 2I/4I/8I 的情況，因為 nmos 並聯 2/4/8 個，所以電流會流 2/4/8 倍，因為連接相同的 V(Bmagic)/V(M1D)，所以全部的 nmos 也會在 saturation。

原本我的 L 是設 0.18u，後來發現在開啟全部的開關時，Vout 有明顯的誤差，所以後來加大了 L 來減少 channel length modulation 可能造成的影響，讓 Vds 不要影響電流太多，而變得更加穩定。

模擬出來的波形有些震盪，發生在較大電流的開或關時，也就是 S3(4I)與 S4(8I)開關時，會造成不穩定的情況，而模擬出來的波形 DNL 和 INL 誤差都很小，DNL 誤差小，代表每個 step 的寬度都很接近理想值，不會因為某個 step 寬度過寬而造成 missing code 的情況，而 INL 誤差小，代表 step 的 Vout 與理想值接近，這些誤差的來源可能來自於並聯 N 個的 nmos，其 W/L 不會真的是 N 倍，與 nmos 的 Vth 稍微不同，而產生誤差，且誤差有電流越大誤差越大的趨勢，查看.lis 檔案後，發現開關全打開後，DAC unit nmos 的 Vth 和 Vds 會稍微變動，因為 channel length modulation，Vds 還是會影響電流，進而讓 Vout 產生誤差，但誤差也只有 1%~2%。

```
*hw4
.prot
.lib 'cic018.l' TT
.unprot
.option
+ post=1
+ACCURATE=1
+ runlvl=6
+ measdgt=6
.temp 25


M1 M1D M1G M1S gnd n_18 w=6.125u l=0.735u m=1
M2 M1S M1D gnd gnd n_18 w=6.125u l=0.735u m=1

*S1
M11 M11D M11G M11S gnd n_18 w=6.125u l=0.735u m=1
M12 M11S M1G M12S gnd n_18 w=6.125u l=0.735u m=1
M13 M12S M1D gnd gnd n_18 w=6.125u l=0.735u m=1

*S2
M21 M11D M21G M21S gnd n_18 w=6.125u l=0.735u m=2
M22 M21S M1G M22S gnd n_18 w=6.125u l=0.735u m=2
M23 M22S M1D gnd gnd n_18 w=6.125u l=0.735u m=2

*S3
M31 M11D M31G M31S gnd n_18 w=6.125u l=0.735u m=4
M32 M31S M1G M32S gnd n_18 w=6.125u l=0.735u m=4
M33 M32S M1D gnd gnd n_18 w=6.125u l=0.735u m=4

*S4
M41 M11D M41G M41S gnd n_18 w=6.125u l=0.735u m=8
M42 M41S M1G M42S gnd n_18 w=6.125u l=0.735u m=8
M43 M42S M1D gnd gnd n_18 w=6.125u l=0.735u m=8



vdd vdd gnd 1.5V
RL vdd M11D 0.5k
Vb M1G gnd 1.1V
IM vdd M1D 0.0001

VSX1 M11G gnd PULSE 0 1.5 10n 1n 1n 9n 20n
VSX2 M21G gnd PULSE 0 1.5 20n 1n 1n 19n 40n
VSX3 M31G gnd PULSE 0 1.5 40n 1n 1n 39n 80n
VSX4 M41G gnd PULSE 0 1.5 80n 1n 1n 79n 160n
```

```
.op
.tran 0.01n 160n
.meas TRAN vout1 FIND V(M11D) at=5n
.meas TRAN vout2 FIND V(M11D) at=15n
.meas TRAN vout3 FIND V(M11D) at=25n
.meas TRAN vout4 FIND V(M11D) at=35n
.meas TRAN vout5 FIND V(M11D) at=45n
.meas TRAN vout6 FIND V(M11D) at=55n
.meas TRAN vout7 FIND V(M11D) at=65n
.meas TRAN vout8 FIND V(M11D) at=75n
.meas TRAN vout9 FIND V(M11D) at=85n
.meas TRAN vout10 FIND V(M11D) at=95n
.meas TRAN vout11 FIND V(M11D) at=105n
.meas TRAN vout12 FIND V(M11D) at=115n
.meas TRAN vout13 FIND V(M11D) at=125n
.meas TRAN vout14 FIND V(M11D) at=135n
.meas TRAN vout15 FIND V(M11D) at=145n
.meas TRAN vout16 FIND V(M11D) at=155n

.alter
VSX1 M11G gnd PWL 0n 1.5 10n 1.5 11n 1.45 20n 1.45 21n 1.4 30n 1.4 31n 1.35 40n 1.35 41n 1.3
+ 50n 1.3 51n 1.25 60n 1.25 61n 1.2 70n 1.2 71n 1.15 80n 1.15 81n 1.1 90n 1.1 91n 1.05
+ 100n 1.05 101n 1 110n 1 111n 0.95 120n 0.95 121n 0.9 130n 0.9 131n 0.85 140n 0.85
+ 141n 0.8 150n 0.8 151n 0.75 160n 0.75


.end
```