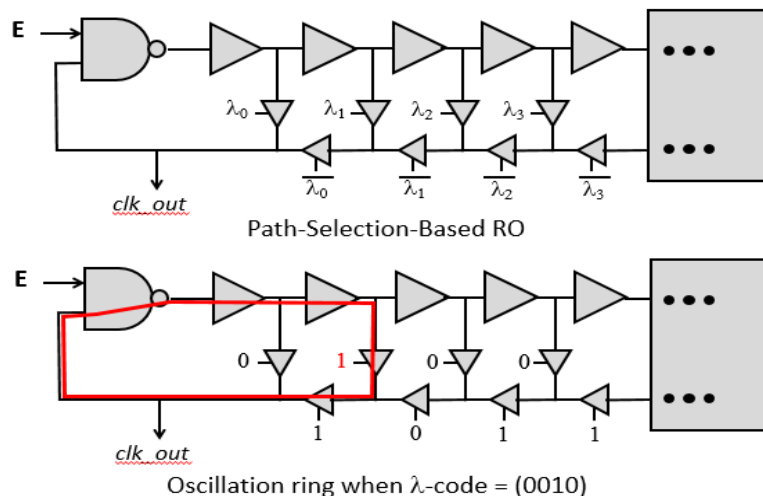


◆ **Objective:** To design a simple cell-based Phased-Locked Loop (PLL) and perform frequency acquisition.

◆ **Step-by-Step Procedure**

Design a low-resolution Phase-Locked Loop to produce a 500MHz clock signal, denoted as *clk_out*, from a 10MHz reference clock signal, *clk_ref*.

- (a) Design a **path-selection-based Digital Controlled Oscillator (DCO)** as indicated below. Report the oscillation frequency of your DCO under various control code values. Note that you may need to use a longer buffer chain and a control code with more bits than what is shown in the figure to ensure that the oscillation frequency fits your needs. (30%)



- (b) Design a **frequency divider** and a **controller** that works with your **DCO** and some Phase Detector (**PD**) you have developed in homework #1 so that your PLL will produce a frequency closest to the designated clock frequency after **frequency acquisition**. Verify your DLL design by Verilog simulation using as accurate delay model as possible for your DCO, frequency divider, and controller. Use the behavior model you have constructed in homework #1 for your PD. **Show the average clock cycle times of *clk_out* observed over 10 clock cycles after the frequency acquisition and its error as compared to the ideal clock cycle time (which is 2000ps).** (40%)
- (c) Try to use SOC Encounter to **generate the layout** of your design. What is the size of your layout? (15%)
- (d) Try to do **post-layout Verilog simulation** for your PLL. Your TDL, frequency divider, and controller should be back-annotated with the post-layout SDF information, while using the behavior model for your PD. Compare your results with those derived in the pre-layout simulation. (15%)

◆ **Deliverables:** Submit the following documents (combined into a PDF file) to our iLMS system.

- ◆ A cover page containing 所有組員之系所，中英文姓名，學號等資訊
- ◆ Your results to questions (a)-(d).
- ◆ 各個組員的負責項目，或是貢獻方式的一段簡述。