國立清華大學 電機工程學系

一〇九學年度第二學期

EE-5216 時序電路設計及應用 (Timing Circuit Designs and Their Applications)

Homework #1 (This is a team homework, with up to 3 members per team)

Due Date：23:59pm, April 8 (Thursday), 2021, (逾時不收)

Submission to iLMS @http://lms.nthu.edu.tw

- **Objective: Characterization of a Phase Detector**
- **Experience to be Learnt from this Homework:**

To get familiar with the SPICE simulation for the characterization of a timing sensitive circuit and then convert the results into a behavior model. Such a model can be used to support more efficient system-level simulation using Verilog simulators.

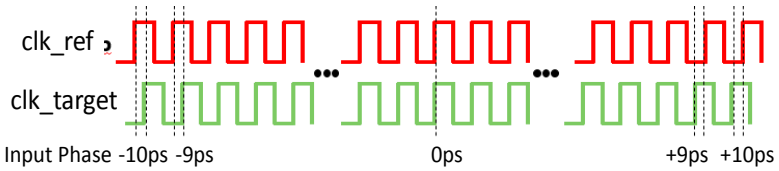
- **Step-by-Step Procedure**

Consider the design and characterization process for a Phase Detector (PD) used to determine the polarity of the phase of two clock signal. The two 1GHz input clock signals are named *clk_ref* and *clk_target*. The output is an one-bit flag signal, called *lead_lag*. At each clock cycle, if the rising edge of *clk_target* arrives earlier than that of *clk_ref*, then the output *lead_lag* becomes '0' (to indicate a *leading condition*). On the other hand, if the rising edge of *clk_target* arrives later than that of *clk_ref*, then the output *lead_lag* becomes '1' (to indicate a *lagging condition*).

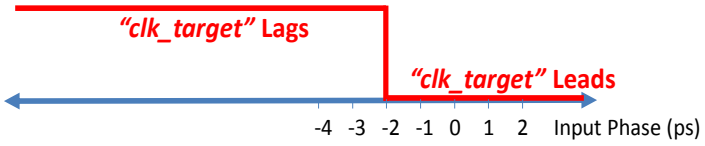
(a) Compose the SPICE circuit files for each of the 3 PDs discussed in class – (1) simple Flip-Flop based PD, (2) A sense amplifier based PD, and (3) racing based PD with 2 Flip-Flops, 1 racing circuit, and 1 SR latch. (30%)

(b) Run pre-layout SPICE simulation with two scenarios in terms of the two clock signals – (1) *clk_target* lags *clk_ref* by 10ps, and (2) *clk_target* leads *clk_ref* by 10ps. Report your output waveforms, respectively for the 3 types of PDs. (10%)

(c) Run pre-layout SPICE simulation to characterize the "**Flipping Input Phase (FIP)**" using the "sweeping input stimuli" shown in Fig. 1 below. Note that the "**Input Phase**" here is defined as the "the phase of *clk_ref*" minus "the phase of *clk_target*". Use a table to summarize the FIB values of the 3 different PDs. Note that, for a PD, a smaller absolute FIP value indicates a higher resolution. Rank the resolution of the 3 different PDs. (30%)



(a) Sweeping Input stimuli to derive Flipping Input Phase (FIP) value



(b) The lead/lag signal of a PD (indicating a FIP value of -2ps)

Fig. 1. Illustration of the Flipping Input Phase (FIP) value of a PD.

(d) Try to compose the behavior model for each of the 3 PDs using Verilog while including the FIB values you have derived in (c). Also, develop a testbench in Verilog generating the above "sweeping input stimuli" to verify that your behavior models are correct in producing the expected FIP value for each of the 3 different PDs. (30%)

- **Deliverables: Submit the following documents (combined into a PDF file) to our iLMS system.**
  - Your results to questions (a)-(d).
  - 各個組員的負責項目，或是貢獻方式的一段簡述。