國立清華大學 電機工程學系

一〇九學年度第二學期

EE-5216 時序電路設計及應用 (Timing Circuit Designs and Their Applications)

Homework #3 (This is a team homework, with up to 3 members per team)

Due Date：23:59pm, May 27 (Thursday), 2021, (逾時不收)

Submission to iLMS @http://lms.nthu.edu.tw

◆ **Objective: Duty-Cycle Correction Circuit Design**

◆ **Experience to be Learnt from this Homework:**

To get familiar with the design process of a timing circuit and a hybrid simulation method performed on a system consisting of both netlists and behavior model extracted from SPICE simulation.

◆ **Step-by-Step Procedure**

Consider a design process for a duty-cycle corrector for a 1GHz input clock signal, denoted as *clk_in*. The output clock signal is denoted as *clk_dcc*. Once locked, *clk_dcc* will have a duty cycle very close to 50%.

(a) (20%) Draw a block diagram of your design and summarizing how you plan to achieve the duty-cycle correction with a paragraph.

(b) (20%) Realize the design as a synthesizable Verilog code. (Your design can be a mixed format containing both netlists and RTL codes). (Hint: you may need Tunable Delay Lines, A Phase Detector, and a Controller, etc.) In this homework, we only need to use simple TDL, e.g., path-selection-based TDL, and some cell-based Phase Detector from homework #1). Resolution is not a concern in this homework.

(c) (15%) Try to use Design Compiler to synthesize your design into standard-cell netlists.

(d) (15%) Verify the correctness of your design by running gate-level Verilog simulation using as accurate delay model as possible. (Note: you may need to use your behavior model from homework #1 for the PD part). Show the waveforms of *clk_in* and *clk_dcc*. Try the following input duty cycle samples for *clk_in* – {30%, 40%, 50%, 60%, 70%}.

(e) (15%) Try to use SOC Encounter to generate the layout of your design. What is the size of your layout?

(f) (15%) Try to re-do what you have done for problem (d), but back-annotated with the post-layout SDF information except the PD part. Compare your results with those derived in the pre-layout simulation.

◆ **Deliverables: Submit the following documents (combined into a PDF file) to our iLMS system.**

- ◆ A cover page containing 所有組員之系所，中英文姓名，學號等資訊
- ◆ Your results to questions (a)-(f)
- ◆ 各個組員的負責項目，或是貢獻方式的一段簡述。