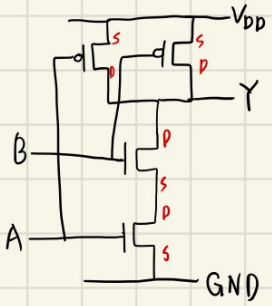
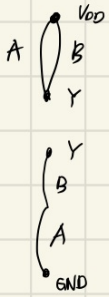
HW1　106010006 黃詩瑜 電機 21

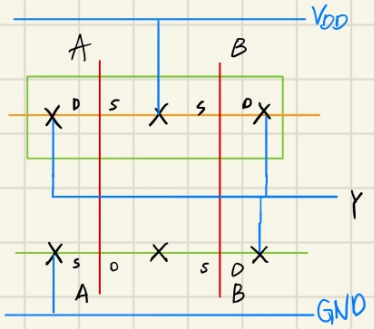
1.

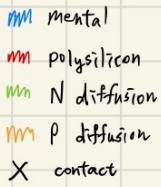
(a) $Y = A' + B'$

$= \overline{A \cdot B}$



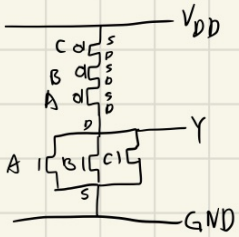


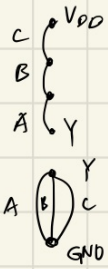


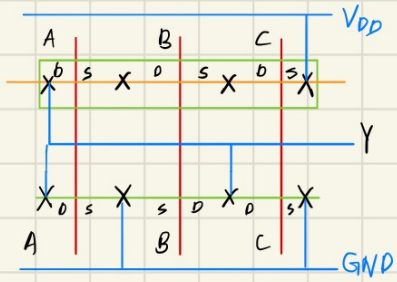


(b) $Y = A'B'C'$

$= \overline{A+B+C}$







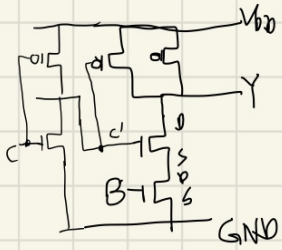
(c) $Y = AC + BC + B'$

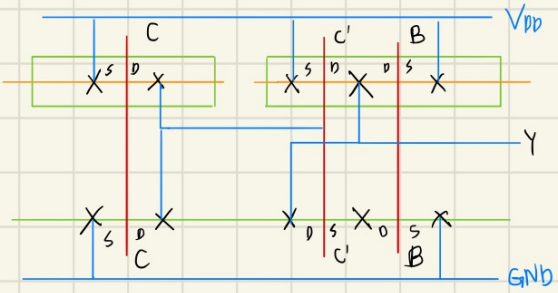
$= C(A+B) + B'$

$= \overline{\overline{C(A+B)}\ B}$

$= \overline{\left[C' + \overline{(A+B)}\right] B}$

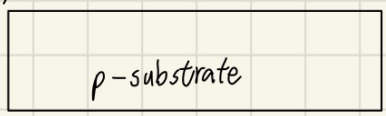
$= \overline{BC'}$



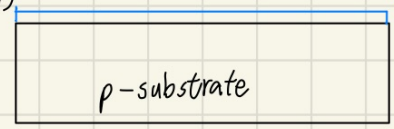


2.

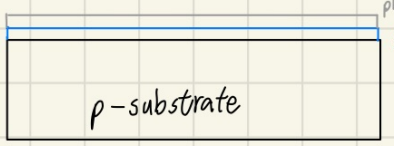
(a)



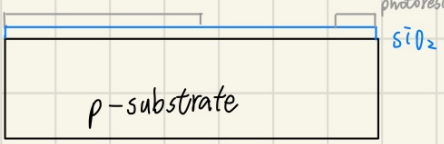
(b)



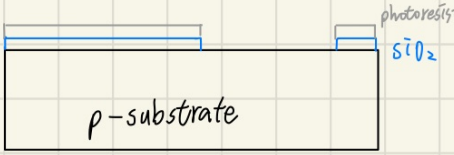
(c)



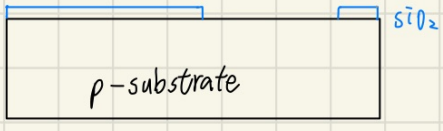
(d)



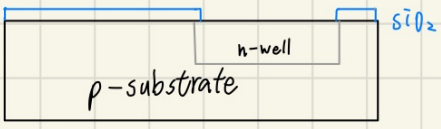
(e)



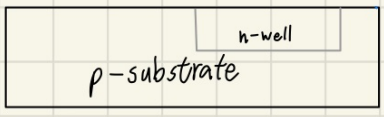
(f)



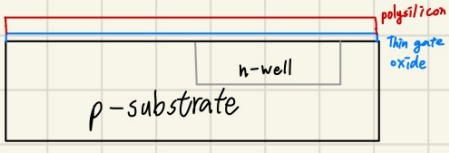
(g)

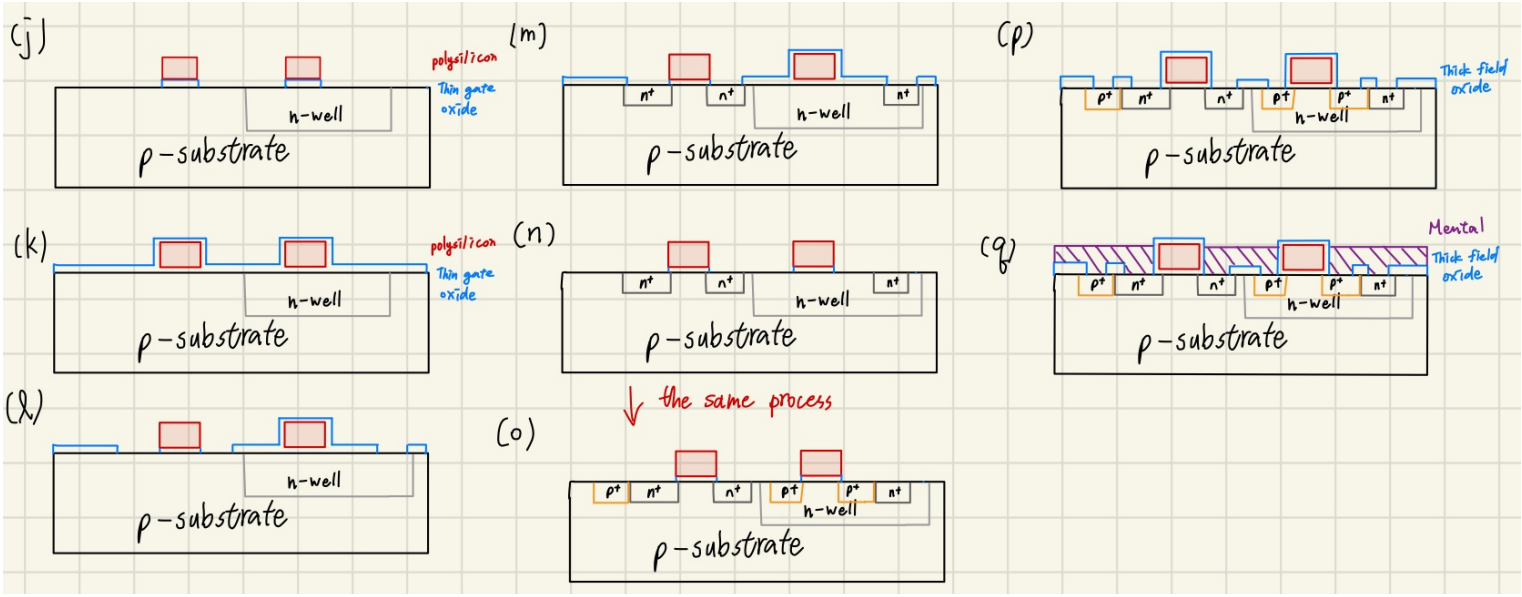


(h)



(i)





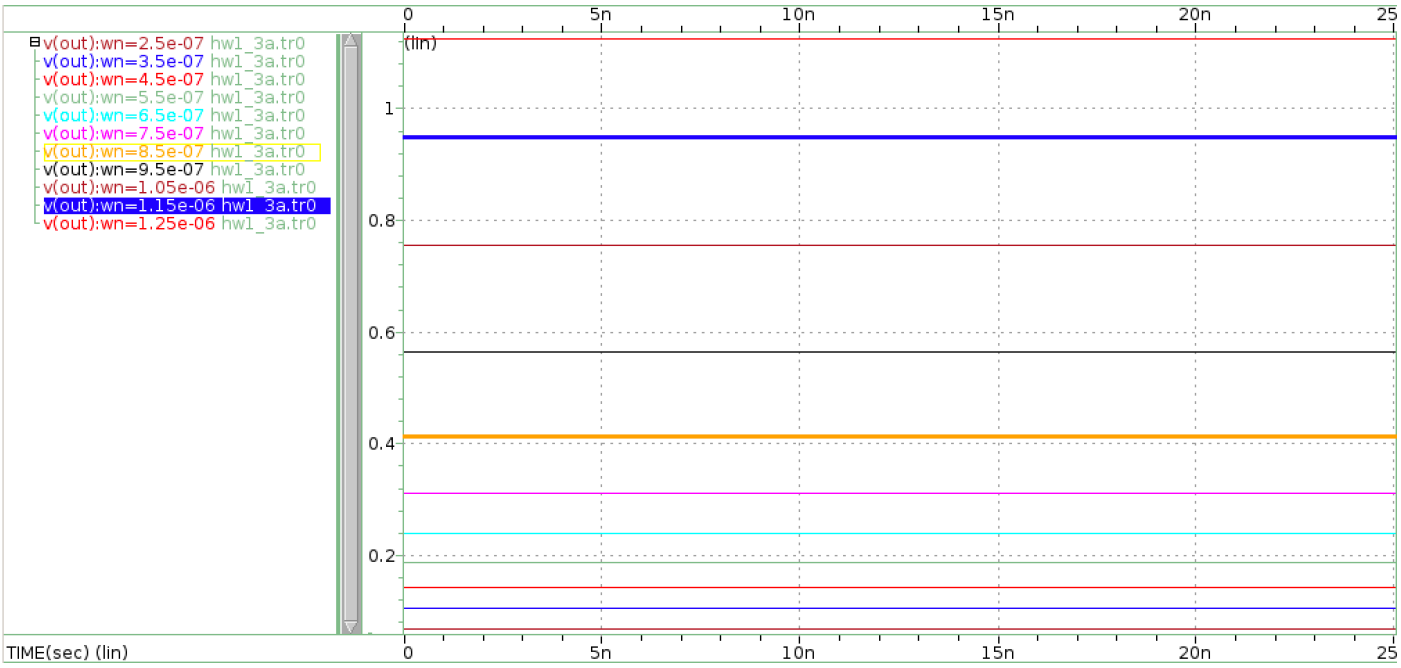
self-aligned poly-silicon gate: 就是先把 Gate 的 POLY 做好再做擴散，這樣自然會有通道產生，不需要額外的光罩去做通道，也比較不會有 Gate, Source, Drain 重疊而產生的寄生電容或 resistance，用 Gate 的 POLY 當作通道的遮罩

lightly-doped drain (LDD): 因為 GATE 愈做愈小，使得 source 和 drain 兩端的距離變得很近，若電位不變，使得電場強度因微縮而增大，因此在 GATE 兩端接面間的載子很容易就會受到這樣的大電場而被加速，形成熱載子，而造成導通，為了避免大量的熱載子產生，便將 GATE 兩旁 S/D 緊鄰 GATE 的地方做極輕度的摻雜，以降低接面載子數量，進而降低熱載子效應

3.

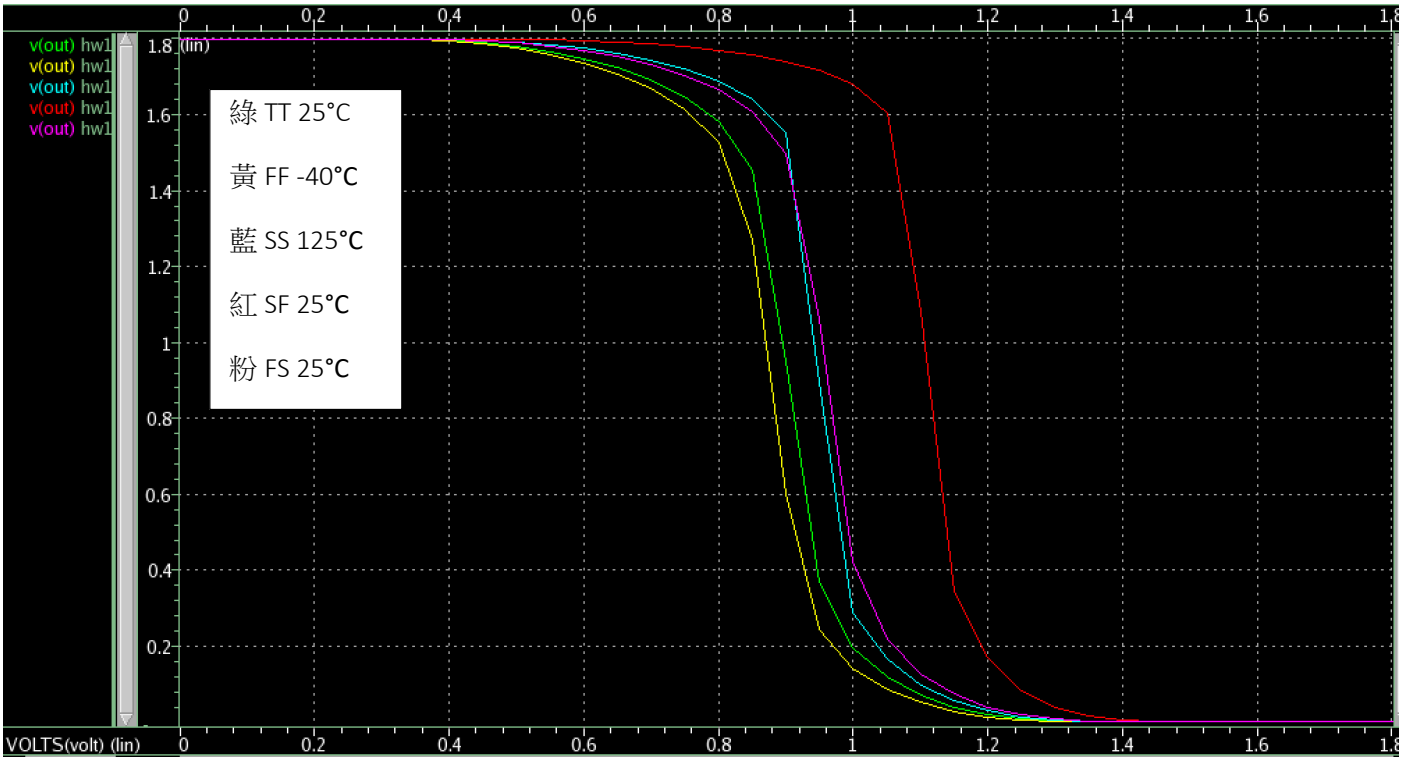
(a)

Width 約為 1.15u



單位 X 軸：sec　Y 軸：V

(b)



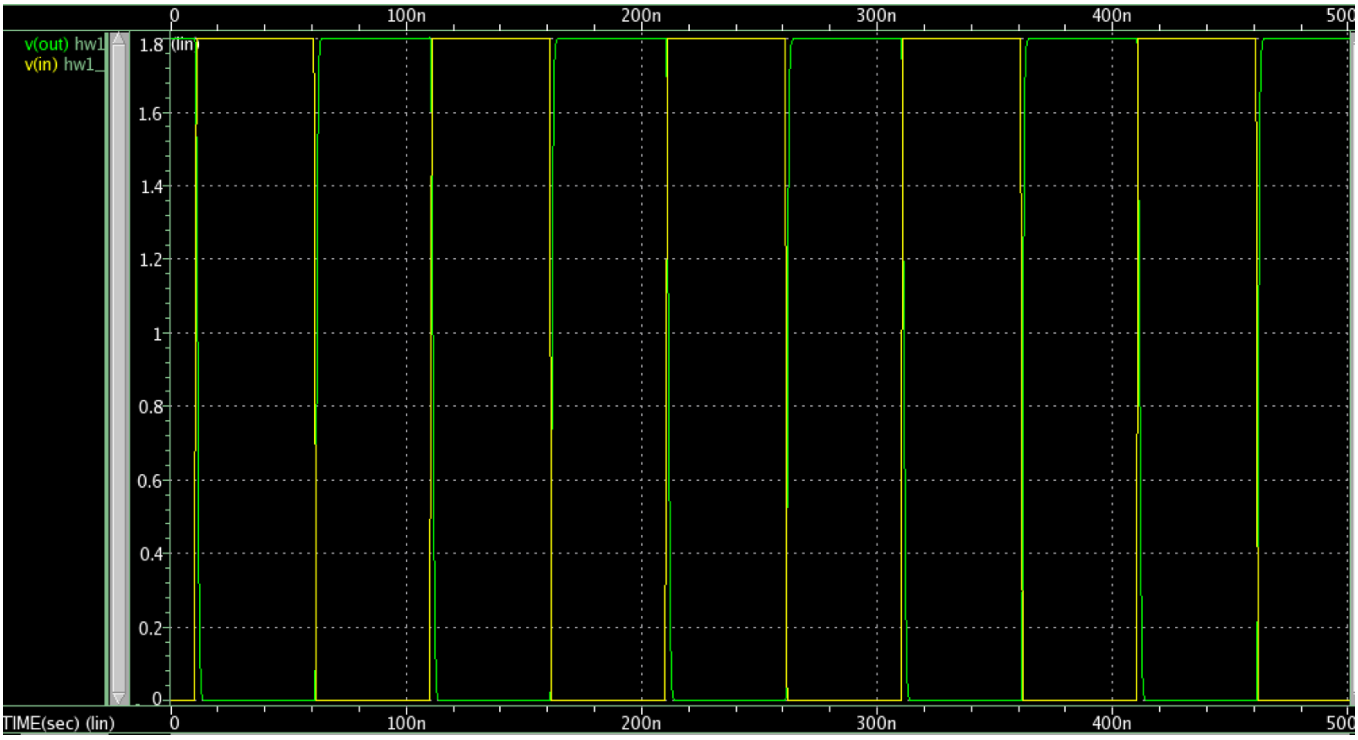
單位 X 軸：V　Y 軸：V

(C)

Process	Temperature	NMOS width 1X	NMOS width 5X
		Vout at Vin=0.5×VDD 單位：V	Vout at Vin=0.5×VDD 單位：V
TT	25°C	948m	74m
FF	−40°C	601m	58.5m
SS	125°C	1.55	92.1m
SF	25°C	1.74	1.24
FS	25°C	1.5	115m

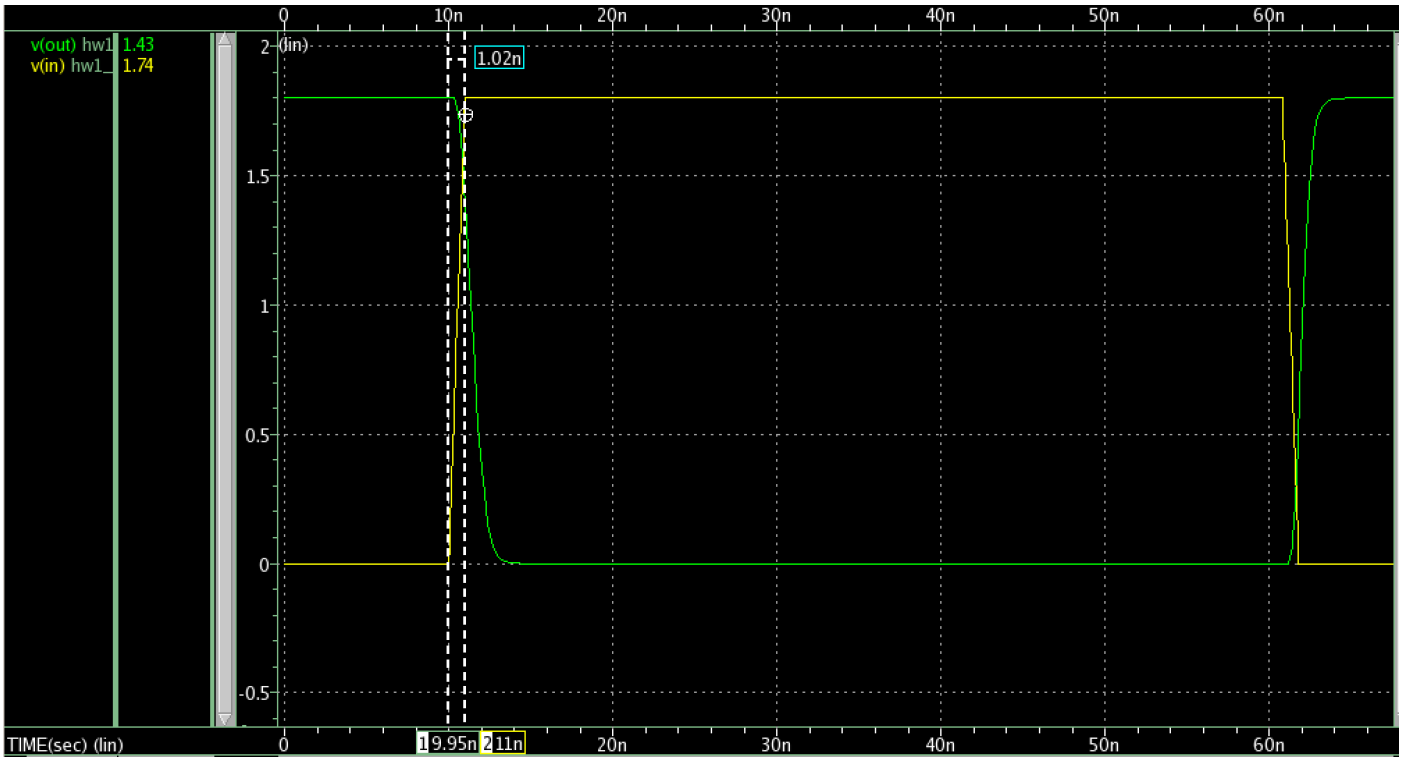
4.

TT 25°C 1X NMOS



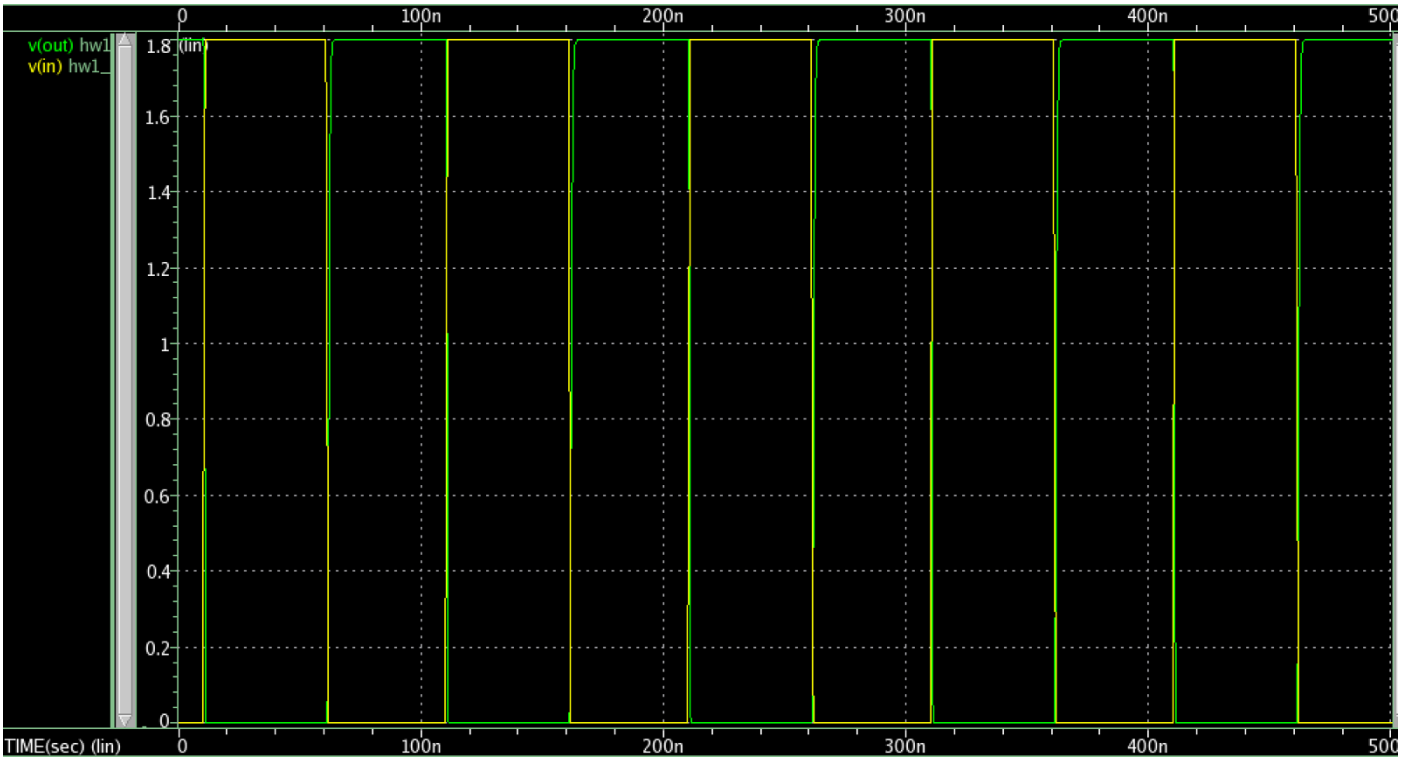
單位 X 軸：sec　Y 軸：V

Rise time:



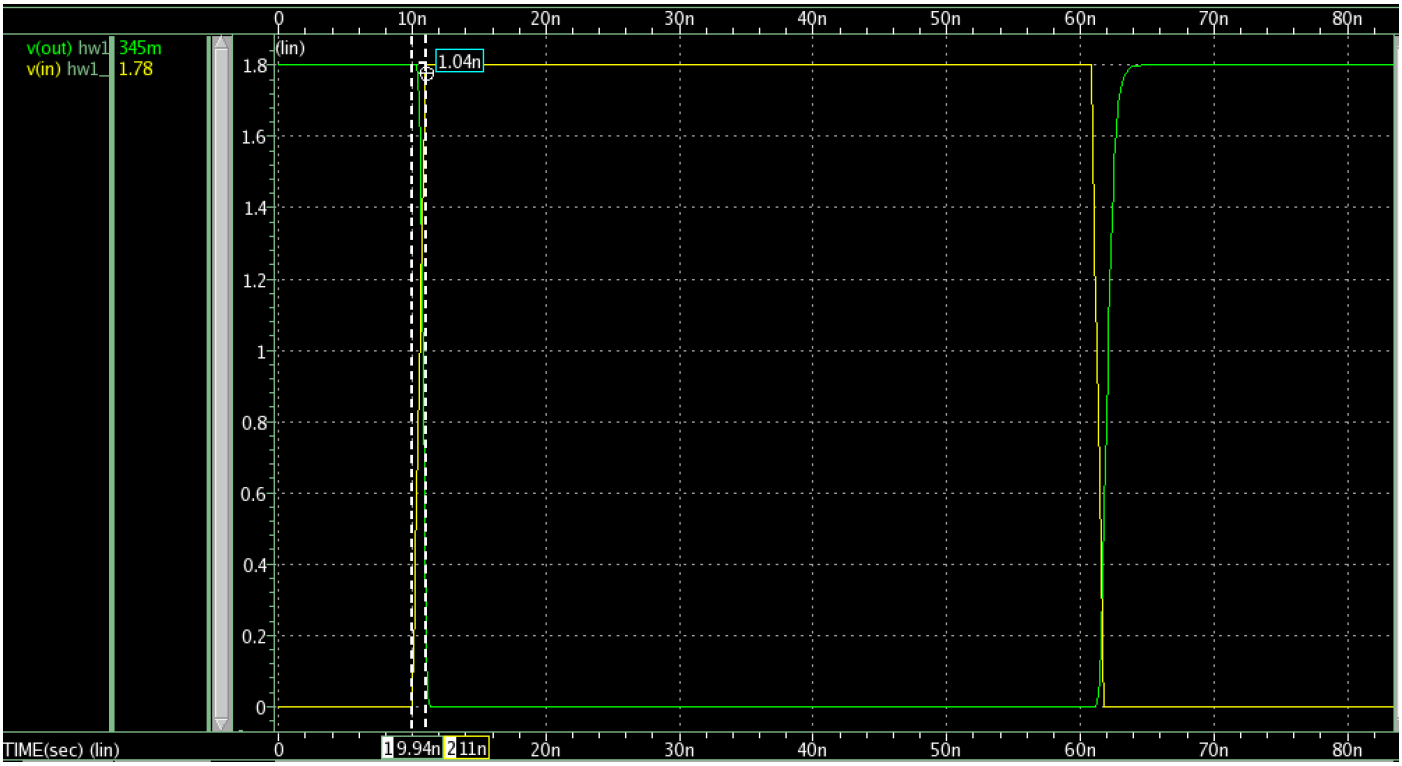
Fall time:

TT 25°C 5X NMOS

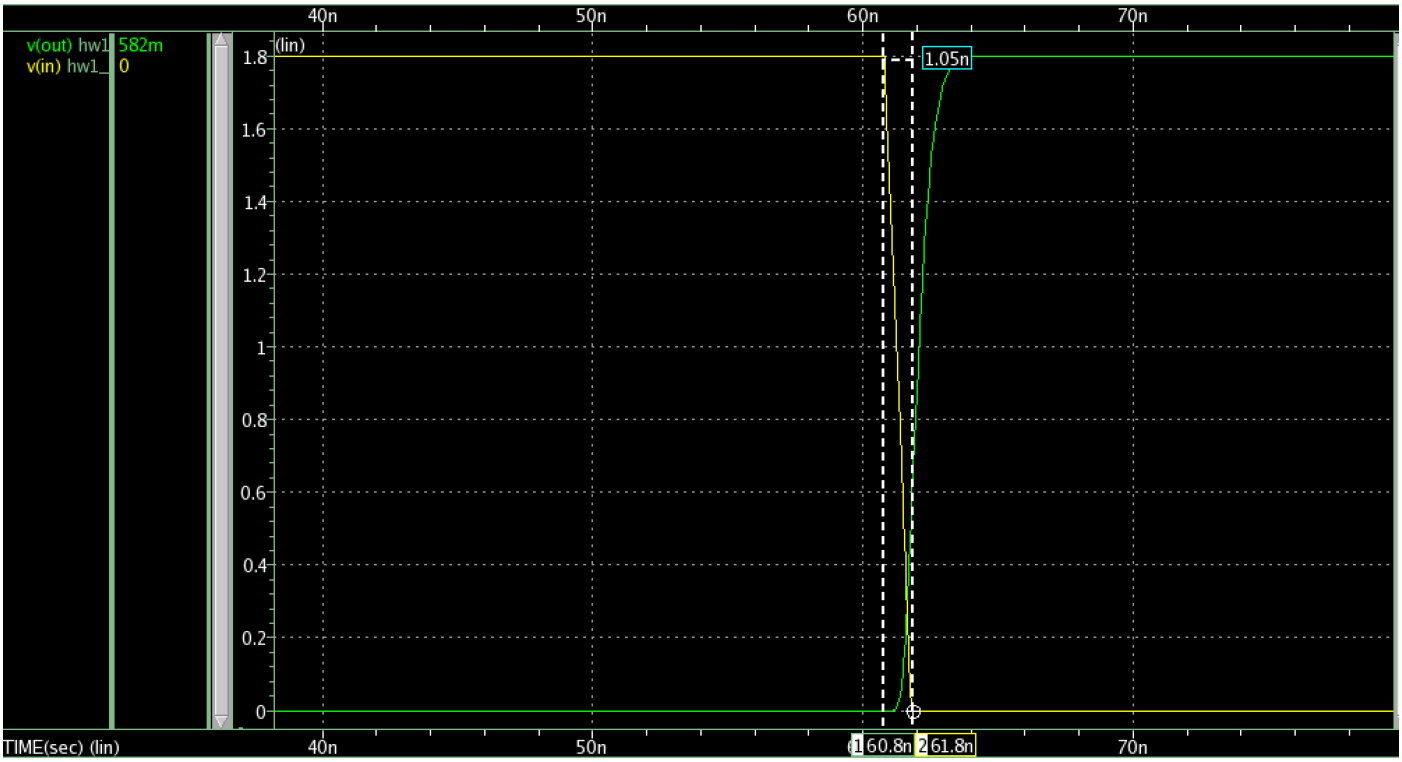


單位 X 軸：sec　Y 軸：V

Rise time:



Fall time:



Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay 單位：sec	Rise Delay 單位：sec	Fall Delay 單位：sec	Rise Delay 單位：sec
TT	25°C	930p	708p	287p	754p
FF	–40°C	692p	613p	196p	673p
SS	125°C	2.41n	1.37n	639p	1.43n
SF	25°C	2.01n	613p	562p	626p
FS	25°C	1.06n	660p	334p	713p