**106010006 黃詩瑜 電機 21**

# Pre-Lab 3: Counters and Shift Registers I

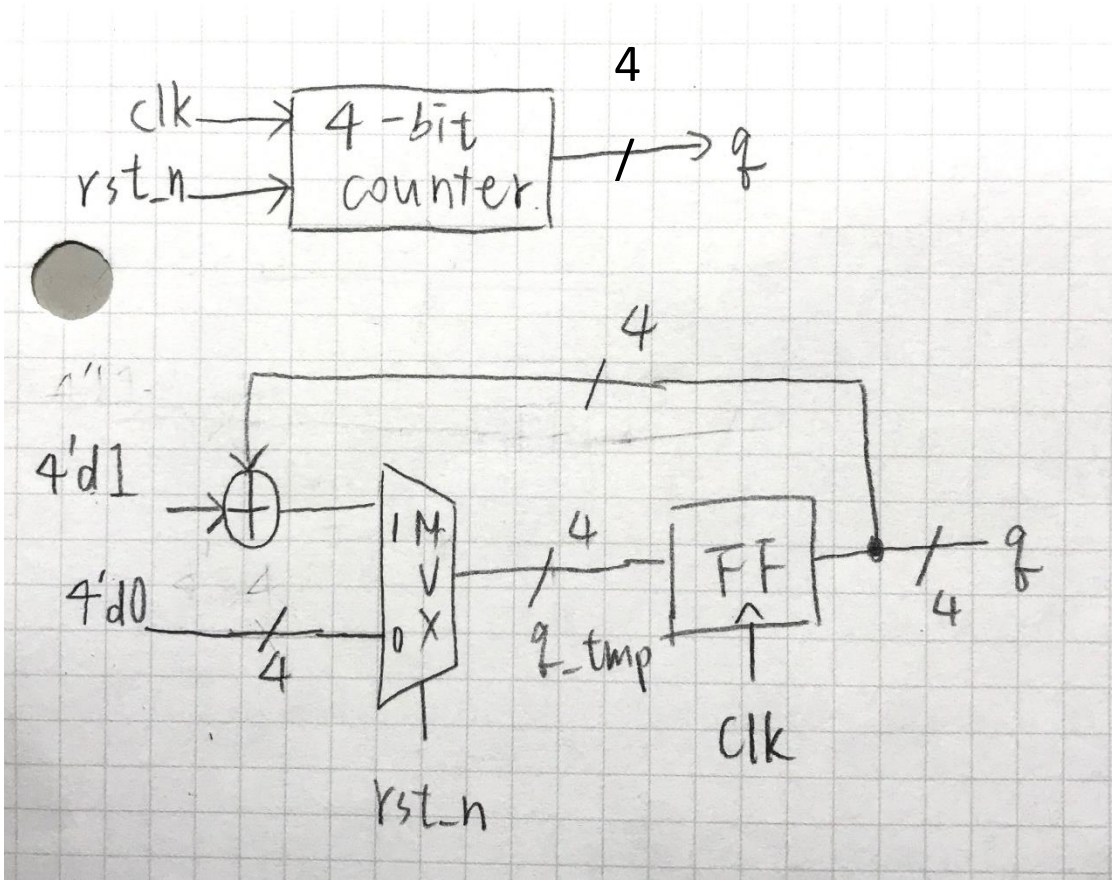
**1. Consider a 4-bit synchronous binary up counter.**

## Design Specification:

Input: rst_n, clk

Output: [3:0]q

**1.1 Draw the logic diagram**




**1.2 Construct Verilog RTL representation for the logics with verification.**

## Module code:

```
module prelab3_1(
q, // output
clk, // global clock
rst_n // active low reset
```

```
);
output [3:0] q; // output
input clk; // global clock
input rst_n; // active low reset
reg [3:0] q; // output (in always block)
reg [3:0] q_tmp; // input to dff (in always block)
// Combinational logics
always @*
q_tmp = q + 4'd1;
// Sequential logics: Flip flops
always @(posedge clk or negedge rst_n)
if (~rst_n) q<=4'd0;
else q<=q_tmp;
endmodule
```

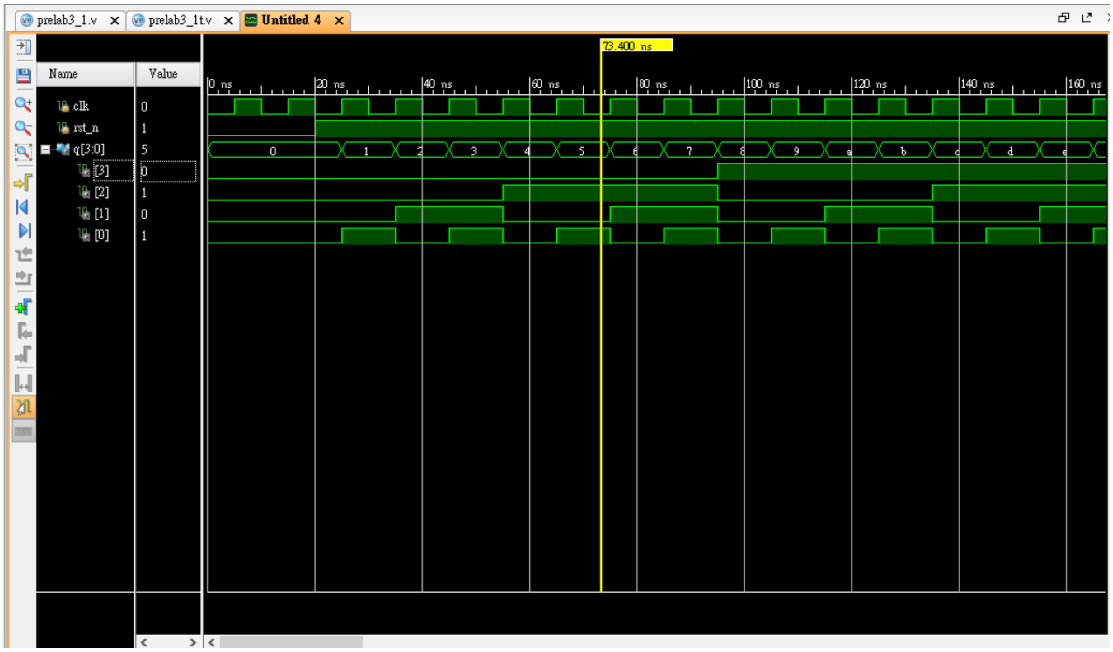
## Testbench:

```
module prelab3_1t;
reg clk,rst_n;
wire [3:0]q;
prelab3_1 U0(.q(q),.clk(clk),.rst_n(rst_n));

initial begin
clk=0;
forever #5 clk=~clk;
end

initial begin
rst_n=0;
#20;
rst_n=1;
end
endmodule
```

## 波形圖:

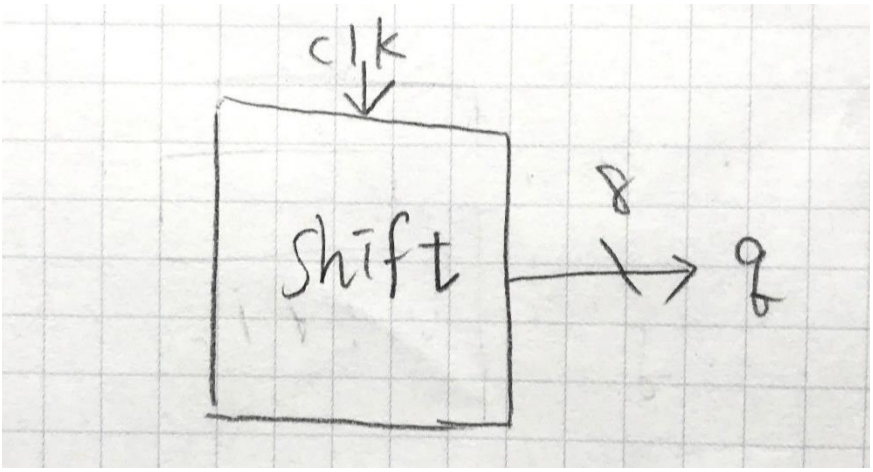


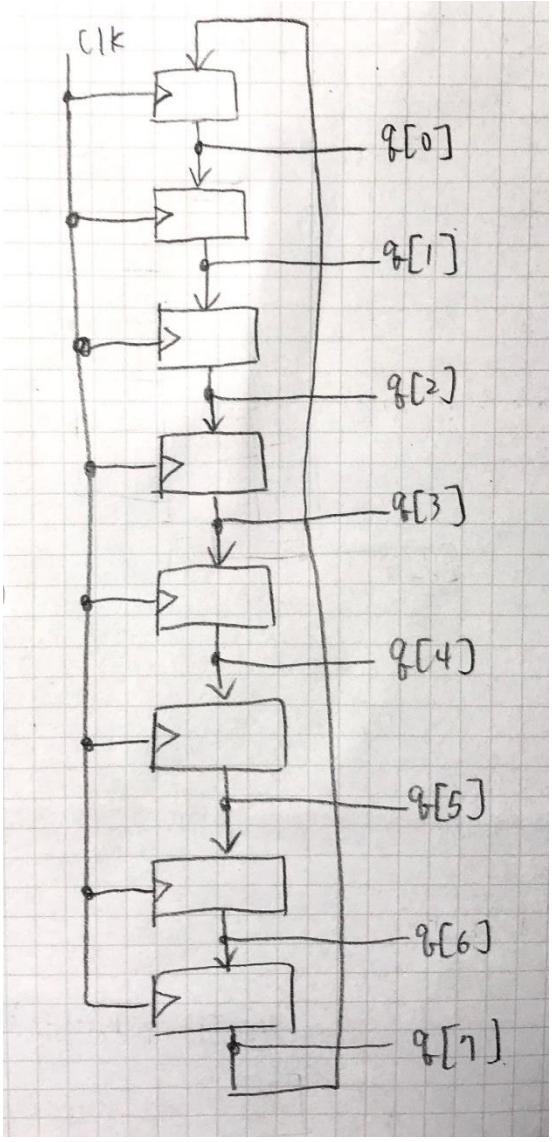

2. **Cascade eight DFFs together as a shift register. Connect the output of the last DFF to the input of the first DFF as a ringer counter. Let the initial value of DFF output after reset be 01010101. Construct the Verilog RTL representation for the logics with verification.**

## Design Specification:

Input: clk , rst_n

Output: [7:0]q






**Module code:**

```
module prelab3_2(
q, // shifter output
clk, // global clock
rst_n // active low reset
);
output [7:0] q; // output
input clk; // global clock
input rst_n; // active low reset
reg [7:0] q; // output
// Sequential logics: Flip flops
always @(posedge clk or negedge rst_n)
```

```
if (~rst_n)
begin
q<=8'b01010101;
end
else
begin
q[0]<=q[7];
q[1]<=q[0];
q[2]<=q[1];
q[3]<=q[2];
q[4]<=q[3];
q[5]<=q[4];
q[6]<=q[5];
q[7]<=q[6];
end
endmodule
```

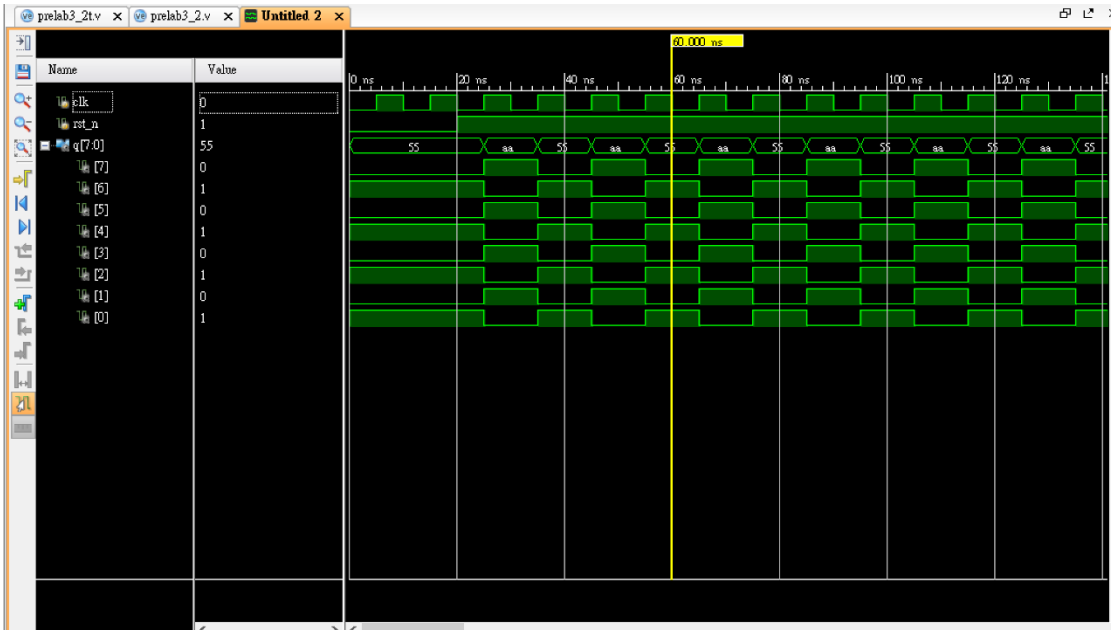
## testbench:

```
module prelab3_2t;
reg clk,rst_n;
wire [7:0]q;
prelab3_2 U0(.q(q),.clk(clk),.rst_n(rst_n));

initial begin
clk=0;
forever #5 clk=~clk;
end

initial begin
rst_n=0;
#20;
rst_n=1;
end
endmodule
```

## 波形圖:


prelab3_2t.v
prelab3_2.v
Untitled 2
Name
Value
clk
rst_n
q[7:0]
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
0
1
55
0
1
0
1
0
1
0
1
60.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
55
aa