



SCHEME AND SYLLABUS - B.E. COMPUTER ENGINEERING

Course Code	Type	Subject	L	T	P	Credits	CA	MS	ES	CA	ES	Pre-requisites
CEC03	CC	Digital Logic Design	3	0	2	4	15	15	40	15	15	None

COURSE OUTCOMES

1. To be able to design a fairly complex digital system from a set of specifications or a description of the system
2. To be able to analyze, test and troubleshoot a digital system
3. To be proficient in using the design tools used in industry to synthesize the digital circuits.

COURSE CONTENT

Introduction to Digital Systems

Number Systems and Codes: Binary, octal and hexadecimal number systems, Number-Base Conversions, Complements of Numbers, Signed numbers, Fixed and floating point numbers, Binary Arithmetic, Binary Codes: BCD, Gray, Excess-3, ASCII, Error detection and correction codes - parity check codes and Hamming code.

Combinatorial Logic Systems: Basic logic operation, Logic gates and Truth tables, Positive and Negative Logic, Boolean Algebra: Basic postulates and fundamental theorems, SOP and POS forms, Min terms, Max terms, Canonical Form, Gate level Minimization: K-map and Quine-McCluskey tabular methods, NAND/NOR implementations

Design Concepts using Hardware Description Language: VHDL Programming Structure, Model, Test Bench, Simulation Tool

Combinational Logic Modules, their applications and VHDL Modeling: Decoders, encoders, multiplexers, demultiplexers, Parity circuits, Comparators, Code Converters, Arithmetic modules- adders, subtractors, BCD Adder, ALU and multipliers, Implementing boolean function with multiplexers / decoders

Introduction to different logic families: Operational characteristics of BJT and MOSFET as switch, Structure and operations of TTL and CMOS gates, Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation



SCHEME AND SYLLABUS - B.E. COMPUTER ENGINEERING

delay, transition time, power consumption and power-delay product etc, Gates with Open Collector/Drain outputs, Tristate logic gates

Sequential Logic systems and VHDL Modeling: Basic sequential circuits- latches and flip-flops: RS-latch, SR-flipflop, D-latch, D flip-flop, JK flip-flop, T flip-flop, Setup-time, HOLD Time, Propagation delay, Timing hazards and races, Characteristic Equations

Sequential logic modules, their applications and VHDL Modeling: Multi-bit latches and registers, shift register: Bidirectional, Universal and Ring Counter; counters: Ripple, Up/Down, Mod N, BCD Counters etc.

State machines: Definition, Classification: Mealy, Moore; Analysis of state machines using D flip-flops and JK flip-flops, Design of state machines - state table, state assignment, transition / excitation table, excitation maps and equations, logic realization, State machine design using State Diagram, and using ASM charts, Design examples

Memory: Read-only memory, Read/Write memory - SRAM and DRAM, EPROM, EEPROM, USB Flash drive

Advanced Topics: synchronous sequential circuits, Testing and testability of logic circuits, Programmable Logic Devices: PROM, PLA, PAL, GAL, SPLDs, CPLDs and their applications, State-machine design with sequential PLDs, FPGAs

Guidelines for Practical Work: In the practical portion of this course, students will use VHDL to model digital systems in a simulator. Students will model basic gates, combinational circuits, sequential circuits, memory and state machine based designs.

1. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL Design", 3rd Edition, McGraw-Hill
2. R.J. Tocci., N.S.Widmer, G.L. Moss, "Digital Systems, Principles and Applications", 11th Edition, Pearson Education
3. M. Morris Mano and Michael D. Ciletti, "Digital Design", 5th Edition, Pearson
4. Mohammed Ferdjallah, "Introduction to Digital Systems: Modeling, Synthesis, and Simulation Using VHDL", Wiley.