Date: Roll No. 2n(we/19

B.E (ECE/COE) END-SEMESTER EXAMINATION 2016

ECE/COE-214

DIGITAL CIRCUITS AND SYSTEMS I

Time: 3:00 Hrs M.M.: 70

Attempt any TEN questions. All questions carry equal marks.

Q[1] Using the Quine-McClusky (Tabulation) method minimize the function given below having don't care terms

$$f(w,x,y,z) = \prod_{M}(1,3,9,11,12,13) + don't\,care(2,10,14,15)$$

Q[2] Design a multiplier that multiplies two numbers of two bit each and and implement it by using complimentary output decoder of suitable size and AND/NAND gates.

Q[3] Design a circuit that converts 2421 code to BCD code and implement it using NAND gates only.

Q[4] Using a positive edge triggered AB flip flop (whose characteristic table is given) design *a synchronous mod-5 counter* whose counting sequence is

$$110 \rightarrow 101 \rightarrow 111 \rightarrow 001 \rightarrow 011 \rightarrow 110$$

A	B	$Q(t+1)$
0	0	0
0	1	$\overline{Q}(t)$
1	0	$Q(t)$
1	1	1

Table 1: Table for AB Flip-flop

Q[5] Design a register, incorporating four multiplexers and four positive edge triggered D flip-flop, having the behavior specified by table 2.

Q[6] Implement 4 bit Ring counter and Johnson counter using J-K flip flop and also give their applications.

Q[7] Design and implement a circuit using gates to identify the error in (7,4) Hamming code.

Select lines		Register operation
S_1	S_2	
0	0	Compliment content
0	1	Synchronous clear
1	0	Hold
1	1	Circular shift left

Table 2: Table for shift register

Q[8] Explain with the help of circuit diagram the operation of a Emitter Coupled Logic (ECL) 3 input OR/NOR gate. Show that the transistors in this circuit operate in the active region and not in saturation. Calculate the noise margins. Find the average power dissipated by the gate. Assume a base-emitter voltage of 0.7 V for a transistor conducting in active region.

Q[9] Explain in detail the gated version of Mono stable Multi-Vibrator. Design the MMV circuit for the pulse of duration 1 μs.

Q[10] Explain with the help of diagram the dual slope A/D convertor.

Q[11] A D/A converter has a full scale analog output of 12 V and accepts eight binary bits as inputs. Find the voltage corresponding to each analog step.
Explain with the help of a diagram ladder type R-2R digital to analog convertor.

Q[12] Explain in detail the invertor circuit fabricated by using the following logic families:
(i) Integrated Injection Logic (IIL)
(ii) CMOS

Q[13] Write short notes on the transistorized version of the Schmitt Trigger citcuit.

Q[14] Explain in detail the storage and erasure mechanism of an EEPROM cell.

Date:

Roll No.

B.E (ECE/COE) END-SEMESTER EXAMINATION 2015

ECE/COE-214

DIGITAL CIRCUITS AND SYSTEMS I

Time: 3:00 Hrs

M.M.: 70

Attempt any TEN questions. All questions carry equal marks.

Q[1] Using the Quine-McClusky (Tabulation) method minimize the function given below having don't care terms

$$f(w,x,y,z) = \sum_m (0,6,7,8,9,13) + d(3,5,10,15)$$

Q[2] Design a code convertor that converts 84-2-1 code into 8421 code and implement it by using 4X1 MUXs and external gates.

Q[3] Design a synchronous mod-10 counter whose counting sequence corresponds to the 2421 code using negative edge triggered J-K flip-flops.

Q[4] Explain the totem-pole output configuration for a TTL gate. How is propagation delay reduced by this configuration.

Q[5] Two numbers A and B are of two bit each. Design a circuit to implement the function $X = \frac{A}{B}$ where $B \neq 0$ and X is an integer. Implement the circuit by using NOR gates only.

Q[6] Design a logic circuit using decoder that generates the 3 parity bits for hamming code when the messages are 4 bit BCD codes.

Q[7] Explain with the help of diagram the successive approximation A/D convertor.

Q[8] Explain the following parameters:
(a) Propagation Delay
(b) Noise Margin
(c) Fan-out
(d) Power dissipation

Q[9] Draw the circuit diagram for a CMOS circuit that realizes the Boolean expression

$$f(w,x,y,z) = [\overline{(w+x)}.z + \bar{y}\bar{z}]$$

Q[10] Design an astable multivibrator with NPN switching transistors having $h_{FE(min)} = 30$ to operate at frequency 150 KHz with a power supply of 12 V. Also explain its working.

Q[11] Explain with the help of a diagram weighted resistor digital to analog convertor. Using suitable example also explain the parameters (i) settling time (ii) accuracy.

Q[12] Implement the following functions using a cost efficient PLA assuming both true and complementary form are available at the output. Draw PLA table.

$$F1(A,B,C,D) = \sum_m(0,1,2,3,6,7)$$
$$F2(A,B,C,D) = \sum_m(0,1,2,3,8,9)$$
$$F3(A,B,C,D) = \sum_m(0,1,6,7,14,15)$$

Q[13] What do you understand by timing sequences. How are they generated. What are their applications.

Q[14] Explain in detail the storage and erasure mechanism of an EPROM cell.

Date: Roll No.

B.E (ECE/COE) END-SEMESTER EXAMINATION 2014

ECE/COE-214

DIGITAL CIRCUITS AND SYSTEMS I

Time: 3:00 Hrs M.M.: 70

Attempt any TEN questions. All questions carry equal marks.

Q[1] Using the Quine-McClusky (Tabulation) method minimize the function given below having don't care terms

$$f(w,x,y,z) = \prod_{M}(0,6,7,8,9,13) + d(5,15)$$

Q[2] Design and implement an adder that adds two numbers of two bit each using complimentary output decoder of suitable size and AND/NAND gates.

Q[3] Design a combinational logic circuit that detects the presence of any of the six illegal code groups in the 2421 code by providing a logic-1 output. Implement it by using NOR gates only.

Q[4] Explain with the help of circuit diagram the operation of a Emitter Coupled Logic (ECL) 3 input OR/NOR gate. Show that the transistors in this circuit operate in the active region and not in saturation. Calculate the noise margins. Find the average power dissipated by the gate. Assume a base-emitter voltage of 0.7 V for a transistor conducting in active region.

Q[5] A panel light in the control room at the launching of a satellite is to go on if and only if the pressure in both the fuel and the oxidizer tanks is equal to or above a required minimum and there are 10 min or less to liftoff, or if the pressure in the oxidizer tank is equal to or above a required minimum and the pressure in the fuel tank is below a required minimum but there are more than 10 min to liftoff, or of the pressure in the oxidizer tank is below a required minimum but there are more than 10 min to liftoff. Design a combinational network to control the panel light.

Q[6] A D/A convertor has a full scale analog output of 10 V and accepts six binary bits as inputs. Find the voltage corresponding to each analog step.
Explain with the help of a diagram ladder type R-2R digital to analog convertor.

Q[7] Explain with the help of diagram the dual slope A/D convertor.

Q[8] Explain in detail the gated version of Mono-stable Multi-Vibrator.

Q[9] Design and implement the arbitrary counter, using J-K flip-flop, with self starting and self correcting conditions. The states through which the counter goes are

$001 \rightarrow 000 \rightarrow 011 \rightarrow 111 \rightarrow 100 \rightarrow 001$

Q[10] Design a circuit that converts excess-3 code to BCD code and implement it by using four 4X1 Multiplexers and external gates.

Q[11] Implement 4 bit Ring counter and Johnson counter using S-R flip flop and also give their applications.

Q[12] With the help of suitable diagram explain the tri-state logic of TTL logic family.

Q[13] Write short notes on the transistorized version of the Schmitt Trigger citcuit.

Q[14] Design a register, incorporating four multiplexers and four positive edge triggered D flip-flop, having the behavior specified by table 1.

Select lines		Register operation
S_1	S_2	
0	0	Hold
0	1	Synchronous preset
1	0	Complement contents
1	1	Parallel input

Table 1: Table for shift register

ECE/COE 214

DIGITAL CIRCUITS AND SYSTEMS I

Time: 3:00 Hrs M.M.: 70

Attempt any TEN questions. All questions carry equal marks.

Q[1] Using the Quine-McClusky (Tabulation) method minimize the function given below having don't care terms

$$f(w,x,y,z) = \sum_m (1,5,6,12,13,14) + d(0,2,4)$$

Q[2] Implement the function

$$F(a,b,c,d) = a\bar{b} + acd + b\bar{c} + d$$

using MUX of size 4×1, and external gates.

Q[3] Design a circuit that converts Excess-3 code to BCD code and implement it using NAND gates only.

Q[4] What are the advantages of TTL over DTL and how are they achieved.

Q[5] Using an approach similar to that for the design of a single decade 8421 BCD adder, design a single decade adder in which the operand digits are in excess-3 code.

Q[6] Design a synchronous mod-10 counter whose counting sequence corresponds to the 84-2-1 code using positive edge triggered J-K flip-flops.

Q[7] Convert a positive edge triggered T flip-flop into a positive edge triggered AB flip-flop whose characteristic table is given.

A	B	$Q(t+1)$
0	0	0
0	1	$\overline{Q}(t)$
1	0	$Q(t)$
1	1	1

Q[8] Explain the following parameters:

(a) Propagation Delay
(b) Noise Margin
(c) Fan-out
(d) Power dissipation

Q[9] Draw the circuit diagram for a CMOS circuit that realizes the Boolean expression

$$f(w,x,y,z) = [(w + \bar{x})y + \bar{y}\bar{z}]$$

Q[10] Design a logic circuit using decoder that generates the 3 parity bits for hamming code when the messages are 4 bit BCD codes.

Q[11] Explain with the help of a diagram weighted resistor digital to analog convertor. Using suitable example also explain the parameters (i) resolution (ii) Linearity.

Q[12] Explain in detail with the help of diagram the successive approximation A/D convertor.

Q[13] Write short notes on transistorized implementation of Astable multivibrator.

Q[14] Explain in detail the storage and erasure mechanism of an EEPROM cell.

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FOURTH SEMESTER B.E. (COE/EC)

2ND SEMESTER EXAMINATION MAY-2009

COE/EC-214 DIGITAL CIRCUITS & SYSTEMS

Time: 3 Hours Max. Marks : 70

Note : Answer any *FIVE* questions.
Assume suitable missing data, if any.

1 [a] Given the function f(A,B,C,D) = ∑m (0,4,9,10,11,12) and f_1 = B⊕D. Determine f_2 and f_3 such that $f = f_1 f_2 + f_3$. 7

[b] Using the Quine –McClusky method, minimize the function given below having don't care terms
$(w,x,y,z) = \sum m(1,5,7,9,13,15) + d(8,10,11,14)$ 7

2[a] Explain with the help of circuit diagram the operation of ECL OR/NOR gate. Show that the transistors in this circuit operate in the active region and not in saturation. Calculate the noise margins. Find the average power dissipated by the gate. Assume a phase –emitter voltage of 0.7 V for a transistor conducting in active region. 10

[b] Explain the operation of CMOS NAND gate. 4

3 Using a positive edge triggered AB flip-flop (whose characteristic table is given below), design a synchronous counter which counts as per Gray code sequence i.e. 000, 001, 011, 010, 110, 111, 101, 100, 000 etc. 14

4[a] Realize the Boolean expression
$f(w,x,y,z) = \sum m(0,2,4,5,7,9,10,14)$ using a multiplexer tree structure, the first level should consist of two 4-to-1 line multiplexers with variables w and z on their select lines s_1 and s_0 respectively and the second level should consist of single 2 to 1 line multiplexer with variable y on its select line. 7

[b] Design a register, incorporating four multiplexers and four positive edge triggered D-flip-flop having the behaviour specified

Select Line		Register operation
S_1	S_0	
0	0	Hold
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right

5[a] Explain with the help of diagram the successive approximation A/D converter. 7

[b] A D/A converter has a full scale analog output of 10V and accepts six binary bits as inputs. Find the voltage corresponding to each step. 4

[c] Differentiate between linearity & accuracy in case of D/A converter. 3

6[a] Realize the following multiple output function using 3×4×2 PLA 6

$$f_1(x,y,z) = \sum m(0,1,3,5)$$

$$f_2(x,y,z) = \sum m(3,5,7)$$

[b] Explain the concept of Duality in Boolean algebra. 3

[c] A transmits Hamming code (even parity) for a BCD digit and B receives 0111100. Assuming that only one bit can be in error during the transmission, find out the BCD digit that was transmitted by A. 5

7[a] Explain the basic static RAM cell and dynamic RAM cell. 7

[b] Draw the diagram of Schmitt trigger ckt. constructed with either BJT or OP-AMP and explain the circuit operation. What is hystersis & how does it benefit in the Schmitt trigger? 7

8 Write short notes on any *TWO*: 7,7

[a] Monostable multivibrator

[b] Voltage to frequency converter

[c] Transistor-Transistor Logic

Total No. of Pages 2 *Roll No. .....*

FOURTH SEMESTER **B.E. (EC/COE)**

END SEM EXAMINATION ***May-2008***

EC/COE-214 DIGITAL CIRCUITS & SYSTEMS-I

Time: 3:00 Hours ***Max. Marks : 70***

Note : Answer any ***FIVE*** questions.
Attempt all parts of a question in continuity.
Assume suitable missing data, if any.

1[a] Identify the prime and essential prime implicants for the following functions
$S=f(a,b,c,d)=\sum m(1,5,7,8,9,10,11,13,15)$ **2**

[b] Simplify using K-map
$I=f(d,e,f,g,h) = \prod M(5,7,8,21,23,26,30) + \prod D(10, 14,24,28)$ **4**

[c] Design a combinational logic circuit to find the 9's complement of a BCD number and implement the circuit using NOR gates only. **8**

2[a] Design a transistorized (using npn transistor) monostable multivibrator to generate a pulse of 0.1μsec. **7**

[b] Explain the principle of the EPROM and EEPROM. State the difference between the two. **7**

3[a] Using the Quine-McClusky (Tabulation) method, minimize the function given below having don't care terms.
$F(x,y,z) = \prod M (0,2,3,4,5,12,13) + \text{don't care } (8,10)$ **9**

[b] Design a three input, one output minimal two level gate combinational network that has a logic-1 output when the majority of its inputs are logic-1 and has a logic-0 output when majority of its inputs are logic-0. **5**

4[a] Using OR gates and /or NOR gates along with a 3-to-8 line decoder with true outputs realize the given functions.
$f(x,y,z) = \prod M(1,2,5); \quad g(x,y,z) = \prod M(0,4,5,6,7)$

The gates should be selected so as to minimize their total number of input terminals. **6**

[b] Explain the operation of Schmitt Trigger using BJT with the help of appropriate circuit diagram. 8

5[a] Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to square of input number using ROM. 7

[b] Explain a 4-bit R-2R ladder type D/A converter in detail. Describe the various specifications of D/A converter. 7

6[a] Explain with the help of circuit diagram the operation of a TTL-3 input NAND gate with tristate logic and the totempole output stage. 10

[b] Explain the following characteristics of the logic families
(i) Propagation delay (ii) Noise Margin
(iii) Power dissipation (iv) Fan Out. 4

7[a] Design a synchronous mod-10 counter whose counting sequence correspond to 8, 4, -2, -1 code using positive edge triggered T flip-flop. 6

[b] The following serial data are applied to flip-flop as shown in Fig.1 What will be resulting serial data that will appear on the Q output of the flip-flop.
Assume initially Q=0 and there is one clock pulse for each bit time.
J_1 = 101101; J_2= 0111010; J_3=1111000
K_1=0001110; K_2 1101100; K_3= 1010101 3

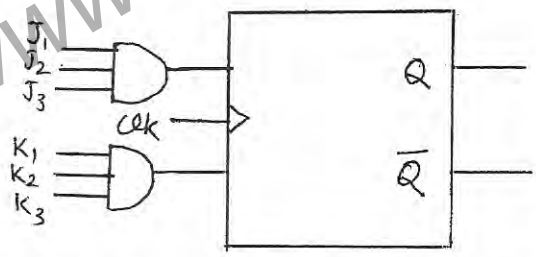

Fig. 1

[c] What do you understand by universal shift register? Explain its working with appropriate circuit and timing diagrams. 5

8 Write short notes on:
(i) Static RAM and Dynamic RAM
(ii) Dual slope A/D converter and its application as V-F converter. 2x7