Shikhar Tuli

PhD Candidate
Electrical Engineering
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Academic Details

Year	Degree	Institute	CGPA/Percentage
2020-Present	Ph.D. in Elec. and Comp. Eng.	Princeton University	3.9/4.0
2016-2020	B.Tech in Electrical Engineering	Indian Institute of Technology Delhi	9.5/10.0
2016	Class XII, CBSE	Amity International School	96.6%
2014	Class X, CBSE	Amity International School	10.0/10.0

Research Interests

- **Efficient Machine Learning:** Exploring diverse models and hardware architectures for efficient training and inference.
- **Edge Computing:** Applying machine learning techniques to optimize the full stack: from transistor to the cloud.
- **Other:** Neuro-inspired AI, Neuro-symbolic AI, Embedded Systems, and Nanoelectronics.

Professional Appointments

- Research Associate at CoCoSci Lab, under the supervision of Prof. Tom Griffiths. *Jan 2021 - July 2021*
- Research Associate at NAITS Lab under the supervision of Prof. Debanjan Bhowmik. *Jan 2020 - July 2020*
- Research Associate at ESL, under the supervision of Prof. David Atienza. *May 2019 - Aug 2019*
- Research Associate at DWLCL, under the supervision of Prof. Abhisek Dixit. *May 2018 - Nov 2019*
- Research Associate at CLOUDS Lab, under the supervision of Prof. Rajkumar Buyya. *May 2018 - July 2019*
- Founder and CEO. Qubit Inc. *Jan 2020 - Present*
- Research Consultant. Coral Telecom Ltd. *Apr 2016 - Nov 2021*

Awards and Achievements

- Received **Pramod Subramanyan *17 Early Career Graduate Award** at Princeton University.
- Awarded **Ph.D. Fellowship** for the first year of study.
- Received **Rajiv Bhambawale Award for Best B.Tech thesis** at the undergraduate level.
- Awarded **ThinkSwiss Research Scholarship** for a summer internship at Embedded Systems Laboratory (ESL), EPFL under the E3 program.
- Received **Summer Undergraduate Research Award** for outstanding research at undergraduate level.
- Received **Design Innovation Summer Award** (DISA 2017) and **DIT Seed Grant** at undergraduate level.
- Placed among the **Top 7%** of IIT Delhi in the first, second, fifth, and seventh semesters based on academic performance.
- Won **2nd Runners Up**, **Best Mechanical Design Award**, and **Best Technical Report** Cash Prize for Bomb Disposal Robotics National Competition at IIT Kharagpur (December 2016).
- Secured **All India Rank 1624** in Joint Entrance Exam Advanced 2016 among 150,000 candidates.
- Awarded **Chairperson's Trophy** for being the **School Topper** with 96.60% in CBSE AISSCE XII standard.
- Awarded **All Rounder** for VIII and IX standard.
- Received **Best Alliance award** and **Rockwell Collin's Innovation award** for National Robotics Competition - First Tech Challenge in X standard.
- Awarded **Second Runners Up** position and **Award for Best Marketing** in F1 in schools national competition in which students design, manufacture, and race with miniature Formula 1 cars.

Selected Research Projects

Exploration of the Transformer design space — Prof. Niraj K. Jha, Princeton University
Research Project — Dec 2021 - Present

Studying the effects of design decisions for transformers along with various training recipes in order to find the best architecture for each common task in the natural language processing domain. Heterogeneous and flexible architectures have shown to outperform traditional homogeneous and rigid models that have the same set of hyperparameters across all layers in the network. Resultant models are much smaller and energy-efficient (shown by accelerator implementations on RTL).

Co-design of CNNs and Accelerators — Prof. Niraj K. Jha, Princeton University
Research Project — Aug 2020 - May 2022

Designing and developing a novel framework that co-designs machine learning models (namely CNNs) along with the accelerator chip to which it would be mapped. Proposed novel neural architecture search techniques along with an expanded suit of CNN models and hardware accelerators for energy-efficient designs.

Inductive biases in CNNs and Transformers — CoCoSci Lab, Princeton University
Research Project — Jan - Jul 2021

Studied various human inductive biases on common computer-vision models including CNNs and transformers. Trained and evaluated models on the stylized Imagenet dataset to test shape/texture biases. Through a diverse set of experiments, it was found that transformers are superior models with improved inductive biases compared to CNNs. Github Repository link.

Supervised and Unsupervised Spiking Neural Networks — Prof. Debanjan Bhowmik, IIT Delhi
Research Project — Aug - Nov 2019

Simulated Supervised and Unsupervised Spiking Neural Networks employing STDP Learning rule (thesis link). Implemented code-level and circuit-level simulations of a novel neuromorphic system capable of learning common machine learning benchmarks.

Architectures of Emerging Non-Voltatile Memories — Embedded Systems Lab, EPFL
Summer Research Project — May - Nov 2019

Developed novel architectures for Emerging Non-Volatile Memories (NVMs) like RRAMs, STT-MRAMs, SOT-MRAMs, PC-RAMs, etc. For this, a Variability-Aware Controller (VAC) was proposed to asynchronously write to the NVM. This resulted in performance and energy improvements in low-power Edge applications. Computing overheads and implementing an adaptive and dynamic version of the VAC for further optimizing design-space parameters.

Modeling of HCI Degradation in GAA NWFETs — Prof. Abhisek Dixit, DWLCL, IIT Delhi
Summer Research Project (SURA) — May 2018 - Nov 2019

Investigated and modeled Hot-Carrier Injection based degradation effects in gate-all-around nanoWire FETs. Various model dependencies of device reliability were proposed for HCD in NWFETs. These models were backed by experimental study (using SMUs and WGFMUs) and physical justification. The project was under the Design and Wafer-Level Charectarization Lab (DWLCL), IIT Delhi and in collaboration with IMEC Leuven, Belgium (link).

FogBus — CLOUDS Lab, University of Melbourne
Remote Summer Research Project — May - July 2018

Developed a blockchain-based lightweight framework, named FogBus for Edge and Fog Computing, for end-to-end integration of IoT-Edge-Cloud. FogBus offers a platform independent interface to IoT applications and computing instances for execution and interaction. A Sleep Apnea analysis application was deployed using this framework for real time notification and diagnosis by analyzing pulse oximeter data. Github Repository link.

Coral IP-phone — Coral Telecom Pvt. Ltd.
Industrial Project — Aug 2020 - Nov 2021

Developing a VoIP phone with the use of system-on-module (SOM). integrating RGB TTL LCD with a capacitive touch panel, MIPI-CSI camera, PoE functionality, L2 switch, keyboard, speaker and mic onto the SOM. The phone supports all video calling features.

Coral Cloud — Coral Telecom Pvt. Ltd. and ST Microelectronics
Industrial Project — Jan - Mar 2018

Designed and developed a high availability and load-balanced, Electronic Private Automatic Branch Exchange (EPABX) for SIP communication using Free-Switch open source software. The system features no-single-point-of-failure with hot-swappable power supply (SMPS).

Publications

Updated list of publications with software repositories, datasets, and preprint links can be found on my website.

Refereed Conference and Workshop Publications

C7. NeurIPS '21 — Shreshth Tuli, Shikhar Tuli, Giuliano Casale and Nicholas R. Jennings. *Generative Optimization Networks for Memory Efficient Data Generation.* NeurIPS 2021 - Workshop on ML for Systems. [acc. rate: 9.2%]. link.

C6. CogSci '21 — Shikhar Tuli, Ishita Dasgupta, Erin Grant, and Thomas L. Griffiths. *Are Convolutional Neural Networks or Transformers more like human vision?* Annual Meeting of the Cognitive Science Society, 2021. [acc. rate: 18.2%]. link.

C5. ICONS '20 — Shikhar Tuli and Debanjan Bhowmik. *Design of a Conventional-Transistor-Based Analog Integrated Circuit for On-Chip Learning in a Spiking Neural Network.* International Conference on Neuromorphic Systems, 2020. link.

C4. ISCAS '20 — Shikhar Tuli and Shreshth Tuli. *AVAC: A Machine Learning based Adaptive RRAM Variability-Aware Controller for Edge Devices.* IEEE International Symposium on Circuits and Systems, 2020. link.

C3. ASP-DAC '20 — Shikhar Tuli, Marco Antonio Rios, Alexandre Sébastien Julien Levisse, and David Atienza Alonso. *RRAM-VAC: A Variability-Aware Controller for RRAM-based Memory Architectures.* Asia and South Pacific Design Automation Conference, 2020. link.

C2. Cloudcom '19 — Shreshth Tuli, Shikhar Tuli, Udit Jain, and Rajkumar Buyya, *APEX: Adaptive Ext4 File System for Enhanced Data Recoverability in Edge Devices.* International Conference on Cloud Computing, 2019. link.

C1. DAC '19 — Neetu Jindal, Sandeep Chandran, Preeti Ranjan Panda, Sanjiva Prasad, Abhay Mitra, Kunal Singhal, Shubham Gupta, and Shikhar Tuli, *DHOOM: Reusing design-for-debug hardware for online monitoring.* Design and Automation Conference, 2019. link.

Refereed Journal Publications

J6. MedRxiv '20 — Shreshth Tuli, Shikhar Tuli, Ruchi Verma, and Rakesh Tuli. *Modelling for prediction of the spread and severity of COVID-19 and its association with socioeconomic factors and virus types.* MedRxiv (2020). link.

J5. IoT '20 — Shreshth Tuli, Shikhar Tuli, Rakesh Tuli, and Sukhpal Singh Gill. *Predicting the Growth and Trend of COVID-19 Pandemic using Machine Learning and Cloud Computing.* Internet of Things (2020). link.

J4. ITL '20 — Shreshth Tuli, Shikhar Tuli, Gurleen Wander, Praneet Wander, Sukhpal Singh Gill, Schahram Dustdar, Rizos Sakellariou, Omer Rana, *Next Generation Technologies for Smart Healthcare: Challenges, Vision, Model, Trends and Future Directions*, Internet Technology Letters. link. **Top downloaded article award** link.

J3. IoT '20 — Sukhpal Singh Gill, Shreshth Tuli, Minxian Xu, Inderpreet Singh, Karan Vijay Singh, Dominic Lindsay, Shikhar Tuli, et al. *Transformative Effects of IoT, Blockchain and Artificial Intelligence on Cloud Computing: Evolution, Vision, Trends and Open Challenges*, Internet of Things, Volume 8. link.

J2. TED '20 — Charu Gupta, Anshul Gupta, Shikhar Tuli, Erik Bury, Bertrand Parvais, and Abhisek Dixit. *Characterization and modeling of Hot Carrier Degradation in N-Channel Gate-All-Around Nanowire FETs.* IEEE Transactions on Electron Devices, 2020. link.

J1. JSS '19 — Shreshth Tuli, Redowan Mahmud, Shikhar Tuli, and Rajkumar Buyya. *FogBus: A Blockchain-based Lightweight Framework for Edge and Fog Computing.* Journal of Systems and Software, Volume 154, 2019, Pages 22-36, link. **Top ten downloaded article of 2019 award** link.

Under Review and Work-in-progress Articles

W7. CogSci '23	Shikhar Tuli, Niraj K. Jha. *GiT: Can learning from good-old English grammar make Transformers more human-like?.* Cognitive Science, 2023.
W6. TCAD '23	Shikhar Tuli, Niraj K. Jha. *TransCODE: Co-designing Transformers and Accelerators.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023.
W5. TMC '22	Shikhar Tuli, Niraj K. Jha. *EdgeTran: Co-designing Transformers for Efficient Inference on Mobile Edge Platforms.* IEEE Transactions on Mobile Computing, 2022 (under review).
W4. TCAD '22	Shikhar Tuli, Niraj K. Jha. *AccelTran: A Sparsity-Aware Accelerator for Dynamic Inference with Transformers.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022 (under review).
W3. SciRep '22	Shikhar Tuli, Niraj K. Jha. *DINI: Data Imputation using Neural Inversion for Edge Applications.* Nature Scientific Reports: Special Track on Edge intelligence for the next generation Internet of Things, 2022 (under review).
W2. JAIR '22	Shikhar Tuli, Bhishma Dedhia, Shreshth Tuli, Niraj K. Jha. *FlexiBERT: Are Current Transformer Architectures too Homogeneous and Rigid?.* Journal of Artificial Intelligence Research, 2022 (under review; preprint link).
W1. TECS '22	Shikhar Tuli, Chia-Hao Li, Ritvik Sharma, Niraj K. Jha. *CODEBench: A Neural Architecture and Hardware Accelerator Co-Design Framework.* ACM Transactions on Embedded Computing Systems, 2022 (under review).

Patents

- *Low Cost Air Purification System*, Shikhar Tuli, Shreshth Tuli, Sujeet K. Sinha, IIT Delhi. Filed at the Indian Patent Office. Date: 2^{nd} August 2017, App. No.: 201711027523
- *Combination Lock with limited trial and resetting mechanism*, Shikhar Tuli, Shreshth Tuli, Harshit Abrol, Shivang Dwivedi, Saujanya Chaudhary, Kargil Singh, Sivanandam Aravindan IIT Delhi. Filed at the Indian Patent Office. Date: 10^{th} August 2017, App. no.: 201711028520

Reviewing

I have served as a reviewer for many journals and conferences. See my Publons profile at this link.

- Wiley: Software Practices and Experience (4)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (3)
- IEEE Transactions on Emerging Topics in Computing (1)
- IEEE Transactions on Industrial Informatics (1)
- International Conference on Machine Learning (1)
- Annual Meeting of the Cognitive Science Society (1)
- Conference on Information Sciences and Systems (1)

Teaching Experience

Department of Electrical and Computer Engineering, Princeton University:

- Machine Learning for Predictive Data Analytics. **Head T.A**. *Sep 2021 - Dec 2021.*

Department of Electrical Engineering, Indian Institute of Technology Delhi:

- Introduction to Electrical Engineering. **T.A**. *Jul 2019 - Nov 2019.*

Courses

- **Electrical Engineering:**
  Computer Architecture, Digital Electronics, Machine Learning and Intelligence, Analog Electronics, Physical Electronics, Power Electronics, Communication Engineering, Control Engineering, Engineering Electromagnetics, Signals and Systems, Electromechanics, Circuit Theory, IC Technology*, MOS VLSI Design*, Neuromorphic Engineering*, Mixed-Signal Circuit Design*, Compact modeling of Semiconductor Devices*, CMOS RF IC Design*, Digital Signal Processing†, Embedded Computing†.
- **Computer Science, Mathematics, Physics, and Cognitive Science:** Data Structures and Algorithms, Probability and Stochastic Processes, Calculus, Linear Algebra, Principles of Semiconductors, Computer Vision†, Machine Learning and Pattern Recognition†, Natural Language Processing†, Reinforcement Learning†, Probabilistic Models of Cognition†, Dynamics in Cognition†.

*Graduate-level course at IIT Delhi, †Graduate-level course at Princeton University

Technical Skills

- **Programming Languages:** Python, MATLAB, Java, C/C++, Verilog, RTL, x86 and ARM assembly, Verilog-A, PEL, OpenCL, HTML, R.
- **Frameworks:** PyTorch, Tensorflow, Keras, OpenCV, CUDA, Git, Xilinx Vivado, AnSYS HFSS, Synopsys Design Compiler, Capo Floor-planner, CACTI/FinCACTI, NVMain, NVSim, Keysight EasyEXPERT, Keysight IC-CAP, Altium Designer, Eagle, PSIM, Origin Pro, Adobe Photoshop, Adobe Illustrator, Arduino, Solidworks, Cinema 4D.

Positions of Responsibility

- **Technical Executive** at Makerspace: Design and Innovation Centre at IIT Delhi.
- **Coordinator** at Sportech '17: Sports fest at IIT Delhi.

Other Interests

Endurance Running (first 5k in 2021, 10k and half marathon in 2022), Lawn Tennis, Street Jazz and Hip-Hop Dance, Graphics Designing, Poster Making, Video Editing, Poem writing.