Sensor Control & Processing Hardware, Firmware and Post Processing requirement for 9K Time Delayed Integration (TDI) Sensor

Introduction:

Space Applications Centre, Ahmedabad is involved in development of various scientific remote sensing optical camera systems. Generation of appropriate high speed timings, processing the sensor data in real time and its acquisition in the Host computer for statistical analysis is primary requirement and this requirement varies sensor to sensor. Dedicated development of hardware, firmware and processing software is required to support evaluation of DUT (Detector under the test) with respect to electro-optical parameters evaluation. To enable DUT evaluation, bias, clock, video processing, data acquisition and data processing test boards/software modules are required as part of development. Mechanical structure is also required to support these test boards and mount DUT in front of the optical stimuli. This document gives details about requirement of real-time very High Speed Sensor processing unit development of Dual array 9k TDI sensor. Document brings out scope of work, requirements from vendors, electro-optical performance required to be measured for sensor evaluation, delivery schedule, deliverables and responsibilities.

Vendors are requested to submit their technical and commercial offers separately. Commercial bid without price information shall be attached along with the Technical offer.

Proposals are invited from vendors having experience in Real-time High Speed TDI Characterization hardware (H/W) development, software (S/W) development, mechanical design & fabrication of high speed very low read noise sensor operation.

This document gives details of the development distributed in the following sections:
Section-1: Real-time TDI Sensor Processing Hardware interface with TDI
Section-2: Detector Bias requirement
Section-3: TDI sensor timings and Data interface details
Section-4: Scope of Work
Section-5: Assembly, Integration, Testing and DUT characterization
Section-6: Vendor selection criteria
Section-7: Acceptance Criteria for Deliverables
Section-8: Performance Requirement / Specifications for processing unit
Section-9: IP Clause
Section-9: Deliverables
Section-10: Project execution Schedule and Payment Milestone
Section-11: Warranty

Section-1: Real-time TDI Sensor Processing Hardware interface with TDI

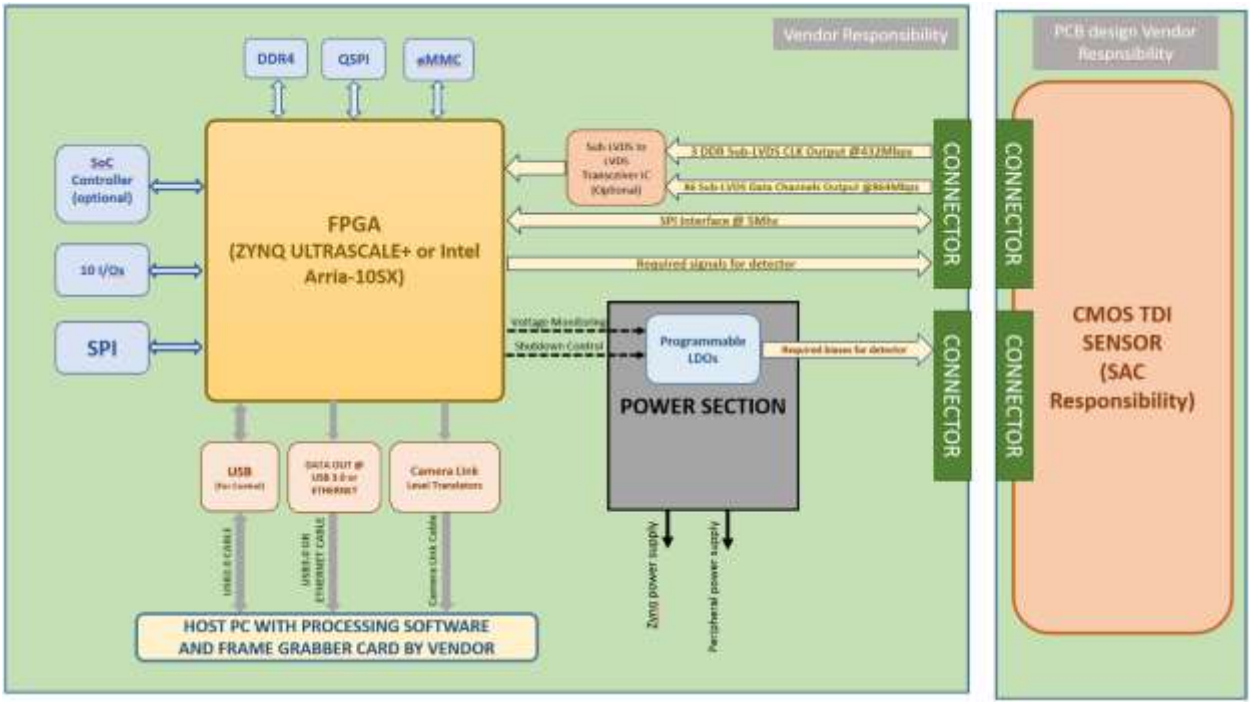


Figure-1(A): Real-time High Speed Sensor Characterization Test Setup Block diagram

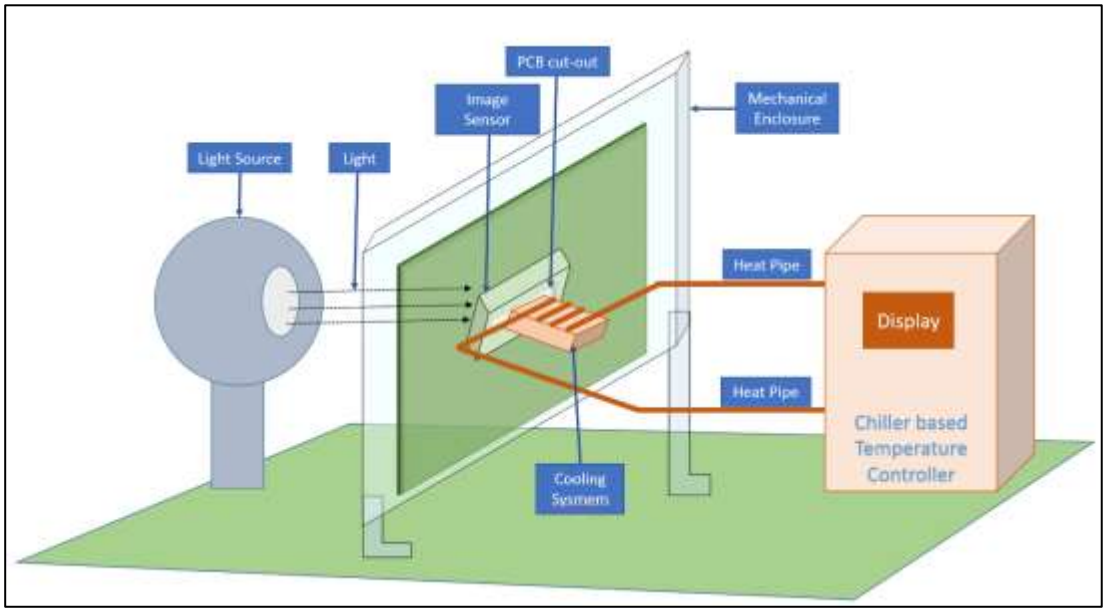


Figure-1B: Detector Thermal control system Block diagram

Figure-1(A) shows detailed block schematic for the required development and Figure-1(B) shows detector thermal system block diagram.. As shown in the Figure-1(A), SAC has procured 9000 element dual array

very high speed TDI sensor. Test setup required for this development is to generate required biases and electrical stimuli to sensor, capture the high speed video data, process captured data and transmit to the HOST PC through USB3.0 / Ethernet1G or more interface. Detail explanation of each of these blocks in the block diagram mentioned as below:

1. **9k Dual array TDI (SAC Procured & SAC responsibility):** SAC has procured 9000 element very high speed, TDI sensor (GLT5009) with dual array. This sensor has capability to operate up to 600 kHz line rate in 10-bit mode. Sensor requires multiple DC low noise biases for its operation, reference input clock in the range of 35MHz to 70MHz, 86 Sub-LVDS pixel outputs + 3DDR CLK output ports, video data rate of upto75Gbps and SPI interface to program the internal registers of the sensor. Figure-2 shows typical block diagram of the sensor.

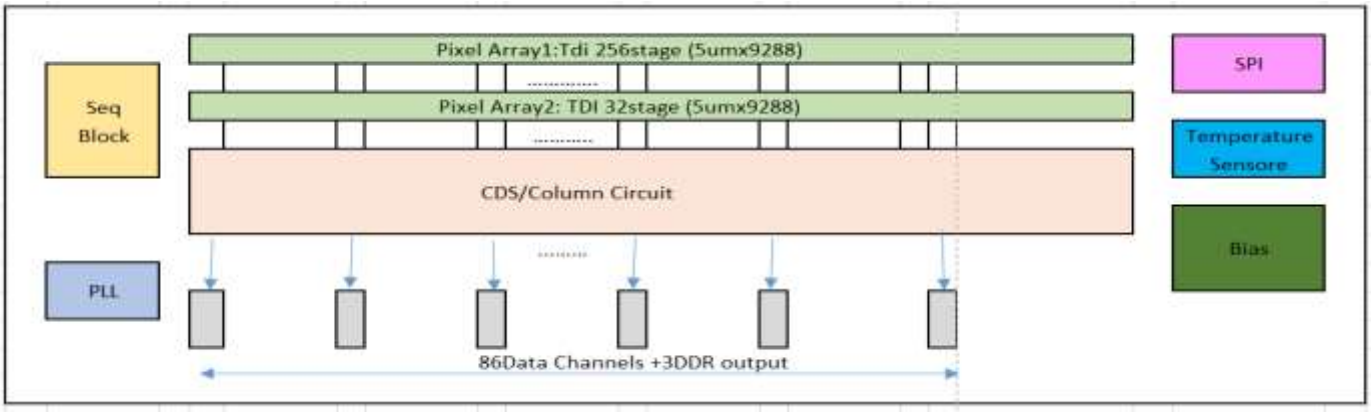


Figure-2: Typical block diagram of the sensor

2. **Programmable Bias Section (Vendor development):** Developed test setup by the vendor shall have multiple Low Dropout regulators (LDOs) required for biasing of TDI sensor. Approximately Seventeen programmable LDOs are required for biasing of detector. Details of required range with typical bias values are mentioned in the next section. Required bias on each of these bias lines shall be user programmable and same shall be monitored through SoC controller for controlling purpose.
3. **TDI Processing Hardware:** Processing hardware shall have to perform (i) Generate the required timings and control signals for detector (ii) Power ON/OFF sequence for detector biases and clocks (iii) acquisition of dual array data with total data rate of 75Gbps (iv) real-time processing of sensor data and store in the Hardware memory with pixel data rate of 75Gbps (v) Two data acquisition interfaces are required to receive the stored sensor data from the memory. One of the Data acquisition interface will be based on either USB3.0 or Ethernet1G or more, which will be captured the stored data at very high speed as per industry standard specifications of USB3.0 or Ethernet1G or more. The second interface would be based on Camera Link standard interface **with Medium Configuration**. This interface is required to measure the sensor motion MTF.

   Proposed Processing Hardware shall have Zynq Ultrascale+/Intel Arria-10SX for required development. This FPGA shall provide SPI interface between FPGA and Sensor for programming various internal registers of the sensor. FPGA module will receive sensor data at the rate of 75Gbps, format and store in the high speed DDR memory (having capacity of more than 128 frames). Stored data will be transferred to the Host PC through USB3.0 or Ethernet1G or more interface and / or to camera link interface. Memory requirement in the FPGA module will be 4GB or more and its speed

shall compatible to receive the sensor data at 75Gbps. Vendor shall develop required Verilog/VHDL codes meeting these requirements and same shall be submitted as part of deliverables. It is to be noted that sensor has two arrays with independent TDI stage selection provision. Any Intellectual Property block (IP Block) used by vendor for the development also to be provided to SAC as part of delivery.

Processing Hardware shall also have SoC Processor (Optional). SoC processor receives user required configuration details of sensor from Host PC through USB interface, program the required bias of programmable LDOs and also monitor all detector biases in real-time. SoC will shut down all the biases in case any of the bias is deviated from its typical programmable range. There will be around ten I/O interface pins will be used as data transmission / reception bridge between SoC and FPGA. These pins can be used as SPI/I2C/parallel data transfer mechanism. Vendor shall develop required SoC firmware codes meeting these requirement and same shall be submitted as part of deliverables.

4. **Host PC with processing S/w (Vendor Development):** Host PC will be used to capture the sensor data from processing unit through USB3.0 / Ethernet1G or more and through Frame Grabber. Vendor shall develop GUI based software application in the host PC for necessary commands to be given to the sensor, captures the sensor data and able to do all the electro-optical analysis of captured data set (in dark as well as in illumination conditions). Application software developed either in labview/.net is preferred. Application software will also save the acquired data, analyzed statistical results and result summary in user defined location.
5. **Detector Board (Vendor Development):** Vendor shall develop detector board as shown in the block diagram. SAC procured detector will be soldered in this board for detailed electrical and electro-optical evaluation of the sensor.

Section-2: Detector Bias Requirements

Table-1 shows requirement of biases on various lines of detector along with its minimum and maximum voltage ranges for required programmability.

Table-1: Required biases for detector

Voltage Name	Minimum (V)	Nominal (V)	Maximum (V)	Avg. power consumption (mW) 12-bit mode	Avg. power consumption (mW) 10-bit mode	Supply	Remark
VDD5A	4.95	5	5.05	2028	3856	Analog Supply	Analog
VDD18PLL	1.75	1.8	1.85	<10	<10	Analog Supply	
VDD18AD	1.8	1.85	1.9	923	995	Digital Supply	Digital
ADD18D	1.75	1.8	1.85	1357	1627	Digital Supply	
VDDSF	5.25	5.3	5.35	620	678	Current source	Pixel

VABGN	5.45	5.5	5.55	<10	<10	Current source & sink	
VABD	3.45	3.5	3.55	<10	<10	Current source & sink	
VOG	0.95	1	1.05	<10	<10	Current source & sink	
VRD	4.45	4.5	4.55	<10	<10	Current source & sink	
VRSTH	4.95	5	5.05	<10	<10	Current source & sink	
SWH	4.95	5	5.05	74	167	Current source	
SWL	-1.55	-1.5	-1.45	22	34	Current sink	
VBGH	4.45	4.5	4.55	206	224	Current source	
VAGH1	2.55	2.6	2.65	180	277	Current source	
VAGL1	-1.55	-1.5	-1.45	85	145	Current sink	
VAGH2	2.55	2.6	2.65	40	46	Current source	
VAGL2	-1.55	-1.5	-1.45	18	19	Current sink	

As mentioned in Table-1, total around 17 biases are required to be generated through programmable LDOs. Programing range for each of the bias lines along with programming steps are also mentioned in the table.

Section-3: TDI sensor timings and Data interface details

Sensor has one CMOS reference clock as an input and around five 1.8V CMOS input control signals required for sensor operation. Sensor has also SPI interface for programing internal registers of the sensor. Figure-3 shows RESET sequence of the detector which is required to be generated through processing module.

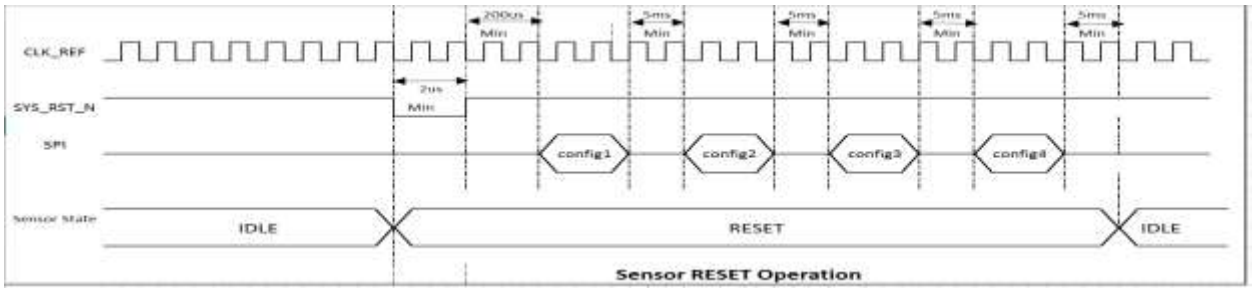


Figure-3: Sensor RESET Operation

There will be total 452 bytes of registers are available for the programming the TDI detector. Based on the required operating configuration of the sensor, required registers to be programmed after the POWER ON sequence. These registers are programmed through 4-Wire SPI interface. Timing relations for SPI Read and Write operation are shown in figure-4 & 5 respectively.

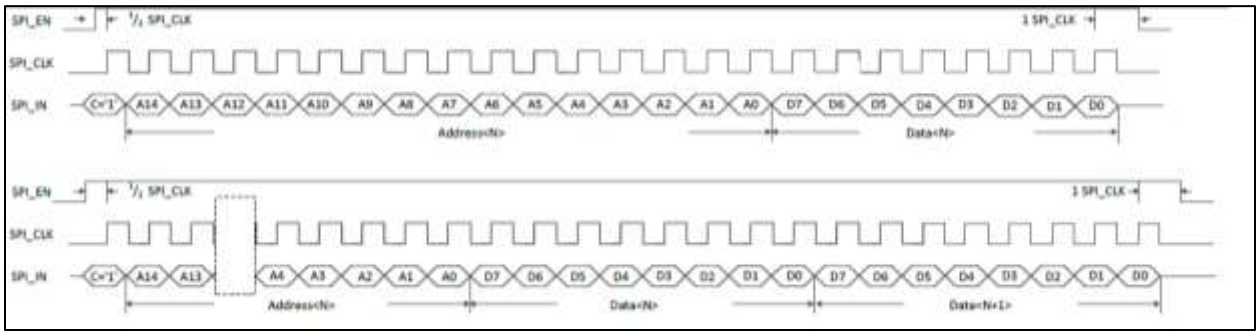


Figure-4: SPI Write Operation

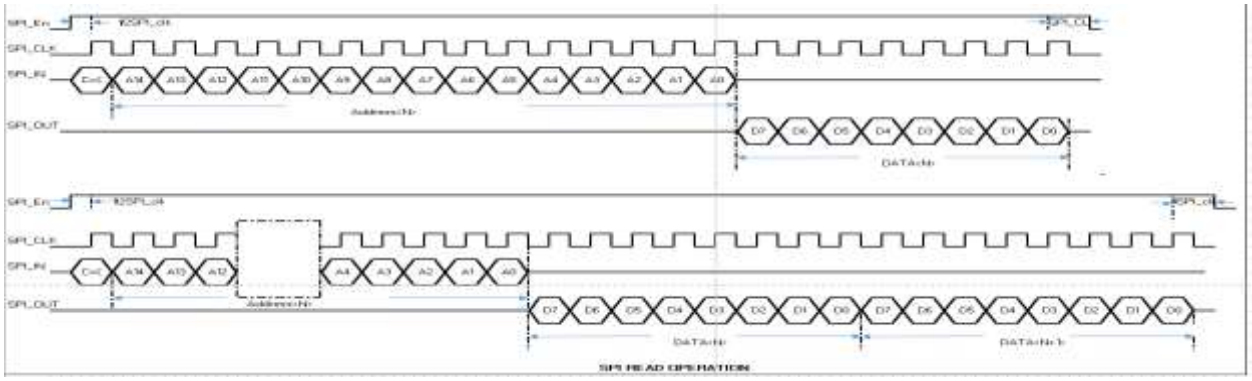


Figure-5: SPI Read Operation

Sensor has 86-Sub LVDS lines and 03 DDR clock-out channels. Reading out the image data occurs in blocks as indicated in Figure-6. The green line is stitching line, and the M area between two stitching lines is the stitching cell. TDI sensor contains 3 stitching cells. There is a data channel in left, a data channel in right and 28 data channels in each stitching cell. Note that the leftmost and rightmost channels will send out data which contains both OB and dummy pixels data. The rightmost column is defined as the first column and the leftmost column is defined as the last column for the whole sensor.

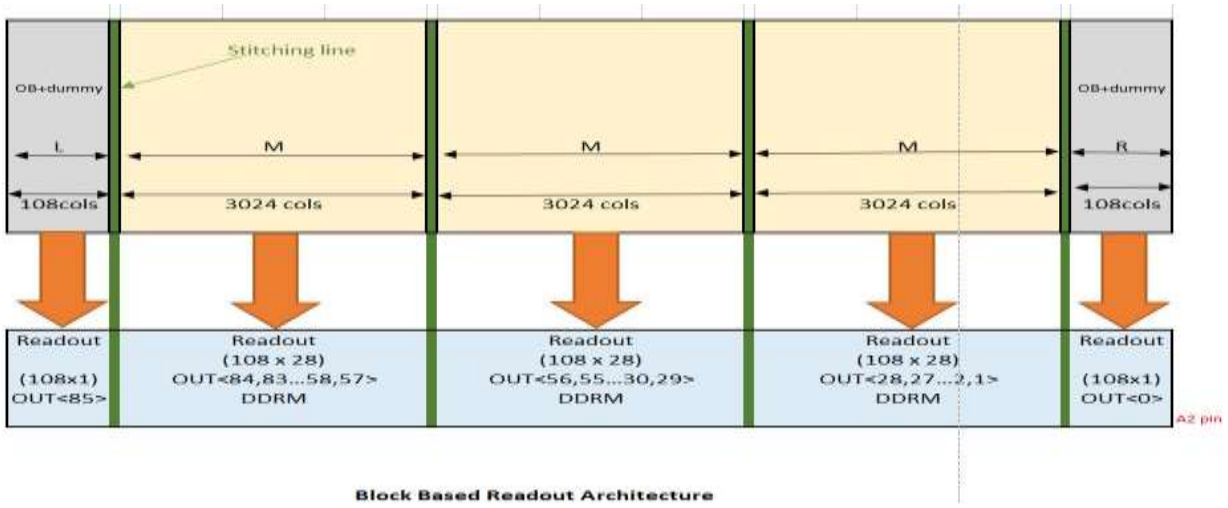
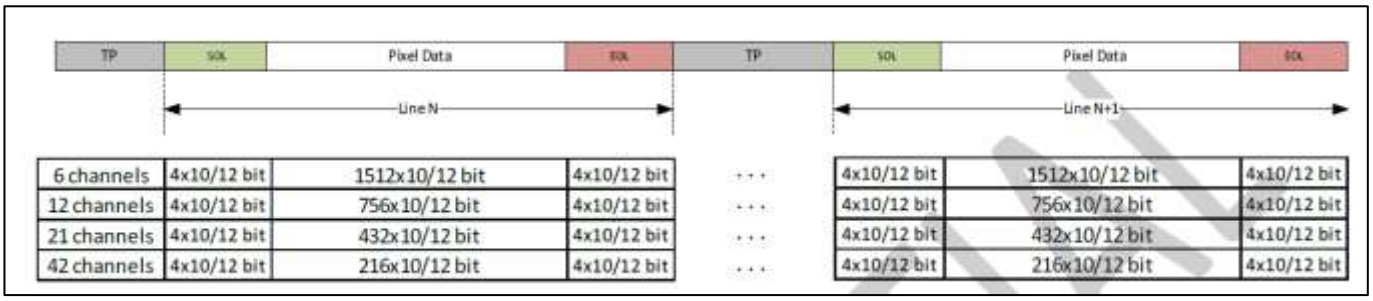


Figure-6: Block based readout architecture

The sensor supports several channel multiplexing modes. In these modes, the image data is sent out over a limited number of output channels, which are 86, 44, 23, 14 and 8. The sensor supported maximal number of readout channels are 86 in default.

Processing hardware shall have provision to capture the data in channel multiplexing mode also with multiplexing setting of 86, 44, 23, 14 and 8.

Line format for readout: Sensor supports 10-bit and 12-bit ADC output. Figure-6 graphically represents the line data format in the stitch region. A single line period outputs all the column pixel data. The data of multiple output channels are shows in the table in Figure-7.



6 channels	4x10/12 bit	1512x10/12 bit	4x10/12 bit	. . .	4x10/12 bit	1512x10/12 bit	4x10/12 bit
12 channels	4x10/12 bit	756x10/12 bit	4x10/12 bit	. . .	4x10/12 bit	756x10/12 bit	4x10/12 bit
21 channels	4x10/12 bit	432x10/12 bit	4x10/12 bit	. . .	4x10/12 bit	432x10/12 bit	4x10/12 bit
42 channels	4x10/12 bit	216x10/12 bit	4x10/12 bit	. . .	4x10/12 bit	216x10/12 bit	4x10/12 bit

Figure-7: Line format

- If no image readout is ongoing, the Training Pattern (TP) is sent out.
- Image data is always enclosed between ‘Start’ and ‘End’ synchronization (SYNC) codes. Each of such SYNC code consists of 4 words. These codes can by design never occur in an image data stream, as in the image data stream the code 000h will not be present.
- The start of the first column of a line is indicated by a ‘Start Of Line’ (SOL) SYNC code.
- The end of the last column of a line is indicated by an ‘End Of Line’ (EOL) SYNC code.
- In order to distinguish the pixel data output from the Pixel Array1 or the Pixel Array2, two sets of sync codes are defined.

Further details about the SYNC Codes for Pixel Array-1 and Pixel Array-2 shall be given to the vendor at the time of contract finalization.

Power ON-OFF Sequence:

The power supplies should follow the power on/off sequence as illustrated in Figure-8. To avoid current peaks during power on and off, minimum time delays should be guaranteed. After power on, SPI configuration should include five phases as illustrated in Figure-8 which are named SPI config1, SPI config2, SPI config3, SPI config4, SPI config5 respectively. Configuration in each phase should be:

- SPI config1: Write D<382>-Bit<7:0> as c4(Hex value).
- SPI config2: Write all registers with recommended values depending on the working mode selected, except for the following bits: D<382>-Bit<0>, D<382>-Bit<7> and D<0>-Bit<0>. D<382>-Bit<0>, D<382>-Bit<7> and D<0>-Bit<0> should be written as 0,1 and 0, respectively.
- SPI config3: Write D<382>-Bit<7> as 0;
- SPI config4: Write the register in address D<382>-Bit<0> as 1.
- SPI config5: Write the register in address D<0>-Bit<0> (CLK_STABLE_EN) as 1. (CLK_STABLE_EN should be 0 in former four stages)

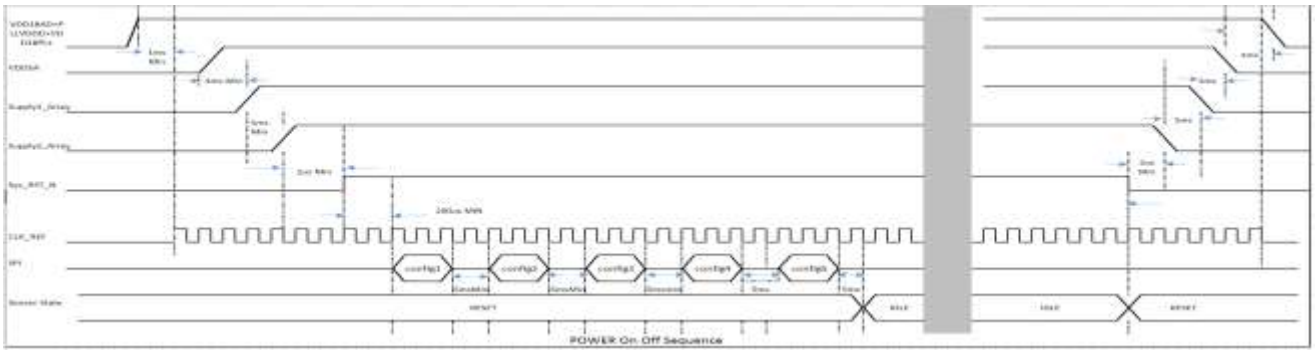


Figure-8: Power ON & Power OFF Sequence details

Trigger & Sensor Line Time:

The sensor trigger signal (TRIG), IDLE, line-time is shown in Figure-9. IDLE has 2-6 CLK_PIX uncertainty for the internal sampling delay. The sensor line-time is defined by trigger period, which is controlled by the customer.

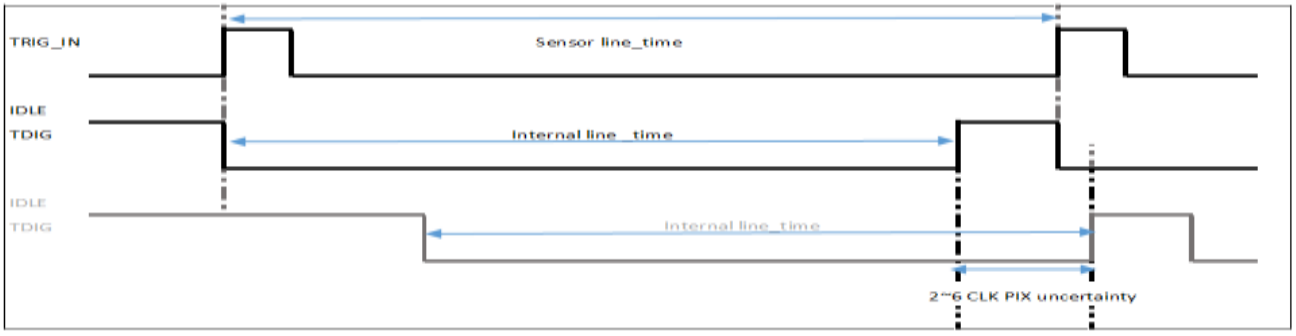


Figure-9: Trigger and Line time details

DDR & Sub-LVDS Output Relations:

Figure-10 shows timing relation between DDR clock and Sub-LVDS outputs.

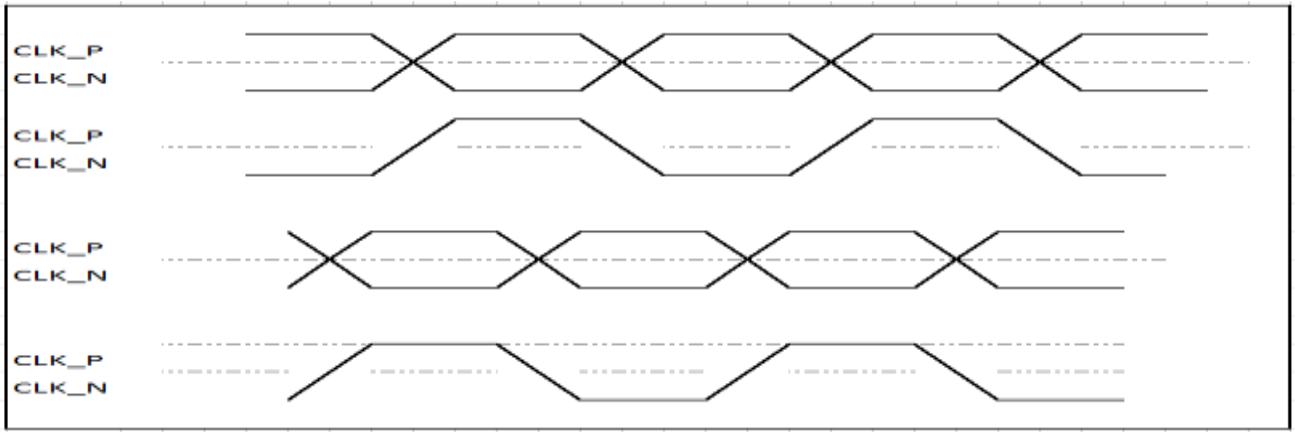


Figure-10: DDR Clock and Sub-LVDS output timing relations

Table-2 shows specifications for Sub-LVDS data interface

Symbol Name	Description	Minimum	Typical	Maximum
VOD	Differential Output Voltage	0.1V	0.15V	0.2V
VOCM	Common Mode Output Voltage	0.8V	0.9V	1.0V
VOSWING	Differential Voltage Swing	200mV	300mV	400mV

Important Note: *More details on sensor operation, required registers to be programmed, input clock and control signal timings relation, its variabilities and output data handling & formatting, detector package size etc. will be provided to the vendor at the time of contract finalization.*

Section-4: Scope of Work

Sensor control & Processing Hardware, firmware and Post processing requirement for TDI sensor requires following activities to be done by the vendor during execution of this project.

4.1 Electrical development: This includes development of different PCB cards for required hardware development as well as fabrication of wire harness for I/O connections of PCBs. These PCB cards should be operable in ambient condition and high operating temperature (up to +60°C). The PCB cards shall have mounting holes on the four corners in order to facilitate mounting of cards. Following are the major hardware to be developed by the vendor:

1) Detector Board
2) Processing Hardware consists:
   (a) Bias generation section / board
   (b) FPGA based Processing section / board

Vendor shall make schematic Entry of Design, PCB layout, component procurement, PCB fabrication, component mounting and soldering, PCB testing and firmware development and wire harness procurement and preparation. All these activities shall be done in close consultation and approvals from SAC engineers.

Work Details:

a. **Schematic entry:** Vendor shall make component footprint design per SAC/ISRO guidelines and circuit schematic as per SAC design. Vendor shall take SAC designer's approval after component placement before proceeding for layout. The design of temperature control system shall be mutually decided between vendor and SAC team.
b. **PCB layout design:** Vendor shall make multilayer (Typ. 16-24 Layers) PCB layout as per designer/ ISRO guidelines using Cadstar/Altium/Cadence/Orcad. PCB shall be designed from testability point of view also. Vendor shall carryout necessary simulations for signal integrity, power integrity and ground bounce related issues and the results shall be reviewed by SAC. Vendor to provide final schematic and layout files to SAC.
c. **Bare PCB fabrication:** Vendor shall be responsible for bare PCB fabrication. SAC shall approve Gerber data prior to fabrication of PCBs.
d. **Components procurement:** Vendor shall procure the components including FPGAs, SoC controller etc. meeting the required specifications. All the electronic components should be at least industrial grade. Vendor shall take approval from SAC engineer during finalization of components. Connectors used for connecting detector board with processing board shall meet the power and speed requirement laid down in this RFP along with appropriate mounting arrangement.
e. **PCB wiring:** Soldering and wiring of fabricated PCBs. Vendor shall perform QC check of populated PCB.
f. **Firmware Development:** Development of code in Zynq UltraScale+ / Intel Arria-10SX based H/w to facilitate programming shall be carried out by vendor. The programmability requirement shall be given by SAC.

   Following are the list of activities to be carried out on Zynq/Arria Platform:

   i. Top level FW design
   ii. Considering USB / Ethernet1G or more to be primary interconnect path to transfer frames from Zynq/Arria to Windows Host PC, Enabling USB3.0/ Ethernet1G or more FPGA Platform as well as on the Host PC side.
   iii. custom RTL, and firmware for related peripherals
   iv. Application on Zynq/Arria platform to configure the TDI sensor and its trigger.
   v. Application to capture the frames and store it in the onboard RAM and transmit the same to the Host PC as and when required
   vi. Unit & integration level testing
   vii. Bug fixing

g. **Electrical testing:** Vendor shall perform detailed electrical testing on all the developed electrical hardware in presence of SAC team before delivering the hardware. SAC team will review the performance as mentioned in acceptance criteria section and shall give clearance for the dispatch.

h. **Host PC Application:** Vendor to develop PC based Data acquisition and post processing software to evaluate sensor electro-optical parameters and stores the data in hard drive along with automatic report generation. Host PC has to acquire data through Ethernet 1G or more or USB-3.0 port from the DDR memory of processing hardware developed by vendor. Vendor shall evaluate dark offset, dark noise, conversion gain, dynamic range, full well capacity etc. from the acquired dataset.

   - Preliminary design of the GUI pages and backend logic
   - Use case implementation to talk to CMOS TDI sensor.
   - Developing Interface logic between Zynq/Arria and Host PC

- Use case implementation to talk to Zynq/Arria Platform to get frames when triggered.
- Encoding Raw Sensor Data to human readable format like .jpg & .MP4 etc.,
- Integrating free-downloadable video or Image player in GUI to show recorded frames
- Host based GUI Application development
- Overall Software integration
- Unit Testing

4.2 Temperature Control Mechanism development:

Vendor shall design and develop close loop temperature control system for maintaining the DUT temperature under the operating environmental condition. Image sensor shall be evaluated for its performance throughout set temperature range of +10°C to +35°C in step of 2°C minimum. At a given set temperature, the sensor shall be maintained with a band of ±0.5°C during operation and testing phase of typically two hours. Vendor shall provide close loop temperature control system to cater DUT dissipation of 3W (typical) during operation in ambient and vacuum condition.

Work details to be carried out by vendor are provided below:

- Design the control system and meet overall requirements of temperature controlling based on configuration design provided by SAC.
- Vendor shall procure components e.g. chiller/TEC, Cu finger, interface plate, and heat pipe required as per design of temperature control system.
- Design, fabrication, wiring and testing of PCBs required in temperature control system.
- Integrate the sub systems.
- Test and validation of thermal control system with load simulator and submission of detailed test report to SAC.
- Delivery of complete thermal control system at SAC after review of test results by SAC team.
- Validation of temperature control with actual load.

Accessories or materials like thermal glue or thermal grease shall not be used in temperature control mechanism.

4.3 Mechanical Hardware Development:

Manufacturer shall design and fabricate mechanical structures and packages (black anodized) to hold all the PCB cards and other components like lens, optical test targets. Lens and optical test target holders should have provision for height and position adjustability. Light throughput falls on the DUT from front side, therefore whole unit shall be mounted in vertical configuration. The mechanical structure shall be designed such that it does not produce continuous vibration in the PCBs and also support the thermal control mechanism.

4.4 Host PC Specifications:

Table-2 shows specification details for HOST PC requirement

Sr.No	Parameter	Requirement
1	Processor	Intel core i7, 4GHz and above
2	No. of Cores	8 core and above
3	Installed RAM	16 GB DDR5 and above

4	HD drive	2TB HDD and 512GB SSD or more
5	Operating System	Licensed version of Window 10 or above
6	Graphics card	2GB or more
7	Accessories	LED Monitor (27 inch or more), Keyboard, Mouse
8	USB ports	5 or more (with at least 02 USB-3.0 ports)
9	Ethernet Ports	02 (1G or higher)
10	Ethernet Interface	Required
11	Microsoft office	Licensed version of MS office 2016 or above pre-installed
12	Display port	Compatible with Monitor
13	Power Supply	Indian Standard
14	PCIe Interface	Required

Section-5: Assembly, Integration, Testing and DUT Characterization

Vendor has to carry out assembly and integration of developed electronics hardware along with mechanical fixtures and harness at SAC with SAC provided DUT. Vendor shall demonstrate performance of integrated system and results shall be verified as per acceptance criteria. After assembly and integration, integrated unit shall undergo burn-in as per SAC guidelines. After successful burn-in of test bench, vendor has to perform detailed testing and characterization of DUT at SAC. Estimated overall time duration for assembly, integration and detailed electro-optical testing of image sensors utilizing with delivered hardware is 18 Months after delivery of hardware to the SAC. Vendor shall provide trained Man Power in SAC during the warranty period to carry out the Software & hardware integration of the Drive Electronics along with other test Hardware present in the SAC Labs.

It is mandatory that same set of people should be involved in testing of cards, firmware, software development, assembly, integration and testing and DUT characterization. Vendor shall carry out different types of E-O Measurements on DUT in ambient condition and thermo-vacuum condition at SAC during the testing phase. The measurements shall be categorized in three different categories:

1. Light Transfer Characteristics (LTC) measurement:
In this measurement, DUT response shall be measured at twenty different aperture settings of uniform light source from dark to saturation. This measurement covers processing of following EO parameters:

- Photon transfer curve (PTC)
- Dark Counts
- Dark noise
- Signal to noise ratio
- Saturation count
- Response non-uniformity
- Dynamic Range
- Non Linearity

2. MTF measurement:
In this measurement, DUT shall be illuminated with collimated target. Measurement shall be done by projecting BAR targets of different frequency (ηc, ηc/2 and ηc/4) on DUT. Vendor has to design and fabricate/procure these targets and deliver to SAC. Details for target design shall be given by SAC at the time of PO or during development phase.

3. Quantum Efficiency (QE) measurement:
In this measurement monochromatic light covering wavelength range from 350nm to 1050nm shall fall on DUT. DUT data shall be acquired at each wavelength and QE shall be processed as per formula/procedure defined in measurement and analysis methodology.

4. Motion MTF measurement:
In this measurement, data received from the frame grabber card will be used for measurement of motion MTF. SAC has sophisticated calibrated test bench available for measurement of this parameter where sensor charge transfer is get synchronized with dynamic movement of object under the interest.

Section 6: Vendor selection criteria

Following are the vendor selection criteria for development of High Speed Sensor Characterization Test Setup. It is mandatory for vendor to fulfil all the listed below criteria for consider its offer.

For any non-compliance in this criteria by the vendor, SAC reserves right to reject the offer on non-compliance basis.

1. Vendor shall have prior experience on development of high speed electronics which has capability to handle the real time data of 1Gbps or more per lane. Vendor shall submit sufficient technical details / proof showing carried out development in past. This requirement is mandatory and shall not be relaxed for any bidder.
2. Vendor shall have in-house test facility/capabilities for electrical and electro-optical evaluation of image sensors:
    a. Cleanroom of class-10000 or less
    b. Tunable DC Power supply units generating DC voltages in the range of 0 to 10V with at least 1A current capacity
    c. CRO/DSO with probes having minimum 500MHz bandwidth
    d. Zynq UltraScale+ / Intel Arria-10SX based evaluation kits/ equivalent developed H/w (for evaluation of firmware)
    e. Vendor shall have experience in high speed sensor drive and processing logic design in Zynq UltraScale+ MPSoC Xilinx / Intel Arria-10SX FPGA. Vendor shall also have prior experience to provide either USB3.0 or Ethernet1G or more interface for data acquisition meeting data rate of 1.0Gbps or more per lane. Vendor shall provide sufficient details on this along with submitted offer.

    Vendor shall provide sufficient details of this facilities along with submitted offer.
3. Vendor shall have prior experience of real-time camera data streaming and camera data processing algorithms like Histogram, bad pixel identification and correction, Non-uniformity correction. Vendor shall provide sufficient details of these algorithms along with submitted offer.
4. Vendor shall have prior experience in embedded application development, Board support package (BSP) and driver development, operating system porting and optimization of middleware libraries. Vendor shall provide sufficient details on this along with submitted offer.
5. Vendor shall submit technical document detailing their proposed test bench configuration (arrangement of cards), thermal control configuration and component details for interface connectors and thermal control scheme. In the absence of such details the offer shall be rejected.

6. Vendor has to provide point-by-point compliance of RFP requirement in their technical proposal (in all sections and/or sub sections) and shall submit sufficient information supporting the compliance to evaluate proposal.
7. Vendor shall have licensed version of PCB development tool, software development application and FPGA/Controller programming software. Details of available software will be provided by vendor.
8. Vendor shall provision necessary human and technical resources at SAC during assembly, integration and testing activities of delivered hardware and firmware along with SAC procured detector.
9. This entire development is a Turnkey project and vendor shall deliver all the items as mentioned in the deliverable section along with required development. Any offer having partial delivery / development will be rejected straightaway.
10. Vendor shall provide consolidated development cost including all NRE as single line item.

Section 7: Acceptance Criteria for Deliverables

This section details about acceptance level requirements to be fulfilled by vendor for deliverables at individual sub system level and full integrated system level. Vendor shall validate performance with respect to points listed for each level.

7.1 Hardware acceptance criteria

7.1.1 Detector Board

- Electrical test at Lab conditions initially and after powered burn-in at +25°C for 168 hrs.
- Deviation between initial and after powered burn-in measurement values (biases and current on each detector lines) shall not more than ±10%.

7.1.2 Programmable Bias generating Section/Board:

- Electrical test for generated biases (with desired programmed value in the specified range mentioned in table-1) values meeting requirements of Table-1 at lab conditions initially and after powered burn-in at +25°C /168 hrs.
- Deviation between initial and after powered burn-in measurement values shall not more than ±10%.

7.1.3 FPGA based Processing Section/Board:

- Timing logic generation meeting requirements and jitter tolerance of ≤10% at lab conditions initially and after powered burn-in at +25°C /168 hrs.
- Deviation between initial and after powered burn-in measurement values shall not more than ±10%.

7.2 Pre-dispatch board interface test for board build-up firmware

- Vendor shall demonstrate power on DUT bias and timing relations, clock relations in FPGA and on-line bias monitor logic developed in SoC/FPGA at vendor premises (pre-dispatch).
- Verification of clock relation programmability.
- Verification of USB3.0/Ethernet1G or more interface by sending known pattern from processing board to host PC.
- Verification of sensor data acquisition at 70Gbps and store inside the DDR memory of processing board.
- Copy of editable firmware Code shall be submitted to SAC
- Vendor shall provide pre-dispatch test report on developed firmware

7.3 Board build-up and interface test-setup software

- Validation of DAQ module which acquires data at USB3.0/Ethernet1G or more interface
- Validation of DAQ module which acquires data with Camera link Medium interface
- Validation of processing module using data simulator
- Demonstration of Electro-optical parameter evaluation statistics with known input datasets
- Copy of editable Software Code shall be submitted to SAC

Section-8: Performance Requirement / Specifications for Processing Unit

This section gives required requirement / specifications to be met by vendor for developed processing unit. Table-3 gives broad requirement details.

Table-3: Performance requirement / specification of processing unit

Parameter	**Requirement**
Clock input to detector board	Typ. 36MHz Range: 20MHz to 80MHz
DDR input clocks to Processing Unit	03Nos. Sub LVDS
Sensor data input to Processing Unit	86 Nos. Sub LVDS Max. Data rate: 76Gbps per frame
Control signals to detector board	06 Nos. LVCMOS interface
Control signals to Processing Unit	05 Nos. LVCMOS interface
Memory requirement	At least 4GB DDR-3/4 with speed to store the data at 75Gbps per frame
Programmable bias section	Required (as per section-2)
Processing Section	Required (as per sections –1, 3, 4)
Host Interface	USB2.0/3.0 → For command to configure detector USB3.0/Ethernet1G or more → To transmit captured processed data stored from Processing unit memory to Host PC Camera Link with Medium Interface: Required to measure motion MTF of the sensor
Real-time processing requirement	Dark data subtraction, PRNU correction, AGC, Dead pixel correction, noise correction algorithm, Edge enhancement, Median and Gaussian filter, exposure control, gray to binary conversion, Programmable TDI stage selection, Frame imaging mode of operation of sensor

Section 9: IP Clause

“The Intellectual property rights relating to the design, development, processes, technical information, documents and other fabrication details shared/ published by SAC/ISRO and received from the Service Provider/ manufacturer shall remain the exclusive property of SAC/ISRO. Service Provider or Personnel deputed/ deployed/ assigned job by the Service Provider/ manufacturer shall make no attempt to unlawfully reveal, misuse or encroach upon the intellectual or private data/ information/ Computer systems at SAC/ISRO or provide by SAC/ ISRO to which they may have access to, as part of the work carried out”.

"This is a development contract from SAC/ISRO. SAC/ISRO will be the sole proprietor for the intellectual property developed under this project and it's usage by the executing agency is subject to written permission by SAC/ISRO. All the IP should be delivered to SAC/ISRO in source form without any licensing obligation and SAC/ISRO will be free to use it for any of it's ongoing and future project without obligation to any third party."

Section 10: Deliverables

Table-4: Deliverables

Sr No.	Deliverable	Quantity
01	Detector Board	02
02	Real-time High Speed Sensor characterization H/w having following: I. Low noise programmable detector bias section / Hardware II. FPGA and SoC based high speed Module as mentioned in the requirement	02
03	Host PC unit with pre-installed IDE/toolchain of selected FPGA	01
04	VHDL/Verilog code source files along with used IPs used for FPGA programming	One Set
05	SoC firmware source code used for SoC controller	One Set
06	Application Software along with Source code for Host PC data acquisition, statistical analysis of electro-optical parameter etc.	One Set
07	Mechanical hardware	02 Set
08	Compatible Interface harnesses, consumable items	05 set
09	PCIe based Frame Grabber card (Medium interface)	One Set

Note-1: Vendor shall provide consolidated development cost including all NRE as single line item.

Section 11: Project execution Schedule and Payment Milestone

Table-5: Project Execution Schedule

Sr No.	Activity	Timeline	Vendor Responsibility	SAC Responsibility
1	Kick off meeting / Detailed Design Review (DDR)	T0 (within 02 weeks from the date of PO placement)	Design Document	-
2	Schematic design of different PCB H/w	T2: T0 + 07 Weeks	Block level architecture design, schematic entry	Schematic review and clearance for Layout design
3	Bare PCB Layout design	T3: T2 +08 Weeks	Multi-layer PCB layout, signal integrity simulations	Layout review, SI performance review and clearance for PCB fabrication
4	Hardware development	T4: T3 + 06 Weeks	Bare PCB fabrication, component soldering, electrical testing	Electrical testing result review and clearance for next step
5	FPGA & SoC firmware development, PC	T5: T4+08 Weeks	Vendor shall start design of Firmware	FPGA and SoC firmware

	based processing S/w development		and software from T0 itself	simulation review and PC based software development review. Clearance for next step
6	Development of mechanical and thermal hardware	T5	Vendor shall carryout this development from T0 itself	-
7	Delivery of developed Hardware	T6 = T5 + 04 Weeks	Electrical and electro-optical testing of developed hardware (electronics, mechanical, thermal) at vendor premise before delivery of H/w	Clearance for hardware delivery
8	Final assembly, testing, integration and Electro-Optical evaluation at SAC	T7 = T6 + 78 Weeks	Hardware interface with SAC provided detector, Firmware and software development for SAC provided detector operation and EO performance evaluation, testing and analysis	Clearance for all contract activities completed
Total time: 111 weeks				

Table-6: Payment Milestone

Milestone	**% amount to be released by SAC**
Detailed design review	10*
Delivery of all the hardware, board build-up interface Firmware and Software	60
Completion of Final assembly, testing, integration and Electro-Optical evaluation at SAC with SAC provided detector	30

* Vendor shall submit equal amount of Bank Guarantee (BG) against the released amount. This BG shall valid till execution of the order for its entire scope.

Section 12: Warranty

Vendor shall provide warranty on all the deliverables for at least 2 years from the date of delivery. During warranty period, vendor shall provide support for free of cost repair of hardware deliverables and bug fixing of software deliverables.