A High Efficiency Flyback Converter With New Active Clamp Technique

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***Abstract*—This paper proposes a flyback converter with a new noncomplementary active clamp control method. With the proposed control method, the energy in the leakage inductance can be fully recycled. The soft switching can be achieved for the main switch and the absorbed leakage energy is transferred to the output and input side. Compared to the conventional active clamp technique, the proposed methods can achieve high efficiency both for heavy-load and light-load condition, and the efficiency is almost not affected by the leakage inductance. The detailed operation principle and design considerations are presented. Performance of the proposed circuit is validated by the experimental results from a 16 V/4 A prototype.**

***Index Terms*—Active clamp, flyback, high efficiency, noncomplementary control.**

I. Introduction

WITH MORE and more emphasis on the environment protection and energy saving, the efficiency and standby power loss of the power supply are much concerned. For external power supplies, such as adaptors, the average efficiency instead of the full-load efficiency is more important to save the energy. Therefore, both the light-load efficiency and full-load efficiency need to be carefully considered, which creates new challenge for the power supply design.

Flyback converters are widely adopted for low-power offline application due to its simplicity and low cost. Usually, an RCD clamp circuit is necessary to dissipate the leakage energy during the switch is OFF. And a well-coupled transformer with minimized leakage inductance is critical to achieve the high efficiency and to minimize the voltage spikes across the switch. However, a labor-intensive manufacturing process is required to produce these well-coupled transformers as well as passing the safety regulation. How to further improve the efficiency of a flyback converter still challenges the power supply designers.

The first way to improve the efficiency is reducing the leakage inductance energy loss. The conventional RCD clamp circuit absorbed the leakage energy and dissipated it in the snubber resistor. If the leakage inductance is large, the dissipated energy is much larger than the energy stored in the leakage inductance due to part of the magnetizing energy fed to the snubber circuit during the commutation time, which deteriorate the efficiency. The lossless snubber for single-end converter was proposed to recycle the leakage energy, but the snubber parameters makes the circulating energy relative large during normal operation, which limited the efficiency improvement [1]. The active clamp flyback converter can recycle the energy in the leakage inductor and achieve soft switching for both primary and auxiliary switch [2]–[8]. Although it has good performance in efficiency at full-load condition, it is sensitive to parameters variations. The variation of leakage inductance and snubber capacitor affects the conduction angle of the secondary-side rectifier, which lowers the efficiency. And the two active switches also increase the cost. Furthermore, the conventional complementary gate signal and constant frequency (CF) control method result in poor efficiency at light-load condition, which also leads to lower average efficiency.

Other topologies with two active switches in half-bridge structure can absorb the leakage energy with pulsewidth modulation control or resonant control, such as asymmetrical half-bridge (AHB), asymmetrical flyback, or LLC converter [9]–[14], [17], [18], they can achieve soft switching for main switches and high efficiency, but most of them are not suitable for wide input range application as usually required for universal input condition without front-end power factor corrected (PFC) converter.

Also, many control schemes are proposed to improve the efficiency of the conventional flyback converter. They mainly focus on how to reduce the switching loss. The efficiency of conventional CF control usually is low due to the high-switching loss caused by high drain to source voltage across the switch. Many variable frequency (VF) control schemes are proposed in the recent years to improve the performance compared to the conventional CF control [15], [16]. The quasi-resonant (QR) control method operates the converter at critical continuous mode (CRM), and turns ON the switch at the minimal point of switch voltage to reduce the switching loss, such as NCP1207 from ON Semiconductor. In low-input voltage condition, zero voltage switching (ZVS) for primary-side switch can be achieved. And switching loss still exists in high-input condition. However, the switching frequency increases at light-load and high-input condition, which leads to a low-light-load efficiency. The maximum switching frequency need to be clamped to reduce the electromagnetic interference (EMI) noise and burst mode operation is necessary to improve the light-load efficiency [15]. In QR control, the ZVS of primary-side switch can be achieved if the secondary synchronous rectifier is adopted. The reversed

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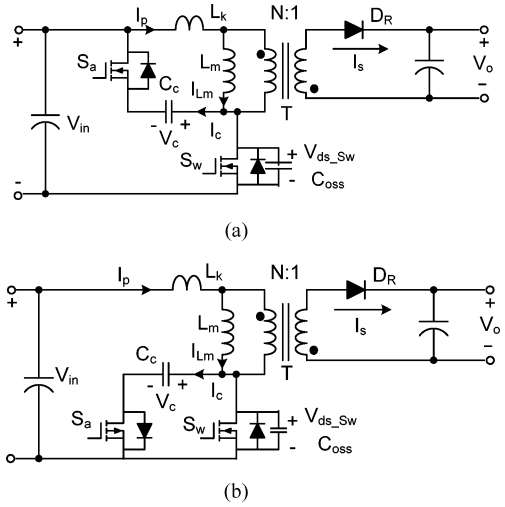


Fig. 1. Topology of the active clamp flyback converter. (a) N-type clamp circuit. (b) P-type clamp circuit.

magnetizing current is used to achieve ZVS operation, there is circulating energy from secondary to the primary side and the save switching loss is offset by the increased conduction loss [16]. The OFF-time control scheme reduces the switching frequency when the load decreases by fixing the primary-side peak current, which results in a very good light-load efficiency and transformer core utilization, such as NCP1351 from ON Semiconductor. But the switching loss is larger due to valley switching was lost. To further optimize the operation performance, many mutlimode control schemes are also implemented by combining these mentioned control scheme with an optimized sequence, like QR at heavy load, CF/OFF-time control at light load and burst at very light-load condition, such as TEA1552 from NXP and UCC28600 from TI. But all these did not have much effect on the leakage energy.

This paper presents a flyback converter with a new active clamp control method to achieve soft switching and high efficiency in whole load range, which is quite attractive for low-power application with universal ac inputs, such as external adaptors. The power stage is shown in Fig. 1, which is the same as the conventional active-clamp circuit, but the control method and operation principle are different. In the proposed control method, the auxiliary switch is turned ON for a short time before the main switch is turned ON. And the recycled leakage energy is used to achieve the soft switching of the main switch, which dramatically reduce the circulating energy compared to the conventional active clamp flyback. Furthermore, the proposed control scheme can be adopted to VF control to reduce the switching loss and improve light-load efficiency.

The detailed operation principle will be illustrated in Section II. The design considerations are given in Section III. Section IV will present the detailed experimental results from a 64 W (16 V/4 A) prototype with universal ac input. A comparison of the experimental results with the other control scheme is also provided to validate the advantages of the flyback converter with proposed noncomplementary control signal.

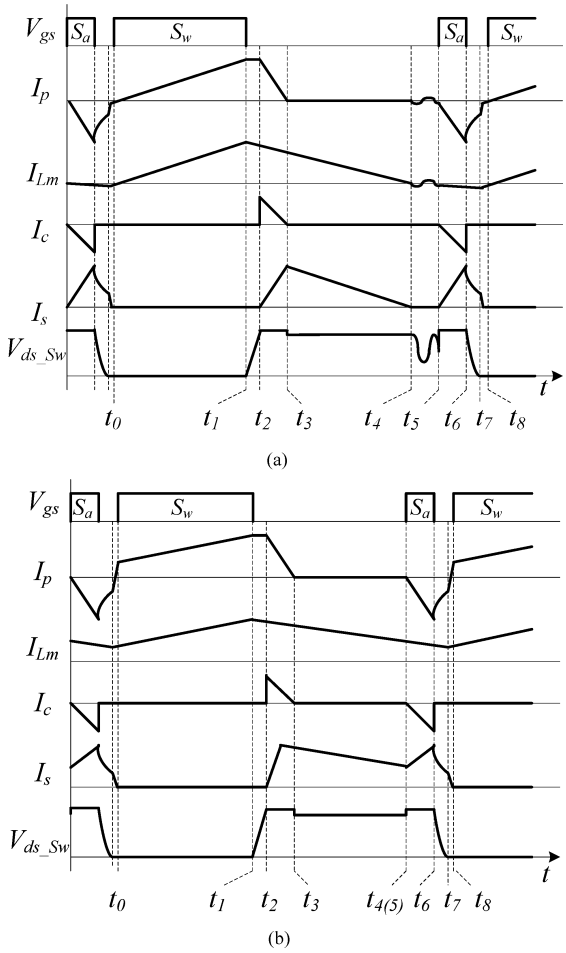


Fig. 2. Steady-state operation waveforms with proposed noncomplementary control method. (a) DCM operation. (b) CCM operation.

II. Principle of Operation

Fig. 1 shows the circuit configuration of the proposed active clamp flyback converter, which is identical for the conventional active clamp flyback. L_m is the transformer magnetizing inductance and L_k is the transformer leakage inductance. S_W is the primary main switch, and D_R is the output rectifier diode. Auxiliary switch S_a can be a NMOS or PMOS, as shown in Fig. 1. $C_{\rm oss}$ is the equivalent parasitic capacitance of S_w, S_a, and the parasitic winding capacitance of the transformer. The transformer turns ratio is N. The output voltage is V_o.

To simplify analysis of the steady-state circuit operation, the clamp voltage is assumed to be constant. The theoretical waveforms at discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation are shown in Fig. 2. The N-type in DCM operation is used as example, the steady-state waveform and equivalent circuit are shown in Figs. 2(a) and 3, respectively. Each operation mode is described next.

Mode 1 [t_0–t_1]: In this mode, primary-side switch S_w is ON and the auxiliary switch S_a is OFF. The energy is stored to the magnetizing inductor and the primary-side current I_p increases linearly, which is the same as the conventional flyback converter.

Mode 2 [t_1–t_2]: At t_1, when S_w turns OFF, $C_{\rm oss}$ is charged up by the magnetizing current. Due to relative large magnetizing

inductance, the drain–source voltage $V_{\mathrm{ds\_}S_w}$ of main switch S_w increases linearly.

This mode ends when the drain–source voltage $V_{\mathrm{ds\_}S_w}$ reaches the input voltage V_{in} plus the clamp voltage V_c, i.e., $V_{\mathrm{in}}+V_c$. Due to the large clamp capacitor, there is no parasitic ring or voltage spike, which helps to reduce the EMI noise and the voltage rating of S_w.

During this mode, the secondary-side rectifier D_R may turn ON, which depends on the clamp voltage V_c and the ratio of the leakage inductance and the magnetizing inductance, i.e., $m=L_k/L_m$. Once the clamp voltage V_c is larger than $(1+m)NV_o$, the secondary-side rectifier diode D_R turns ON firstly, and then, the leakage energy keeps to charge up the parasitic capacitor C_{oss}. If the V_c is smaller than $(1+m)NV_o$, the clamp voltage may charges up, once the V_c reaches $(1+m)NV_o$, the secondary-side rectifier D_R turns ON. Based on the aforementioned assumption, here we simply assumed that the V_c is almost equals to $(1+m)NV_o$, detailed discussion of clamp voltage V_c will be presented in the next section. Once the $V_{\mathrm{ds\_}S_w}$ reaches $V_{\mathrm{in}}+V_c$, the secondary-side rectifier D_R also turns ON.

Mode3 [t_2–t_3]: At t_2, the voltage $V_{\mathrm{ds\_}S_w}$ reaches $V_{\mathrm{in}}+V_c$, the antiparalleled diode of S_a turns ON and the secondary-side rectifier D_R also turns ON. The energy stored in the magnetizing inductor starts to deliver to the output. And the energy in the leakage inductor is absorbed by the clamp capacitor. This mode can be treated as a primary to secondary commutation period.

If the clamp capacitor is large enough and the circuit is lossless, the leakage inductor current I_p decreases linearly. Otherwise, the current may decay like a transient in a two-order circuit. The detailed expressions will be presented in the next section.

During this mode, the difference between the magnetizing current and primary current is delivered to secondary side. As soon as the current in the leakage inductor reaches zero, this mode is finished. And all the magnetizing current is transferred to the secondary side, though part of them is absorbed by the clamp capacitor during this mode.

Mode 4 [t_3–t_4]: At t_3, the current through leakage inductance is zero and the antiparalleled diode of S_a is OFF. The magnetizing energy is delivered to the load as conventional flyback converter and the magnetizing current decreases linearly.

Mode 5 [t_4–t_5]: At t_4, magnetizing current decreased to zero, and D_R turns OFF. A parasitic resonance occurs between L_m and C_{oss} as conventional flyback at DCM condition.

Mode 6 [t_5–t_6]: At t_5, auxiliary switch S_a is turned ON. The voltage across the magnetizing inductance L_m and leakage inductance L_k is clamped to V_c, and secondary winding is forward-biased, so D_R is ON. The current through L_k increases reversely. The magnetizing current I_{L_m} increases reversely too, but the magnitude may be smaller than the leakage current. These negative current is used to achieve ZVS of main switch S_w.

The absorbed leakage energy in Mode 3 is transferred to the output side and the leakage inductor again. The auxiliary switch ON time determines the circulating energy and clamp voltage. Detailed design consideration will be discussed in the next section.

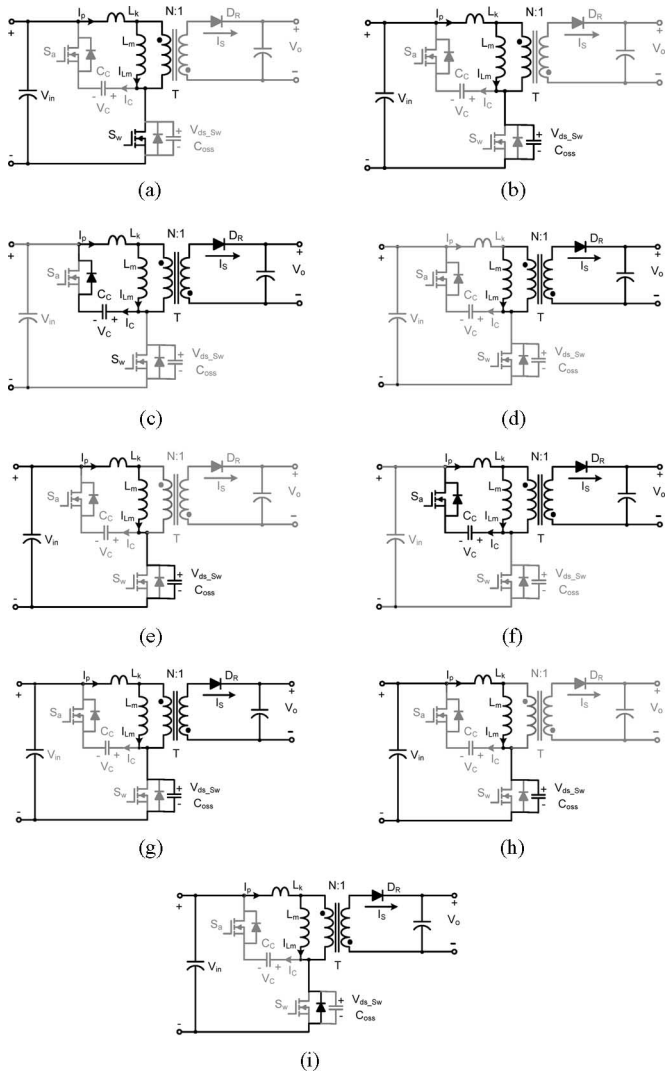


Fig. 3. Equivalent circuits in steady-state operation. (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6]. (g) Mode 7 [t_6–t_7]. (h) Mode 7B [t_6–t_7]. (i) Mode 8 [t_7–t_8].

Mode 7 [t_6–t_7]: At t_6, the auxiliary switch S_a turns OFF. The negative current I_p discharges the parasitic capacitor C_{oss}. If the leakage energy is larger than the energy in the parasitic capacitor C_{oss}, the secondary D_R keeps ON, the difference between I_p and I_{L_m} is fed to the secondary side.

Once the leakage energy is smaller than the parasitic capacitor, the magnetizing inductor also helps to realize the soft switching. As soon as the leakage inductor current I_p reaches I_{L_m}, the secondary D_R is OFF, and both the magnetizing inductor and the leakage inductor discharge C_{oss}, as shown in Fig. 3(h) (referred as Mode 7B).

Mode 8 [t_7–t_8]: At t_7, the output capacitor C_{oss} voltage decreased to zero and the antiparallel diode of main switch S_w turns ON. If the leakage inductor current I_p is still larger than I_{L_m}, the equivalent circuit is shown in Fig. 3(i). If the leakage inductor current I_p reaches I_{L_m} during Mode 7, the equivalent circuit is same as Fig. 3(h). The primary-side switch S_w should be turned ON before the primary current I_p changes the polarity.

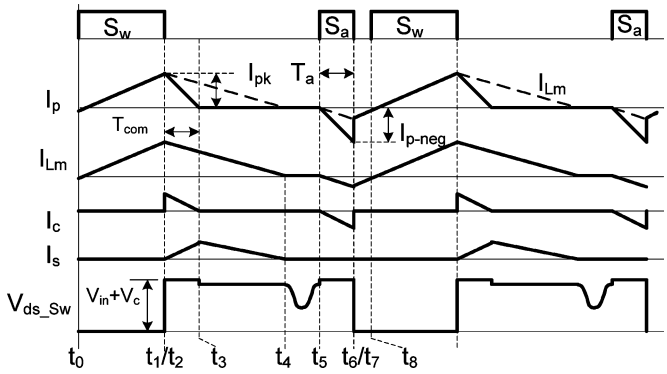


Fig. 4. Simplified steady-state operation waveforms under DCM.

For CCM condition shown in Fig. 2(b), Mode 5 does not exist anymore, and other modes are almost the same as those described earlier. Also, due to CCM operation, only the leakage energy can be used to achieve ZVS.

Based on the aforementioned description, the proposed circuit can be applied to any control scheme to recycle the leakage energy, such as CF or VF.

III. Design Considerations

Based on the steady-state operation mode analysis discussed in Section II, there is an extra power deliver period when the auxiliary switch is ON. But the energy delivered to the load usually is quite small, which will not affect the output. Therefore, the design considerations for the main power stage, such as transformer, primary switch, and secondary rectifier is almost the same as conventional flyback converter, which will not be elaborated here.

The relationship of the key parameters of the clamp circuit will be discussed in this section, such as ZVS operation range, clamp capacitance, auxiliary switch ON time, and the clamp voltage. We still use DCM operation shown in Fig. 2(a) as an example. The conclusion can be adopted to CCM directly.

A. Ideal Condition

We simply assume that the clamp voltage almost constant in the steady-state operation, which is usually true with a relative large clamp capacitor. Also, the resonant period for the leakage inductance L_k and clamp capacitor C_c is much longer than the auxiliary switch S_a ON time T_a, which means the charge and discharge of leakage current can be simply assumed to be linearly. Also, the circuit has no power dissipation.

Since the switching transient period $[t_1$–$t_2]$ and $[t_6$–$t_7]$ is usually very short, in steady-state analysis, the transient period can be neglected to simplify the analysis. The simplified waveforms are shown in Fig. 4.

The clamp voltage is self-balanced based on the charge balance or energy balance, which means that the charge into the clamp capacitor during Mode 3 should be equal to the charge out of the clamp capacitor during Mode 6 for balancing. Based on the equivalent circuit shown in Fig. 3 for Mode 3 $[t_2$–$t_3]$ and Mode 6 $[t_5$–$t_6]$, the secondary-side rectifier diode is ON and the magnetizing inductor is clamped by the reflected output voltage. Based on assumption that the clamp voltage is constant and circuit is ideal, the current slew rate *di/dt* of the leakage inductor is exactly the same during these two modes. Thus, based on the charge balance of the clamp capacitor, the area of the triangle current waveform during these two modes is also the same. Also, the time duration $T_{\rm com}$ for leakage current decreasing to zero is proportional to the peak current $I_{\rm pk}$. And the negative peak current $I_{p\text{-neg}}$ is proportional to the time duration T_a. The primary current I_p and $T_{\rm com}$ should be satisfied

$$\begin{cases} \dfrac{1}{2}\dfrac{I_{\rm pk}^2}{di/dt} = \dfrac{1}{2}\dfrac{I_{p\text{-neg}}^2}{di/dt} \Leftrightarrow I_{\rm pk} = I_{p\text{-neg}} \\ T_{\rm com} = T_a. \end{cases} \tag{1}$$

$I_{\rm pk}$ and $I_{p\text{-neg}}$ represents the positive and negative peak value of the primary-side current. The primary peak current $I_{\rm pk}$ is determined by the load condition. The clamp voltage can be expressed as follows:

$$V_c = NV_o + \frac{L_k I_{\rm pk}}{T_a}. \tag{2}$$

From (2), it is clear that the clamp voltage depends on the leakage inductance, primary peak current, and auxiliary switch ON time T_a. The S_a ON time T_a also affects the circulating energy. The magnetizing energy stored to the clamp capacitor during Mode 3 $[t_2$–$t_3]$ and the energy is transferred back to the output during Mode 6 $[t_5$–$t_6]$, which is the circulating energy and the amount can be calculated as follows:

$$E_{\rm cir} = \frac{NV_o I_{p\text{-neg}}}{2} T_a. \tag{3}$$

A large S_a ON time leads to large circulating energy, though it helps to reduce the clamp voltage. The percentage of the circulating energy to the total output power is given as follows:

$$\text{Cir\%} = \frac{T_a}{T_{\text{s-ON}}} \tag{4}$$

where $T_{\text{s-ON}}$ is the secondary-side rectifier diode ON time. Under CRM operation, the equation can be simplified as follows:

$$\text{Cir\%} = \frac{NV_o + V_{\rm in}}{NN_o}\frac{T_a}{T_s}. \tag{5}$$

In the universal input condition, most VF control scheme (QR or OFF time) operates the converter under CRM mode at full-load and minimal input condition, which determines the maximum circulating energy. Once the load decreased or voltage increased, the converter operated in DCM mode, the circulating energy almost keeps constant. The circulating energy will cause extra conduction loss, which will offset the saved power loss using the proposed method. A small auxiliary switch ON time will reduce the circulating energy, and the clamp voltage will increase. There should be some tradeoff.

Based on the previous analysis and assumption, we can discuss the parameters and control method selection for performance optimization.

1) ZVS Operation Range: During the switching transient, i.e., Mode 7, a more simple equivalent circuit is shown in

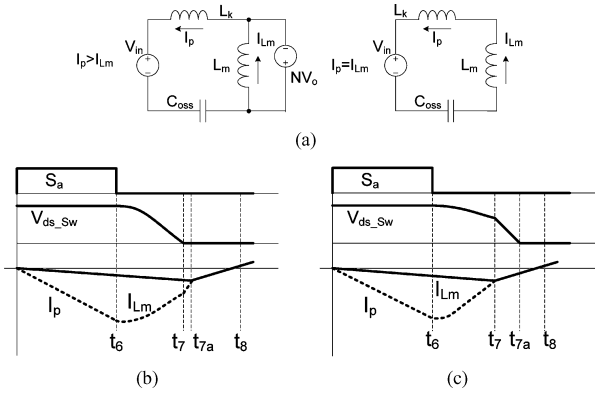


Fig. 5. Switching transient with large and small leakage energy for ZVS. (a) Simplified equivalent circuit for Mode 7. (b) Large leakage energy. (c) Small leakage energy.

Fig. 5(a). In this mode, the leakage inductor current I_p value decreases. If the leakage energy E_{L_k} is larger than the parasitic capacitor energy $E_{C_{\rm oss}}$, the ZVS operation of primary switch S_w can be achieved easily

$$E_{L_k} = \frac{1}{2}L_k I_{p\text{-neg}}^2 \geq E_{C_{\rm oss}} = \frac{1}{2}C_{\rm oss}(V_{\rm in} + NV_o)^2. \quad (6)$$

$I_{p\_\rm neg}$ is given in (1) and the value is related to the load condition. More detailed transient waveforms is shown in Fig. 5(b) if $E_{L_k} > E_{C_{\rm oss}}$. Once the drain–source voltage $V_{{\rm ds}\_S_w}$ of main switch reaches zero, the leakage current drops fast due to the voltage applied to L_k becomes $V_{\rm in} + NV_o$. When leakage current I_p reaches the magnetizing current I_{L_m}, both of them increase linearly through the antiparalleled diode of main switch S_w, as shown in Mode 8 of Fig. 3.

Under DCM operation or critical DCM operation (available for almost all VF control schemes), the magnetizing current increases reversely (secondary-side rectifier diode D_R is ON) during Mode 6 and Mode 7. The ZVS of S_w can be maintained even E_{L_k} is smaller than $E_{C_{\rm oss}}$ due to the magnetizing energy E_{L_m}, which helps to realize ZVS of S_w, as shown in Fig. 5 (c). The expression is shown as follows:

$$\frac{1}{2}L_k I_{p\text{-neg}}^2 + \frac{1}{2}L_m I_{L_m\text{-neg}}^2 \geq \frac{1}{2}C_{\rm oss}(V_{\rm in} + NV_o)^2 \quad (7)$$

$$I_{L_m\text{-neg}} = \frac{NV_o}{L_m}T_a = {\rm Cir}\%I_{\rm pk} \quad (8)$$

where $I_{L_m\text{-neg}}$ is negative peak value of magnetizing current, which is proportional to the peak current (load condition) and circulating energy.

Due to relative large magnetizing inductance, even a very small negative magnetizing current can achieve ZVS of S_w if the dead time is sufficient. However, in the real application, the larger dead time will results in low-equivalent switching frequency, which will deteriorate the overall efficiency. Also, increasing the auxiliary switch ON time helps to increase the negative magnetizing current to help ZVS operation, and it causes extra conduction loss, which may offset the saved switching loss.

For CCM operation, the magnetizing current may not change the polarity, only the leakage energy can be used to realize the ZVS operation. Equation (6) is a necessary to achieve ZVS operation of S_w.

2) Optimized Control Scheme: From (6), it is preferred that the negative peak current keeps constant with load variation. Usually, the peak current is adjusted to regulate the output power, such as QR and CF control scheme, which means the ZVS condition may not satisfied at light-load condition. For the OFF-time control method, the peak magnetizing current is fixed and the switching frequency is used to regulate the output power. Therefore, OFF-time control method is preferred for the proposed control scheme to achieve soft switching at any load condition.

3) Auxiliary switch ON time T_a: Auxiliary switch ON time decides the circulating energy and the clamp voltage as given in (2) and (5). The ON time T_a can be designed by the desired maximum clamp voltage at the full-load condition. It is an important parameter, which also affects the selection of clamp capacitance as analyzed next.

4) Leakage Inductance L_k and Dead Time T_d: For simplicity, we need to select the leakage inductance to satisfy (6) for ZVS operation. With preferred OFF-time control, the $I_{p\_\rm neg}$ in the equation is determined by the maximum switching frequency at full-load condition. Therefore, the required dead time T_d should be smaller than the quarter the resonant period

$$T_d \leq \frac{2\pi}{4}\sqrt{L_k C_{\rm oss}}. \quad (9)$$

As explained earlier, the magnetizing current also helps to achieve the ZVS under CRM or DCM operation, which may need a larger dead time. Thus, the dead time may slightly larger than the calculated value given by (9). But too large dead time will decrease the equivalent switching frequency, which results in higher peak current for full-load condition and results in higher conduction loss. In practical design, 200∼500 ns is a suitable value for proper operation.

5) Clamp Capacitance C_c: The previous analysis is based on the assumption that the clamp voltage is almost constant and the resonant period formed by the leakage inductor and clamp capacitor should be much longer than the auxiliary switch ON time. Usually, the voltage ripple should be within 5% or 10% to treat it as constant. The clamp capacitance can be expressed as follows:

$$C_c \geq \frac{I_{\rm pk}T_a}{2V_c{\rm ripple}\%} \quad (10)$$

where V_c is given in (2) and ripple% is the maximum allowed clamp voltage ripple percentage, such as 5% or 10%. It is clear that smaller T_a helps to reduce the clamp capacitance.

Also, the resonant period should be several times larger than the auxiliary switch ON time to treat it as a linear charge/discharge as given in (11). Usually, k should be above 5.

$$2\pi\sqrt{L_k C_c} \geq kT_a. \quad (11)$$

Based on these two equations, we can determine the clamp capacitance. Though large capacitance makes the operation more close to the ideal condition, it does not help much for the clamping performance and usually causes high cost and bulky

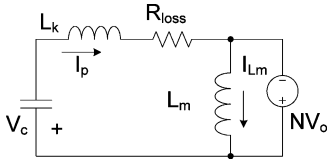


Fig. 6. Simplified equivalent circuit for Mode 3 and Mode 6.

volume. For practical application, the clamp capacitance is usually ranges from tens to hundreds of nanofarad.

6) Auxiliary Switch S_a: For the auxiliary switch S_a, the current rating is quite small, and the rms current ratio of the auxiliary switch S_a to main switch S_w is given in (12). Theoretically, a very small current rating MOSFET can be used. But the ON resistance will affect the negative peak current $I_{p\text{-neg}}$, which will be discussed later.

Compared to the conventional active clamp flyback with complementary gate drive signal, the ZVS operation of auxiliary switch is lost. Due to the small device rating, the turning ON switching loss is small

$$\frac{I_{\mathrm{rms}-S_a}}{I_{\mathrm{rms}-S_w}} = \sqrt{\frac{T_a}{T_{\mathrm{ON}}}} \tag{12}$$

where $I_{\mathrm{rms}-S_w}$ and $I_{\mathrm{rms}-S_a}$ are the rms current of the main switch S_w and auxiliary switch S_a, respectively.

B. Nonideal Condition

These assumptions mentioned earlier are only used to simply the analysis, which is usually satisfied in the practical design. In this part, we will further discuss the circuit operation and parameters design if the assumption is not validated anymore.

In the previous analysis, we simply assume the whole circuit has no power dissipation. It is usually not true for practical application. Firstly, we will discuss the influence of the circuit power loss on the circuit operation.

During Mode 3 and Mode 6, a simple equivalent circuit is given in Fig 6, an equivalent resistor R_{loss} is used to represent the circuit power loss. Though the charge balance is still valid, the negative peak current $I_{p\text{-neg}}$ is not equal to I_{pk} anymore, i.e., (1) is not valid any more. Also, the time T_a is not equal to T_{com}. The negative current can be given as follows:

$$i_p(t) = \frac{(V_{c0} - NV_o)}{L_k(s_2 - s_1)}(e^{s_1 t} - e^{s_2 t}) - \frac{I_{p0}}{(s_2 - s_1)}(s_1 e^{s_1 t} - s_2 e^{s_2 t}) \tag{13}$$

$$v_c(t) = \frac{V_{c0} - NV_o}{(s_2 - s_1)}(s_2 e^{s_1 t} - s_1 e^{s_2 t}) - \frac{I_{p0}}{C_c(s_2 - s_1)}(e^{s_1 t} - e^{s_2 t}) \tag{14}$$

$$s_1 = -\frac{R_{\mathrm{loss}}}{2L_k} + \sqrt{\left(\frac{R_{\mathrm{loss}}}{2L_k}\right)^2 - \frac{1}{L_k C_c}} \tag{15}$$

$$s_2 = -\frac{R_{\mathrm{loss}}}{2L_k} - \sqrt{\left(\frac{R_{\mathrm{loss}}}{2L_k}\right)^2 - \frac{1}{L_k C_c}} \tag{16}$$

where I_{p0} and V_{c0} are the initial current and voltage value at the beginning of the Mode 3 and Mode 6. During Mode 6, $I_{p0} = 0$ and $I_{p0} = I_{\mathrm{pk}}$ during Mode 3. The clamp voltage should be estimated using charge balance during Mode 3 and Mode 6

$$\int_0^{T_a} i_p(t)dt|_{\mathrm{Mode3}} = \int_0^{T_{\mathrm{com}}} i_p(t)dt|_{\mathrm{Mode6}}. \tag{17}$$

T_{com} can be calculated using (13)–(16) when current drops to zero, which is a function of V_c. It is not possible to get a simple expression to calculate V_c like (2). For engineering design, it is still acceptable to estimate V_c using (2).

From the current equation given earlier, the negative peak current $I_{p\text{-neg}}$ will be damped by the equivalent resistor. It is a typical transient response of a two-order circuit. It can be divided into overdamping, critical damping, and underdamping condition. The maximum auxiliary switch ON time and related peak negative current are given as follows:

$$\begin{cases} T_{a-\max} = \dfrac{\ln(s_2/s_1)}{s_1 - s_2} \\ I_{p\text{-neg}-\max} = \dfrac{(V_{c0} - NV_o)}{s_1 L_k} e^{s_2 T_{a-\max}} \end{cases} \quad \text{if } R_{\mathrm{loss}} > 2\sqrt{\frac{L_k}{C_c}} \tag{18}$$

$$\begin{cases} T_{a-\max} = \dfrac{2L_k}{R_{\mathrm{loss}}} \\ I_{p\text{-neg}-\max} = \dfrac{(V_{c0} - NV_o)}{R_{\mathrm{loss}}} e^{-1} \end{cases} \quad \text{if } R_{\mathrm{loss}} = 2\sqrt{\frac{L_k}{C_c}} \tag{19}$$

$$\begin{cases} T_{a-\max} = \dfrac{\omega_d \pi}{2} \\ I_{p\text{-neg}-\max} = \dfrac{(V_{c0} - NV_o)}{L_k \omega_d} e^{-bT_{a-\max}} \end{cases} \quad \text{if } R_{\mathrm{loss}} < 2\sqrt{\frac{L_k}{C_c}} \tag{20}$$

where $\omega_d = \sqrt{(1/L_k C_c)^2 - b^2}$ and $b = R_{\mathrm{loss}}/(2L_k)$.

To achieve soft switching of main switch, the negative peak current is much concerned. In the ideal condition, the $I_{p\text{-neg}}$ always equals to I_{pk} as analyzed before. The extra damping effect caused by the circuit power loss reduces the negative peak value, which will affect the ZVS range as given in (6). For straightforward understanding of the damping effect, the current under these three conditions mentioned earlier during Mode 6 are shown in Fig. 7 by (13). It is preferred that the auxiliary switch ON time T_a is finished when the current reaches its negative peak value as given in (18)–(20). In Fig. 7, the current value is normalized to the negative peak current $I_{p\text{-neg}}$ (equals to I_{pk}) in ideal condition as the base value, i.e., I_{p0} in (13) of Mode 3. In the calculation, $I_{\mathrm{pk}}(I_{p\text{-neg}})$ is 3 A and V_{c0} is 1 V higher above the reflected output voltage NV_o. From Fig. 7, it is clear that maximum negative current value decreases a lot if the damping is large with the same parameters.

Secondary, we will consider the clamp capacitor is not large enough, and the clamp voltage will change a lot. If the auxiliary switch ON time is smaller than $T_{a\text{-}\max}$ given in (20), the equation and analysis given for nonideal condition is still valid. If the auxiliary switch ON time T_a is larger than quarter the resonant

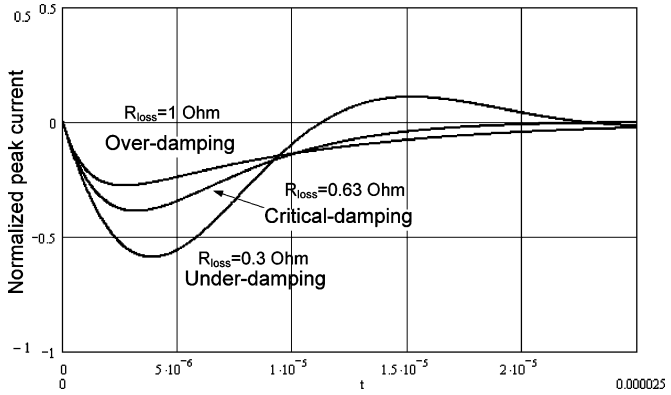


Fig. 7. Current waveforms and the damping effect at $L_k = 1\ \mu$H, $C_c = 10\ \mu$F.

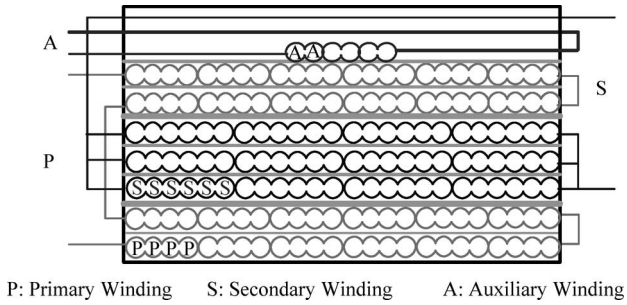


Fig. 8. Transformer structure for the prototype.

period, the leakage current will decrease with increased T_a, as shown in Fig. 7, which is not preferred for ZVS operation and circuit operation.

If the clamp voltage at the end of Mode 1 is larger than $(1+m)NV_o$, part of the leakage energy will be absorbed by the primary-side parasitic capacitor $C_{\rm oss}$ to raise the voltage to V_c and turns ON the antiparalleled diode of S_a. Therefore, the charger absorbed by the clamp capacitor during Mode 3 is slightly reduced, which will leads to a reduced negative peak current both at ideal and nonideal conditions. Usually, the value is small in practical application.

IV. Experimental Results

To verify the theoretical analysis of the proposed topology, the simulation results under ideal condition and nonideal condition are presented in Fig. 9 using PSIM software. A 16 V/4 A prototype with universal ac input is built to verify the simulation and theoretical analysis. The OFF-time control is adopted in the prototype with the controller NCP1351 from ON. The transformer core is PQ26/20 with PC40 equivalent material. The transformer is built with interleaving structure as shown in Fig. 8. The primary-side winding has four strands in parallel (with AWG28 magnet wire, OD = 0.31 mm), six turns per layer, and total four layers in series. The secondary winding has six strands in parallel (with AWG28 magnet wire), four turns per layer, and three layers in parallel. Due to the separator for creep distance is not used in the transformer bobbin, therefore, the leakage inductance is small. The auxiliary winding is only three turns with 2 AWG28 wire in parallel. A PMOS is used as auxiliary switch for simple gate drive. The key parameters of the prototype are given in Table 1. The key parameters in simulation are also the same as the prototype unless otherwise noted.

TABLE I
Key Parameters of the Experimental Prototype

Parameters	Symbol	Value
AC input voltage	V_{in}	AC 90-265V (RMS)
Output	V_o, I_o	16V/4A
Primary side switch	S_w	SPA11N60C3
Rectifier diode	D_R	V40100C
Auxiliary switch	S_a	FDP3P50 (Ron=4.9 Ohm)
Auxiliary switch on time	T_a	400ns
Controller		NCP1351B
Transformer turns ratio	$N=N_p:N_{s1}:N_{s2}$	24:4:3
Magnetizing inductance	L_m	260uH
Leakage inductance	L_k	1.5 uH
Clamp capacitor	C_c	220nF
Dead time	T_d	400ns

The designed maximum frequency is 65 kHz at full-load condition. The circuit operated under CRM at full-load and low-input condition. And the switching frequency is only related to the load condition due to OFF-time control with fixed peak current. The minimum frequency will be several hundreds hertz under very light-load condition, which is almost inaudible.

From Fig. 9, it is clear the negative peak current is not depended on the auxiliary switch time T_a under ideal condition. If the clamp circuit power loss is considered, the negative peak current is much reduced as given in (18)–(20), which is also shown in Fig. 9 (b) and (d). In the simulation, the leakage energy is much smaller than the parasitic capacitor energy. If the auxiliary switch ON time T_a is small with a fixed dead time (here 500 ns), the ZVS operation may lost. With a large T_a (here 1 μs) as shown in Fig. 9(a) and (b), the ZVS operation can be maintained due to the magnetizing energy as mentioned earlier.

The main experimental results are given in Figs. 10–15. The auxiliary switch ON time is set to 400 ns. Fig. 10 shows the gate drive signal, drain to source voltage ($V_{\rm ds\_}S_w$) of S_w and the primary-side current I_p at different load and input condition. It is clear that the soft switching of S_w is achieved at any load and input condition with OFF-time control. The parasitic ring is eliminated by the clamp capacitor. With the parameters used in the prototype, the maximum voltage stress of main switch is about 500 V at high line (ac 265 V), which is much smaller than maximum 570 V of the conventional flyback converter with RCD clamp ($R = 100$ kΩ and $C = 2.2$ nF) at the same condition. If the leakage inductance is larger, the voltage rating for the conventional flyback with RCD clamp circuit will be much higher. But in the proposed converter, it will be well limited as shown in Fig. 15. Thus, a lower voltage rating MOSFET can be used as primary switch for better efficiency with the proposed control scheme.

The equivalent circuit loss resistance is dominated by the auxiliary switch ON resistance, i.e., around 5 Ω. Based on the parameters given in Table I, the circuit is almost critical damping

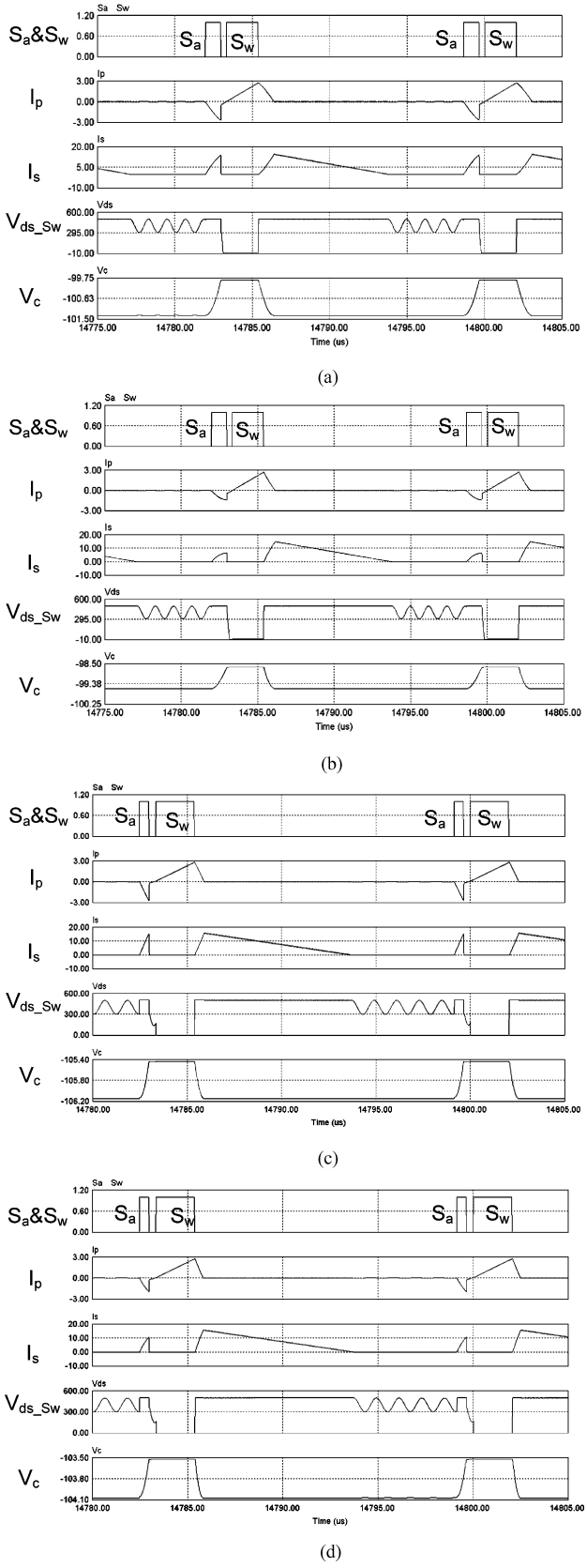


Fig. 9. Simulation waveforms for the proposed active clamp flyback converter, $L_k = 1\ \mu$H, $C_c = 1\ \mu$F, $C_{\rm oss} = 120$ pF, $T_d = 400$ ns (dead time), $V_{\rm in} = 400$ V. (a) $T_a = 1\ \mu$s and $R_{\rm loss} = 0\ \Omega$ (ideal condition). (b) $T_a = 1\ \mu$s and $R_{\rm loss} = 1\ \Omega$ (nonideal condition). (c) $T_a = 0.5\ \mu$s and $R_{\rm loss} = 0\ \Omega$ (ideal condition). (d) $T_a = 0.5\ \mu$s and $R_{\rm loss} = 1\ \Omega$ (nonideal condition).

condition. With (2) and (19), we can get the negative peak current is about 37% of the peak current, which is quite matched by the experimental results shown in Fig. 10.

Fig. 11 shows the waveforms of the primary current I_p, clamp current I_c, and secondary current I_s at different load conditions. The leakage energy is absorbed and transferred to the output side and input side when auxiliary switch S_a turns ON. The more detailed waveform at main switch turns OFF and auxiliary switch turns ON is shown in Figs. 12 and 13, respectively. The commutation period shown in Fig. 12 determines the circulating energy.

Based on the tested waveforms, the soft switching of S_w is achieved, but high *dv*/*dt* may exist in certain condition when S_a turns ON due to hard switching. Also, there is a narrow current pulse in the output side when S_a turns ON, as shown in Fig. 11. We tested the EMI performance of the proposed converter, which is almost the same to the conventional RCD clamp flyback without any input EMI filter. The *dv*/*dt* and narrow current pulse does not have much effect of the EMI performance. And the narrow current pulse still has lower *di*/*dt* than the current slew rate when S_w turns OFF. Also, with the ac ripple on the dc bus, it looks like nature frequency dithering with VF control, which also helps to reduce the *dv*/*dt* of S_a due to the turn ON point of S_a always changing. Due to the complex mechanism of the EMI coupling path and noise source, the effect on the EMI performance may need further investigation [19], [20].

The clamp voltage V_c versus the auxiliary switch ON time T_a and leakage inductance L_k is given in Figs. 14 and 15, respectively. Due to the PFET is used as auxiliary switch, the clamp capacitor voltage also includes the input voltage, which is excluded in the figures.

From Fig. 14, the calculated clamp voltage using (2) quite matches the measured one. The difference is less than 5%. Fig. 15 shows the clamp voltage versus the leakage inductance with a fixed auxiliary switch ON time. It is clear that the calculated value is very close to the measured one with different leakage inductance. The small difference in the high-leakage inductance is caused by the voltage ripple in the clamp capacitor due to high-leakage energy. During the test, an extra inductor is connected in series with the transformer primary winding to adjust the leakage inductance.

The measured efficiency of the prototype is shown in Figs. 16–19. The average efficiency is measured and calculated at 25%/50%/75%/100% load condition.

Fig. 16 shows the average efficiency comparison of the proposed converter with QR flyback (controller by NCP1207 A from ON) and OFF-time flyback with same parameters at different input voltage. The RCD clamp circuit is used for QR and OFF-time-controlled flyback with a 100 kΩ resistor and 4.7 nF capacitor. The voltage rating of S_w is much higher than the proposed circuit. The average efficiency decreases with increased input voltage due to switching loss and leakage energy loss in the conventional QR flyback.

Fig. 17 shows the average efficiency comparison of the proposed converter and the conventional active clamp flyback converter at different input voltage. For proper operation of the conventional active clamp flyback, the leakage is increased to

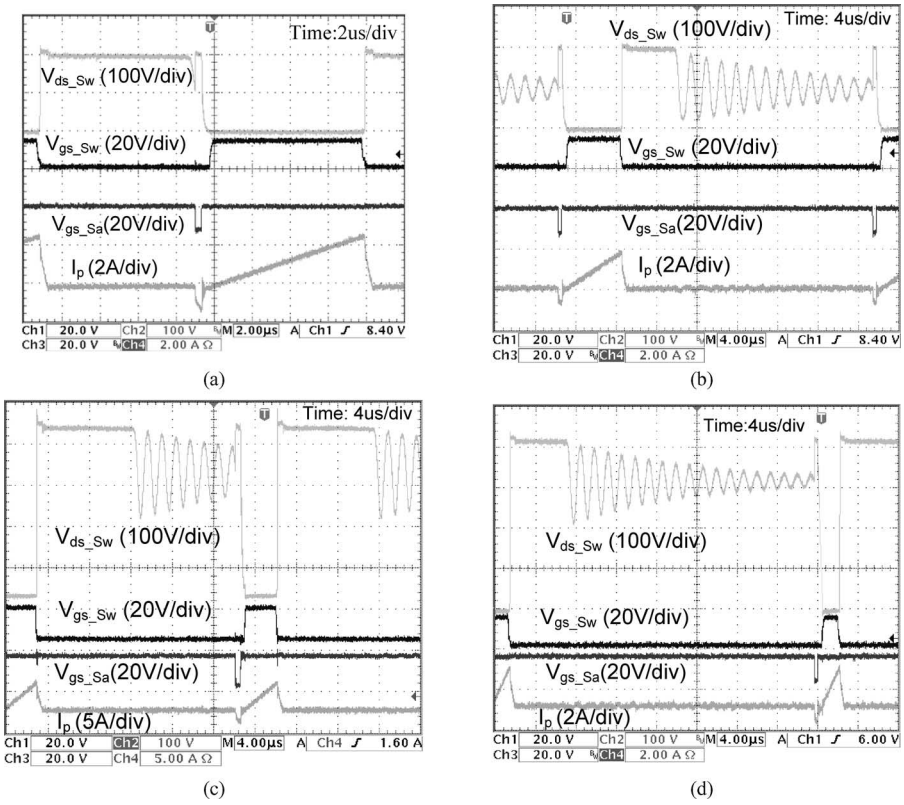


Fig. 10. Switching waveforms and primary-side current at different input and load condition. (a) $V_{\rm in} = 90\ V_{\rm ac}$ and full load ($I_o = 4$ A). (b) $V_{\rm in} = 90\ V_{\rm ac}$ and light load ($I_o = 1$ A). (c) $V_{\rm in} = 220\ V_{\rm ac}$ and full load ($I_o = 4$ A). (d) $V_{\rm in} = 220\ V_{\rm ac}$ and light load ($I_o = 1$ A).

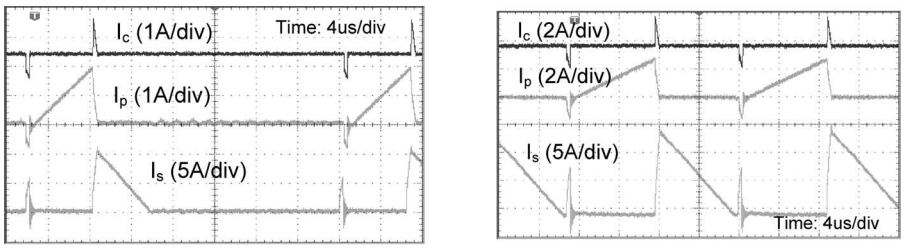


Fig. 11. Primary-side current I_p, secondary-side current I_s, and clamp circuit current I_c at different load. (a) Light-load condition ($I_o = 1$ A). (b) Full-load condition ($I_o = 4$ A).

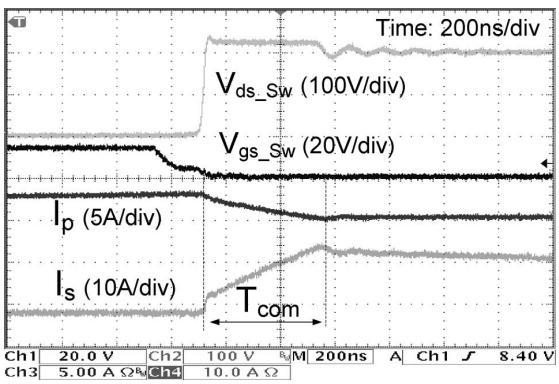


Fig. 12. Transition between I_p and I_s at S_w turns OFF.

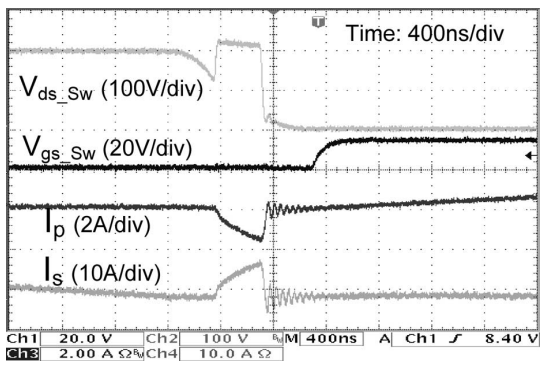


Fig. 13. $V_{\rm ds\_}{}_{S_w}$, I_p, and I_s waveform at S_a turns ON.

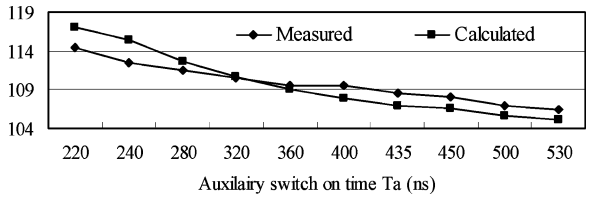


Fig. 14. Clamp voltage V_c versus T_a, $L_k = 1.5\ \mu$H, and $I_{\rm pk} = 3$ A.

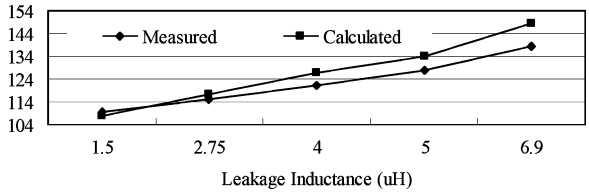


Fig. 15. Clamp voltage V_c versus L_k, $T_a = 350$ ns, and $I_{\rm pk} = 3$ A.

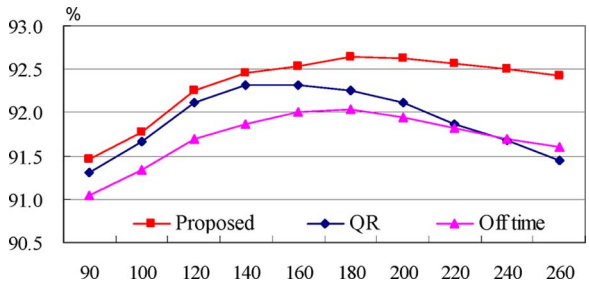


Fig. 16. Average efficiency comparison with QR and OFF-time flyback.

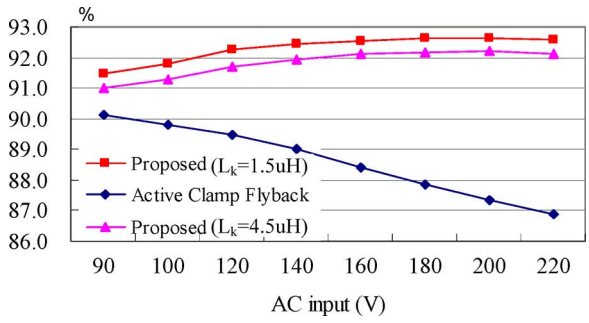


Fig. 17. Average efficiency comparison with conventional active clamp flyback.

4.5 μH. From Fig. 17, it is clear that the conventional one has low-average efficiency due to low-light-load efficiency. And the efficiency drops fast with input voltage due to large circulating energy.

Fig. 18 shows the efficiency versus output current of the proposed converter. The efficiency keeps a high level in the entire load range, especially the light-load efficiency due to OFF-time control. Fig. 19 shows the average efficiency versus the leakage inductance. It is clear that the efficiency is not sensitive to the leakage inductance variation, which makes it very attractive for applications with low cost transformers. Also, the switch voltage rating can keeps constant with proper designed auxiliary switch ON time.

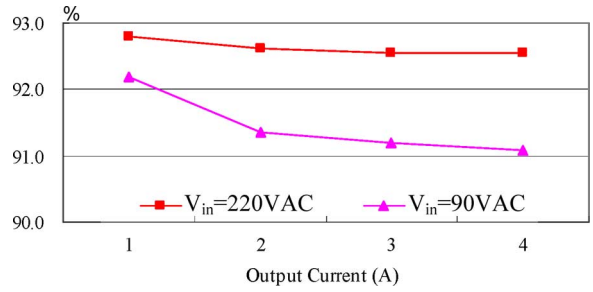


Fig. 18. Efficiency versus output current.

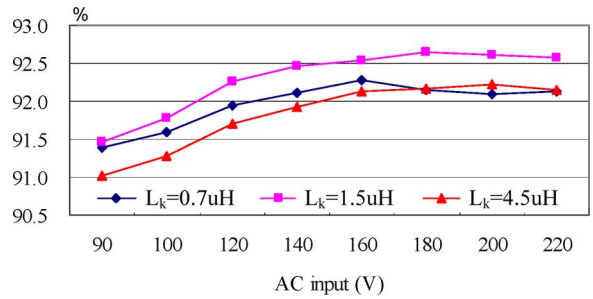
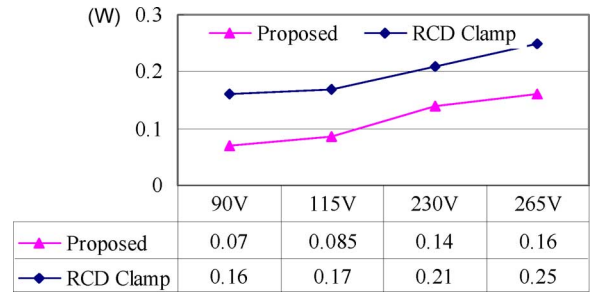
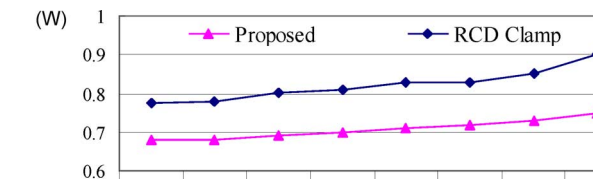


Fig. 19. Average efficiency with different leakage inductance.



	90V	115V	230V	265V
Proposed	0.07	0.085	0.14	0.16
RCD Clamp	0.16	0.17	0.21	0.25

Fig. 20. No-load power loss.



	90V	115V	140V	160V	180V	200V	230V	265V
Proposed	0.68	0.68	0.69	0.7	0.71	0.72	0.73	0.75
RCD Clamp	0.775	0.78	0.8	0.81	0.83	0.83	0.85	0.9

Fig. 21. Input power at 0.5 W output power.

The standby (no load) power loss is shown in Fig. 20, the control circuit power loss is also included. It is well below current 300 mW limitation. The input power at 0.5 W load is shown in Fig. 21. As a comparison, the standby power loss and input power at 0.5 W load for conventional RCD clamp flyback with same parameters and OFF-time control is also presented. It is clear that the proposed converter has higher light-load efficiency and lower standby power loss.

V. Conclusion

This paper proposes a high efficiency flyback converter with new active clamp control method. The proposed circuit has very attractive features, such as low device stress, soft switching operation, and high efficiency both for full-load and light-load condition. It can be adopted to various control schemes, such as CF and VF. Also, it is not sensitive to leakage inductance variation. All the advantages make it suitable for low-power offline application with strict efficiency and standby power requirement. A detailed theoretical analysis for the parameters design is presented in the paper. A 16 V/4 A prototype with universal input and OFF-time control scheme is built and compared to various flyback converter with dissipative clamp circuit or conventional active clamp flyback. The experimental results confirm the theoretical analysis and the advantages mentioned earlier.

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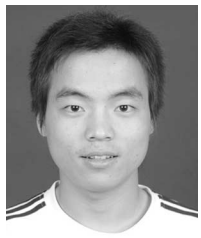

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