Analysis, design and implementation of an active clamp flyback converter

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***Abstract*—This paper presents the detailed circuit operation, mathematical analysis, and design example of the active clamp flyback converter. The auxiliary switch and clamp capacitor are used in the flyback converter to recycle the energy stored in the transformer leakage in order to minimize the spike voltage at the transformer primary side. Therefore the voltage stress of main switch can be reduced. The active clamped circuit can also help the main switch to turn on at ZVS using the switch output capacitor and transformer leakage inductance. First the circuit operation and mathematical analysis are provided. The design example of active clamp flyback converter is also presented. Finally the experimental results based on a 120W prototype circuit are provided to verify the system performance.**

Keywords-flyback converter, active clamp, zero voltage switching

I. INTRODUCTION

The flyback converters are widely used in the conventional switching mode power supplies to supply low power and low output voltage. The transformer in the flyback converter is used to achieve circuit isolation and energy storage. The switch in the flyback converter is operated at hard switching. Therefore the voltage and current stress of switch suffered from the transformer leakage inductance is very high. These high peak voltage and current will result in the low efficiency and high switching losses. The conventional passive clamp circuit can be used to reduce the energy stored in the leakage inductance using the clamp resistor. Therefore the voltage stress of switch can be reduced. However the total efficiency of converter is not greatly improved. The resonant flyback converters [1-3] were proposed to increase the system efficiency and reduce the switching losses at the main switch. However, the voltage stress at the switch is too high in the resonant flyback converters especially for the high input dc voltage. The active clamp technique has been proposed [4-6] to absorb the surge energy stored in the leakage inductance and suppress the voltage stress at the switch by using the active clamp circuit. The clamp capacitor was assumed to be a constant voltage source. The effect of the clamp capacitor on the flyback converter stability was presented in [7].

Although the active clamp flyback converter has been presented for several years, the detailed system analysis with mathematical equations is not presented. The analysis, design and implementation of a 120W active clamp flyback converter is presented in this paper to achieve zero voltage switching (ZVS) for main switch. With the auxiliary switch, clamp capacitor and resonant circuit, the surge energy stored at the leakage inductance can be recycled by the active clamp circuit. The voltage stress at the main switch is also reduced. The circuit operation and mathematical analysis are provided in the paper. A design example is also included in the paper. Finally the experimental results based on a 120W prototype circuit are provided in the paper to verify the effectiveness of the active clamp flyback converter.

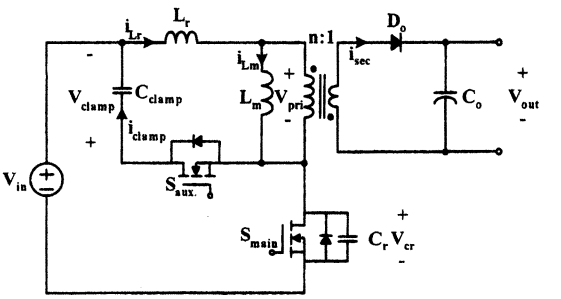


Fig. 1 Circuit configuration of the active clamp flyback converter.

II. SYSTEM ANALYSIS

Fig. 1 shows the circuit configuration of the active clamp flyback converter. The magnetizing inductance is represented as L_m. The resonant inductance L_r is the sum of transformer leakage inductance and external inductance. The resonant capacitance C_r is equal to the parallel combination of the parasitic capacitance of main switch S_{main} and auxiliary switch S_{aux}. The auxiliary switch S_{aux} and clamp capacitor C_{clamp} represent the active clamp circuit to recycle absorb the surge energy due to the leakage inductance so as to reduce the voltage stress of main switch S_{main}. The resonant capacitance C_r and inductance L_r are resonant to achieve ZVS operation for main switch S_{main}. Before the system analysis, some assumptions are made as: (1) The resonant period generated by the clamp capacitance C_{clamp} and resonant inductance L_r is greater than turn-off time of main switch; (2) The resonant inductance is less than magnetizing inductance ($L_r << L_m$); (3) All semiconductors (switches and diodes) are ideal; (4) the converter is operated in the continuous conduction mode; (5) the energy stored in the resonant inductance is greater than energy stored in the resonant capacitance in order to achieve ZVS operation for main switch.

Figs. 2 and 3 give the main waveforms and eight operation states of the converter. In the steady state, the voltage-second product when main switch or body diode is turned on equals the voltage-second product when both main switch and body diode are turned off. Therefore one can obtain the clamp capacitor voltage

$$V_{clamp} = V_{in}\frac{D}{1-D} = nV_o \qquad (1)$$

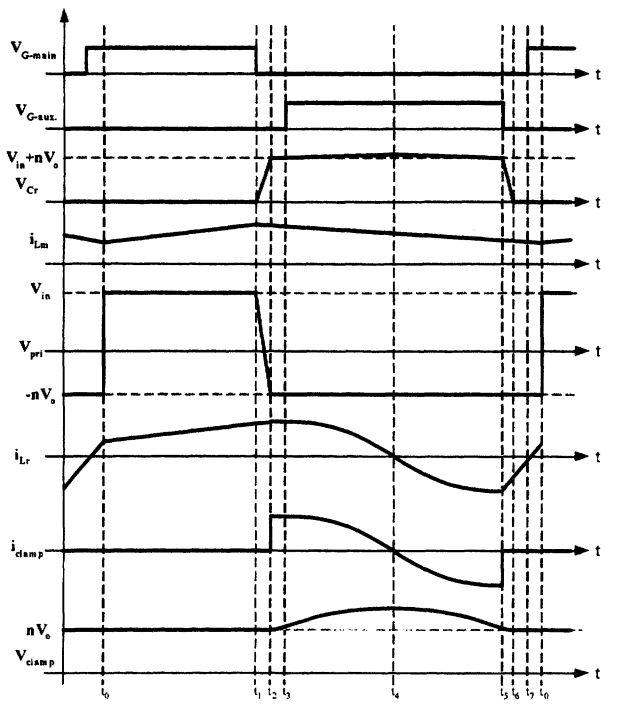
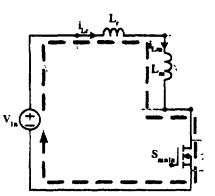
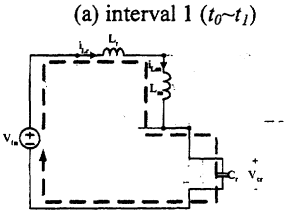


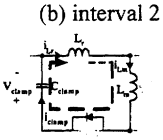
Fig. 2 Main waveforms of the active clamp flyback converter.



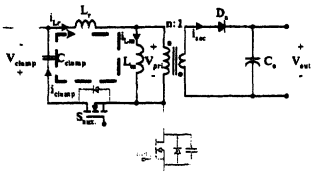
(a) interval 1 (t_0~t_1)



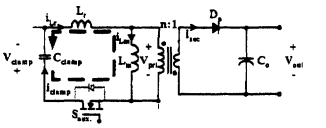
(b) interval 2 (t_1~t_2)



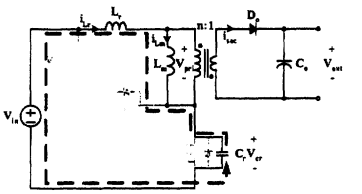
(c) interval 3 (t_2~t_3)



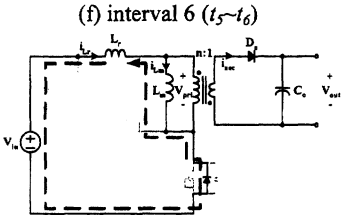
(d) interval 4 (t_3~t_4)



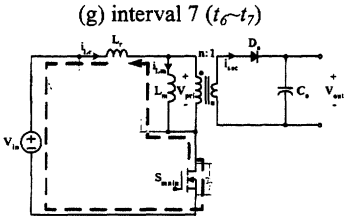
(e) interval 5 (t_4~t_5)



(f) interval 6 (t_5~t_6)



(g) interval 7 (t_6~t_7)



(h) interval 8 (t_7~t_0)

Fig. 3 Eight time intervals during one PWM period of the active clamp flyback converter.

Interval 1 (t_0 ~ t_1): In this time interval switch S_{main} is turned on and switch S_{aux} is turned off. Therefore the resonant capacitor voltage across switch S_{main} is zero ($V_{Cr}(t)=0$). The transformer primary side voltage is approximately equal to input voltage $V_{pri}(t) \approx V_{in}$ and the primary side current is expressed as:

$$i_{Lm}(t) = i_{Lr}(t) = i_{Lm}(t_0) + \frac{V_{in}}{L_m + L_r}(t - t_0) \qquad (2)$$

The secondary side diode D_o is turned off. In this interval the input energy is stored in the magnetizing inductance L_m. The clamp capacitor voltage is equal to nV_o and the clamp capacitor current $i_{clamp}(t)=0$. This interval ends (t=t_1) when main switch is turned off and the primary current at t=t_1 is $i_{Lr}(t_1) = i_{Lm}(t_0) + \frac{V_{in}}{L_m + L_r}(t_1 - t_0)$.

Interval 2 ($t_1 \sim t_2$): This interval starts at time $t=t_1$ when main switch S_{main} is turned off. The parasitic capacitance of main switch is charged from 0V to $V_{in}+V_{clamp} \approx V_{in}+nV_o$. The resonant circuit is composed of capacitor C_r, L_r and L_m. The resonant capacitor voltage and resonant inductor current are expressed as:

$$V_{Cr}(t) = V_{in}(1-\cos(\omega_1(t-t_1))) + i_{Lr}(t_1)Z_1 \sin(\omega_1(t-t_1)),$$
$$i_{Lr}(t) = i_{Lr}(t_1)\cos[\omega_1(t-t_1)] + \frac{V_{in}}{Z_1}\sin(\omega_1(t-t_1)) \quad (3)$$

where

$$\omega_1 = \frac{1}{\sqrt{C_r(L_m+L_r)}}, \qquad Z_1 = \sqrt{\frac{L_m+L_r}{C_r}} \quad (4)$$

In the circuit operation, the magnetizing current is operated in the CCM mode. Therefore $i_{Lr}=i_{Lm}$ is always positive in this interval. Therefore the time interval in this state must be less than one fourth of resonant period. The resonant capacitance is very small and capacitor voltage is charged quickly. The resonant capacitor and inductor current are approximately given as:

$$\begin{aligned} V_{Cr}(t) &= V_{in}(1-\cos(\omega_1(t-t_1))) + i_{Lr}(t_1)Z_1 \sin(\omega_1(t-t_1)) \\ &\approx i_{Lr}(t_1)Z_1\omega_1(t-t_1) = \frac{i_{Lr}(t_1)}{C_r}(t-t_1) \end{aligned} \quad (5)$$

$$\begin{aligned} i_{Lm}(t) &= i_{Lr}(t) = i_{Lr}(t_1)\cos[\omega_1(t-t_1)] + \frac{V_{in}}{Z_1}\sin(\omega_1(t-t_1)) \\ &\approx i_{Lr}(t_1)\cdot 1 + \frac{V_{in}}{Z_1}\omega_1(t-t_1) \approx i_{Lr}(t_1) + \frac{V_{in}}{L_m+L_r}(t-t_1) \end{aligned} \quad (6)$$

In this time interval the resonant capacitor V_{Cr} is less than $V_{in}+nV_o$ so that no current flows through auxiliary switch $i_{clamp}(t)=0$. The clamp capacitor voltage is still equal to nV_o. The transformer primary winding voltage is

$$V_{pri}(t) = V_{in} - V_{Cr}(t) \approx V_{in} - \frac{i_{Lr}(t_1)}{C_r}(t-t_1) \quad (7)$$

This time interval is ended when the junction capacitor voltage V_{Cr} equals $V_{in}+nV_o$ at time $t=t_2$. Therefore this time interval can be expressed as:

$$\Delta t_{12} = t_2 - t_1 \approx \frac{(V_{in}+nV_o)C_r}{i_{Lr}(t_1)} \quad (8)$$

Interval 3 ($t_2 \sim t_3$): At time t_2 the resonant capacitor voltage V_{Cr} equals to $V_{Cr}=V_{in}+V_{clamp}$ so that the body diode across auxiliary switch is turned on. The secondary side diode is still turned off. The energy stored in the inductors L_m and L_r is released to charge clamp capacitor in this interval. Since the clamp capacitance C_{clamp} is much larger than resonant capacitance C_r. Therefore almost the magnetizing current is used to charge clamp capacitor. The inductor current and clamp capacitor voltage are given as:

$$V_{clamp}(t) = nV_o\cos(\omega_2(t-t_2)) + i_{Lr}(t_2)Z_2\sin(\omega_2(t-t_2)),$$
$$i_{clamp}(t) \approx i_{Lr}(t) = i_{Lr}(t_2)\cos[\omega_2(t-t_2)] - \frac{nV_o}{Z_2}\sin(\omega_2(t-t_2)),$$
$$V_{Cr}(t) = V_{in} + nV_o\cos(\omega_2(t-t_2)) + i_{Lr}(t_2)Z_2\sin(\omega_2(t-t_2)) \quad (9)$$

where $\omega_2 = 1/\sqrt{C_{clamp}(L_m+L_r)}$ and $Z_2 = \sqrt{(L_m+L_r)/C_{clamp}}$. The transformer primary voltage is expressed as:

$$V_{pri} = -V_{clamp}\frac{L_m}{L_m+L_r} \quad (10)$$

This interval is ended when the transformer primary voltage V_{pri} equals $-nV_o$ at time $t=t_3$. In this moment the clamp capacitor voltage V_{clamp} equals $nV_o(L_m+L_r)/L_m$ and secondary side diode conducts.

Interval 4 ($t_3 \sim t_4$): At time $t=t_3$ the primary side voltage V_{pri} equals $-nV_o$ so that the secondary diode D_o is turned on. The resonant inductance L_r and clamp capacitance C_{clamp} begin to resonant. In order to ensure ZVS operation for auxiliary switch, the auxiliary switch should be turned on before i_{clamp} goes to negative. The energy stored in the magnetizing inductance is transferred to output load. The magnetizing current is decreased and expressed as:

$$i_{Lm}(t) = i_{Lm}(t_3) - \frac{nV_o}{L_m}(t-t_3) \quad (11)$$

The clamp capacitor voltage and leakage current are expressed as:

$$\begin{aligned} V_{clamp}(t) &= nV_o - (nV_o - V_{clamp}(t_3))\cos(\omega_3(t-t_3)) \\ &\quad + i_{Lr}(t_3)Z_3\sin(\omega_3(t-t_3)), \\ V_{Cr}(t) &= V_{in} + nV_o - (nV_o - V_{clamp}(t_3))\cos(\omega_3(t-t_3)) \\ &\quad + i_{Lr}(t_3)Z_3\sin(\omega_3(t-t_3)), \\ i_{clamp}(t) &\approx i_{Lr}(t) = \frac{(nV_o - V_{clamp}(t_3))}{Z_3}\sin(\omega_3(t-t_3)) \\ &\quad + i_{Lr}(t_3)\cos(\omega_3(t-t_3)) \end{aligned} \quad (12)$$

where $\omega_3 = 1/\sqrt{C_{clamp}L_r}$ and $Z_3 = \sqrt{L_r/C_{clamp}}$. The secondary side current is given as:

$$i_{Do}(t) = n(i_{Lm}(t) - i_{Lr}(t)) \quad (13)$$

The auxiliary switch is turned on in this interval to ensure the ZVS turn-on operation. This interval is ended when the clamp current is zero.

Interval 5 ($t_4 \sim t_5$): The system analysis in this interval is the same as in interval 4 except the clamp capacitor current is reversed. This interval is ended when the auxiliary switch is turned off.

Interval 6 ($t_5 \sim t_6$): At time $t=t_5$ the auxiliary switch is turned off. In this interval the secondary side diode D_o still turns on and $V_{pri}=-nV_o$. The magnetizing current is

$$i_{Lm}(t) = i_{Lm}(t_5) - \frac{nV_o}{L_m}(t-t_5) \quad (14)$$

The negative current i_{Lr} will discharge capacitor voltage V_{Cr}. The resonant circuit is formed by the resonant inductance L_r and parasitic capacitance C_r. The capacitor voltage V_{Cr} and inductor current i_{Lr} are expressed as:

$$\begin{aligned} V_{Cr}(t) &= V_{in} + nV_o - (V_{in} + nV_o - V_{Cr}(t_5))\cos(\omega_4(t-t_5)) \\ &\quad + i_{Lr}(t_5)Z_4\sin(\omega_4(t-t_5)) \end{aligned},$$

$$i_{Lr}(t) = i_{Lr}(t_5)\cdot\cos(\omega_3(t-t_5)) + \frac{(V_{in}+nV_o-V_{Cr}(t_5))}{Z_4}\cos(\omega_4(t-t_5)) \quad (15)$$

where $\omega_4 = 1/\sqrt{C_r L_r}$ and $Z_4 = \sqrt{L_r/C_r}$. The clamped capacitor voltage $V_{clamp}(t) \approx nV_o$ and $i_{clamp}(t) = 0$. The secondary side diode current is expressed as:

$$i_{Do}(t) = n(i_{Lm}(t) - i_{Lr}(t)) \quad (16)$$

To ensure the ZVS of the main switch, the energy stored in L_r must be greater than the energy stored in C_r. The following condition must hold:

$$V_{Cr}(t_5) \approx V_{in} + nV_o > i_{Lr}(t_5)Z_4 \quad (17)$$

This interval is ended when $V_{Cr}=0$.

Interval 7 ($t_6 \sim t_7$): At time $t=t_6$ the resonant capacitor voltage $V_{Cr}=0$ and the anti-parallel diode across main switch is turned on. The transformer primary voltage $V_{pri}(t) = -nV_o$ and the magnetizing current $i_{Lm}(t) = i_{Lm}(t_6) - \frac{nV_o}{L_m}(t-t_6)$. The voltage across leakage inductor V_{Lr} equals $V_{in}+nV_o$ and the leakage inductor current is linearly increased.

$$i_{Lr}(t) = i_{Lr}(t_6) + \frac{(V_{in}+nV_o)}{L_r}(t-t_6) \quad (18)$$

The transformer secondary side current is decreased with negative current slope

$$\frac{di_{Do}}{dt} = -n\left(\frac{nV_o}{L_m} + \frac{V_{in}+nV_o}{L_r}\right) \approx -n\frac{V_{in}+nV_o}{L_r} \quad (19)$$

The secondary side diode current $i_{Do}(t)=n(i_{Lm}(t)-i_{Lr}(t))$.

The clamped capacitor voltage $V_{clamp} \approx nV_o$ and $i_{clamp}=0$. Before the inductor current i_{Lr} is positive, the main switch is turned on to ensure ZVS operation. This interval is ended when main switch is turned on.

Interval 8 ($t_7 \sim t_0$): This interval starts when the main switch is turned on at time $t=t_7$. The transformer secondary side current i_{Do} is decreasing and the leakage inductor current i_{Lr} is increasing. At time $t=t_0$ the transformer secondary side current $i_{Do}=0$ and this interval is ended. In this interval the main voltage and current in the circuit are expressed as:

$$V_{pri}(t) = -nV_o,\ V_{Cr}(t) = 0,\ V_{clamp}(t) = nV_o,$$

$$i_{Lr}(t) = i_{Lr}(t_7) + \frac{(V_{in}+nV_o)}{L_r}(t-t_7),$$

$$i_{Lm}(t) = i_{Lm}(t_7) - \frac{nV_o}{L_m}(t-t_7),\ i_{clamp}(t) = 0. \quad (20)$$

III. Circuit Design Procedure

One assumed that the maximum duty cycle of active clamp flyback converter is D_{max}. The turn ratio between the transformer primary side and secondary side is equal to

$$n = \frac{N_1}{N_2} = \frac{V_{in,\min}}{V_o}\frac{D_{\max}}{1-D_{\max}} \quad (21)$$

If the clamp capacitance is large enough, the voltage across the resonant inductance can be neglected. The voltage stress of main switch is approximately equal to

$$V_{Smain,\max} = V_{in,\max} + n\cdot V_o + i_{Lr}(t_3)Z_3 \quad (22)$$

The peak current of main switch is expressed as:

$$I_{Smain,p} = \frac{P_o}{\eta\cdot V_{in,\min}\cdot D_{\max}} + \frac{V_{in,\min}}{L_m}D_{\max}T_{sw} \quad (23)$$

where T_{sw} is the switching period. To ensure the ZVS operation for main switch, the energy stored in the resonant inductance must be greater than the energy stored in the resonant capacitance.

$$L_r > \frac{C_r(V_{in,\max}+nV_o)^2}{I^2_{Smain,p}} \quad (24)$$

From Figs. 2 and 3 the clamp capacitor and leakage inductor are resonant about half of period. Therefore the half of the resonant period is approximately equal to the turn-off time of main switch.

$$\frac{T_r}{2} = \pi\sqrt{L_r C_{clamp}} = (1-D_{\min,Vin})T_{sw} \quad (25)$$

where $D_{min,Vin}=(D_{max}V_{in,min})/V_{max,min}$. Therefore the clamp capacitance can be obtained as:

$$C_{clamp} = \frac{[(1-D_{\min Vin})T_{sw}]^2}{\pi^2 L_r} \quad (26)$$

The voltage stress of rectifier diode at the transformer secondary side is

$$V_{Do,\max} = \frac{V_{in,\max}}{n} + V_o \quad (27)$$

The peak secondary diode current is expressed as:

$$I_{Do,p} = \frac{2P_o}{V_o\cdot(1-D_{\max})} \quad (28)$$

The output filter capacitance C_o is expressed as:

$$C_o \approx \frac{D_{\max}\cdot P_o}{f_{sw}\cdot V_o\cdot\Delta V_o} \quad (29)$$

where ΔV_o is output voltage ripple.

IV. Design Example

The system parameters of the design circuit are:

- input ac voltage range $V_{s,RMS}$: 90V~130V
- output voltage V_o= 12V
- rated output power P_o=120W
- switching frequency f_{sw}=150 kHz
- circuit efficiency $\eta > 0.85$
- Output voltage ripple $\triangle V_o$=0.1V.

The ETD-39 core with B_{max}=2000G and A_e=1.25cm^2 was used as an isolation transformer. The designed maximum duty cycle D_{max} is equal to 0.45. The turn ratio between the transformer primary side and secondary side is equal to $n = \frac{N_1}{N_2} = \frac{V_{in,\min}}{V_o}\frac{D_{\max}}{1-D_{\max}} \approx 8$. The voltage stress of main switch is $V_{Smain,max} \approx 130\sqrt{2} + 8\cdot 12 = 280V$. The magnetizing inductance of the transformer is designed as

L_m=524μH. The peak current of main switch is $I_{Smain,p}$=3.2A. The voltage stress of the secondary side diode is $V_{Do,max}$=35V. The peak secondary diode current is $I_{Do,p}$=36.3A. The selected resonant frequency by L_r and C_r is 1MHz. To ensure ZVS operation, the delay time (t_d) between intervals 6 and 7 is t_d=1/(4f_r)=250ns. The MOSFETs IRFP460 are used for main and auxiliary switches in the adopted converter. The C_{oss} of IEFP460 is about 500pF. Therefore the equivalent resonant capacitor C_r is approximately equal to 1.5nF. The selected resonant inductor L_r is about 17μH. The clamp capacitance C_{clamp}=0.18μF.

V. Experimental Results

A 120W prototype circuit was built and tested in the laboratory. The system parameters of converter are shown in section IV. Fig. 4 shows the experimental prototype circuit of active clamp flybacj converter. Fig. 5 shows the experimental waveforms of the gate-to-source voltages of main switch and auxiliary switch and the drain-to-source voltage of main switch. There is a time delay between the auxiliary switch turn-off and main switch turn-on to ensure main switch turn-on at ZVS. Fig. 6 gives the experimental waveforms of gate signals of main switch $v_{Smain,gs}$ and auxiliary switch $v_{Saux,gs}$ and transformer primary voltage v_{pri}. When main switch is turned on, the transformer primary side voltage is equal to V_{in}. If the main switch is turned off, the primary side voltage equals -nV_o=-96V. Fig. 7 illustrates the measured results of gate signals $v_{Smain,gs}$ and $v_{Saux,gs}$ and clamped capacitor voltage v_{clamp}. When the auxiliary switch is turned on, the clamp capacitance is resonant with resonant inductance. Therefore the clamp voltage is resonant in this period. When the auxiliary switch is turned off, the clamp capacitor voltage is clamped to nV_o=96V. Fig. 8 shows the measured results of gate-to-source and drain-to-source voltage for main switch. Before the mains switch is turned on the drain-to-source voltage has been reached zero. Therefore the main switch is ZVS turn-on. Fig. 9 gives the experimental waveform of output capacitor voltage v_o at 120W output load. The system efficiency of the adopted system is about 83%.

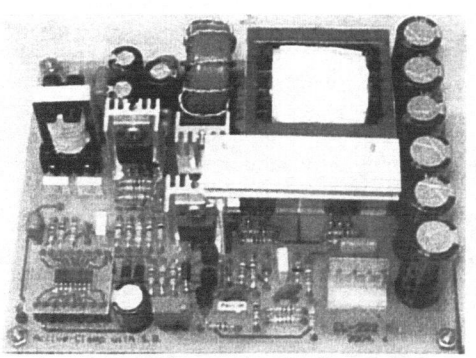


Fig. 4 Experimental prototype circuit of active clamp flyback converter.

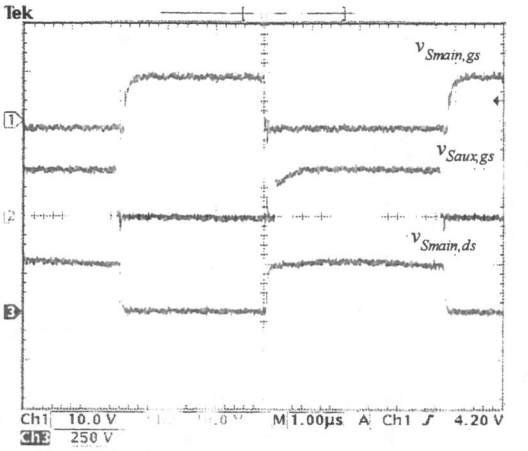


Fig. 5 Experimental waveforms of gate signals for main switch $v_{Smain,gs}$ and auxiliary switch $v_{Saux,gs}$ and drain to source voltage $v_{Smain,ds}$.

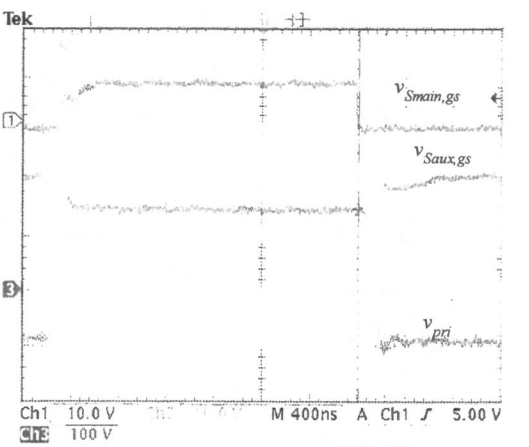


Fig. 6 Experimental waveforms of gate signals for main switch $v_{Smain,gs}$ and auxiliary switch $v_{Saux,gs}$ and transformer primary voltage v_{pri}.

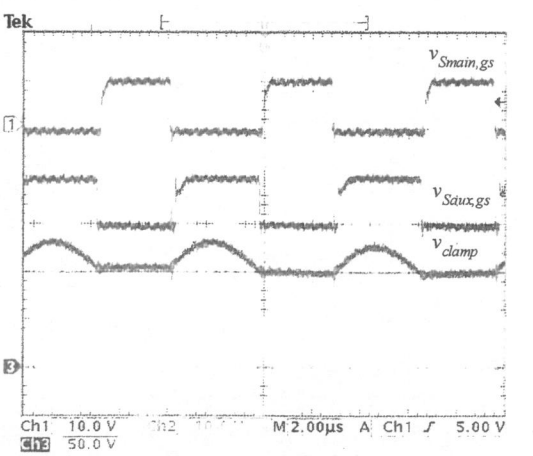


Fig. 7 Experimental waveforms of gate signals for main switch $v_{Smain,gs}$ and auxiliary switch $v_{Saux,gs}$ and clamped capacitor voltage v_{clamp}.

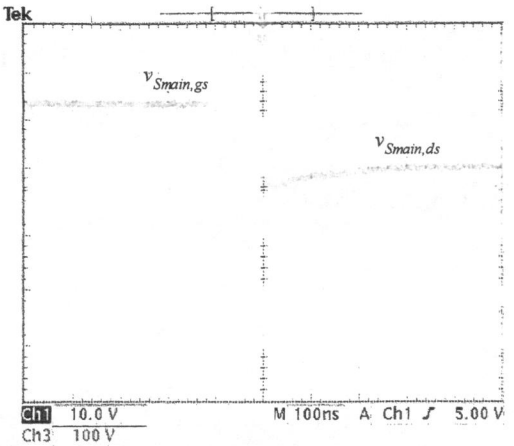


Fig. 8 Experimental waveforms of gate-to-source and drain-to-source voltage for main switch.

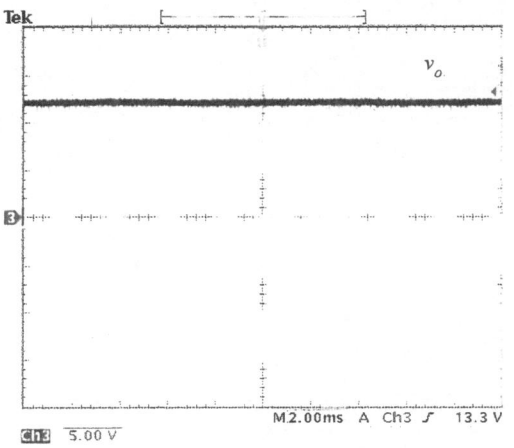


Fig. 9 Measured output voltage v_o waveform at 120W output load.

VI. CONCLUSION

This paper gives a detailed circuit description and mathematical analysis of the active clamp flyback converter. The auxiliary clamp circuit is used to recycle the energy stored in the leakage inductance and suppress the voltage stress of main switch. The clamp circuit can also help the main switch to turn on at ZVS. The circuit design procedure and design example of a 120W converter is also presented in this paper. The experimental results of prototype circuit demonstrate the features of high efficiency and ZVS operation.

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