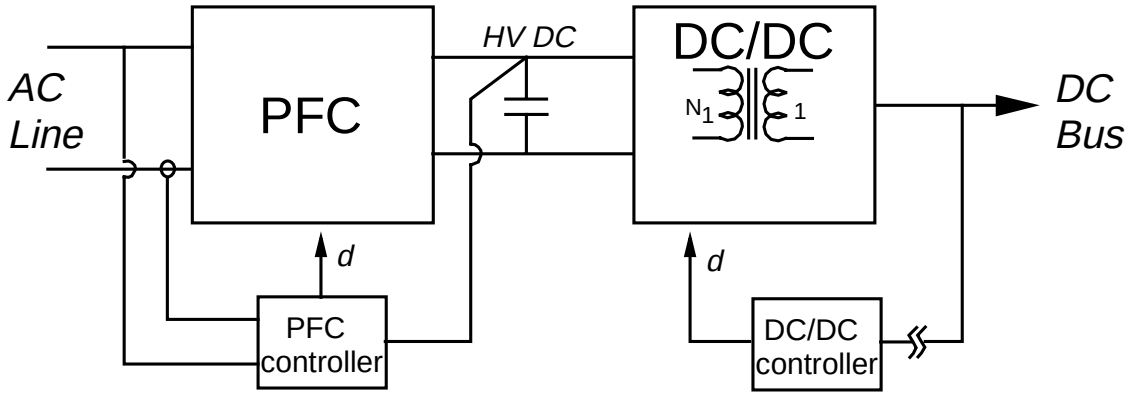
3. ACTIVE-CLAMP FLYBACK AS AN ISOLATED PFC FRONT-END CONVERTER

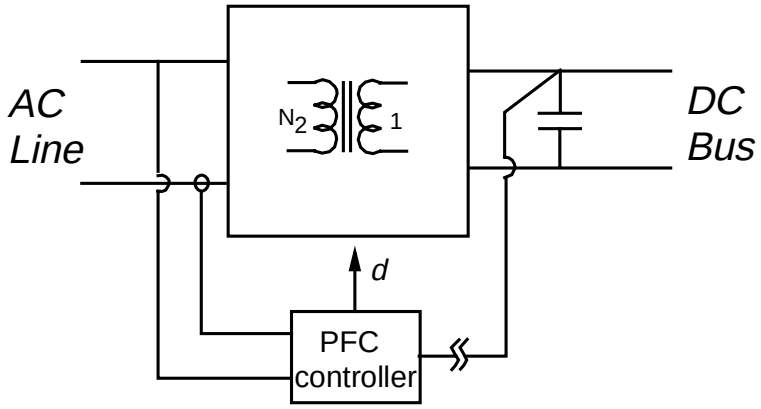
3.1 Introduction

In this chapter, the flyback (isolated buck/boost) topology is used to simplify the two-stage front-end design to a single isolated PFC conversion stage. This is conceptually illustrated in Fig. 3.1, where it is assumed unity power factor is present at the line input. The two keys to the process of simplifying the two-stage approach are the incorporation of transformer isolation in the PFC converter and the subsequent movement of the bulk capacitor from the primary to the secondary. The result of this is that the input line current's second harmonic (at 120 Hz) is processed by the isolation transformer and appears as voltage ripple on the output DC bus. Therefore, in effect, the post-regulators in the DC distributed power system take the functional place of the second-stage DC/DC converter in the two-stage front-end approach.

The flyback topology has long been attractive because of its relative simplicity when compared with other topologies used in low power applications. The flyback "transformer" serves the dual purpose of providing energy storage as well as converter isolation, theoretically minimizing the magnetic component count when compared with, for example, the forward converter. A drawback to the use of the flyback is the relatively high voltage and current stress suffered by its switching components. High peak and RMS current stress is a particular problem for flybacks



(a) Two-stage front-end.



(b) Front-end consisting of an isolated PFC converter only.

Fig. 3.1 Two-stage and isolated PFC front-end conceptual designs.

when operating in discontinuous conduction mode (DCM) and is in fact a primary detriment to increasing output power. An addition, high turn-off voltage (caused by the parasitic oscillation between the transformer leakage inductance and the switch capacitance) seen by the primary switch traditionally requires the use of a RCD clamp to limit the switch voltage excursion. Unfortunately, in this scheme the energy stored in the transformer leakage is dissipated in the clamp resistor, resulting in a difficult design trade-off between clamping action and clamp circuit power dissipation.

The limitations presented by the RCD clamp can be largely overcome by replacing the passive clamp with an active-clamp circuit as shown in Figure 3.2. Active-clamp methods have been explored in detail for forward converters [40, 46]. The active-clamp circuit provides the benefits of recycling the transformer leakage energy while minimizing turn-off voltage stress across the power switch. In addition, the active-clamp circuit provides a means of achieving zero-voltage-switching (ZVS) for the power switch and subsequent lowering of the output rectifier di/dt. This results in decreased rectifier switching loss and output switching noise. To achieve soft-switching characteristics over a useful operating range, the addition of a small resonant inductor in the active-clamp loop is usually necessary (see Fig. 3.2).

The use of the active-clamp circuit to achieve soft switching in flyback converters operating with bi-directional magnetizing current is well documented [40, 41, 42]. By bi-directional magnetizing current it is meant that the flyback transformer ripple current is allowed to become negative (i.e. reverse direction relative to magnetizing current flow defined in Fig. 3.2) for a portion of each switching cycle. This is only possible in conjunction with the operation of the active-clamp network. The (negative) magnetizing current can then be used to discharge the primary switch capacitance and achieve ZVS. However, for higher output power operation, it is more desirable to minimize the transformer's ripple current content to reduce device current stress [15, 43]. This is directly analogous to CCM vs. DCM operation in "conventional" flyback converters, where, given identical operating conditions, DCM operation will result in greater device

peak current stress and RMS currents than CCM operation. However, ZVS can still be realized with unidirectional magnetizing current by utilizing the energy stored in the resonant inductor [44]. The presence of the resonant inductor also helps to softly commute the turn-off of the output rectifier, resulting in reduced output noise and rectifier switching losses. This would also be a particular advantage in high output voltage applications where slower rectifiers are more likely to be used.

This chapter presents evaluation of a constant-frequency, soft switching, active-clamp flyback converter suitable for both PFC and DC/DC conversion applications. The basic principle of operation is analyzed and a design procedure is developed. Experimental results are then presented which illustrate converter function and verify the analysis presented. These results are then extended to active-clamp flyback single-stage and interleaved PFC applications where the system power levels are limited to about 500 - 600 W.

3.2 Active-Clamp Flyback Converter Overview

The incorporation of an active-clamp circuit into the basic flyback topology is shown in Fig. 3.2. In the figure, the flyback transformer has been replaced with an equivalent circuit model showing the magnetizing and leakage inductances (L_r represents the total transformer leakage inductance reflected to the primary in addition to any external inductance). Switches S1 and S2 are shown with their associated body diodes. C_r represents the parallel combination of the parasitic capacitance of the two switches. It is this device capacitance resonating with L_r that enables ZVS for S1. With the active-clamp circuit, the transistor turn-off voltage spike is clamped, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for both primary (S1) and auxiliary (S2) switches becomes a possibility. These advantages come at the expense of additional

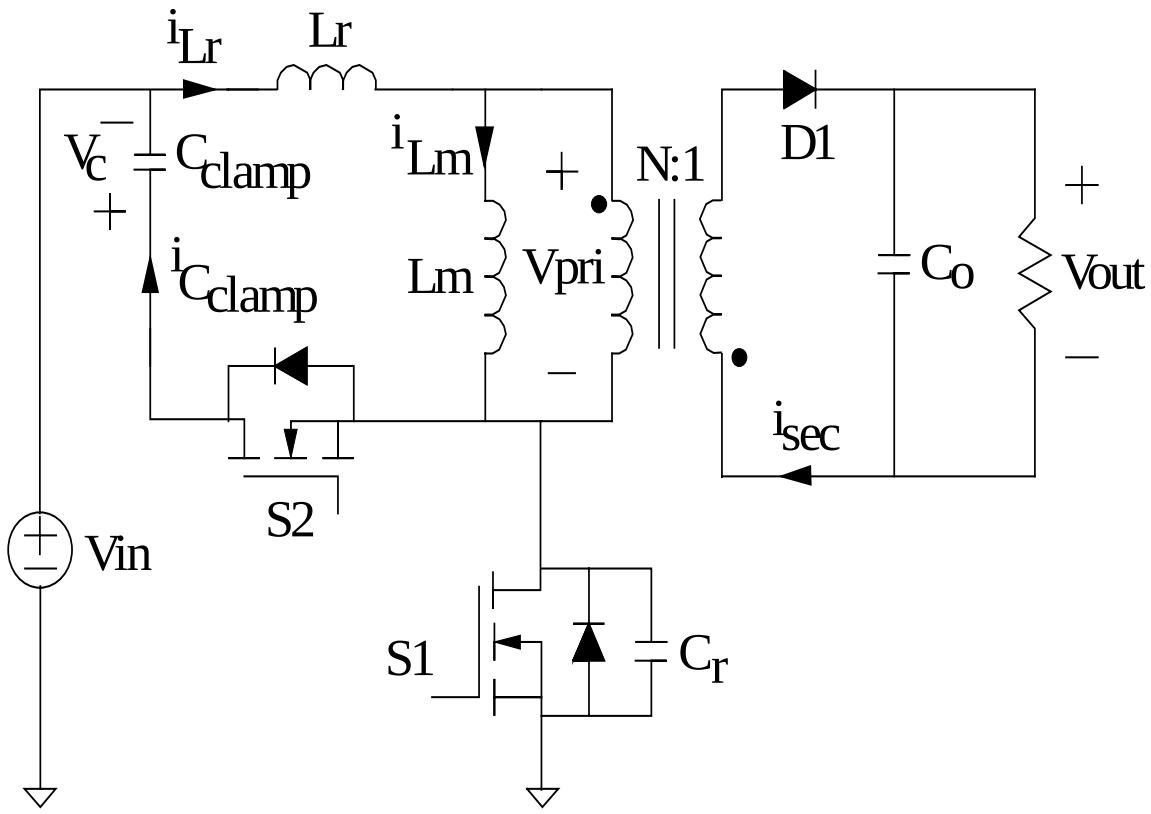


Fig. 3.2 Simplified schematic of the active-clamp flyback converter

power stage components and increased control circuit complexity (two switches as opposed to the usual one switch).

Figure 3.3 illustrates the topological states and Fig. 3.4 the key waveforms for the active-clamp flyback converter. For this description of circuit operation (and for the subsequent development of a design procedure in the next section), the following assumptions are made:

- ideal switching components;
- the magnetizing current is always non-zero and positive (positive direction as defined by Fig. 3.2);
- L_r (includes the transformer leakage inductance) is much less than the transformer magnetizing inductance, L_m (typically 5% to 10% of L_m);
- sufficient energy is stored in L_r to completely discharge C_r and turn on S1's body diode;
- and, $\pi\sqrt{L_r C_{clamp}} >> T_{off}$.

The last assumption simply states that one-half the resonant period formed by L_r and C_{clamp} is much longer than the maximum off time of S1 ($T_{off} \cong (1-D)T_S$). The sequence of topological states is described below:

T_0 - T_1: At T_0, switch S1 is on, and the auxiliary switch, S2, is off. The output rectifier, D1, is reversed biased as is the anti-parallel diode of S2. The magnetizing inductance (along with the resonant inductance) is being linearly charged just as it would be during the inductor-charging phase in "normal" flyback operation.

T_1 - T_2: S1 is turned off at T_1. C_r is charged by the magnetizing current (which is also equal to the current through the resonant inductor). C_r is actually charged in a resonant manner, but the charge time is very brief, leading to an approximately linear charging characteristic.

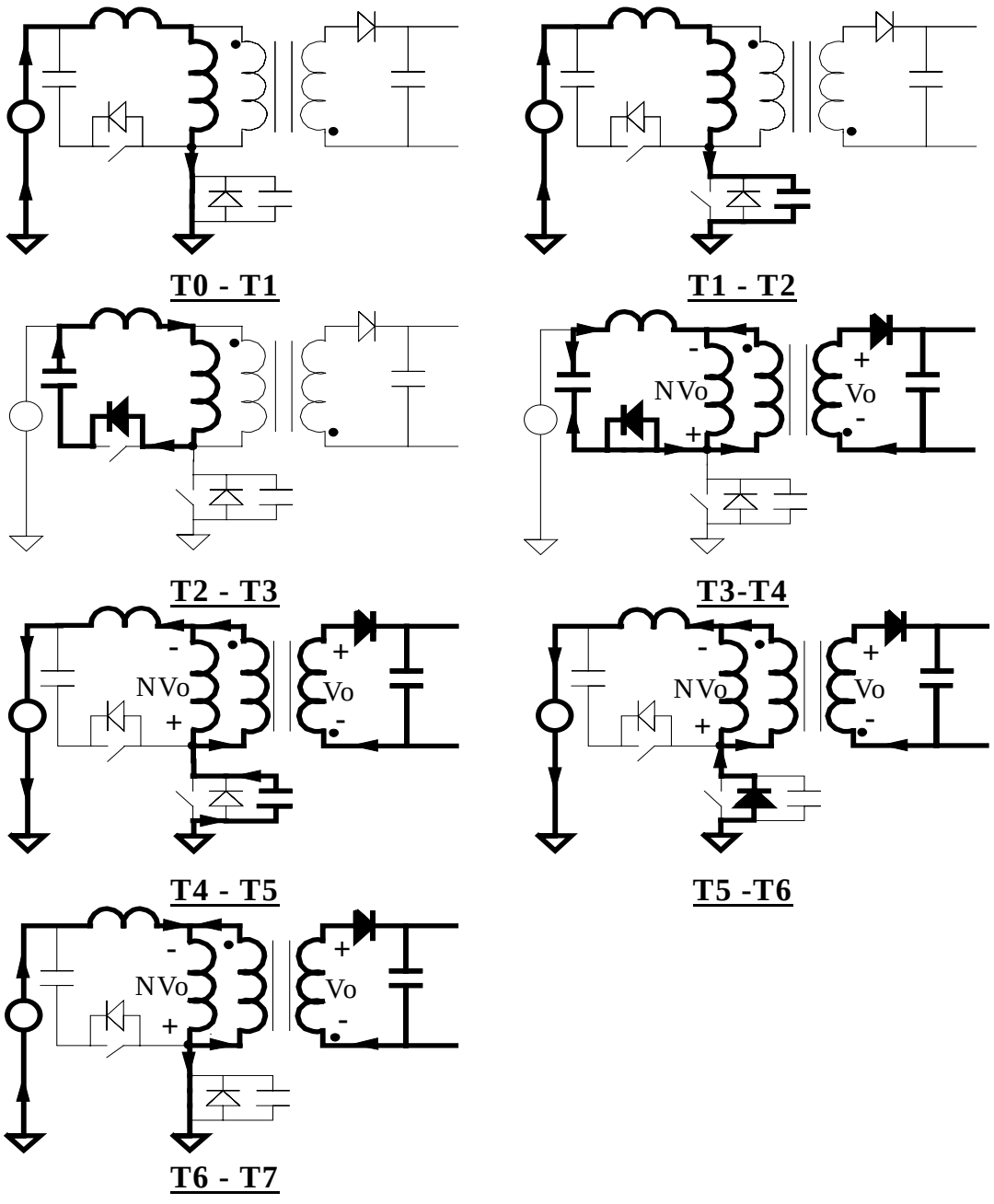


Fig. 3.3 Active-clamp flyback topological states.

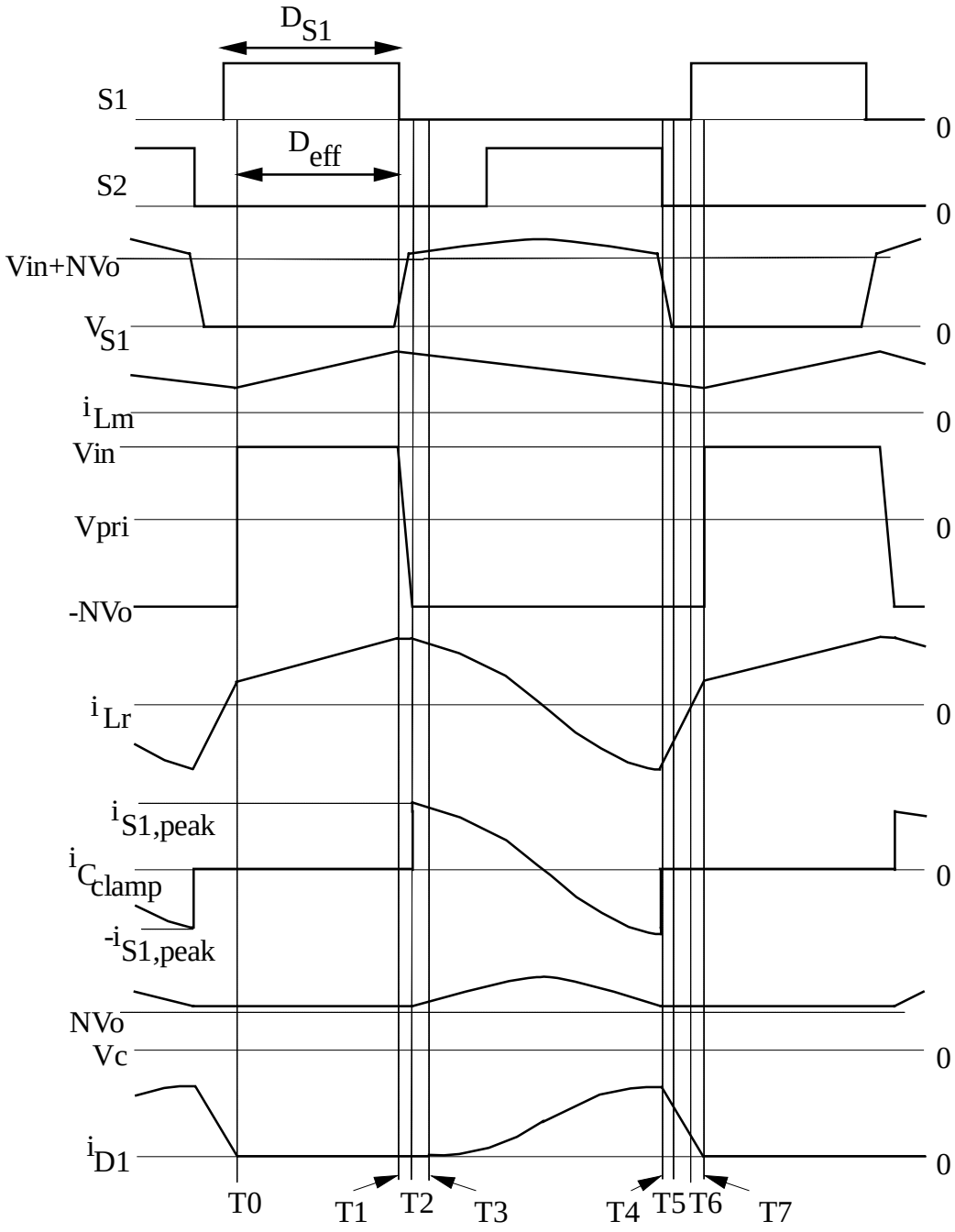


Fig. 3.4 Active-clamp flyback steady-state waveforms.

T_2 - T_3: At T_2, C_r is charged ($V_{DS} = V_{in} + V_c$) to the point where the anti-parallel diode of S2 starts to conduct. The clamp capacitor fixes the voltage across L_r and the transformer magnetizing inductance to V_c ($\cong NV_o$), forming a voltage divider between the two inductances. Since C_{clamp} is much larger than C_r, nearly all of the magnetizing current is diverted through the diode to charge the clamp capacitor. Consequently, the voltage appearing across the magnetizing inductance, V_{pri}, decreases as V_c increases, according to the voltage divider action described by Eq. (3.1):

$$V_{pri} = -V_c \frac{L_m}{L_r + L_m}. \tag{3.1}$$

T_3 - T_4: At T_3, V_{pri} has decreased to the point where the secondary transformer voltage is sufficient to forward bias D1. The transformer primary voltage is then clamped by the (very large) output capacitance to approximately NV_o. L_r and C_{clamp} begin to resonate. In order for S2 to achieve ZVS, the device should be turned on before $i_{C_{clamp}}$ reverses direction.

T_4 - T_5: The auxiliary switch, S2, is turned off at T_4, effectively removing C_{clamp} from the circuit. A new resonant network is formed between the resonant inductor and the MOSFET parasitic capacitances. The transformer primary voltage remains clamped at NV_o as C_r is discharged.

T_5 - T_6: Assuming the energy stored in L_r is greater than the energy stored in C_r, at T_5 C_r will be sufficiently discharged to allow S1's body diode to start conducting. The voltage across the resonant inductor becomes clamped at $V_{in} + NV_o$. This also fixes the rate of decay of the output rectifier current to:

$$\frac{di_{D1}}{dt} = -N\left(\frac{NV_o}{L_m} + \frac{V_{in} + NV_o}{L_r}\right). \quad (3.2)$$

For $L_m >> L_r$ Eq. (3.2) simplifies to:

$$\frac{di_{D1}}{dt} \cong -N\frac{V_{in} + NV_o}{L_r}. \quad (3.3)$$

It is during this interval that switch S1 can be turned on under zero-voltage conditions.

T_6 - T_7: S1 is on, and the secondary current is decreasing as the resonant inductor current increases. At T_7, the secondary current decreases to zero (because the resonant inductor current has equaled the magnetizing current), and D1 reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and resonant inductances begin to linearly charge again, starting another switching cycle ($T_7 = T_0$).

Note that the length of the time intervals T_1 to T_3 and T_4 to T_7 have been greatly exaggerated in Fig. 3.4 in order to more clearly show the transition periods.

3.3 Soft-Switching Flyback Design Considerations

To achieve zero-voltage switching for S1, S2 must be turned on during the T_5 to T_6 time interval. If not, the resonant inductor current reverses (becoming positive again), recharging C_r, and ZVS is lost (or at least partially lost). Therefore, the delay time between the turn off of S2 and the turn on of S1 is critical to ZVS operation. The optimum value of this delay is one-quarter of the resonant period formed by L_r and C_r:

$$T_{delay} = \frac{\pi}{2}\sqrt{L_r C_r} \ . \qquad (3.4)$$

The value of C_r is also a function of applied voltage (particularly at small drain-to-source voltages). Eq. (3.4) is an approximation.

In addition to the S1/S2 timing requirement there must also be sufficient energy stored in the resonant inductor to completely discharge the switch capacitance. This requirement is valid at time instant T_4 (when S2 is turned off):

$$E_{L_r} \geq E_{C_r}\Big|_{@\ S2\ turn\ off} \ . \qquad (3.5)$$

It should be noted that even if insufficient energy is stored in L_r to completely discharge the switch capacitance, meeting the timing requirement called for in Eq. (3.4) guarantees switching with the minimum possible voltage stress for the given operating condition. Equation (3.5) can be used to develop a design equation determining an appropriate resonant inductor value that realizes ZVS at a desired operating point. This will be detailed in the section concerned with the design of L_r.

3.3.1 ZVS Active-Clamp Flyback Design Procedure

3.3.1.1 Select flyback transformer inductance

The presence of the active-clamp circuit does not significantly alter the primary switch current waveform from that of a seen in non active-clamp CCM flyback designs. Therefore, the usual methods of determining the appropriate value of magnetizing inductance can be used. Of course, the peak and RMS switch currents are heavily influenced by the amount of allowed inductor ripple current. This is usually expressed as

some percentage of the maximum average inductor current (occurring at maximum load and minimum line) so as to limit switch currents.

3.3.1.2 Select transformer turns ratio

The transformer turns ratio is chosen to accommodate as low a voltage rating for the switching devices as possible while still being able to realize a reasonable range of duty cycles over the input line range. Assuming that the active clamping provides for perfect voltage clamping across the primary switch (i.e., no overshoot), then the maximum off-state voltage appearing across S1 and S2 is given by:

$$V_{S1,S2}^{max} \approx V_{in}^{HL} + NV_o + \frac{2L_r F_S P_o^{max}}{\eta V_{in}^{HL} D^{HL}\left(1 - D^{HL}\right)}, \tag{3.6}$$

where D^{HL} denotes operation at the maximum input voltage.

The last part of the expression in Eq. (3.6) is the value of the voltage developed across L_r. Although an explicit value of the resonant inductor hasn't yet been determined, for the purposes of estimating the maximum voltage stress on S1 and S2 a value of $L_m/10$ can be used as a conservative design guideline. Also, as long as $L_m >> L_r$ the converter duty cycle behavior is approximately the same as for a non active-clamp flyback operating in CCM. With the addition of L_r the effective duty cycle (as defined by the charge and discharge cycle of the flyback inductor) is slightly less than switch S1's duty cycle (see Fig. 3.4):

$$D_{eff} = D_{S1} - \Delta D \cong D_{S1} - \frac{1}{D_{S1}} \frac{2L_r P_o F_S}{\left(V_{in} + NV_o\right) V_{in}}. \tag{3.7}$$

Eq. (3.7) is approximate in that it assumes lossless switching. For typical applications $\Delta D \approx 5$ % of D_{S1} so for the purposes of developing Eq. (3.6) and subsequent design equations it will be assumed $D = D_{eff} = D_{S1}$.

3.3.1.3 Design resonant inductor

After the value of L_m has been fixed the resonant inductor can be designed. As mentioned previously, it is assumed its value will be a small fraction of L_m. For a given converter operating point and value of C_r, achieving ZVS requires that L_r be of sufficient size to completely discharge the switch capacitance. At time instant T_4, from Eq. (3.5):

$$I_{S1,peak} = I_{Lm,peak} = I_{L_r,peak} \geq V_{C_r}\sqrt{\frac{C_r}{L_r}}, \tag{3.8}$$

where the peak primary switch current is

$$I_{S1,peak} \cong \frac{P_o}{\eta V_{in} D} + \frac{1}{2}\frac{V_{in} D}{L_m F_S}. \tag{3.9}$$

The difficulty in solving Eq. (3.8) for L_r is the fact that the resonant capacitor voltage (V_{Cr}) is a function of the value of L_r. However, in a practical design situation, the resonant inductor voltage at T_4 is relatively small (compared to $V_{in} + NV_o$) and Eq. (3.8) can be solved for an approximate minimum value of L_r necessary to achieve ZVS:

$$L_r\big|_{ZVS} \geq \frac{C_r\left(V_{in} + NV_o\right)^2}{I_{S1,peak}^2}. \tag{3.10}$$

It should be noted that in applications requiring high output voltage, it may be more desirable to specifically tailor the soft-switching characteristics of the output rectifier than to necessarily realize ZVS of the primary switch. In this case Eq. (3.3) may be the more important design criteria for the resonant inductor.

The RMS current carried by L_r can be estimated from Eq. (3.11):

$$I_{L_r,RMS} \approx \sqrt{\frac{\left(\frac{P_o}{\eta V_{in} D}\right)^2 (2D+1) + \frac{P_o}{\eta L_m F_S}(1-D) + \frac{1}{4}\left(\frac{V_{in} D}{L_m F_S}\right)^2}{3}}. \tag{3.11}$$

The expression for this current is complicated by the fact that the resonant inductor carries both primary switch and circulating clamp current.

3.3.1.4 Select auxiliary switch

For the purposes of estimating the required current rating of S2, advantage is taken of the assumption that the L_r-C_{clamp} resonant period is much longer than the off time of S1. Under this assumption the current through S2 (same as $i_{C_{clamp}}$) approximates a sawtooth waveform with endpoint currents equal to the peak current through S1 (see Fig. 3.4). The MOSFET body diode conducts clamp current for half the S2 on time with the MOSFET itself conducting current for the remaining half of the cycle. Therefore, the worst case maximum currents seen by both the MOSFET and its body diode are approximately:

S2 MOSFET:

$$I_{S2,RMS}^{max} \approx I_{S1,peak}^{max}\sqrt{\frac{1-D^{LL}}{6}}, \tag{3.12}$$

and

S2 body diode:

$$I_{S2,AVG}^{max} \approx I_{S1,peak}^{max}\frac{1-D^{LL}}{4}, \tag{3.13}$$

where D^{LL} denotes operation from the minimum line input. The peak primary switch current can be obtained from Eq. (3.9). It should be noted that as a practical matter it may be necessary to complicate the implementation of S2 by "defeating" its slow body diode by placing a diode in series with S2 and placing a fast recovery rectifier in parallel with the S2-diode series combination. This will prevent conduction of S2's body diode, necessary if a condition in the circuit ever occurred where S2's body diode was conducting when S1 is turned on. This could possibly occur, for example, during a line or load transient. Of course, the possibility of ZVS for S2 is lost using such a realization.

3.3.1.5 Select clamp capacitor

Choosing the value of clamp capacitance is done based on the design of L_r. The resonant frequency formed by the clamp capacitor and the resonant inductor should be sufficiently low so that there is not excessive resonant ringing across the power switch when the switch is turned off. However, using too large a value of clamp capacitance yields no improvement in clamping performance at the expense of a larger (more costly and bulky) capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and resonant inductance exceeds the maximum off time of S1. Therefore:

$$C_{clamp} >> \frac{(1-D^{HL})^2}{\pi^2 L_r F_S^2}. \quad (3.14)$$

The capacitor voltage rating has to exceed NV_o by the amount of voltage dropped across L_r:

$$V_{C_{clamp}}^{max} \approx NV_o + \frac{2L_r F_S P_o^{max}}{\eta V_{in}^{HL} D^{HL}\left(1-D^{HL}\right)}. \quad (3.15)$$

The required ripple current rating for the capacitor is:

$$I_{C_{clamp},RMS}^{max} \approx I_{S1,peak}^{max}\sqrt{\frac{1-D^{LL}}{3}}. \quad (3.16)$$

Equation (3.16) was derived using the same simplifying assumption used to derive Eqs. (3.12) and (3.13).

3.3.1.6 Choose output rectifier

The maximum theoretical reverse voltage seen by the output rectifier in the active-clamp flyback is the same as for a standard flyback design. However, the rectifier current is another matter. Due to the presence of the clamp circuit, the secondary current is "discontinuous" in shape even though the flyback inductor magnetizing current is

always positive and greater than zero. This is illustrated in Fig. 3.4. The result is much higher peak secondary currents than would normally be expected in a non active-clamp CCM flyback designs:

$$I_{D1,peak}^{max} \approx \frac{2P_o^{max}}{V_o(1-D^{LL})}. \tag{3.17}$$

The average rectifier current is just the load current. As was pointed out previously, the addition of L_r reduces the rate of diode turn-off di/dt. This improves rectifier switching losses and converter noise levels (see Figs. 3.7 through 3.9).

3.3.1.7 Select output capacitor(s)

The principle factor affecting the value of output capacitance is utilization of enough capacitance to meet device ripple current ratings:

$$I_{C_o,RMS}^{max} \approx \frac{P_o^{max}}{V_o}\sqrt{\frac{1+3\left(D^{LL}\right)}{3\left(1-D^{LL}\right)}}. \tag{3.18}$$

Theoretically, the capacitance value would be selected based on output voltage ripple specifications. However, in practice, meeting the RMS current rating called for in Eq. (3.18) sets a lower limit on an amount of capacitance that usually easily meets any ripple voltage specification.

3.3.1.8 Design flyback transformer:

Still constrained by the assumption that $L_r << L_m$, the transformer design for the active-clamp flyback is no different than that for a non active-clamp CCM flyback, except the primary and secondary RMS currents are somewhat different. The transformer secondary and output rectifier RMS currents are equivalent, so:

$$I_{sec,RMS}^{max} = I_{D1,RMS}^{max} \approx \frac{2P_o^{max}}{V_o\sqrt{3\left(1-D^{LL}\right)}}. \tag{3.19}$$

The transformer primary current is identical to the resonant inductor current, consequently its RMS value is given by Eq. (3.11).

3.4 Experimental Results

To experimentally characterize the soft-switching properties of the active-clamp flyback converter, a breadboard was constructed to the specifications listed below:

- input voltage: 100 Vdc
- output voltage: 48 Vdc
- output power: 500 W maximum
- switching frequency: 100 kHz

Using the design procedure discussed in the previous section as a guide, the experimental converter was constructed using the following components:

- Transformer:

  core: Toshiba PC40ETD49-Z

primary: 45T of 3 strands of 150/42 Litz wire

secondary: 15T of 5 strands of 150/42 Litz wire

L_m: 215 μH, L_{leak} (referred to primary): 2.3 μH

- Resonant inductor:

  core: MPP 55530

  winding: 8T of 10 strands of AWG 26

  L_r: 7 μH (measured with no DC bias)

- Clamp circuit:

  C_{clamp}: 2.2 μF, 250 V

  S2: IRFP360

- S1: IRFP360

- Output stage:

  D1: 2 x BYV44-500

  C_o: 3 x 2200 μF, 100 V Aluminum electrolytic

For the experimental circuit ZVS was realized above 145 W. Fig. 3.5 compares experimental efficiencies using an RCD clamp with no resonant inductor and the active-clamp circuit with L_r = 7 μH (all other circuit parameters are identical). It can be seen that the active-clamp circuit yields an improvement of at least 4% in power stage efficiency. Maximum output power for the RCD clamped power stage is about 250 W due to power dissipation limitations in the clamp resistor.

Figures 3.6 and 3.7 are experimental waveforms pertinent to illustrating the converter's soft-switching characteristics. Figure 3.6 displays S1's gate drive voltage, the

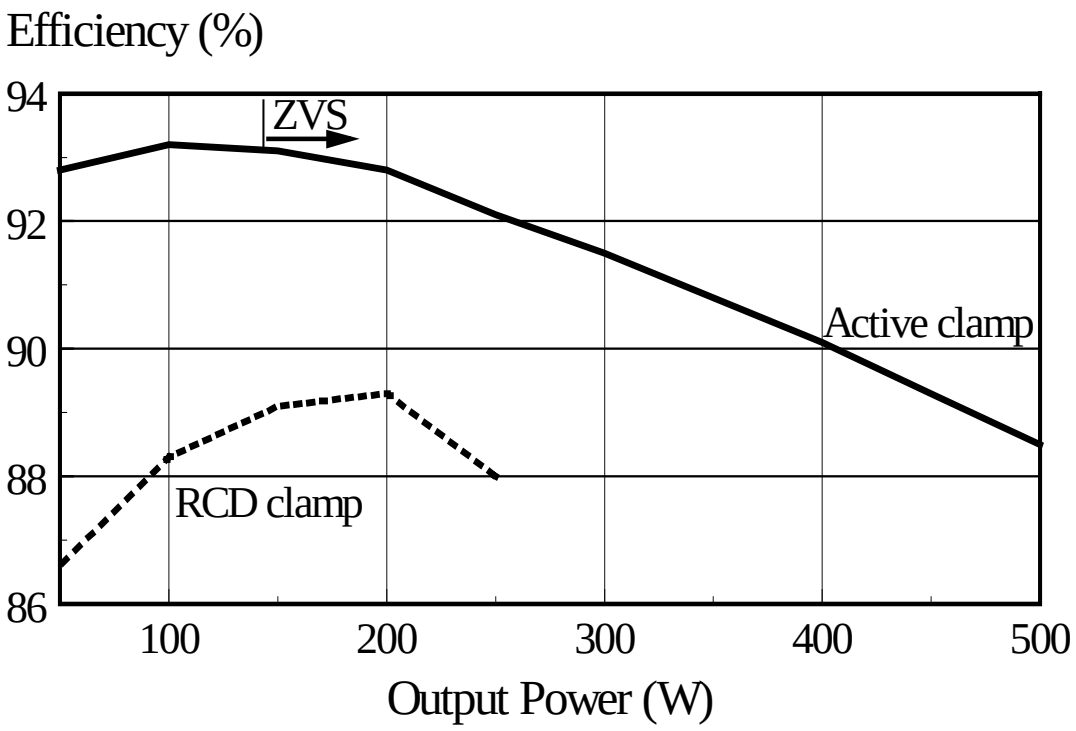


Fig. 3.5 Efficiency comparison between RCD and active-clamp configurations. For RCD clamp, R = 4.7 KΩ, 10 W and C = 2.2 μF.

resonant inductor current, and S1's drain-to-source voltage. Operation is at P_O = 300 W. Figure 3.7 compares the output rectifier current with and without L_r in the circuit. The operating point of the converter is identical for both cases (P_O = 300 W, ZVS with L_r, hard switching without it). As can be seen from the figure, with the resonant inductor the rectifier reverse recovery current characteristic is substantially improved. Not only is switching loss in the diode decreased, but the output voltage high-frequency (HF) noise is reduced. This is illustrated in Figs. 3.8 and 3.9 which show the output voltage noise spectrum with and without L_r. In particular, the noise levels in the frequency range of about 2.5 to 3 MHz show a reduction of nearly 20 dB between the two cases. Coincidentally, HF noise in the range of about 2 to 5 MHz is typically very difficult to filter because the frequency is somewhat low for effective use of ferrite beads and is too high for standard capacitive bypassing.

Another attractive usage for the active-clamp circuit is as a low-loss turn-off snubber when using an IGBT as the primary switch device (S1). IGBTs have superior conduction characteristics compared to MOSFETs (of the same voltage rating). The drawback to the use of IGBTs is that they display excessive turn-off losses as their switching frequency is increased. The severity of this problem can be reduced by adding an external capacitor (C_r) from the collector to the emitter of the IGBT to slow down the rate of increase in collector voltage as the device turns off. This allows time for the device current to tail to zero without excessive device voltage being present. Subsequently, before S1 is turned on, the resonant inductor discharges C_r so that its stored energy is not dissipated in the IGBT at device turn on.

Experimental results comparing power stage efficiencies using an IGBT with and without external capacitance is shown in Fig. 3.10. With C_r = 3000 pF the efficiency is improved by about 1% over most of the load range. Also, for comparison purposes, efficiencies for a single and dual 600 V MOSFETs are plotted. As can be seen, at P_O = 400 W circuit efficiency using a single IGBT is equal to the efficiency obtained using *two* MOSFETs.

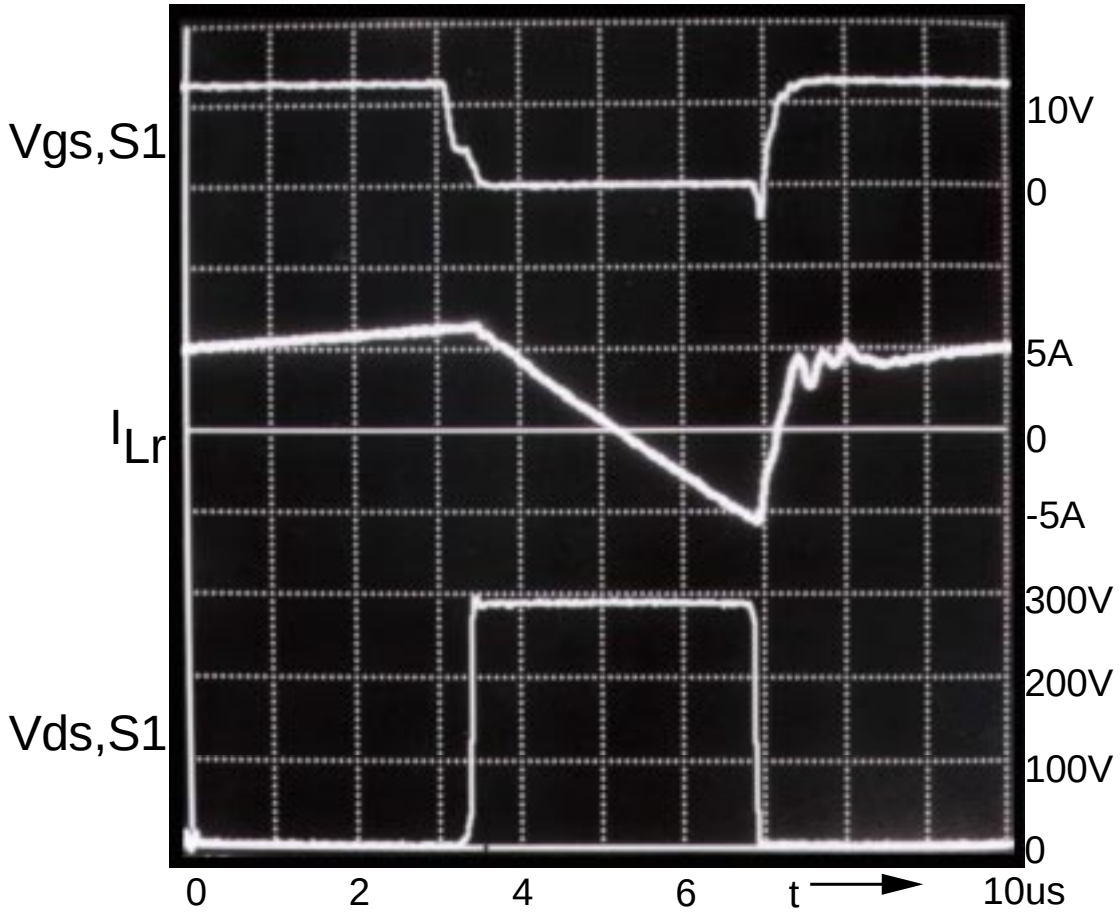


Fig. 3.6 ZVS active-clamp flyback experimental waveforms.

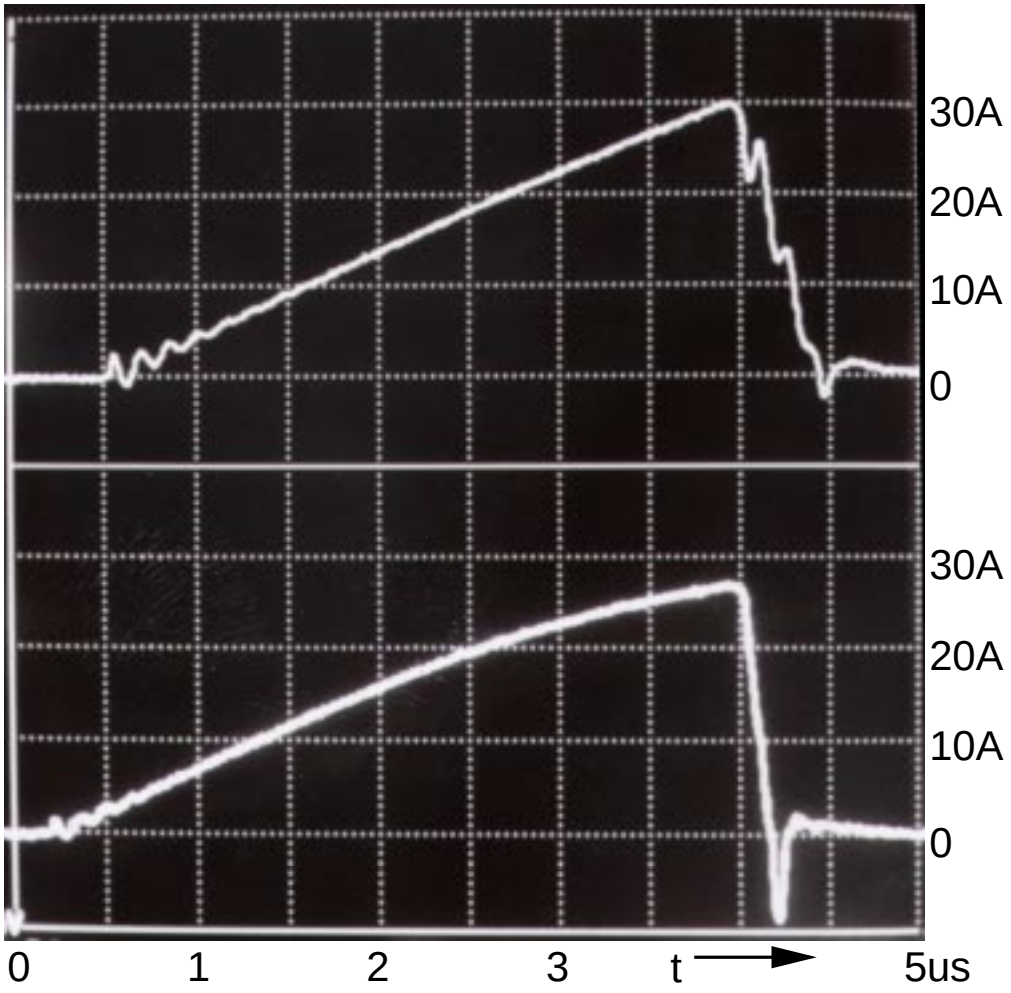


Fig. 3.7 Output rectifier current waveforms. Top trace: L_r = 7 μH; bottom trace: $L_r = L_{leak} \approx 2$ μH.

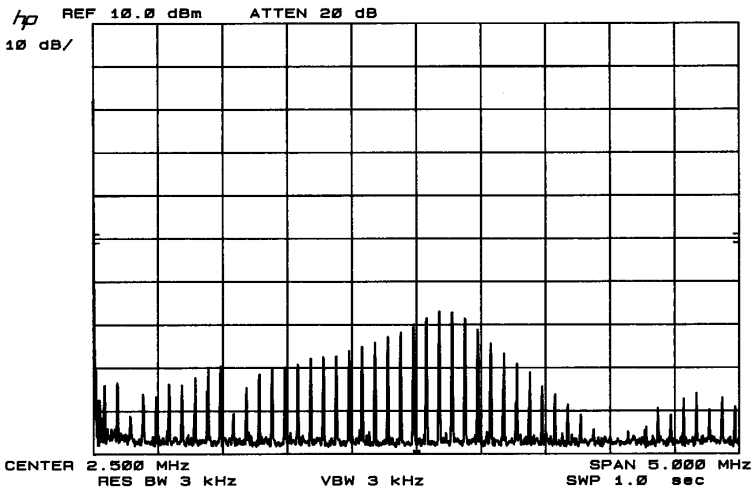


Fig. 3.8 Output voltage noise, $L_r = L_{leak}$.

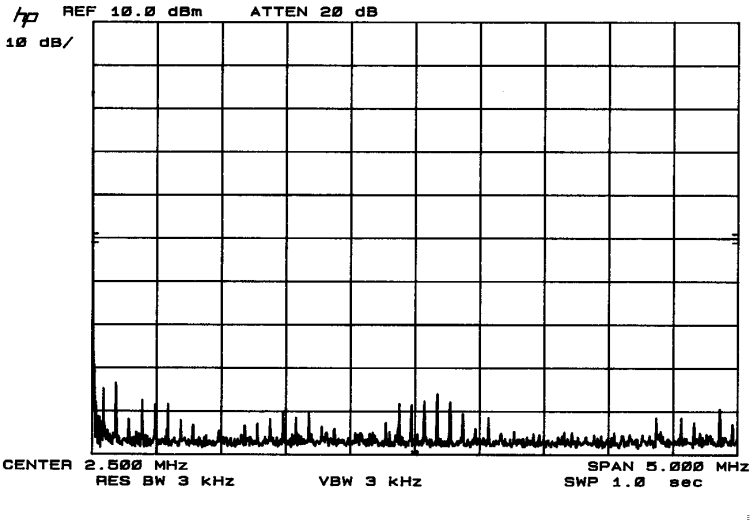


Fig. 3.9 Output voltage noise, $L_r = 7\ \mu H$.

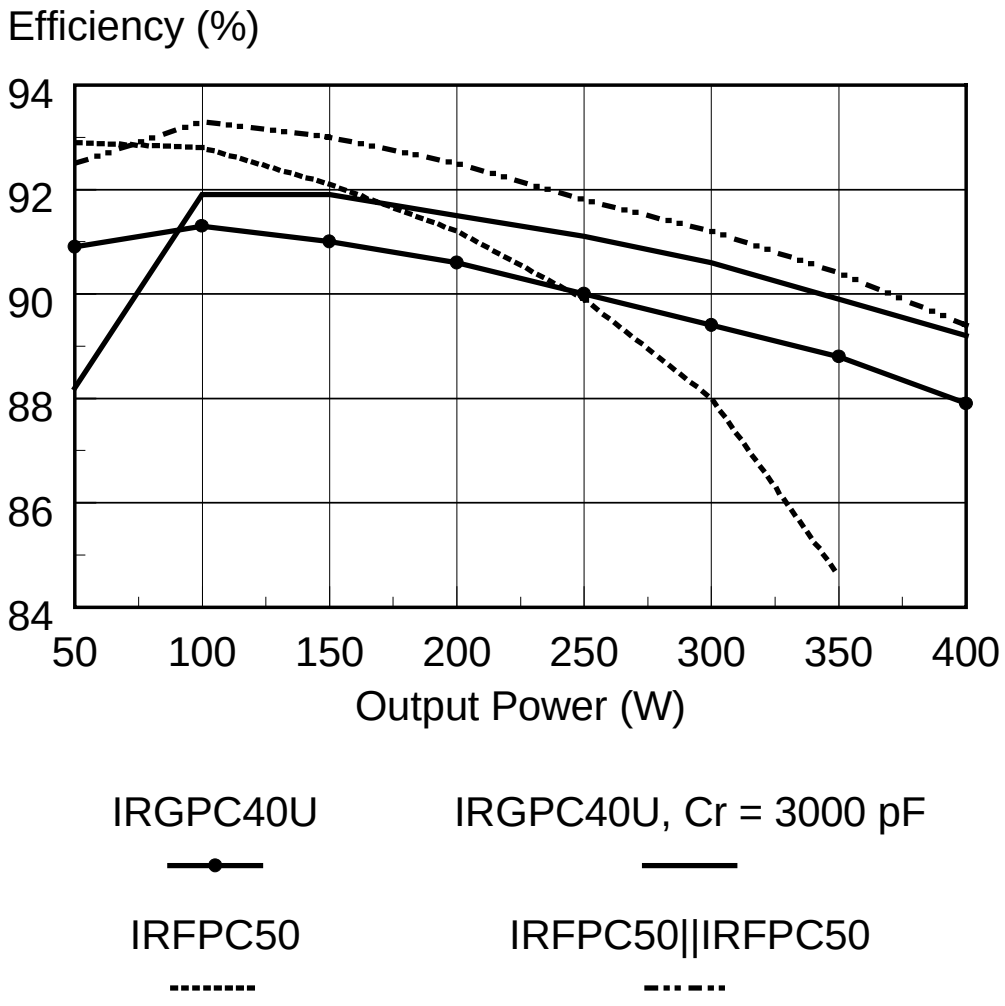


Fig. 3.10 Efficiency comparison using the active-clamp network with various switch configurations. F_S = 100 kHz.

3.5 Active-Clamp Flyback for PFC Applications

The following sections evaluate the soft-switched active-clamp flyback converter developed above as a PFC front-end converter, as was discussed in the introduction to this chapter. Experimental results for both single power stage (to 500 W) and interleaved power stage (to 600 W total) designs are presented. Flyback interleaving significantly reduces input filter requirements over single power stage designs by introducing 180° out of phase input current harmonics, resulting in a reduction of input current ripple. A solution to the hold-up problem is also presented and experimentally verified.

The active-clamp flyback offers essentially the same advantages in PFC applications as it does in DC/DC conversion applications. Because relatively high output power levels are still desired, "CCM" (unidirectional magnetizing current) operation, as described in the previous sections is required. This somewhat complicates the control strategy to realize power factor correction, when compared with the DCM operation, which can obtain good power factor with simple duty cycle control [20]. However, the method of charge control [16, 48] can be applied to CCM operation, resulting in excellent power factor at the expensive of adding a slightly more complicated control scheme. Figure 3.11 shows a block diagram and the basic waveforms pertinent to charge control. This PFC control method forces the input charge to follow an input line replica reference pulse-by-pulse, resulting in a sinusoidal input current waveform. The switching frequency is constant, and (because of the integrating capacitor) the control scheme offers good immunity from switching noise.

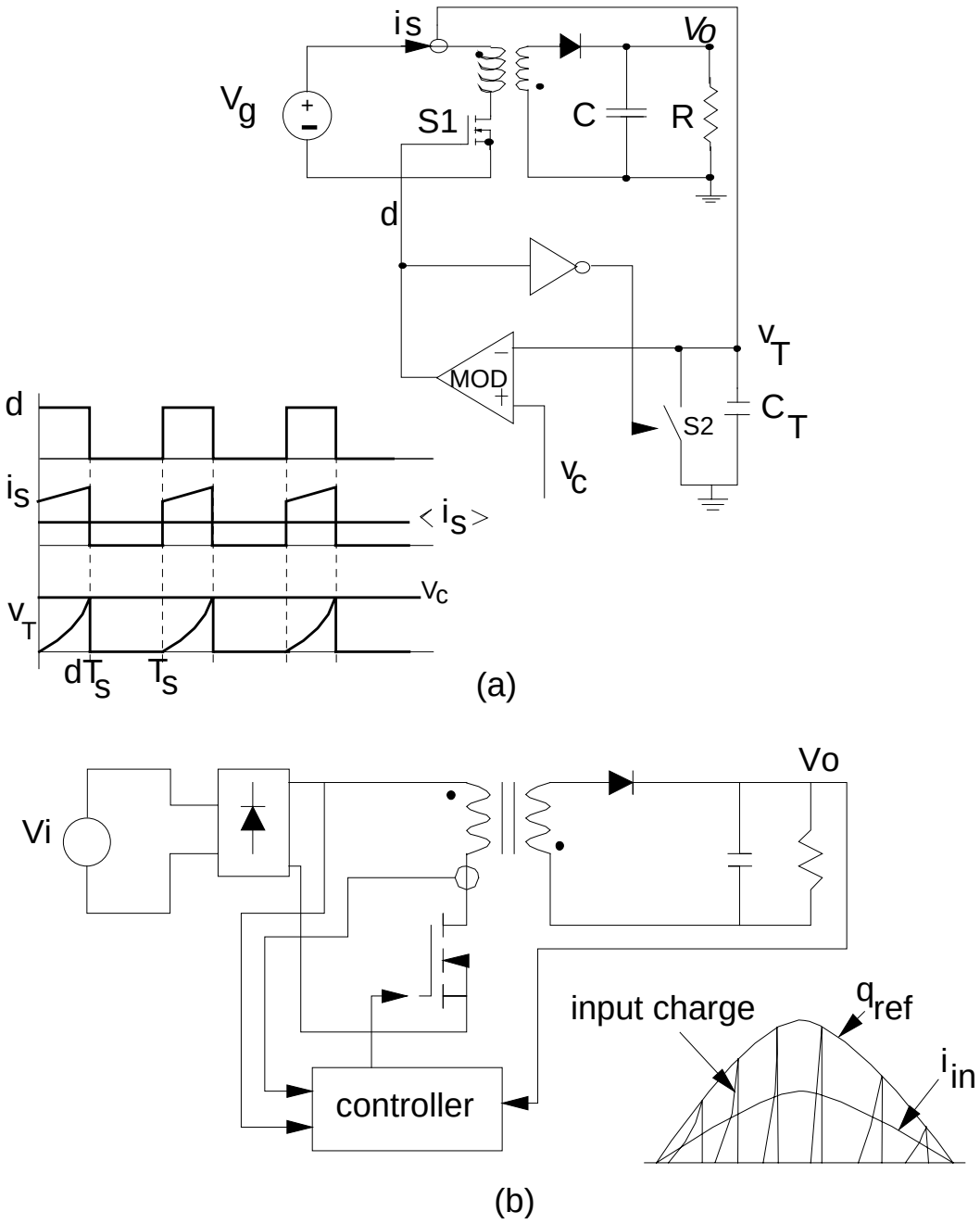


Fig. 3.11 Charge control method: (a) Switching frequency waveforms; (b) Line frequency waveforms.

3.6 500 W PFC Active-Clamp Flyback Stage Design

3.6.1 PFC specifications

To determine the feasibility of using the active clamp flyback in PFC applications, a single-stage converter operating at 70 kHz was built to the following input/output specifications:

- input: 90 - 270 V rms (Universal Line);
- output: 48 Vdc nominal; and
- output power: 500 W maximum.

3.6.2 Primary switch selection

3.6.2.1 Transformer turns ratio selection

The transformer turns ratio is selected to accommodate as low a voltage-rated device as possible while still being able to realize reasonable values for the range of minimum duty cycles. Assuming initially that the active clamping provides for perfect suppression of the leakage spike appearing across the main switch (i.e., no overshoot), then the maximum off-state voltage appearing across S1 is given by Eq. (3.6).

The range of the minimum duty cycle is given by:

$$D_{min}^{LL} = \frac{V_o}{V_o + \frac{\sqrt{2}V_{rms}^{LL}}{N}}, \tag{3.20}$$

and

$$D_{min}^{HL} = \frac{V_o}{V_o + \frac{\sqrt{2}V_{rms}^{HL}}{N}}. \tag{3.21}$$

For the 500 W design the turns ratio was selected to be 3, which resulted in a peak voltage stress of 526 V for S1. Therefore, a 600 V device can be used. The minimum duty cycle ranges from 0.53 at minimum line to 0.27 at high line.

3.6.2.2 Calculating primary switch currents

The maximum average current seen by S1 over one switching cycle occurs at maximum load and minimum line voltage (assuming approximately unity power factor) and is given by:

$$I_{S1,avg}^{max} = \frac{P_o^{FL}\sqrt{2}}{\eta V_{rms}^{LL}}, \tag{3.22}$$

where η is the converter efficiency at the maximum output power, minimum line operating condition. Assuming an efficiency of 85% at full load and minimum line, the maximum average switch current is 9.2 A. The worst case maximum peak switch current also occurs under the same operating conditions as above and is calculated from:

$$I_{S1,peak}^{max} = \frac{P_o^{FL}\sqrt{2}}{\eta D_{min}^{LL} V_{rms}^{LL}} + \frac{D_{min}^{LL} V_{rms}^{LL}\sqrt{2}}{2 L_m F_S}, \tag{3.23}$$

where L_m is the flyback transformer magnetizing inductance and F_S is the switching frequency. For this particular design, with a 20% peak-to-peak ripple current at low line, full load, $L_m \cong 220\ \mu H$. Assuming $\eta = 0.85$, the resulting peak switch current is about 19.6 A.

These calculated switch currents preclude using a single MOSFET for S1. The alternatives are to parallel MOSFETs, use the active-clamp network as a low-loss turn-off snubber for an IGBT (as discussed Section 3.4) or parallel IGBTs and MOSFETs to form a mixed device switch.

3.6.2.3 Device paralleling

The limiting factor in being able to switch an IGBT at higher frequencies is the presence of a collector current tail at device turn off, resulting in excessive switching losses. As shown in Fig. 3.12, the paralleling of a MOSFET with an IGBT, acting as a single switch, enables the IGBT to be turned off without the simultaneous presence of high collector voltage and current [47]. The MOSFET is left on for a sufficient length of time after the IGBT has been turned off (about 750 ns in the case of the IGBT selected for use in this circuit) to allow the collector current to reach zero before the collector voltage is allowed to rise. Because the on-state voltage drop of the IGBT is typically lower than for the MOSFET, the strengths of both types of switches are taken advantage of in this type of arrangement. Fig. 3.13 displays the dc/dc conversion efficiencies for a dual MOSFET switch (IRFPC40), a single IGBT switch (IRGPC40U), and the mixed device switch as a function of output power. All measurements were made at 90 VDC input to approximate the worst-case AC low-line operating condition.

3.6.3 Clamp circuit design

3.6.3.1 Auxiliary switch selection

The selection procedure for the auxiliary switch is essentially the same as outlined in Section 3.3.1.4. However, in this PFC application, device power dissipation is modulated at a frequency of 120 Hz. Therefore, the junction-to-case thermal time constant of the devices will determine how closely the use of Eqs. (3.9), (3.12), and (3.13) in calculating power dissipations approximates the actual steady-state power dissipation condition.

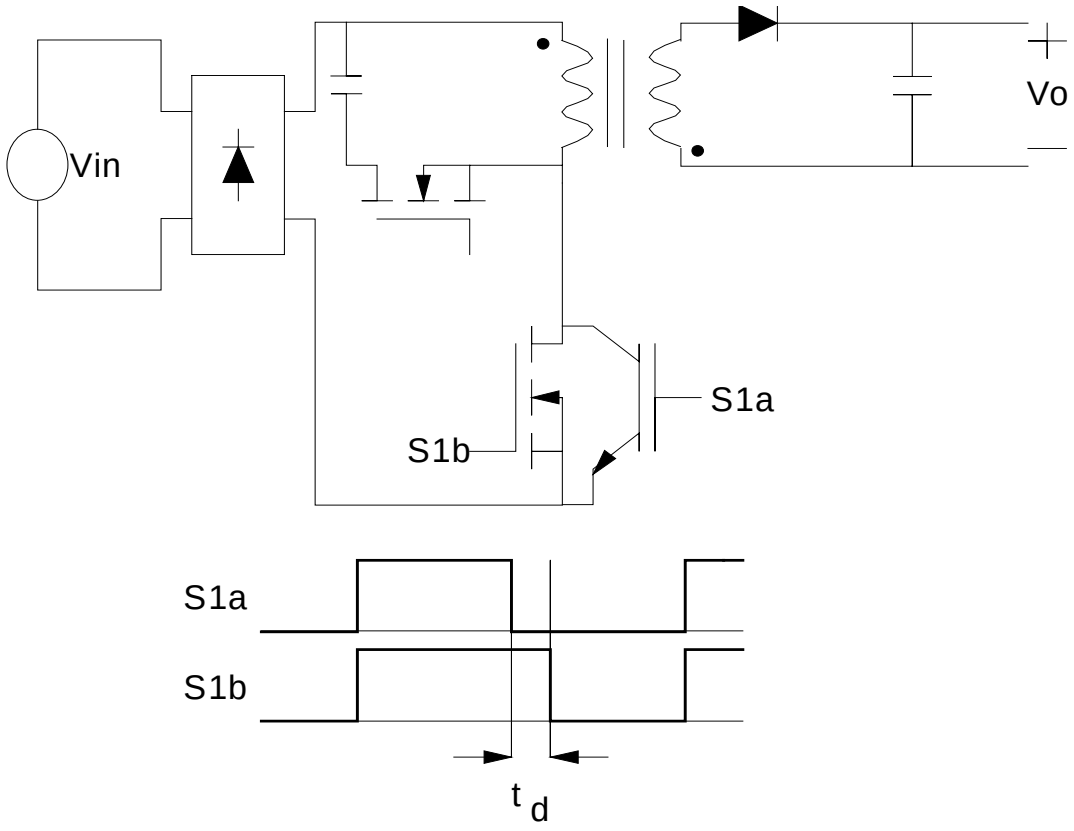


Fig. 3.12 Basic concept of mixed power devices.

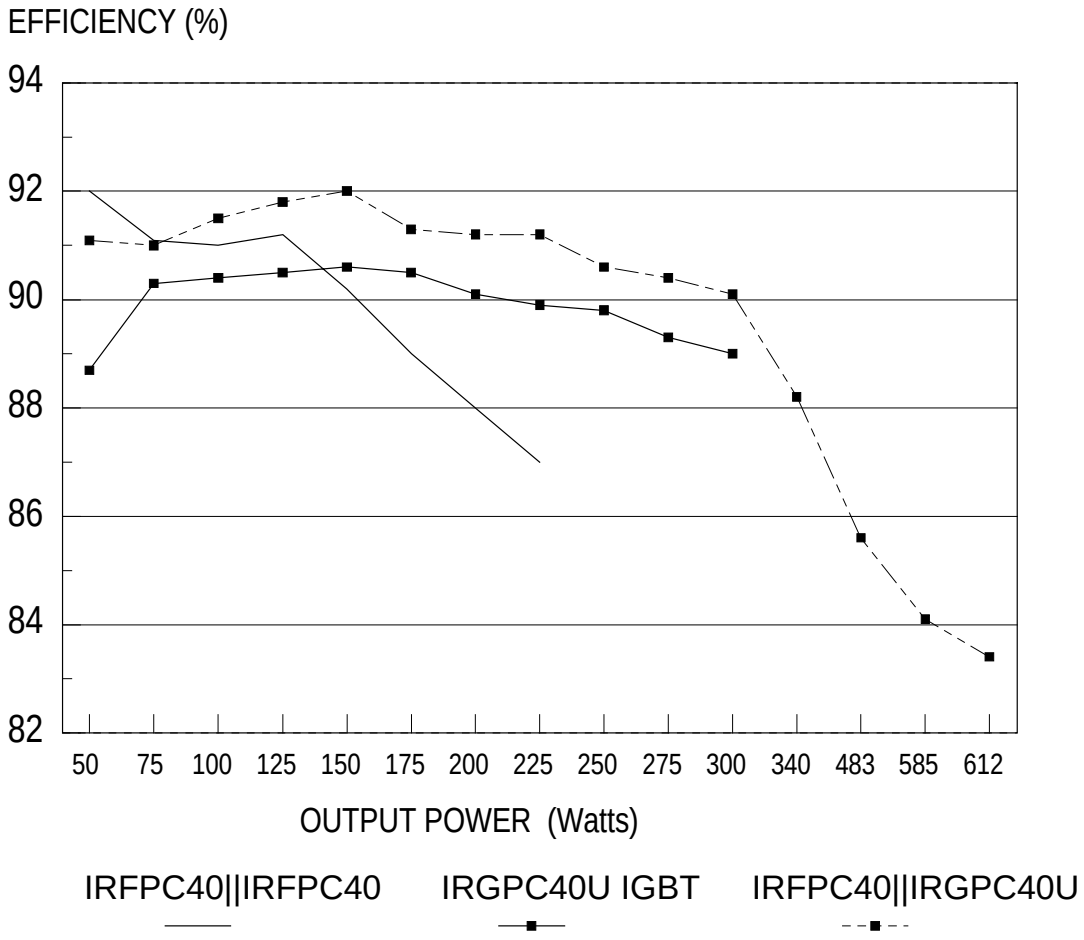


Fig. 3.13 Experimental active clamp flyback dc/dc efficiencies. Vin = 90 VDC and F_S = 90 kHz for all three curves.

3.6.3.2 Clamp capacitor selection

Selection of the clamp capacitor value closely follows that which was outlined in Section 3.3.1.5. With the transformer leakage inductance measuring out at about 4 μH, the calculated value of clamp capacitance is 2.8 μF (with the switching frequency at 70 kHz). After breadboard experimentation a value of 2 μF was settled on (values between 0.47 μF and 2 μF yielded good results). The capacitor voltage rating has to exceed NV_o, which is approximately 150 V in this design. Therefore, a 250 V part is used to provide some margin. The required 120 Hz ripple current rating for the capacitor is:

$$I_{Cclamp,rms}^{max} \approx \frac{P_o^{max}}{\eta N V_o} \sqrt{\frac{2\sqrt{2} N V_o}{3\pi V_{rms}^{LL}} + \frac{3}{8}}. \tag{3.24}$$

This gives about 3.8 A rms for this design.

3.6.4 Transformer design

The transformer design for the active clamp flyback is no different than that for a traditional flyback, except that for PFC applications, the peak switch current is larger than for DC/DC applications (assuming $V_{in,dc/dc} = V_{in,rms,PFC}$).

For the 500 W design, a Toshiba PC40ETD49-Z core was selected and wound with 45 primary turns of 3 strands of 150/42 Litz wire. The secondary consisted of 15 turns of 5 strands of 150/42 Litz wire. The primary and secondary windings were interleaved and the core was gapped to obtain a magnetizing inductance of about 220 μH. For the purposes of selecting wire size, the maximum primary and secondary (120 Hz) RMS currents are:

$$I_{pri,rms}^{max} \approx \frac{P_o^{max}}{\eta N V_o V_{rms}^{LL}} \sqrt{\frac{10\sqrt{2} N V_o V_{rms}^{LL}}{3\pi} + (N V_o)^2 + \frac{3}{8}(V_{rms}^{LL})^2}\,, \tag{3.25}$$

and

$$I_{sec,rms}^{max} \approx \frac{P_o^{max}}{V_o} \sqrt{\frac{3}{2} + \frac{16 N V_o}{3\pi\sqrt{2} V_{rms}^{LL}}}\,. \tag{3.26}$$

In this design the maximum primary and secondary currents are about 9.4 A rms and 19.3 A rms, respectively.

3.6.5 Output stage design

3.6.5.1 Output rectifier selection:

The maximum theoretical reverse voltage seen by the output rectifier is given by:

$$V_{D1,max} = \frac{\sqrt{2} V_{rms}^{HL}}{N} + V_o \tag{3.27}$$

which is 175 V in this case. For design margin, a 300 V part can be used. The maximum average current (averaged over one switching cycle) through the output rectifier is:

$$I_{D1,avg}^{LL,FL} = \frac{2 P_o}{V_o} \tag{3.28}$$

This calculates to about 20.8 A for the 500 W design. As explained in Section 3.3.1.6 , because of the operation of the clamp circuit, the rectifier current appears "discontinuous" even though the flyback inductor operating with unidirectional current. As a result, peak secondary currents are quite high:

$$I_{D1,peak}^{max} \approx \frac{4P_o}{(1 - D_{min}^{LL})V_o} \tag{3.29}$$

The worst case value in this design example is about 89 A. Because of the quasi-resonant nature of the current through the rectifier the peak won't be quite this high, but it is much greater than the peak rectifier currents seen in a non active-clamp flyback operating in CCM.

3.6.5.2 Output capacitor selection:

The principle factor affecting the selection of the output capacitor is the output voltage ripple specification. C_O is selected to achieve some maximum 120 Hz voltage ripple:

$$C_o = \frac{P_o^{max}}{240\pi V_o V_{or}}, \tag{3.30}$$

where V_{or} is the maximum specified peak output voltage ripple. For a 6 V pp ripple, C_o ≅ 4700 pF. The required 120 Hz ripple current rating for the output capacitor is given by:

$$I_{C_o,rms}^{max} = \frac{P_o^{max}}{\sqrt{2}V_o}. \tag{3.31}$$

This gives a 120 Hz ripple current component of 7.4 A rms for a 500 W, 48 V output.

3.6.6 Experimental Results

Figure 3.14 graphs the efficiency vs. output power of the single stage active clamp PFC flyback at the minimum input line (90 V rms). This is the worst-case operating condition with respect to efficiency. The power switch consists of an IRFPC50 MOSFET in parallel with an IRFGPC40U IGBT. The efficiency remains above 83.5% up to 500 W but falls fairly rapidly between 500 W and 550 W. The major loss at the high end of output power is transformer copper loss. The efficiency could be improved through a more careful design of the transformer.

Figure 3.15 shows experimental waveforms of the line current and rectified line voltage at 550 W. The power factor remained above 0.98 over the full load range (to 550 W).

3.7 Interleaved Active-Clamp Flyback PFC [49, 50]

One of the limitations of the flyback converter is the discontinuous nature of the input current which results in a large sized EMI filter (when compared to a topology offering continuous input current operating at similar power levels). To minimize this problem, an interleaved active clamp flyback PFC configuration has been tested up to a 600 W output. The circuit design is similar to that of the single-stage flyback PFC circuit, and differs from the interleaved active-clamp flyback circuit described in [41] by the difference in behavior of the transformer magnetizing current. In [41] inductor ripple

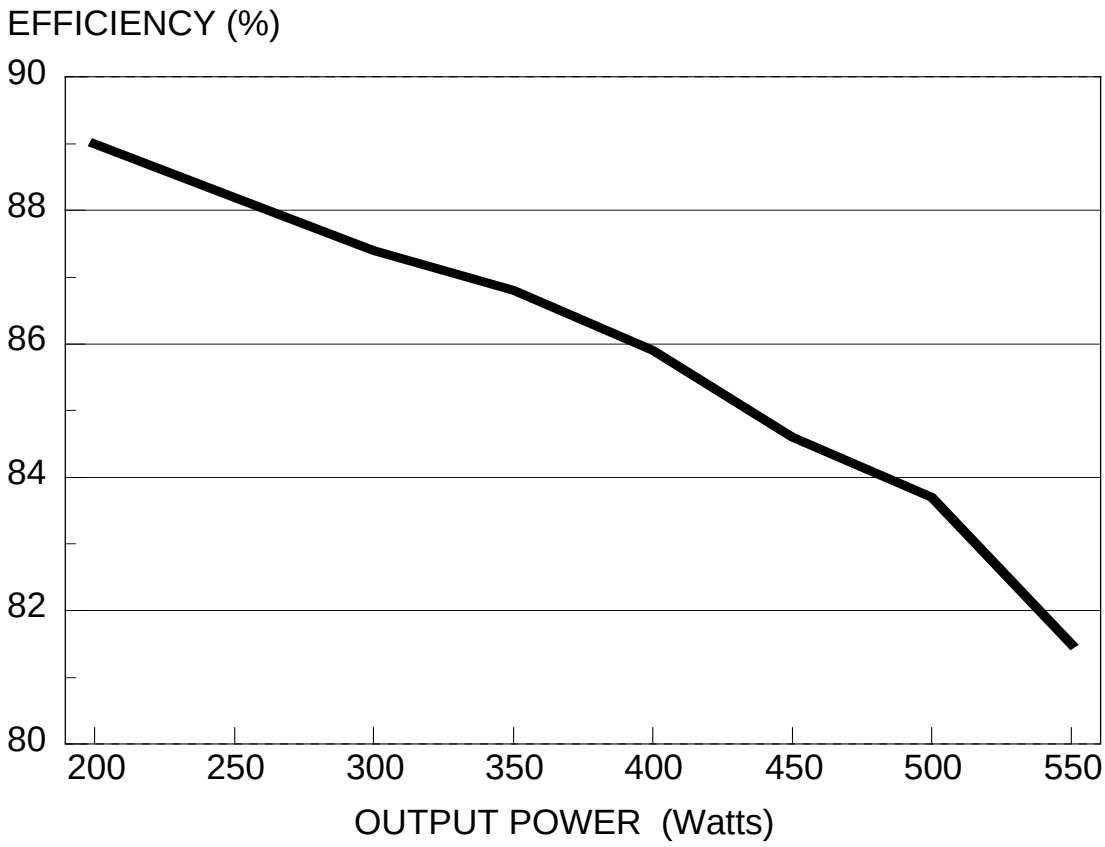


Fig. 3.14 Active clamp flyback PFC efficiency, Vin = 90 V rms.

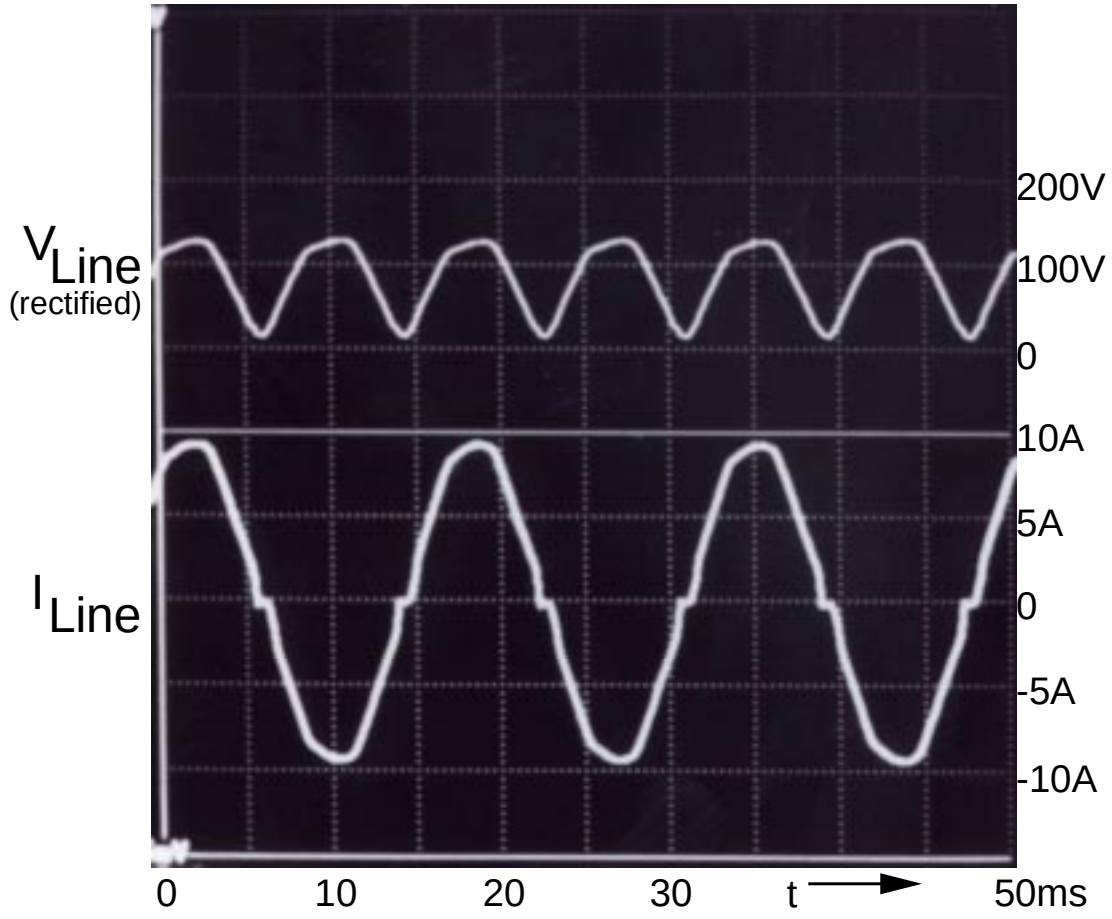


Fig. 3.15 Active clamp flyback experimental waveforms. P_o = 550 W.

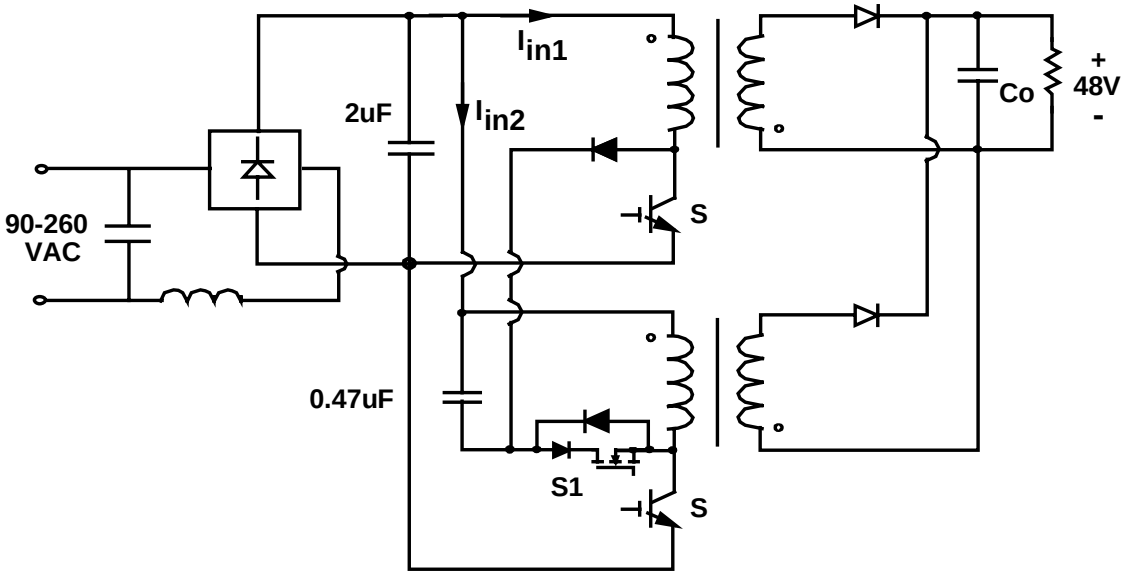
current is deliberately increased to always yield a portion of the switching cycle where the magnetizing current has reversed direction (become negative). This is the method by which soft-switching is achieved in [41]. In the present case, we want to minimize the ripple current to increase efficiency at higher power levels. In the present design the magnetizing current does not go negative (except possibly near the zero crossing points in the input line) - a consequence of reduced ripple current.

3.7.1 Power stage design

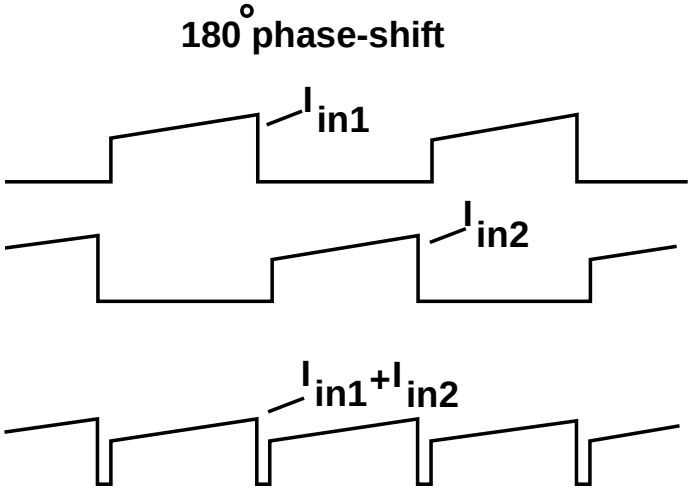
Figure 3.16 shows the circuit diagram of the interleaved flyback PFC power stage. The clamp circuit uses only one active clamp switch and one diode. The leakage energy from both transformers is stored in the clamp capacitor and is returned to the load through the lower transformer only. This approach simplifies the circuit design and reduces cost. Each power transformer is built using a Philips ETD44-3F3 core with 47 primary turns (80/37 Litz wire) and 18 secondary turns (2 paralleled 80/37 Litz wires).

3.7.2 Experimental results

The 70 kHz switching frequency was selected to limit the fundamental ripple frequency to 140 kHz and take advantage of the step change in the VDE EMI specification at 150 kHz. Lowering the switching frequency would provide higher efficiency, but the input filter size would correspondingly increase. Figure 3.17 shows the efficiency as a function of line voltage with a 600 W output and for comparison purposes, the efficiency of a two-stage design consisting of a boost PFC followed by an active-clamp forward converter. A schematic of the two-stage design is shown in [50]. As can be seen from the figure, the interleaved approach yields increased efficiency over almost the entire line range.



(a) Power stage design.



(b) Input current with 180° ϕ-shift of individual power stage switch timing.

Fig. 3.16 Interleaved active clamp flyback PFC.

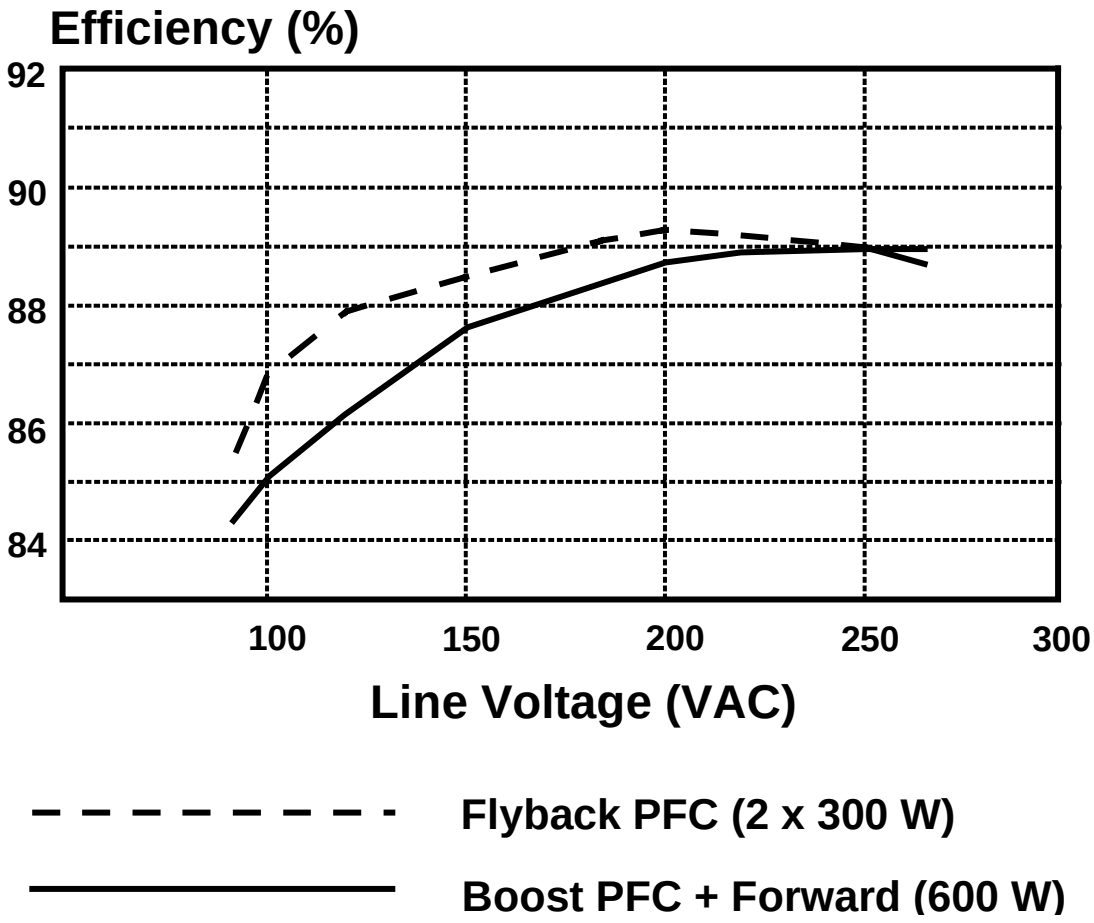


Fig. 3.17 Efficiency of the interleaved active clamp flyback PFC as a function of input voltage (P_o = 600 W) [50].

3.7.3 Hold-up circuit design

One disadvantage of the single-stage flyback topology compared to a conventional two-stage front-end for a power distribution system is that it does not have inherent hold-up capability. To provide for a reasonable hold-up period after the loss of line voltage, a secondary-side hold-up capacitor would have to be very large. Figure 3.18 shows a simple method of providing a specified hold-up time by storing the required hold-up energy in the 470 μF capacitor located on the primary side. This capacitor is trickle charged through the 47 K resistor and a diode connected to the drain of the primary switch, S1.

During normal operation, the line voltage is sensed using R1 and the bridge rectifier, resulting in Q1 being on. When the line voltage disappears (requiring the hold-up function to be enabled), Q1 turns off after a short delay, activating the optoisolator. This turns on switch Sa, which connects the energy-storage capacitor to the input of the flyback converter. Figure 3.19 shows hold-up operation with the primary side hold-up circuit. It can be seen that practically all of the energy stored in the hold-up capacitor is utilized. For a primary side capacitor value of 470 μF, the resulting hold-up time is about 24 ms.

3.8 Summary

This chapter has presented analysis, design, and experimental results of a soft-switched active-clamp flyback topology suitable for utilization as an isolated front-end PFC conversion stage in computer system distributed power architectures. The converter's operating characteristics were analytically determined. Performance was experimentally verified for both a 500 W single-stage and a 600 W interleaved designs. These results demonstrated that the active clamp variation of the traditional flyback topology offers an attractive alternative to the more usual two-stage approach (boost cascaded by a buck) to off-line power conditioning for distributed power systems.

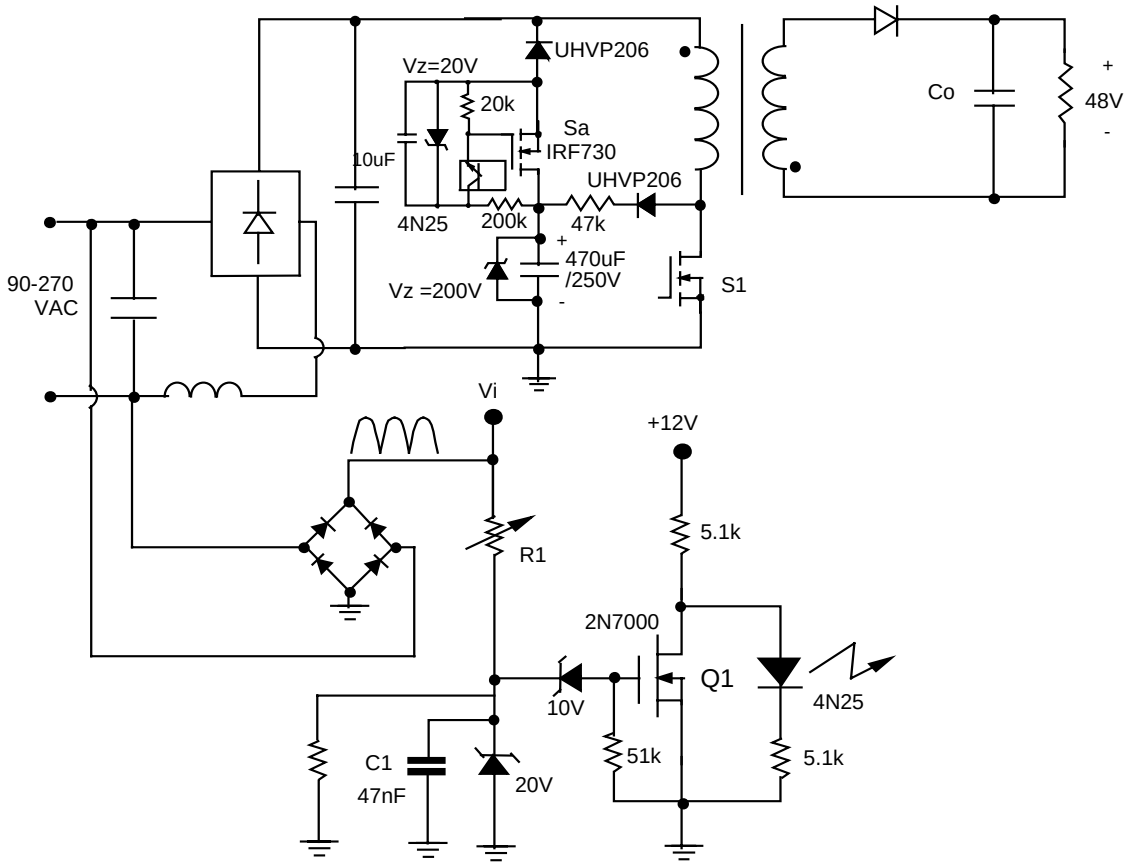


Fig. 3.18 Flyback converter circuit diagram with primary side hold-up.

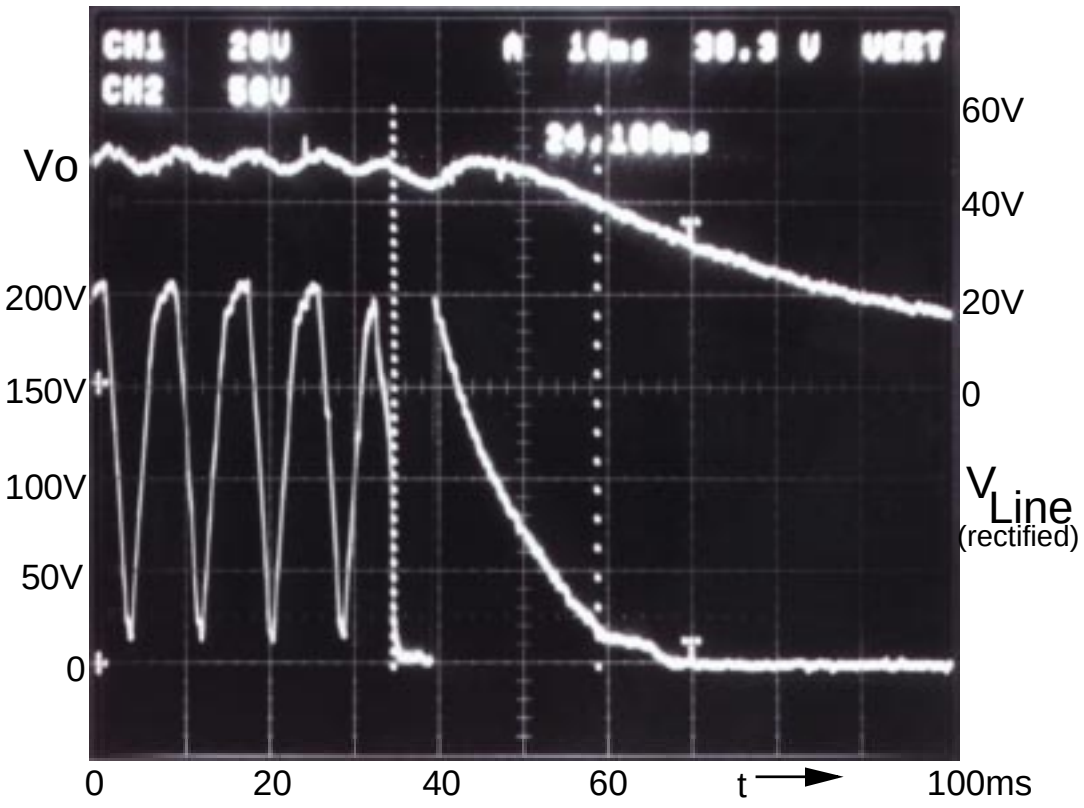


Fig. 3.19 Hold up operation of the flyback PFC converter.