# Shiladitya Biswas

### **Indian Institute of Technology Madras**

529, Pampa Hostel, IIT Madras

### Education

Program	Institution
M.Tech. (CSE) - <b>2019</b>	IIT Madras
B.E. (CSE) - <b>2014</b>	IIEST, Shibpur

## **Industry Experience**

**Ericsson India Global Services Pvt. Ltd.** – Solution Integrator (2015 - 2017)

- Worked on Ericsson's Telecommunication Billing and Charging Systems.
- Worked on projects with customers like AMX, TSTT, Entel Chile/Peru and Saudi Telecom.
- My work included Billing infrastructure setup like Environment Creation/Restoration, DMF execution, Authentication, Database Creation, Cloning, Data pumping etc.
- Developed various types of report generation scripts for Ericssons New Generation Voucher Servers.

## **Academic Projects**

## 1. Analysis and Application of the Dynamic Orienteering Problem

Jan 2018 - Present

M.Tech. Project – (Guide: NS Narayanaswamy)

IIT Madras

**Skills Used:** Approximation Algorithms, Heuristic Algorithms, C++, PHP, Perl

- Orienteering is an optimization problem in routing where the aim is to find a route constrained by a distance budget that visits the maximum number of vertices.
- The problem models many important sub-goals in vehicle routing problems.
- In this work our aim is to study the algorithmic issues in a dynamic setting where the routes have to be updated in the presence of dynamic cost changes in the network.

### 2. Designing a scalable Cache Simulator supporting multiple cores

Feb 2018

Course Project – (Parallel Computer Architecture)

IIT Madras

**Skills Used:** C++, Intel PIN Tool, Cache Memory Internal Structure

- An object oriented cache simulator was designed with scalability and modularity in mind.
- Each entity in cache architecture was an object with abstraction of its functionalities.
- Intel PIN Tool was used to generate memory trace from an application to test the simulator.

#### 3. Simulating Relay Race between threads

Nov 2017

Course Project – (Computer Architecture)

IIT Madras

**Skills Used:** C, pThreads

• Relay Race among 4 different threads and 1 referee thread was simulated using atomic (mutex) locks, barriers and other synchronisation techniques.

### 4. Cell Selection Scheme For Densely Deployed Femto BS and Wi-fi APs

Aug 2017 - Nov 2017

Course Project – (Wireless Communication Networks)

IIT Madras

Skills Used: Java, Eclipse IDE

- Selected the potentially best femtocell based on an empirical calculation of expected bitrate obtained from signal to noise plus interference ratio of various femtocells.
- Looked at the possibility of obtaining unlicensed spectrum based on expected blank frame transmissions of wifi.

### **Course Work**

- **Theory**: Advanced Data Structures and Algorithms, Logic and Combinatorics for Computer Science, Topics in Design and Analysis of Algorithms
- o Systems: Computer Architecture, Parallel Computer Architecture, Digital Systems Testing, Operating Systems

o Miscellaneous: Advanced Programming Lab, Wireless Communication Networks, Ontology

## **Technical Skills**

- Programming Languages/Technologies: C, C++, Oracle, Perl, SQL, Ontology Languages
- HPC: POSIX Threads, OpenMP, AVX, AVX2 Tools/Simulators: Intel MLC, Gem5, Protege

## **Achievements**

- o Named as STAR TA by Department of Computer Science & Engineering, IIT Madras (Nov. 2017)
- Named as one of the most high-performing employees in Ericsson (April, 2016)
- Won the ROCKSTAR Award in Ericsson (Nov, 2015)

## **Teaching Experience**

- o Teaching Assistant: CS2200 Languages, Machines and Computations (Spring, 2019)
- Teaching Assistant: CS5800 Advanced Data Structures and Algorithms (Fall, 2018)
- Project Assistant: Centre for Computational Brain Research (CCBR) (Spring, 2018)
- o Teaching Assistant: CS1100 Computational Engineering (Fall, 2017)