Simulation of 4H-SiC MESFET for High Power and High Frequency Response

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Abstract—**In this paper, we report an analytical modeling and 2-D Synopsys Sentaurus TCAD simulation of ion implanted silicon carbide MESFETs. The model has been developed to obtain the threshold voltage, drain-source current, intrinsic parameters such as, gate capacitance, drain-source resistance and transconductance considering different fabrication parameters such as ion dose, ion energy, ion range and annealing effect parameters. The model is useful in determining the ion implantation fabrication parameters from the optimization of the active implanted channel thickness for different ion doses resulting in the desired pinch off voltage needed for high drain current and high breakdown voltage. The drain current of approximately 10 A obtained from the analytical model agrees well with that of the Synopsys Sentaurus TCAD simulation and the breakdown voltage approximately 85 V obtained from the TCAD simulation agrees well with published experimental results. The gate-to-source capacitance and gate-to-drain capacitance, drain-source resistance and transconductance were studied to understand the device frequency response. Cut off and maximum frequencies of approximately 10 GHz and 29 GHz respectively were obtained from Sentaurus TCAD and verified by the Smith's chart.**

Index Terms—**SiC, ion implantation, MESFET, analytical device modeling, Sentaurus TCAD, RF power amplifier, high temperature device, RESURF, offset gate**

I. INTRODUCTION

SiC semiconductor material has a wide-band gap (~3.3 eV), high breakdown electric field ($2 - 4\times10^6$ V/cm), high thermal conductivity (3-5 W/cm-°C), high electron saturation velocity (2.7×10^7 cm/s), and stable chemical bonding. SiC based power MESFET has attracted considerable attention for applications in high power and high frequency electronic devices [1-4].

The wide band-gap makes it possible to use SiC for very high temperature operation, up to 600 °C compared to 150 °C for Silicon [5]. SiC devices also have been shown to have low susceptibility to high radiation doses up to 100 megarad [6].

A high breakdown voltage 4H-SiC Schottky diode with edge termination structure was demonstrated with 5 kV breakdown voltage [7,8]. 6H-and 4H-SiC Schottky barrier diodes with breakdown voltages of 1000 V and 1400 V and current densities 100 A/cm^2 and 700 A/cm^2 respectively were reported by several research groups [9,10]. The fabrication of high voltage 6H-SiC Schottky barrier diodes and experimentally observed breakdown voltage exceeding 400 V has been reported [11].

I-V characteristics of submicron 4H-SiC MESFETs have been studied by several research groups. Devices have been demonstrated with an RF output power density of 2.8 W/mm at 1.8 GHz. This power density is three times higher than comparable GaAs devices along with higher reliability and lower forward losses at operating temperature [12]. High power SiC MESFET devices fabricated by K. P. Hilton, et.al. were capable of a single device power output of 6.8 W and 16 W from a single

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three device chip at a pulse frequency of 4 GHz [13]. S-band 4H-SiC MESFETs for microwave power applications have shown ultra high power densities in the range of 5.6 W/mm and 36% associated power-added efficiency (PAE) as well as CW power of 80 W. This demonstrates the applicability of SiC MESFETs and their circuits in linear transmitters for commercial and military use [14]. Baliga, et. al. have reported a high voltage 6H-SiC MESFET fabricated with ion-implantation process and a novel highly asymmetric source-gate-drain structure was created, which is capable of forward blocking voltage of 450 V with a gate voltage of -20 V [15]. Other groups have also developed the SiC MESFETs and reported f_{max} of 11 GHz in 6H-SiC, 12.9 GHz in 4H-SiC [16,17].

Our developed analytical model of the ion implanted SiC MESFET and the 2-D simulation using Synopsys Sentaurus TCAD consider different fabrication parameters. The ion implantation process is preferred in order to precisely optimize the impurity concentration of n-drift region to reduce surface electric field (RESURF) for breakdown voltage enhancement. Impurity diffusion due to annealing has been incorporated in the fabrication parameters to obtain higher accuracy in the device modeling. The drain current obtained from the analytical model is compared to the results from TCAD. We also found that the breakdown voltage obtained from TCAD agrees well with the experimental result [15]. The drain current, breakdown voltage and frequency response of the device using the analytical model and TCAD simulation establish the SiC MESFET devices' applicability for high power and high frequency applications.

II. THEORY

A schematic cross-section of a silicon carbide MESFET is illustrated in Fig. 1. The device structure parameters include the gate length L, gate width W and channel depth *a*, etc. and an offset gate structure in the device has been considered in order to improve high power performance as described in the results and discussions section. Considering impurity diffusion due to annealing, the impurity distribution can be represented by a symmetric Gaussian distribution as follows [18]:

$$N(x,t)=\frac{Q}{\sqrt{2\pi}\sqrt{(\sigma^2+2Dt)}}\exp\left(-\left(\frac{x-R_p'}{\sqrt{2}\sqrt{(\sigma^2+2Dt)}}\right)^2\right)-N_A \quad (1)$$

where $R_p' = R_p + k\Delta X_j$,

Where ΔX_j is the change in the junction depth due to post annealing and is estimated from the implanted profile, where the value of k lies between 0 and 1 [18], and where:

Q = ion dose,
R_P = implant range parameter,
σ = straggle parameter,
D = diffusion coefficient,
t = diffusion time (annealing time).
and N_A = substrate concentration

The diffusion coefficient due to post-implant annealing is assumed to be independent of position and defect concentrations. The active channel depth doped with phosphorus ion implantation with the dose range of 1×10^{13} to 2×10^{13} /cm^2 with implant energy of 14 KeV. The ion implanted distribution profile at post-implant annealing includes the effect of diffusion coefficient for various annealing temperatures as mentioned in Table 1. The model incorporates an annealing time of one hour and the range and straggle parameters calculated using SRIM software.

Solving Poisson's equation using appropriate device boundary condition $\phi'(X_{DG})=0$, the electric field can be expressed by the following equation [20]:

$$\phi'(x)=\frac{qQ}{2\varepsilon}\left[erf\left(\frac{X_{DG}-R_P}{\sqrt{2}\sqrt{\sigma^2+2Dt}}\right)-erf\left(\frac{X-R_P}{\sqrt{2}\sqrt{\sigma^2+2Dt}}\right)\right]+\frac{qN_A}{\varepsilon}(X-X_{DG}) \quad (2)$$

The potential at any point of the channel can be obtained by integration of equation (2) using the boundary conditions $\phi'(X_{DG})=0$ and $\phi(X_{DG})=-\Delta+V(Y)$ which yields:

Table 1. Ion Implantation Parameters for 14 KeV ion energy and Diffusion Coefficients for Phosphorus [19].

Dopant	R_p (cm)	σ (cm)	D_0 (cm^2/s)	Diffusion Coefficient at different annealing temperatures (cm^2/s)			
				2050 °C	2100 °C	2150°C	2200°C
Phosphorus	0.0123×10^{-4}	0.0032×10^{-4}	1.3×10^{10}	6.05×10^{-21}	2.63×10^{-20}	1.08×10^{-19}	4.18×10^{-19}

$$\phi(X)=-\frac{qQ}{2\varepsilon}\left(X-R'_p\right)\left[erf\left(\frac{X-R'_p}{\sqrt{2}\sqrt{\left(\sigma^2+2Dt\right)}}\right)-erf\left(\frac{X_{DG}-R'_p}{\sqrt{2}\sqrt{\left(\sigma^2+2Dt\right)}}\right)\right]+\frac{qN_A}{2\varepsilon}(X-X_{DG})^2$$
$$-\frac{qQ\sqrt{\left(\sigma^2+2Dt\right)}}{\varepsilon\sqrt{2\pi}}\left[\exp\left\{-\frac{\left(X-R'_p\right)^2}{2\left(\sigma^2+2Dt\right)}\right\}-\exp\left\{-\frac{\left(X_{DG}-R'_p\right)^2}{2\left(\sigma^2+2Dt\right)}\right\}\right]+V-\Delta \tag{3}$$

The surface potential can be evaluated by substituting the boundary condition $\phi(X=0)=V_{GS}-\phi_B$ in equation (3) [18]:

$$V-(V_{GS}-\phi_B)=\frac{qQ}{2\varepsilon}\left(R'_p\right)\left[erf\left(\frac{R'_p}{\sqrt{2}\sqrt{\left(\sigma^2+2Dt\right)}}\right)-erf\left(\frac{X_{DG}-R'_p}{\sqrt{2}\sqrt{\left(\sigma^2+2Dt\right)}}\right)\right]$$
$$-\frac{qQ\sqrt{\left(\sigma^2+2Dt\right)}}{\varepsilon\sqrt{2\pi}}\left[\exp\left\{-\frac{\left(R'_p\right)^2}{2\left(\sigma^2+2Dt\right)}\right\}-\exp\left\{-\frac{\left(X_{DG}-R'_p\right)^2}{2\left(\sigma^2+2Dt\right)}\right\}\right]-\frac{qN_A}{2\varepsilon}(X_{DG})^2+\Delta. \tag{4}$$

Where:

V_{GS} = gate-source voltage

Φ_B = Schottky barrier height (Ti – n-type SiC ~ 1.01 eV)

Δ = depth of the Fermi level below the conduction band

ε = permittivity of 4H-SiC

X_{DG} = distance from surface to edge of gate depletion region in the channel

1. Threshold Voltage

The threshold voltage can be obtained from equation (4) considering V(y) = 0 throughout the channel and using boundary conditions $X_{DG} = X_{DS} = X_{PM}$, V(y) = Vp = 0 and $\phi(0)=V_T-\phi_B$ as:

$$V_T=\phi_B-\Delta-\frac{qQR'_p}{2\varepsilon}\left[erf\left(\frac{R'p}{\sqrt{2}\sqrt{\left(\sigma^2+2Dt\right)}}\right)+1-\frac{2N_A}{Q}\left(\frac{2\varepsilon}{qN_A}\left(V_{bi}-V_{BS}\right)\right)^{\frac{1}{2}}\right]$$
$$-\frac{qQ\sqrt{\left(\sigma^2+2Dt\right)}}{\varepsilon\sqrt{2\pi}}\left[\exp\left\{-\frac{R'^2_p}{2(\sigma)}\right\}\right] \tag{5}$$

Where:

V_{bi} = built-in voltage between n-drift layer and p-substrate,

V_{BS} = substrate biasing,

X_{DS} = distance from surface to edge of substrate depletion region in the channel

V_p = pinchoff voltage,

X_p = distance from surface to channel potential minimum.

and

X_{PM} = maximum value X_p above threshold condition,

The ion dose Q and substrate concentration N_A in above equation are the key fabrication parameters for threshold adjustment for enhancement and depletion MESFET devices. The channel impurity concentration N_D is taken as average impurity concentration, which has been computed by iterative method and has been incurporated in this model. The technique for finding the average value of N_D for non-uniform doping distribution is a novel approach for device modeling to accurately determine the donor impurity concentration in the channel region to model the device for evaluating accurate device performance.

2. I-V Characterstics

In order to estimate the power from the drain current and the breakdown voltage of the silicon carbide MESFET, the channel current is evaluated from:

$$I_{DS}=q\mu\frac{Z}{L}\int_0^{V_{DS}}Q_n(V)dV \tag{6}$$

Where the channel charge Q_n is obtained as:

$$Q_n=\int_{X_{DG}}^{X_{DS}}N(X)dX \tag{7}$$

Using gradual channel approximation, the I-V characteristics at different gate-source voltages V_{GS} are evaluated by deriving the following equation [18]:

$$I_{DS}=\frac{qQ\mu Z}{2L}\left[\begin{array}{l}V_{DS}(1+\alpha)-\frac{2qN_A^2}{3Q\varepsilon}\left[\left(\frac{2\varepsilon}{qN_A}\right)\left(V_{bi}-V_{BS}+V_{DS}\right)\right]^{3/2}+\frac{2qN_A^2}{3Q\varepsilon}\left[\left(\frac{2\varepsilon}{qN_A}\right)\left(V_{bi}-V_{BS}\right)\right]^{3/2}\\ -\frac{qQ\sigma}{3\varepsilon}\sqrt{\frac{2}{\pi}}\left[\alpha^2-2\alpha C_1+C_1^2+R\left(V_{DS}-V_{GS}+\phi_{Bn}-\Delta\right)\right]^{3/2}\\ +\frac{qQ\sigma}{3\varepsilon}\sqrt{\frac{2}{\pi}}\left[\alpha^2-2\alpha C_1+C_1^2+R\left(-V_{GS}+\phi_{Bn}-\Delta\right)\right]^{3/2}\end{array}\right] \tag{8}$$

Where:

$$\alpha=\frac{R_P}{2\sigma}\sqrt{\frac{\pi}{2}} \tag{9a}$$

$$R=\frac{\varepsilon\sqrt{2\pi}}{qQ\sigma} \tag{9b}$$

$$C_1=erf\left(\frac{R_P}{\sigma\sqrt{2}}\right) \tag{9c}$$

$$C_2 = V - V_{GS} + \phi_B - \Delta \tag{9d}$$

μ = electron mobility

The above equation is derived by gradual channel approximation modeling and the result is compared with 2-D Synopsis Sentaurus TCAD software simulation. In order to obtain the desired pinch off voltage, the ion implantation doses at specific ion energies were optimized from another set of I-V equations to obtain different drain currents for various pinch-off voltages [18]. This enables optimization of the active channel implant thickness and pinch off voltage for desired I-V characteristics to meet high power device performance [21].

3. Internal Gate Capacitance (Intrinsic Parameters)

The gate space-charge region of a silicon carbide MESFET is divided into three divisions I, II and III with charge segments as Q_1, Q_2 and Q_3 respectively [22,23]. The total internal gate-source capacitance in the region below pinch-off, defined as

$$C_{GS} = C_{GS1} + C_{GS2} + C_{GS3} = \left[\left(\frac{\partial Q_T}{\partial V_S}\right)_{V_G}\right] = \text{constant} \tag{10}$$

The charge Q_1 in region I just underneath the gate is defined as

$$Q_1 = qZL\int_0^{X_{SG}} N(X)dX + \frac{qZL}{X_{DG}-X_{SG}}\int_{X_{DS}}^{X_{DG'}} N(X)(X_{DG}-X)dX$$
$$= qZL\int_0^{X_{DG'}} N(X)dX - \frac{qZL}{X_{DG}-X_{SG}}\int_{X_{DS}}^{X_{DG'}} N(X)(X-X_{SG})dx \tag{11}$$

Where:

X_{SG} = distance from surface to edge of gate depletion region at the source end of the channel

$X_{DG'}$ = distance from surface to edge of gate depletion region at the drain end of the channel

The charges Q2 and Q3 in sections II and III can be expressed as:

$$Q_2 = \frac{\pi}{2}\varepsilon Z(V_{bi} - V_{GS}) \tag{12a}$$

and

$$Q_3 = \frac{\pi}{2}\varepsilon Z(V_{bi} - V_{GD}) \tag{12b}$$

Thus, the internal gate-source and gate-drain capacitance for a silicon carbide MESFET has been derived as:

$$C_{GS} = \frac{qQZL}{2}\left[\frac{M}{2(MR+A_1)^{\frac{1}{2}}} + \frac{\sqrt{N}}{2\left(\sqrt{N}-\sqrt{R}\right)^2}\left\{\begin{array}{l}\frac{(MN+A_1)^{\frac{1}{2}}}{\sqrt{R}} - \frac{M\left(\sqrt{N}-\sqrt{R}\right)}{(MR+A_1)^{\frac{1}{2}}} - \frac{(MR+A_1)^{\frac{1}{2}}}{\sqrt{R}} \\ -\frac{1}{Q}\left(\frac{2N_B\varepsilon}{q}\right)^{\frac{1}{2}}\left\{\frac{2\left(\sqrt{N}-\sqrt{R}\right)}{\sqrt{R}} + \frac{V_{DS}}{\sqrt{RN}}\right\}\end{array}\right\}\right] + \frac{\pi}{2}\varepsilon Z \tag{13}$$

Where,

$$N = V_{bi} - V_{GS} + V_{DS} \tag{14a}$$

$$R = V_{bi} - V_{GS} \tag{14b}$$

$$M = \frac{4\alpha\varepsilon}{qQR_p'} \tag{14c}$$

$$A_1 = \alpha^2 + A_3 \tag{14d}$$

$$\alpha = \frac{R_p'}{2\sqrt{\sigma^2+2Dt}}\left(\sqrt{\pi/2}\right) \tag{14e}$$

$$A_2 = erf\left(\frac{R_p'}{2\sqrt{\sigma^2+2Dt}}\right) - \alpha \tag{14f}$$

$$A_3 = 1 - \exp\left(-\left(\frac{R_p'}{\sqrt{2(\sigma^2+2Dt}}\right)^2\right) - 2\alpha erf\left(\frac{R_p'}{\sqrt{2(\sigma^2+2Dt}}\right) \tag{14g}$$

Similarly, the gate-drain capacitance for ion-implanted silicon carbide MESFET is derived as:

$$C_{GD} = \frac{qQZL}{2}\left[\frac{M}{2(MN+A_1)^{\frac{1}{2}}} + \frac{\sqrt{R}}{2\left(\sqrt{N}-\sqrt{R}\right)^2}\left\{\begin{array}{l}\frac{(MR+A_1)^{\frac{1}{2}}}{\sqrt{N}} - \frac{M\left(\sqrt{N}-\sqrt{R}\right)}{(MN+A_1)^{\frac{1}{2}}} - \frac{(MN+A_1)^{\frac{1}{2}}}{\sqrt{N}} \\ -\frac{1}{Q}\left(\frac{2N_B\varepsilon}{q}\right)^{\frac{1}{2}}\left\{\frac{2\left(\sqrt{N}-\sqrt{R}\right)}{\sqrt{R}} - \frac{V_{DS}}{\sqrt{RN}}\right\}\end{array}\right\}\right] + \frac{\pi}{2}\varepsilon Z \tag{15}$$

4. Internal Drain-Source Resistance

The internal drain-source resistance is calculated by differentiating the I-V equation (6) with respect to V_{DS} for low impedance of the FET switch for which, $V_{GS} = V_{DS} = 0$ [18]:

$$R_{DS} = \left[\frac{q\mu ZQ}{2L}\left[(1+\alpha) - \left(a_p^2 - \frac{V_p}{V_1}\right)^{\frac{1}{2}} - \left((\alpha+1-a_p)^2 - \frac{V_p}{V_2}\right)^{\frac{1}{2}}\right] + \frac{\pi\mu}{2}\left[\frac{2\varepsilon qV_{bi}Q}{\sqrt{2\pi(\sigma^2+2Dt)}}\right]^{\frac{1}{2}}\right]^{-1} \tag{16}$$

$$V_1 = \frac{qQ^2}{8N_A\varepsilon} \tag{17a}$$

$$V_2 = \frac{qQ\sqrt{\sigma^2+2Dt}}{\sqrt{2\pi\varepsilon}} \tag{17b}$$

and

$$a_p = \frac{2N_A}{Q}\sqrt{\frac{2\varepsilon}{qN_A}\left(V_{bi} - V_{BS} + V_p\right)} \quad (17c)$$

5. Specific on-Resistance

The conductivity of the channel is modulated by the gate bias potential and the current flow is obtained by the resistance of various resistive components. The total specific on-resistance ($R_{on\text{-}sp}$) can be expressed as [24,25]:

$$R_{on-sp} = R_n + R_c + R_d + R_s = R_n + R_c + R_d + R_{epi} + R_{sub}$$
$$= \rho_n W_n + \rho_c W_c + \rho_p W_{pp} + \rho_{epi} W_{epi} + \rho_{sub} W_{sub} \quad (18a)$$

Where R_n = contribution from the n+ source diffusion, R_c = channel resistance, R_d = drift region resistance, R_{epi} = epi-layer resistance, R_{sub} = substrate resistance, ρ_n = resistivity of n+ sources diffusion, ρ_c = resistivity of channel, ρ_p = resistivity of drift region, ρ_p = resistivity of drift region, ρ_{epi} = resistivity of epi-layer, ρ_{sub} = resistivity of substrate, W_n = thickness of source region, W_c = thickness of active channel, W_{pp} = depletion width of drift region, W_{epi} = thickness of epi-layer, and W_{sub} = thickness of substrate.

At lower breakdown voltages, all these resistive components are comparable, therefore the contributions of each of these resistances should be considered when calculating the $R_{on\text{-}sp}$. The SiC MESFET showed high breakdown voltage in Fig. 3b, so the drift region resistance R_d is significantly higher than other resistances. Thus, $R_{on\text{-}sp}$ can be approximated by R_d. The specific on-resistance is calculated as follows [26]:

$$R_{on-sp} \approx R_d = \frac{W_{pp}}{q\mu N_D} \quad (18b)$$

With the maximum depletion width layer derived as:

$$W_{pp}(4H-SiC) = 1.82x10^{11} N_D^{-7/8}$$

6. Transconductance (gm)

The transconductance of the silicon carbide MESFET is obtained by differentiating I_{DS} with respect to V_{GS}, with constant V_{DS} [18]:

$$g_m = \frac{q\mu ZQ}{4L}\left[\frac{1}{V_1 a_p} + \frac{1}{V_2\left(\alpha + 1 - a_p\right)}\right]\left(V_{GS} - V_T\right) \quad (19)$$

III. Numerical Calculations, Results and Discussions

The results based on analytical modeling and Synopsys Sentaurus TCAD version Y-2006.06 are presented here to evaluate the characteristics of threshold voltage, drain-source currents, gate capacitances and cut-off frequency response of an ion-implanted 4H-SiC MESFET device. The TCAD simulation involves the use of several parameters such as channel depth, doping concentrations of drift region and source and drain, velocity saturation, cell density (~1500 nodes) and others as stated in the corresponding text. TCAD uses for consideration of mobility during simulation the following models: doping dependence SRH and Auger Recombination model, doping dependence and electric field dependence mobility models and incomplete ionization model.

Fig. 1 shows a schematic diagram of the SiC MESFET device where L_{gs} (distance between source and gate) = 0.7 μm, L_{gd} (distance between gate and drain) = 3 μm, and L (channel length) = 1μm are considered to form an offset gate structure. The annealing effect on ion implanted impurity distribution was included in order to precisely determine the fabrication parameters for navigating the fabrication process and process integration.

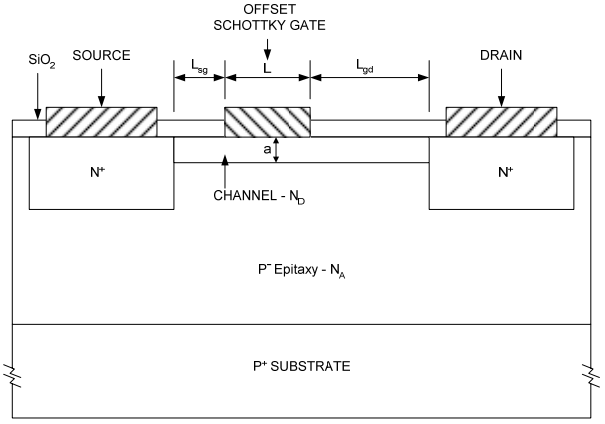

Fig. 1. Schematic diagram of an ion implanted silicon carbide MESFET. Dimension W is perpendicular to this cross section view.

Fig. 2(a) shows the threshold voltage (V_T) versus ion dose (Q) of SiC MESFET calculated from equation (5), where the substrate concentration N_A =5×10^{15} /cm^3 with device structure Z = 1000 μm and L = 1 μm are considered. The plot shows that the threshold voltage (V_T) is linearly decreasing with respect to an increase in ion doses (Q). It is clear from the threshold voltage variation from -1.1 V to -3.54 V with incremental ion doses from 9×10^{12} to 2×10^{13} /cm^2 that the FET device behaves in depletion mode. The increasing of the ion dose pushes the threshold voltage further into depletion mode region, where as decreasing of the ion dose pushes the threshold voltage toward the enhancement mode region. The space charge distribution in the gate depletion region under threshold condition is extracted from the Synopsys software as shown in Fig. 2(b). This space charge distribution plot shows that the channel region is totally depleted under threshold condition $V_{GS} \leq V_T$.

In order to study the I-V characteristics, Fig. 3(a) is derived from equation (8) and shows the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) for different gate-source biasing (V_{GS}), considering the substrate

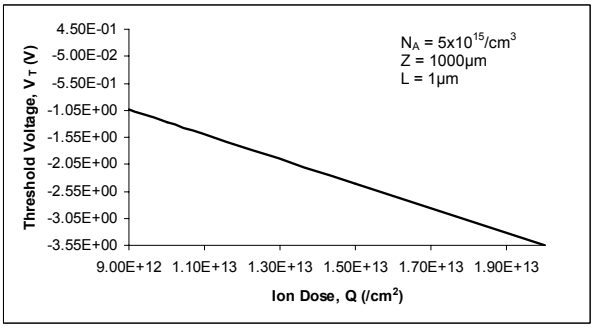

Fig. 2(a). Threshold voltage (V_T) versus ion dose (Q) for ion implanted SiC MESFET.

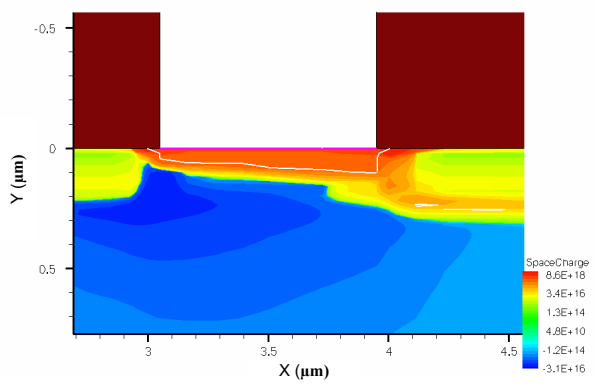

Fig. 2(b). Space charge distribution and gate depletion region under threshold voltage condition.

concentration $N_A = 5\times10^{15}$ /cm^3, $N_D = 1.38\times10^{18}$ /cm^3 with the device structure, Z = 1000 μm, and L = 1 μm. The computations for the I-V curve plots are performed using MatLab for the analytical model and Synopsys Sentaurus TCAD software. The saturation current using MatLab is found to be 10 A for V_{DS} = 10 V at V_{GS}= 4 V, whereas the saturation current using TCAD is found to be 9.3 A for same device biasing configurations. Saturation currents of approximately 5.5 A and 5.7 A for V_{DS} = 10 V at V_{GS} = 2 V are also obtained respectively using MatLab and TCAD. This analytical result agrees well with the TCAD results with a difference of less than 10% between the analytical model and the TCAD simulation. Hence, the value of field dependent electron mobility in MatLab agrees well with the Synopsys result. The device with n-drift region length of 7 μm is able to support a breakdown voltage of >85 V as shown in Fig. 3(b), when a positive gate bias of 4 V is applied. In order to maintain two dimensional charge coupling between the n-drift layer ($N_D = 1.38\times10^{18}$ /cm^3) and p-type of substrate ($N_A = 5\times10^{15}$ /cm^3), the ion dose and substrate concentration respectively have been optimized to modify the lateral electric field (applying reduced surface electric field concept) so that the breakdown voltage is increased. Fig. 3(c) and (d) show the optimized electric field at the edge of Schottky gate (4 μm) after optimization of n-drift region and p-substrate concentrations. The estimated electric field at the surface and bulk in the metal Schottky contact towards the drain has a range of approximately 1.4-1.8 MV/cm (from color chart), which is below the critical electric field of 4H-SiC material. Hence, edge termination in this device structure is not required for 4H-SiC material. The estimated dc power of our offset gate structure is expected to be 110W [27]. A lateral 6H-SiC based MESFET structure with an offset gate structure (L_{gs} = 3.5 μm and L_{gd} = 15 μm) has been reported with a high breakdown voltage of 450 V [15]. If the reported 6H-SiC MESFET is scaled down for scaling factor 5, the device structure (L_{gs} = 0.7 μm and L_{gd} = 3 μm) would be similar to our device and the breakdown voltage should be in the range of 90 V. While the ion dose requirements differ for 6H and 4H-SiC, the results are otherwise very comparable, and our simulated value of 85 V is close to the experimental results of 90 V.

The electrostatic potential distribution at 0.05 μm bulk with V_{GS} = 4 V is obtained from the Synopsys software and is plotted in Fig. 4(a). The channel potential at the

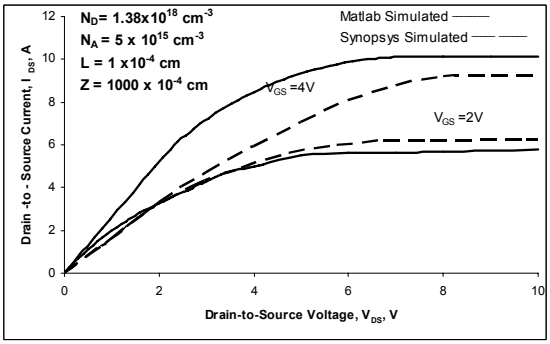

Fig. 3(a). Drain-to-source current (I_{DS}) versus drain-to-source voltage (V_{DS}) for different Gate-to-source voltage (V_{GS}) simulated by analytical modeling and Synopsys Sentaurus TCAD.

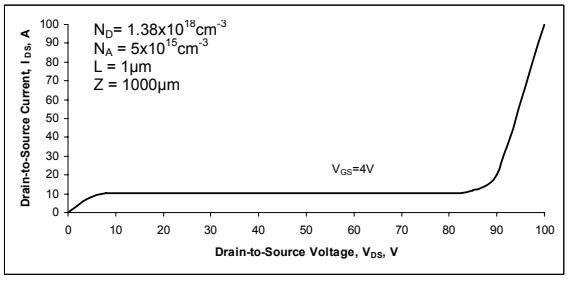

Fig. 3(b). Drain-to-source current versus drain-to-source voltage for breakdown characteristic simulated by Synopsys Sentaurus TCAD.

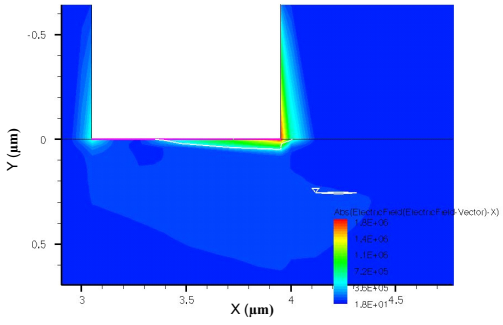

Fig. 3(c). Electric field distribution with color contour lines in a silicon carbide MESFET in the gate region simulated by Synopsys Sentaurus TCAD.

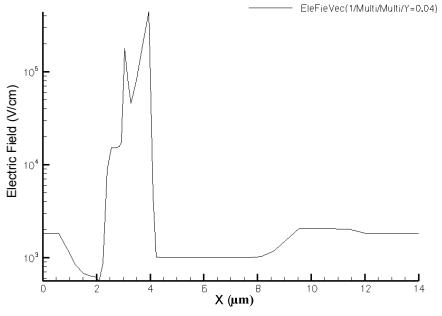

Fig. 3(d). Electric Field distribution in a SiC MESFET with a y-cut at y=0.05 microns in the gate region simulated by Synopsys Sentaurus TCAD.

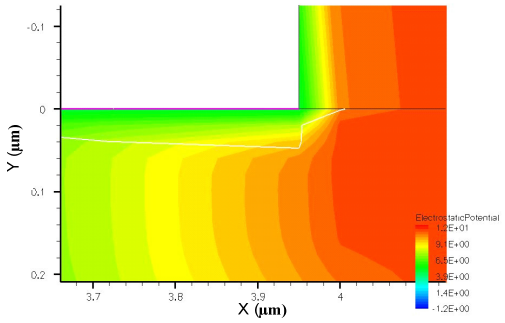

Fig. 4(a). Electrostatic potential distribution of the ion implanted SiC MESFET in the channel region at V_{GS} = 4 V simulated by Synopsys Sentaurus TCAD towards gate-to-drain end.

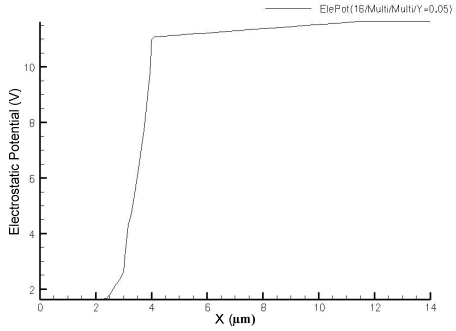

Fig. 4(b). Electrostatic potential distribution of the ion implanted SiC MESFET at 0.05 micron bulk in the channel region of 2 μm to 4 μm at VGS = 4 V simulated by Synopsys Sentaurus TCAD.

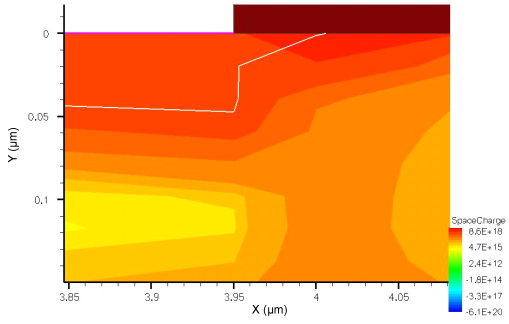

Fig. 4(c). Space charge distribution of the ion–implanted SiC MESFET at V_{GS}= 4 V simulated by Synopsys Sentaurus TCAD towards gate-to-drain end.

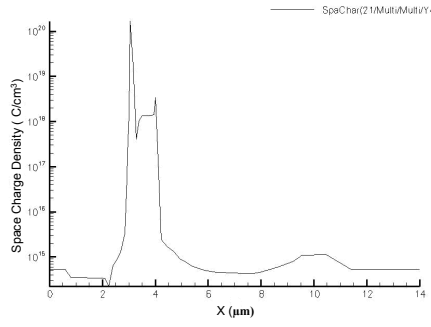

Fig. 4(d). Space charge density of ion implanted SiC MESFET at 0.01 micron bulk in the gate region at V_{GS} = 4 V simulated by Synopsys Sentaurus TCAD.

Schottky metal corner is minimized by reducing the electric field as a result of optimizing n-drift region concentration, which in turn increases the breakdown voltage to >85 V. Fig. 4(b) shows clearly the channel potential, which increases up to 4 μm and then saturates as seen in the drain potential V_{DS} = 10 V in Fig. 3(a).

Fig. 4(c) and (d) represent the space charge distribution at 0.01 μm bulk at V_{GS} = 4 V under the same conditions as the I-V curve plots of Fig. 3(a). This result obtained from TCAD indicates that the maximum space charge (on the order of 10^{18} /cm^3) in the gate depletion forms on the gate-drain side, therefore minimizing the gate depletion width allowing the channel cross-section to be open. However, as plotted in Fig. 6(d) there appears a spike of excessively high space charge density (10^{20} /cm^3) which seems to be an anomalous error and should be ignored.

Fig. 5 shows the temperature dependent I-V characteristics simulated by the analytical model using the MatLab which includes the effect of temperature dependent parameters (intrinsic carrier concentration, carrier mobility, bandgap, etc.). The plot shows the drain-source current (I_{DS}) versus the drain-source voltage (V_{DS}) for different gate-source voltages V_{GS} = 2 V, 4 V and -3 V with channel impurity concentration $N_D = 1.38\times10^{18}$ /cm^3 (ion dose Q = 2×10^{13} /cm^2) and substrate concentration $N_A = 5\times10^{15}$ /cm^3 with a lateral device structure of channel length L = 1 μm, channel width Z = 1000 μm. The plot indicates the effect of increase in temperature on the device. The change in the nature of I-V characteristics is insignificant with differences limited to about 5%. Thus the I-V characteristics of SiC MESFET are extremely stable from the room temperature to high temperature (600 °C) indicating excellent viability for use in a wide range of extreme environment applications.

The calculated results for gate-source capacitance from equation (13) are illustrated in Fig. 6, which shows the characteristics of gate-source capacitance C_{GS} as a function of various gate-source voltages V_{GS} for ion dose of 2×10^{13} /cm^2 and 1.5×10^{13} /cm^2 at a fixed drain source voltage V_{DS} = 7 V. The variation of the gate-source capacitance C_{GS} with respect to gate-source biasing V_{GS} reveals that the gate-source capacitance increases with respect to a positive increase in negatively biased gate-source voltage V_{GS}. The gate-source capacitance C_{GS} for ion dose 2×10^{13} /cm^2 is initially increasing with low slope for V_{GS} = -3 V to 0.7 V and rises very sharply up to approximately 2.2×10^{-11} F as V_{GS} approaches 3 V, where as the gate-source capacitance C_{GS} for ion dose 1.5×10^{13} cm^{-3} also increases very slowly up to approximately 0.7×10^{-13} F between the gate-source voltage V_{GS} = -3 V to 1.5 V and then rises sharply to 1.9×10^{-13} F.

The computed results from equation (15) are shown in Fig. 7 which are the gate-drain capacitances C_{GD} versus drain-source voltages V_{DS} for constant gate-source voltages V_{GS} = 4 V with ion doses of 2×10^{13} /cm^2, 1.5×10^{13} /cm^2, 1×10^{13} /cm^2, and 9×10^{12} /cm^2. At drain-source voltage V_{DS} = 0.25 V, the gate-drain capacitances C_{GD} is approximately 7.7×10^{-12} under ion dose 2×10^{13} /cm^2 and 1.5×10^{13} /cm^2. The gate-drain capacitance C_{GD} at V_{DS} = 0 are approximately 7.45×10^{-12} F and 7.2×10^{-12} F with ion doses of 1×10^{13} and 9×10^{12} /cm^2 respectively. As the drain-source voltage approaches V_{DS} = 3 V to 7 V, the gate-drain capacitances C_{GD} drop to approximately 3.9×

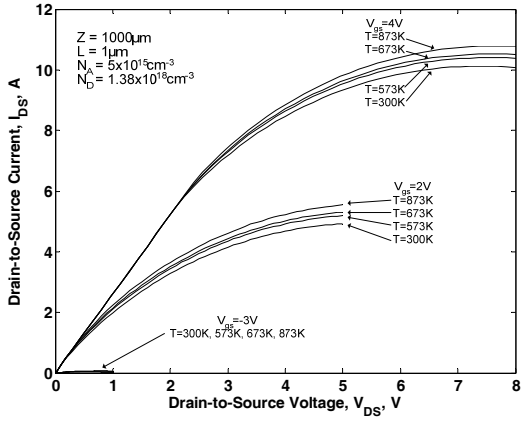

Fig. 5. Drain-to-source voltage versus drain-to-source current at different gate-to-source voltages for different temperatures.

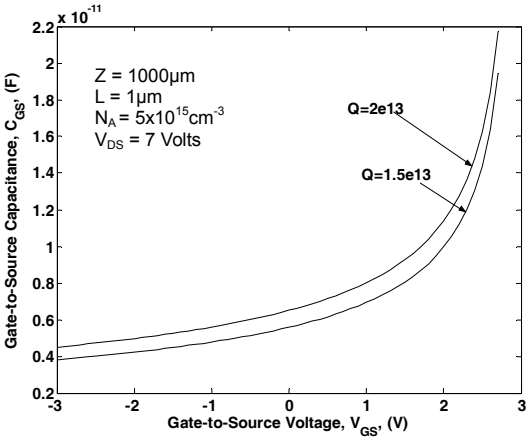

Fig. 6. Gate-to-source capacitances (C_{GS}) versus gate-to-source voltages (V_{GS}) at different ion doses.

10^{-12} F to 3.7×10^{-12} F for ion doses 2×10^{13} /cm^2 to 9×10^{12} /cm^2 respectively. Thus the variation of the internal gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} are strongly influenced by the device biasing and n-drift impurity concentration leading to improved frequency performance of the SiC MESFET. The above simulation for the gate capacitances using Takada modeling [21] is considered to be fairly accurate and the nature of gate capacitance indicated by Takada modeling is very similar to our results.

Fig. 8 shows a plot of drain-source resistance R_{DS} versus the ion dose (Q) calculated from the equation (16) and the variation of R_{DS} as the ion dose (Q) is increased from 5×10^{12} /cm^2 to 2×10^{13} /cm^2 at channel length L = 1 μm, 2 μm and 3 μm for V_{DS} = 0 V and V_{GS} = 0 V. As the ion dose increases, the value of R_{DS} slowly decreases from 1.4 ohm to 0.6 ohm for the channel length L = 1 μm, where as R_{DS} rapidly decrease from 2.8 to 1.3 ohms and 4.3 to 1.9 ohms for the channel length L = 2 μm and 3 μm respectively. Thus it is clearly evident from the plots that the channel-resistance is decreasing with increasing ion dose, which results in n-drift being highly doped in order to increase the breakdown voltage. The ion dose in the n-drift layer must optimized due to: (1) when the charge in n-drift region is too small, it becomes depleted at low drain bias voltage and so a high electric field is developed at the drain side within the n-drift layer resulting in a reduction of the breakdown voltage and (2) if the charge in the n-drift region is too high, the n-region will not be depleted by the drain bias and the charge coupling effect between the n-drift layer and substrate will be lost. Additional a high electric field will develop at the gate side within the n-drift region also resulting in a low breakdown voltage.

The specific on-resistance $R_{on\text{-}sp}$ is decreasing as the n-drift region concentration N_D becomes more doped which results in breakdown voltage enhancement. The plot of specific on-resistance $R_{on\text{-}sp}$ versus n-drift region concentration N_D is obtained from equation (18b). The result is shown in Fig. 9 where the specific on-resistance $R_{on\text{-}sp}$ is decreasing with increasing of n-drift region concentration N_D. The typical value of $R_{on\text{-}sp}$ of 4H-SiC MESFET is obtained approximately 0.6 mΩ-cm^2, which agrees well with other results described below. The reported specific on-resistance ($R_{on\text{-}sp}$) of GaAs based devices are in the order of 10^{-6} Ω-cm^2 with corresponding limitations in the breakdown voltage, where as $R_{on\text{-}sp}$ of Si and 4H-SiC based devices are in the order of 10^{-5} Ω-cm^2 and 10^{-4} Ω-cm^2 respectively with correspondingly higher

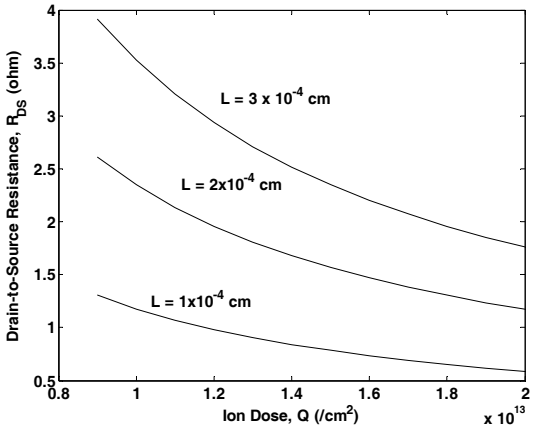

Fig. 8. Drain-to-source resistance (R_{DS}) versus ion dose (Q) for different channel lengths.

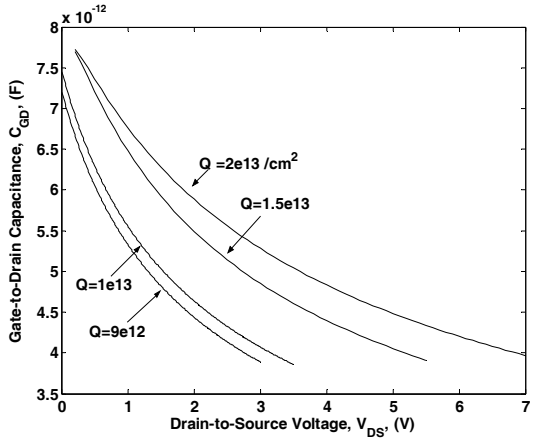

Fig. 7. Gate-to-drain capacitances versus drain-to-source voltages (V_{DS}) for different ion doses.

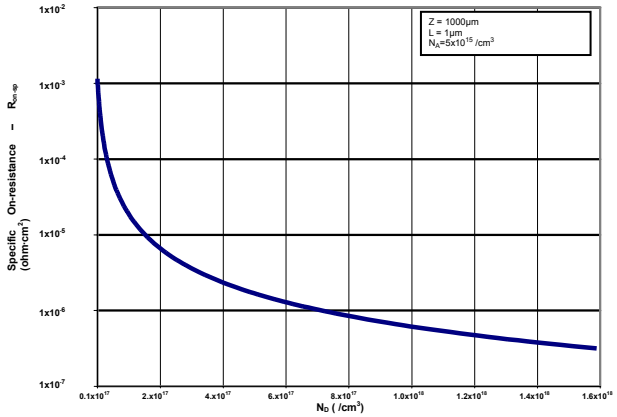

Fig. 9. Specific on-resistance versus n-drift layer concentration for device with Z=1000 μm, gate length L=1 μm, and N_A= 5×10^{15} /cm^3.

breakdown voltages [28-29]. $R_{on\text{-}sp}$ of 4H-SiC is nearly constant to above value up to approximate breakdown voltage of 10^3 V. The reported 4H-SiC $R_{on\text{-}sp}$ therefore agrees very well with our results.

A plot of transconductance g_m versus gate-source voltage V_{GS} for different ion doses Q = 2×10^{13} /cm^2, 1.5×10^{13} /cm^2 and 9×10^{12} /cm^2 as shown in Fig. 10 are derived from equation (19) to understand the device frequency response. The transconductance g_m is linearly increasing up to approximately 2 siemens, 1.60 simens and 1.25 simens with the increasing of gate-source voltage swing from V_{GS} = -4 V to V_{GS} = +4 V for different ion doses Q = 2×10^{13} /cm^2, 1.5×10^{13} /cm^2 and 9×10^{12} /cm^2. The threshold voltage for ion dose Q = 2×10^{13} /cm^2, 1.5×10^{13} /cm^2 and 9×10^{12} /cm^2 is found to be -3.5 V, -2.35 V, and -1.05 V respectively obtained from equation (5), which agrees well with the threshold voltage obtained from the plot in Fig. 10 at the V_{GS} axis for g_m = 0. The alternate method was required due to the limited support in TCAD for 4H SiC device simulation of intrinsic and extrinsic parameters. However, all intrinsic parameters as shown in Fig. 6, 7 and 10 indicate high frequency device response.

Fig. 11 shows the plot of cut-off frequency f_t versus gate-source voltage V_{GS} obtained from TCAD. The cut-off frequencies shown are 11.66 GHz and 10.81 GHz at unity-gain point and 10 dB point respectively. 10 dB frequency is the frequency where the attenuation of H21 is at a magnitude of 10 dB (considered severe attenuation). Fig. 12 shows the plot of maximum frequency f_{max} versus gate-source voltage V_{GS} obtained from TCAD. The maximum frequencies f_{max} obtained are 26.66 GHz and 29.76

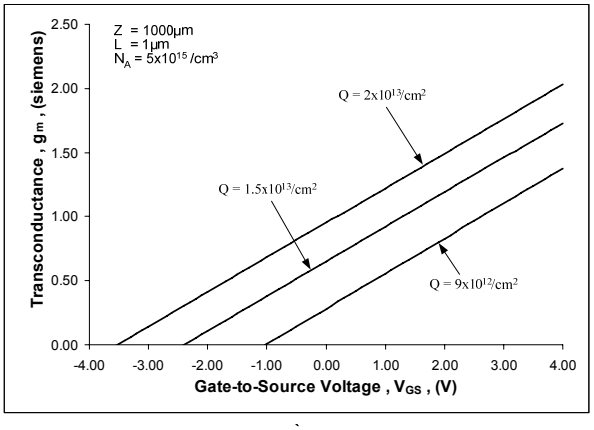

Fig. 10. Transconductance (g_m) versus gate-to-source voltage (V_{GS}) for different ion doses.

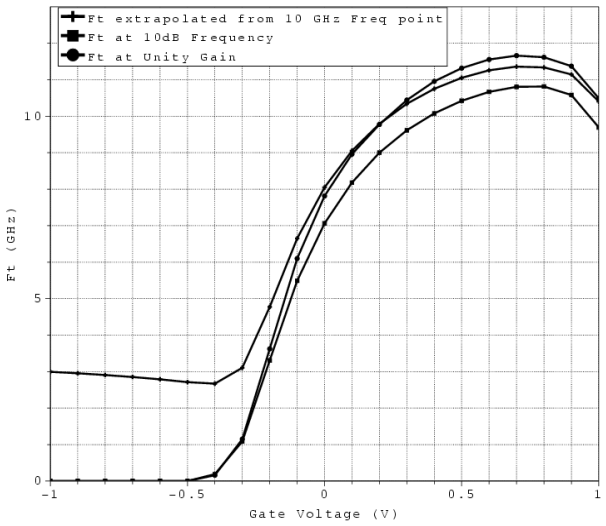

Fig. 11. Cut-off frequency (f_T) versus gate voltage for unity gain point and 10 dB attenuation point simulated by Synopsys Sentaurus TCAD for SiC MESFET.

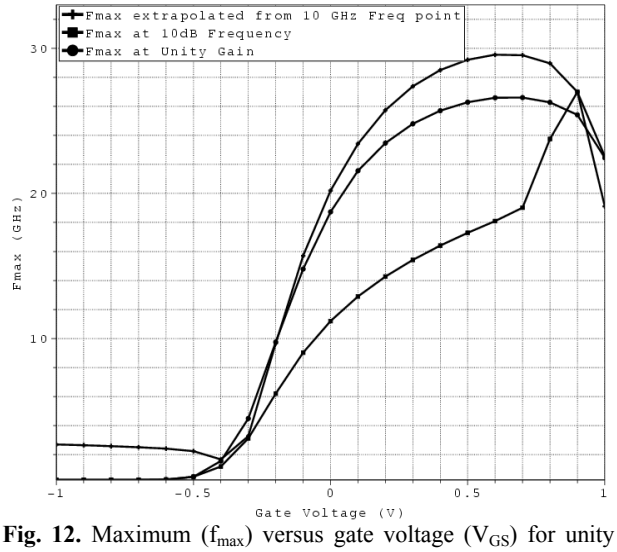

Fig. 12. Maximum (f_{max}) versus gate voltage (V_{GS}) for unity gain point and 10 dB attenuation point simulated by Synopsys Sentaurus TCAD for SiC MESFET.

GHz at unity-gain and 10 dB points respectively.

The S-parameters for the SiC MESFET are obtained from the Smith Chart generated in TCAD as depicted in Fig. 13, and agree with plots in Fig. 11 and 12. Smith chart can only be used to plot S11 and S22 parameters (transmission/reflectance). This research area will be extended further in future studies to explore more rf characteristics of 4H-SiC including S12 and S21 by polar plots. At present the Smith chart shows S11 gate-source (input) impedance and S22 drain-source (output) impedance are approximately 1-j0.028 Ω ($1\angle-1.60°$ Ω) at 0.1 GHz and 0.93 – j0.04 Ω ($0.93\angle-2.46°$ Ω) at 0.1 GHz res-

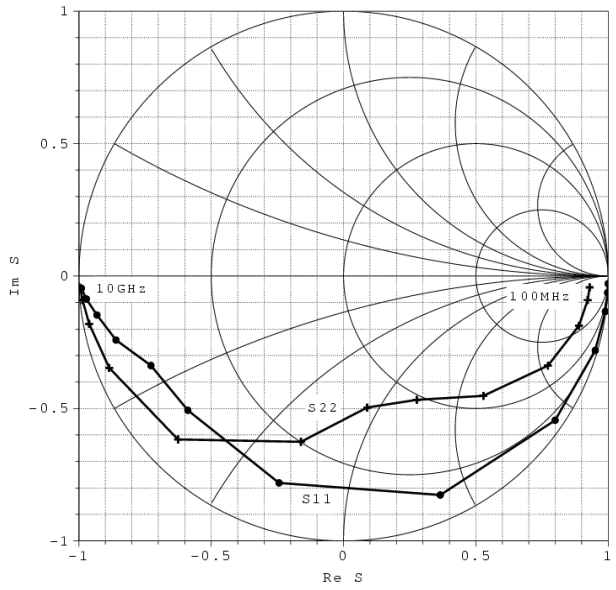

Fig. 13. Smith chart simulated S- parameters using Synopsys Sentaurus TCAD for SiC MESFET.

pectively, because the device behaves as depletion device (normally-on) with device width of 1000 μm.

IV. CONCLUSIONS

Analytical modeling with numerical calculations and software simulations have been performed for evaluation of the threshold voltage, drain-source current, breakdown characteristics, intrinsic parameters, cut-off frequency and other related parameters for 4H-SiC MESFET.

The results show the potential application of the device for high power and high frequency amplification for the aerospace and defense telemetry and communication applications. The drain current of the device is extremely stable for temperature variations from 30 °C to 600 °C. Such excellent features of SiC MESFET can be very useful for applications in high temperature environments. The device simulation using Synopsys Sentaurus TCAD shows that the SiC MESFET exhibits a large drain current and high breakdown voltage, which allow the device to be used for high power amplification. The Smith chart indicates the cut-off frequency and maximum frequency in the range of 10 GHz to 29 GHz, which make the device suitable for use at high frequencies (up to Ka band).

The device performance of SiC MESFETs has begun to look very promising to use in high frequency and high power amplification. This inherent quality of the SiC MESFET device may enable solid state replacement of the traveling wave tube for high frequency and high power amplifier application in some applications.

Further enhancing of the high power density potential of this family of device by developing and implementing the RESURF concept at it applies to fabrication of SiC MESFETs will be investigated by this team in the near future.

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