An Analytical Model for SiC MESFETs

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Abstract

An improved analytical model for simulating the performance of SiC MESFETs has been developed for use in device design for high frequency, high power applications. The model is based on a two-dimensional analysis of the charge distribution under the gate and incorporates a field-dependent mobility, velocity saturation and charge buildup in the channel. The model is used to generate the large signal current-voltage characteristics of the device and transconductance, output conductance and capacitances for a small signal model.

Introduction

SiC MESFETs are attractive devices for high temperature, high power applications due to their large bandgap, high breakdown voltage, large saturation velocity, high thermal conductivity and simplicity of fabrication [1-3]. As an aid in SiC MESFET device design and development, device modeling has been pursued along several directions [4-6]. Based on a two-region model for the channel that incorporates a field dependent mobility and velocity saturation, Tsap [6] has derived an analytical model that takes into account the fact that since the critical field for velocity saturation is large in SiC, unlike the case in GaAs MESFETs, the electrons do not reach velocity saturation for a significant portion of the channel. As a result, the constant mobility approximation is not adequate to describe the electron transport in the low field region and leads to an inaccurate estimation of the drain current and device characteristics. Using his model, he investigated the effects of inclusion of the field dependent mobility on the device's power gain and cutoff frequency.

In this paper we describe the development of an improved analytical model for the SiC MESFET which takes into account not only the field dependent mobility of the electrons near the source, but also the charge buildup effect due to velocity saturation at the drain end of the channel. Our approach follows that previously employed for GaAs MESFETs [7,8], but avoids the complications introduced by the velocity overshoot in the velocity-field characteristic, which is very small in SiC [9].

Analytical Model

For SiC, the electric field dependence of the electron mobility can be described following the empirical Caughey-Thomas [5,10] model for silicon

$$\mu(E)=\frac{\mu_o}{\left[1+\left(\frac{\mu_o E}{v_s}\right)^{\beta}\right]^{1/\beta}} \tag{1}$$

where μ_o is the low field mobility, v_s is the saturation velocity, E is the electric field strength and β is a curvature parameter describing the saturation tendency (~0.8). For simplicity, we assume $\beta = 1$ in our analytical model, which is a good approximation as seen in Figure 1 where we have compared the field dependence of the mobility for $\beta = 1$ with that for a value ($\beta = 0.84$) typical of Monte Carlo simulations [3] and that reported from experimental observations ($\beta = 1.2$) [11].

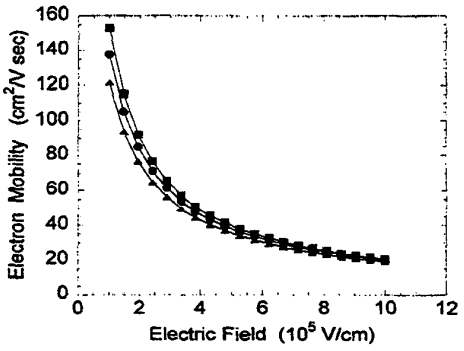

Figure 1 Field dependent electron mobility for β = 0.84 (▲), 1 (●) and 1.2 (■).

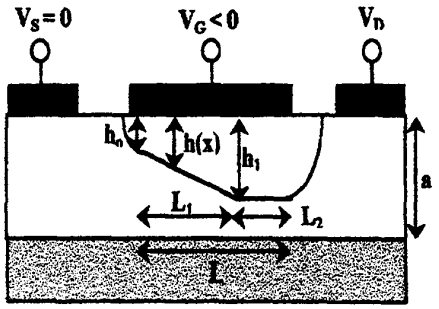

Figure 2 Device cross-section for saturation region operation.

For describing device operation, the field dependent mobility can be incorporated in the drain current I_D expression

$$I_D = qWn(x)\mu(E)E(x)[a - h(x)] \tag{2}$$

where W is the channel width, a is the epitaxial channel layer thickness, E(x) is the field along the channel, n(x) is the electron concentration, and h(x) is the depletion layer thickness under the gate at a distance x from the source. For small drain biases, we assume the electron velocity in the channel does not reach its saturation value and that the gate bias is not sufficient to pinch off the channel. Then, n(x) is simply N_D, the doping in the channel. Relating the electric field to the potential V(x) in the channel and integrating over the channel length L following Tsap [6] and Sze [12] we obtain for the drain current

$$I_D(V_G, V_D) = I_P \frac{\left[3\left(u_d^2 - u_o^2\right) - 2\left(u_d^3 - u_o^3\right)\right]}{1 + Z\left(u_d^2 - u_o^2\right)} \tag{3}$$

where u_d (u_o) is the depletion layer width h_d (h_o) at the drain (source) end of the channel normalized to the epi channel layer thickenss a and given by

$$u_o(V_G) = \frac{h_o}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon}{qN_D}\left(V_G + V_{bi}\right)} \qquad u_d(V_G, V_D) = \frac{h_d}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon}{qN_D}\left(V_D + V_G + V_{bi}\right)} \tag{4}$$

where V_G is the magnitude of the negative bias on the gate, V_{bi} is the builtin potential for the Schottky gate, and V_D is the drain bias and I_P and Z are constants given by

$$I_P = \frac{q^2 N_D^2 \mu_o W a^3}{6\varepsilon\ L} \quad \text{and} \quad Z = \frac{qN_D a^2 \mu_o}{2\varepsilon\ L v_s} \tag{5}$$

where L is the gate length.

As the drain bias increases, the channel is increasingly constricted near the drain and the electron velocity rises toward its saturation value. When the electron velocity approaches close to its saturation value, i.e. $v(L) = \gamma v_s$ where γ is a factor close to one, then $u_d = u_s$ and the drain current reaches saturation and is given simply by

$$I_{Dsat} = qN_D W \gamma v_s \left(1 - u_s\right) \tag{6}$$

where u_s is found by equating (3) and (6). The drain saturation voltage can then be found from (4)

$$V_{Dsat} = u_s^2 V_P - V_G - V_{bi} = V_P\left(u_s^2 - u_o^2\right) \tag{7}$$

where V_P is a constant given by $V_P = qN_D a^2/2\varepsilon$.

For the MESFET in the saturation mode, we divide the region under the gate into two regions: region I near the source where the velocity is less than the saturation value and region II corresponding to a velocity saturation region near the drain as shown in Figure 2. For region I, following Tsap [6] and our previous analysis for (3) we get for the drain current

$$I_D(V_G,V_D) = I_P \frac{\left(\frac{L}{L_1}\right)\left[3\left(u_1^2 - u_o^2\right) - 2\left(u_1^3 - u_o^3\right)\right]}{1 + Z\left(\frac{L}{L_1}\right)\left(u_1^2 - u_o^2\right)} \tag{8}$$

where L_1 is the length of region I and u_1 is given by

$$u_1(V_G,V_D) = \frac{h_1}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon}{qN_D}\left(V(L_1) + V_G + V_{bi}\right)} \tag{9}$$

where h_1 is the depletion layer width and $V(L_1)$ is the potential in the channel at $x = L_1$ which is given by

$$V(L_1) = V_P(u_1^2 - u_o^2) \tag{10}$$

The location L_1 corresponds to where the velocity nearly reaches the saturation velocity, i.e. where $v(L_1) = \gamma v_s$ where γ is the velocity saturation factor defined above, so we can also write for the drain current

$$I_D = qWN_D\gamma v_s a[1 - u_1] \tag{11}$$

Equating (8) and (11) we obtain an expression for the length of region I L_1 in terms of u_1

$$L_1 = LZ\left[\frac{\left(u_1^2 - u_o^2\right) - \frac{2}{3}\left(u_1^3 - u_o^3\right)}{\gamma\left(1 - u_1\right)} - \left(u_1^2 - u_o^2\right)\right] \tag{12}$$

which is slightly different from Tsap's [6] result due to γ. We also note here that the electric field E_s corresponding to the velocity saturation condition can be found by using $v(L_1) = \gamma v_s$ and (1) to obtain

$$E(L_1) = E_s = \frac{v_s}{\mu_o}\left(\frac{\gamma}{1-\gamma}\right) \tag{13}$$

Following the analysis of Chang and coworkers [7,8] for GaAs MESFETs and HEMTs, we examine the two dimensional nature of the potential under the gate. Solving Poisson's Equation and using the boundary conditions we obtain a useful result by evaluating the potential at the drain end of the channel ($x = L$, $y = h_1$) where the potential is just equal to the drain bias V_D.

$$V_P\left(u_1^2 - u_o^2\right) + \frac{2E_s a u_1}{\pi}\sinh\left(\frac{\pi(L - L_1)}{2au_1}\right) = V_D \tag{14}$$

where the first term is the voltage drop across region I and the second term corresponds to the voltage drop along the velocity saturation region (region II). What is useful about this result is that (14) can be used in combination with our earlier expression for L_1 given in (12) to solve for u_1 at the velocity saturation point for a given device structure and set of biases. Once u_1 is found, L_1 can be found from (12) and the drain current found from (11). This result is similar to (1) in Tsap [6] except that u_1 appears in the prefactor to the hyperbolic sine function and in the denominator of the argument of that same function, which leads to somewhat different results.

Simulation Results

To illustrate the model, we have simulated the current-voltage characteristics for a device similar to a recently reported MESFET fabricated in 4H SiC [4]. Shown in Table I is a summary of material parameters obtained from the literature and employed in the simulation [1,4, 9, 11,13-20]. For the low field electron mobility, the doping dependence described by the empirical Caughey-Thomas model [10] was used to calculate the mobility based on the channel doping.

Table I Summary of Material Parameters for 4H Silicon Carbide

Parameter	Value	References
Energy bandgap	3.25 eV	[1]
Dielectric constant	9.7	[4,13]
Electron mobility		
μ_{max} , μ_{min}	950, 40 cm^2/V sec	[9]
N_{ref} , α	$2x10^{17}/cm^3$, 0.76	
Saturation Velocity	$2.2x10^7$ cm/sec	[9,11,13]

Shown in Figure 3 are the output characteristics for a device with a channel doping of $1x10^{17}/cm^3$, channel layer thickness of 0.15 μm and gate length and width of 1 μm and 10 μm, respectively. Figure 4 shows the transconductance as a function of the gate bias for two drain biases, one in saturation and one in the linear region.

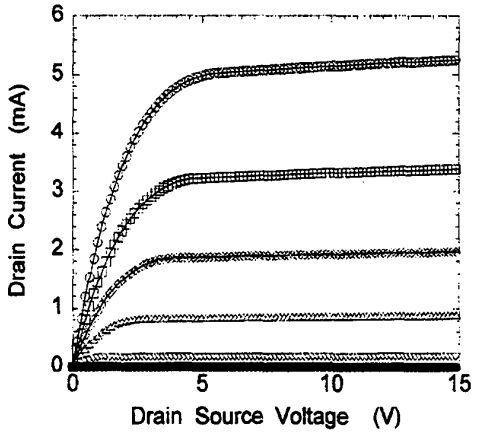

Figure 3 Output I-V characteristics for MESFET with 1 μm channel length for gate biases $V_G = 0$, -2, -4, -6, -8 and –9.4 V.

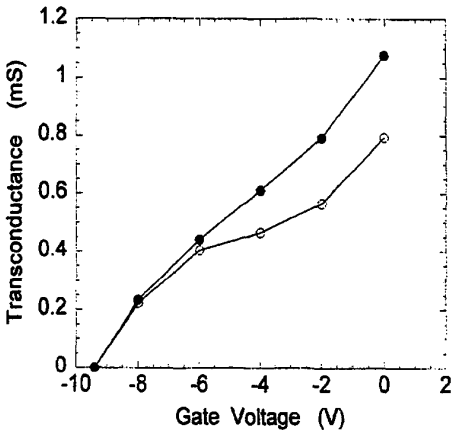

Figure 4 Transconductance as a function of gate bias for drain biases of 2.5 V (○) and 10 V(●).

Discussion and Conclusions

In summary, we have developed an improved drift-diffusion model for the SiC MESFET which takes into account the field dependence of the mobility, velocity saturation near the drain and the two dimensional nature of the depletion region under the gate. The model has been used to predict the large and small signal behavior of the device and is suitable for use in device design and development.

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