

# Masayuki Shimoda

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## Research Interests

- **FPGA-based Accelerators:** Application-specific Architectures
- **Design Automation:** Design Space Exploration and Hardware Design Generation
- **Optical Networking:** Edge/Fog Computing, Machine Learning

## Education

### Tokyo Tech (Tokyo Institute of Technology)

M.E. IN INFORMATION AND COMMUNICATIONS ENGINEERING. ADVISOR IS HIROKI NAKAHARA.

Tokyo, Japan  
Apr. 2018 - Mar. 2020

### Tokyo Tech (Tokyo Institute of Technology)

B.E. IN COMPUTER SCIENCE. ADVISOR IS HIROKI NAKAHARA.

Tokyo, Japan  
Apr. 2016 - Mar. 2018

### Ichinoseki National College of Technology

ASSOC. B.E. IN ENGINEERING. ADVISOR IS KOJI OBOKATA.

Iwate, Japan  
Apr. 2010 - Mar. 2015

## Work Experience

### Researcher at NTT Network Innovation Laboratories

RESEARCH OPTICAL NETWORKING IN SUPPORT OF BOTH EDGE/FOG COMPUTING AND HIGH-PERFORMANCE COMPUTING.

Yokosuka, Japan  
Apr. 2020 - Now

### Intern at Preferred Networks Inc.

RESEARCHED FINE-GRAINED DATAFLOW ACCELERATOR FOR CNN INFERENCE.

Tokyo, Japan  
Aug. 2019 - Sep. 2019

### Intern at SONY Corp.

DEVELOPED AN FPGA-BASED ACCELERATOR FOR A PROPRIETARY NEURAL NETWORK MODEL, AND CONTRIBUTED TO THE OPEN-SOURCE PROJECT NEURAL NETWORK LIBRARIES.

Tokyo, Japan  
Aug. 2018 - Sep. 2018

### Research Assistant at Nakahara Lab, Tokyo Institute of Technology

CONTRIBUTED TO THE OPEN-SOURCE PROJECT GUINNESS.

Tokyo, Japan  
Apr. 2017 - Mar. 2020

## Awards and Scholarships

### INTERNATIONAL

- |      |  |                           |
|------|--|---------------------------|
| 2019 | <b>Best Paper Award Runner-up</b> , IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) | Nanyang Avenue, Singapore |
| 2019 | <b>Iron Award</b> , InnovateFPGA Global Design Contest (APJ Regional Competition)  | Tokyo, Japan              |

### DOMESTIC

- |      |   |              |
|------|---|--------------|
| 2020 | <b>Half Payment Exemption of Master's Scholarship of Japan Student Services Organization for Outstanding Students</b> | Tokyo, Japan |
| 2019 | <b>IEICE RECONF Young Presentation Award</b>  | Tokyo, Japan |
| 2019 | <b>Obtained Fixters Corp. Scholarship for Outstanding STEM Students</b>   | Tokyo, Japan |
| 2018 | <b>IPSJ ARC Young Presentation Award</b>  | Tokyo, Japan |
| 2014 | <b>FUJITSU Corp. Award</b> , 25th National College of Technology Programming Contest                                  | Iwate, Japan |

## Publications

### JOURNAL (PEER REVIEW)

- (Invited)**Masayuki Shimoda**, Youki Sada, Hiroki Nakahara: FPGA-based Inter-layer Pipelined Accelerators for Filter-wise Weight-balanced Sparse Fully Convolutional Networks with Overlapped Tiling, J Sign Process Syst, (in review), 2020.
- **Masayuki Shimoda**, Youki Sada, Ryosuke Kuramochi, Shimpei Sato, Hiroki Nakahara: SENTEI: Filter-wise Pruning with Distillation Towards Efficient Sparse Convolutional Neural Network Accelerators, IEICE Transactions, (to be published), 2020.

- Hiroki Nakahara,Haruyoshi Yonekawa,Tomoya Fujii,**Masayuki Shimoda**,Shimpei Sato: GUINNESS: A GUI Based Binarized Deep Neural Network Framework for Software Programmers, IEICE Transactions, 102-D, 1003-1011, 2019 [URL].
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera for Moving Object Surveillance on an FPGA, IEICE Transactions, 102-D, 1020-1028, 2019 [URL].
- Koji Obokata, Genki Oniyanagi, Kenta Sato, **Masayuki Shimoda**,Hiroki Chiba: Development of a Consensus Building System to Support Community Planning that Centers on Information Sharing Using the Map, Theory and applications of GIS, vol. 24, no. 2, pp. 115–124, 2016 (in Japanese)[URL].

## CONFERENCE (PEER REVIEW)

- Naoto Soga,Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Simpei Sato and Hiroki Nakahara: Fast Monocular Depth Estimation on an FPGA, IPDPS Workshop (RAW), (to be appear), 2020.
- Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Hiroki Nakahara: A Dataflow Pipelining Architecture for Tile Segmentation with a Sparse MobileNet on an FPGA, FPT, 2019 [URL].
- Ryosuke Kyuramochi,**Masayuki Shimoda**,Youki Sada,Shimpei Sato,Hiroki Nakahara: FPGA-based Accurate Pedestrian Detection with Thermal Camera for Surveillance System, ReConFig, 2019 [URL].
- **Masayuki Shimoda**,Hiroki Nakahara: A Deep Neuro-Fuzzy for False Decision Prevention on an FPGA, SASIMI, 56 - 61, 2019 [URL].
- Ryosuke Kuramochi,Youki Sada,**Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Many Universal Convolution Cores for Ensemble Sparse Convolutional Neural Networks, MCSoc, 2019 [URL].
- Hiroki Nakahara,Youki Sada,**Masayuki Shimoda**,Kouki Sayama,Akira Jinguji,Shimpei Sato: FPGA-based Training Accelerator Utilizing Sparseness of Convolutional Neural Network, FPL, 2019 [URL].
- **Masayuki Shimoda**,Youki Sada,Ryosuke Kuramochi,Hiroki Nakahara: An FPGA implementation of Real-time Object Detection with a Thermal Camera, FPL, 2019 [URL].
- **Masayuki Shimoda**,Youki Sada,Hiroki Nakahara: Filter-Wise Pruning Approach to FPGA Implementation of Fully Convolutional Network for Semantic Segmentation, ARC, 371-386, 2019 [URL].
- Hiroki Nakahara,Akira Jinguji,**Masayuki Shimoda**,Shimpei Sato: An FPGA-based Fine Tuning Accelerator for a Sparse CNN, FPGA, 186, 2019 [URL].
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Demonstration of FPGA-Based You Only Look Once Version2 (YOLOv2), FPL, 457-458, 2018 [URL].
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Demonstration of Object Detection for Event-Driven Cameras on FPGAs and GPUs, FPL, 461-462, 2018 [URL].
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Tri-State Weight Convolutional Neural Network for an FPGA: Applied to YOLOv2 Object Detector, FPT, 298-301, 2018 [URL].
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera on an FPGA, HEART, 10:1-10:6, 2018 [URL].
- Hiroyuki Nakahara,Haruyoshi Yonekawa,Tomoya Fujii,**Masayuki Shimoda**,Simpei Sato: A demonstration of the GUINNESS: A GUI based neural NETwork Synthesizer for an FPGA, FPL, 1, 2017 [URL].
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: All binarized convolutional neural network and its implementation on an FPGA, ICFPT, 291-294, 2017 [URL].

## Qualification and Skills

- **TOEIC:** 790 (Apr.2017)
- **Design Tools:** Xilinx Vitis, SDSoc, Vivado HLS, Vivado
- **Programming Languages:** C/C++, Python3, Go, Verilog
- **Operating Systems:** Ubuntu, macOS

## Activities

- 2019 **Volunteer at the 24th Asia and South Pacific Design Automation Conference (ASP-DAC)**
- 2017 **Won award for excellence in Wantedly Inc. Data Analysis Contest**
- 2016 **Participated in Hackathon at Tokyo Institute of Technology**

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