

# Masayuki Shimoda

✉ moshimoshimoshida@gmail.com | 🏠 shimoshida.github.io | 📷 shimoshida | 🌐 masayuki-shimoda | 🎓 Masayuki Shimoda

## Research Interests

- **FPGA-based Accelerators:** Application-specific Architectures
- **Design Automation:** Design Space Exploration and Hardware Design Generation
- **Optimization via Reinforcement Learning:** Especially, Routing Optimization

## Education

### Institute of Science Tokyo

D.E. IN INFORMATION AND COMMUNICATIONS ENGINEERING. ADVISOR IS ATSUSHI TAKAHASHI.

Tokyo, Japan  
Apr. 2022 - Dec. 2024

### Tokyo Institute of Technology

M.E. IN INFORMATION AND COMMUNICATIONS ENGINEERING. ADVISOR IS HIROKI NAKAHARA.

Tokyo, Japan  
Apr. 2018 - Mar. 2020

### Tokyo Institute of Technology

B.E. IN COMPUTER SCIENCE. ADVISOR IS HIROKI NAKAHARA.

Tokyo, Japan  
Apr. 2016 - Mar. 2018

### Ichinoseki National College of Technology

ASSOC. B.E. IN ENGINEERING. ADVISOR IS KOJI OBOKATA.

Iwate, Japan  
Apr. 2010 - Mar. 2015

## Work Experience

### Assistant Professor at Institute of Science Tokyo

RESEARCH EDA (ELECTRONIC DESIGN AUTOMATION).

Tokyo, Japan  
Jan. 2025 - Now

### Software Engineer at rinna Co., Ltd.

DEVELOPED BACKEND ML APIS FOR CHARARU.

Tokyo, Japan  
Jun. 2021 - Jan. 2023

### Researcher at NTT Network Innovation Laboratories

RESEARCH ROUTING AND SPECTRUM ASSIGNMENT USING REINFORCEMENT LEARNING FOR OPTICAL NETWORKS.

Yokosuka, Japan  
Apr. 2020 - Jun. 2021

### Intern at Preferred Networks Inc.

RESEARCHED FINE-GRAINED DATAFLOW ACCELERATOR FOR CNN INFERENCE.

Tokyo, Japan  
Aug. 2019 - Sep. 2019

### Intern at SONY Corp.

DEVELOPED AN FPGA-BASED ACCELERATOR FOR A PROPRIETARY NEURAL NETWORK MODEL, AND CONTRIBUTED TO THE OPEN-SOURCE PROJECT NEURAL NETWORK LIBRARIES.

Tokyo, Japan  
Aug. 2018 - Sep. 2018

### Research Assistant at Nakahara Lab, Tokyo Institute of Technology

CONTRIBUTED TO THE OPEN-SOURCE PROJECT GUINNESS.

Tokyo, Japan  
Apr. 2017 - Mar. 2020

### Intern at So-net Media Networks Co.,Ltd. (SMN Corporation)

DEVELOPED CRAWLER(PYTHON) AND IN-HOUSE SYSTEM(JAVASCRIPT(JQUERY), JAVA(SPRING)), AND CONDUCTED LANDING PAGE OPTIMIZATION(PYTHON(SCIKIT-LEARN))

Tokyo, Japan  
Nov. 2016 - Mar. 2018

### Intern at Fringe81 Inc. (Unipos Inc.)

DESIGNED AND DEVELOPED THE BACKEND API FOR THE APPLICATION SHINKURU BY USING TYPESCRIPT WITH BOTH DOMAIN DRIVEN DESIGN AND CLEAN ARCHITECTURE.

Tokyo, Japan  
Aug. 2016 - Sep. 2016

## Awards and Scholarships

### INTERNATIONAL

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|------|--|------------------------------|
| 2019 | <b>Best Paper Award Runner-up</b> , IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) | Nanyang Avenue,<br>Singapore |
| 2019 | <b>Iron Award</b> , InnovateFPGA Global Design Contest (APJ Regional Competition)  | Tokyo, Japan                 |

### DOMESTIC

2020	<b>Half Payment Exemption of Master's Scholarship of Japan Student Services Organization for Outstanding Students</b>	Tokyo, Japan
2019	<b>IEICE RECONF Young Presentation Award</b>	Tokyo, Japan
2019	<b>Obtained Fixters Corp. Scholarship for Outstanding STEM Students</b>	Tokyo, Japan
2018	<b>IPJS ARC Young Presentation Award</b>	Tokyo, Japan
2014	<b>FUJITSU Corp. Award</b> , 25th National College of Technology Programming Contest	Iwate, Japan

## Skills

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- **FPGA Design Tools:** SDSoc, Vivado HLS
- **Programming Languages:** C/C++, Python, Go
- **MLOps:** NVIDIA Triton Server, NVIDIA FasterTransformer, AzureML
- **Others:** Docker, Kubernetes (Helm, Istio), GitHub Actions, Argo CD
- **Operating Systems:** Ubuntu, macOS

## Qualification

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- **TOEIC:** 790 (Apr.2017)
- **Azure:** AZ-900, AI-900, DP-100, AZ-104
- **Others:** CKAD, CKA
- **Coursera:** Reinforcement Learning, VLSI CAD Part II: Layout

## Publications

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### JOURNAL (PEER REVIEW)

- **Masayuki Shimoda**, Atsushi Takahashi: Gridless Gap Channel Routing to Minimize Wirelength, IPSJ Trans. on System LSI Design Methodology, Vol.18, 2025. [\[URL\]](#).
- Zezhong Wang, **Masayuki Shimoda**, Atsushi Takahashi: SDG channel routing to minimize wirelength for generalized channel, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Communications and Computer Sciences, 2025..
- **Masayuki Shimoda**, Atsushi Takahashi: Gridless gap channel routing with variable-width wires, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2024. [\[URL\]](#).
- Takafumi Tanaka, **Masayuki Shimoda**: Pre- and post-processing techniques for reinforcement-learning-based routing and spectrum assignment in elastic optical networks, J. Opt. Commun. Netw. 15, 1019-1029, 2023 [\[URL\]](#).
- (Invited) **Masayuki Shimoda**, Youki Sada, Hiroki Nakahara: FPGA-based Inter-layer Pipelined Accelerators for Filter-wise Weight-balanced Sparse Fully Convolutional Networks with Overlapped Tiling, J Sign Process Syst, 1-14, 2021 [\[URL\]](#).
- **Masayuki Shimoda**, Youki Sada, Ryosuke Kuramochi, Shimpei Sato, Hiroki Nakahara: SENTEI: Filter-wise Pruning with Distillation Towards Efficient Sparse Convolutional Neural Network Accelerators, IEICE Transactions, Vol.E103-D, pp.2463-2470, 2020 [\[URL\]](#).
- Hiroki Nakahara, Haruyoshi Yonekawa, Tomoya Fujii, **Masayuki Shimoda**, Shimpei Sato: GUINNESS: A GUI Based Binarized Deep Neural Network Framework for Software Programmers, IEICE Transactions, Vol.E102-D, pp.1003-1011, 2019 [\[URL\]](#).
- **Masayuki Shimoda**, Shimpei Sato, Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera for Moving Object Surveillance on an FPGA, IEICE Transactions, Vol.E102-D, pp.1020-1028, 2019 [\[URL\]](#).
- Koji Obokata, Genki Oniyanagi, Kenta Sato, **Masayuki Shimoda**, Hiroki Chiba: Development of a Consensus Building System to Support Community Planning that Centers on Information Sharing Using the Map, Theory and applications of GIS, vol. 24, no. 2, pp. 115-124, 2016 (in Japanese) [\[URL\]](#).

### CONFERENCE (PEER REVIEW)

- **Masayuki Shimoda**, Atsushi Takahashi, Kosuke Yanagidaira, Mikiko Hirai, Toshikazu Watanabe, Toshimitsu Iwasawa, Chikaaki Kodama: Gap Channel Routing with Fixed Wires, IEEE International Symposium on Circuits and Systems (ISCAS), 2025
- **Masayuki Shimoda**, Atsushi Takahashi: Wirelength Minimization by Gap Swap-Flip in Gridless Gap Channel Routing, IEEE International SoC Design Conference (ISOCC), 2024 [\[URL\]](#).
- Zezhong Wang, **Masayuki Shimoda**, Atsushi Takahashi: BCA channel routing to minimize wirelength for generalized channel problem, IEEE International Symposium on Circuits and Systems (ISCAS), 2024 [\[URL\]](#).

- **Masayuki Shimoda**,Takafumi Tanaka: Mask RSA: End-To-End Reinforcement Learning-based Routing and Spectrum Assignment in Elastic Optical Networks, ECOC, 2021 [\[URL\]](#).
- Takafumi Tanaka, **Masayuki Shimoda**: Impact of Operational Mode Selection and Grooming Policies on Auxiliary Graph-Based Multi-layer Network Planning, ECOC, 2021 [\[URL\]](#).
- **Masayuki Shimoda**,Takafumi Tanaka: Deep Reinforcement Learning-based Spectrum Assignment with Multi-metric Reward Function and Assignable Boundary Slot Mask, OECC, 2021 [\[URL\]](#).
- Naoto Soga,Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Simpei Sato and Hiroki Nakahara: Fast Monocular Depth Estimation on an FPGA, IPDPS Workshop (RAW), 2020 [\[URL\]](#).
- Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Hiroki Nakahara: A Dataflow Pipelining Architecture for Tile Segmentation with a Sparse MobileNet on an FPGA, FPT, 2019 [\[URL\]](#).
- Ryosuke Kyuramochi,**Masayuki Shimoda**,Youki Sada,Shimpei Sato,Hiroki Nakahara: FPGA-based Accurate Pedestrian Detection with Thermal Camera for Surveillance System, ReConFig, 2019 [\[URL\]](#).
- Ryosuke Kuramochi,Youki Sada,**Masayuki Shimoda**,Shimpei Satoo,Hiroki Nakahara: Many Universal Convolution Cores for Ensemble Sparse Convolutional Neural Networks, MCSoc, 2019 [\[URL\]](#).
- Hiroki Nakahara,Youki Sada,**Masayuki Shimoda**,Kouki Sayama,Akira Jinguji,Shimpei Sato: FPGA-based Training Accelerator Utilizing Sparseness of Convolutional Neural Network, FPL, 2019 [\[URL\]](#).
- **Masayuki Shimoda**,Youki Sada,Ryosuke Kuramochi,Hiroki Nakahara: An FPGA implementation of Real-time Object Detection with a Thermal Camera, FPL, 2019 [\[URL\]](#).
- **Masayuki Shimoda**,Youki Sada,Hiroki Nakahara: Filter-Wise Pruning Approach to FPGA Implementation of Fully Convolutional Network for Semantic Segmentation, ARC, 371-386, 2019 [\[URL\]](#).
- Hiroki Nakahara,Akira Jinguji,**Masayuki Shimoda**,Shimpei Sato: An FPGA-based Fine Tuning Accelerator for a Sparse CNN, FPGA, 186, 2019 [\[URL\]](#).
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Demonstration of FPGA-Based You Only Look Once Version2 (YOLOv2), FPL, 457-458, 2018 [\[URL\]](#).
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Demonstration of Object Detection for Event-Driven Cameras on FPGAs and GPUs, FPL, 461-462, 2018 [\[URL\]](#).
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Tri-State Weight Convolutional Neural Network for an FPGA: Applied to YOLOv2 Object Detector, FPT, 298-301, 2018 [\[URL\]](#).
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera on an FPGA, HEART, 10:1-10:6, 2018 [\[URL\]](#).
- Hiroyuki Nakahara,Haruyoshi Yonekawa,Tomoya Fujii,**Masayuki Shimoda**,Simpei Sato: A demonstration of the GUINNESS: A GUI based neural NETwork Synthesizer for an FPGA, FPL, 1, 2017 [\[URL\]](#).
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: All binarized convolutional neural network and its implementation on an FPGA, ICFPT, 291-294, 2017 [\[URL\]](#).