Masayuki **Shimoda**

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Research Interests

- **FPGA-based Accelerators:** Application-specific Architectures
- **Design Automation:** Design Space Exploration and Hardware Design Generation
- **Optical Networks:** Machine Learning in Optical Systems and Networks

Education

Tokyo Tech (Tokyo Institute of Technology) — *Tokyo, Japan*
M.E. in Information and Communications Engineering. Advisor is Hiroki Nakahara. — *Apr. 2018 - Mar. 2020*

Tokyo Tech (Tokyo Institute of Technology) — *Tokyo, Japan*
B.E. in Computer Science. Advisor is Hiroki Nakahara. — *Apr. 2016 - Mar. 2018*

Ichinoseki National College of Technology — *Iwate, Japan*
Assoc. B.E. in Engineering. Advisor is Koji Obokata. — *Apr. 2010 - Mar. 2015*

Work Experience

Researcher at NTT Network Innovation Laboratories — *Yokosuka, Japan*
Research routing and spectrum assignment using reinforcement learning for optical networks. — *Apr. 2020 - Now*

Intern at Preferred Networks Inc. — *Tokyo, Japan*
Researched fine-grained dataflow accelerator for CNN Inference. — *Aug. 2019 - Sep. 2019*

Intern at SONY Corp. — *Tokyo, Japan*
Developed an FPGA-based accelerator for a proprietary neural network model, and contributed to the open-source project Neural Network Libraries. — *Aug. 2018 - Sep. 2018*

Research Assistant at Nakahara Lab, Tokyo Institute of Technology — *Tokyo, Japan*
Contributed to the open-source project GUINNESS. — *Apr. 2017 - Mar. 2020*

Awards and Scholarships

International

2019	**Best Paper Award Runner-up**, IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)	*Nanyang Avenue, Singapore*
2019	**Iron Award**, InnovateFPGA Global Design Contest (APJ Regional Competition)	*Tokyo, Japan*

Domestic

2020	**Half Payment Exemption of Master's Scholarship of Japan Student Services Organization for Outstanding Students**	*Tokyo, Japan*
2019	**IEICE RECONF Young Presentation Award**	*Tokyo, Japan*
2019	**Obtained Fixters Corp. Scholarship for Outstanding STEM Students**	*Tokyo, Japan*
2018	**IPSJ ARC Young Presentation Award**	*Tokyo, Japan*
2014	**FUJITSU Corp. Award**, 25th National College of Technology Programming Contest	*Iwate, Japan*

Publications

Journal (peer review)

- (Invited)**Masayuki Shimoda**,Youki Sada,Hiroki Nakahara: FPGA-based Inter-layer Pipelined Accelerators for Filter-wise Weight-balanced Sparse Fully Convolutional Networks with Overlapped Tiling, J Sign Process Syst, 1-14, 2021 **[URL]**.
- **Masayuki Shimoda**,Youki Sada,Ryosuke Kuramochi,Shimpei Sato,Hiroki Nakahara: SENTEI: Filter-wise Pruning with Distillation Towards Efficient Sparse Convolutional Neural Network Accelerators, IEICE Transactions, Vol.E103-D, pp.2463-2470, 2020**[URL]**.

- Hiroki Nakahara,Haruyoshi Yonekawa,Tomoya Fujii,**Masayuki Shimoda**,Shimpei Sato: GUINNESS: A GUI Based Binarized Deep Neural Network Framework for Software Programmers, IEICE Transactions, Vol.E102-D, pp.1003-1011, 2019 **[URL]**.
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera for Moving Object Surveillance on an FPGA, IEICE Transactions, Vol.E102-D, pp.1020-1028, 2019 **[URL]**.
- Koji Obokata, Genki Oniyanagi, Kenta Sato, **Masayuki Shimoda**,Hiroki Chiba: Development of a Consensus Building System to Support Community Planning that Centers on Information Sharing Using the Map, Theory and applications of GIS, vol. 24, no. 2, pp. 115–124, 2016 (in Japanese)**[URL]**.

Conference (peer review)

- **Masayuki Shimoda**,Takafumi Tanaka: Deep Reinforcement Learning-based Spectrum Assignment with Multi-metric Reward Function and Assignable Boundary Slot Mask, OECC, 2021(to appear).
- Naoto Soga,Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Simpei Sato and Hiroki Nakahara: Fast Monocular Depth Estimation on an FPGA, IPDPS Workshop (RAW), 2020 **[URL]**.
- Youki Sada,**Masayuki Shimoda**,Akira Jinguji,Hiroki Nakahara: A Dataflow Pipelining Architecture for Tile Segmentation with a Sparse MobileNet on an FPGA, FPT, 2019 **[URL]**.
- Ryosuke Kyuramochi,**Masayuki Shimoda**,Youki Sada,Shimpei Sato,Hiroki Nakahara: FPGA-based Accurate Pedestrian Detection with Thermal Camera for Surveillance System, ReConFig, 2019 **[URL]**.
- **Masayuki Shimoda**,Hiroki Nakahara: A Deep Neuro-Fuzzy for False Decision Prevention on an FPGA, SASIMI, 56 - 61, 2019 **[URL]**.
- Ryosuke Kuramochi,Youki Sada,**Masayuki Shimoda**,Shimpei Satoo,Hiroki Nakahara: Many Universal Convolution Cores for Ensemble Sparse Convolutional Neural Networks, MCSoC, 2019 **[URL]**.
- Hiroki Nakahara,Youki Sada,**Masayuki Shimoda**,Kouki Sayama,Akira Jinguji,Shimpei Sato: FPGA-based Training Accelerator Utilizing Sparseness of Convolutional Neural Network, FPL, 2019 **[URL]**.
- **Masayuki Shimoda**,Youki Sada,Ryosuke Kuramochi,Hiroki Nakahara: An FPGA implementation of Real-time Object Detection with a Thermal Camera, FPL, 2019 **[URL]**.
- **Masayuki Shimoda**,Youki Sada,Hiroki Nakahara: Filter-Wise Pruning Approach to FPGA Implementation of Fully Convolutional Network for Semantic Segmentation, ARC, 371-386, 2019 **[URL]**.
- Hiroki Nakahara,Akira Jinguji,**Masayuki Shimoda**,Shimpei Sato: An FPGA-based Fine Tuning Accelerator for a Sparse CNN, FPGA, 186, 2019 **[URL]**.
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Demonstration of FPGA-Based You Only Look Once Version2 (YOLOv2), FPL, 457-458, 2018 **[URL]**.
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Demonstration of Object Detection for Event-Driven Cameras on FPGAs and GPUs, FPL, 461-462, 2018 **[URL]**.
- Hiroki Nakahara,**Masayuki Shimoda**,Shimpei Sato: A Tri-State Weight Convolutional Neural Network for an FPGA: Applied to YOLOv2 Object Detector, FPT, 298-301, 2018 **[URL]**.
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: Power Efficient Object Detector with an Event-Driven Camera on an FPGA, HEART, 10:1-10:6, 2018 **[URL]**.
- Hiroyuki Nakahara,Haruyoshi Yonekawa,Tomoya Fujii,**Masayuki Shimoda**,Simpei Sato: A demonstration of the GUINNESS: A GUI based neural NEtwork SyntheSizer for an FPGA, FPL, 1, 2017 **[URL]**.
- **Masayuki Shimoda**,Shimpei Sato,Hiroki Nakahara: All binarized convolutional neural network and its implementation on an FPGA, ICFPT, 291-294, 2017 **[URL]**.

Qualification and Skills

- **TOEIC:** 790 (Apr.2017)
- **Design Tools:** Xilinx Vitis, SDSoC, Vivado HLS, Vivado
- **Programming Languages:** C/C++, Python3, Go, Verilog
- **Operating Systems:** Ubuntu, macOS

Activities

2019	**Volunteer at the 24th Asia and South Pacific Design Automation Conference (ASP-DAC)**	*Tokyo, Japan*
2017	**Won award for excellence in Wantedly Inc. Data Analysis Contest**	*Tokyo, Japan*
2016	**Participated in Hackathon at Tokyo Institute of Technology**	*Tokyo, Japan*