60V/41.1V Buck Converter Design for 3s2p Battery Configuration (June 2021)

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***Abstract*—A DC-DC asynchronous buck converter with 60V input and 41.1V output was designed to charge a 3s2p battery bank. In the power stage design, the buck converter consists of a PMOS as the high-side switch and a Schottky diode as the low-side switch. An LTC3824 IC was utilized to handle PWM generation for the switches, and error amplification. Simulation shows that the output voltage has an average value of 41.50V with 0.07% ripple. Furthermore, fabrication of the design and testing are recommended to consider temperature variability.**

I. Design Specifications

THE design problem requires us to charge a 3s2p battery bank using an asynchronous buck converter. Each cell in the configuration is an LC-P127R2P lead acid battery from Panasonic. An individual cell can be charged using an initial current of 1.08A or smaller, and a 13.6V to 13.8V control voltage [1]. Thus, through Kirchhoff's Voltage Law and Current Law, the 3s2p configuration will require an average of 41.1 V and will draw a maximum current of 2.16A.

In the power stage design, to draw some margins for the maximum output current of the power supply, the buck converter is designed to have an output current of 2.00A, and a regulated output voltage of 41.1V with an allowable 10% ripple (39.045V to 43.155V output). The input parameter is 60V with an assumed ripple of 5%. Moreover, the inductor current has a maximum allowable ripple equal to $5\%I_{o,max}$.

On the other hand, the driver circuit is required to be driven at 350kHz.

Table I summarizes the design specifications of the buck converter.

TABLE I
DESIGN SPECIFICATIONS

Parameters	Min.	Ave.	Max.
Input Voltage (V)	58.5	60	61.5
Output Voltage (V)	39.405	41.1	43.155
Output Current (A)	1.90	2.00	2.10
Inductor Current (A)	1.9475	2.00	2.0525
Switching Freq. (kHz)	-	350	-

II. Methodology

We divide this section into two subsections: the power stage design, and the driver circuit design. In both subsections, we discuss the selection of components required to achieve the desired specifications.

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A. Power Stage Design

Figure 1 shows the schematic of the power stage of the buck converter.

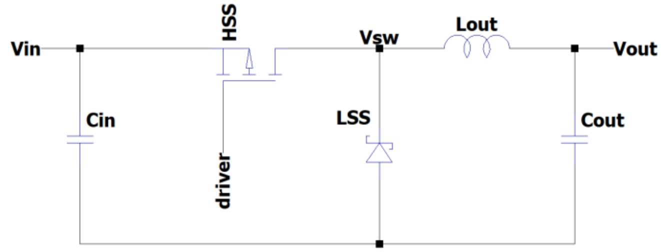

Fig. 1. Buck converter power stage schematic

Before the selection of component for power stage, we first identify the duty cycle (D) of the switching voltage (V_{sw}). According to [2], this is given by

$$D = \frac{V_{out}+v_D}{V_{in}+v_D} \quad (1)$$

where v_D the voltage across the power diode to be used as the low-side switch (LSS). In this design, we assumed $v_D = 0.75V$ since we will later use a diode with this forward voltage. Hence, $D \approx 68.89\%$

1) Inductor Selection

According to [3], the minimum inductance of the output inductor is given by

$$L_{min} = \frac{D(v_i - v_o)}{\Delta i_{L,p-p} f_{sw}} \quad (2)$$

Hence, an inductor of at least $354.29\mu H$ should be used. In the design, we used an AGP4233-474 inductor with rated inductance of $470\mu H$ from Coilcraft. The data sheet [4] shows the following characteristics:

TABLE II
INDUCTOR CHARACTERISTICS

Specifications	Values
Inductance (μH)	470
Core	Ferrite
Tolerance (%)	20
I_{sat} (A)	3
I_{rms} (A)	12.4
Max DC resistance ($m\Omega$)	11.55

The inductor has $I_{sat} > I_{L,max}$ and $I_{rms} > I_{out,max}$. Furthermore, the DC resistance of the inductor has insignificant effect to the output due to its low value with respect to the load. Therefore, this inductor qualifies as the output for the power stage.

2) Output Capacitor Selection

The output capacitor in the power stage controls the ripple of the output voltage. Since the design requires the maximum allowable ripple to be 10%, the capacitor must satisfy the inequality [5]

$$C_{out} > \frac{\Delta i_{L,p-p}}{8 f_{sw}\, \Delta v_{out,p-p}} \tag{3}$$

Computation shows the capacitor must be at least 187.5 nF. For lower ripple in the design, we used a single $1\mu F$ X7R capacitor from KEMET. Below are its characteristics from the data sheet [6].

TABLE III
OUTPUT CAPACITOR SPECIFICATIONS

Specifications	Values
Part number	C1206C105K5RAC
Capacitance (µF)	1
Tolerance (%)	10%
Voltage Rating (V)	50
Dissipation Factor (%)	2.5%
I_{rms} (A)	3.41

The equivalent series resistance (ESR) of a capacitor is given by

$$ESR = 2\pi f C Q \tag{4}$$

where Q the dissipation factor, f the switching frequency and C the rated capacitance. The computed ESR is approximately $54.978 m\Omega$.

The single capacitor qualifies as the output capacitor due to the following:

i. The capacitor meets the minimum capacitance for the output voltage ripple.
ii. I_{rms} requirement is satisfied since the maximum output current is 2.10A.
iii. Voltage rating of the capacitor is strictly greater than the maximum output voltage.
iv. ESR is insignificant relative to the output load.

3) Input Capacitor Selection

The input capacitor in the buck converter reduces the input voltage ripple such that the input is close to DC. According to [2], the input capacitance must satisfy the following inequality

$$C_{in} > \frac{i_{out,ave}(1-D)D}{\Delta v_{in,p-p} f_{sw}} \tag{5}$$

where $\Delta v_{in,p-p}$ is assumed to be 5% of the input voltage. Thus, the input capacitance must exceed $0.408\mu F$.

The selected capacitors are three identical $0.33\mu F$ X7R capacitors from KEMET. Below are its characteristics [7].

TABLE IV
INPUT CAPACITOR SPECIFICATIONS

Specifications	Values
Part number	C1206C334K1RAC
Capacitance (µF)	0.33
Tolerance (%)	10
Voltage Rating (V)	100
Dissipation Factor (%)	3.5
I_{rms} (A)	0.813

Equation 4 shows the ESR of each input capacitor is about $25.40 m\Omega$.

The input capacitors qualify due to the following reasons.

i. The equivalent capacitance $(0.99\mu F)$ meets the minimum capacitance to handle a 5% input voltage ripple.
ii. Three capacitors are used to satisfy I_{rms} requirement. Note that the buck converter will run a maximum current of 2.0525A.
iii. Voltage rating is strictly more than the input voltage.
iv. The effective ESR $(8.47 m\Omega)$ of the capacitor network is insignificant compared to the load.

4) High Side Switch Selection

For the design, a PMOS is selected as the high-side switch since it is required by the driver circuit. Particularly, the Si7469DP from Vishay Siliconix is used. From the data sheet [8], the MOSFET has the following characteristics.

TABLE V
POWER MOSFET SPECIFICATIONS

Specifications	Values
Part number	Si7469DP
$V_{DS,max}\ (V)$	-80
$R_{DSon,max}\ (m\Omega)$	29
$C_{RSS}\ (pF)$	235
$Q_G\ (nC)$	160

The buck converter has a 0-60V switching voltage. Thus, the transistor satisfies the V_{DS} requirements of the design.

According to [3], dissipation on the MOSFET has two components: conduction loss (P_{cond}) and switching loss (P_{sw}). We also add the gate charging loss of the MOSFET These can be calculated using the following equations.

$$P_{cond} = D\left(i_{out,max}\right)^2 (R_{DSon,max})(1+\delta) \tag{6}$$

$$P_{sw} = 1.7 V_{in}^2 i_{out,max} (C_{RSS}) f_{sw} \tag{7}$$

$$P_{drive} = V_{GS} Q_G f_{sw} \tag{8}$$

where δ the temperature coefficient of R_{DSon} which is assumed the typical value of $0.4\%/°C$. For P_{drive} calculation, note that the driver voltage is clamped at 8V when the supply or input voltage is above 9V [3].

Table VI shows the dissipation of the PMOS.

TABLE VI
DISSIPATION OF POWER MOSFET

Loss component	Dissipation
P_{cond} (mW)	88.454
P_{sw} (mW)	1057.077
P_{drive} (mW)	448
Total loss (W)	1.594

Assuming that all other components are ideal, and the input supplies a real power of 82.2W based on the power requirements of the load, the MOSFET will dissipate less than 2% of the power. The transistor is acceptable if the buck converter should operate above 90% efficiency.

5) *Low Side Switch Selection*

The asynchronous buck converter utilizes a Schottky diode for its low-side switch. In this design, the diode used is the MBRS1100 from ON Semiconductors. The power diode has the following characteristics [9]:

TABLE VII
POWER DIODE CHARACTERISTICS

Characteristics	Values
Forward Voltage (V)	0.75
Max reverse voltage (V)	100
Average Forward Current (A)	1

With the following characteristics, the diode qualifies for the low side switch due to the following reasons.

i. MBRS1100 is a Schottky diode capable of fast switching for power applications.

ii. The maximum reverse voltage rating of the diode is strictly greater than the input voltage.

iii. Average forward current of the diode is at least 10% higher than the maximum diode current ($\sim 653mA$) of the circuit. Note that the maximum diode current is given by

$$I_{D,max} = (1 - D)I_{out,max} \tag{9}$$

iv. Power dissipated by the diode is given by

$$P_D = I_{D,max}V_F \tag{10}$$

Thus, the diode dissipates 490mW of power which is less than 0.6% of the real power supplied by the input. With the PMOS dissipation considered, the buck converter can still operate above 90% efficiency.

6) *Heat Generation of Power Switches*

In this part, we assumed an ambient temperate T_A of $25°C$. The table below lists the maximum operating junction temperature of the components in power stage and the driver IC from their corresponding datasheets [3,4,6,7,8,9].

TABLE VIII
TEMPERATURE CHARACTERISTICS OF COMPONENTS

Component	Max Operating Junction Temperature ($°C$)	Max Junction-Ambient Thermal Resistance ($°C/W$)
Inductor	125	-
Output Capacitor	125	-
Input Capacitor	125	-
Si7649DP	150	24
MBRS1100	175	22
LTC3824	150	-

Hence, the buck converter should operate at junction temperature less than $125°C$. The operating junction temperature of the PCB can be computed by

$$T_J = P_D R_{\theta JA,D} + P_{PMOS} R_{\theta JA,PMOS} + T_A \tag{11}$$

which is approximately $74.04\,°C$. Thus, $T_j < 125°C$ due to the low power dissipation of the switches. This saves the design the need for heat sinks.

B. *Driver Circuit Design*

The buck converter's PWM generator and error amplifier are handled by the LTC3824 from Linear Technology. According to the datasheet [3], the integrated circuit consists of ten pins: GND, MODE, R_{set}, V_C, V_{FB}, SS, SENSE, V_{CC}, GATE, and CAP. The IC also has the following features:

i. Burst Mode operation can be configured to enhance light load efficiency. In the design, we will not be using this mode. Thus, the MODE pin is grounded.

ii. Switching frequency can be programmed. This is controlled by a resistor connected to R_{set}. Figure 2 shows the graph for the driver frequency.

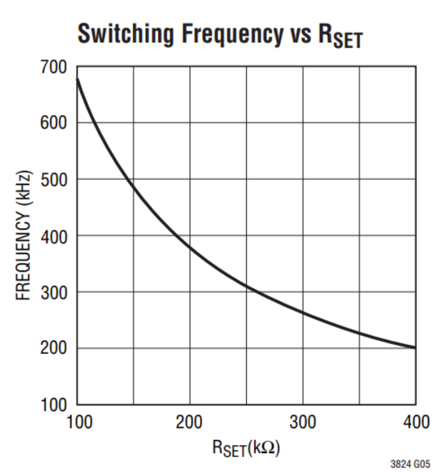

Fig. 2. Switching Frequency vs. R_{set} [3]

To set the driver at 350kHz, the resistance R_{set} should be set to approximately $220k\Omega$. In the design, we used a $221k\Omega$ resistor for R_{set}.

iii. Soft-start is programmable. Soft-start or the time for the output to ramp-up is controlled by a function dependent to the capacitor connected at the SS pin to GND. This is given by

$$t_{out,ramp-up} = C_{SS}\left(\frac{0.8V}{5\mu A}\right) \quad (12)$$

We choose a $0.01\mu F$ capacitor since the design is not strict of the ramp-up rate of the buck converter, and we intend to charge lead acid batteries for hours.

iv. Current limit of the buck converter can be controlled using a sensing resistor R_S connected from the input to SENSE. The current limit is given by

$$I_{limit} = \frac{100mV}{R_S} \quad (13)$$

Since the buck converter is intended to deliver a maximum charging current of 2.16A, the current limit is set at 4A with $R_S = 25m\Omega$. While multiple standard resistors in parallel can be used to attain the resistance, a current sensing resistor is used in the design, particularly the RCWE120625 from Vishay.

v. Output voltage is controlled by a resistor divider at the error amplifier from the power stage to the V_{FB} pin. The ratio of the resistor divider $\frac{R_{FB,1}}{R_{FB,2}}$ can be deduced from the equation

$$V_{out} = 0.8V\left(1 + \frac{R_{FB,1}}{R_{FB,2}}\right) \quad (14)$$

Thus, $\frac{R_{FB,1}}{R_{FB,2}} = \frac{403}{8}$. In the design, we used $R_{FB,1} = 200k\Omega$ and $R_{FB,2} = 3.92k\Omega$. A 100pF capacitor is connected parallel to $R_{FB,1}$ to reduce ripples into the feedback pin. This configuration is similar to an RC network in the Type III compensator.

While these features also discuss the use of some pins of the IC, all other pins are utilized for I/O, necessity, and internal regulation. V_{CC} acts as the supply pin of the IC and is connected at the input of the buck regulator. Meanwhile, the GATE pin delivers PWM signals and is directly connected to the PMOS. Furthermore, V_C is connected to an RC network to keep the pin above 25mV and prevent micropower shutdown [3]. The CAP pin is connected at V_{CC} with a $0.1\mu F$ capacitor to bypass the internal regulator for biasing the gate driver circuitry [3].

Table IX shows the passive components utilized in the driver circuit, and some of their characteristics [6, 7, 10, 11]

TABLE IX
PASSIVE COMPONENTS OF THE DRIVER

Components	Values	Rated Voltage	Part Number
SS capacitor (C_{ss})	$0.75\mu F$	100V	C1206C684K3RAC
CAP capacitor (C_{cap})	$0.1\mu F$	100V	C1206C104K1RAC
Error amplifier capacitor	$100pF$	50V	GCM0335C1H101
Sensing resistor	$25m\Omega$	-	RCWE120625

Figure 3 shows the driver circuit design using the LTC3824 IC. A detailed schematic of the driver circuit with the power stage design can also be seen at Appendix A.

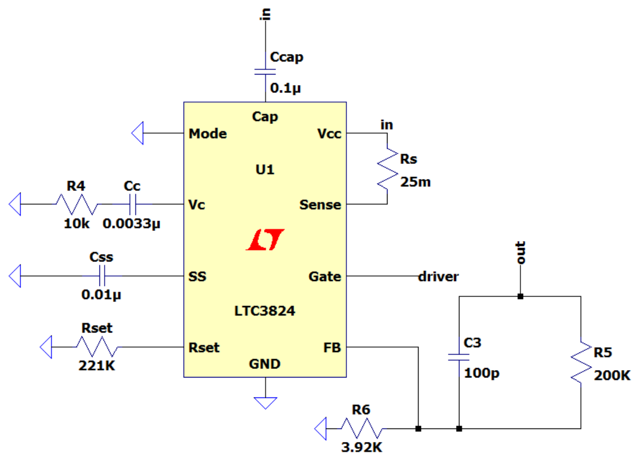

Fig. 3. Driver circuit schematic

III. RESULTS AND ANALYSIS

In this section, we discuss the results of the simulation of the design in different charging currents: 2.16A for 100% current, 1.62A for 75%, 1.05A for 50%, and 0.216A for 10%. Standard models from LTSpice were used to simulate most components of the buck regulator. For the sensing resistor of LTC3824, the resistor is modelled using the characteristics from its datasheet.

A. Inductor Current

Figure 4 shows the steady-state inductor current of the buck converter at different charging currents.

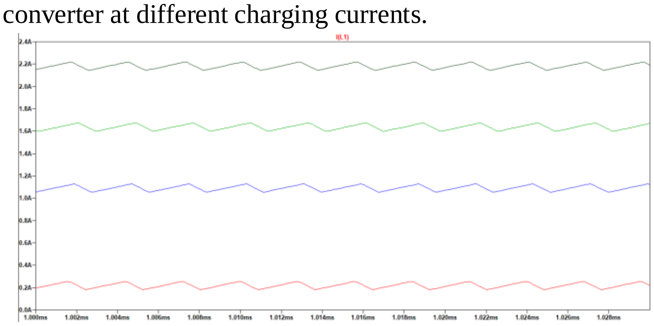

Fig. 4. Inductor current at 100% charging current (black), at 75% charging current (green), at 50% charging current (blue), and at 10% charging current (red).

It can be observed from the plot the output inductor current ripple hardly varies for all charging currents. However, Table X shows that at higher precision, very little differences with variance $\sim 1.5 \times 10^{-6}$ can be observed.

TABLE X
INDUCTOR CURRENT CHARACTERISTICS

Charging current (%)	Average current (A)	Percent error of Average current (%)	Current Ripple (mA)
100	2.18132	0.987	77.0731
75	1.63604	0.990	77.0426
50	1.09076	0.996	76.8298
10	0.218329	1.078	74.1626

Moreover, the error on average inductor current at each charging current is approximately 1%. This small error may be due to the inaccuracy of the resistor divider used for error amplifier. Nonetheless, the inductor ripple is within the acceptable 5% of $I_{out,max}$ (108mA) regardless of the charging current.

B. *Output Voltage*

Figure 5 shows the output voltage of the buck converter at different charging current.

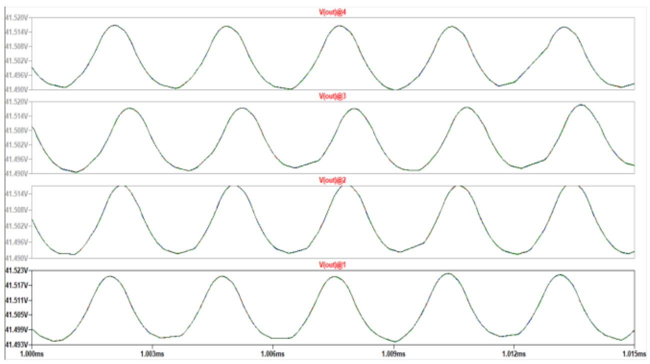

Fig. 5. Output voltage of the buck converter at 100%, 75%, 50%, and 10% charging current (top to bottom).

TABLE XI
OUTPUT VOLTAGE CHARACTERISTICS

Charging current (%)	Average voltage (V)	Percent error of average voltage (%)	Ripple (%)
100	41.5021	0.978	0.072222
75	41.5022	0.979	0.0727786
50	41.5023	0.979	0.0746355
10	41.5052	0.986	0.0722274

Simulation shows the output voltage is constant and independent of the charging current. From Table XI, the average output voltage has variance $1.69 \times 10^{-6}\ V^2$ while the ripple has variance $0.1685\ mV^2$. Furthermore, in all charging currents, the output voltage has an average of 41.50V with ~1% margin from the expected value. This error is due to the sensitivity of the driver's feedback pin to the error amplifier voltage divider with standard valued resistors.

Nonetheless, the output voltage ripple is within the maximum allowable 10% ripple.

C. *Efficiency*

To calculate the efficiency of the buck converter in the simulation, we divide the real power dissipated by the load to the real power supplied by the input. Table XII shows the power dissipation of the supply, load, and other major component of the buck converter in the simulation at different charging currents.

TABLE XII
DISSIPATION OF BUCK CONVERTER COMPONENTS

Charging current (%)	Dissipation (W)			
	Load	Supply	PMOS	Diode
100	90.5216	-95.565	2.44922	0.445617
75	67.8914	-72.2272	1.89572	0.319552
50	45.2611	-48.9213	1.3507	0.204137
10	9.05352	-12.0429	0.86042	0.0302955

Notice that PMOS dissipates the largest power due to its high frequency switching losses. Moreover, Table XIII shows the efficiency of the buck converter at different charging currents.

TABLE XIII
EFFICIENCY

Charging current (%)	Efficiency (%)
100	94.7225
75	93.997
50	92.5182
10	75.1775

At 100% charging current, the 94.7% efficiency of the buck converter can be achieved. Efficiency declines as the charging current is lowered. Hence, the load must be charged at higher charging current to maximize efficiency.

D. *Switching Voltage and Current experienced by HSS*

To analyze the switching voltage of the buck converter, plots of the switching voltage at different charging currents and their Fast Fourier Transforms (FFT) are generated.

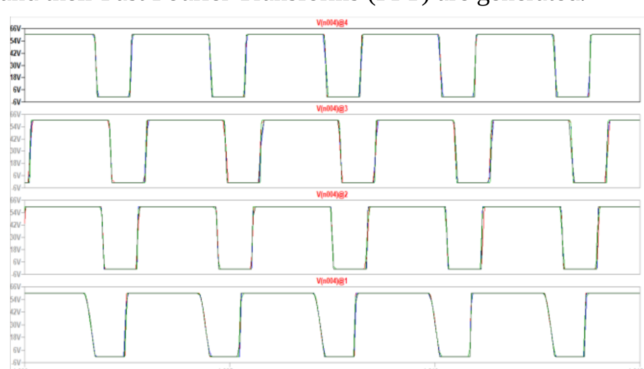

Fig. 6. Switching voltage of the buck converter at 100%, 75%, 50%, and 10% charging current (top to bottom).

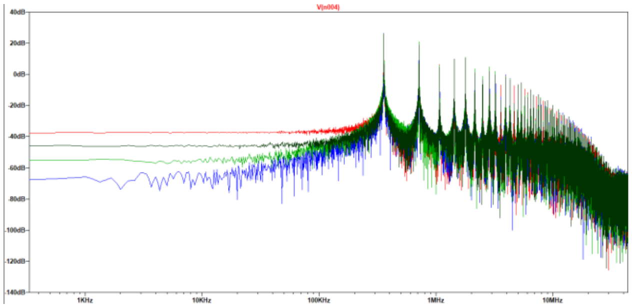

Fig. 7. FFT of the switching voltage at 100% charging current (black), at 75% charging current (green), at 50% charging current (blue), and at 10% charging current (red).

From Figure 6, the duty cycle at each charging currents and their corresponding percent error from the expected value are computed. Note that a single cycle of the switching voltage for each charging current is used for the computations.

TABLE XIV
SWITCHING VOLTAGE DUTY CYCLE

Charging current (%)	Duty Cycle (%)	Error (%)
100	67.83	1.53
75	68.33	0.81
50	67.85	1.52
10	64.33	6.62

At 10% charging current, the duty cycle error is significantly increased which may affect the output voltage at that cycle. Nonetheless, at high charging currents, the duty cycle error is reduced to less than 2%.

Furthermore, the frequency of the simulated switching voltage can be approximated by the dominating term of the FFT. Figure 7 shows that at all charging currents, the frequency of the switching voltage is about 357.4kHz. The value has a margin of 2.11% from the expected frequency.

Meanwhile, Figure 8 shows the drain current across the high side switch.

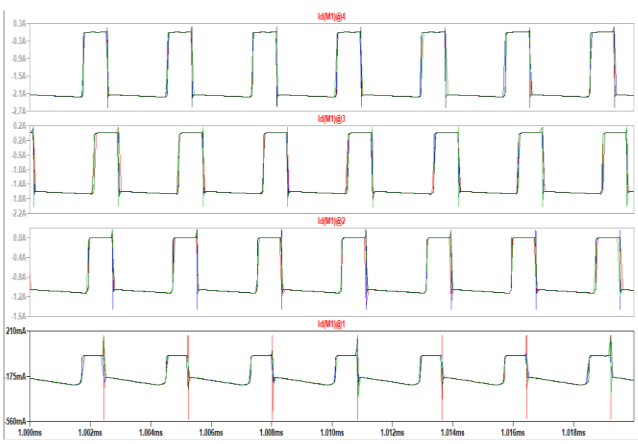

Fig. 8. PMOS drain current at 100%, 75%, 50%, and 10% charging current (top to bottom).

Reverse drain current flows when the switch is on which is controlled by the driver. At on time, the switching voltage is connected to the input. At off time, the switching voltage is grounded. This explains the plots at Figure 6.

It can also be observed that distortion or spikes caused by the transition delay of the switch is increased at lower charging current.

IV. CONCLUSION

Simulation shows that the designed asynchronous buck converter meets the desired specifications, with output voltage differing by ~1%. However, it is recommended to test an actual fabrication of the design since temperature may be a significant factor to the buck converter's efficiency.

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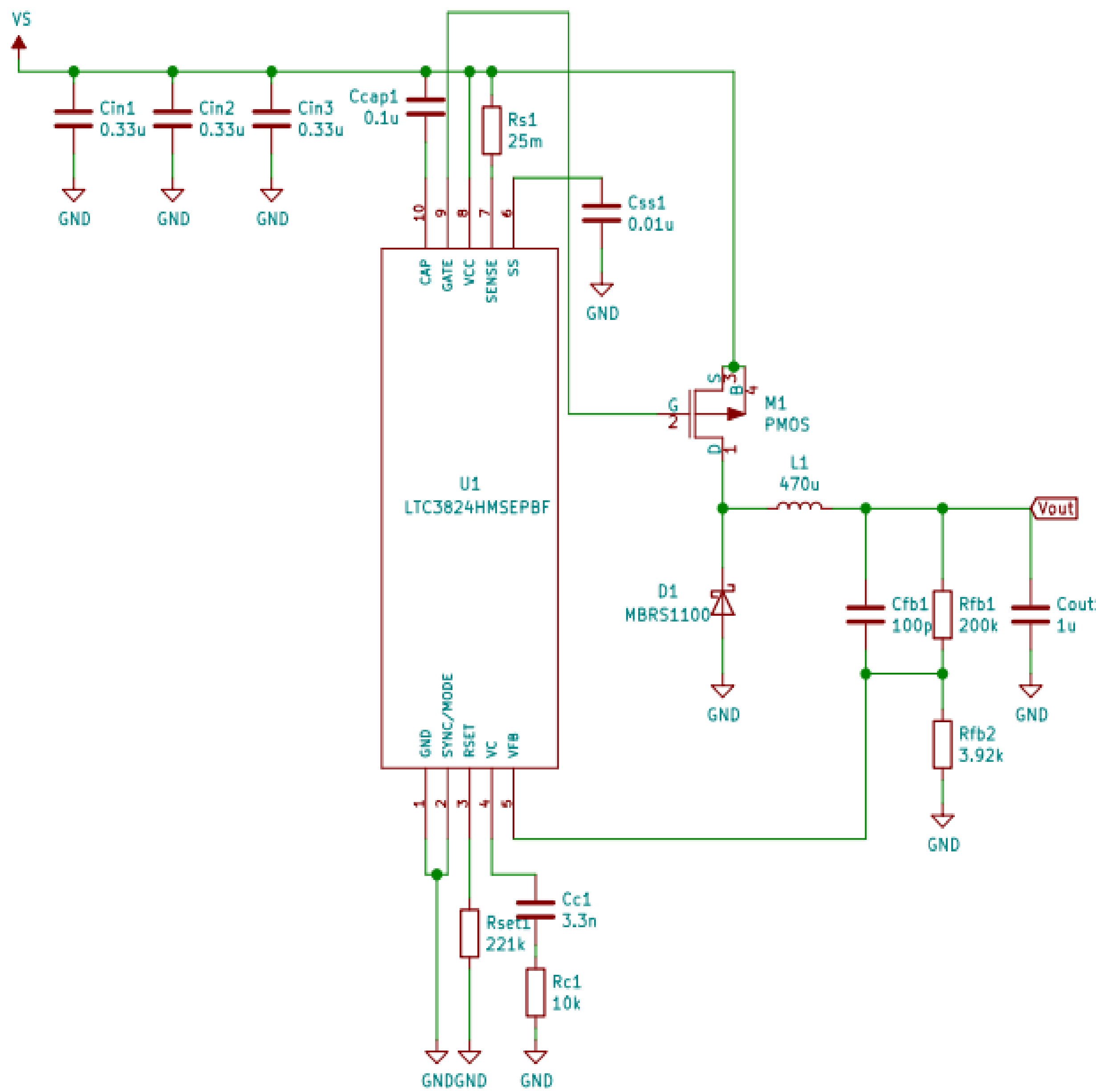
APPENDIX A



Appendix Fig. 1. Eeschema of the buck converter design using LTC3824 IC as driver.

APPENDIX B

APPENDIX TABLE I
BILL OF MATERIALS

Ref	Value	Footprint	Datasheet	Manufacturer	Vendor
Cc1	3.3n	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Ccap1	0.1u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Cfb1	100p	Capacitor_SMD:C_0201_0603Metric_Pad0.64x0.40mm_HandSolder	link	Murata	Digi-key
Cin1	0.33u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Cin2	0.33u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Cin3	0.33u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Cout1	1u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
Css1	0.01u	Capacitor_SMD:C_1206_3216Metric_Pad1.33x1.80mm_HandSolder	link	KEMET	Digi-key
D1	MBRS1100	Diode_SMD:D_SMB_Handsoldering	link	On Semiconductors	Digi-key
L1	470u	Inductor_THT:L_Radial_D40.6mm_P27.94mm_Vishay_IHB-4	link	Coilcraft	Coilcraft
M1	PMOS	Package_SO:PowerPAK_SO-8_Dual	link	Vishay Siliconix	Digi-key
Rc1	10k	Resistor_SMD:R_0805_2012Metric_Pad1.20x1.40mm_HandSolder	~		Digi-key
Rfb1	200k	Resistor_SMD:R_0805_2012Metric_Pad1.20x1.40mm_HandSolder	~		Digi-key
Rfb2	3.92k	Resistor_SMD:R_0805_2012Metric_Pad1.20x1.40mm_HandSolder	~		Digi-key
Rs1	25m	Resistor_SMD:R_1206_3216Metric_Pad1.30x1.75mm_HandSolder	link	Vishay	Digi-key
Rset1	221k	Resistor_SMD:R_0805_2012Metric_Pad1.20x1.40mm_HandSolder	~		Digi-key
U1	LTC3824HMSEPBF	Package_SO:MSOP-10-1EP_3x3mm_P0.5mm_EP1.68x1.88mm_ThermalVias	link	Linear Technology	Digi-key