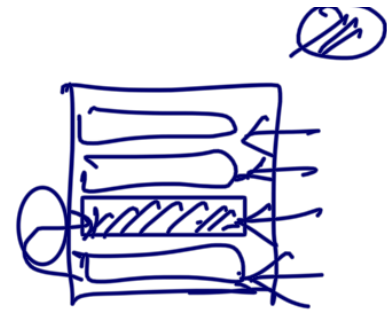
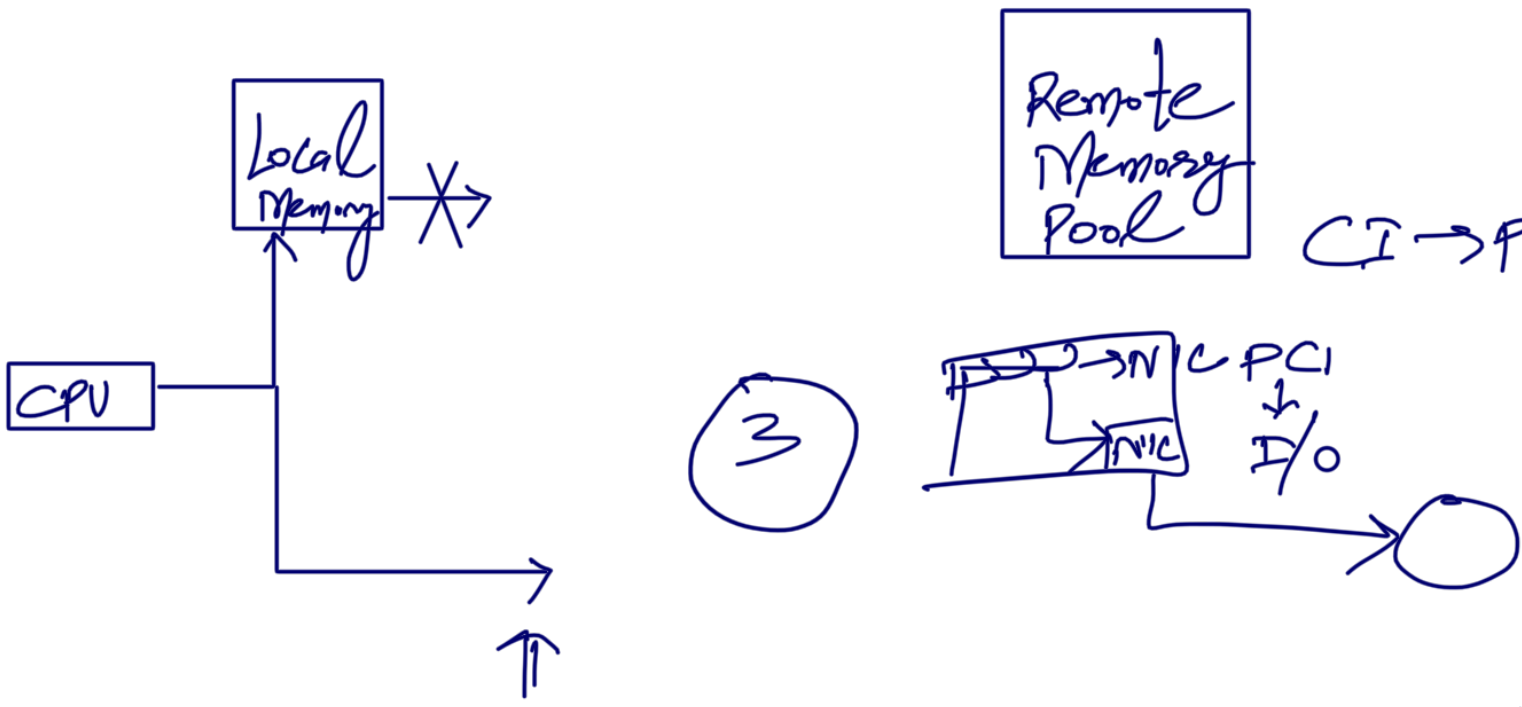
Network / Interconnect Simulation





Forward CPU Requests through

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Multiple ways to do.

- Forward remote address to NIC through PCI bus.
- Put the NIC on chip, no need to send through PCI.

Then from NIC, we can forward it to remote memory pool.

Use of Switches?

- Directly forward the remote memory request using PCI from server to Remote memory pool.

→ What need to be modeled?

- Chip-interconnect bus → PCI
- PCI → NIC → Remote Memory Switch → Memory

Protocol Model ?

- Chip-interconnect bus → NIC → Remote Memory Switch → Memory

Protocol Model ?

- Chip-interconnect bus → PCI
  ↓
  Memory ← Remote memory PCI switch

Protocol Model ?

⇒ What else?

- Configure-able bandwidth / delays
- All types of network delays to be configured through a file.
- Multiple standard hardware.

⇒ Implementation style

Pipelined ⇒ Dividing total functionality into pipelined modules where all components can run in parallel.

⇒ What we actually need through it?

For each request, total delay caused by network to & fro.

Plus, some more statistics.

E.g.:

- Average delay incurred by all the requests.
- Performance with different bandwidth/hardware delays.
- Which module is responsible for most of the delays.

and others, to be updated later.

⇒ Simulator validation

By comparing it with real hardware.

Will decide later, how to do that?