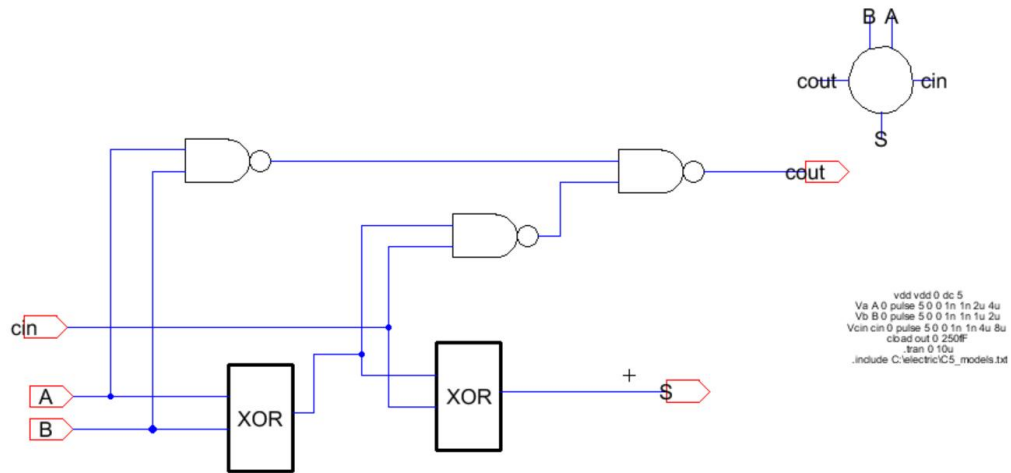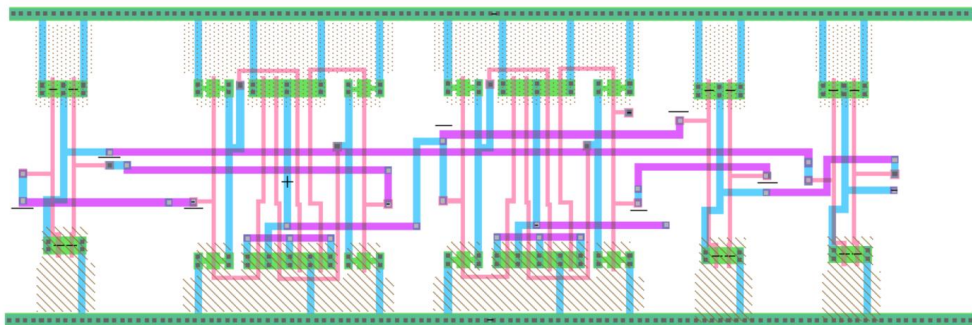# VLSI DESIGN in Electric Software
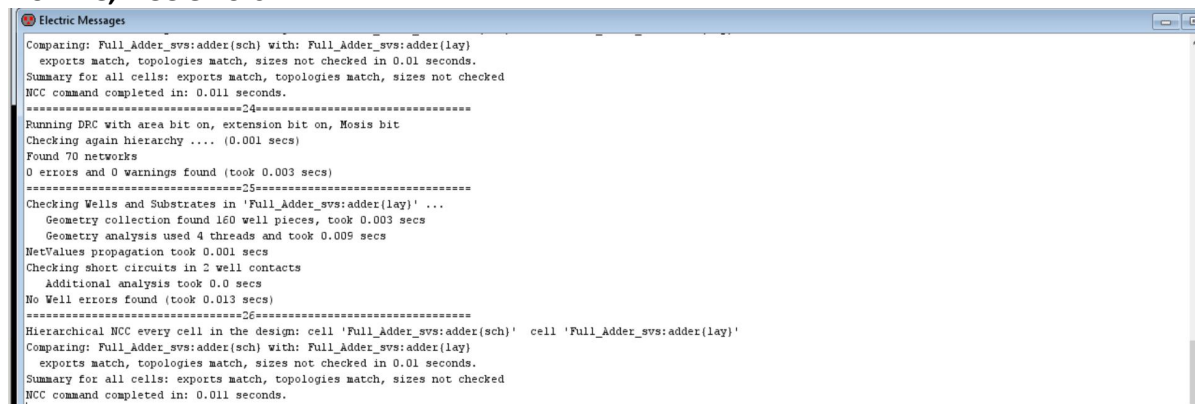
One bit Full-adder :
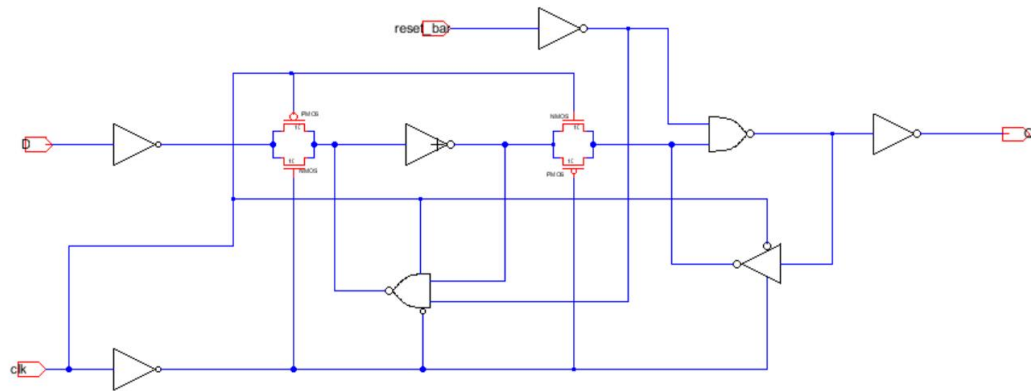**Schematic**

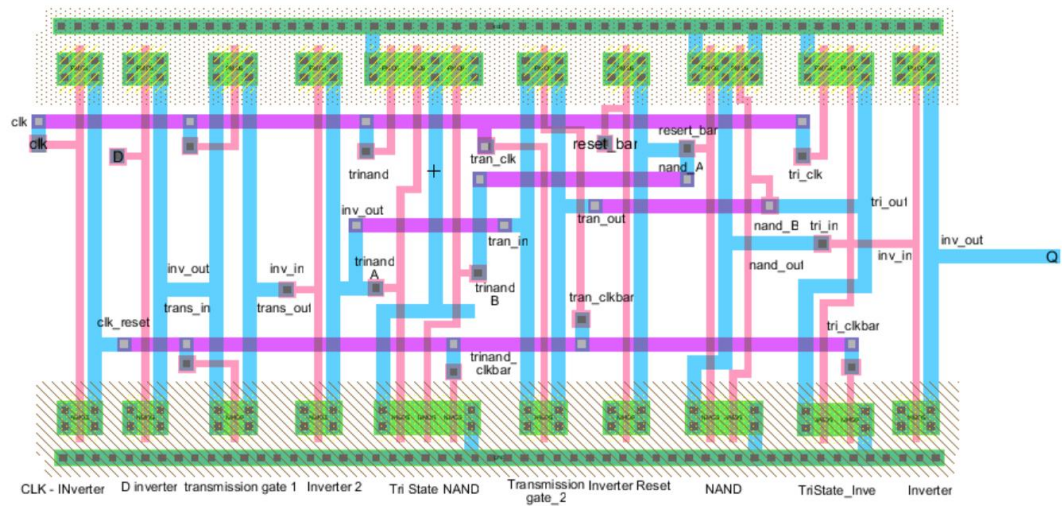**Layout:**

No DRC, NCC errors:


```
Comparing: Full_Adder_svs:adder{sch} with: Full_Adder_svs:adder{lay}
   exports match, topologies match, sizes not checked in 0.01 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.011 seconds.
==============================24================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 70 networks
0 errors and 0 warnings found (took 0.003 secs)
==============================25================================
Checking Wells and Substrates in 'Full_Adder_svs:adder{lay}' ...
   Geometry collection found 160 well pieces, took 0.003 secs
   Geometry analysis used 4 threads and took 0.009 secs
NetValues propagation took 0.001 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.013 secs)
==============================26================================
Hierarchical NCC every cell in the design: cell 'Full_Adder_svs:adder{sch}'  cell 'Full_Adder_svs:adder{lay}'
Comparing: Full_Adder_svs:adder{sch} with: Full_Adder_svs:adder{lay}
   exports match, topologies match, sizes not checked in 0.01 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.011 seconds.
```

D-FlipFlop:
Schematic

Layout

16-bit Accumulator Layout: