VHDL ASSIGNMENT
8 BIT ADDER

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SOURCE :

HALF ADDER CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bit2_add is
port (
                b_sum   : out std_logic ;
                b_carry : out std_logic ;
                b_a     : in std_logic :='0';
                b_b     : in std_logic :='0'
                );
end bit2_add;

architecture Behavioral of bit2_add is

begin
b_sum <= (not(b_a) and (b_b)) or (b_a and not(b_b)) ;
b_carry <= b_a and b_b ;


end Behavioral;
```

FULL ADDER:

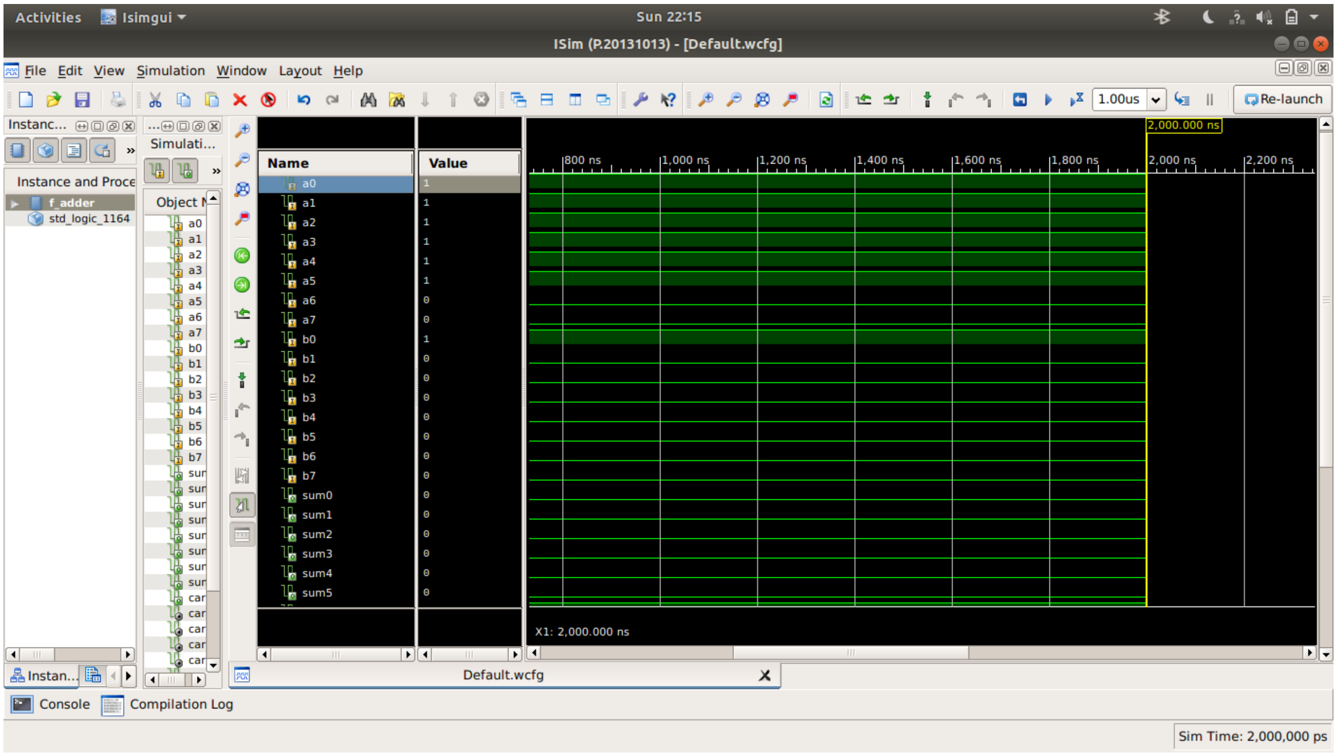
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bit4_add is
port (
h_a : in std_logic := '0';
h_b : in std_logic := '0';
h_cin: in std_logic := '0';
h_sum : out std_logic;
h_carry :out std_logic
);
```

```
end bit4_add;

architecture Behavioral of bit4_add is
signal carry1 : std_logic :='0';
signal carry2 : std_logic :='0';
signal carry : std_logic :='0';
signal sum : std_logic :='0';

component bit2_add
port (

                b_a     : in std_logic :='0';
                b_b     : in std_logic :='0' ;
                b_sum   : out std_logic ;
                b_carry : out std_logic
                );
end component ;
begin
H0:bit2_add port map(h_a,h_b,sum,carry1);
H1:bit2_add port map(sum,h_cin,h_sum,carry2);
carry<=carry1 or carry2;

h_carry<=carry1 or carry2;

end Behavioral;
```

8 BIT ADDER :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity f_adder is
port(
        a0 : in std_logic:='1';
        a1 : in std_logic:='1';
        a2 : in std_logic:='1';
        a3 : in std_logic:='1';
        a4 : in std_logic:='1';
        a5 : in std_logic:='1';
        a6 : in std_logic:='0';
        a7 : in std_logic:='0';
        b0 : in std_logic:='1';
        b1 : in std_logic:='0';
        b2 : in std_logic:='0';
        b3 : in std_logic:='0';
        b4 : in std_logic:='0';
        b5 : in std_logic:='0';
        b6 : in std_logic:='0';
        b7 : in std_logic:='0';
        sum0 :out std_logic:='0';
        sum1 :out std_logic:='0';
        sum2 :out std_logic:='0';
        sum3 :out std_logic:='0';
        sum4 :out std_logic:='0';
        sum5 :out std_logic:='0';
        sum6 :out std_logic:='0';
        sum7 :out std_logic:='0';

        carry_all : out std_logic:='0');
end f_adder;

architecture Behavioral of f_adder is
signal carry_0 : std_logic :='0';
signal carry_1 : std_logic ;
signal carry_2 : std_logic ;
signal carry_3 : std_logic ;
signal carry_4 : std_logic ;
signal carry_5 : std_logic ;
signal carry_6 : std_logic ;
signal carry_7 : std_logic ;
signal carry_8 : std_logic ;
component bit4_add
port (
h_a : in std_logic := '0';
h_b : in std_logic := '0';
h_cin: in std_logic := '0';
h_sum : out std_logic;
h_carry :out std_logic
);
end component;

begin
bit0 :bit4_add port map(a0,b0,carry_0,sum0,carry_1);
bit1 :bit4_add port map(a1,b1,carry_1,sum1,carry_2);
bit2 :bit4_add port map(a2,b2,carry_2,sum2,carry_3);
bit3 :bit4_add port map(a3,b3,carry_3,sum3,carry_4);
bit4 :bit4_add port map(a4,b4,carry_4,sum4,carry_5);
bit5 :bit4_add port map(a5,b5,carry_5,sum5,carry_6);
bit6 :bit4_add port map(a6,b6,carry_6,sum6,carry_7);
bit7 :bit4_add port map(a7,b7,carry_7,sum7,carry_all);




end Behavioral;
```

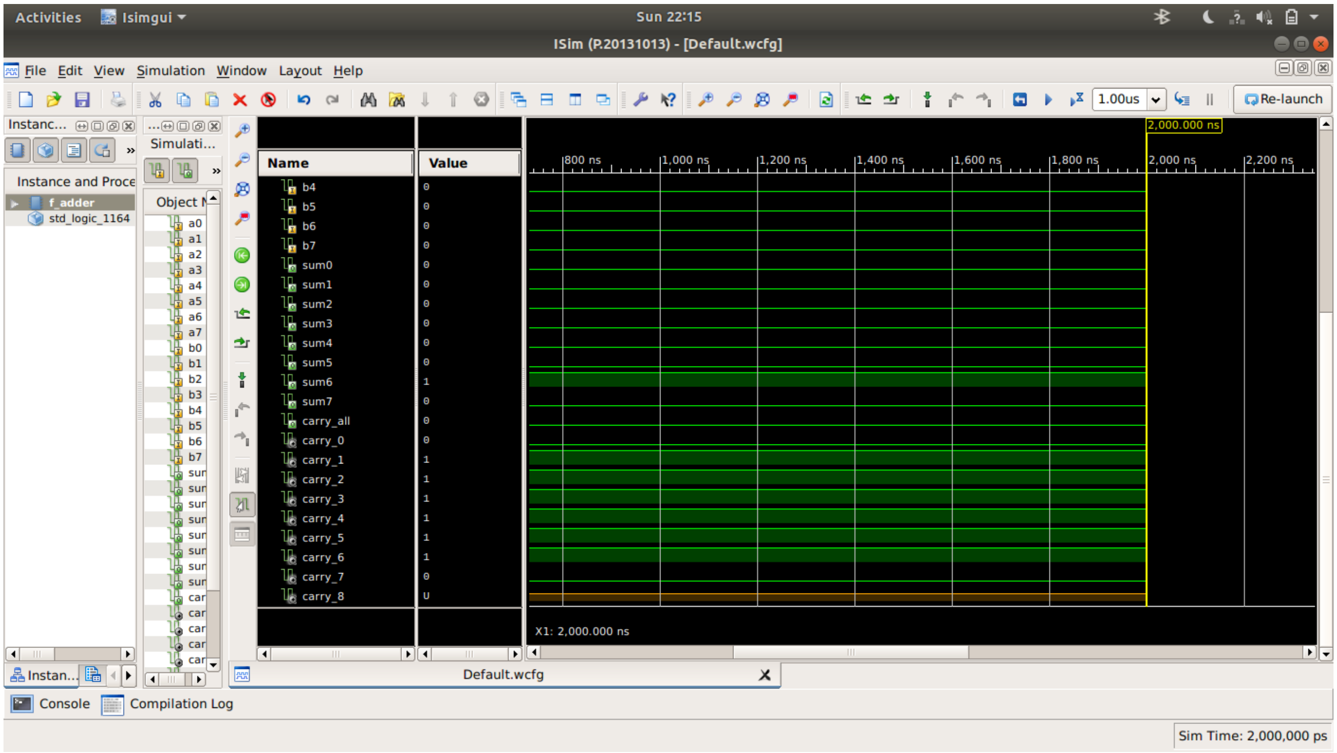
PULSE WAVE OUTPUT:



Name	Value
a0	1
a1	1
a2	1
a3	1
a4	1
a5	1
a6	0
a7	0
b0	1
b1	0
b2	0
b3	0
b4	0
b5	0
b6	0
b7	0
sum0	0
sum1	0
sum2	0
sum3	0
sum4	0
sum5	0

X1: 2,000.000 ns

Sim Time: 2,000,000 ps

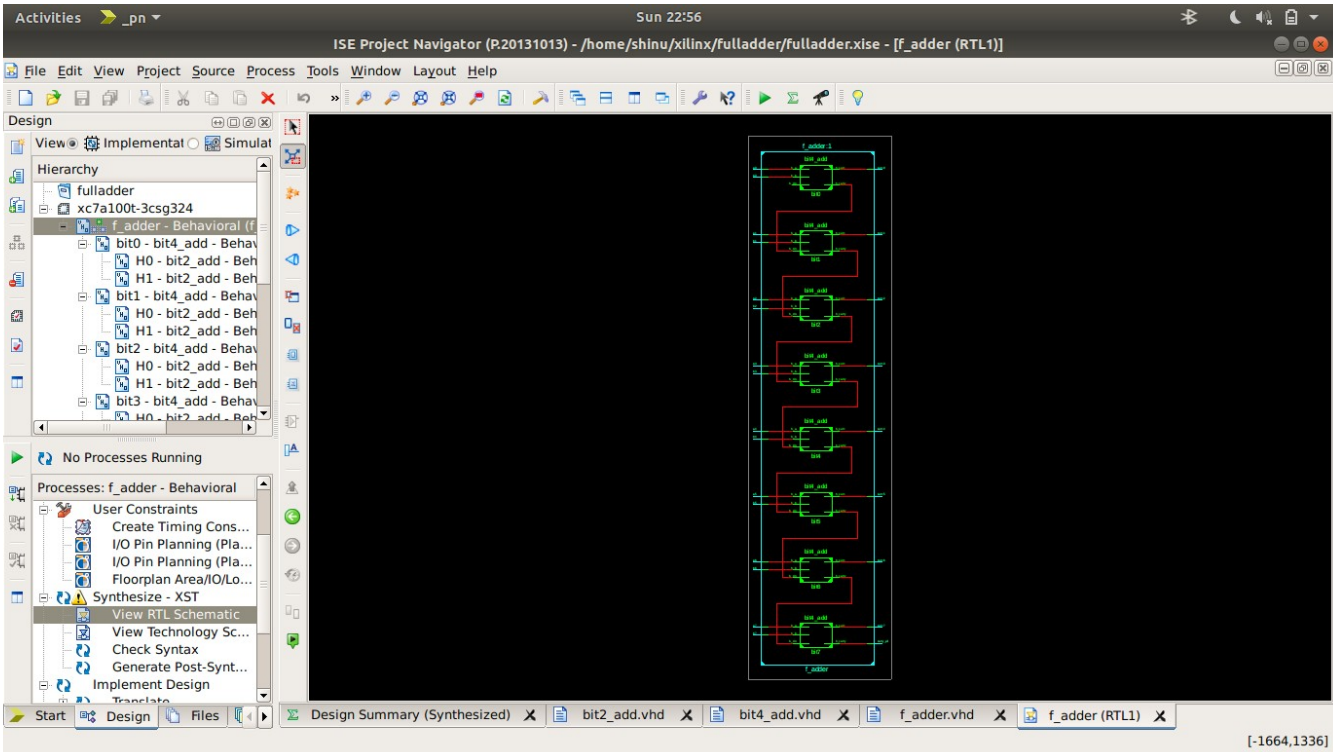


Name	Value
b4	0
b5	0
b6	0
b7	0
sum0	0
sum1	0
sum2	0
sum3	0
sum4	0
sum5	0
sum6	1
sum7	0
carry_all	0
carry_0	0
carry_1	1
carry_2	1
carry_3	1
carry_4	1
carry_5	1
carry_6	1
carry_7	0
carry_8	U

X1: 2,000.000 ns

Sim Time: 2,000,000 ps

SCHEMATIC DIAGRAM:


Activities
_pn
Sun 22:56
ISE Project Navigator (P.20131013) - /home/shinu/xilinx/fulladder/fulladder.xise - [f_adder (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: ● Implementat ○ Simulat
Hierarchy
fulladder
xc7a100t-3csg324
f_adder - Behavioral (f
bit0 - bit4_add - Behav
H0 - bit2_add - Beh
H1 - bit2_add - Beh
bit1 - bit4_add - Behav
H0 - bit2_add - Beh
H1 - bit2_add - Beh
bit2 - bit4_add - Behav
H0 - bit2_add - Beh
H1 - bit2_add - Beh
bit3 - bit4_add - Behav
H0 - bit2_add - Beh
No Processes Running
Processes: f_adder - Behavioral
User Constraints
Create Timing Cons...
I/O Pin Planning (Pla...
I/O Pin Planning (Pla...
Floorplan Area/IO/Lo...
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Translate
f_adder:1
bit4_add
bit0
bit4_add
bit1
bit4_add
bit2
bit4_add
bit3
bit4_add
bit4
bit4_add
bit5
bit4_add
bit6
bit4_add
bit7
f_adder
Start
Design
Files
Design Summary (Synthesized)
bit2_add.vhd
bit4_add.vhd
f_adder.vhd
f_adder (RTL1)
[-1664,1336]