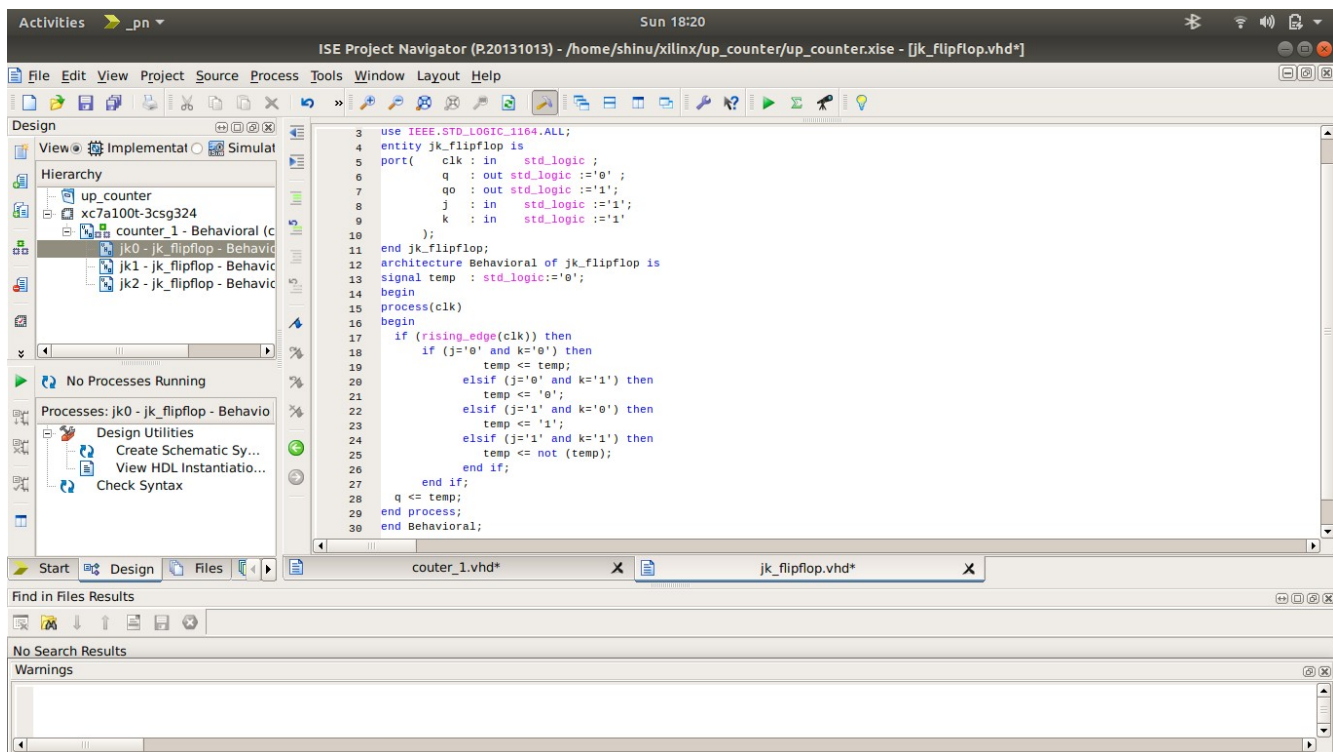


VHDL ASSIGNMENT

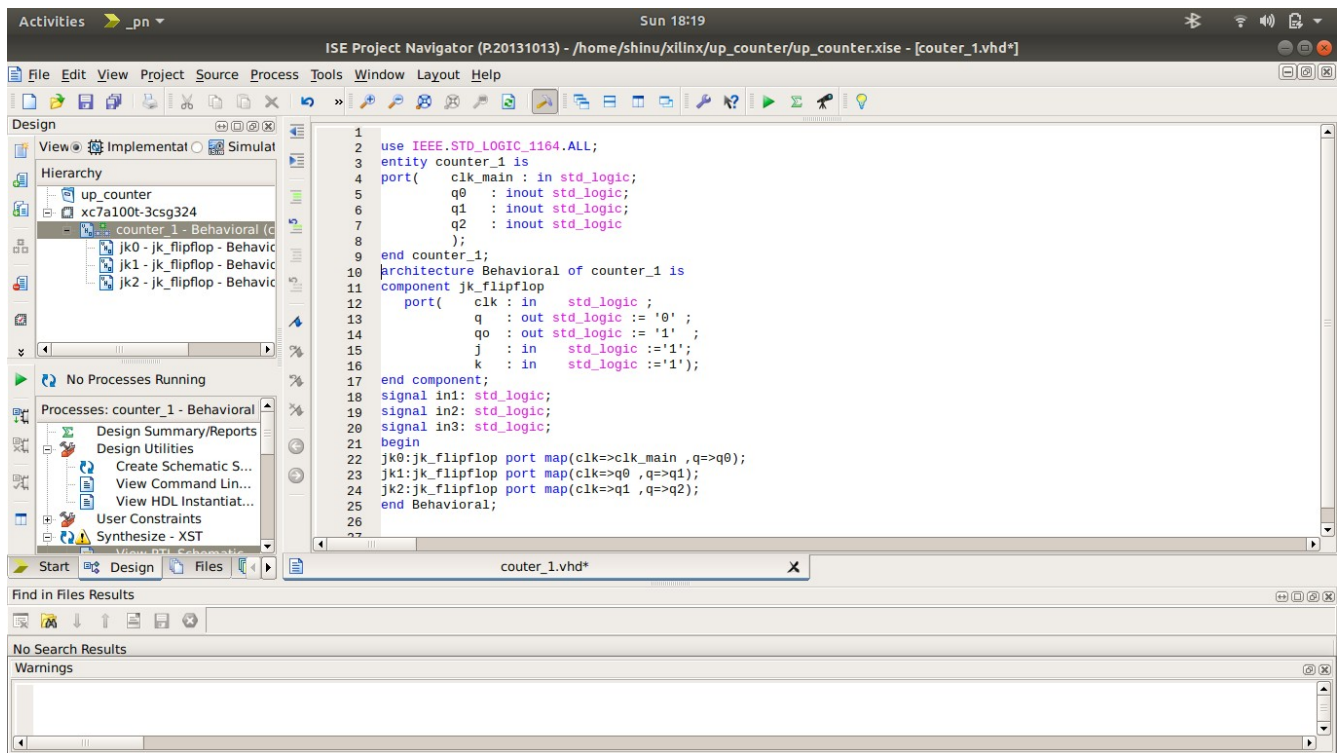
UP RIPPLE COUNTER USING J K FLIP FLOP

SHINU SHAJI C0761203

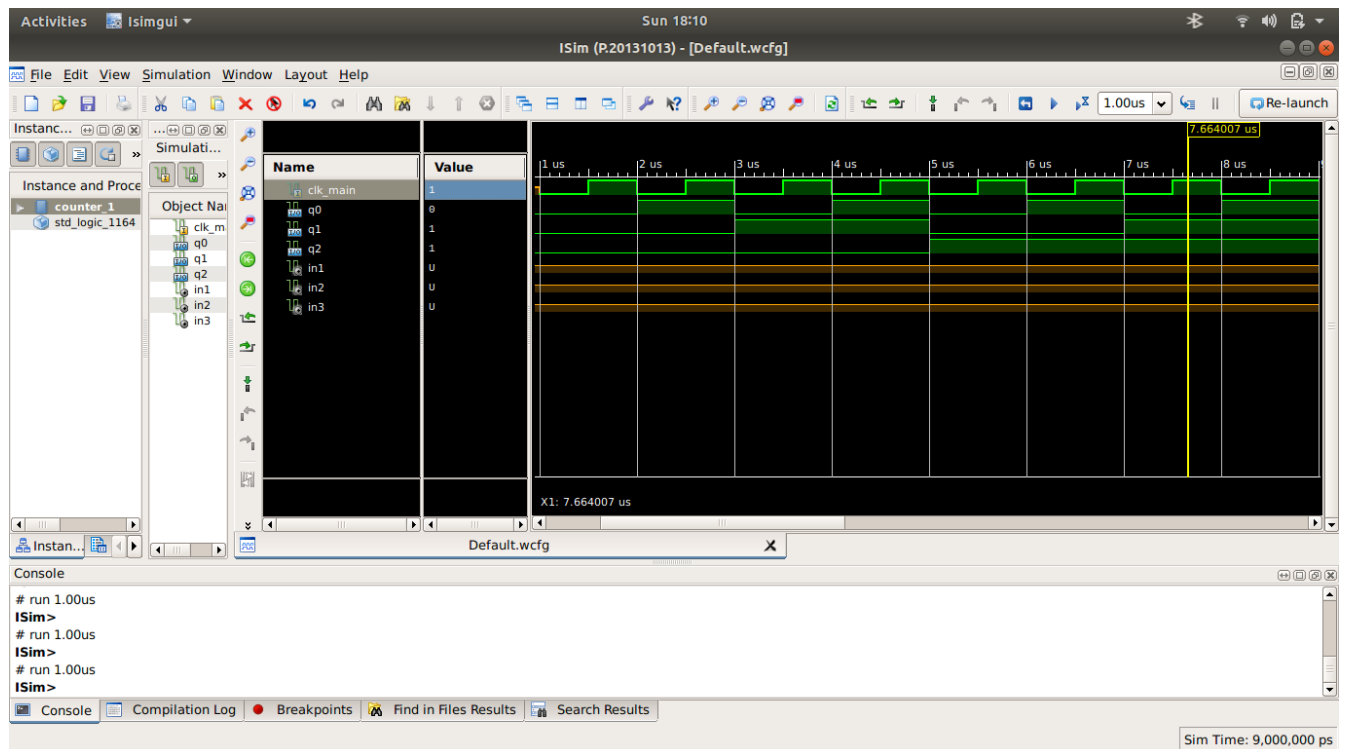
JK FLIP FLOP PROGRAMME



COUNTER PROGRAMME



PULSE WAVEFORM OUTPUT



SCHEMATICS OUTPUT

Activities

_pn

Sun 18:28

ISE Project Navigator (P.20131013) - /home/shinu/xilinx/up_counter/up_counter.xise - [counter_1 (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design

View

Implementat

Simulat

Hierarchy

up_counter

xc7a100t-3csg324

counter_1 - Behavioral (0)

jk0 - jk_flipflop - Behavior

jk1 - jk_flipflop - Behavior

jk2 - jk_flipflop - Behavior

No Processes Running

Processes: counter_1 - Behavioral

Design Summary/Reports

Design Utilities

Create Schematic S...

View Command Lin...

View HDL Instantiat...

User Constraints

Synthesize - XST

View RTL Schematic

Start

Design

Files

Design Summary (Synthesized)

coutner_1.vhd

counter_1 (RTL1)

View by Category

Design Objects of Top Level Block

Instances

counter_1

jk0

jk1

Pins

counter_1

Signals

counter_1

Properties of Instance: jk0

Name	Value
Type	jk_flipflop
Instance Name	jk0

Console

Errors

Warnings

Find in Files Results

View by Category

[1896,792]

