Exam: 30/01/2017

1-) Considering the MIPS64 architecture presented in the following:

Integer ALU: 1 clock cycle
Data memory: 1 clock cycle
FP multiplier unit: pipelined 10 stages
FP arithmetic unit: pipelined 4 stages
FP divider unit: not pipelined unit that requires 12 clock cycles
branch delay slot: 1 clock cycle, and the branch delay slot is not enable
forwarding is enabled
it is possible to complete instruction EXE stage in an out-of-order fashion.

and using the following code fragment, show the timing of the presented loop-based program and compute how many cycles does this program take to execute?

```
Main:   daddui R1,R0,0
        daddui R2,R0,100
Loop:   l.d F1,V1(R1)
        l.d F2,V2(R1)
        mul.d F5,F1,F2
        s.d F5,V5(R1)
        l.d F3,V3(R1)
        mul.d F6,F2,F3
        s.d F6,V6(R1)
        l.d F4,V4(R1)
        div.d F7,F6,F4
        add.d F7,F7,F3
        s.d F7,V7(R1)
        daddui R2,R2,-1
        bnez R2, LOOP
        halt
```

2-) Using the static scheduling technique and enabling the Branch Delay Slot, re-schedule the presented code in order to eliminate the most data hazards. Compute the number of clock cycles necessary to execute the new program.