Examples about Tomasulo's architecture



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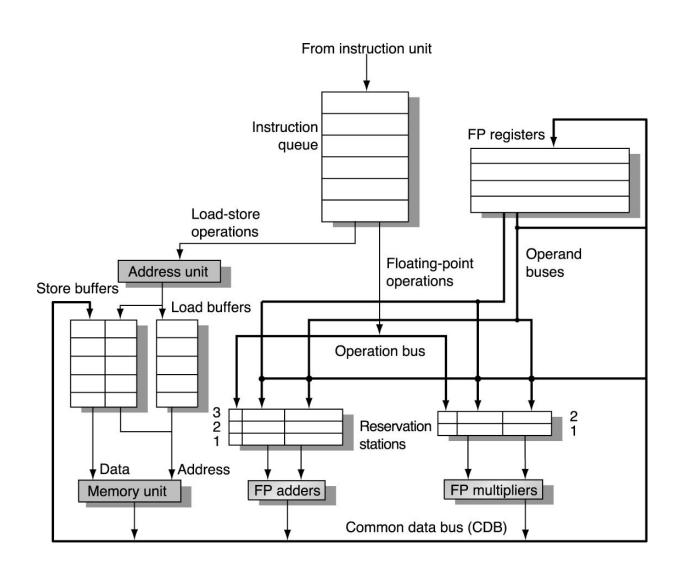
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Tomasulo Organization



Reservation Station fields

Op Operation to be perform by the unit (e.g., + or –)

Qj, Qk Reservation stations producing the source registers

Vj, Vk Value of source operands

Rj, Rk Flags indicating whether Vj, Vk are ready

Busy Indicates reservation station and FU is busy

Register file additional field

Register result status Indicates which functional unit will write each register, if any. Blank when no pending instructions are going to write into the register.

Three Stages of Tomasulo Algorithm

- 1. Issue get instruction from FP Op Queue If reservation station free, the scoreboard issues instr & sends operands (renames registers).
- Execution operate on operands (EX)
 When both operands ready then execute;
 if not ready, watch CDB for result
- 3. Write result finish execution (WB)

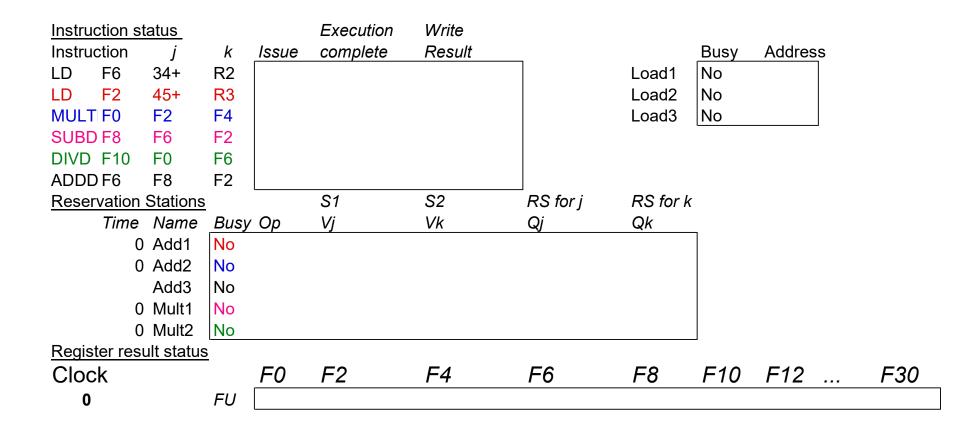
 Write on Common Data Bus to all awaiting units;
 mark reservation station available.

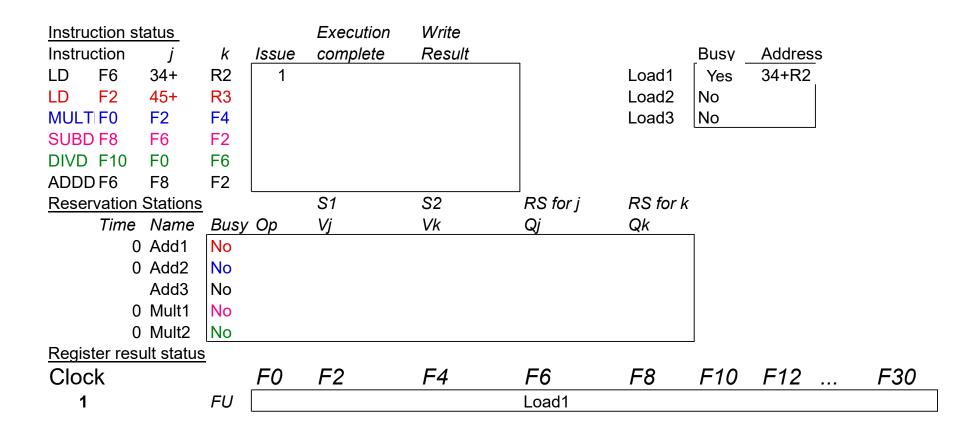
Tomasulo Example #1

```
1 L.D F6, 34(R2)
2 L.D F2, 45(R3)
3 MUL.D F0, F2, F4
4 SUB.D F8, F2, F6
5 DIV.D F10, F0, F6
6 ADD.D F6, F8, F2
```

Assumptions:

- Add takes 2 clock cycles, Multiply 10, Divide 40
- Loads requires 2 ccs





Instru	ction s	<u>tatus</u>			Execution	Write					
Instru	ction	j	k	Issue	complete	Result			Busy	Address	
LD	F6	34+	R2	1				Load1	Yes	34+R2	
LD	F2	45+	R3	2				Load2	Yes	45+R3	
MULT	F0	F2	F4					Load3	No		
SUBD) F8	F6	F2								
DIVD	F10	F0	F6								
ADDE	DF6	F8	F2								
Reser	rvation	Stations	<u>i</u>		S1	S2	RS for j	RS for k	-		
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk			
	C	Add1	No								
	C	Add2	No								
		Add3	No								
	C	Mult1	No								
	C	Mult2	No								
Regis	ter res	ult status	<u>3</u>								
Cloc	ck			F0	F2	F4	F6	F8	F10	F12	F30
2			FU		Load2		Load1				

Instruction				Execution	Write					
Instruction	ı j	k	<u>Issue</u>	complete	Result			Busy	<u>Addres</u> s	
LD F6	34+	R2	1	3			Load1	Yes	34+R2	
LD F2	45+	R3	2				Load2	Yes	45+R3	
MULT F0	F2	F4	3				Load3	No		
SUBD F8	F6	F2								
DIVD F10) F0	F6								
ADDD F6	F8	F2								
Reservation	on Stations	<u> </u>		S1	S2	RS for j	RS for k	•		
Tin	ne Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0 Add1	No								
	0 Add2	No								
	Add3	No								
	0 Mult1	Yes	MULTE		R(F4)	Load2				
	0 Mult2	No								
Register r	esult statu	<u>s</u>								
Clock			F0	F2	F4	F6	F8	F10	F12	F30
3		FU	Mult1	Load2		Load1				

Instruction	status ;	k	logue	Execution	Write			Puov	Address	
Instruction	J	k	Issue	complete	Result	\neg		Busy	Address	
LD F6	34+	R2	1	3	4		Load1	No		
LD F2	45+	R3	2				Load2	Yes	45+R3	
MULT F0	F2	F4	3				Load3	No		
SUBD F8	F6	F2	4							
DIVD F10	F0	F6								
ADDD F6	F8	F2								
Reservation	n Stations	<u> </u>		S1	S2	RS for j	RS for k			
Tim	e Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0 Add1	Yes	SUBD	M(34+R2)			Load2			
	0 Add2	No								
	Add3	No								
	0 Mult1	Yes	MULTE)	R(F4)	Load2				
	0 Mult2	No								
Register re	sult statu:	<u>s</u>								
Clock			F0	F2	F4	F6	F8	F10	F12	F30
4		FU	Mult1	Load2		M(34+R2)	 Add1			

Instruct		tatus_		_	Execution	Write			_		
Instruct	tion	j	k	<u>Issue</u>	complete	Result	_		Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD I	F2	45+	R3	2	5			Load2	Yes	45+R3	
MULT	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4							
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2								
Reserv	/ation	Stations			S1	S2	RS for j	RS for k			
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0	Add1	Yes	SUBD	M(34+R2)			Load2			
	0	Add2	No								
		Add3	No								
	0	Mult1	Yes	MULTE)	R(F4)	Load2				
	0	Mult2	Yes	DIVD		M(34+R2)	Mult1				
Registe	er res	ult status	3								
Clock	K			F0	F2	F4	F6	F8	F10	F12 .	F30
5			FU	Mult1	Load2		M(34+R2)	Add1	Mult2		

Instruction s	status_			Execution	Write						
Instruction	j	k	Issue	complete	Result	_		Busy	Addres	S	
LD F6	34+	R2	1	3	4		Load1	No			
LD F2	45+	R3	2	5	6		Load2	No			
MULT F0	F2	F4	3				Load3	No			
SUBD F8	F6	F2	4								
DIVD F10	F0	F6	5								
ADDD F6	F8	F2	6								
Reservation	Stations	<u> </u>		S1	S2	RS for j	RS for k	-			
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	2 Add1	Yes	SUBD	M(34+R2)	M(45+R3)						
(O Add2	Yes	ADDD		M(45+R3)	Add1					
	Add3	No									
10) Mult1	Yes	MULTE	M(45+R3)	R(F4)						
(0 Mult2	Yes	DIVD		M(34+R2)	Mult1					
Register res	sult status	<u>s</u>									
Clock			F0	F2	F4	F6	F8	F10	F12		F30
6		FU	Mult1	M(45+R3)		Add2	Add1	Mult2			

Instruction s	status_			Execution	Write						
Instruction	j	K	Issue	complete	Result	_		Busy	Addres	S	
LD F6	34+	R2	1	3	4		Load1	No			
LD F2	45+	R3	2	5	6		Load2	No			
MULT F0	F2	F4	3				Load3	No			
SUBD F8	F6	F2	4					,		_	
DIVD F10	F0	F6	5								
ADDD F6	F8	F2	6								
Reservation	Stations	<u>i</u>		S1	S2	RS for j	RS for k				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	1 Add1	Yes	SUBD	M(34+R2)	M(45+R3)						
(O Add2	Yes	ADDD		M(45+R3)	Add1					
	Add3	No									
9	9 Mult1	Yes	MULTE	M(45+R3)	R(F4)						
(0 Mult2	Yes	DIVD		M(34+R2)	Mult1					
Register res	sult status	<u>3</u>									
Clock			F0	F2	F4	F6	F8	F10	F12		F30
7		FU	Mult1	M(45+R3)		Add2	Add1	Mult2			

Instruct		tatus ;	l.	lagua	Execution	Write			Duay	۸ ما مارد م. م.	
Instruct		J	k	Issue	complete	Result	\neg		Busy	Address	
LD I	F6	34+	R2	1	3	4		Load1	No		
LD I	F2	45+	R3	2	5	6		Load2	No		
MULT	F0	F2	F4	3				Load3	No		
SUBD I	F8	F6	F2	4	8						
DIVD I	F10	F0	F6	5							
ADDDI	F6	F8	F2	6							
Reserv	/ation	Stations	<u> </u>	•	S1	S2	RS for j	RS for k			
•	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0	Add1	Yes	SUBD	M(34+R2)	M(45+R3)					
	0	Add2	Yes	ADDD		M(45+R3)	Add1				
		Add3	No								
	8	Mult1	Yes	MULTE	M(45+R3)	R(F4)					
	0	Mult2	Yes	DIVD		M(34+R2)	Mult1				
Registe	er res	ult status	<u>3</u>								
Clock	<			F0	F2	F4	F6	F8	F10	F12	F30
8			FU	Mult1	M(45+R3)		Add2	Add1	Mult2		

Instruction sta	<u>tus</u>			Execution	Write						
Instruction	j	k	Issue	complete	Result	_		Busy	Addres	S	
LD F6	34+	R2	1	3	4		Load1	No			
LD F2	45+	R3	2	5	6		Load2	No			
MULT FO	F2	F4	3				Load3	No			
SUBD F8	F6	F2	4	8	9						
DIVD F10 I	F0	F6	5								
ADDD F6	F8	F2	6								
Reservation S	tations			S1	S2	RS for j	RS for k				
Time I	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
0 /	Add1	No									
0 /	Add2	Yes	ADDD	M()-M()	M(45+R3)						
,	Add3	No									
7 1	Mult1	Yes	MULTD	M(45+R3)	R(F4)						
0 1	Mult2	Yes	DIVD		M(34+R2)	Mult1					
Register resul	t status	<u>}</u>									
Clock			F0	F2	F4	F6	F8	F10	F12		F30
9		FU	Mult1	M(45+R3)		Add2	M()–M()	Mult2			

Instruction	on stat	us			Execution	Write						
Instruction	on	j	k	Issue	complete	Result	_		Busy	Addres	s	
LD F	6 3	34+	R2	1	3	4		Load1	No			
LD F	2 4	5+	R3	2	5	6		Load2	No			
MULT F	0 F	2	F4	3				Load3	No			
SUBD F	8 F	6	F2	4	8	9						
DIVD F	10 F	0	F6	5								
ADDD F	6 F	8	F2	6								
Reserva	tion St	ations			S1	S2	RS for j	RS for k				
Ti	ïme ∧	lame	Busy	Ор	Vj	Vk	Qj	Qk	_			
	0 A	Add1	No									
	2 A	Add2	Yes	ADDD	M()–M()	M(45+R3)						
	A	Add3	No									
	6 N	/lult1	Yes	MULTE	M(45+R3)	R(F4)						
	υN	/lult2	Yes	DIVD		M(34+R2)	Mult1					
Register	result	status	<u>s</u>									
Clock				FO	F2	F4	F6	F8	F10	F12		F30
10			FU	Mult1	M(45+R3)		Add2	M()–M()	Mult2			

Instruc		tatus			Execution	Write			_			
Instruc	ction	J	k	Issue	complete	Result	_		Busy	Addres	3	
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	5	6		Load2	No			
MULT	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	8	9						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6								
Reser	vation	Stations	<u>i</u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	C	Add1	No									
	1	Add2	Yes	ADDD	M()-M()	M(45+R3)						
		Add3	No									
	5	Mult1	Yes	MULTE	M(45+R3)	R(F4)						
	C) Mult2	Yes	DIVD		M(34+R2)	Mult1					
Regist	ter res	ult status	<u> </u>									
Cloc	k			F0	F2	F4	F6	F8	F10	F12		F30
11			FU	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Instruction status			Execution	Write						
Instruction j	k	Issue	complete	Result	_		Busy	Addres	S	
LD F6 34+	R2	1	3	4		Load1	No			
LD F2 45+	R3	2	5	6		Load2	No			
MULT F0 F2	F4	3				Load3	No			
SUBD F8 F6	F2	4	8	9						
DIVD F10 F0	F6	5								
ADDD F6 F8	F2	6	12							
Reservation Stations			S1	S2	RS for j	RS for k				
Time Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
0 Add1	No									
0 Add2	Yes	ADDD	M()-M()	M(45+R3)						
Add3	No									
4 Mult1	Yes	MULTE	M(45+R3)	R(F4)						
0 Mult2	Yes	DIVD		M(34+R2)	Mult1		_			
Register result status	<u> </u>									
Clock		F0	F2	F4	F6	F8	F10	F12		F30
12	FU	Mult1	M(45+R3)		Add2	M()–M()	Mult2			

Instruction status			Execution	Write					
Instruction j	k <u>I</u>	ssue	complete	Result			Busy	Address	
LD F6 34+ R	R2	1	3	4		Load1	No		
LD F2 45+ R	3	2	5	6		Load2	No		
MULT F0 F2 F	4	3				Load3	No		
SUBD F8 F6 F	2	4	8	9					
DIVD F10 F0 F	6	5							
ADDD F6 F8 F.	2	6	12	13					
Reservation Stations			S1	S2	RS for j	RS for k			
Time Name B	Busy C	Ор	Vj	Vk	Qj	Qk			
0 Add1 N	10								
0 Add2 N	Ю								
Add3 N	Ю								
3 Mult1 Y	es N	MULTD	M(45+R3)	R(F4)					
0 Mult2 Y	es [DIVD	,	M(34+R2)	Mult1				
Register result status				•					
Clock	ŀ	F0	F2	F4	F6	F8	F10	F12	 F30
13 F	U	/lult1	M(45+R3)		(M-M)+M()	M()-M()	Mult2		

	ction s	tatus_		_	Execution	Write			_			
Instru	ction	j	k	Issue	complete	Result			Busy	Addres	3	
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	5	6		Load2	No			
MULT	F0	F2	F4	3				Load3	No			
SUBE) F8	F6	F2	4	8	9			,			
DIVD	F10	F0	F6	5								
ADDE	DF6	F8	F2	6	12	13						
Rese	rvation	Stations	<u>.</u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	C) Add1	No									
	C) Add2	No									
		Add3	No									
	2	2 Mult1	Yes	MULTE	M(45+R3)	R(F4)						
	C) Mult2	Yes	DIVD		M(34+R2)	Mult1					
Regis	ter res	ult status	<u> </u>									
Cloc	ck			F0	F2	F4	F6	F8	F10	F12		F30
14			FU	Mult1	M(45+R3)		(M–M)+M()	M()-M()	Mult2			

Instructi		atus_			Execution	Write					
Instructi	on	j	k	Issue	complete	Result	_		Busy	Address	
LD F	6	34+	R2	1	3	4		Load1	No		
LD F	2	45+	R3	2	5	6		Load2	No		
MULT F	0	F2	F4	3				Load3	No		
SUBD F	8	F6	F2	4	8	9					
DIVD F	10	F0	F6	5							
ADDD F	6	F8	F2	6	12	13					
Reserva	ation	Stations			S1	S2	RS for j	RS for k			
T	ime	Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0	Add1	No								
	0	Add2	No								
		Add3	No								
	1	Mult1	Yes	MULTE	M(45+R3)	R(F4)					
	0	Mult2	Yes	DIVD		M(34+R2)	Mult1				
Register	r resu	ult status	<u> </u>						_		
Clock				F0	F2	F4	F6	F8	F10	F12 .	F30
15			FU	Mult1	M(45+R3)		(M-M)+M()	M()–M()	Mult2		

Instruction	status			Execution	Write					
Instruction	j	k	Issue	complete	Result	_		Busy	Address	
LD F6	34+	R2	1	3	4		Load1	No		
LD F2	45+	R3	2	5	6		Load2	No		
MULT F0	F2	F4	3	16			Load3	No		
SUBD F8	F6	F2	4	8	9					
DIVD F10	F0	F6	5							
ADDD F6	F8	F2	6	12	13					
Reservation	n Stations	<u> </u>		S1	S2	RS for j	RS for k			
Tim	e Name	Busy	Ор	Vj	Vk	Qj	Qk	-		
	0 Add1	No								
	0 Add2	No								
	Add3	No								
	0 Mult1	Yes	MULTE	M(45+R3)	R(F4)					
	0 Mult2	Yes	DIVD		M(34+R2)	Mult1				
Register re	sult statu	<u>s</u>								
Clock			F0	F2	F4	F6	F8	F10	F12	. F30
16		FU	Mult1	M(45+R3)		(M–M)+M()	M()–M()	Mult2		

Instruct		tatus			Execution	Write			_			
Instruct	tion	J	k	Issue	complete	Result	_		Busy	Address	6	
LD I	F6	34+	R2	1	3	4		Load1	No			
LD I	F2	45+	R3	2	5	6		Load2	No			
MULTI	F0	F2	F4	3	16	17		Load3	No			
SUBD I	F8	F6	F2	4	8	9						
DIVD I	F10	F0	F6	5								
ADDDI	F6	F8	F2	6	12	13						
Reserv	/ation	Stations	1		S1	S2	RS for j	RS for k				
•	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	0	Add1	No									
	0	Add2	No									
		Add3	No									
	0	Mult1	No									
	0	Mult2	Yes	DIVD	M*F4	M(34+R2)						
Registe	er res	ult status	3									
Clock	<			F0	F2	F4	F6	F8	F10	F12		F30
17			FU	M*F4	M(45+R3)		(M–M)+M()	M()-M()	Mult2			

Instruction	status			Execution	Write						
Instruction	j	k	Issue	complete	Result	_		Busy	Addres	S	
LD F6	34+	R2	1	3	4		Load1	No			
LD F2	45+	R3	2	5	6		Load2	No			
MULT F0	F2	F4	3	16	17		Load3	No			
SUBD F8	F6	F2	4	8	9						
DIVD F10	F0	F6	5								
ADDD F6	F8	F2	6	12	13						
Reservation	n Stations	<u> </u>		S1	S2	RS for j	RS for k				
Tim	e Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	0 Add1	No									
	0 Add2	No									
	Add3	No									
	0 Mult1	No									
4	0 Mult2	Yes	DIVD	M*F4	M(34+R2)						
Register re	esult statu	<u>s</u>									
Clock			F0	F2	F4	F6	F8	F10	F12		F30
18		FU	M*F4	M(45+R3)		(M–M)+M()	M()-M()	Mult2			

Instruction s	status_			Execution	Write						
Instruction	j	k	Issue	complete	Result	_		Busy	Address	i	
LD F6	34+	R2	1	3	4		Load1	No			
LD F2	45+	R3	2	5	6		Load2	No			
MULT F0	F2	F4	3	16	17		Load3	No			
SUBD F8	F6	F2	4	8	9						
DIVD F10	F0	F6	5								
ADDD F6	F8	F2	6	12	13						
Reservation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	0 Add1	No									
	0 Add2	No									
	Add3	No									
	0 Mult1	No									
	1 Mult2	Yes	DIVD	M*F4	M(34+R2)						
Register res	sult statu	<u>s</u>									
Clock			F0	F2	F4	F6	F8	F10	F12		F30
57		FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	Mult2			

Instruction s	status_			Execution	Write					
Instruction	j	k	Issue	complete	Result	_		Busy	Address	
LD F6	34+	R2	1	3	4		Load1	No		
LD F2	45+	R3	2	5	6		Load2	No		
MULT F0	F2	F4	3	16	17		Load3	No		
SUBD F8	F6	F2	4	8	9					
DIVD F10	F0	F6	5	58						
ADDD F6	F8	F2	6	12	13					
Reservation	Stations	<u> </u>		S1	S2	RS for j	RS for k			
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_		
	0 Add1	No								
	0 Add2	No								
	Add3	No								
	0 Mult1	No								
	0 Mult2	Yes	DIVD	M*F4	M(34+R2)					
Register res	sult statu:	<u>s</u>								
Clock			F0	F2	F4	F6	F8	F10	F12	. F30
58		FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	Mult2		

	ction s	tatus_		_	Execution	Write			_			
Instru	ction	j	k	Issue	complete	Result	_		Busy	Addres	S	
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	5	6		Load2	No			
MULT	F0	F2	F4	3	16	17		Load3	No			
SUBD) F8	F6	F2	4	8	9						
DIVD	F10	F0	F6	5	58	59						
ADDD) F6	F8	F2	6	12	13						
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	_			
	C	Add1	No									
	C	Add2	No									
		Add3	No									
	C) Mult1	No									
	C) Mult2	No									
Regis	ter res	ult status	<u> </u>						_			
Cloc	k			F0	F2	F4	F6	F8	F10	F12		F30
59			FU	M*F4	M(45+R3)		(M–M)+M()	M()-M()	M*F4/M			

Tomasulo Loop Example

Loop:	LD	F0	0	R1
	MULTD	F4	F0	F2
	SD	F4	0	R1
	SUBI	R1	R1	#8
	BNEZ		R1	Loop

Assumptions:

- Multiply takes 4 ccs
- Load cache misses require 8 ccs, hits 1 cc

Instruc	tion st	atus_				Execution	Write			
Instruc	tion	j	k	iteration	Issue	complete	Result	_	Busy Add	ress
LD	F0	0	R1	1				Load1	No	
MULT	F4	F0	F2	1				Load2	No	
SD	F4	0	R1	1				Load3	No	Qi
LD	F0	0	R1	2				Store1	No	
MULT	F4	F0	F2	2				Store2	No	
SD	F4	0	R1	2				Store3	No	
Reserv	vation S	Stations	<u> </u>		S1	S2	RS for j	RS for k		
	Time I	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:	
	0 /	Add1	No						LD F0	0 R1
	0 /	Add2	No						MULT F4	F0 F2
	0 /	Add3	No						SD F4	0 R1
	0 1	Mult1	No						SUBI R1	R1 #8
	0 1	Mult2	No						BNEZ R1	Loop
<u>Regist</u>	er resu	ılt status	<u>s</u>							
Cloc	k	R1		F0	F2	F4	F6	F8	F10 F12	2 F30
0		80	Qi					-		

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1				Load2	No			
SD	F4	0	R1	1				Load3	No		Qi	
LD	F0	0	R1	2				Store1	No			
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	<u>s</u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	No						SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	ult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
1		80	Qi	Load1							<u> </u>	

Instructio	n status				Execution	n Write					
Instruction	n <i>j</i>	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD FO)	0 R1	1	1			Load1	Yes	80		
MULT F4	F	0 F2	1	2			Load2	No			
SD F4	ļ	0 R1	1				Load3	No		Qi	
LD FO)	0 R1	2				Store1	No			
MULT F4	F	0 F2	2				Store2	No			
SD F4		0 R1	2				Store3	No			
Reservat	ion Statio	<u>ns</u>		S1	S2	RS for j	RS for k				
Ti	me Name	Bus	у Ор	Vj	Vk	Qj	Qk	Code:	•		
	0 Add1	No						LD	F0	0	R1
	0 Add2	No						MULT	F4	F0	F2
	0 Add3	No						SD	F4	0	R1
	0 Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0 Mult2	No						BNEZ	R1	Loo	p
Register	result sta	<u>tus</u>									
Clock	R1		F0	F2	F4	F6	F8	F10	F12	2	F30
2	80	Qi	Load1		Mult1						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mult	t1
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	sult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
3		80	Qi	Load1		Mult1						

<u>Instruc</u>	tion sta	atus_				Execution	Write					
Instruc	tion	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mult	:1
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reserv	ation S	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time I	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0 /	Add1	No						LD	F0	0	R1
	0 A	Add2	No						MULT	F4	F0	F2
	0 A	Add3	No						SD	F4	0	R1
	1 0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	1 0	Mult2	No						BNEZ	R1	Loo	O
Registe	<u>er resu</u>	<u>lt status</u>	<u>s</u>									
Clock	<	R1		F0	F2	F4	F6	F8	F10	F12	·	F30
4		72	Qi	Load1		Mult1						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mult	1
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	sult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12) 	F30
5		72	Qi	Load1		Mult1		-				

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mult	t1
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	sult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12) 	F30
6		72	Qi	Load1		Mult1						

Instruct	tion sta	atus_				Execution	Write					
Instruct	tion	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD I	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3			Load3	No		Qi	
LD I	F0	0	R1	2	6			Store1	Yes	80	Mult	1
MULT I	F4	F0	F2	2	7			Store2	No			
SD I	F4	0	R1	2				Store3	No			
Reserv	ation S	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time I	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0 A	Add1	No						LD	F0	0	R1
	0 A	Add2	No						MULT	F4	F0	F2
	0 A	Add3	No						SD	F4	0	R1
	0 1	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0 1	Mult2	Yes	MULTD		R(F2)	Load2		BNEZ	R1	Loop)
Register result status												
Clock	(R1		F0	F2	F4	F6	F8	F10	<i>F</i> 12	• • • •	F30
7		72	Qi	Load2		Mult2						

Instructi	on stat	tus_				Execution	<i>Write</i>					
Instructi	on	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD F	0	0	R1	1	1			Load1	Yes	80		
MULT F	4	F0	F2	1	2			Load2	Yes	72		
SD F	4	0	R1	1	3			Load3	No		Qi	
LD F	0	0	R1	2	6			Store1	Yes	80	Mult ²	1
MULT F	4	F0	F2	2	7			Store2	Yes	72	Mult2	2
SD F	4	0	R1	2	8			Store3	No			
Reserva	ation S	tations	<u> </u>		S1	S2	RS for j	RS for k				
7	īme N	lame	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0 A	dd1	No						LD	F0	0	R1
	0 A	dd2	No						MULT	F4	FO I	F2
	0 A	dd3	No						SD	F4	0	R1
	0 M	lult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1 7	#8
	0 M	lult2	Yes	MULTD		R(F2)	Load2		BNEZ	R1	Loop)
Registe	r result	t statu	<u>s</u>									
Clock		R1		F0	F2	F4	F6	F8	F10	F12) 	F30
8		72	Qi	Load2		Mult2						

Instructio	n status				Execution	Write				
Instructio	n <i>j</i>	k	iteration	Issue	complete	Result	_	Busy	Addr	ess
LD F0	() R1	1	1	9		Load1	Yes	80	
MULT F4	- F() F2	1	2			Load2	Yes	72	
SD F4	. () R1	1	3			Load3	No		Qi
LD F0	() R1	2	6			Store1	Yes	80	Mult1
MULT F4	- F() F2	2	7			Store2	Yes	72	Mult2
SD F4	. () R1	2	8			Store3	No		
Reservat	ion Statior	<u>ıs</u>		S1	S2	RS for j	RS for k			
Tii	ne Name	Busy	[,] Ор	Vj	Vk	Qj	Qk	Code:		
	0 Add1	No						LD	F0	0 R1
	0 Add2	No						MULT	F4	F0 F2
	0 Add3	No						SD	F4	0 R1
	0 Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1 #8
	0 Mult2	Yes	MULTD		R(F2)	Load2		BNEZ	R1	Loop
Register	result statı	<u>us</u>								
Clock	R1		F0	F2	F4	F6	F8	F10	F12	? F30
9	64	Qi	Load2		Mult2					

Instructio	n status				Execution	Write				
Instruction	n <i>j</i>	k	iteration	Issue	complete	Result	_	Busy	Addr	ess
LD FO)	0 R1	1	1	9	10	Load1	No		
MULT F	l F	0 F2	1	2			Load2	Yes	72	
SD F4	ļ	0 R1	1	3			Load3	No		Qi
LD FO)	0 R1	2	6	10		Store1	Yes	80	Mult1
MULT F	l F	0 F2	2	7			Store2	Yes	72	Mult2
SD F4	ļ	0 R1	2	8			Store3	No		
Reservat	ion Static	<u>ns</u>		S1	S2	RS for j	RS for k			
Ti	me Name	9 <u>Bu</u>	sy Op	Vj	Vk	Qj	Qk	Code:		
	0 Add1	No						LD	F0	0 R1
	0 Add2	No						MULT	F4	F0 F2
	0 Add3	No						SD	F4	0 R1
	4 Mult1	Ye	s MULTD	M(80)	R(F2)			SUBI	R1	R1 #8
	0 Mult2	Ye	s MULTD		R(F2)	Load2		BNEZ	R1	Loop
Register	result sta	<u>tus</u>								
Clock	R1		F0	F2	F4	F6	F8	F10	F12	? F30
10	64	Qi	Load2		Mult2					

Instruction	status				Execution	1 Write				
Instruction	ı j	k	iteration	Issue	complete	Result		Busy	Addr	ess
LD F0	0	R1	1	1	9	10	Load1	No		
MULT F4	F0	F2	1	2			Load2	No		
SD F4	0	R1	1	3			Load3	Yes	64	Qi
LD F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MULT F4	F0	F2	2	7			Store2	Yes	72	Mult2
SD F4	0	R1	2	8			Store3	No		
Reservation	on Station	<u>s</u>		S1	S2	RS for j	RS for k			
Tim	ne Name	Busy	[,] Ор	Vj	Vk	Qj	Qk	Code:		
	0 Add1	No						LD	F0	0 R1
	0 Add2	No						MULT	F4	F0 F2
	0 Add3	No						SD	F4	0 R1
	3 Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1 #8
	4 Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loop
Register re	esult statu	<u>IS</u>								
Clock	R1		F0	F2	F4	F6	F8	F10	F12	? F30
11	64	Qi			Mult2					

Instructio	n statı	<u>us</u>				Execution	Write				
Instruction	n	j	k	iteration	Issue	complete	Result		Busy	Addr	ess
LD F)	0	R1	1	1	9	10	Load1	No		
MULT F	1	F0	F2	1	2			Load2	No		
SD F4	1	0	R1	1	3			Load3	Yes	64	Qi
LD F)	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MULT F	1	F0	F2	2	7			Store2	Yes	72	Mult2
SD F4	1	0	R1	2	8			Store3	No		
Reservat	ion St	ations	<u>3</u>		S1	S2	RS for j	RS for k			
Ti	me Na	ame	Busy	Ор	Vj	Vk	Qj	Qk	Code:		
	0 Ac	dd1	No						LD	F0	0 R1
	0 Ac	dd2	No						MULT	F4	F0 F2
	0 Ac	td3	No						SD	F4	0 R1
	2 Mu	ult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1 #8
	3 Mu	ult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loop
Register	result	<u>statu</u>	<u>s</u>								
Clock		R1		F0	F2	F4	F6	F8	F10	F12	? F30
12		64	Qi			Mult2					

Instruction	status				Execution	Write				
Instruction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess
LD F0	0	R1	1	1	9	10	Load1	No		
MULT F4	F0	F2	1	2			Load2	No		
SD F4	0	R1	1	3			Load3	Yes	64	Qi
LD F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MULT F4	F0	F2	2	7			Store2	Yes	72	Mult2
SD F4	0	R1	2	8			Store3	No		
Reservatio	n Stations	<u>s</u>		S1	S2	RS for j	RS for k			
Tim	e Name	Busy	[,] Ор	Vj	Vk	Qj	Qk	Code:		
(0 Add1	No						LD	F0	0 R1
(0 Add2	No						MULT	F4	F0 F2
(0 Add3	No						SD	F4	0 R1
	1 Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1 #8
:	2 Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loop
Register re	esult statu	<u>s</u>						_		
Clock	R1		F0	F2	F4	F6	F8	F10	F12	? F30
13	64	Qi			Mult2					

Instru	ction s	tatus_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14		Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mult	t1
MULT	F4	F0	F2	2	7			Store2	Yes	72	Mult	2
SD	F4	0	R1	2	8			Store3	No			
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1	#8
	1	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo	p
Regis	ter res	ult statu	<u>s</u>									
Cloc	k	R1		<i>F</i> 0	F2	F4	F6	F8	F10	F12	·	F30
14		64	Qi			Mult2						

Instructio	n statu	<u>s</u>				Execution	Write					
Instructio	n <i>j</i>		k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD F0		0	R1	1	1	9	10	Load1	No			
MULT F4		F0	F2	1	2	14	15	Load2	No			
SD F4		0	R1	1	3			Load3	Yes	64	Qi	
LD F0		0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT F4		F0	F2	2	7	15		Store2	Yes	72	Mult	2
SD F4		0	R1	2	8			Store3	No			
Reservat	ion Sta	tions	<u>3</u>		S1	S2	RS for j	RS for k				
Tii	ne Nai	me	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0 Add	11	No						LD	F0	0	R1
	0 Add	12	No						MULT	F4	F0	F2
	0 Add	8t	No						SD	F4	0	R1
	0 Mul	lt1	No						SUBI	R1	R1	#8
	0 Mul	lt2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo)
Register	result s	tatu	<u>s</u>									
Clock	R	1		F0	F2	F4	F6	F8	F10	F12) 	F30
15	6	4	Qi			Mult2						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7)	2)*R(7:
SD	F4	0	R1	2	8			Store3	No			
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	sult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
16		64	Qi			Mult1						

Instruc	tion st	atus_				Execution	Write					
Instruc	tion	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7)	2)*R(7:
SD	F4	0	R1	2	8			Store3	Yes	64	Mult	:1
Reserv	ation :	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Registe	er resu	ult status	<u>s</u>									
Clock	<	R1		F0	F2	F4	F6	F8	F10	F12	2	F30
17		64	Qi			Mult1						

Instruct	tion sta	atus_				Execution	Write				
Instruct	tion	j	k	iteration	Issue	complete	Result		Busy	Addr	ess
LD I	F0	0	R1	1	1	9	10	Load1	No		
MULT I	F4	F0	F2	1	2	14	15	Load2	No		
SD I	F4	0	R1	1	3	18		Load3	Yes	64	Qi
LD I	F0	0	R1	2	6	10	11	Store1	Yes	80	M(80)*R(F
MULT I	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(72)*R(72
SD I	F4	0	R1	2	8			Store3	Yes	64	Mult1
Reserv	ation S	Stations	<u> </u>		S1	S2	RS for j	RS for k			
•	Time I	Vame	Busy	Ор	Vj	Vk	Qj	Qk	Code:		
	0 A	Add1	No						LD	F0	0 R1
	0 A	Add2	No						MULT	F4	F0 F2
	0 A	Add3	No						SD	F4	0 R1
	0 1	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1 #8
	0 1	Mult2	No						BNEZ	R1	Loop
Registe	er resu	It status	<u>s</u>								
Clock	(R1		F0	F2	F4	F6	F8	F10	F12	2 F30
18		56	Qi			Mult1					

Instruct	ion st	atus_				Execution	Write				
Instruct	ion	j	K	iteration	Issue	complete	Result		Busy	Addr	ess
LD F	- 0	0	R1	1	1	9	10	Load1	No		
MULT F	-4	F0	F2	1	2	14	15	Load2	No		
SD F	-4	0	R1	1	3	18	19	Load3	Yes	64	Qi
LD F	-0	0	R1	2	6	10	11	Store1	No		
MULT F	- 4	F0	F2	2	7	15	16	Store2	Yes	72	M(72)*R(72
SD F	- 4	0	R1	2	8			Store3	Yes	64	Mult1
Reserva	ation (Stations	<u> </u>		S1	S2	RS for j	RS for k			
7	Гіте	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:		
	0 /	Add1	No						LD	F0	0 R1
	0 /	Add2	No						MULT	F4	F0 F2
	0 /	Add3	No						SD	F4	0 R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1 #8
	0	Mult2	No						BNEZ	R1	Loop
Registe	r resu	ılt statu:	<u>s</u>								
Clock		R1		F0	F2	F4	F6	F8	F10	F12	? F30
19		56	Qi			Mult1					

Instruc	ction s	<u>tatus</u>										
Instruc	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18	19	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	No			
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7:
SD	F4	0	R1	2	8	20		Store3	Yes	64	Mult	:1
Reservation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Register result status												
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12	2	F30
20		56	Qi			Mult1						

Instruction status					Execution Write							
Instru	ction	j	k	iteration	Issue	complete	Result	_	Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18	19	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	No			
MULT	F4	F0	F2	2	7	15	16	Store2	No			
SD	F4	0	R1	2	8	20	21	Store3	Yes	64	Mult	1
Reser	vation	Stations	<u> </u>		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loop)
Register result status												
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12	2	F30
21		56	Qi			Mult1						