4 July 2011 -- Computer Architectures -- part 2/2

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Question 1

Considering the MIPS64 architecture presented in the following:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP multiplier unit: pipelined 8 stages
- FP arithmetic unit: pipelined 2 stages
- FP divider unit: not pipelined unit that requires 8 clock cycles
- branch delay slot: 1 clock cycle, and the branch delay slot is not enable
- forwarding is enabled
- it is possible to complete instruction EXE stage in an out-of-order fashion.
- o and using the following code fragment, show the timing of the presented loop-based program and compute how many cycles does this program take to execute?

	.data					
V1:	.double "100 values"					
V2:	.double "100 values"					
V3:	.double "100 values"					
V4:	.double "100 values"					
V5:	.double "100 zeroes"					

.text

main:	daddui r1,r0,0			
	daddui r2,r0,100			
loop:	l.d f1,v1(r1)			
	1.d f2,v2(r1)			
	1.d f3,v3(r1)			
	1.d f4,v4(r1)			
	div.d f6,f3,f4			
	div.d f7,f1,f2			
	mul.d f5,f6,f7			
	s.d f5,v5(r1)			
	daddui r1,r1,8			
	daddi r2,r2,-1			
	bnez r2,loop			
	halt			

comments	Clock cycles			
r1← pointer	5			
r2 <= 100	1			
f1 <= v1[i]	1			
f2 <= v2[i]	1			
f3 <= v3[i]	1			
f4 <= v4[i]	1			
$f6 \le v3[i]/v4[i]$	9			
f7 <= v1[i]/v2[i]	8			
f5 <= f6*f7	8			
	1			
r1 <= r1 + 8	1			
r2 <= r2 - 1	1			
	2			
	1			
	2507			
	3506			
1				

total

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Question 2

Considering the same loop-based program, and assuming the following processor architecture for a superscalar MIPS64 processor implemented with multiple-issue and speculation:

- issue 2 instructions per clock cycle
- jump instructions require 1 issue
- handle 2 instructions commit per clock cycle
- timing facts for the following separate functional units:
 - i. 1 Memory address 1 clock cycle
 - ii. 1 Integer ALU 1 clock cycle
 - iii. 1 Jump unit 1 clock cycle
 - iv. 1 FP multiplier unit, which is pipelined: 8 stages
 - v. 1 FP divider unit, which is not pipelined: 8 clock cycles
 - vi. 1 FP Arithmetic unit, which is pipelined: 2 stages
- Branch prediction is always correct
- There are no cache misses
- There are 2 CDB (Common Data Bus).

o Complete the table reported below showing the processor behavior for the 2 initial iterations.

0

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	I.d f1,v1(r1)	1	2m	3	4	5
1	I.d f2,v2(r1)	1	3m	4	5	6
1	l.d f3,v3(r1)	2	4m	5	6	7
1	l.d f4,v4(r1)	2	5m	6	7	8
1	div.d f6,f3,f4	3	14d		22	23
1	div.d f7,f1,f2	3	6d		14	23
1	mul.d f5,f6,f7	4	23x		31	32
1	s.d f5,v5(r1)	4	6m			32
1	daddui r1,r1,8	5	6i		7	33
1	daddi r2,r2,-1	5	7i		8	33
1	bnez r2,loop	6	9j			34
2	l.d f1,v1(r1)	7	8m	9	10	34
2	I.d f2,v2(r1)	7	9m	10	11	35
2	l.d f3,v3(r1)	8	10m	11	12	35
2	l.d f4,v4(r1)	8	11m	12	13	36
2	div.d f6,f3,f4	9	22d		30	36
2	div.d f7,f1,f2	9	30d		38	39
2	mul.d f5,f6,f7	10	39x		47	48
2	s.d f5,v5(r1)	10	12m			48
2	daddui r1,r1,8	11	12i		13	49
2	daddi r2,r2,-1	11	13i		14	49
2	bnez r2,loop	12	15j			50