

Architetture dei sistemi di elaborazione

Esame del 27.6.2019 - parte I

A1

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Question #2

Considering the MIPS64 architecture presented in the following:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP arithmetic unit: pipelined, 2 stages
- FP multiplier unit: pipelined, 6 stages
- FP divider unit: unpipelined, 10 stages
- branch delay slot: 1 clock cycle, and the branch delay slot is not enabled
- forwarding is enabled
- it is possible to complete instruction EXE stage in an out-of-order fashion.

Considering the following code fragment, show the timing of the loop-based program and compute how many cycles does this program take to execute, filling the table.

```
; ***** MIPS64 *****
; for (i = 0; i < 10; i++) {
;     v5[i] = v1[i]*v2[i] - v3[i]/v4[i];
; }
```

```
.data
V1: .double "10 values"
V2: .double "10 values"
V3: .double "10 values"
...
V5: .double "10 zeros"
```

```
.text
main: daddui r1,r0,0
      daddui r2,r0,10
loop: l.d f1,v1(r1)
      l.d f2,v2(r1)
      mul.d f5,f1,f2
      l.d f3,v3(r1)
      l.d f4,v4(r1)
      div.d f6, f3, f4
      sub.d f5,f5,f6
      s.d f5,v5(r1)
      daddui r1,r1,8
      daddi r2,r2,-1
      bnez r2,loop
      halt
```

total

comments	Clock cycles
r1 ← pointer	5
r2 ≤ 10	1
f1 ≤ v1[i]	1
f2 ≤ v2[i]	1
f5 ≤ v1[i]*v2[i]	7
f3 ≤ v3[i]	0
f4 ≤ v4[i]	0
f6 ≤ v3[i]/v4[i]	8
f5 ≤ f5-f6	2
v5[i] ≤ f5	1
r1 ≤ r1 + 8	1
r2 ≤ r2 - 1	1
	2
	1
total	256

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[illegible]