Power control

R. Ferrero , P. Bernardi

Politecnico di Torino

Dipartimento di Automatica e Informatica (DAUIN)

Torino - Italy

Power saving mechanisms

- Entering into a power control mode
  - Sleep mode
  - Deep Sleep mode
  - Power-down mode
  - Deep Power-down mode
- Reducing CPU clock frequency
  - changing clock source
  - configuring PLL values
  - altering the value of CPU clock divider
- shutting down clocks of individual peripherals.

Sleep mode

- The clock to the core is stopped.
  - no more power used by the processor, memory systems and its controllers, and internal buses.
- The SMFLAG bit in PCON is set.
- Peripheral functions continue operation
  - they may generate interrupts to cause the processor to resume execution.
- Wake-up: when any enabled interrupt occurs.

Deep Sleep mode

- All clocks are stopped, except IRC and RTC.
  - all dynamic operations of the chip are suspended.
- The DSFLAG bit in PCON is set.
- Wake-up: when some interrupts occur, like:
  - external interrupts EINT0-EINT3
  - watchdog timer (driven by IRC clock)
  - RTC alarm interrupt
  - GPIO interrupts
  - NMI.

Power-down mode

- Same as deep sleep mode; in addition flash memory is turned off
  - higher power savings, but waking-up takes more time: flash operation must be resubmitted.
- The PDFLAG bit in PCON is set.
- Wake-up: same kinds of interrupt as deep sleep mode.

Deep Power-down mode

- The entire chip is powered off, except:
  - real-time clock
  - RESET pin
  - Wake-up Interrupt Controller
  - RTC backup registers
- The DPDFLAG bit in PCON is set.
- Wake-up:
  - external reset
  - RTC alarm interrupt.

Entering into a power control mode

- Two instructions suspend execution and enter a low-power state:
  - `WFI`: Wait For Interrupt
  - `WFE`: Wait For Event
- With both instructions, the processor remains in low-power state until it detects an interrupt.
- In a multiprocessor system, the low-power state after `WFE` can be exited also when another process executes a `SEV` instruction.

Power control registers (page 62)

- The power control function uses two registers
- When debugging, the content of the registers can be seen in Peripheral -> Clocking & power Control -> Power Control.

Table 43. Power Control registers

Name	Description	Access	Reset value[1]	Address
PCON	Power Control Register. This register contains control bits that enable some reduced power operating modes of the LPC176x/5x. See Table 44.	R/W	0x00	0x400F C0C0
PCONP	Power Control for Peripherals Register. This register contains control bits that enable and disable individual peripheral functions, allowing elimination of power consumption by peripherals that are not needed.	R/W		0x400F C0C4

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

PCON register (page 63)

selection of power mode

brown-out disabling

exclusive flags for power mode

Table 44. Power Mode Control register (PCON - address 0x400F C0C0) bit description

Bit	Symbol	Description	Reset value
0	PM0	Power mode control bit 0. This bit controls entry to the Power-down mode. See Section 4.8.7.1 below for details.	0
1	PM1	Power mode control bit 1. This bit controls entry to the Deep Power-down mode. See Section 4.8.7.1 below for details.	0
2	$\overline{\text{BODRPM}}$	Brown-Out Reduced Power Mode. When BODRPM is 1, the Brown-Out Detect circuitry will be turned off when chip Power-down mode or Deep Sleep mode is entered, resulting in a further reduction in power usage. However, the possibility of using Brown-Out Detect as a wake-up source from the reduced power mode will be lost. When 0, the Brown-Out Detect function remains active during Power-down and Deep Sleep modes. See the System Control Block chapter for details of Brown-Out detection.	0
3	$\overline{\text{BOGD}}$[1]	Brown-Out Global Disable. When BOGD is 1, the Brown-Out Detect circuitry is fully disabled at all times, and does not consume power. When 0, the Brown-Out Detect circuitry is enabled. See the System Control Block chapter for details of Brown-Out detection. **Note:** the Brown-Out Reset Disable (BORD, in this register) and the Brown-Out Interrupt (xx) must be disabled when software changes the value of this bit.	0
4	$\overline{\text{BORD}}$	Brown-Out Reset Disable. When BORD is 1, the BOD will not reset the device when the $V_{DD(REG)(3V3)}$ voltage dips goes below the BOD reset trip level. The Brown-Out interrupt is not affected. When BORD is 0, the BOD reset is enabled. See the Section 3.5 for details of Brown-Out detection.	0
7:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	SMFLAG	Sleep Mode entry flag. Set when the Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
9	DSFLAG	Deep Sleep entry flag. Set when the Deep Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
10	PDFLAG	Power-down entry flag. Set when the Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
11	DPDFLAG	Deep Power-down entry flag. Set when the Deep Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][4]
31:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

PCONP register

- Each bit of PCONP turns off an individual peripheral by gating off its clock source.
  - see the complete list in the user manual, page 65.
- Few peripheral functions cannot be turned off
  - Watchdog timer
  - Pin Connect block
  - System Control block.
- Some peripherals have a separate disable control if their power consumption is not clock dependent (e.g., analog functions).

System Control Register (page 784)

- Content is shown in Peripheral -> Core peripherals -> System control and configuration.

Table 662. SCR bit assignments

Bits	Name	Function
[31:5]	-	Reserved.
[4]	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wakeup the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an `SEV` instruction or an external event.
[3]	-	Reserved.
[2]	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep.
[1]	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	-	Reserved.

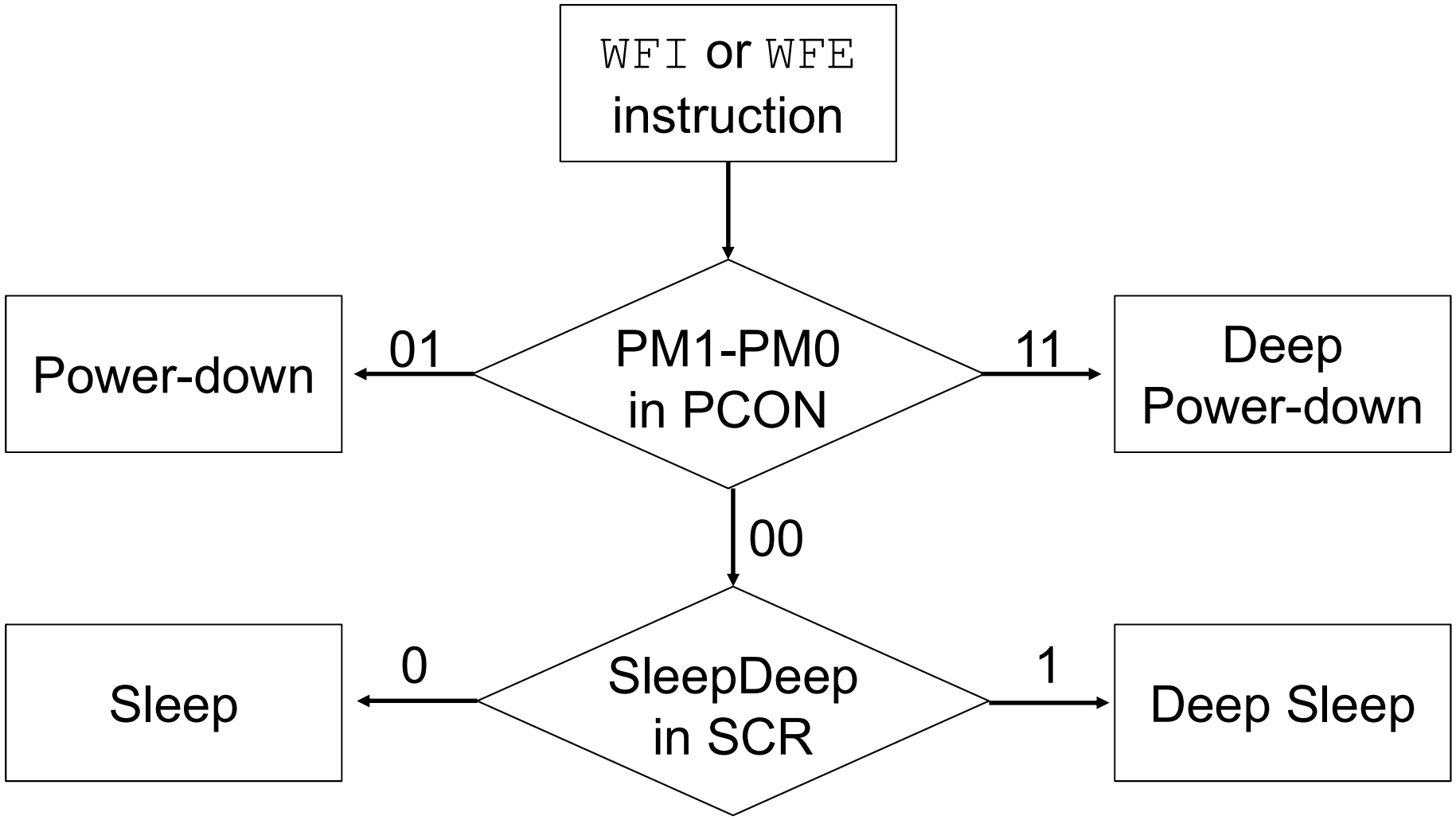
Power control according to manual

Table 45. Encoding of reduced power modes

PM1, PM0	Description
00	Execution of WFI or WFE enters either Sleep or Deep Sleep mode as defined by the SLEEPDEEP bit in the Cortex-M3 System Control Register.
01	Execution of WFI or WFE enters Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.
10	Reserved, this setting should not be used.
11	Execution of WFI or WFE enters Deep Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.

PM1-PM0	SLEEPDEEP	
	0	1
00	Sleep	Deep sleep
01	-	Power-down
11	-	Deep Power-down

Power control in practice



Debug limitations

- Very important: do not use Deep Sleep and Deep Power-down modes while debugging!
  - the board cannot wake up in the usual manner.
- A debug event like single stepping is a wake-up event
  - `WFI` and `WFE` do not have effect if debugged step by step.
- Power savings during debugging is lower than during normal execution.