27 January 2014 -- Computer Architectures –- part 2/2

Name, Student ID .....

Question 1

Considering the following processor architecture for a superscalar MIPS64 processor implemented with multiple-issue and speculation:

- issue 2 instructions per clock cycle
- jump instructions require 1 issue
- handle 2 instructions commit per clock cycle
- timing facts for the following separate functional units:
  i. 1 Memory address 1 clock cycle
  ii. 1 Integer ALU 1 clock cycle
  iii. 1 Jump unit 1 clock cycle
  iv. 1 FP multiplier unit, which is pipelined: 8 stages
  v. 1 FP divider unit, which is not pipelined: 10 clock cycles
  vi. 1 FP Arithmetic unit, which is pipelined: 4 stages
- Branch prediction is always correct
- There are no cache misses
- There are 2 CDB (Common Data Bus).

o Complete the table reported below showing the processor behavior for the 2 initial iterations of the reported loop-based program.

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	l.d f1,v1(r1)	1	2M	3	4	5
1	l.d f2,v2(r1)	1	3M	4	5	6
1	l.d f3,v3(r1)	2	4M	5	6	7
1	mul.d f4,f1,f2	2	6X		14	15
1	s.d f4,v4(r1)	3	5M			15
1	sub.d f4,f1,f2	3	6A		10	16
1	div.d f2,f1,f3	4	7D		17	18
1	add.d f1,f4,f2	4	18A		22	23
1	s.d f1,v5(r1)	5	6M			23
1	daddui r1,r1,8	5	6I		7	24
1	daddi r2,r2,-1	6	7I		8	24
1	bnez r2,loop	7	9J			25
2	l.d f1,v1(r1)	8	9M	10	11	25
2	l.d f2,v2(r1)	8	10M	11	12	26
2	l.d f3,v3(r1)	9	11M	12	13	26
2	mul.d f4,f1,f2	9	13X		21	27
2	s.d f4,v4(r1)	10	12M			27
2	sub.d f4,f1,f2	10	13A		17	28
2	div.d f2,f1,f3	11	17D		27	28
2	add.d f1,f4,f2	11	28A		32	33
2	s.d f1,v5(r1)	12	13M			33
2	daddui r1,r1,8	12	13I		14	34
2	daddi r2,r2,-1	13	14I		15	34
2	bnez r2,loop	14	16J			35

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Question 2

Considering a (2,2) correlating predictor of 1K entries, and assuming that the processor executes the following code fragment, determine the BPU final state and calculate the final misprediction ratio in the presented case. The BPU initial state is indicated in the table.

General assumptions:

- R10 is the main loop control register and it is initialized to 100, then, the program iterates 100 times.
- R3 is the reference value, set to 1
- R2 is the input register
  - the input value for R2 is the sequence of integer numbers starting from 0 (in the first iteration) to 99 (during the last iteration), i.e., [0,1,2,3,4,5…99]
- The initial value of the BPU 2-bit shit register is 00
- The grayed instructions in the program do not contain any branch or jump instruction

R3 = 1
R2 = 0 .. 99
R10 = 100

ITERATION 1 2 3 4 5 100
EVEN ITERATIONS

Address	Instruction	2-bit predictors				2-bit shift register	misprediction counting
		00	01	10	11	00-11-01-11-01	
0x0000	L0: …	0	0	0	0		
…	; Reading input values in R2	0	0	0	0		
0x0020	AND R1, R2, R3	0	0	0	0		
0x0024	BEQZ R1, L1	0 1	0 1 2 3	0	0 0 0	01-10-11-10-11-...	1 1 2 2 3 3
0x0028	…	0	0	0	0		
0x002C	L1: XOR R4, R1, R3	0	0	0	0		
0x0030	BEQZ R4, L2	0	0 0	0 1 2 3	0 0 0	10-01-10-01-10-...	0 1 1 2 2 2
0x0034	…	0	0	0	0		
0x0038	L2: AND R5, R1, R3	0	0	0	0		
0x003C	BEQZ R5, L3	0	0 0	0 1 2 3	0	01-10-01-10-01-10	1 1 2 2 2 2
0x0040	L3: …	0	0	0	0		
0x0050	DADDI R10, R10, #-1	0	0	0	0		
0x0054	BNEZ R10, L0	0	0 1 2 3	0 1 2 3 2	0	11-01-11-01-11-00-...	1 2 3 4 4 4 5
	…	0	0	0	0		

misprediction ratio $= \frac{3+2+2+5}{4 \cdot 100} \cdot 100 = \frac{12}{400} \cdot 100 = 3\%$

SUM OF FINAL VALUES OF MISPREDICTION COUNTING

NUMBER OF BRANCHES

NUMBER OF ITERATIONS