ARM Cortex-A8
Intel Core i7

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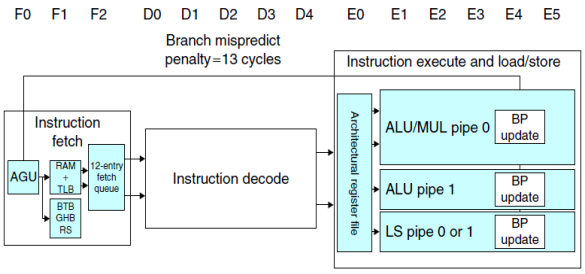
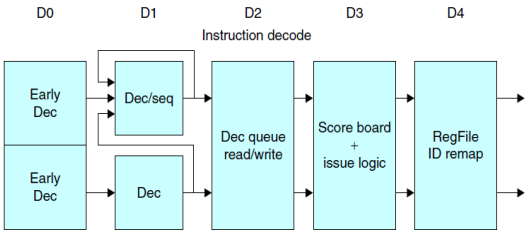
ARM Cortex-A8

- Introduced by ARM in 2005, it is the first processor supporting the ARMv7-A architecture.
- First ARM superscalar processor, running at high frequencies: from 600MHz to 1GHz.
- Used in Personal Mobile Devices (PMDs), mainly in smart phones and tablets.
- Main characteristics:
  - Dual issue
  - Statically scheduled
  - Dynamic issue detection
  - Dynamic branch prediction two-level with a BTB.

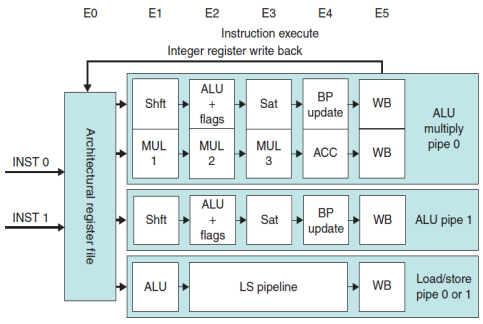
A8 pipeline



Decode unit



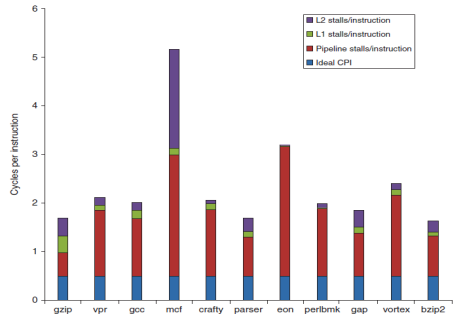
Execution unit



Pipeline stalls

- Structural hazards
  - 2 instructions in the issue packet use the same functional unit
- Data hazards
  - It is a compiler task to avoid data hazards
- Control hazards
  - Misprediction penalty: 13 cc

A8 performance



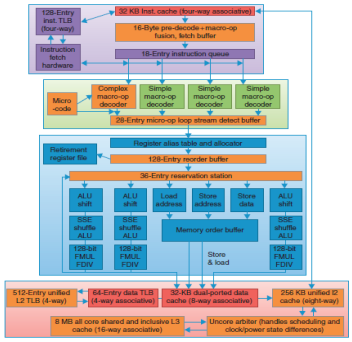
ARM Cortex-A9

- It is a dynamically scheduled superscalar processor using speculation
- issues up to two instructions per clock cycle
- up to four instructions (two ALUs, one load/store or FP/multimedia, and one branch) can begin execution in a clock cycle
- uses a more powerful branch predictor, instruction cache prefetch, and a nonblocking L1 data cache.

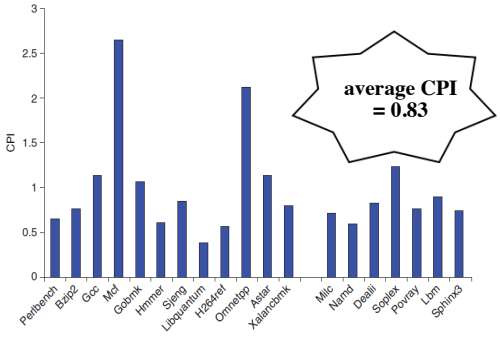
Intel core i7

- Intel 64-bit x86-64 processor introduced in 2008. Superscalar processor core with out-of-order and speculation features.
- Distributed as multicore devices for the desktop and laptop markets.
  - 3 cache levels
  - 45 nm
  - ~ 730 million transistors
  - High clock frequencies: 2.66 GHz – 3.20 GHz

Intel Core i7 pipeline



Processor performance



Area	Specific characteristic	Intel i7 920 Four cores, each with FP	ARM A8 One core, no FP	Intel Atom 230 One core, with FP
Physical chip properties	Clock rate	2.66 GHz	1 GHz	1.66 GHz
	Thermal design power	130 W	2 W	4 W
	Package	1366-pin BGA	522-pin BGA	437-pin BGA
Memory system	TLB	Two-level All four-way set associative 128 I/64 D 512 L2	One-level fully associative 32 I/32 D	Two-level All four-way set associative 16 I/16 D 64 L2
	Caches	Three-level 32 KB/32 KB 256 KB 2–8 MB	Two-level 16/16 or 32/32 KB 128 KB–1MB	Two-level 32/24 KB 512 KB
	Peak memory BW	17 GB/sec	12 GB/sec	8 GB/sec
Pipeline structure	Peak issue rate	4 ops/clock with fusion	2 ops/clock	2 ops/clock
	Pipeline scheduling	Speculating out of order	In-order dynamic issue	In-order dynamic issue
	Branch prediction	Two-level	Two-level 512-entry BTB 4K global history 8-entry return stack	Two-level