Lab 2 Multiplexers, Design Hierarchy, and HEX Displays

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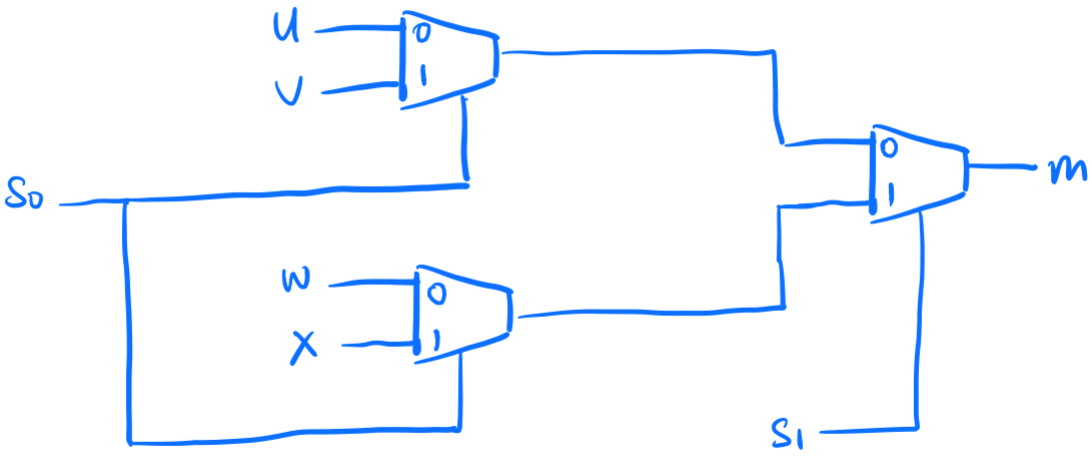
Part II

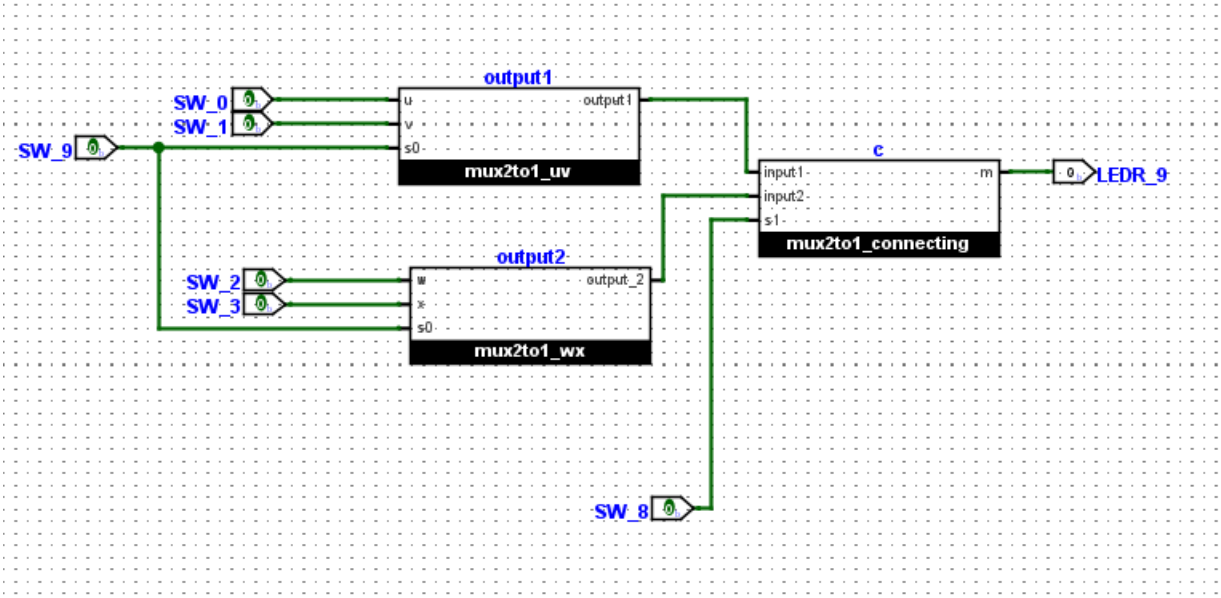
1. 6 variables are needed, so there will be $2^6 = 64$ rows.

2. We can use three $mux2to1$ to connect a 4-to-1 multiplexer.



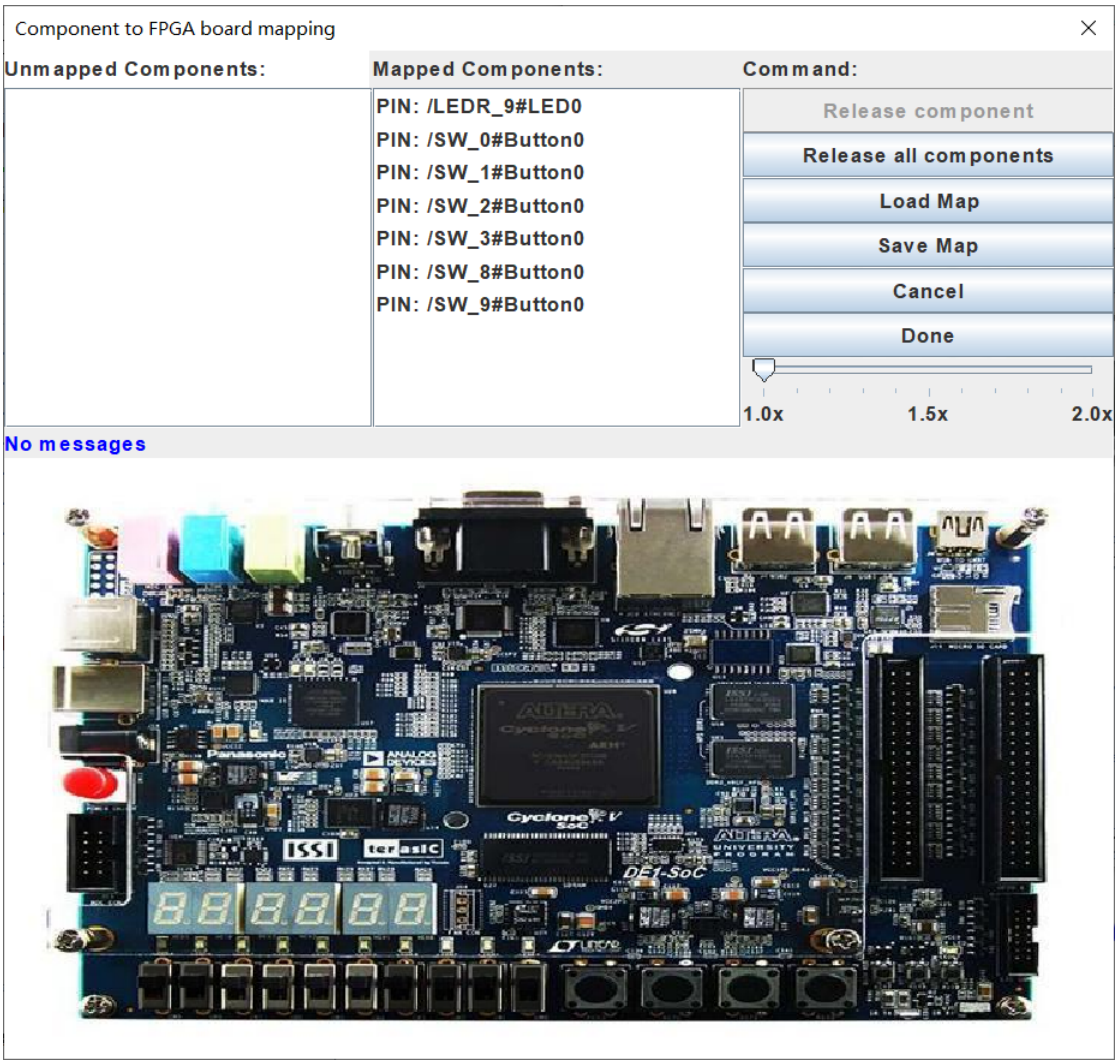
   In this design, s_0 decides the output of the two multiplexers on the left, s_1 decides the output of m.

3.



4. if $s_1s_0 = 00$, output value is determined by u, if $s_1s_0 = 01$, output value is determined by v, if $s_1s_0 = 10$, output value is determined by w, if $s_1s_0 = 11$, output value is determined by x.

5.


Component to FPGA board mapping
Unmapped Components:
Mapped Components:
Command:
PIN: /LEDR_9#LED0
PIN: /SW_0#Button0
PIN: /SW_1#Button0
PIN: /SW_2#Button0
PIN: /SW_3#Button0
PIN: /SW_8#Button0
PIN: /SW_9#Button0
Release component
Release all components
Load Map
Save Map
Cancel
Done
1.0x
1.5x
2.0x
No messages
DE1-SoC

Part III

1. segment 0 truth table:

z	y	x	w	HEX[0]
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	0	1	1
$\overline{z} * y$	0	1	1	1
$z * y$	1	0	1	1
$z * \overline{y}$	1	1	0	1

output: $u = x'y'z + w'y'z' + wyz' + xz' + xy + w'z$

segment 1 truth table:

z	y	x	w	HEX[1]
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	1	1	1
$\overline{z} * y$	1	0	1	0
$z * y$	0	1	0	0
$z * \overline{y}$	1	1	0	1

output: $u = w'x'z' + wxz' + w'y'z + y'z' + wx'z$

segment 2 truth table:

z	y	x	w	HEX[2]
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	1	1	0
$\overline{z} * y$	1	1	1	1
$z * y$	0	1	0	0
$z * \overline{y}$	1	1	1	1

output: $u = x'z' + wz' + yz' + x'w + y'z$

segment 3 truth table:

z	y	x	w	HEX[3]
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	0	1	1
$\overline{z} * y$	0	1	0	1
$z * y$	1	1	0	1
$z * \overline{y}$	1	1	1	0

output: $u = wx'y + wxy' + x'z + w'y'z' + w'xy$

segment 4 truth table:

z	y	x	w	HEX[4]
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	0	0	1
$\overline{z} * y$	0	0	0	1
$z * y$	1	1	1	1
$z * \overline{y}$	1	0	1	1

output: $u = w'x + yz + xz + w'x'y'$

segment 5 truth table:

z	y	x	w	HEX[5]
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Karnaugh Map:

	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	1	0	0	0
$\overline{z} * y$	1	1	0	1
$z * y$	1	0	1	1
$z * \overline{y}$	1	1	1	1

output: $u = w'x' + x'yz' + y'z + w'y + xz$

segment 6 truth table:

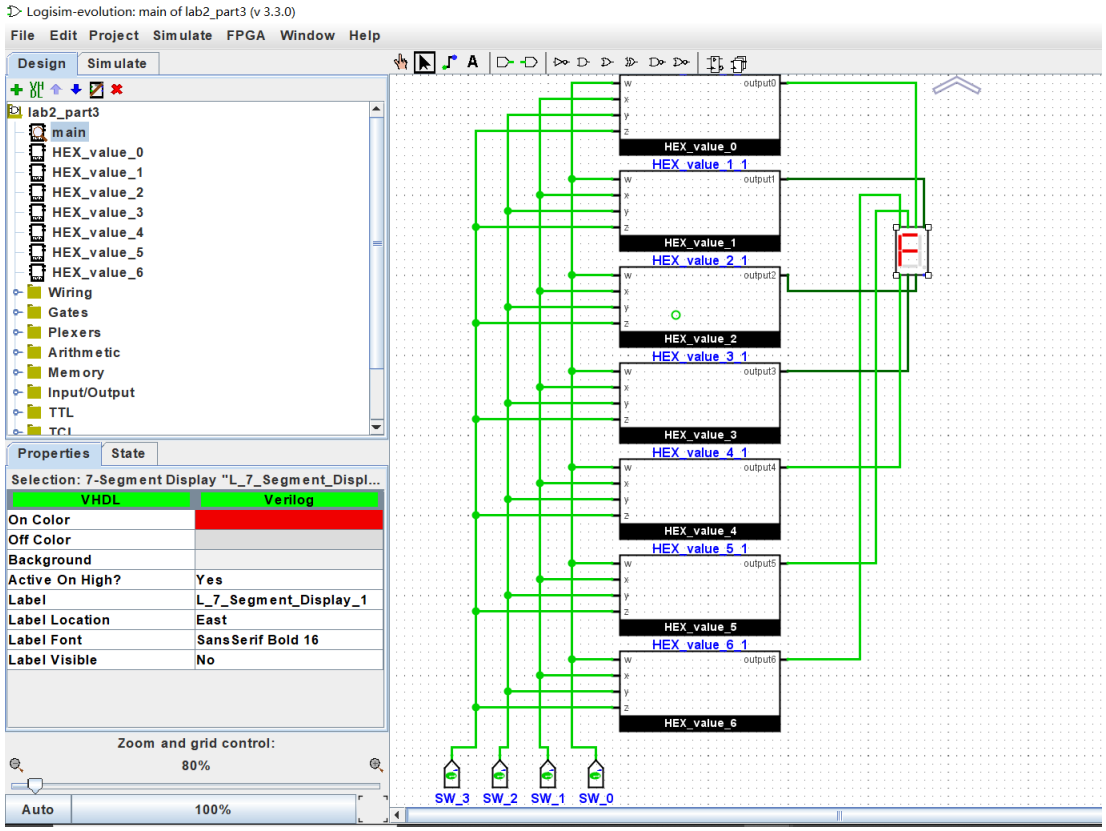
z	y	x	w	HEX[6]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Karnaugh Map:

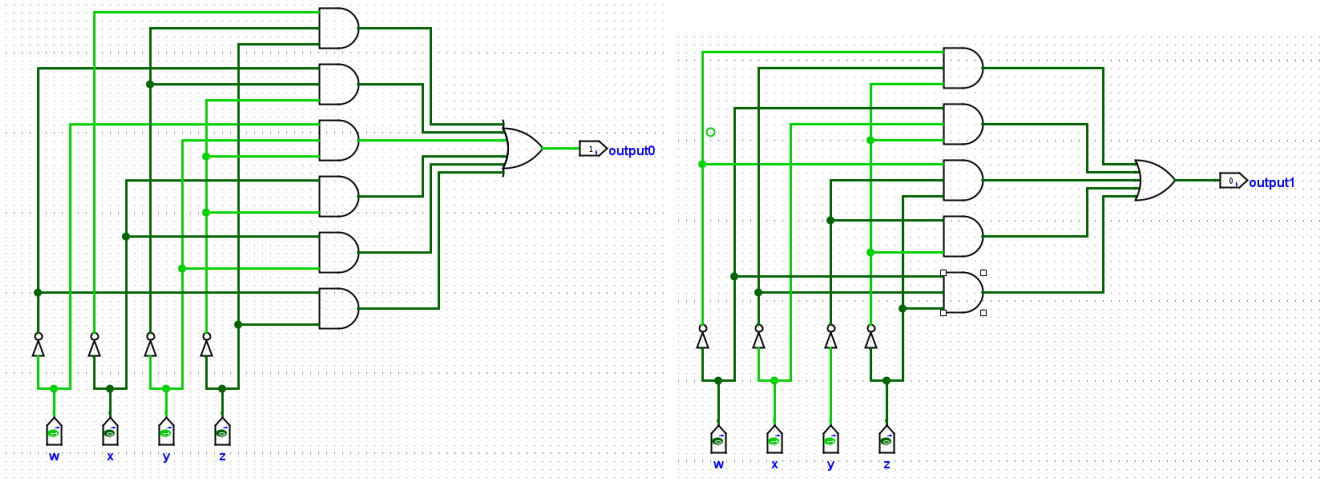
	$\overline{x} * \overline{w}$	$\overline{x} * w$	$x * w$	$x * \overline{w}$
$\overline{z} * \overline{y}$	0	0	1	1
$\overline{z} * y$	1	1	0	1
$z * y$	0	1	1	1
$z * \overline{y}$	1	1	1	1

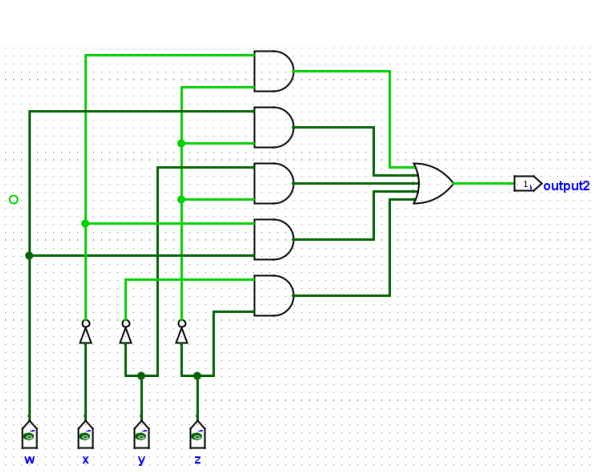
output: $u = x'yz' + w'x + y'z + xy' + wz$.

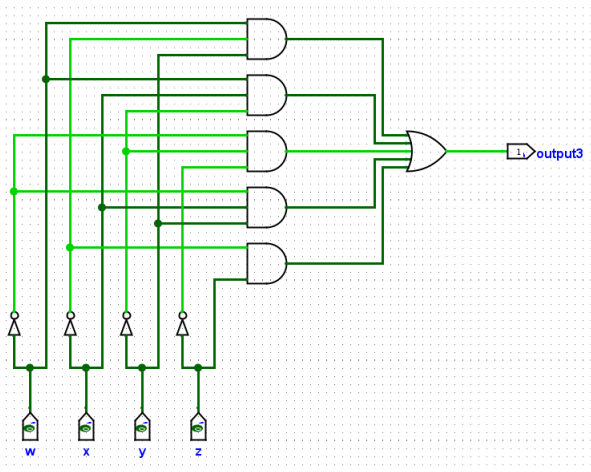
2.

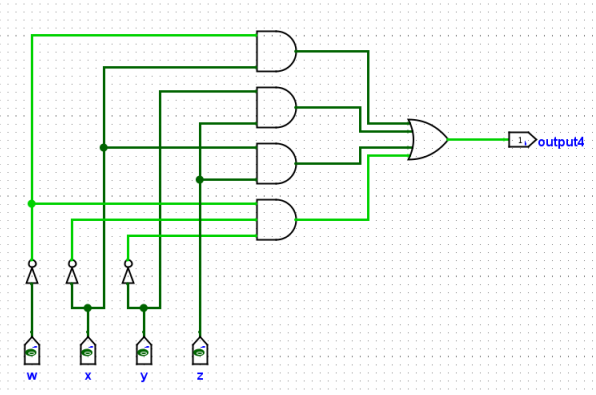


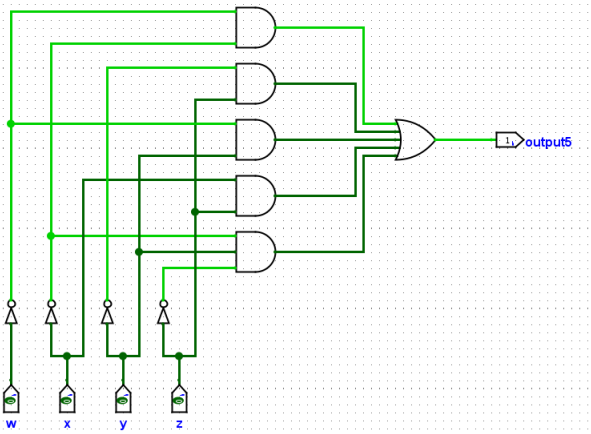
Below are circuit for each HEX value, respectively.



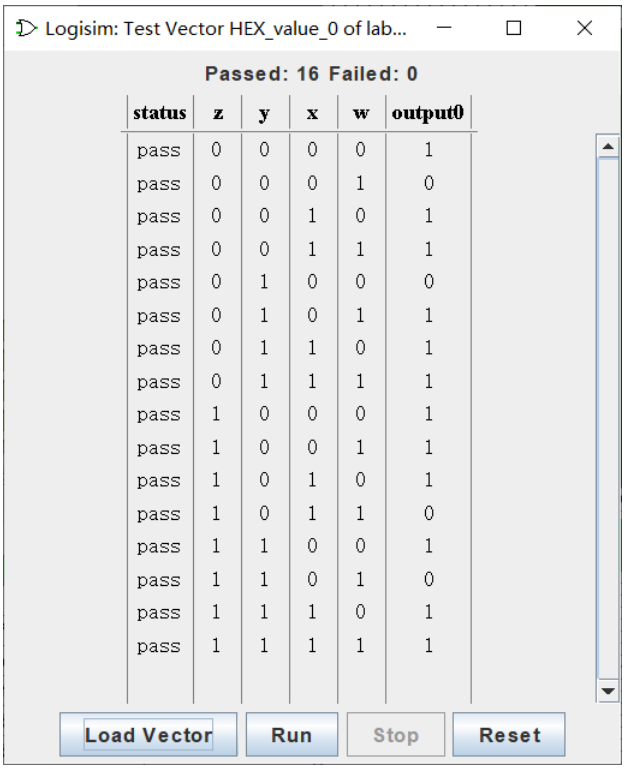

output2
w
x
y
z


output3
w
x
y
z


output4
w
x
y
z


output5
w
x
y
z

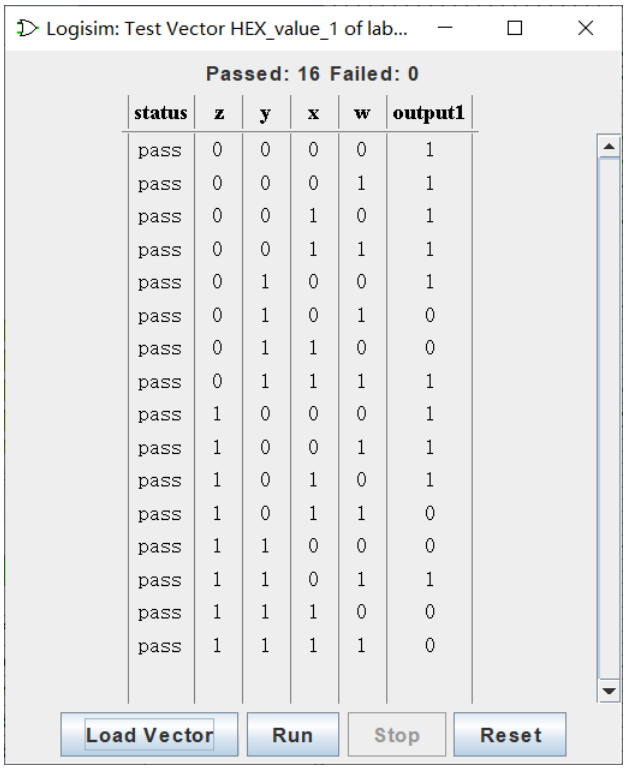
3. The followings are the screenshots of test vectors for each module, respectively.


Logisim: Test Vector HEX_value_0 of lab...

Passed: 16 Failed: 0

status	z	y	x	w	output0
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	0
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	0
pass	1	1	0	0	1
pass	1	1	0	1	0
pass	1	1	1	0	1
pass	1	1	1	1	1

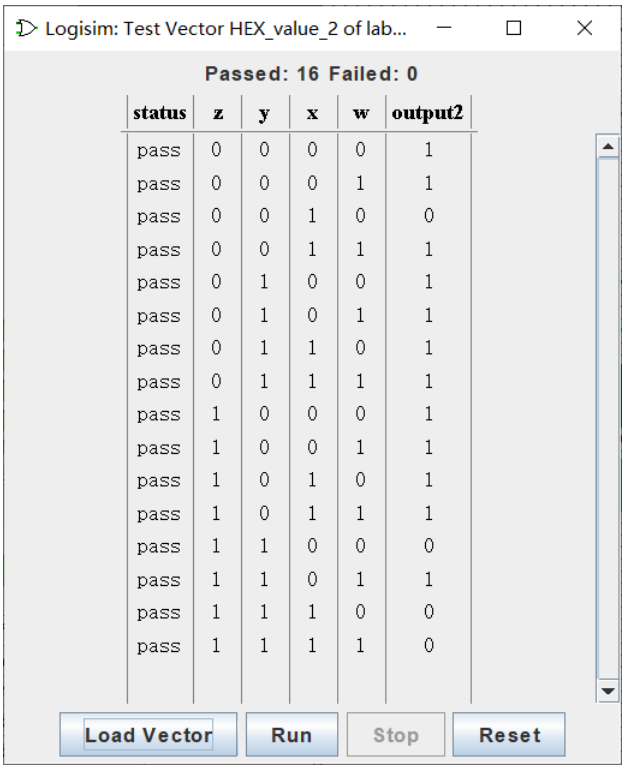
Load Vector | Run | Stop | Reset


Logisim: Test Vector HEX_value_1 of lab...

Passed: 16 Failed: 0

status	z	y	x	w	output1
pass	0	0	0	0	1
pass	0	0	0	1	1
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	1
pass	0	1	0	1	0
pass	0	1	1	0	0
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	0
pass	1	1	0	0	0
pass	1	1	0	1	1
pass	1	1	1	0	0
pass	1	1	1	1	0

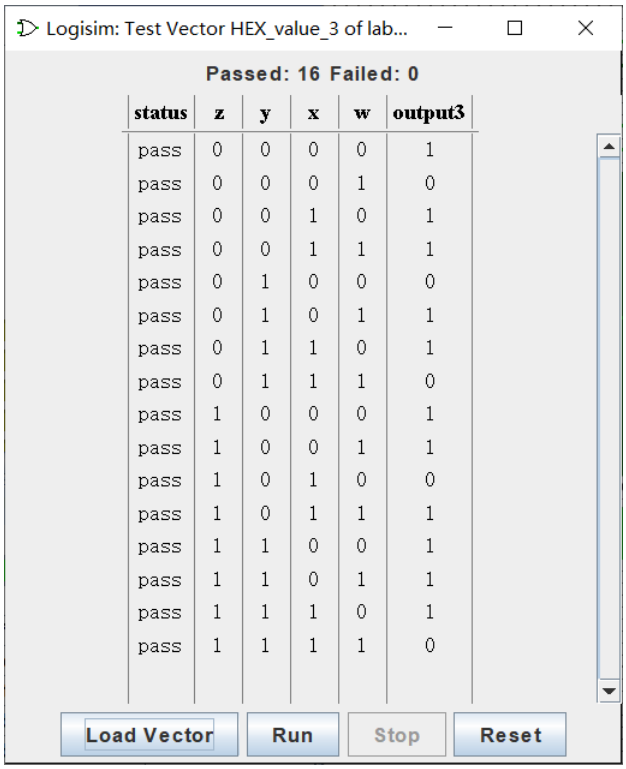
Load Vector | Run | Stop | Reset


Logisim: Test Vector HEX_value_2 of lab...

Passed: 16 Failed: 0

status	z	y	x	w	output2
pass	0	0	0	0	1
pass	0	0	0	1	1
pass	0	0	1	0	0
pass	0	0	1	1	1
pass	0	1	0	0	1
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	1
pass	1	1	0	0	0
pass	1	1	0	1	1
pass	1	1	1	0	0
pass	1	1	1	1	0

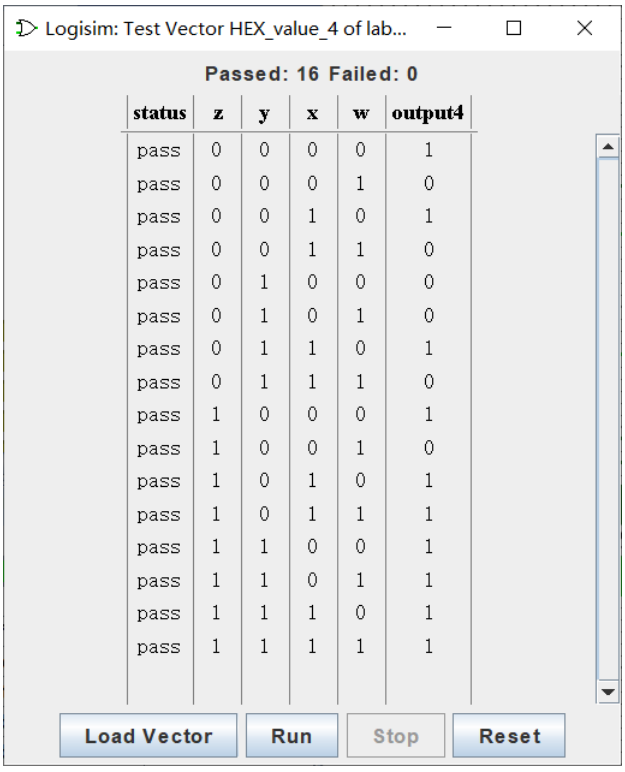
Load Vector | Run | Stop | Reset

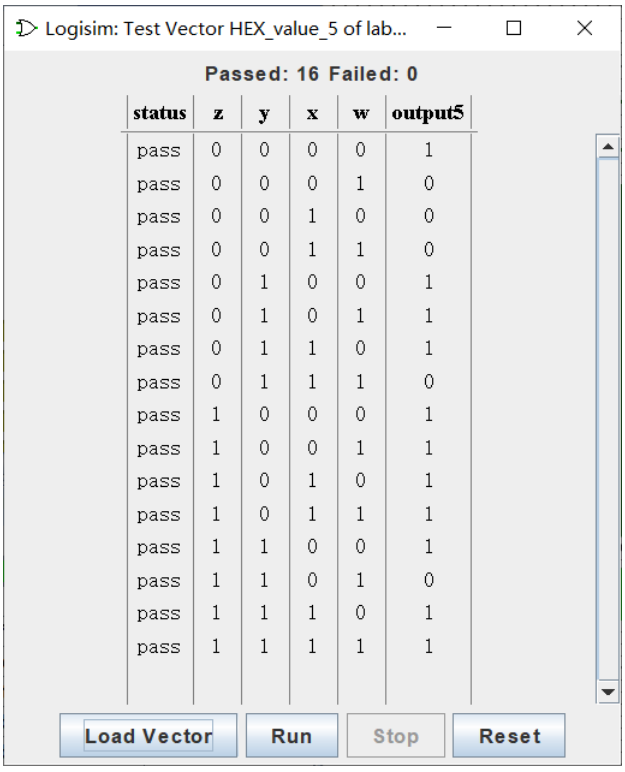

Logisim: Test Vector HEX_value_3 of lab...

Passed: 16 Failed: 0

status	z	y	x	w	output3
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	0
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	0
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	0
pass	1	0	1	1	1
pass	1	1	0	0	1
pass	1	1	0	1	1
pass	1	1	1	0	1
pass	1	1	1	1	0

Load Vector | Run | Stop | Reset


Logisim: Test Vector HEX_value_4 of lab...
Passed: 16 Failed: 0
status z y x w output4
pass 0 0 0 0 1
pass 0 0 0 1 0
pass 0 0 1 0 1
pass 0 0 1 1 0
pass 0 1 0 0 0
pass 0 1 0 1 0
pass 0 1 1 0 1
pass 0 1 1 1 0
pass 1 0 0 0 1
pass 1 0 0 1 0
pass 1 0 1 0 1
pass 1 0 1 1 1
pass 1 1 0 0 1
pass 1 1 0 1 1
pass 1 1 1 0 1
pass 1 1 1 1 1
Load Vector
Run
Stop
Reset


Logisim: Test Vector HEX_value_5 of lab...
Passed: 16 Failed: 0
status z y x w output5
pass 0 0 0 0 1
pass 0 0 0 1 0
pass 0 0 1 0 0
pass 0 0 1 1 0
pass 0 1 0 0 1
pass 0 1 0 1 1
pass 0 1 1 0 1
pass 0 1 1 1 0
pass 1 0 0 0 1
pass 1 0 0 1 1
pass 1 0 1 0 1
pass 1 0 1 1 1
pass 1 1 0 0 1
pass 1 1 0 1 0
pass 1 1 1 0 1
pass 1 1 1 1 1
Load Vector
Run
Stop
Reset