Lab 7 Memory and RGB Video

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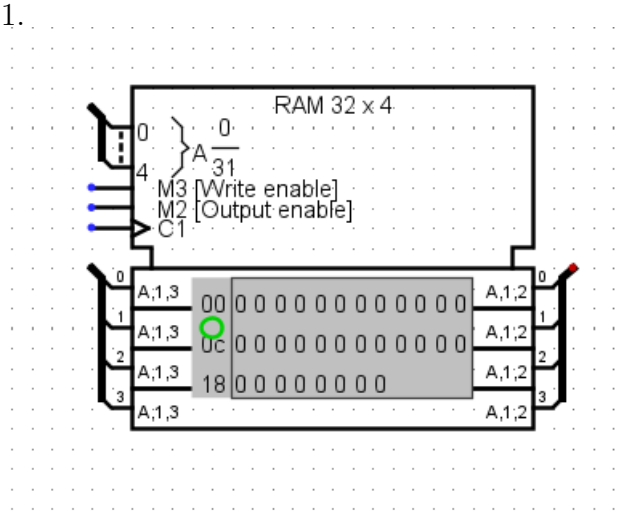
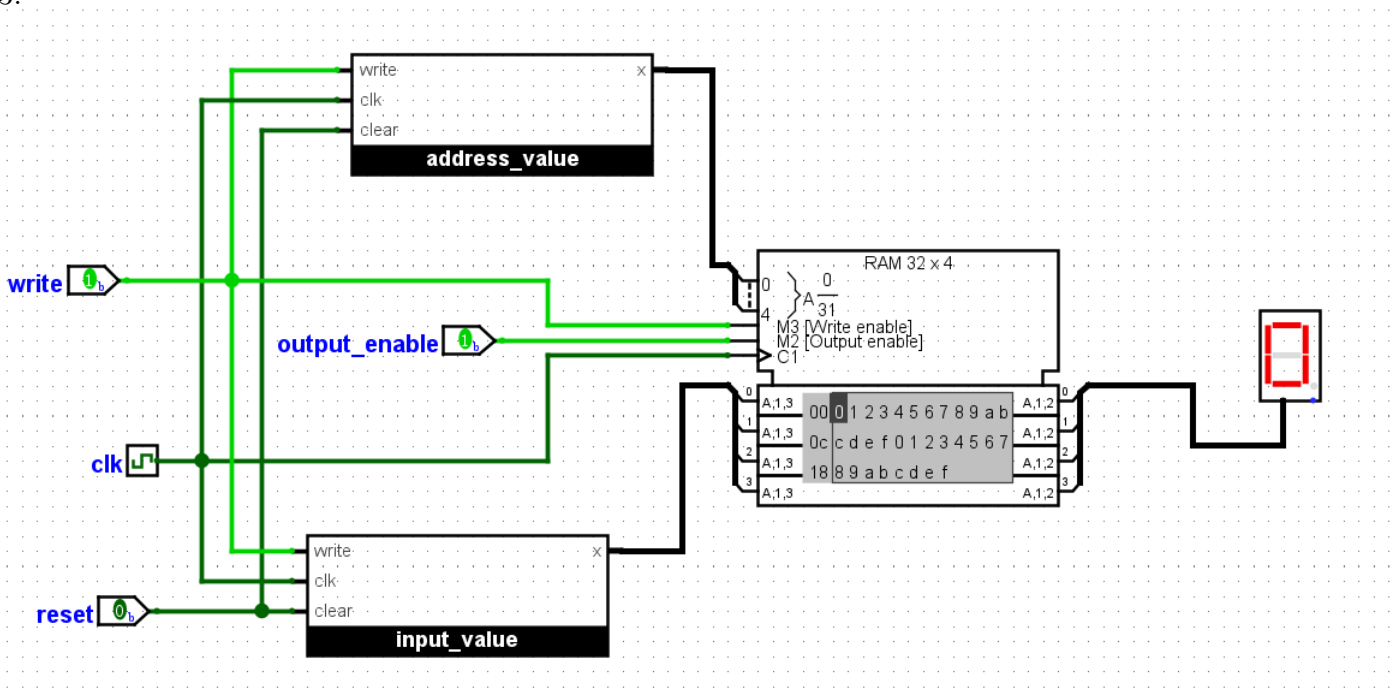
Part I

1.

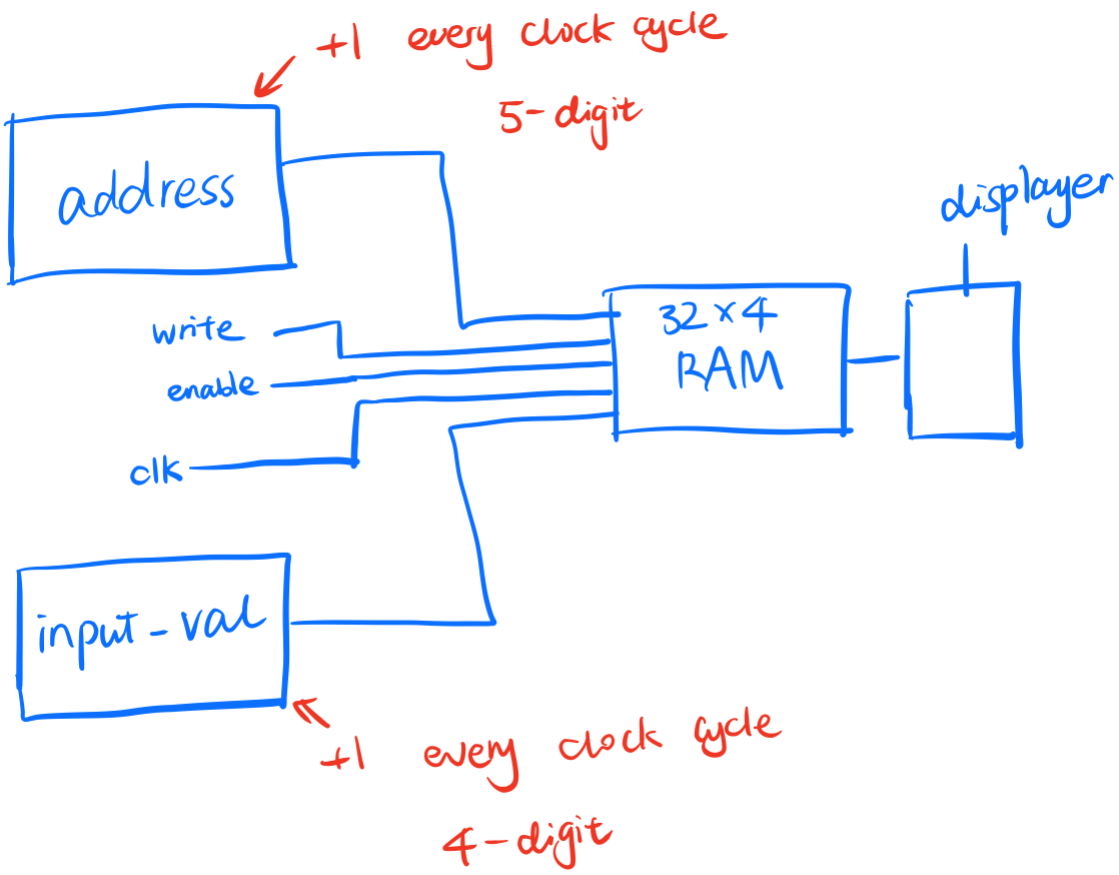


2. If they are both off, nothing happens; if they are both on, the RAM writes then reads the value to the output, so output value will equal input value.

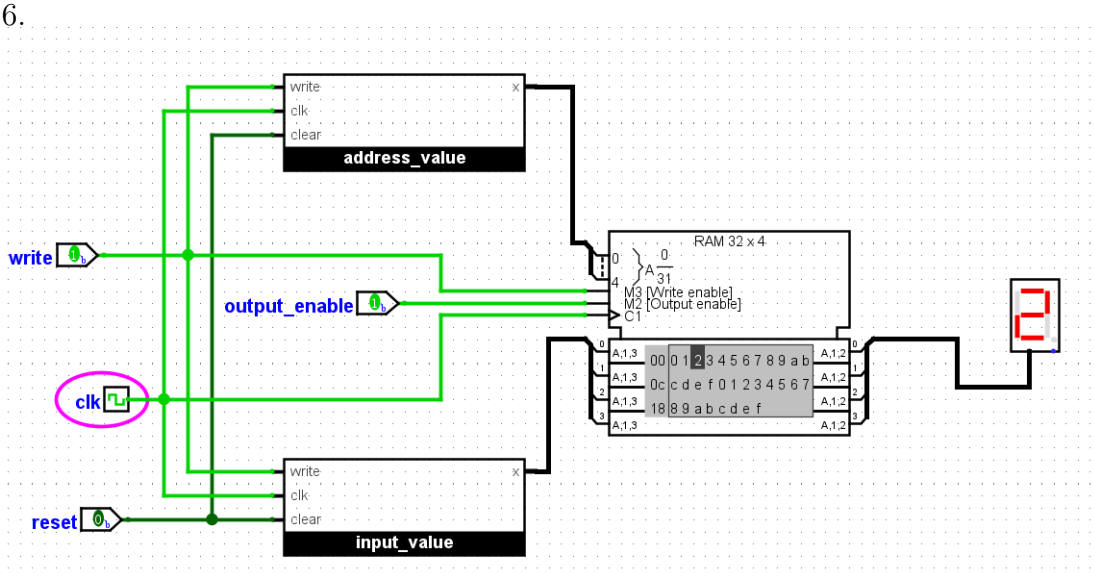
3.

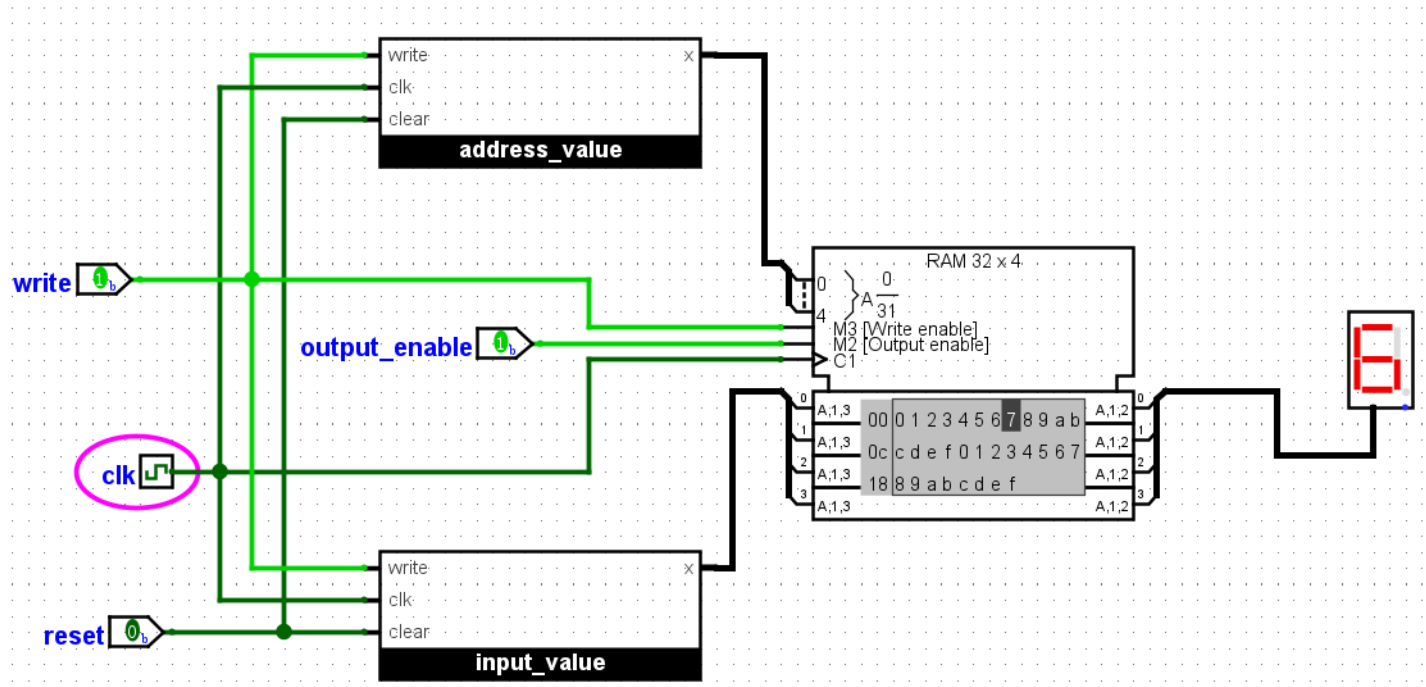


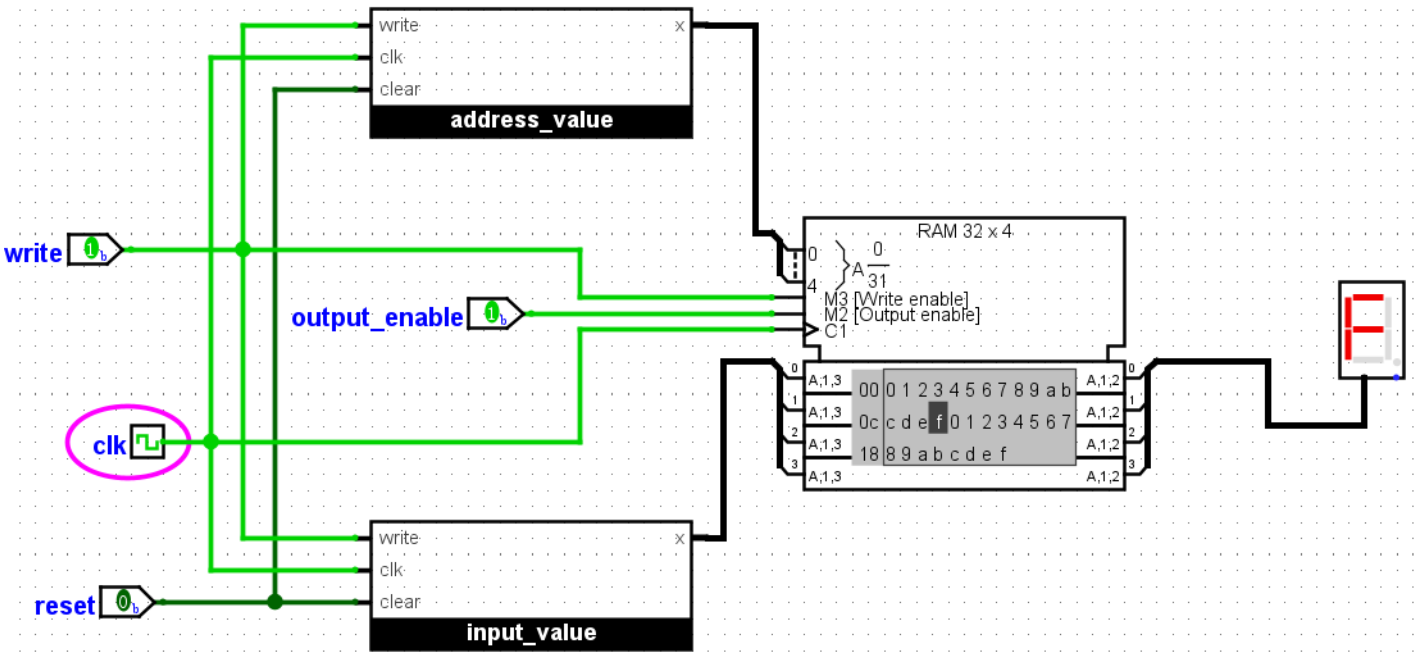
5.

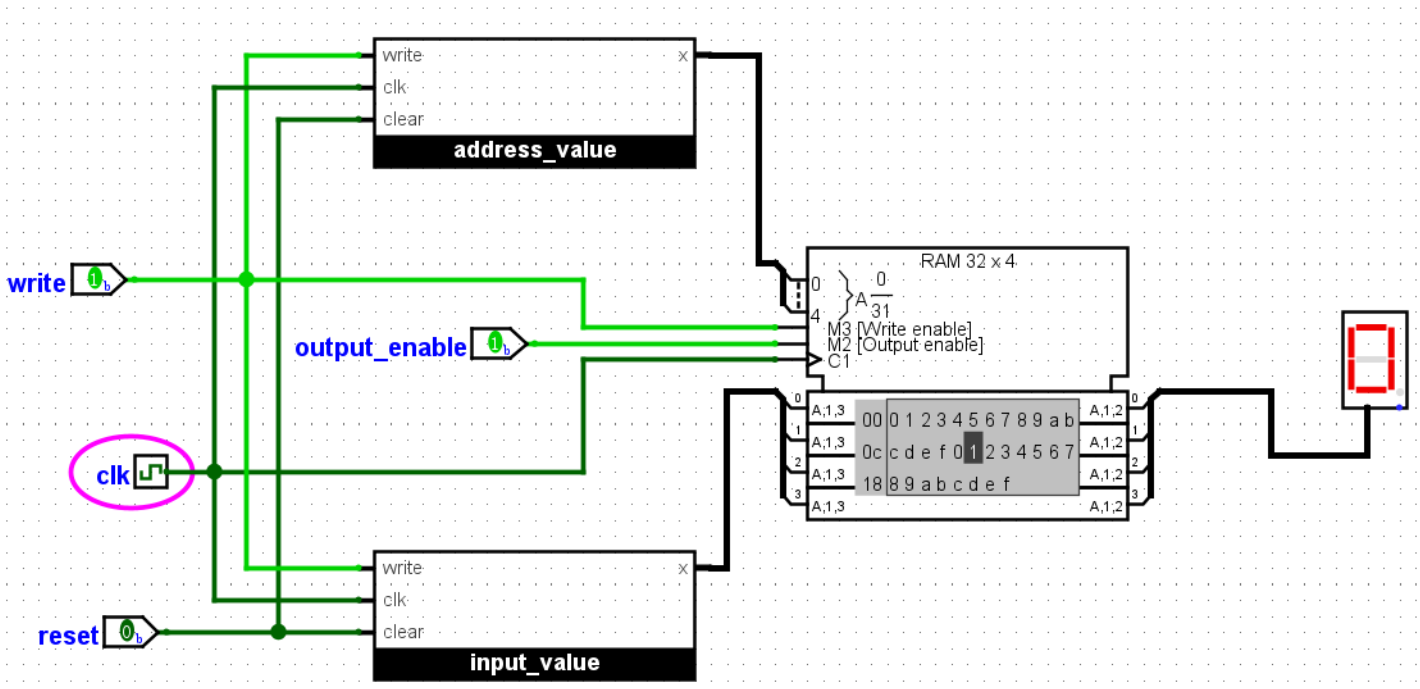

+1 every clock cycle
5-digit
address
displayer
write
enable
clk
32x4
RAM
input-val
+1 every clock cycle
4-digit

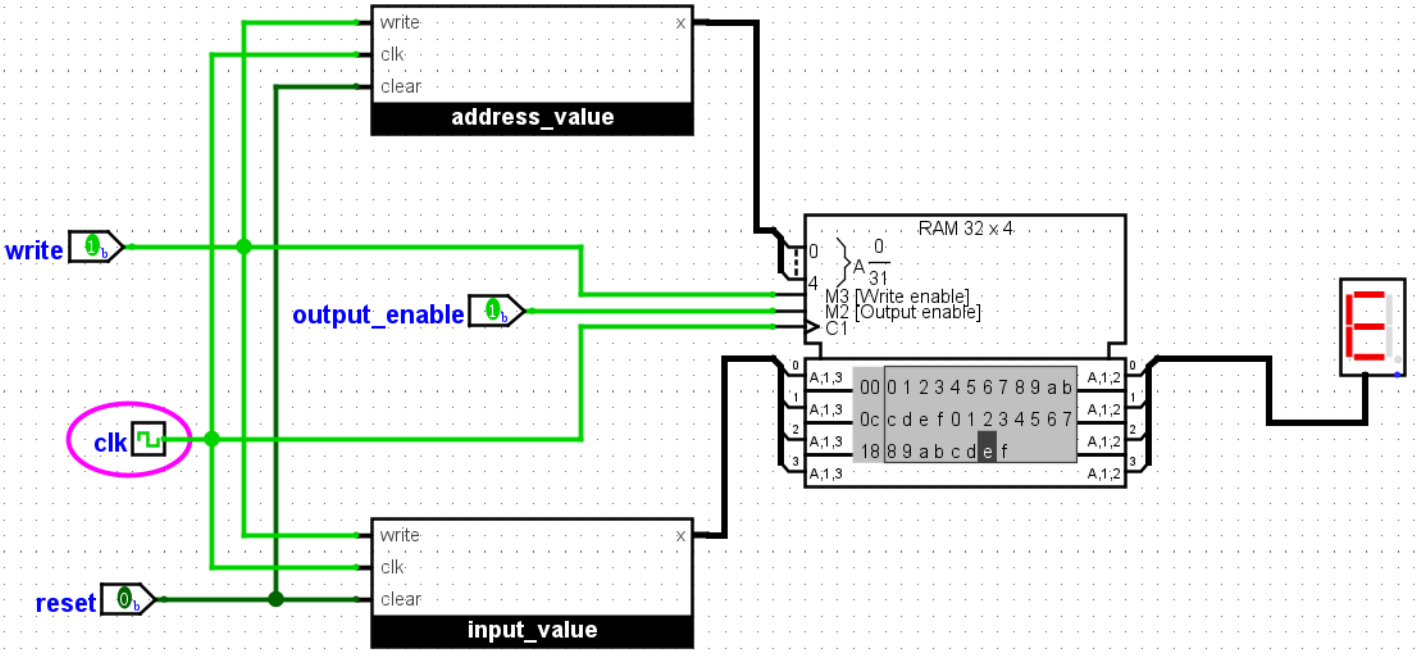
6.


write
clk
clear
address_value
write
output_enable
clk
reset
RAM 32 x 4
M3 [Write enable]
M2 [Output enable]
C1
write
clk
clear
input_value


write
clk
clear
address_value
write
output_enable
clk
reset
write
clk
clear
input_value
RAM 32 x 4
M3 [Write enable]
M2 [Output enable]
C1
00 0 1 2 3 4 5 6 7 8 9 a b
0c c d e f 0 1 2 3 4 5 6 7
18 8 9 a b c d e f

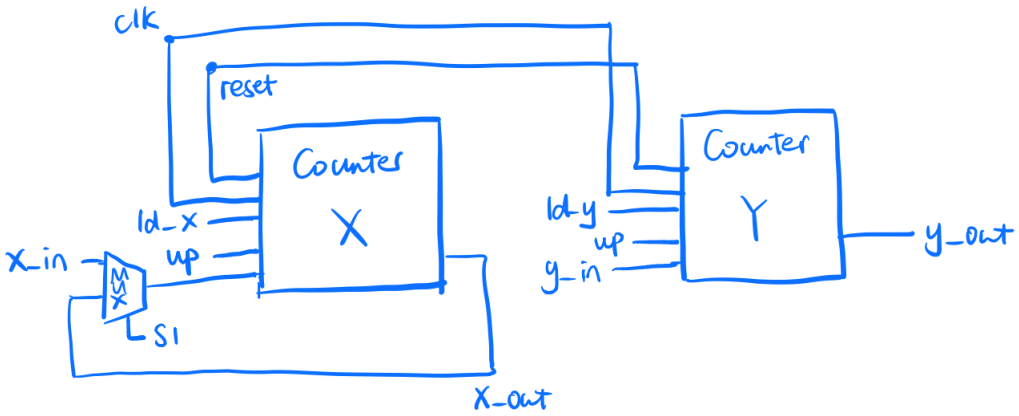

write
clk
clear
address_value
write
output_enable
clk
reset
write
clk
clear
input_value
RAM 32 x 4
M3 [Write enable]
M2 [Output enable]
C1
00 0 1 2 3 4 5 6 7 8 9 a b
0c c d e f 0 1 2 3 4 5 6 7
18 8 9 a b c d e f


write
clk
clear
address_value
write
output_enable
clk
reset
RAM 32 x 4
M3 [Write enable]
M2 [Output enable]
C1
write
clk
clear
input_value

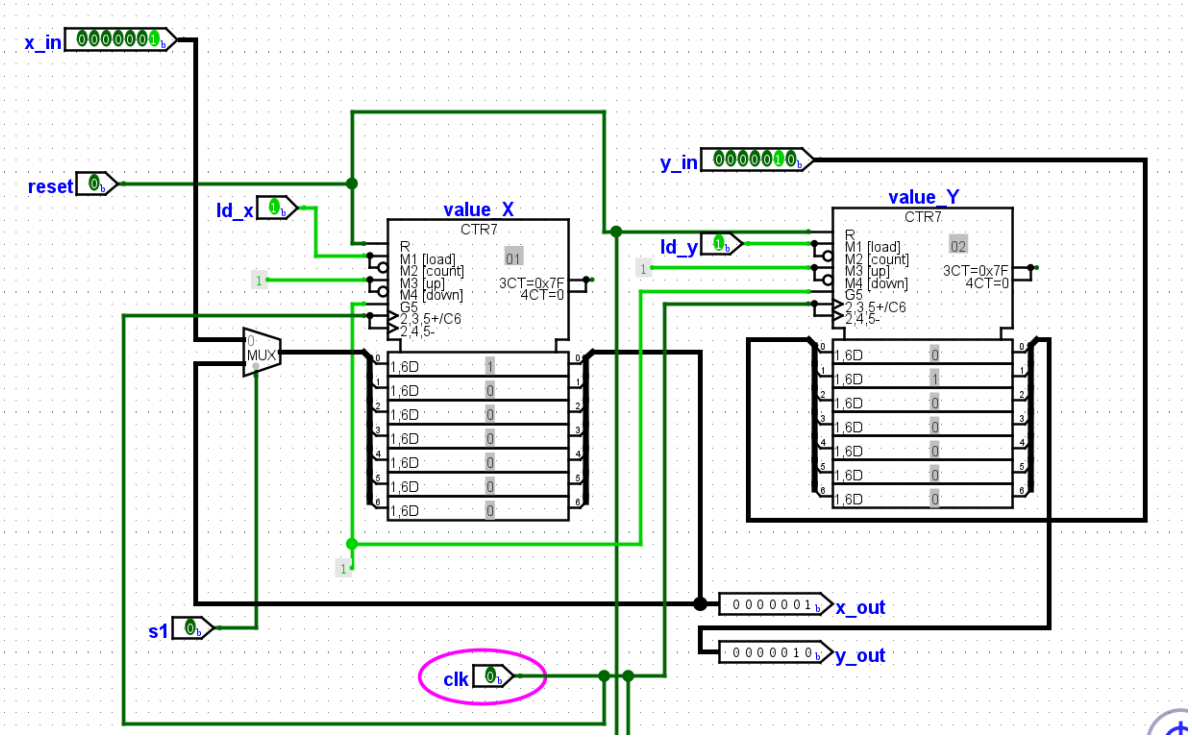

write
clk
clear
address_value
write
output_enable
clk
reset
RAM 32 x 4
M3 [Write enable]
M2 [Output enable]
C1
write
clk
clear
input_value

Part II

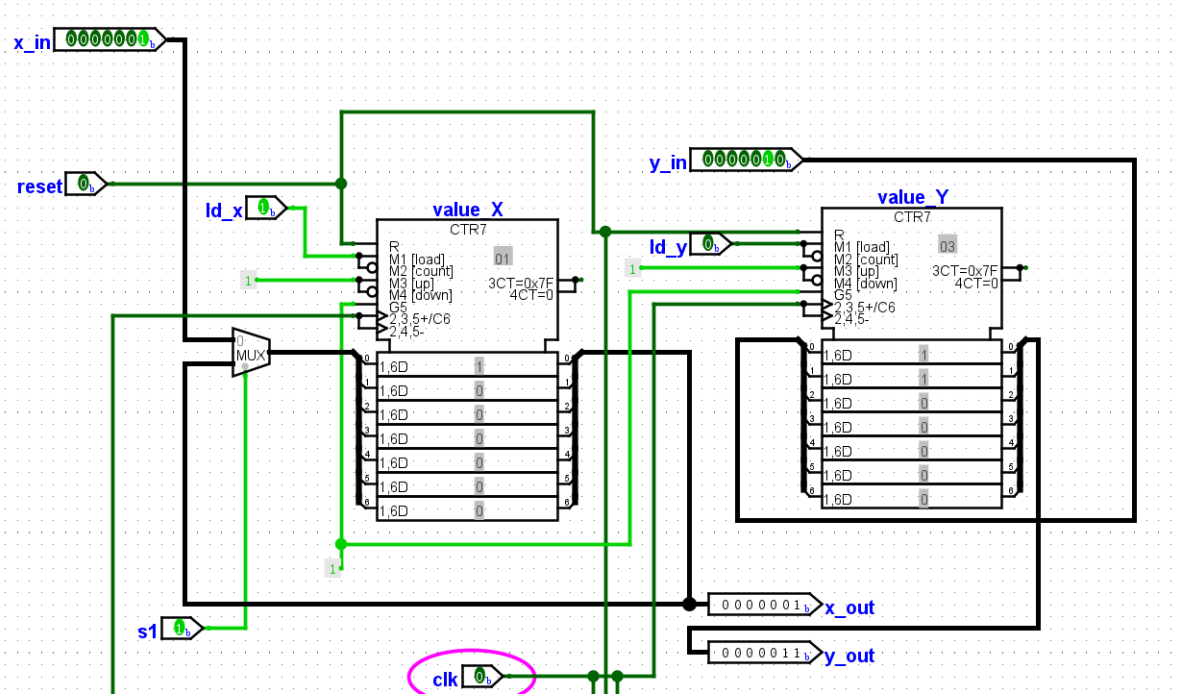
1.



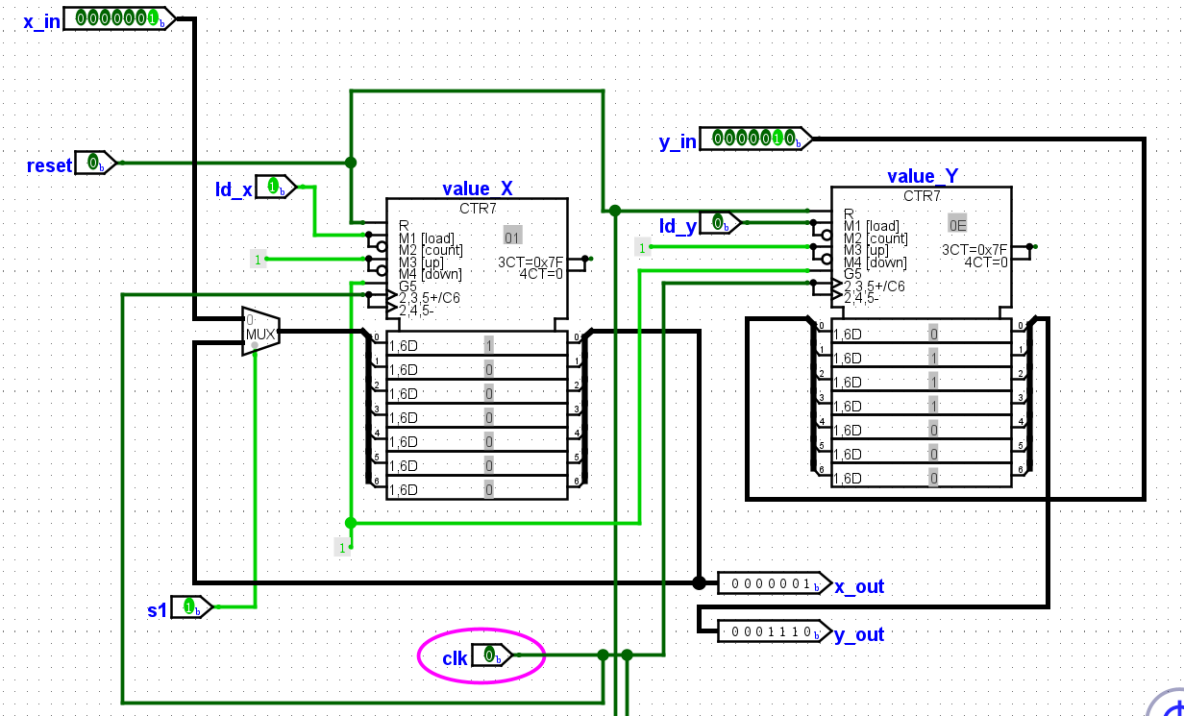
Load x and y, output (x, y).



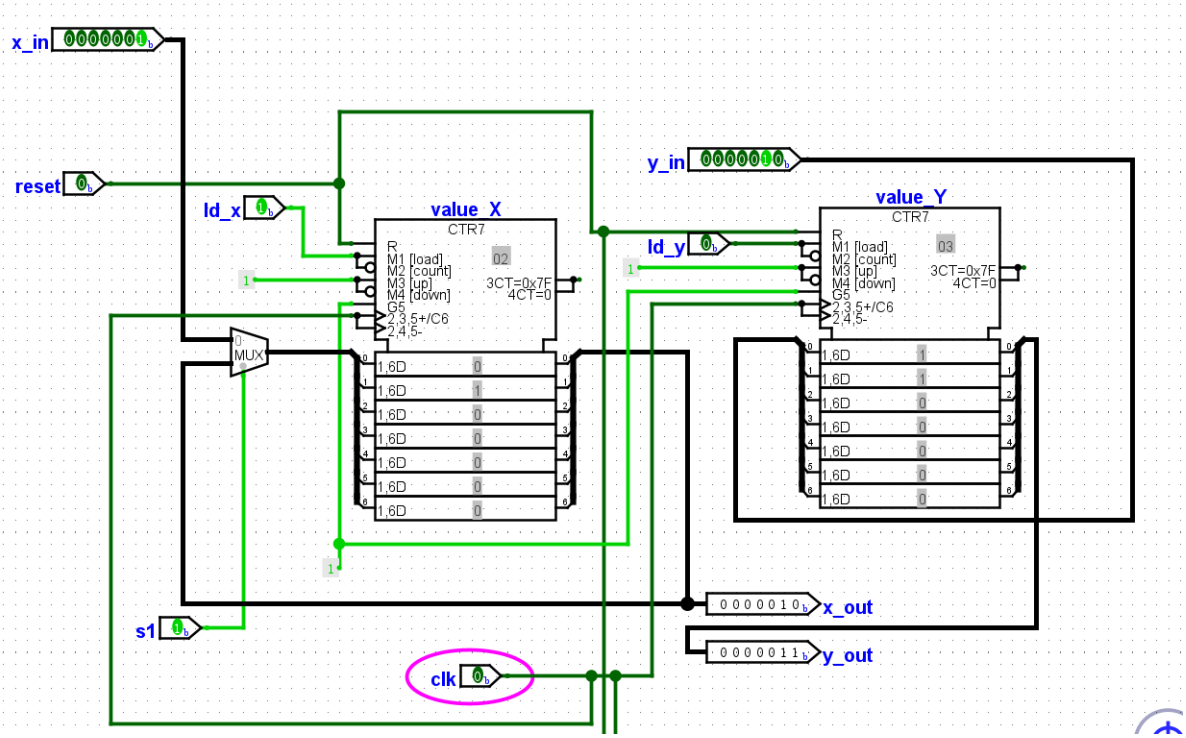
Output $(x, y+1)$.



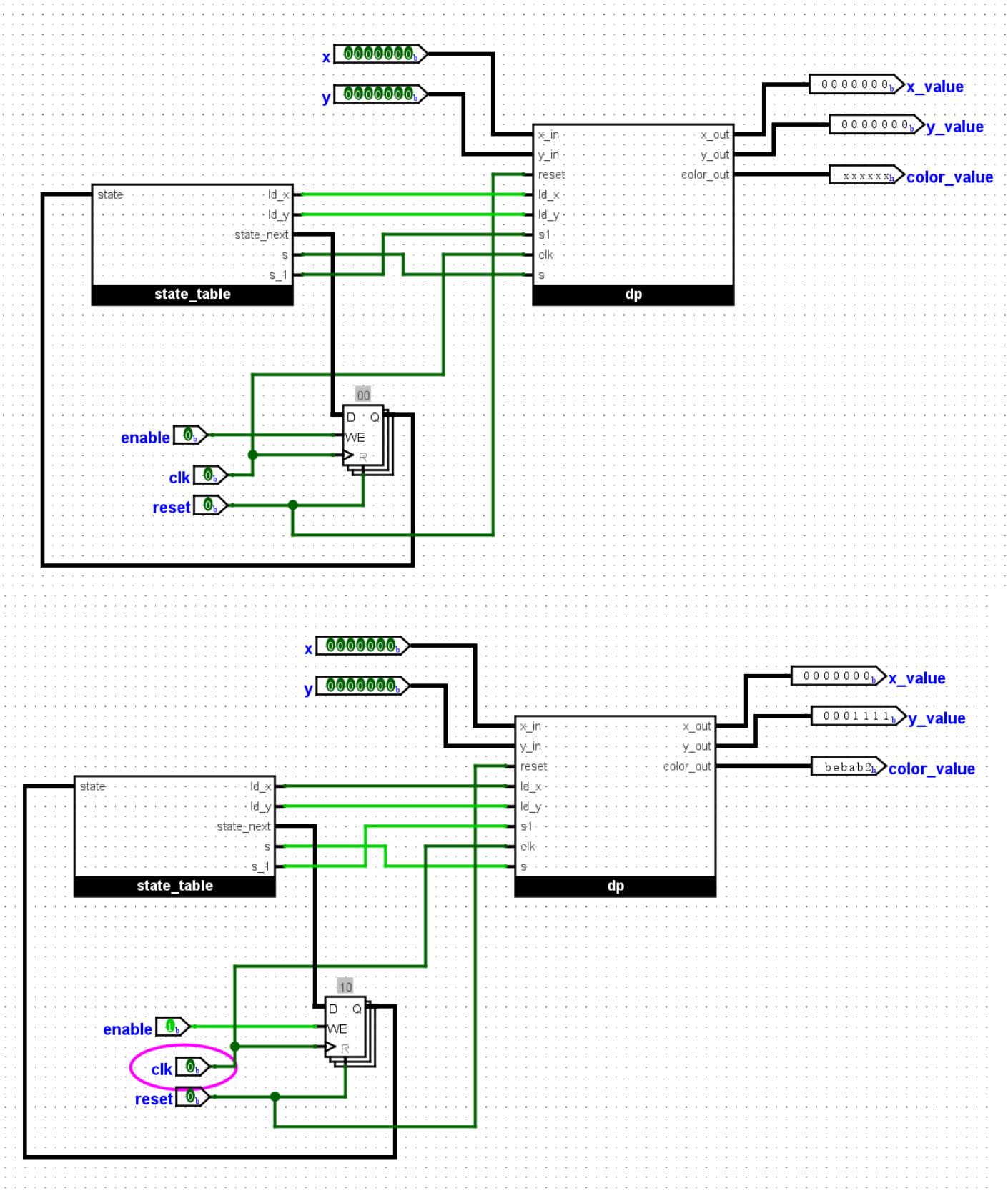
Output $(x, y+15)$.

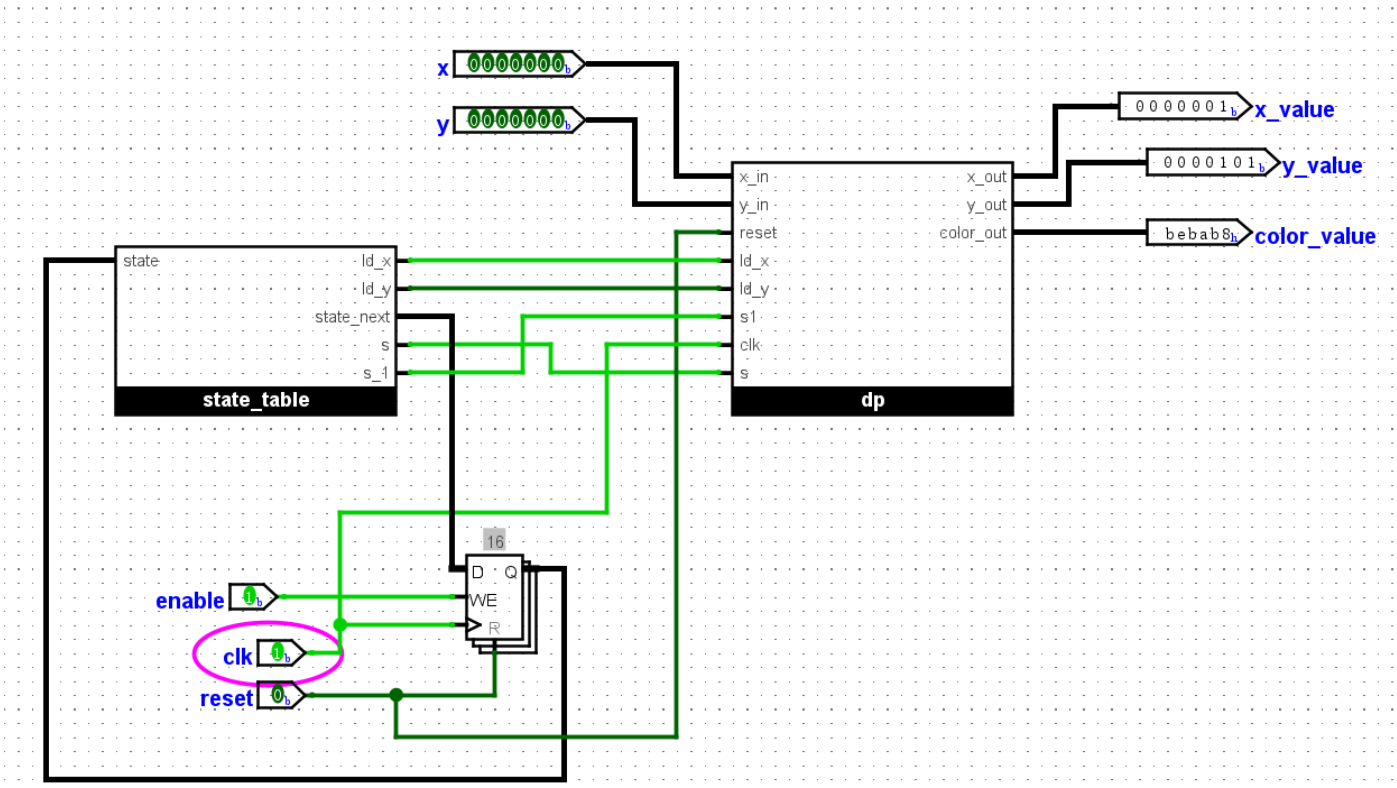


Output $(x+1, y+1)$.

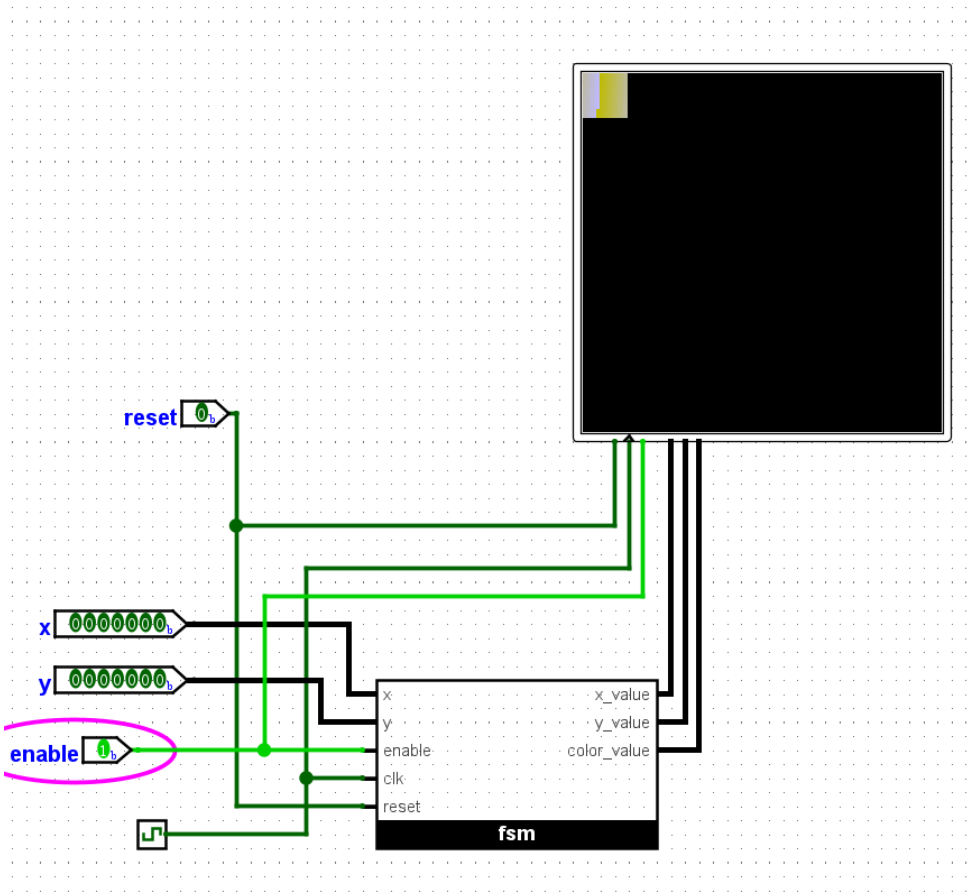

x_in
reset
ld_x
value_X
CTR7
R
M1 [load]
M2 [count]
M3 [up]
M4 [down]
G5
2,3,5+/C6
2,4,5-
02
3CT=0x7F
4CT=0
MUX
s1
clk
y_in
ld_y
value_Y
03
x_out
y_out

2.


x
y
x_in
y_in
reset
ld_x
ld_y
s1
clk
s
x_out
y_out
color_out
x_value
y_value
color_value
state
ld_x
ld_y
state_next
s
s_1
state_table
dp
00
D
Q
WE
R
enable
clk
reset
10


x
y
x_in
y_in
reset
ld_x
ld_y
s1
clk
s
x_out
y_out
color_out
dp
state
ld_x
ld_y
state_next
s
s_1
state_table
16
D
Q
WE
R
enable
clk
reset
x_value
y_value
color_value

3.


reset
x
y
enable
x
y
enable
clk
reset
x_value
y_value
color_value
fsm