

# Latches, Flip-flops, and Registers

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# Part I

1. Diagram of gated D latch:

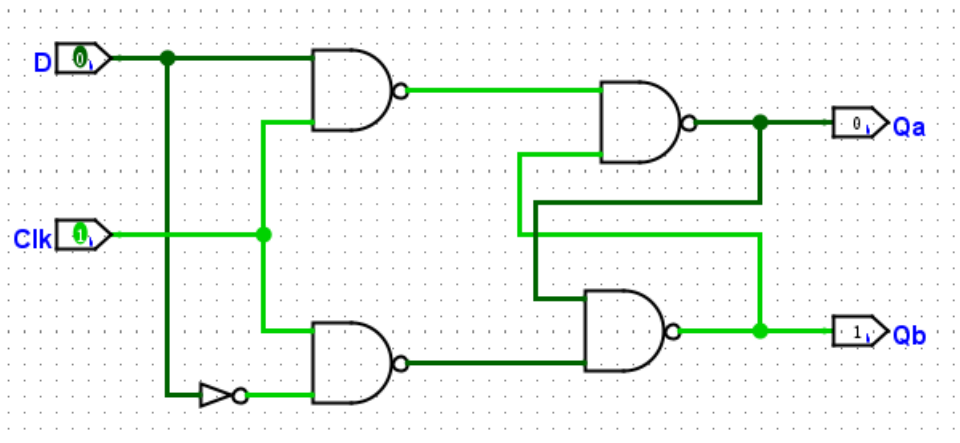
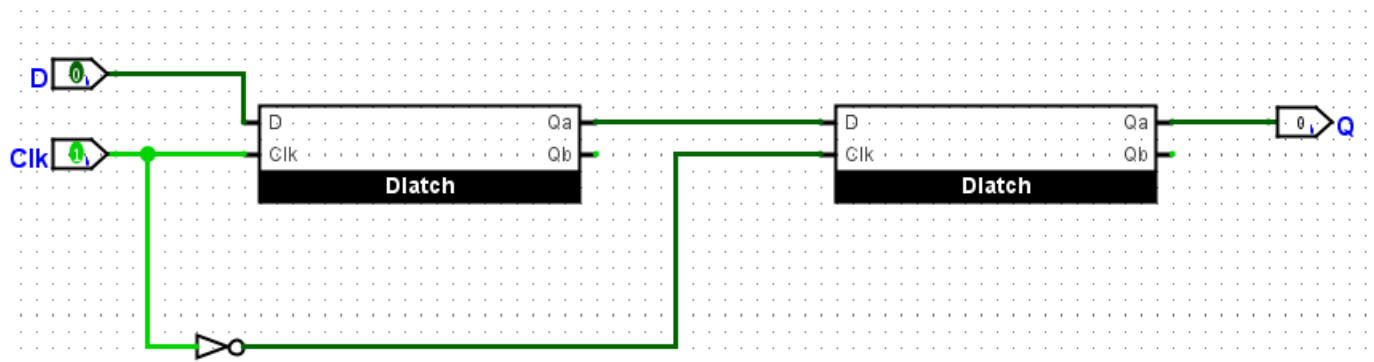


Diagram of a master slave flip-flop:



- 2.
3. For the D latch, any input combination with Clk being 0 should not be tested first. When Clk has value 0, the outputs holds the previous values. But it does not have a previous value when connected the first time. So 10 and 00 should not be tested first in the D latch.  
For the flip flop, when Clk has value 1, the behavior changes in the first D latch, but the second D latch received value 0 as the clock, so it holds the previous value, which is not yet existed. So any combination of inputs with Clk being 1 should not be tested first. Namely 01 and 11 should not be tested first.

## Part II

2. a) Without a register, oscillation apparent error will appear when calculation involves value of B. This is because without a register, the ALU calculates whenever there is a new input, and since value of B is obtained from ALU itself, it continuously gets a new value and keeps calculating.

b)  $2n$  bits are needed

3. a)

A[4]	s[3]	B[4]	Clk	x[8]
0101	000	0110	1	00000110
0101	000	0110	0	00000110
1111	001	0110	0	00000110
1111	001	0101	1	00010101
1001	010	0101	1	00010101
1101	010	0101	0	00010101
1101	010	0010	1	00010010
1011	011	0010	0	00010101
1010	011	1000	1	10101000
1010	100	1000	0	10101000
1010	100	0001	1	00000001
1010	101	0001	0	00000001
1010	101	0100	1	00000100
1001	110	0100	0	00000100
1001	110	0010	1	00000010
1001	111	0010	0	00000010
1101	111	1010	1	00011010
1101	111	1010	0	00011010
1111	111	0110	1	10010110

b) test vector for function 5

Logisim: Test Vector function5 of lab4\_part2

Passed: 9 Failed: 0

status	A	B	w
pass	0000	0110	0000 0110
pass	0001	0110	0000 1100
pass	0011	0011	0001 1000
pass	0101	1111	1110 0000
pass	0110	1111	1100 0000
pass	0111	1111	1000 0000
pass	1111	1111	1000 0000
pass	1000	0111	0000 0111
pass	1001	0111	0000 1110

Load Vector Run Stop Reset Close Window

test vector for function 6

Logisim: Test Vector function6 of lab4\_part2

Passed: 9 Failed: 0

status	A	B	w
pass	0000	1111	0000 1111
pass	0001	1111	0000 0111
pass	0011	1111	0000 0001
pass	1011	1000	0000 0001
pass	0100	1111	0000 0000
pass	1010	1001	0000 0010
pass	0010	1100	0000 0011
pass	0111	1111	0000 0000
pass	0101	1100	0000 0000

Load Vector Run Stop Reset Close Window

test vector for function 7

Logisim: Test Vector function7 of lab4\_part2

Passed: 8 Failed: 0

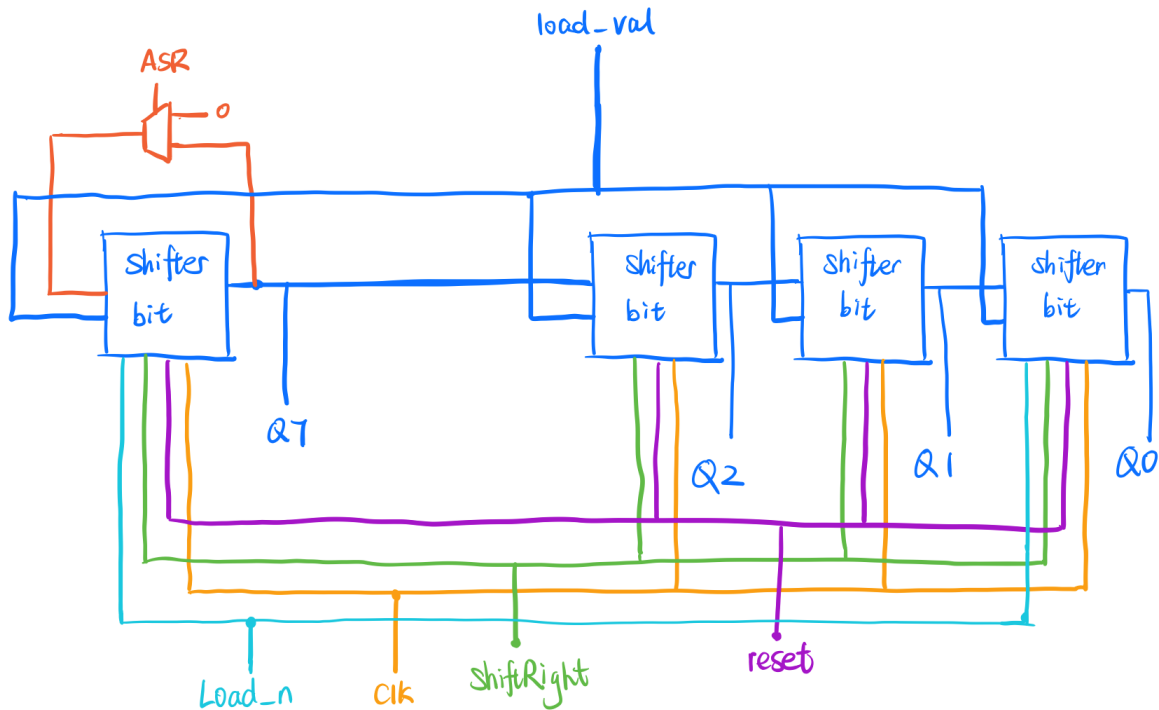
status	A	B	w
pass	0000	0000	0000 0000
pass	1111	1111	1110 0001
pass	1101	1001	0111 0101
pass	0101	1010	0011 0010
pass	0001	1101	0000 1101
pass	0110	1100	0100 1000
pass	0010	0111	0000 1110
pass	1110	0111	0110 0010

Load Vector Run Stop Reset Close Window

## Part III

1. The output remains the same regardless of what you do to other inputs. When  $load_n = 1$  and  $rightShift = 0$ , the second mux chooses the second input, and the first mux choose the first input inside the shifter bit. So whatever is in the output get passed to the output, making the output remains the same.

2.



5.

