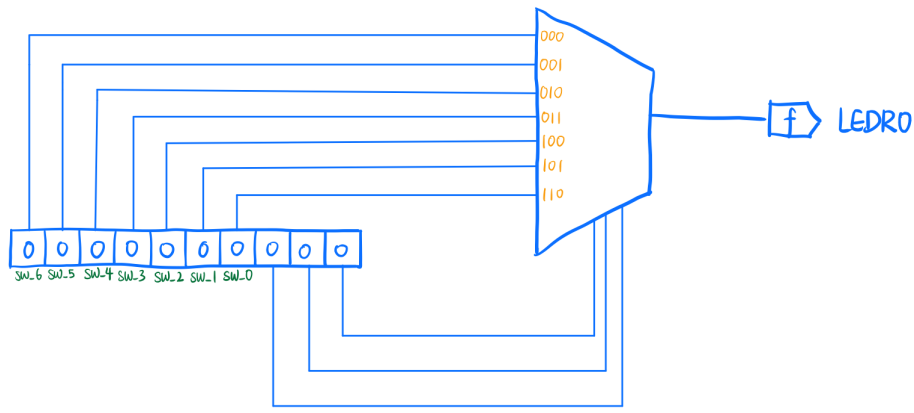


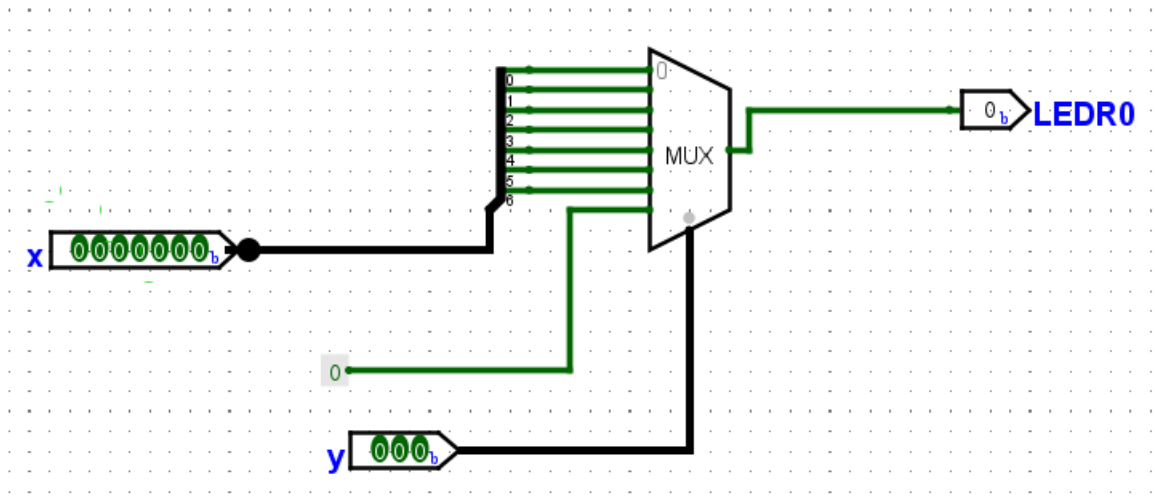
Part I

1.



b) The input needs to be 10 bits large in order to provide all inputs for a 7to1 multiplexer.

2.



3.

Logisim: Test Vector main of lab3_part1

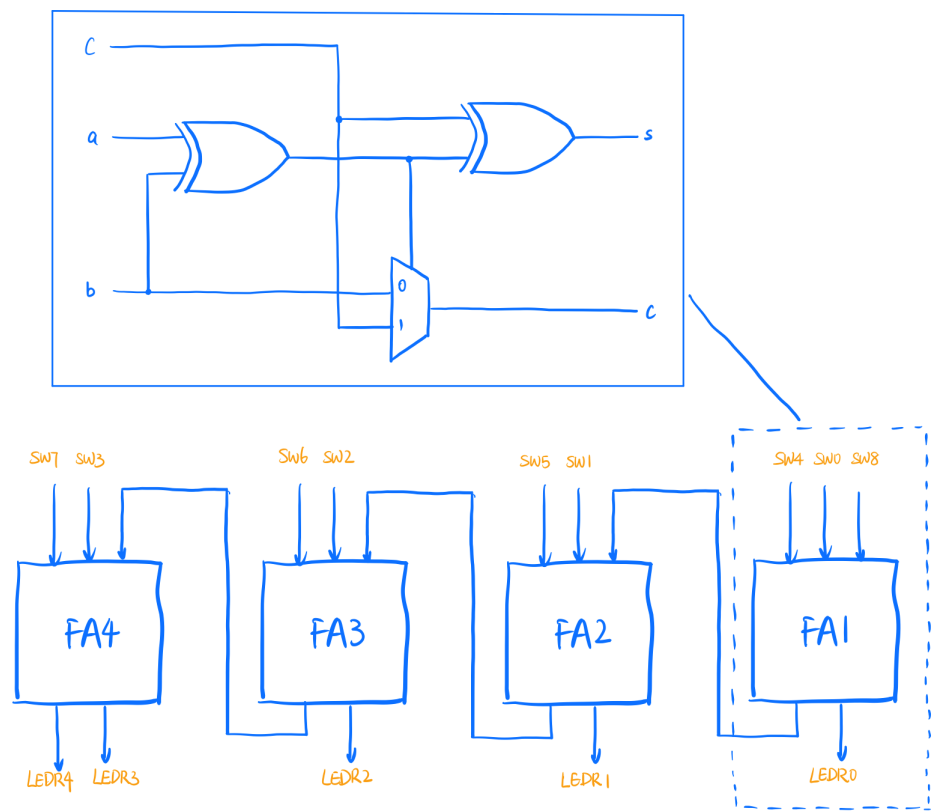
Passed: 16 Failed: 0

status	x	y	LED0
pass	000 0000	000	0
pass	000 0001	000	1
pass	000 0001	001	0
pass	000 0010	001	1
pass	111 1011	010	0
pass	000 0100	010	1
pass	110 0000	011	0
pass	000 1000	011	1
pass	110 1000	100	0
pass	001 0000	100	1
pass	100 1000	101	0
pass	010 0000	101	1
pass	100 1000	101	0
pass	011 0000	101	1
pass	010 1011	110	0
pass	101 0110	110	1

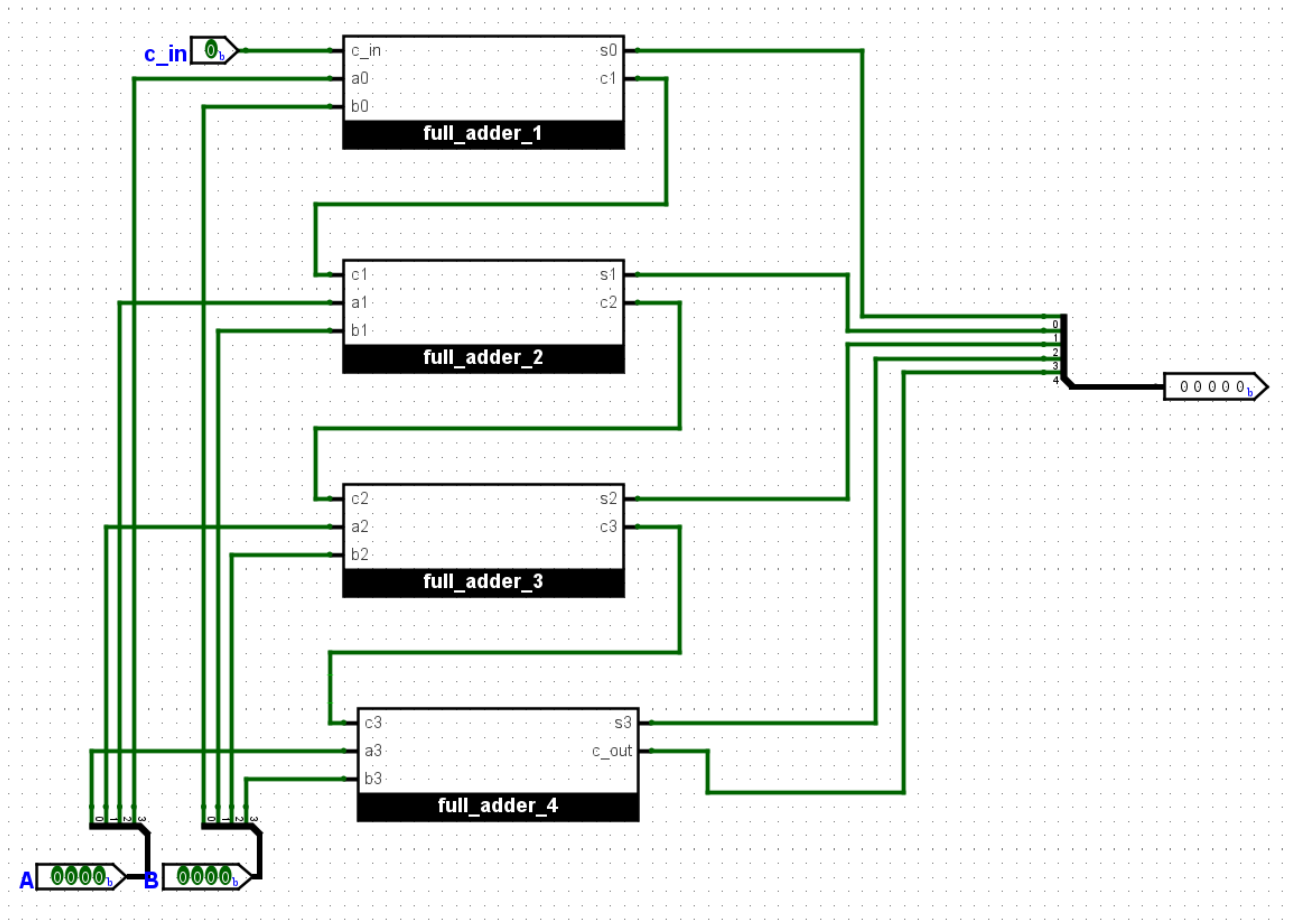
Load Vector Run Stop Reset

Part II

1.



2.



3.

Logisim: Test Vector main of lab3_part2

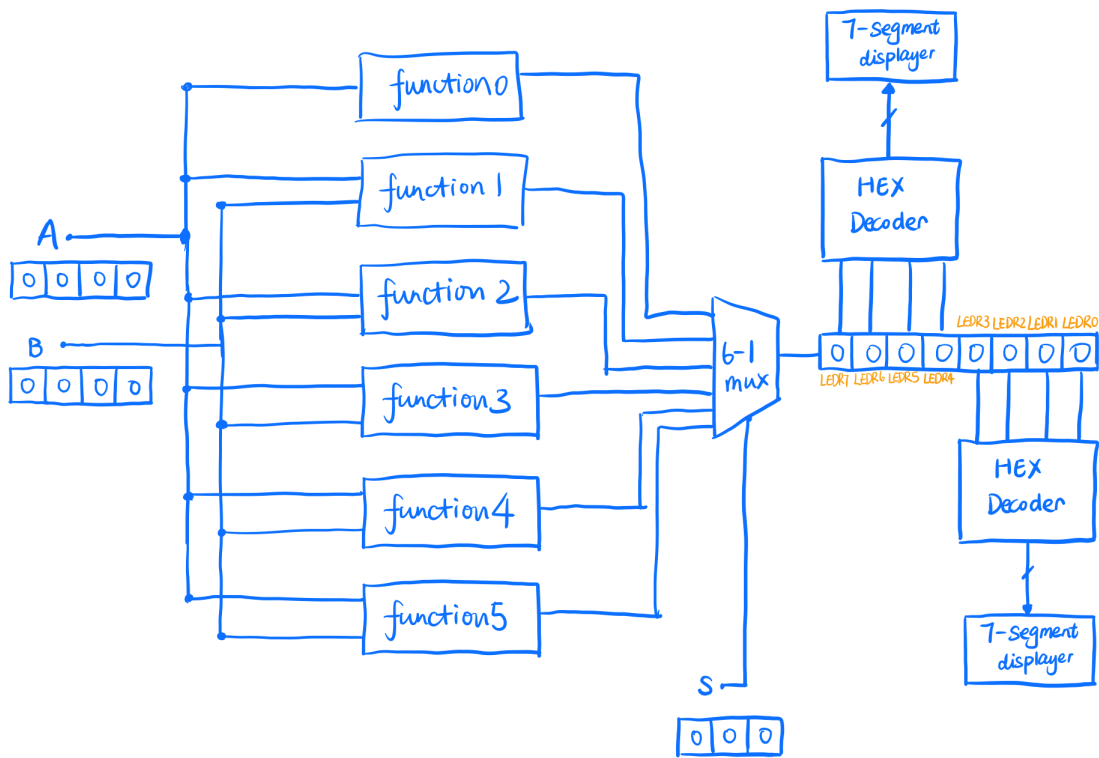
Passed: 16 Failed: 0

status	A	B	c_in	s
pass	0000	0000	0	0 0000
pass	1111	1111	1	1 1111
pass	1111	0000	0	0 1111
pass	0000	1111	1	1 0000
pass	0001	0010	0	0 0011
pass	0101	1010	0	0 1111
pass	0001	0010	1	0 0100
pass	0101	1010	1	1 0000
pass	0011	1001	0	0 1100
pass	0001	0001	0	0 0010
pass	0010	0010	0	0 0100
pass	0100	0100	0	0 1000
pass	1000	1000	0	1 0000
pass	0110	0110	0	0 1100
pass	0111	0111	0	0 1110
pass	1001	1001	0	1 0010

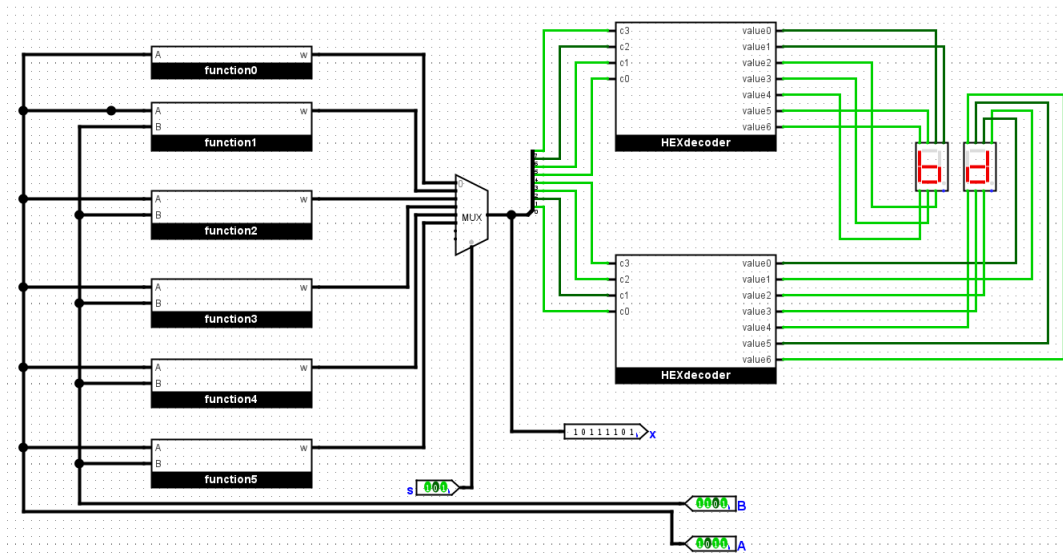
Load Vector Run Stop Reset Close Window

Part III

1.



2.



3.

Logisim: Test Vector main of lab3_part3

Passed: 24 Failed: 0

status	A	B	s	x
pass	0000	0000	000	0000 0001
pass	0000	0110	000	0000 0001
pass	0101	0000	000	0000 0110
pass	1010	0000	000	0000 1011
pass	0110	1101	001	0001 0011
pass	0110	1101	010	0001 0011
pass	1111	1001	001	0001 1000
pass	1111	1001	010	0001 1000
pass	1001	0111	001	0001 0000
pass	1001	0111	010	0001 0000
pass	1010	1110	001	0001 1000
pass	1010	1110	010	0001 1000
pass	1111	0000	011	1111 1111
pass	0000	0000	011	0000 0000
pass	1111	1111	011	1111 0000
pass	1010	0111	011	1111 1101
pass	0000	0000	100	0000 0000
pass	0001	0000	100	0000 0001
pass	0000	0001	100	0000 0001
pass	0110	1011	100	0000 0001
pass	0101	1010	101	0101 1010
pass	1111	1100	101	1111 1100
pass	0001	1011	101	0001 1011
pass	1011	1101	101	1011 1101

Load Vector Run Stop Reset Close Window