Latches, Flip-flops, and Registers

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October 15, 2020

Part I

1. Diagram of gated D latch:

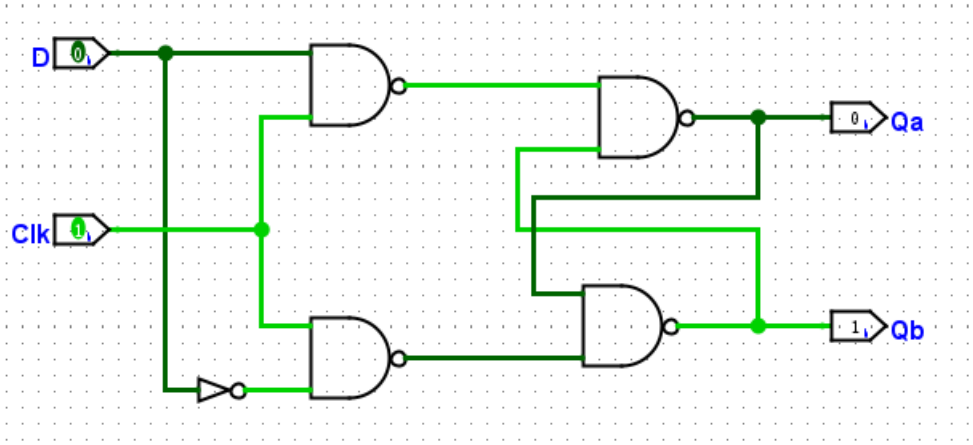
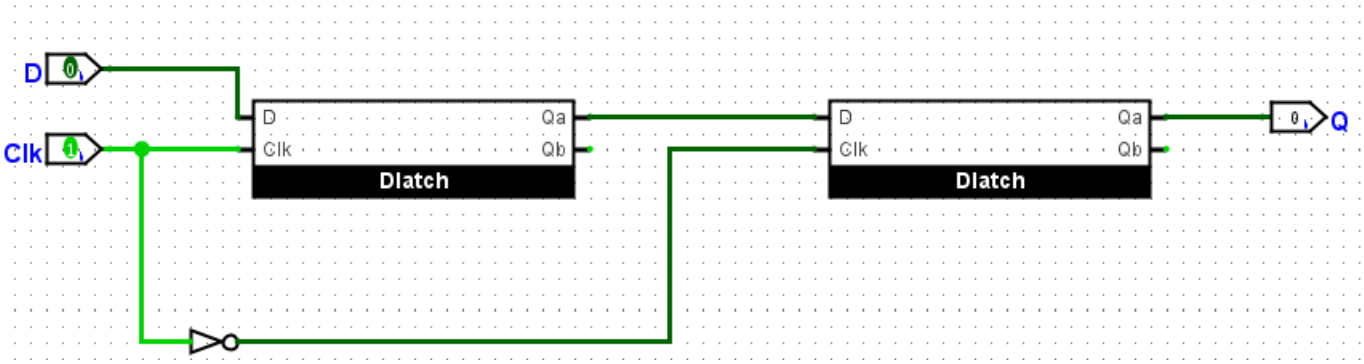


Diagram of a master slave flip-flop:



2.

3. For the D latch, any input combination with Clk being 0 should not be tested first. When Clk has value 0, the outputs holds the previous values. But it does not have a previous value when connected the first time. So 10 and 00 should not be tested first in the D latch.

   For the flip flop, when Clk has value 1, the behavior changes in the first D latch, but the second D latch received value 0 as the clock, so it holds the previous value, which is not yet existed. So any combination of inputs with Clk being 1 should not be tested first. Namely 01 and 11 should not be tested first.

Part II

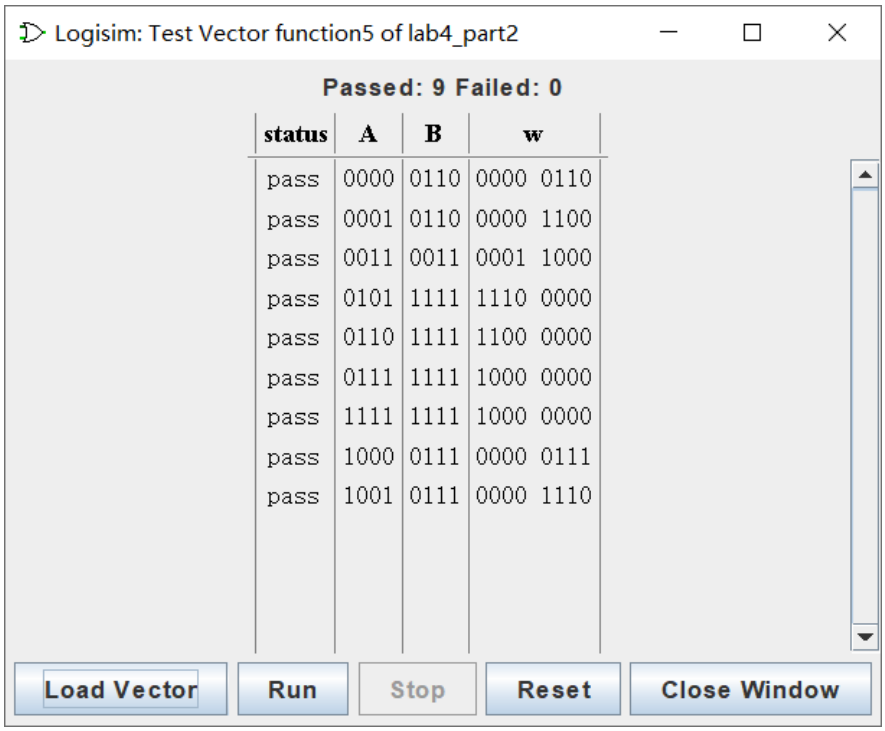
2. a) Without a register, oscillation apparent error will appear when calculation involves value of B. This is because without a register, the ALU calculates whenever there is a new input, and since value of B is obtained from ALU itself, it continuously gets a new value and keeps calculating.

b) $2n$ bits are needed

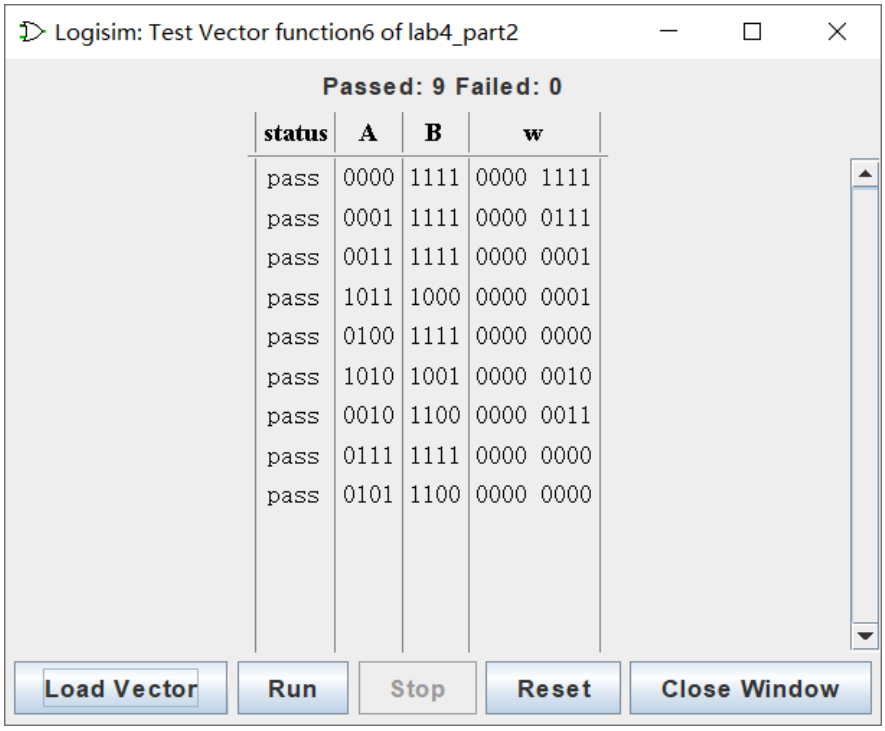
3. a)

A[4]	s[3]	B[4]	Clk	x[8]
0101	000	0110	1	00000110
0101	000	0110	0	00000110
1111	001	0110	0	00000110
1111	001	0101	1	00010101
1001	010	0101	1	00010101
1101	010	0101	0	00010101
1101	010	0010	1	00010010
1011	011	0010	0	00010101
1010	011	1000	1	10101000
1010	100	1000	0	10101000
1010	100	0001	1	00000001
1010	101	0001	0	00000001
1010	101	0100	1	00000100
1001	110	0100	0	00000100
1001	110	0010	1	00000010
1001	111	0010	0	00000010
1101	111	1010	1	00011010
1101	111	1010	0	00011010
1111	111	0110	1	10010110

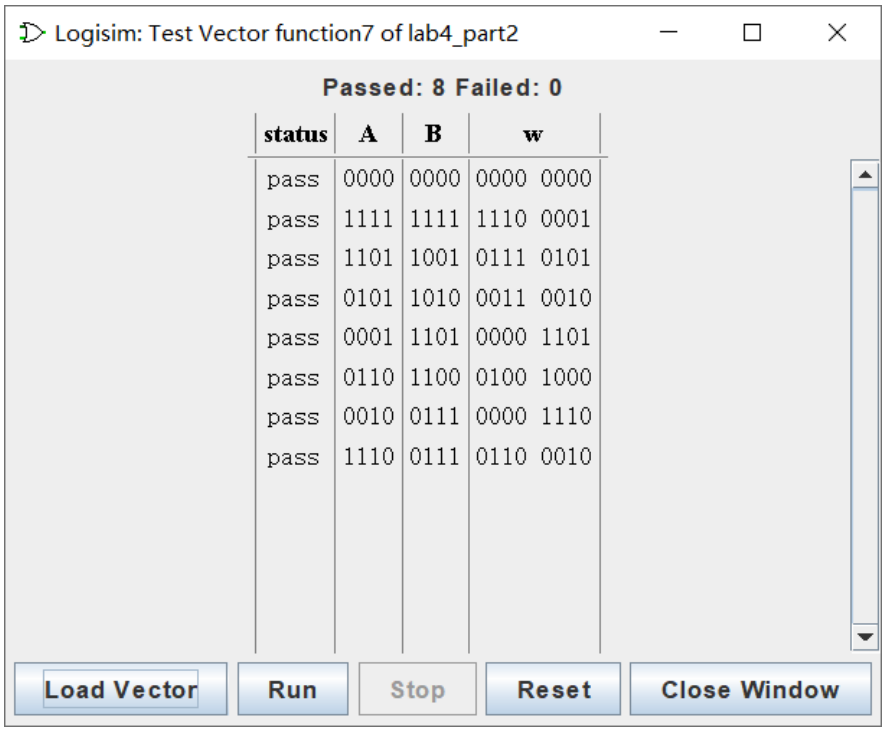
b) test vector for function 5



test vector for function 6



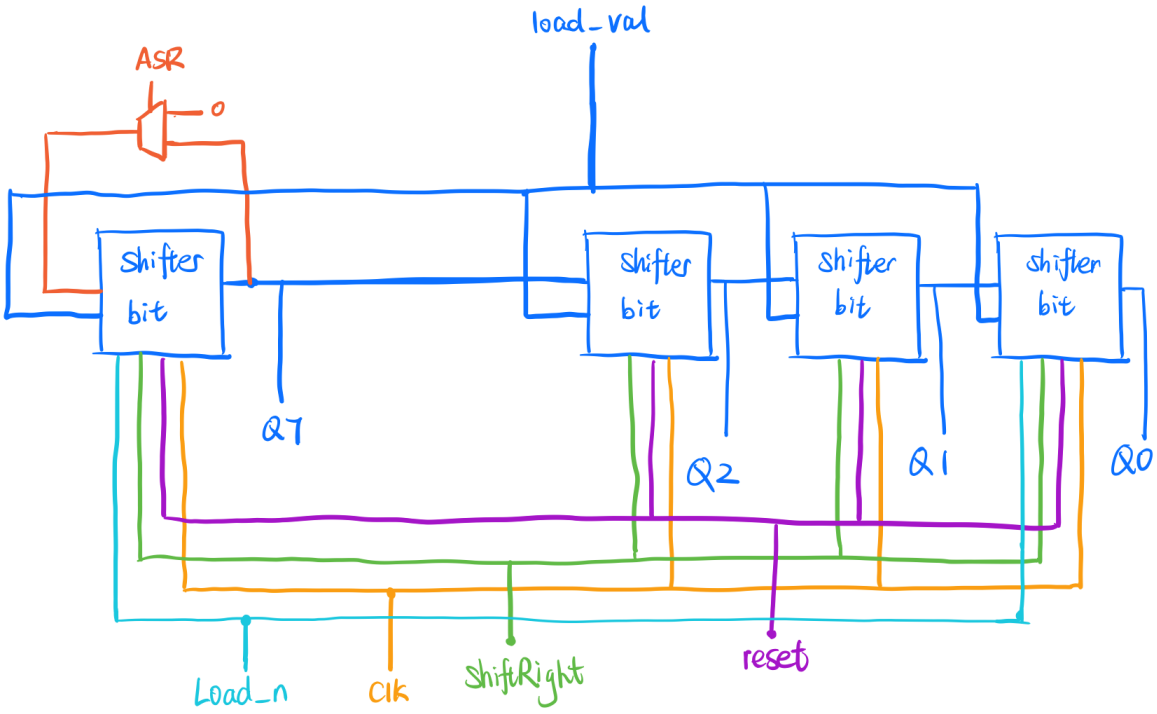
test vector for function 7



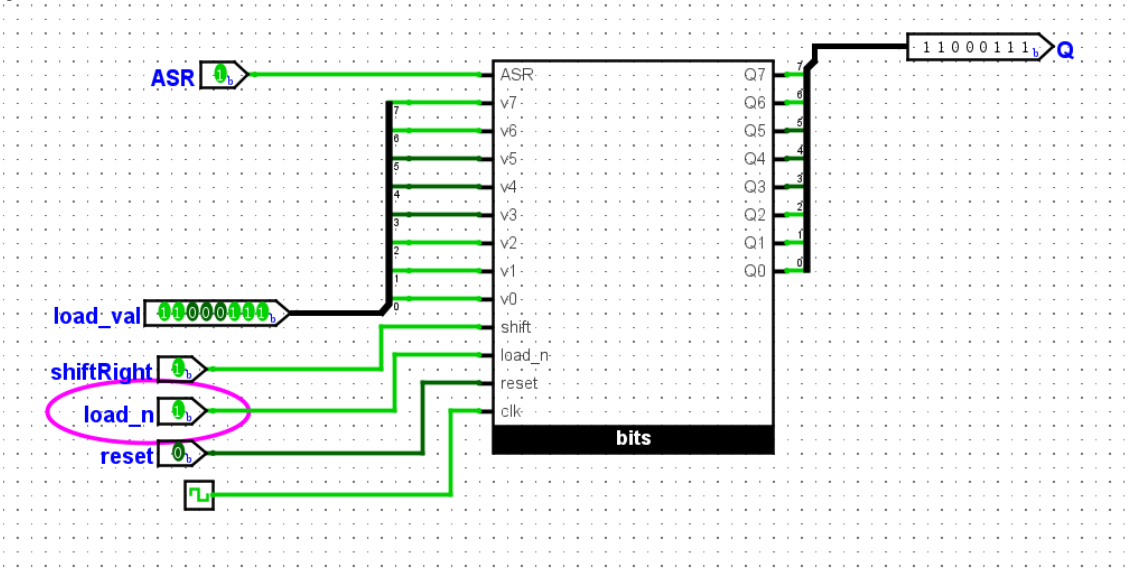
Part III

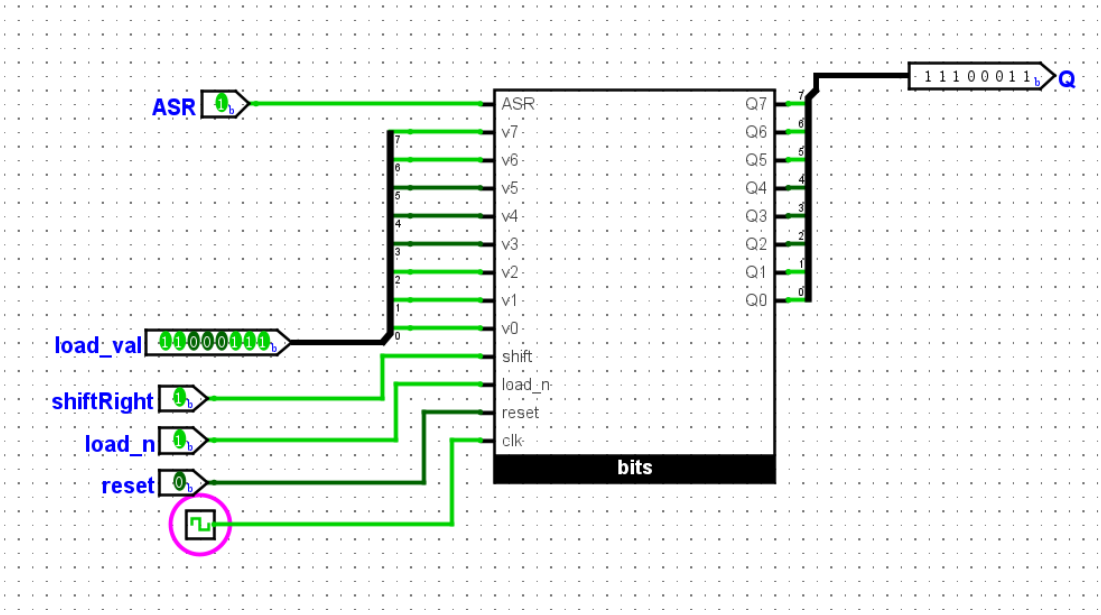
1. The output remains the same regardless of what you do to other inputs. When $load_n = 1$ and $rightShift = 0$, the second mux chooses the second input, and the first mux choose the first input inside the shifter bit. So whatever is in the output get passed to the output, making the output remains the same.

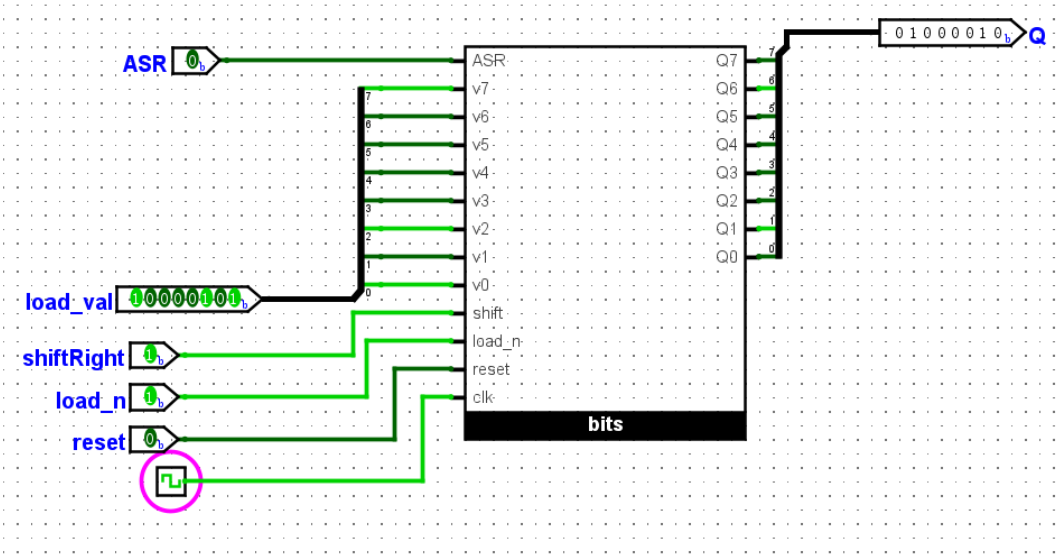
2.



5.




ASR
load_val
shiftRight
load_n
reset
ASR
v7
v6
v5
v4
v3
v2
v1
v0
shift
load_n
reset
clk
bits
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
Q


ASR
load_val
shiftRight
load_n
reset
ASR
v7
v6
v5
v4
v3
v2
v1
v0
shift
load_n
reset
clk
bits
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
Q