Lab 1 Building Circuits using Logism Evolution

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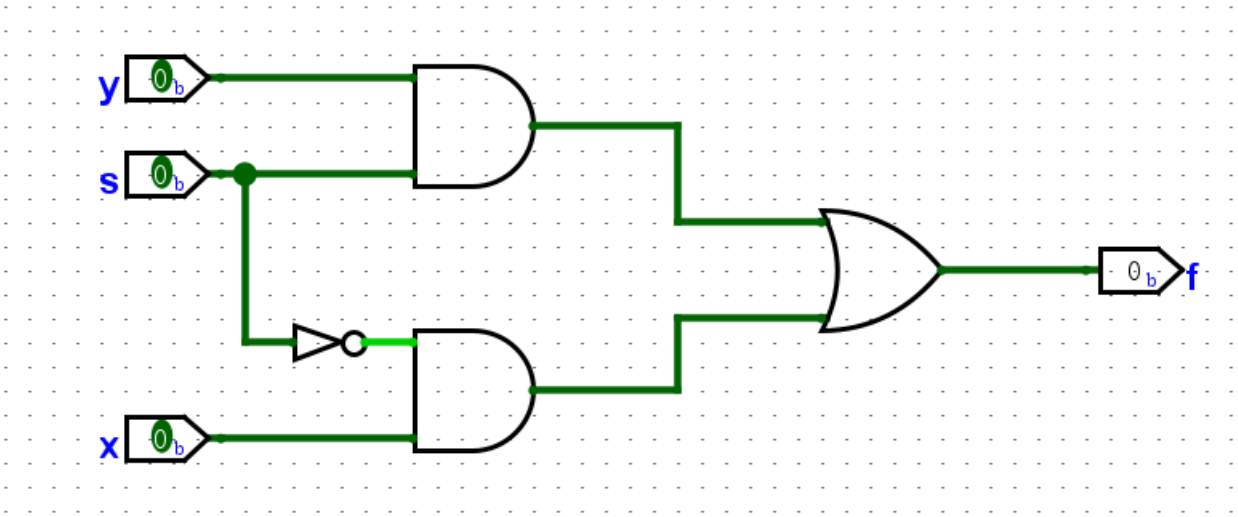
September 23, 2020

Part I

1. Below is the gate diagram for $f = xs' + ys$

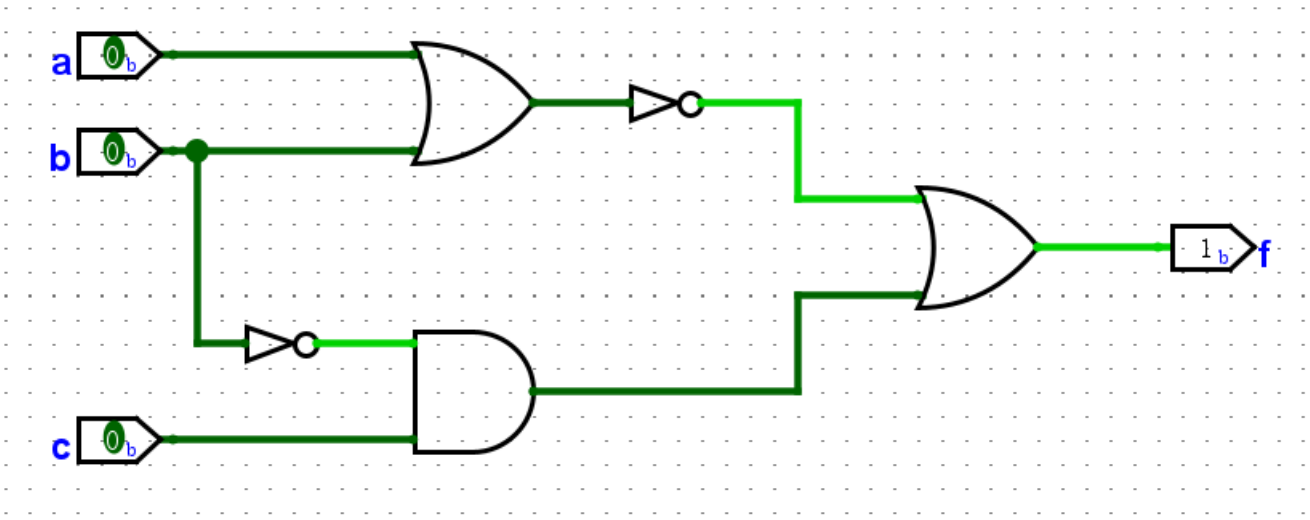


2. The truth table for the function:

y	s	x	f
0	0	0	0
0	0	1	1
0	1	0	0
1	0	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	1

Part II

1. Below is the gate diagram for $f = (a + b)' + cb'$



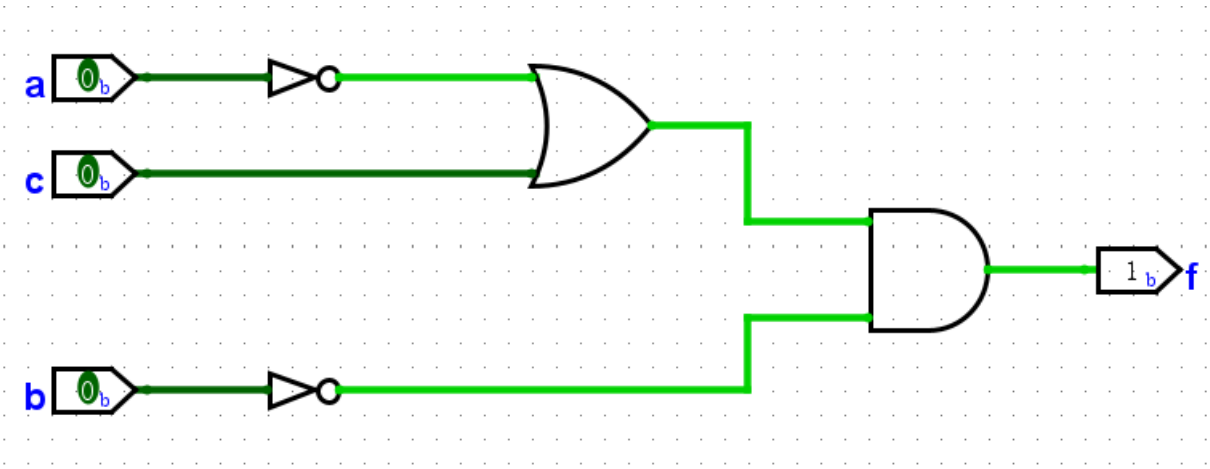
2. The truth table for the function:

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
1	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0
1	1	1	0

3. The diagram in section 1 can be simplified. Perform the following calculation:

$$
\begin{aligned}
f &= (a+b)' + cb' \\
&= (a'b') + cb' \\
&= (a'b' + c)(a'b' + b') && \text{(by distributive law)} \\
&= (a'b' + c)b' && \text{(since b' being true is equvalent to a'b'+b' being true)} \\
&= (a' + c)b' && \text{(since b' is satisfied by the second part, it can be removed)}
\end{aligned}
$$

Re-draw the diagram:



Note there are five gates in the diagram in section 1, but there are only four gates in this diagram, so this is a cheaper implementation of the design.