Cyclone V SoC Development & Education Board (DE0-Nano-SoC-HDMI)

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Title: **DE0-Nano-SoC-HDMI Board**

Size	Document Number	Rev
B	Cover Page	B0

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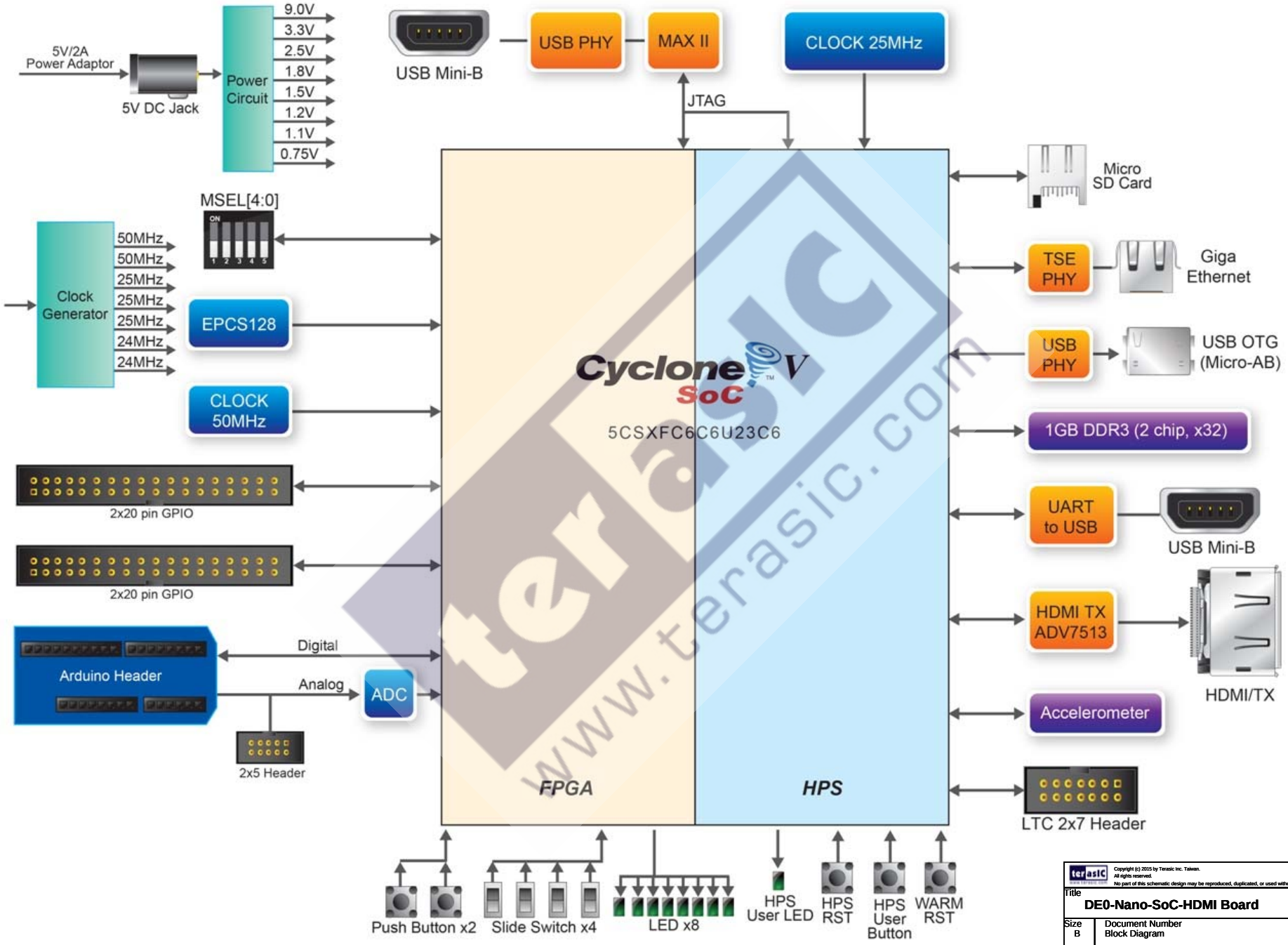

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Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	Block Diagram	B0

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CYCLONE V SoC BANK 3

Bank 3A
VCCIO = 3.3V

GPIO_0_D32	Y11	IO_3A/PR_ERROR/DIFFIO_RX_B7P	
GPIO_0_D35	AA11	IO_3A/PR_DONE/DIFFIO_RX_B7N	
GPIO_0_D10	AD5	IO_3A/DIFFIO_TX_B8P/DQ1B	
GPIO_0_D13	AE6	IO_3A/PR_READY/DIFFIO_TX_B8N/DQ1B	

Bank 3B
VCCIO = 3.3V

HDMI_TX_D16	AE4	IO_3B/DIFFIO_TX_B9P/B_WEN/DQ2B	IO_3B/DIFFIO_TX_B17P/B_BA_0/DQ3B	AF7	GPIO_0_D6
GPIO_0_D8	AF4	IO_3B/DIFFIO_TX_B9N/GND	IO_3B/DIFFIO_TX_B17N/GND	AG6	HDMI_TX_D21
HDMI_TX_D5	AD10	IO_3B/DIFFIO_RX_B10P/B_A_14/DQ2B	IO_3B/DIFFIO_RX_B18P/B_BA_1/DQ3B	AF11	HDMI_TX_INT
HDMI_TX_D10	AE9	IO_3B/DIFFIO_RX_B10N/B_A_15/DQ2B	IO_3B/DIFFIO_RX_B18N/B_BA_2/DQ3B	AF10	HDMI_TX_D8
HDMI_LRCLK	T11	IO_3B/DIFFIO_RX_B11P/B_CSN_0/DQS2B	IO_3B/DIFFIO_RX_B19P/B_CK/DQS3B	T13	HDMI_I2S0
HDMI_MCLK	U11	IO_3B/DIFFIO_RX_B11N/B_CSN_1/DQSN2B	IO_3B/DIFFIO_RX_B19N/B_CKN/DQSN3B	T12	HDMI_SCLK
HDMI_TX_D12	AE7	IO_3B/DIFFIO_TX_B12P/B_A_12	IO_3B/DIFFIO_TX_B20P/B_A_6	AH3	GPIO_0_D9
HDMI_TX_D14	AF8	IO_3B/DIFFIO_TX_B12N/B_A_13/DQ2B	IO_3B/DIFFIO_TX_B20N/B_A_7/DQ3B	AH2	HDMI_TX_D17
HDMI_TX_D23	AE8	IO_3B/DIFFIO_TX_B13P/B_A_10/DQ2B			
HDMI_TX_D22	AF9	IO_3B/DIFFIO_TX_B13N/B_A_11/DQ2B			
HDMI_TX_D4	AD11	IO_3B/DIFFIO_RX_B14P/B_A_8/DQ2B	IO_3B/DIFFIO_RX_B22P/B_A_4/DQ3B	AE12	HDMI_TX_D1
HDMI_TX_D6	AE11	IO_3B/DIFFIO_RX_B14N/B_A_9/DQ2B	IO_3B/DIFFIO_RX_B22N/B_A_5/DQ3B	AD12	HDMI_TX_D0
HDMI_TX_D15	AF5	IO_3B/DIFFIO_TX_B16P/B_CASN/DQ2B	IO_3B/DIFFIO_TX_B24P/B_A_0/DQ3B	AH6	HDMI_TX_D20
HDMI_TX_D13	AF6	IO_3B/DIFFIO_TX_B16N/B_RASN/DQ2B	IO_3B/DIFFIO_TX_B24N/B_A_1/DQ3B	AH5	HDMI_TX_D19

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CYCLONE V SoC BANK 5

Bank 5A
VCCIO = 3.3V

LED4	AF26	IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R			
LED5	AE26	IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R			
			IO_5A/DIFFIO_RX_R6P/DQS1R	Y16	LED6
			IO_5A/DIFFIO_RX_R6N/DQSN1R	W15	LED0
			IO_5A/DIFFIO_TX_R7P/DQ1R	AA24	LED1
GPIO_1_D3	AD26		IO_5A/DIFFIO_TX_R7N	AA23	LED7
GPIO_0_D29	Y17	IO_5A/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R	IO_5A/DIFFIO_RX_R8P/DQ1R	V16	LED2
GPIO_0_D28	Y18	IO_5A/DIFFIO_RX_R4P/DQ1R	IO_5A/DIFFIO_RX_R8N/DQ1R	V15	LED3
		IO_5A/DIFFIO_RX_R4N/DQ1R			

Bank 5B
VCCIO = 3.3V

GPIO_0_D30	AB25	IO_5B/RZQ_2/DIFFIO_TX_R24N

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CYCLONE V SoC BANK 4

Bank 4A
VCCIO = 3.3V

Arduino_Reset_n	AH7	IO_4A/RZQ_0/DIFFIO_TX_B25N			
Arduino_IO6	AG8	IO_4A/DIFFIO_TX_B25P/B_DQ_2/DQ4B	IO_4A/DIFFIO_TX_B41P/B_DQ_18/DQ6B	AF18	GPIO_1_D30
Arduino_IO0	AG13	IO_4A/DIFFIO_RX_B26P/B_DQ_1/DQ4B	IO_4A/DIFFIO_RX_B42P/B_DQ_17/DQ6B	AE19	GPIO_1_D34
Arduino_IO1	AF13	IO_4A/DIFFIO_RX_B26N/B_DQ_0/DQ4B	IO_4A/DIFFIO_RX_B42N/B_DQ_16/DQ6B	AD19	HDMI_TX_DE
Arduino_IO4	U14	IO_4A/DIFFIO_RX_B27P/B_DQS_0/DQS4B	IO_4A/DIFFIO_RX_B43P/B_DQS_2/DQS6B	AA19	GPIO_0_D24
Arduino_IO5	U13	IO_4A/DIFFIO_RX_B27N/B_DQSN_0/DQSN4B	IO_4A/DIFFIO_RX_B43N/B_DQSN_2/DQSN6B	AA18	GPIO_0_D26
Arduino_IO3	AG9	IO_4A/DIFFIO_TX_B28P/B_ODT_0	IO_4A/DIFFIO_TX_B44P/B_RESETN	AG18	GPIO_1_D28
Arduino_IO7	AH8	IO_4A/DIFFIO_TX_B28N/B_DQ_3/DQ4B	IO_4A/DIFFIO_TX_B44N/B_DQ_19/DQ6B	AH18	GPIO_1_D29
Arduino_IO2	AG10	IO_4A/DIFFIO_TX_B29P/B_DQ_6/DQ4B	IO_4A/DIFFIO_TX_B45P/B_DQ_22/DQ6B	AG19	GPIO_1_D26
Arduino_IO14	AH9	IO_4A/DIFFIO_TX_B29N/B_ODT_1/DQ4B	IO_4A/DIFFIO_TX_B45N/GND/DQ6B	AH19	GPIO_1_D27
Arduino_IO10	AF15	IO_4A/DIFFIO_RX_B30P/B_DQ_5/DQ4B	IO_4A/DIFFIO_RX_B46P/B_DQ_21/DQ6B	AE20	GPIO_1_D33
Arduino_IO9	AE15	IO_4A/DIFFIO_RX_B30N/B_DQ_4/DQ4B	IO_4A/DIFFIO_RX_B46N/B_DQ_20/DQ6B	AD20	GPIO_0_D17
Arduino_IO15	AG11			AF20	GPIO_1_D31
Arduino_IO12	AH11	IO_4A/DIFFIO_TX_B32P/B_DM_0/DQ4B	IO_4A/DIFFIO_TX_B48P/B_DM_2/DQ6B	AG20	GPIO_1_D24
		IO_4A/DIFFIO_TX_B32N/B_DQ_7/DQ4B	IO_4A/DIFFIO_TX_B48N/B_DQ_23/DQ6B		
Arduino_IO13	AH12	IO_4A/DIFFIO_TX_B33P/B_DQ_10/DQ5B	IO_4A/DIFFIO_TX_B49P/B_DQ_26/DQ7B	AG21	GPIO_1_D19
Arduino_IO8	AF17	IO_4A/DIFFIO_RX_B34P/B_DQ_9/DQ5B	IO_4A/DIFFIO_RX_B50P/B_DQ_25/DQ7B	AF22	GPIO_1_D22
Arduino_IO11	AG16	IO_4A/DIFFIO_RX_B34N/B_DQ_8/DQ5B	IO_4A/DIFFIO_RX_B50N/B_DQ_24/DQ7B	AF21	GPIO_1_D25
GPIO_0_D27	W14	IO_4A/DIFFIO_RX_B35P/B_DQS_1/DQS5B	IO_4A/DIFFIO_RX_B51P/B_DQS_3/DQS7B	AD23	GPIO_0_D14
HDMI_TX_VS	V13	IO_4A/DIFFIO_RX_B35N/B_DQSN_1/DQSN5B	IO_4A/DIFFIO_RX_B51N/B_DQSN_3/DQSN7B	AE22	GPIO_1_D23
GPIO_0_D11	AG14	IO_4A/DIFFIO_TX_B36P/B_CKE_1			
GPIO_0_D5	AH13	IO_4A/DIFFIO_TX_B36N/B_DQ_11/DQ5B	IO_4A/DIFFIO_TX_B52N/B_DQ_27/DQ7B	AH21	GPIO_1_D18
GPIO_1_D32	AG15	IO_4A/DIFFIO_TX_B37P/B_DQ_14/DQ5B	IO_4A/DIFFIO_TX_B53P/B_DQ_30/DQ7B	AH23	GPIO_1_D20
GPIO_0_D7	AH14	IO_4A/DIFFIO_TX_B37N/B_CKE_0/DQ5B	IO_4A/DIFFIO_TX_B53N/GND/DQ7B	AH22	GPIO_1_D17
GPIO_0_D19	AD17	IO_4A/DIFFIO_RX_B38P/B_DQ_13/DQ5B	IO_4A/DIFFIO_RX_B54P/B_DQ_29/DQ7B	AG23	GPIO_1_D14
GPIO_1_D35	AE17	IO_4A/DIFFIO_RX_B38N/B_DQ_12/DQ5B	IO_4A/DIFFIO_RX_B54N/B_DQ_28/DQ7B	AF23	GPIO_1_D15
KEY0	AH17			AG24	GPIO_1_D16
KEY1	AH16	IO_4A/DIFFIO_TX_B40P/B_DM_1/DQ5B	IO_4A/DIFFIO_TX_B56P/B_DM_3/DQ7B	AH24	GPIO_1_D12
		IO_4A/DIFFIO_TX_B40N/B_DQ_15/DQ5B	IO_4A/DIFFIO_TX_B56N/B_DQ_31/DQ7B		
			IO_4A/DIFFIO_TX_B57P/B_DQ_34/DQ8B	AG26	GPIO_1_D8
			IO_4A/DIFFIO_RX_B58P/B_DQ_33/DQ8B	AE24	GPIO_0_D15
			IO_4A/DIFFIO_RX_B58N/B_DQ_32/DQ8B	AE23	GPIO_0_D12
			IO_4A/DIFFIO_RX_B59P/B_DQS_4/DQS8B	AC22	GPIO_0_D21
			IO_4A/DIFFIO_RX_B59N/B_DQSN_4/DQSN8B	AC23	GPIO_0_D20
			IO_4A/DIFFIO_TX_B60N/B_DQ_35/DQ8B	AH26	GPIO_1_D11
			IO_4A/DIFFIO_TX_B61P/B_DQ_38/DQ8B	AG28	GPIO_1_D4
			IO_4A/DIFFIO_TX_B61N/GND/DQ8B	AH27	GPIO_1_D9
			IO_4A/DIFFIO_RX_B62P/B_DQ_37/DQ8B	AF25	GPIO_1_D13
			IO_4A/DIFFIO_RX_B62N/B_DQ_36/DQ8B	AG25	GPIO_1_D10
			IO_4A/DIFFIO_TX_B64P/B_DM_4/DQ8B	AF27	GPIO_1_D7
			IO_4A/DIFFIO_TX_B64N/B_DQ_39/DQ8B	AF28	GPIO_1_D5

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User Interface (FPGA)

20	KEY[1..0]	
20	LED[7..0]	

GPIO

6,7,19	GPIO_0_D[35..0]	
6,19	GPIO_1_D[35..0]	

Arduino Digital Interface

19	Arduino_IO[15..0]	
19	Arduino_Reset_n	

HDMI TX

6,21	HDMI_TX_D[23..0]	
6,21	HDMI_TX_CLK	
6,21	HDMI_TX_HS	
6,21	HDMI_TX_VS	
6,21	HDMI_TX_DE	

HDMI Audio Interface

21	HDMI_MCLK	
21	HDMI_LRCLK	
21	HDMI_I2S0	
21	HDMI_SCLK	

HDMI Interface

21	HDMI_TX_INT	
21	HDMI_TX_DE	
21	HDMI_TX_VS	

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Title: **DE0-Nano-SoC-HDMI Board**

Size	Document Number	Rev
B	FPGA Bank 3, 4, 5, 8	B0

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DDR3 Interface (HPS)

12 HPS_DDR3_ADDR[14..0]
12 HPS_DDR3_BA[2..0]
12 HPS_DDR3_DM[3..0]
12 HPS_DDR3_DQ[31..0]
12 HPS_DDR3_DQS_P[3..0]
12 HPS_DDR3_DQS_N[3..0]
12 HPS_DDR3_RESET_N
12 HPS_DDR3_CK_P
12 HPS_DDR3_CK_N
12 HPS_DDR3_CAS_N
12 HPS_DDR3_RAS_N
12 HPS_DDR3_CS_N
12 HPS_DDR3_WE_N
12 HPS_DDR3_ODT
12 HPS_DDR3_CKE
12 HPS_DDR3_CS1_N
12 HPS_DDR3_CKE1
12 HPS_DDR3_ODT1

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CYCLONE V SoC BANK 6 (HPS)

Bank 6A
VCCIO = 1.5V

R117 100 HPS_DDR3_RZQ D25 — HPS_RZQ_0

HPS_DDR3_ADDR0	C28	HPS_DDR/HPS_A_0
HPS_DDR3_ADDR1	B28	HPS_DDR/HPS_A_1
HPS_DDR3_ADDR2	E26	HPS_DDR/HPS_A_2
HPS_DDR3_ADDR3	D26	HPS_DDR/HPS_A_3
HPS_DDR3_ADDR4	J21	HPS_DDR/HPS_A_4
HPS_DDR3_ADDR5	J20	HPS_DDR/HPS_A_5
HPS_DDR3_ADDR6	C26	HPS_DDR/HPS_A_6
HPS_DDR3_ADDR7	B26	HPS_DDR/HPS_A_7
HPS_DDR3_ADDR8	F26	HPS_DDR/HPS_A_8
HPS_DDR3_ADDR9	F25	HPS_DDR/HPS_A_9
HPS_DDR3_ADDR10	A24	HPS_DDR/HPS_A_10
HPS_DDR3_ADDR11	B24	HPS_DDR/HPS_A_11
HPS_DDR3_ADDR12	D24	HPS_DDR/HPS_A_12
HPS_DDR3_ADDR13	C24	HPS_DDR/HPS_A_13
HPS_DDR3_ADDR14	G23	HPS_DDR/HPS_A_14
	F24	HPS_DDR/HPS_A_15

HPS_DDR3_CK_P	N21	HPS_DDR/HPS_CK
HPS_DDR3_CK_N	N20	HPS_DDR/HPS_CKn
HPS_DDR3_CKE	L28	HPS_DDR/HPS_CKE_0
HPS_DDR3_CKE1	K28	HPS_DDR/HPS_CKE_1
HPS_DDR3_BA0	A27	HPS_DDR/HPS_BA_0
HPS_DDR3_BA1	H25	HPS_DDR/HPS_BA_1
HPS_DDR3_BA2	G25	HPS_DDR/HPS_BA_2
HPS_DDR3_RAS_N	A25	HPS_DDR/HPS_RASn
HPS_DDR3_CAS_N	A26	HPS_DDR/HPS_CASn
HPS_DDR3_WE_N	E25	HPS_DDR/HPS_WEn
HPS_DDR3_CS_N	L21	HPS_DDR/HPS_CSn_0
HPS_DDR3_CS1_N	L20	HPS_DDR/HPS_CSn_1
HPS_DDR3_ODT	D28	HPS_DDR/HPS_ODT_0
HPS_DDR3_ODT1	G26	HPS_DDR/HPS_ODT_1

HPS_DDR3_DQ0	J25	HPS_DDR/HPS_DQ_0
HPS_DDR3_DQ1	J24	HPS_DDR/HPS_DQ_1
HPS_DDR3_DQ2	E28	HPS_DDR/HPS_DQ_2
HPS_DDR3_DQ3	D27	HPS_DDR/HPS_DQ_3
HPS_DDR3_DQ4	J26	HPS_DDR/HPS_DQ_4
HPS_DDR3_DQ5	K26	HPS_DDR/HPS_DQ_5
HPS_DDR3_DQ6	G27	HPS_DDR/HPS_DQ_6
HPS_DDR3_DQ7	F28	HPS_DDR/HPS_DQ_7
HPS_DDR3_DQS_P0	R17	HPS_DDR/HPS_DQS_0
HPS_DDR3_DQS_N0	R16	HPS_DDR/HPS_DQSn_0
HPS_DDR3_DM0	G28	HPS_DDR/HPS_DM_0
HPS_DDR3_DQ8	K25	HPS_DDR/HPS_DQ_8
HPS_DDR3_DQ9	L25	HPS_DDR/HPS_DQ_9
HPS_DDR3_DQ10	J27	HPS_DDR/HPS_DQ_10
HPS_DDR3_DQ11	J28	HPS_DDR/HPS_DQ_11
HPS_DDR3_DQ12	M27	HPS_DDR/HPS_DQ_12
HPS_DDR3_DQ13	M26	HPS_DDR/HPS_DQ_13
HPS_DDR3_DQ14	M28	HPS_DDR/HPS_DQ_14
HPS_DDR3_DQ15	N28	HPS_DDR/HPS_DQ_15
HPS_DDR3_DQS_P1	R19	HPS_DDR/HPS_DQS_1
HPS_DDR3_DQS_N1	R18	HPS_DDR/HPS_DQSn_1
HPS_DDR3_DM1	P28	HPS_DDR/HPS_DM_1

	U15	HPS_GPI10
	U16	HPS_GPI11
	AC27	HPS_GPI12
	V24	HPS_GPI13

Bank 6B
VCCIO = 1.5V

HPS_DDR3_DQ16	N24	HPS_DDR/HPS_DQ_16
HPS_DDR3_DQ17	N25	HPS_DDR/HPS_DQ_17
HPS_DDR3_DQ18	T28	HPS_DDR/HPS_DQ_18
HPS_DDR3_DQ19	U28	HPS_DDR/HPS_DQ_19
HPS_DDR3_DQ20	N26	HPS_DDR/HPS_DQ_20
HPS_DDR3_DQ21	N27	HPS_DDR/HPS_DQ_21
HPS_DDR3_DQ22	R27	HPS_DDR/HPS_DQ_22
HPS_DDR3_DQ23	V27	HPS_DDR/HPS_DQ_23
HPS_DDR3_DQS_P2	T19	HPS_DDR/HPS_DQS_2
HPS_DDR3_DQS_N2	T18	HPS_DDR/HPS_DQSn_2
HPS_DDR3_DM2	W28	HPS_DDR/HPS_DM_2
HPS_DDR3_DQ24	R26	HPS_DDR/HPS_DQ_24
HPS_DDR3_DQ25	R25	HPS_DDR/HPS_DQ_25
HPS_DDR3_DQ26	AA28	HPS_DDR/HPS_DQ_26
HPS_DDR3_DQ27	W26	HPS_DDR/HPS_DQ_27
HPS_DDR3_DQ28	R24	HPS_DDR/HPS_DQ_28
HPS_DDR3_DQ29	T24	HPS_DDR/HPS_DQ_29
HPS_DDR3_DQ30	Y27	HPS_DDR/HPS_DQ_30
HPS_DDR3_DQ31	AA27	HPS_DDR/HPS_DQ_31
HPS_DDR3_DQS_P3	U19	HPS_DDR/HPS_DQS_3
HPS_DDR3_DQS_N3	T20	HPS_DDR/HPS_DQSn_3
HPS_DDR3_DM3	AB28	HPS_DDR/HPS_DM_3

	T26	HPS_DDR/HPS_DQ_32
	U25	HPS_DDR/HPS_DQ_33
	AC28	HPS_DDR/HPS_DQ_34
	V25	HPS_DDR/HPS_DQ_35
	V19	HPS_DDR/HPS_DQ_36
	V20	HPS_DDR/HPS_DQ_37
	AE27	HPS_DDR/HPS_DQ_38
	AD28	HPS_DDR/HPS_DQ_39
	V18	HPS_DDR/HPS_DQS_4
	V17	HPS_DDR/HPS_DQSn_4
	AE28	HPS_DDR/HPS_DM_4
	M25	HPS_GPI0
	K27	HPS_GPI1
	R20	HPS_GPI2
	R21	HPS_GPI3
	R28	HPS_GPI4
	P26	HPS_GPI5
	T17	HPS_GPI6
	T16	HPS_GPI7
	Y28	HPS_GPI8
	Y26	HPS_GPI9
HPS_DDR3_RESET_N	V28	HPS_DDR/HPS_RESETn

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Title: DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	FPGA Bank 6	B0

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UBS PHY Interface (ULPI)

14 HPS_USB_DATA[7..0]
14 HPS_USB_CLKOUT
14 HPS_USB_NXT
14 HPS_USB_DIR
14 HPS_USB_STP
10,14 HPS_USB_RESET

Ethernet PHY Interface (RGMII)

15 HPS_ENET_TX_DATA[3..0]
15 HPS_ENET_GTX_CLK
15 HPS_ENET_TX_EN
15 HPS_ENET_RX_DATA[3..0]
15 HPS_ENET_RX_CLK
15 HPS_ENET_RX_DV
15 HPS_ENET_INT_N
15 HPS_ENET_MDC
15 HPS_ENET_MDIO
10,15,17 HPS_ENET_RESET_N

SD Card Interface

13 HPS_SD_DATA[3..0]
13 HPS_SD_CMD
13 HPS_SD_CLK

UART Interface

13 HPS_UART_RX
13 HPS_UART_TX
13 HPS_CONV_USB_N

HPS Reset

10,17 HPS_WARM_RST_N
10,17 HPS_RESET_N

HPS Clock

6 HPS_CLK1_25
6 HPS_CLK2_25

HPS JTAG INTERFACE

11 HPS_TCK
11 HPS_TMS
11 HPS_TDI
11 HPS_TDO
10 JTAG_TRST

Accelerometer Interface

16 HPS_I2C0_SDAT
16 HPS_I2C0_SCLK
16 HPS_GSENSOR_INT

LTC Interface

16 HPS_I2C1_SDAT
16 HPS_I2C1_SCLK
16 HPS_SPIM_MOSI
16 HPS_SPIM_MISO
16 HPS_SPIM_CLK
16 HPS_SPIM_SS
16 HPS_LTC_GPIO

HPS Key and LED

17 HPS_KEY
17 HPS_LED

VCC3P3
R143 4.7K HPS_PORSEL
R118 4.7K JTAG_TRST
R119 0 DNI HPS_TCK
HPS_TMS HPS_TDI HPS_TDO
C89 33p 50V DNI

U1M

CYCLONE V SoC BANK 7 (HPS)

Bank 7A
VCCIO = 3.3V

HPS_WARM_RST_N A23 — HPS_NRST
HPS_RESET_N H19 — HPS_NPOR
HPS_CLK1_25 E20 — HPS_CLK1
HPS_CLK2_25 D20 — HPS_CLK2
HPS_PORSEL E18
JTAG_TRST C22 — HPS_TRST
HPS_TCK K19
HPS_TMS C23
HPS_TDI D22
HPS_TDO B23

TRACE_CLK/ - / - /HPS_GPIO48 C21
TRACE_D0/SPIS0_CLK/UART0_RX/HPS_GPIO49 A22 HPS_UART_RX
TRACE_D1/SPIS0_MOSI/UART0_TX/HPS_GPIO50 B21 HPS_UART_TX
TRACE_D2/SPIS0_MISO/I2C1_SDA/HPS_GPIO51 A21 HPS_I2C1_SDAT
TRACE_D3/SPIS0_SS0/I2C1_SCL/HPS_GPIO52 K18 HPS_I2C1_SCLK
TRACE_D4/SPIS1_CLK/CAN1_RX/HPS_GPIO53 A20 HPS_LED
TRACE_D5/SPIS1_MOSI/CAN1_TX/HPS_GPIO54 J18 HPS_KEY
TRACE_D6/SPIS1_SS0/I2C0_SDA/HPS_GPIO55 A19 HPS_I2C0_SDAT
TRACE_D7/SPIS1_MISO/I2C0_SCL/HPS_GPIO56 C18 HPS_I2C0_SCLK
SPIM0_CLK/I2C1_SDA/UART0_CTS/HPS_GPIO57 A18
SPIM0_MOSI/I2C1_SCL/UART0_RTS/HPS_GPIO58 C17
SPIM0_MISO/CAN1_RX/UART1_CTS/HPS_GPIO59 B18
SPIM0_SS0,BOOTSEL0/CAN1_TX/UART1_RTS/HPS_GPIO60 J17 HPS_BOOTSEL0
UART0_RX/CAN0_RX/SPIM0_SS1/HPS_GPIO61 A17 HPS_GSENSOR_INT
UART0_TX,CLKSEL1/CAN0_TX/SPIM1_SS1/HPS_GPIO62 H17 HPS_CLOCKSEL1
I2C0_SDA/UART1_RX/SPIM1_CLK/HPS_GPIO63 C19 HPS_SPIM_CLK
I2C0_SCL/UART1_TX/SPIM1_MOSI/HPS_GPIO64 B16 HPS_SPIM_MOSI
CAN0_RX/UART0_RX/SPIM1_MISO/HPS_GPIO65 B19 HPS_SPIM_MISO
CAN0_TX,CLKSEL0/UART0_TX/SPIM1_SS0/HPS_GPIO66 C16 HPS_SPIM_SS

Bank 7B
VCCIO = 3.3V

HPS_ENET_GTX_CLK J15
HPS_ENET_TX_DATA0 A16
HPS_ENET_TX_DATA1 J14
HPS_ENET_TX_DATA2 A15
HPS_ENET_TX_DATA3 D17
HPS_ENET_RX_DATA0 A14
HPS_ENET_MDIO E16
HPS_ENET_MDC A13
HPS_ENET_RX_DV J13
HPS_ENET_TX_EN A12
HPS_ENET_RX_CLK J12
HPS_ENET_RX_DATA1 A11
HPS_ENET_RX_DATA2 C15
HPS_ENET_RX_DATA3 A9
HPS_BOOTSEL2 D15

NAND_ALE/RGMII1_TX_CLK/QSPI_SS3/HPS_GPIO14
NAND_CE/RGMII1_TXD0/USB1_D0/HPS_GPIO15
NAND_CLE/RGMII1_TXD1/USB1_D1/HPS_GPIO16
NAND_RE/RGMII1_TXD2/USB1_D2/HPS_GPIO17
NAND_RB/RGMII1_TXD3/USB1_D3/HPS_GPIO18
NAND_DQ0/RGMII1_RXD0/ - /HPS_GPIO19
NAND_DQ1/RGMII1_MDIO/I2C3_SDA/HPS_GPIO20
NAND_DQ2/RGMII1_MDC/I2C3_SCL/HPS_GPIO21
NAND_DQ3/RGMII1_RX_CTL/USB1_D4/HPS_GPIO22
NAND_DQ4/RGMII1_TX_CTL/USB1_D5/HPS_GPIO23
NAND_DQ5/RGMII1_RX_CLK/USB1_D6/HPS_GPIO24
NAND_DQ6/RGMII1_RXD1/USB1_D7/HPS_GPIO25
NAND_DQ7/RGMII1_RXD2/ - /HPS_GPIO26
NAND_WP/RGMII1_RXD3/QSPI_SS2/HPS_GPIO27
NAND_WE,BOOTSEL2/QSPI_SS1/ - /HPS_GPIO28

QSPI_IO0/ - /USB1_CLK/HPS_GPIO29 A8
QSPI_IO1/ - /USB1_STP/HPS_GPIO30 H16
QSPI_IO2/ - /USB1_DIR/HPS_GPIO31 A7
QSPI_IO3/ - /USB1_NXT/HPS_GPIO32 J16
QSPI_SS0,BOOTSEL1/ - / - /HPS_GPIO33 A6 HPS_BOOTSEL1
QSPI_CLK/ - / - /HPS_GPIO34 C14
QSPI_SS1/ - / - /HPS_GPIO35 B14 HPS_ENET_INT_N

Bank 7C
VCCIO = 3.3V

HPS_SD_CMD D14
HPS_SD_DATA0 C13
HPS_SD_DATA1 B6
HPS_SD_DATA2 B11
HPS_SD_DATA3 B9
B12

SDMMC_CMD/USB0_D0/ - /HPS_GPIO36
SDMMC_D0/USB0_D2/ - /HPS_GPIO38
SDMMC_D1/USB0_D3/ - /HPS_GPIO39
SDMMC_D2/USB0_DIR/ - /HPS_GPIO46
SDMMC_D3/USB0_NXT/ - /HPS_GPIO47
SDMMC_FB_CLK_IN/USB0_CLK/ - /HPS_GPIO44

SDMMC_PWREN/USB0_D1/ - /HPS_GPIO37 A5
SDMMC_D4/USB0_D4/ - /HPS_GPIO40 H13 HPS_LTC_GPIO
SDMMC_D5/USB0_D5/ - /HPS_GPIO41 A4
SDMMC_D6/USB0_D6/ - /HPS_GPIO42 H12 R120 0 DNI HPS_USB_RESET
SDMMC_D7/USB0_D7/ - /HPS_GPIO43 B4 R121 0 DNI HPS_ENET_RESET_N
SDMMC_CCLK_OUT/USB0_STP/ - /HPS_GPIO45 B8 HPS_SD_CLK

Bank 7D
VCCIO = 3.3V

HPS_USB_DATA4 C8
HPS_USB_STP C5
HPS_USB_DIR E5
HPS_USB_NXT D5
HPS_USB_CLKOUT G4
HPS_USB_DATA7 F4
HPS_USB_DATA5 D4
HPS_USB_DATA6 C7

RGMII0_RXD0/USB1_D4/ - /HPS_GPIO5
RGMII0_RXD1/USB1_STP/ - /HPS_GPIO11
RGMII0_RXD2/USB1_DIR/ - /HPS_GPIO12
RGMII0_RXD3/USB1_NXT/ - /HPS_GPIO13
RGMII0_RX_CLK/USB1_CLK/ - /HPS_GPIO10
RGMII0_RX_CTL/USB1_D7/ - /HPS_GPIO8
RGMII0_MDIO/USB1_D5/I2C2_SDA/HPS_GPIO6
RGMII0_MDC/USB1_D6/I2C2_SCL/HPS_GPIO7

RGMII0_TXD0/USB1_D0/ - /HPS_GPIO1 C10 HPS_USB_DATA0
RGMII0_TXD1/USB1_D1/ - /HPS_GPIO2 F5 HPS_USB_DATA1
RGMII0_TXD2/USB1_D2/ - /HPS_GPIO3 C9 HPS_USB_DATA2
RGMII0_TXD3/USB1_D3/ - /HPS_GPIO4 C4 HPS_USB_DATA3
RGMII0_TX_CTL/ - / - /HPS_GPIO9 C6 HPS_CONV_USB_N
RGMII0_TX_CLK/ - / - /HPS_GPIO0 E4

5CSXFC6C6U23C6N

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0] =00

VCC3P3
DNI R127 1K HPS_BOOTSEL0 (BOOTSEL0) R140 10K
R126 1K HPS_BOOTSEL1 (BOOTSEL1) R139 10K DNI
DNI R125 1K HPS_BOOTSEL2 (BOOTSEL2) R138 10K
R124 1K HPS_SPIM_SS (CLOCKSEL0) R137 10K DNI
R123 1K HPS_CLOCKSEL1 (CLOCKSEL1) R135 10K DNI

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Title: DE0-Nano-SoC-HDMI Board
Size B | Document Number: FPGA Bank 7 | Rev B0
Date: Monday, March 21, 2016 | Sheet 5 of 24

GPIO

3,7,19 GPIO_0_D[35..0]

3,19 GPIO_1_D[35..0]

User Interface (FPGA)

20 SW[3..0]

Clock Generator

5 HPS_CLK1_25

5 HPS_CLK2_25

15 CLK_ENET_25

10 CLK_UB2_24

14 CLK_USB_24

HDMI TX

3,21 HDMI_TX_D[23..0]

21 HDMI_TX_CLK

21 HDMI_TX_HS

21 HDMI_TX_DE

U1B

CYCLONE V SoC Clock

Bank 3B VCCIO = 3.3V

FPGA_CLK1_50	V11	IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P	IO_3B/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B21P/B_A_2/DQ3B
GPIO_0_D25	W11	IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N	IO_3B/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B21N/B_A_3/DQ3B
GPIO_0_D0	V12	IO_3B/CLK1P/DIFFIO_RX_B23P	
GPIO_0_D2	W12	IO_3B/CLK1N/DIFFIO_RX_B23N	

AG5 HDMI_TX_CLK

AH4 HDMI_TX_D18

Bank 4A VCCIO = 3.3V

FPGA_CLK2_50	Y13	IO_4A/CLK2P/DIFFIO_RX_B31P
GPIO_0_D34	AA13	IO_4A/CLK2N/DIFFIO_RX_B31N
GPIO_1_D0	Y15	IO_4A/CLK3P/DIFFIO_RX_B39P
GPIO_1_D2	AA15	IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B VCCIO = 3.3V

SW0	Y24	IO_5B/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P	IO_5B/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R22P
SW1	W24	IO_5B/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N	IO_5B/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R22N
SW2	W21	IO_5B/CLK5P/DIFFIO_RX_R21P	
SW3	W20	IO_5B/CLK5N/DIFFIO_RX_R21N	

AB26 GPIO_0_D31

AA26 GPIO_0_D33

Bank 8A VCCIO = 3.3V

FPGA_CLK1_50 R159 0

FPGA_CLK3_50	E11	IO_8A/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P	IO_8A/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T4P
GPIO_0_D3	D11	IO_8A/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N	IO_8A/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T4N
GPIO_0_D16	D12	IO_8A/CLK7P/DIFFIO_RX_T1P	
GPIO_0_D18	C12	IO_8A/CLK7N/DIFFIO_RX_T1N	

E8 GPIO_0_D1

D8 GPIO_0_D4

5CSXFC6C6U23C6N

Factory Default Configuration:
50MHz x2
25MHz x3
24MHz x2

CAD Note: Place near pin 3 and 5 (C3 & C322)

CAD Note: Place near IC power pin

VCC1P8 — L4 220 ohm, 0.3A — C247 4.7u 6.3V, C49 0.01u 50V, C50 1n 50V

L17 220 ohm, 0.3A — VCC3P3 — C253 0.1u 16V, C244 0.1u 16V, C246 0.1u 16V, C252 4.7u 6.3V

U15 CDCE937PWRG4

C236 4p 6.3V DNI

Y1 24.00MHz

C245 4p 6.3V DNI

CLK_I2C_SDA

CLK_I2C_SCL

R174 4.7K DNI

R175 4.7K DNI

VCC3P3

Y1	R47	18.2	CLK_UB2_24	Default: 24MHz
Y2	R48	18.2	CLK_ENET_25	Default: 25MHz
Y3	R49	18.2	CLK_USB_24	Default: 24MHz
Y4	R54	18.2	HPS_CLK1_25	Default: 25MHz
Y5	R55	18.2	HPS_CLK2_25	Default: 25MHz
Y6	R56	18.2	FPGA_CLK1_50	Default: 50MHz
Y7	R57	18.2	FPGA_CLK2_50	Default: 50MHz

Default : I2C Address 0xDA/0xDB

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Title: DE0-Nano-SoC-HDMI Board

Size B | Document Number: FPGA Clock and Clock Generator | Rev B0

Date: Thursday, April 28, 2016 | Sheet 6 of 24

FPGA JTAG INTERFACE

11 FPGA_TCK
11 FPGA_TMS
11 FPGA_TDI
11 FPGA_TDO

USB Blaster

10 FPGA_NCONFIG
10 FPGA_CONF_DONE

GPIO

3,6,19 GPIO_0_D[35..0]
6,19 GPIO_1_D[35..0]

ADC

18 ADC_CONVST
18 ADC_SCK
18 ADC_SDO
18 ADC_SDI

I2C Interface

6,21 HDMI_I2C_SDA
6,21 HDMI_I2C_SCL

6,21 HDMI_TX_D[23..0]
21 HDMI_TX_HS

R171 0 DNI FPGA_TCK
C35 33p 50V DNI
R169 1K

VCC3P3
R176 10K DNI
R178 0 DNI
R177 1K DNI
C237 12p 50V DNI

Design Note:
Optional termination resistor for DCLK

CAD Note:
Place near FPGA DCLK pin

U1A

CYCLONE V SoC Configuration

Bank 3A
VCCIO = 3.3V

FPGA_TCK	AB5	TCK
FPGA_TMS	AC7	TMS
FPGA_TDI	W10	TDI
FPGA_TDO	Y9	TDO
EPCQ_DCLK	AA8	DCLK
EPCQ_AS_DATA0	AD7	AS_DATA0,ASDO/DATA0
EPCQ_AS_DATA1	AC6	AS_DATA1/DATA1
EPCQ_AS_DATA2	AC5	AS_DATA2/DATA2
EPCQ_AS_DATA3	AB6	AS_DATA3/DATA3
EPCQ_nCSO	AA6	NCSO/DATA4
HDMI_TX_D9	Y4	IO_3A/DATA5/DIFFIO_TX_B2N
HDMI_TX_D3	Y8	IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
HDMI_TX_D7	Y5	IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
HDMI_TX_D2	W8	IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
HDMI_TX_D11	AB4	IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
HDMI_TX_HS	T8	IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B
HDMI_I2C_SDA	AA4	IO_3A/DATA11/DIFFIO_TX_B4P
ADC_CONVST	U9	IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B
ADC_SDO	AD4	IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
ADC_SCK	V10	IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
ADC_SDI	AC4	IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
HDMI_I2C_SCL	U10	IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B

Bank 5A
VCCIO = 3.3V

AA20	GPIO_1_D21	IO_5A/INIT_DONE/DIFFIO_RX_R2P
AC24	GPIO_1_D1	IO_5A/DEV_OE/DIFFIO_TX_R5P
AB23	GPIO_0_D23	IO_5A/DEV_CLRn/DIFFIO_TX_R5N/DQ1R
Y19	GPIO_0_D22	IO_5A/CRC_ERROR/DIFFIO_RX_R2N
AE25	GPIO_1_D6	IO_5A/nCEO/DIFFIO_TX_R3P/DQ1R

Bank 9A
VCCIO = 3.3V

J8	FPGA_CONF_DONE	CONF_DONE
H8	FPGA_NSTATUS	nSTATUS
F7	FPGA_NCONFIG	nCONFIG
E6		nCE
J10	MSEL0	MSEL0
H9	MSEL1	MSEL1
G6	MSEL2	MSEL2
K10	MSEL3	MSEL3
K9	MSEL4	MSEL4

5CSXFC6C6U23C6N

VCC3P3
R147 10K
R144 10K
R136 10K

U1N

CYCLONE V SoC BANK XCVR

Bank GXB_L0

AF1	GXB_RX_L0n,GXB_REFCLK_L0n	GXB_TX_L0p	AD2
AF2	GXB_RX_L0p,GXB_REFCLK_L0p	GXB_TX_L0n	AD1
AB1	GXB_RX_L1n,GXB_REFCLK_L1n	GXB_TX_L1p	Y2
AB2	GXB_RX_L1p,GXB_REFCLK_L1p	GXB_TX_L1n	Y1
V1	GXB_RX_L2n,GXB_REFCLK_L2n	GXB_TX_L2p	T2
V2	GXB_RX_L2p,GXB_REFCLK_L2p	GXB_TX_L2n	T1
V5	REFCLK0Lp		
V4	REFCLK0Ln		

Bank GXB_L1

P1	GXB_RX_L3n,GXB_REFCLK_L3n	GXB_TX_L3p	M2
P2	GXB_RX_L3p,GXB_REFCLK_L3p	GXB_TX_L3n	M1
K1	GXB_RX_L4n,GXB_REFCLK_L4n	GXB_TX_L4p	H2
K2	GXB_RX_L4p,GXB_REFCLK_L4p	GXB_TX_L4n	H1
F1	GXB_RX_L5n,GXB_REFCLK_L5n	GXB_TX_L5p	D2
F2	GXB_RX_L5p,GXB_REFCLK_L5p	GXB_TX_L5n	D1
P8	REFCLK1Lp		
N8	REFCLK1Ln		

5CSXFC6C6U23C6N

VCC3P3
C40 0.1u 16V
U28
NC01 NC02 NC03 NC04 NC05 NC06 NC07 NC08
VCC GND
DATA0 DATA1 DATA2 DATA3 DCLK nCS
EPCQ_AS_DATA0 EPCQ_AS_DATA1 EPCQ_AS_DATA2 EPCQ_AS_DATA3 EPCQ_DCLK EPCQ_NCSO
S25FL128

Default Setup MSEL[4:0] = 10010, AS Fast Mode

VCC3P3
SW10
1 2 3 4 5 6
12 11 10 9 8 7
MSEL0 MSEL1 MSEL2 MSEL3 MSEL4
R8 R9 R10 R11 R12 1K
DIP SWITCH

R3 R4 R5 R6 R7 0 DNI
MSEL0 MSEL1 MSEL2 MSEL3 MSEL4

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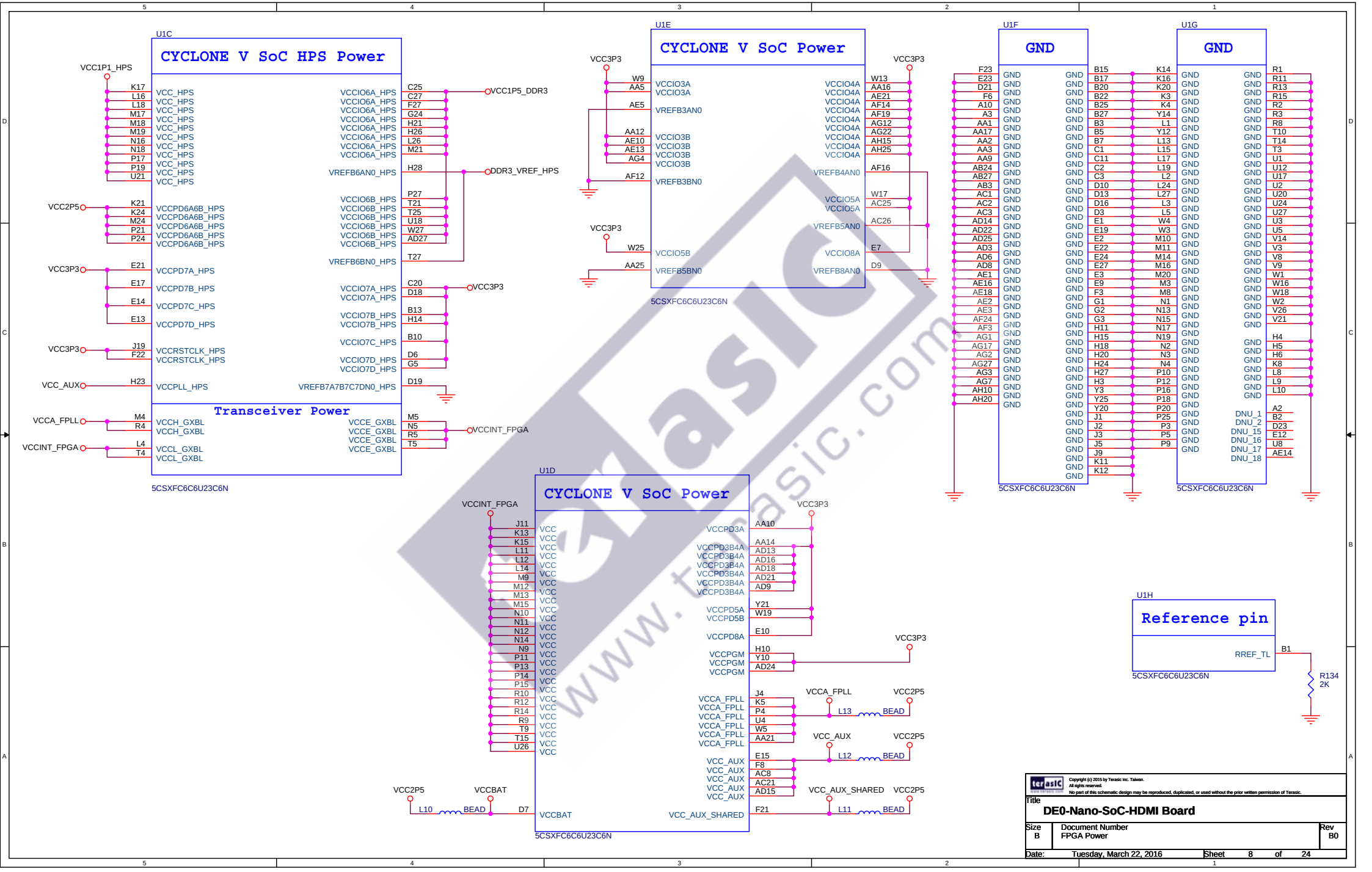
Title: DE0-Nano-SoC-HDMI Board
Size: B
Document Number: FPGA Configuration and EPCS
Rev: B0
Date: Wednesday, March 23, 2016
Sheet 7 of 24


U1C
CYCLONE V SoC HPS Power
VCC1P1_HPS
VCC_HPS
VCCIO6A_HPS
VCCIO6B_HPS
VCCPD6A6B_HPS
VCC2P5
VCCPD7A_HPS
VCCPD7B_HPS
VCCPD7C_HPS
VCCPD7D_HPS
VCC3P3
VCCRSTCLK_HPS
VCC_AUX
VCCPLL_HPS
VCCIO7A_HPS
VCCIO7B_HPS
VCCIO7C_HPS
VCCIO7D_HPS
VREFB6AN0_HPS
VREFB6BN0_HPS
VREFB7A7B7C7DN0_HPS
DDR3_VREF_HPS
VCC1P5_DDR3
Transceiver Power
VCCH_GXBL
VCCL_GXBL
VCCE_GXBL
VCCINT_FPGA
5CSXFC6C6U23C6N
U1E
CYCLONE V SoC Power
VCCIO3A
VCCIO3B
VREFB3AN0
VREFB3BN0
VCCIO5B
VREFB5BN0
VCCIO4A
VREFB4AN0
VCCIO5A
VREFB5AN0
VCCIO8A
VREFB8AN0
U1F
GND
U1G
U1D
CYCLONE V SoC Power
VCC
VCCPD3A
VCCPD3B4A
VCCPD5A
VCCPD5B
VCCPD8A
VCCPGM
VCCA_FPLL
VCC_AUX
VCC_AUX_SHARED
VCCBAT
VCCA_FPLL
VCC2P5
L13
BEAD
VCC_AUX
L12
VCC_AUX_SHARED
L11
VCC2P5
VCCBAT
L10
D7
U1H
Reference pin
RREF_TL
B1
R134
2K
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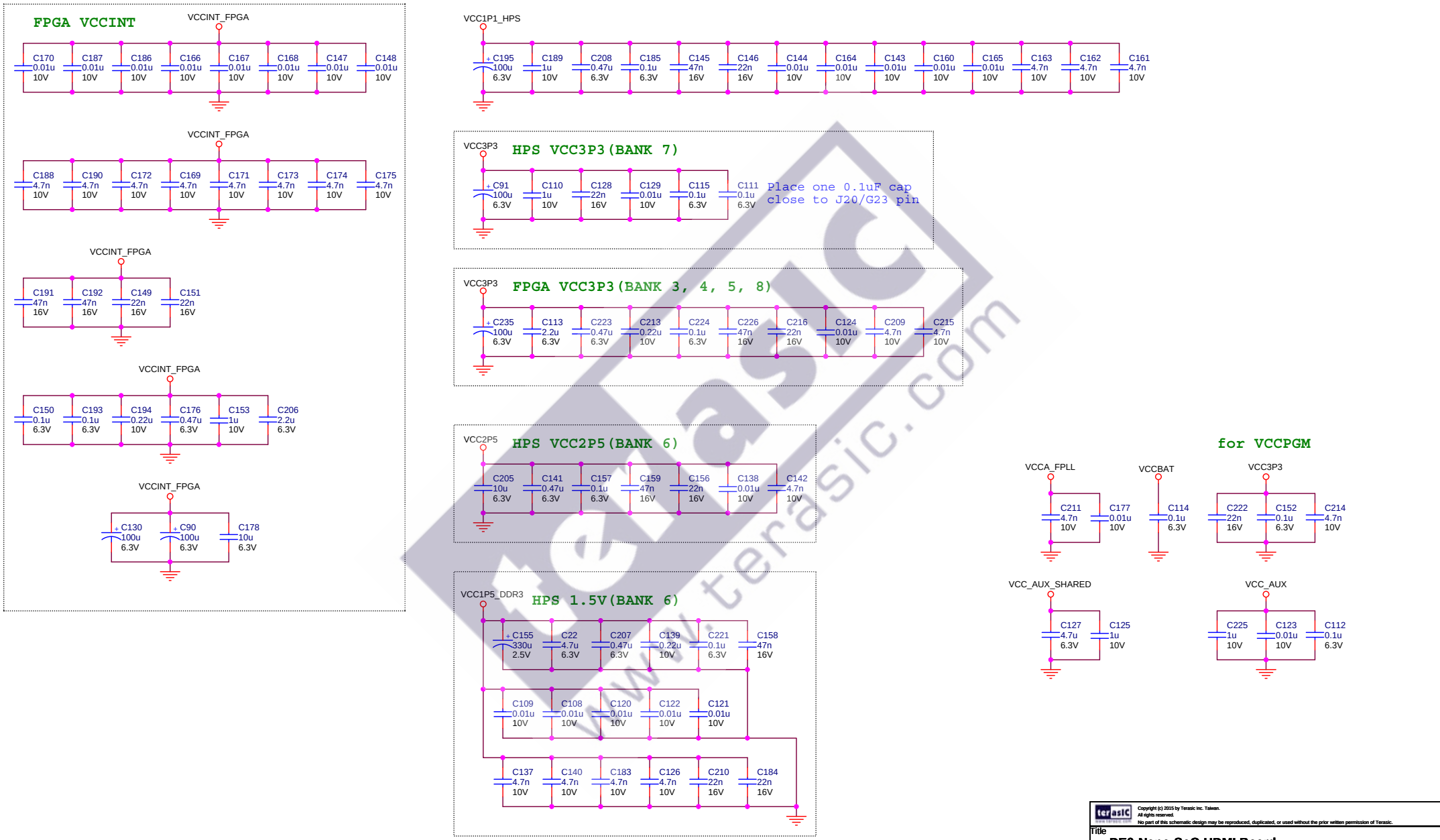
Title
DE0-Nano-SoC-HDMI Board
Size
B
Document Number
FPGA Power
Rev
B0
Date:
Tuesday, March 22, 2016
Sheet
8
of
24



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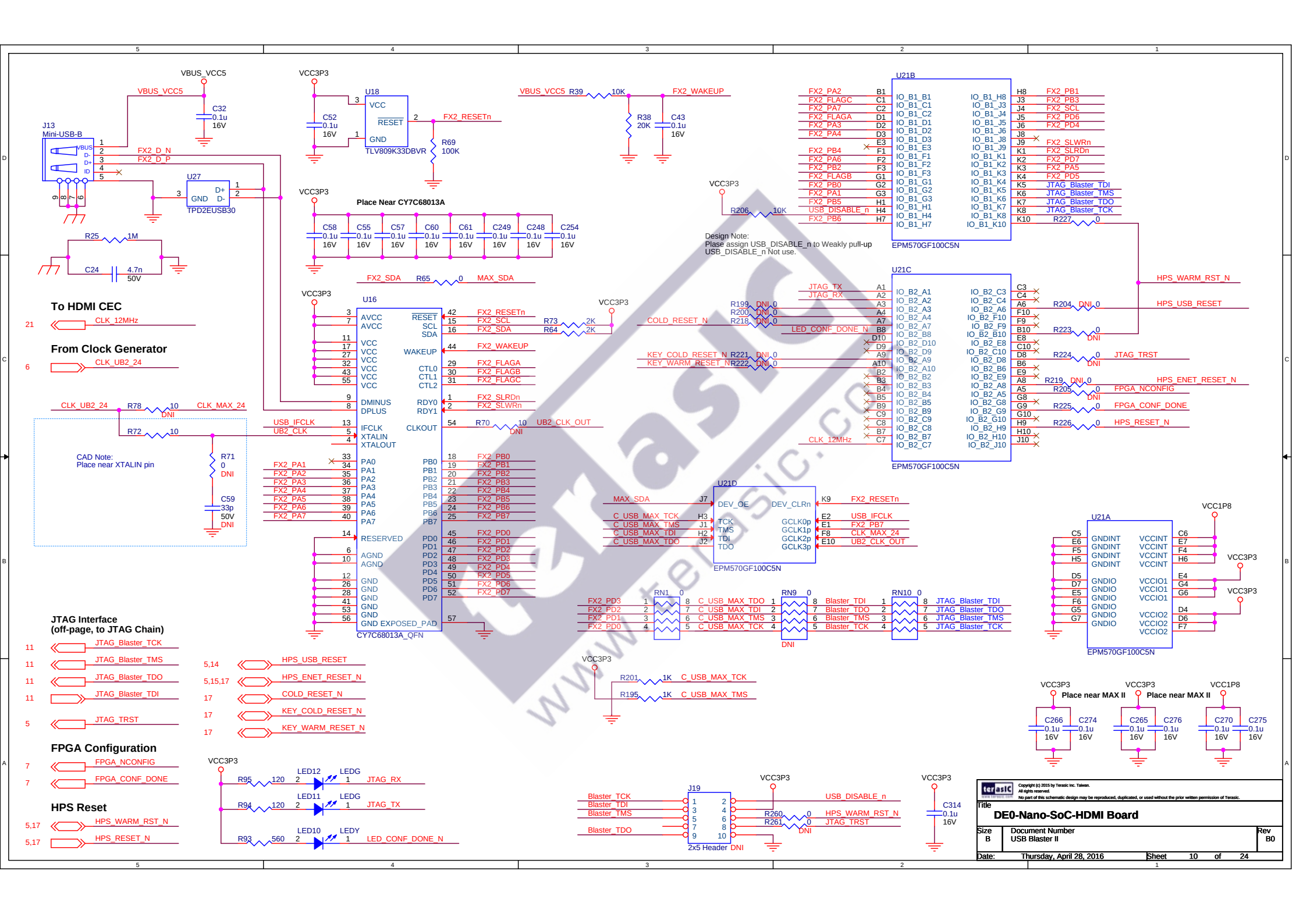
Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	FPGA Decoupling	B0

Date: Tuesday, March 22, 2016 Sheet 9 of 24


VBUS_VCC5
C32 0.1u 16V
J13 Mini-USB-B
FX2_D_N
FX2_D_P
U27 TPD2EUSB30
R25 1M
C24 4.7n 50V
VCC3P3
U18 TLV809K33DBVR
C52 0.1u 16V
R69 100K
FX2_RESETn
VBUS_VCC5 R39 10K
R38 20K
C43 0.1u 16V
FX2_WAKEUP
Place Near CY7C68013A
C58 C55 C57 C60 C61 C249 C248 C254 0.1u 16V
FX2_SDA R65 0 MAX_SDA
U16 CY7C68013A_QFN
To HDMI CEC
CLK_12MHz
From Clock Generator
CLK_UB2_24
CLK_UB2_24 R78 10 DNI CLK_MAX_24
R72 10
R71 0 DNI
C59 33p 50V DNI
CAD Note: Place near XTALIN pin
USB_IFCLK
UB2_CLK
R70 10 DNI UB2_CLK_OUT
FX2_PA1 FX2_PA2 FX2_PA3 FX2_PA4 FX2_PA5 FX2_PA6 FX2_PA7
FX2_PB0 FX2_PB1 FX2_PB2 FX2_PB3 FX2_PB4 FX2_PB5 FX2_PB6 FX2_PB7
FX2_PD0 FX2_PD1 FX2_PD2 FX2_PD3 FX2_PD4 FX2_PD5 FX2_PD6 FX2_PD7
FX2_RESETn FX2_SCL FX2_SDA FX2_WAKEUP FX2_FLAGA FX2_FLAGB FX2_FLAGC FX2_SLRDn FX2_SLWRn
R73 2K R64 2K
JTAG Interface (off-page, to JTAG Chain)
JTAG_Blaster_TCK
JTAG_Blaster_TMS
JTAG_Blaster_TDO
JTAG_Blaster_TDI
JTAG_TRST
FPGA Configuration
FPGA_NCONFIG
FPGA_CONF_DONE
HPS Reset
HPS_WARM_RST_N
HPS_RESET_N
HPS_USB_RESET
HPS_ENET_RESET_N
COLD_RESET_N
KEY_COLD_RESET_N
KEY_WARM_RESET_N
R95 120 LED12 LEDG JTAG_RX
R94 120 LED11 LEDG JTAG_TX
R93 560 LED10 LEDY LED_CONF_DONE_N
U21B EPM570GF100C5N
R206 10K
Design Note: Plase assign USB_DISABLE_n to Weakly pull-up USB_DISABLE_n Not use.
U21C EPM570GF100C5N
R199 R200 R218 DNI 0
R221 R222 DNI 0
R204 R223 R224 R205 R225 R226 0 DNI
R219 DNI 0
HPS_WARM_RST_N
HPS_USB_RESET
JTAG_TRST
HPS_ENET_RESET_N
FPGA_NCONFIG
FPGA_CONF_DONE
HPS_RESET_N
U21D EPM570GF100C5N
MAX_SDA
C_USB_MAX_TCK
C_USB_MAX_TMS
C_USB_MAX_TDI
C_USB_MAX_TDO
USB_IFCLK
FX2_PB7
CLK_MAX_24
UB2_CLK_OUT
RN1 RN9 RN10 0 DNI
C_USB_MAX_TDO C_USB_MAX_TDI C_USB_MAX_TMS C_USB_MAX_TCK
Blaster_TDI Blaster_TDO Blaster_TMS Blaster_TCK
JTAG_Blaster_TDI JTAG_Blaster_TDO JTAG_Blaster_TMS JTAG_Blaster_TCK
U21A EPM570GF100C5N
VCC1P8
VCC3P3
R201 1K C_USB_MAX_TCK
R195 1K C_USB_MAX_TMS
Place near MAX II
C266 C274 C265 C276 C270 C275 0.1u 16V
J19 2x5 Header DNI
Blaster_TCK Blaster_TDI Blaster_TMS Blaster_TDO
USB_DISABLE_n
R260 R261 0 DNI
HPS_WARM_RST_N
JTAG_TRST
C314 0.1u 16V
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Title
DE0-Nano-SoC-HDMI Board
Size B
Document Number USB Blaster II
Rev B0
Date: Thursday, April 28, 2016
Sheet 10 of 24

USB Blaster

10 JTAG_Blaster_TCK
10 JTAG_Blaster_TMS
10 JTAG_Blaster_TDO
10 JTAG_Blaster_TDI

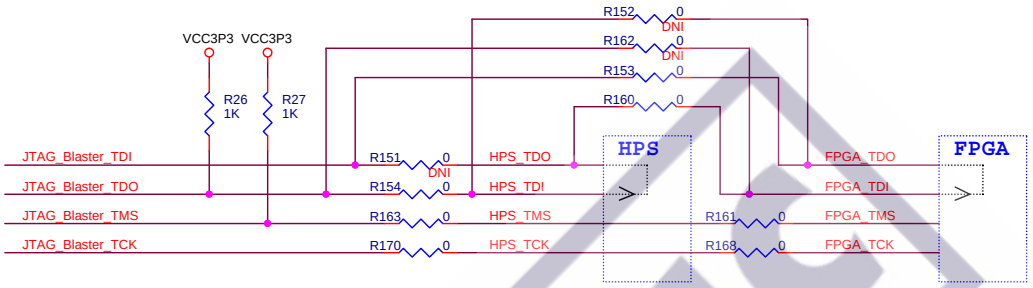
FPGA JTAG INTERFACE

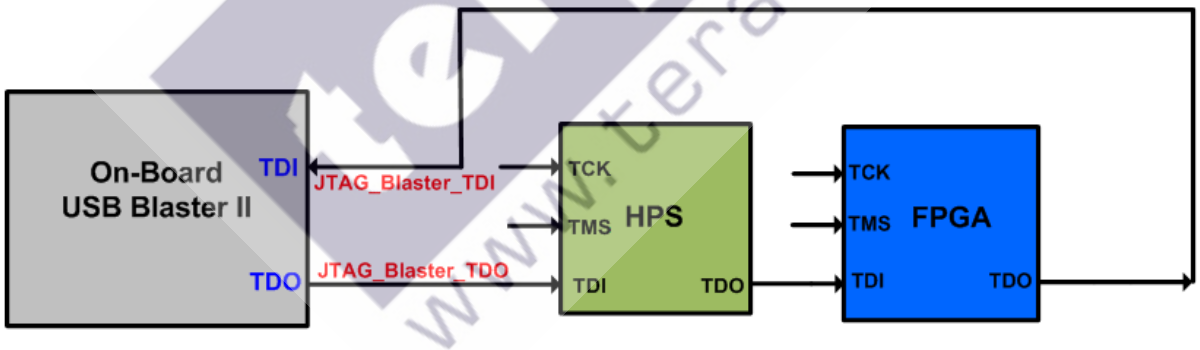
7 FPGA_TCK
7 FPGA_TMS
7 FPGA_TDI
7 FPGA_TDO

HPS JTAG INTERFACE

5 HPS_TCK
5 HPS_TMS
5 HPS_TDI
5 HPS_TDO

JTAG Chain





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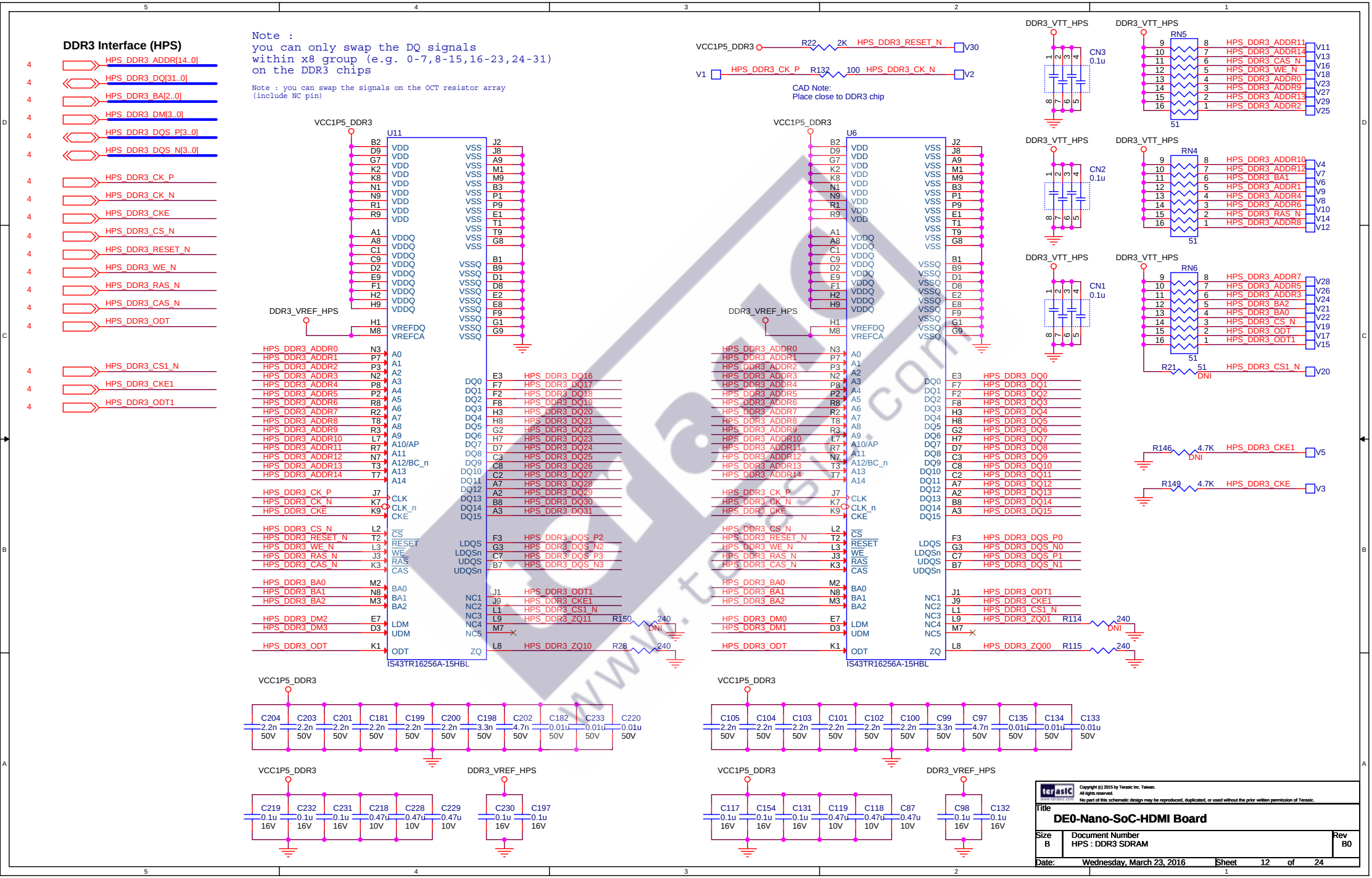
Title: **DE0-Nano-SoC-HDMI Board**

Size	Document Number	Rev
B	JTAG Chain	B0

Date: Thursday, March 03, 2016 Sheet 11 of 24


DDR3 Interface (HPS)
HPS_DDR3_ADDR[14..0]
HPS_DDR3_DQ[31..0]
HPS_DDR3_BA[2..0]
HPS_DDR3_DM[3..0]
HPS_DDR3_DQS_P[3..0]
HPS_DDR3_DQS_N[3..0]
HPS_DDR3_CK_P
HPS_DDR3_CK_N
HPS_DDR3_CKE
HPS_DDR3_CS_N
HPS_DDR3_RESET_N
HPS_DDR3_WE_N
HPS_DDR3_RAS_N
HPS_DDR3_CAS_N
HPS_DDR3_ODT
HPS_DDR3_CS1_N
HPS_DDR3_CKE1
HPS_DDR3_ODT1
Note :
you can only swap the DQ signals
within x8 group (e.g. 0-7,8-15,16-23,24-31)
on the DDR3 chips
Note : you can swap the signals on the OCT resistor array
(include NC pin)
VCC1P5_DDR3
U11
IS43TR16256A-15HBL
DDR3_VREF_HPS
U6
IS43TR16256A-15HBL
CAD Note:
Place close to DDR3 chip
DDR3_VTT_HPS
CN3 0.1u
CN2 0.1u
CN1 0.1u
RN5
RN4
RN6
R22 2K HPS_DDR3_RESET_N V30
V1 HPS_DDR3_CK_P R132 100 HPS_DDR3_CK_N V2
R21 51 DNI HPS_DDR3_CS1_N V20
R146 4.7K DNI HPS_DDR3_CKE1 V5
R149 4.7K HPS_DDR3_CKE V3
R150 240 DNI
R28 240
R114 240 DNI
R115 240
C204 2.2n 50V
C203 2.2n 50V
C201 2.2n 50V
C181 2.2n 50V
C199 2.2n 50V
C200 2.2n 50V
C198 3.3n 50V
C202 4.7n 50V
C182 0.01u 50V
C233 0.01u 50V
C220 0.01u 50V
C105 2.2n 50V
C104 2.2n 50V
C103 2.2n 50V
C101 2.2n 50V
C102 2.2n 50V
C100 2.2n 50V
C99 3.3n 50V
C97 4.7n 50V
C135 0.01u 50V
C134 0.01u 50V
C133 0.01u 50V
C219 0.1u 16V
C232 0.1u 16V
C231 0.1u 16V
C218 0.47u 10V
C228 0.47u 10V
C229 0.47u 10V
C230 0.1u 16V
C197 0.1u 16V
C117 0.1u 16V
C154 0.1u 16V
C131 0.1u 16V
C119 0.47u 10V
C118 0.47u 10V
C87 0.47u 10V
C98 0.1u 16V
C132 0.1u 16V
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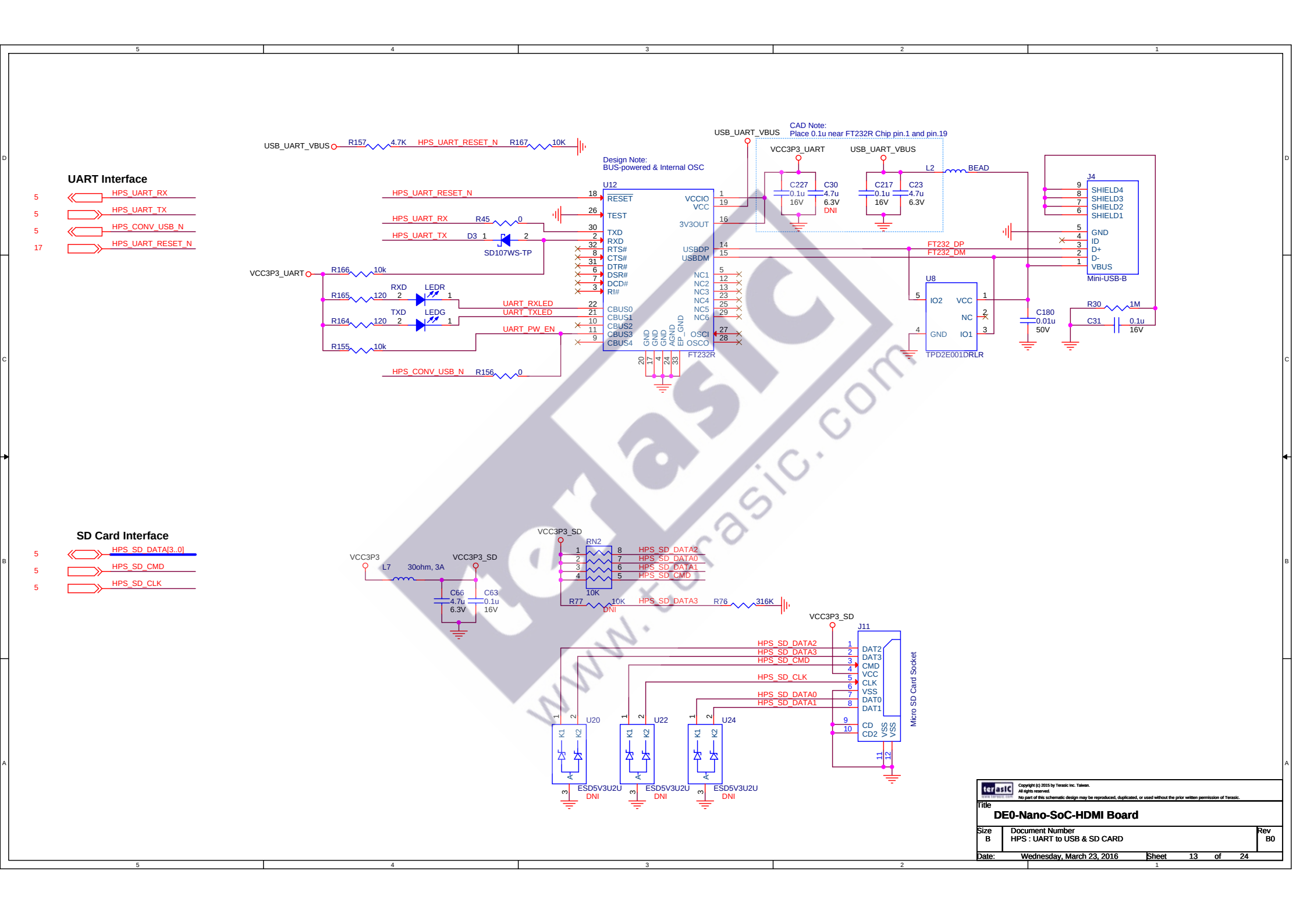
Title
DE0-Nano-SoC-HDMI Board
Size B
Document Number
HPS : DDR3 SDRAM
Rev B0
Date: Wednesday, March 23, 2016
Sheet 12 of 24


UART Interface
HPS_UART_RX
HPS_UART_TX
HPS_CONV_USB_N
HPS_UART_RESET_N
USB_UART_VBUS
R157 4.7K HPS_UART_RESET_N R167 10K
CAD Note:
Place 0.1u near FT232R Chip pin.1 and pin.19
Design Note:
BUS-powered & Internal OSC
U12
VCC3P3_UART
C227 0.1u 16V
C30 4.7u 6.3V DNI
C217 0.1u 16V
C23 4.7u 6.3V
L2 BEAD
J4
SHIELD4
SHIELD3
SHIELD2
SHIELD1
GND
ID
D+
D-
VBUS
Mini-USB-B
FT232_DP
FT232_DM
HPS_UART_RESET_N
HPS_UART_RX
R45 0
HPS_UART_TX
D3
SD107WS-TP
VCC3P3_UART
R166 10k
R165 120
R164 120
RXD
TXD
LEDR
LEDG
R155 10k
UART_RXLED
UART_TXLED
UART_PW_EN
HPS_CONV_USB_N
R156 0
RESET
TEST
TXD
RXD
RTS#
CTS#
DTR#
DSR#
DCD#
RI#
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
VCCIO
VCC
3V3OUT
USBDP
USBDM
NC1
NC2
NC3
NC4
NC5
NC6
OSCI
OSCO
GND
AGND
EP_GND
FT232R
U8
IO2
VCC
NC
GND
IO1
TPD2E001DRLR
C180 0.01u 50V
R30 1M
C31 0.1u 16V
SD Card Interface
HPS_SD_DATA[3..0]
HPS_SD_CMD
HPS_SD_CLK
VCC3P3
L7 30ohm, 3A
VCC3P3_SD
C66 4.7u 6.3V
C63 0.1u 16V
RN2
HPS_SD_DATA2
HPS_SD_DATA0
HPS_SD_DATA1
HPS_SD_CMD
10K
R77 10K DNI
HPS_SD_DATA3
R76 316K
J11
DAT2
DAT3
CMD
VCC
CLK
VSS
DAT0
DAT1
CD
CD2
VSS
Micro SD Card Socket
U20
U22
U24
K1
K2
A
ESD5V3U2U DNI
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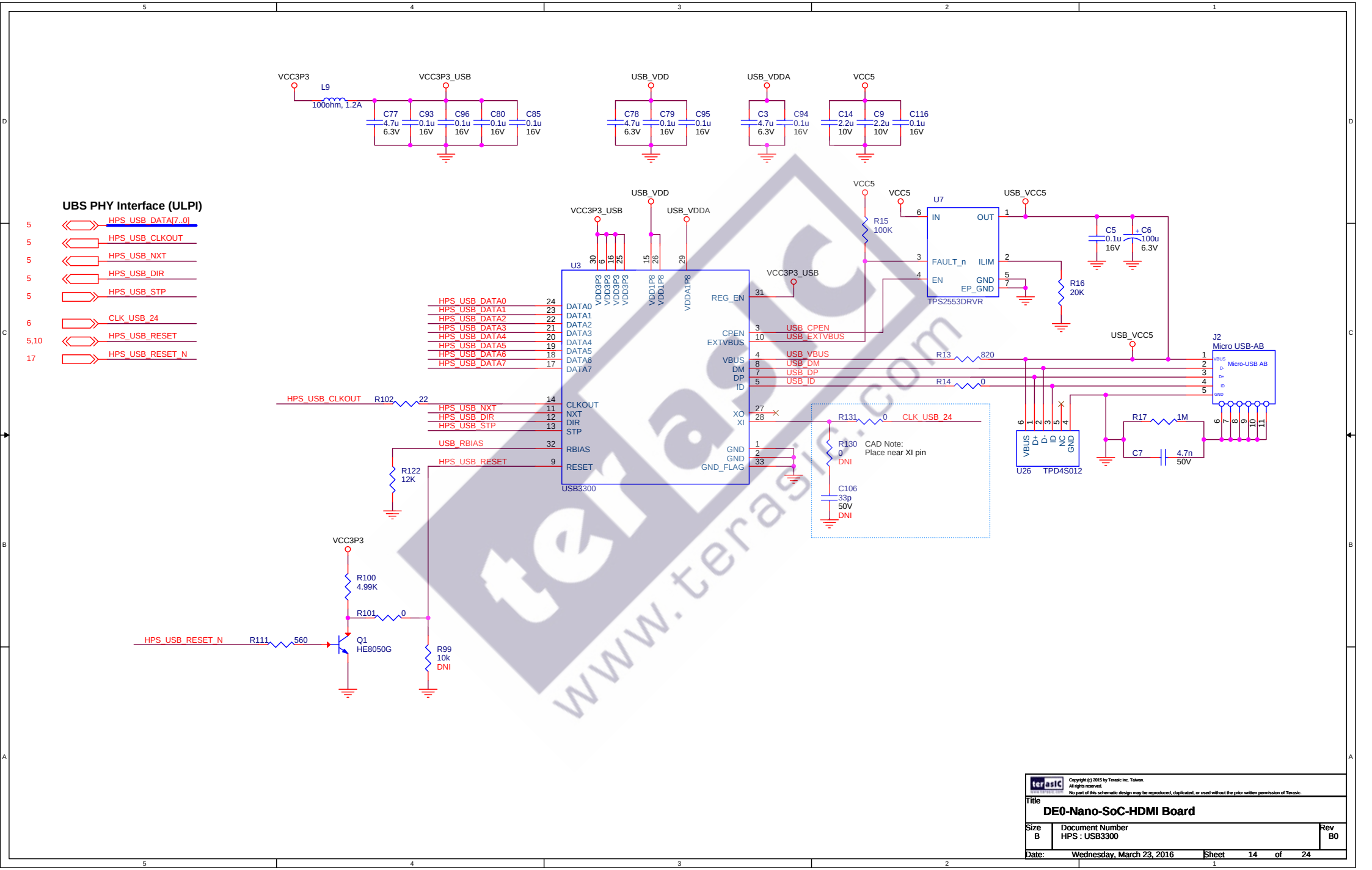
Title
DE0-Nano-SoC-HDMI Board
Size B
Document Number
HPS : UART to USB & SD CARD
Rev B0
Date: Wednesday, March 23, 2016
Sheet 13 of 24



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Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	HPS : USB3300	B0

Date: Wednesday, March 23, 2016 Sheet 14 of 24

Ethernet PHY Interface (RGMII)

HPS_ENET_TX_DATA[3..0]
HPS_ENET_GTX_CLK
HPS_ENET_TX_EN
HPS_ENET_RX_DATA[3..0]
HPS_ENET_RX_CLK
HPS_ENET_RX_DV
HPS_ENET_INT_N
HPS_ENET_MDC
HPS_ENET_MDIO
HPS_ENET_RESET_N
CLK_ENET_25

U17 — KSZ9031RNX

ENET_PLL, ENET_VCCA, ENET_DVDDL, ENET_AVDD, ENET_DVDDH
AVDDL_PLL, AVDDL, DVDDL, AVDDH, DVDDH, LDO_O

GTX_CLK, TX_EN, TXD0, TXD1, TXD2, TXD3
RX_CLK/PHYAD2, RX_DV/CLK125_EN
RXD0/MODE0, RXD1/MODE1, RXD2/MODE2, RXD3/MODE3
CLK125_NDO/LED_MODE, INT_N, RESET_N
MDC, MDIO
VSS, VSS_PS, PADDLE

TXRXP_A, TXRXM_A, TXRXP_B, TXRXM_B, TXRXP_C, TXRXM_C, TXRXP_D, TXRXM_D
MDI_HPS_P0, MDI_HPS_N0, MDI_HPS_P1, MDI_HPS_N1, MDI_HPS_P2, MDI_HPS_N2, MDI_HPS_P3, MDI_HPS_N3
LED1/PHYAD0, LED2/PHYAD1
ISET — R84 12.1K
XI — R82 0 CLK_ENET_25
XO

R83 0 DNI
CAD Note: Place near XI pin
C64 33p 50V DNI

J10 — 8207S-810X4372
GND1, GND2, SHIELD_1, SHIELD_2
LEDG+, LEDG-, LEDY+, LEDY-
R46 10, C47 0.01u 50V
R88 220, R43 220
LED2_DUAL_2, LED2_DUAL_1
VCC3P3

VCC3P3
R202 4.7K HPS_ENET_INT_N
R74 4.7K HPS_ENET_MDC
R203 4.7K HPS_ENET_MDIO
R81 4.7K HPS_ENET_RESET_N

C65 10n 50V DNI — R86 49.9 DNI MDI_HPS_P0 — R85 49.9 DNI MDI_HPS_N0
C62 10n 50V DNI — R75 49.9 DNI MDI_HPS_P1 — R68 49.9 DNI MDI_HPS_N1
C56 10n 50V DNI — R63 49.9 DNI MDI_HPS_P2 — R62 49.9 DNI MDI_HPS_N2
C51 10n 50V DNI — R53 49.9 DNI MDI_HPS_P3 — R52 49.9 DNI MDI_HPS_N3

PHY Address is 00001

ENET_DVDDH
R173 4.7K LED2_DUAL_1 — R181 1K DNI
R220 4.7K DNI LED2_DUAL_2 — R228 1K DNI
R67 4.7K DNI HPS_ENET_RX_CLK — R197 1K DNI

VCC3P3
R80 4.7K DNI CLK125_NDO_LED_MODE — R79 4.7K DNI
R66 4.7K DNI HPS_ENET_RX_DV — R196 4.7K DNI
R41 4.7K DNI HPS_ENET_GTX_CLK — R42 4.7K DNI
R61 4.7K HPS_ENET_RX_DATA0 — R185 4.7K DNI
R60 4.7K HPS_ENET_RX_DATA1 — R184 4.7K DNI
R51 4.7K HPS_ENET_RX_DATA2 — R183 4.7K DNI
R50 4.7K HPS_ENET_RX_DATA3 — R182 4.7K DNI

VCC3P3 — L18 100ohm, 1.2A — ENET_AVDD
C255 0.22u 50V, C239 1u 10V, C267 10u 6.3V

VCC3P3 — L20 100ohm, 1.2A — ENET_DVDDH
C258 0.22u 50V, C259 1u 10V, C269 10u 6.3V

VCC1P2 — L15 100ohm, 1.2A — ENET_VCCA
C251 0.22u 50V, C250 1u 10V, C240 10u 6.3V

VCC1P2 — L19 100ohm, 1.2A — ENET_PLL
C257 0.22u 50V, C256 1u 10V, C268 10u 6.3V

VCC1P2 — L14 100ohm, 1.2A — ENET_DVDDL
C241 0.22u 50V, C243 1u 10V, C242 10u 6.3V

ENET_AVDD — Q5 AO3415 DNI — VCC1P2
HPS_ENET_LDO_O

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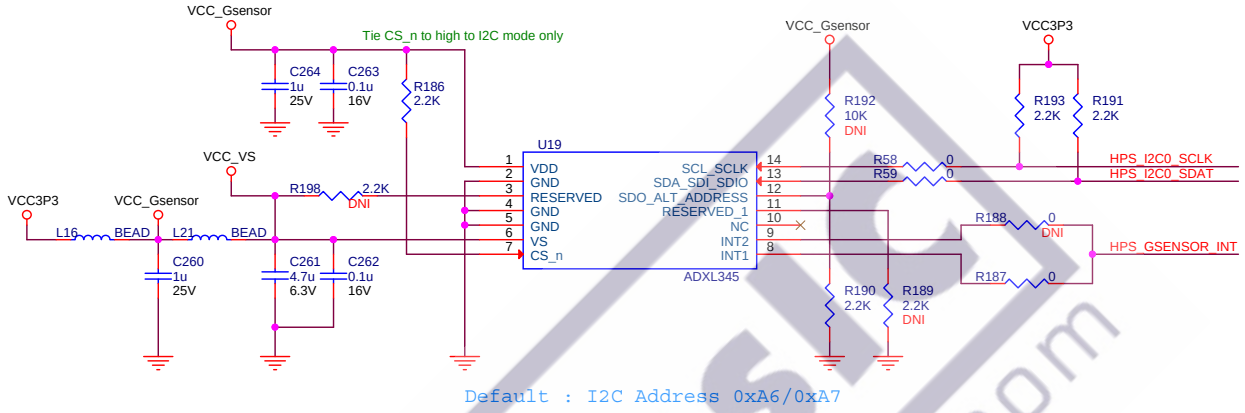
Title: DE0-Nano-SoC-HDMI Board
Size: B | Document Number: HPS : Gagabit Ethernet | Rev: B0
Date: Tuesday, March 22, 2016 | Sheet 15 of 24

Digital Accelerometer



Default : I2C Address 0xA6/0xA7

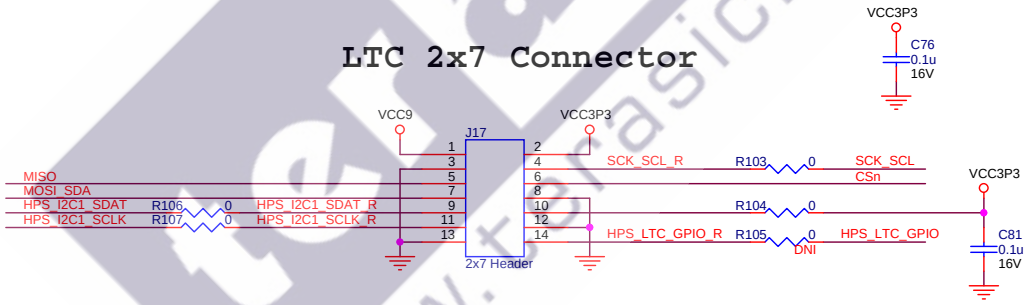
Accelerometer Interface

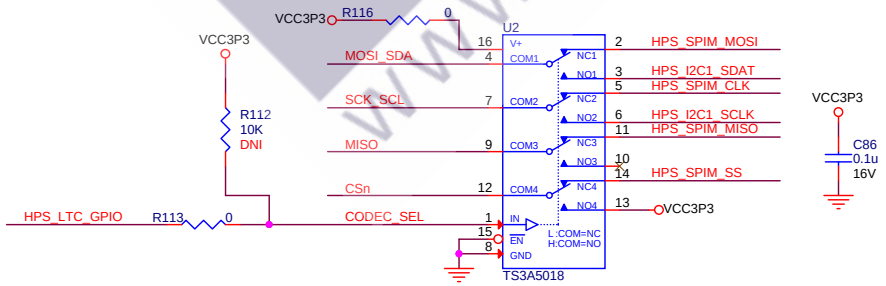
- HPS_I2C0_SDAT
- HPS_I2C0_SCLK
- HPS_GSENSOR_INT

LTC Interface

- HPS_I2C1_SDAT
- HPS_I2C1_SCLK
- HPS_SPIM_MOSI
- HPS_SPIM_MISO
- HPS_SPIM_CLK
- HPS_SPIM_SS
- HPS_LTC_GPIO

LTC 2x7 Connector





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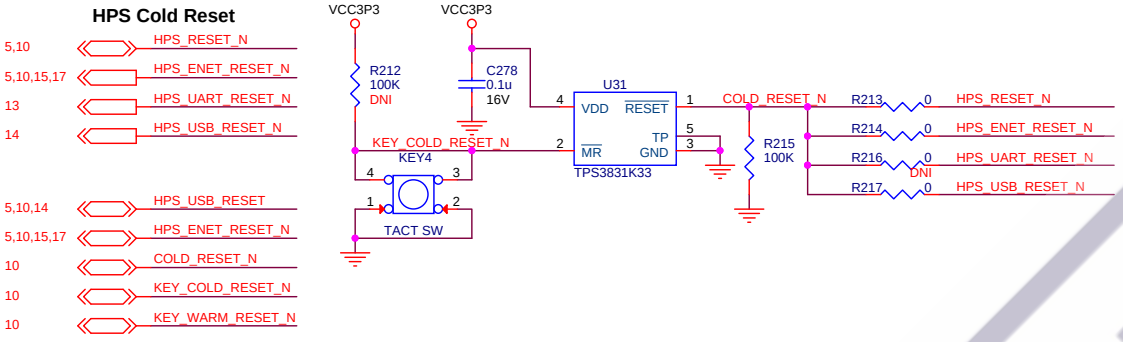
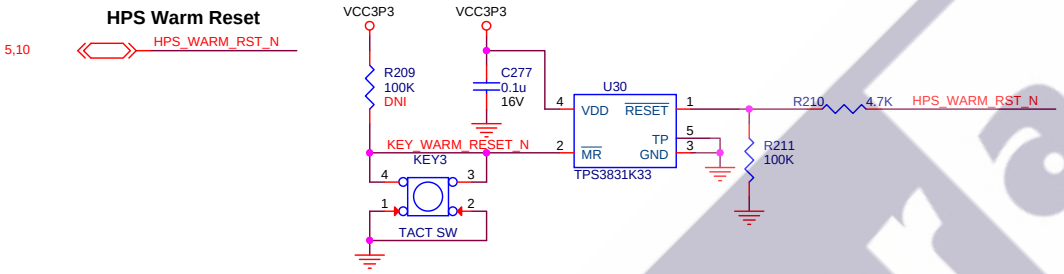
Title	DE0-Nano-SoC-HDMI Board	
Size B	Document Number HPS : Accelerometer, LTC Connector	Rev B0
Date: Wednesday, March 23, 2016	Sheet 16 of 24	

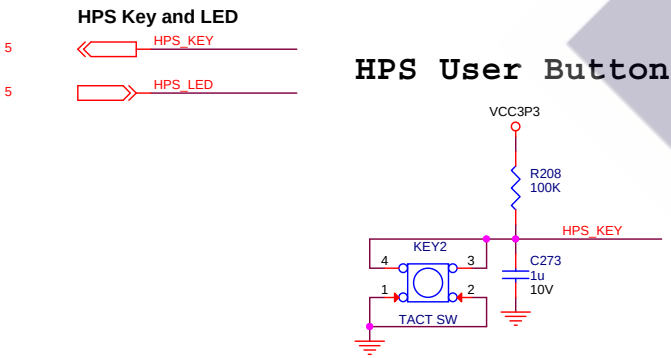
HPS Cold Reset



HPS Warm Reset



HPS User Button



HPS User LED

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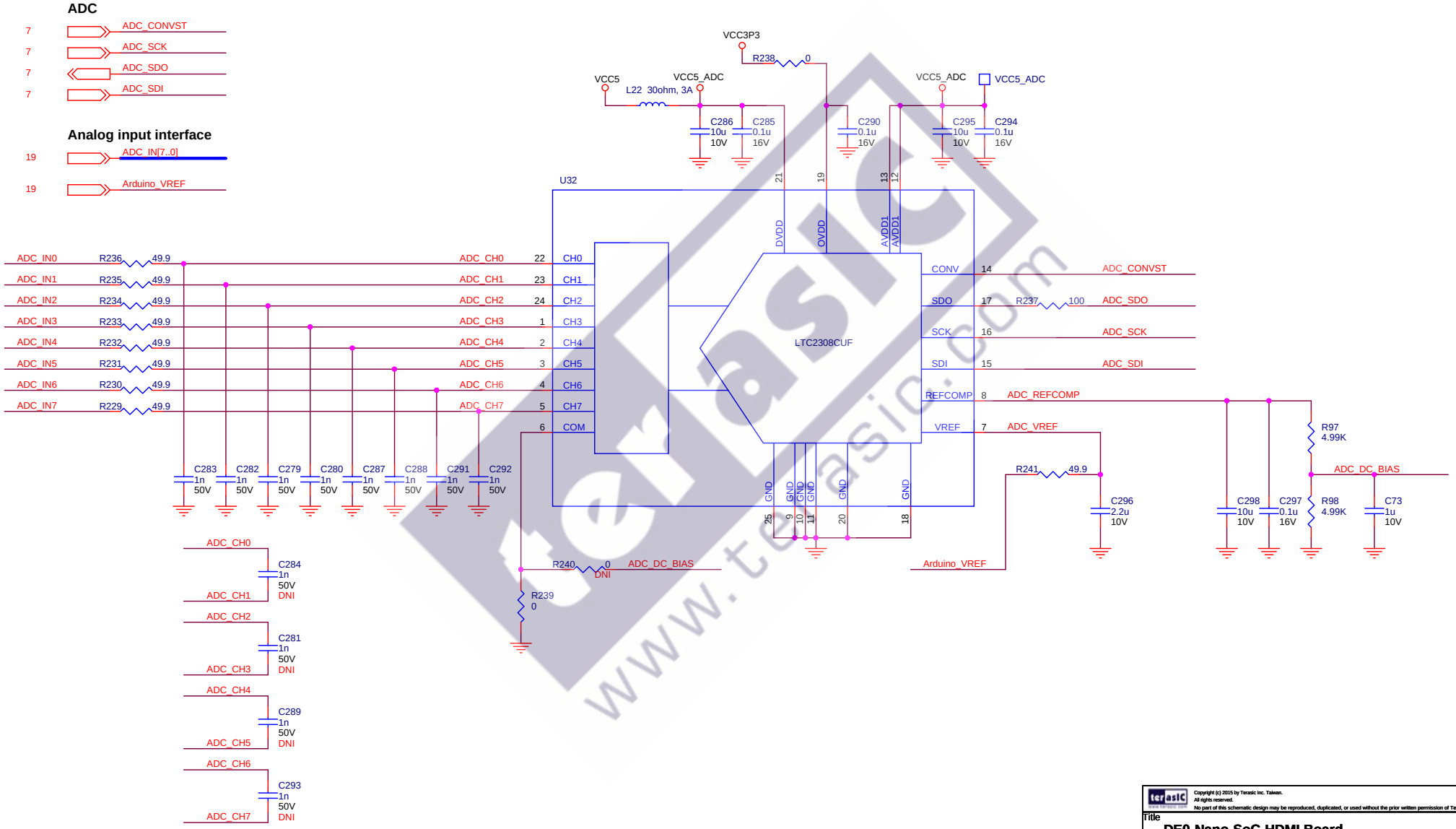
Title: DE0-Nano-SoC-HDMI Board

Size: B | Document Number: HPS : BUTTON and LED | Rev: B0

Date: Wednesday, March 23, 2016 | Sheet 17 of 24



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Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	FPGA : ADC1 - LTC2308 for ADC Header Analog input	B0

Date: Wednesday, March 23, 2016 Sheet 18 of 24

GPIO

3,6,7 GPIO_0_D[35..0]

3,6 GPIO_1_D[35..0]

Arduino Digital Interface

3 Arduino_IO[15..0]

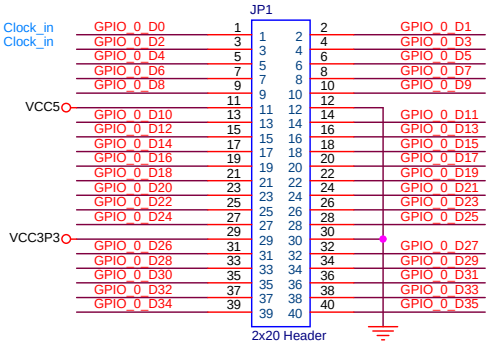
3 Arduino_Reset_n

Analog input interface

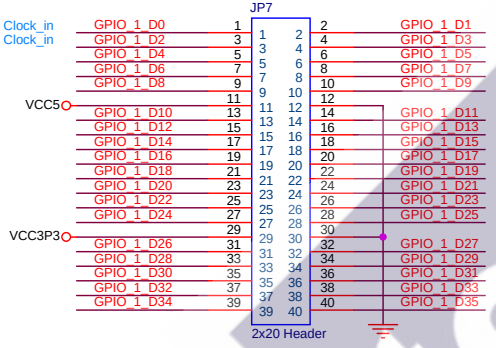
18 ADC_IN[7..0]

18 Arduino_VREF

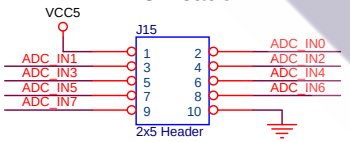
GPIO 0 Header

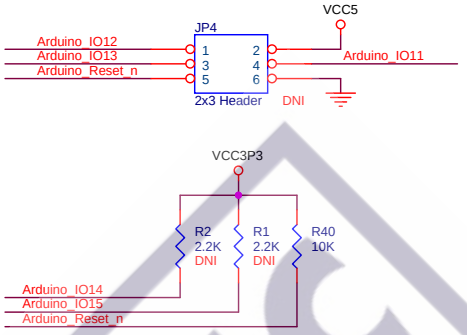


GPIO 1 Header

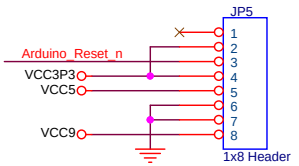


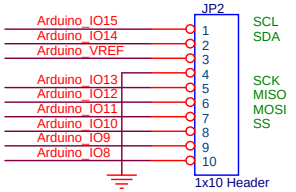
ADC Header

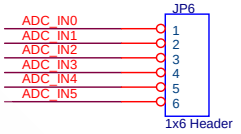


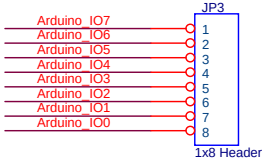


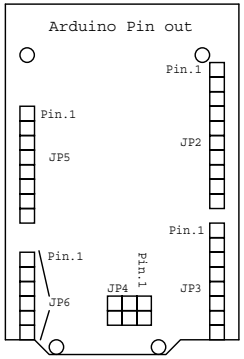
Arduino UNO Rev3











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Title: **DE0-Nano-SoC-HDMI Board**

Size	Document Number	Rev
B	FPGA : GPIO, ADC & Arduino Expansion Header	B0

Date: Tuesday, March 22, 2016 Sheet 19 of 24

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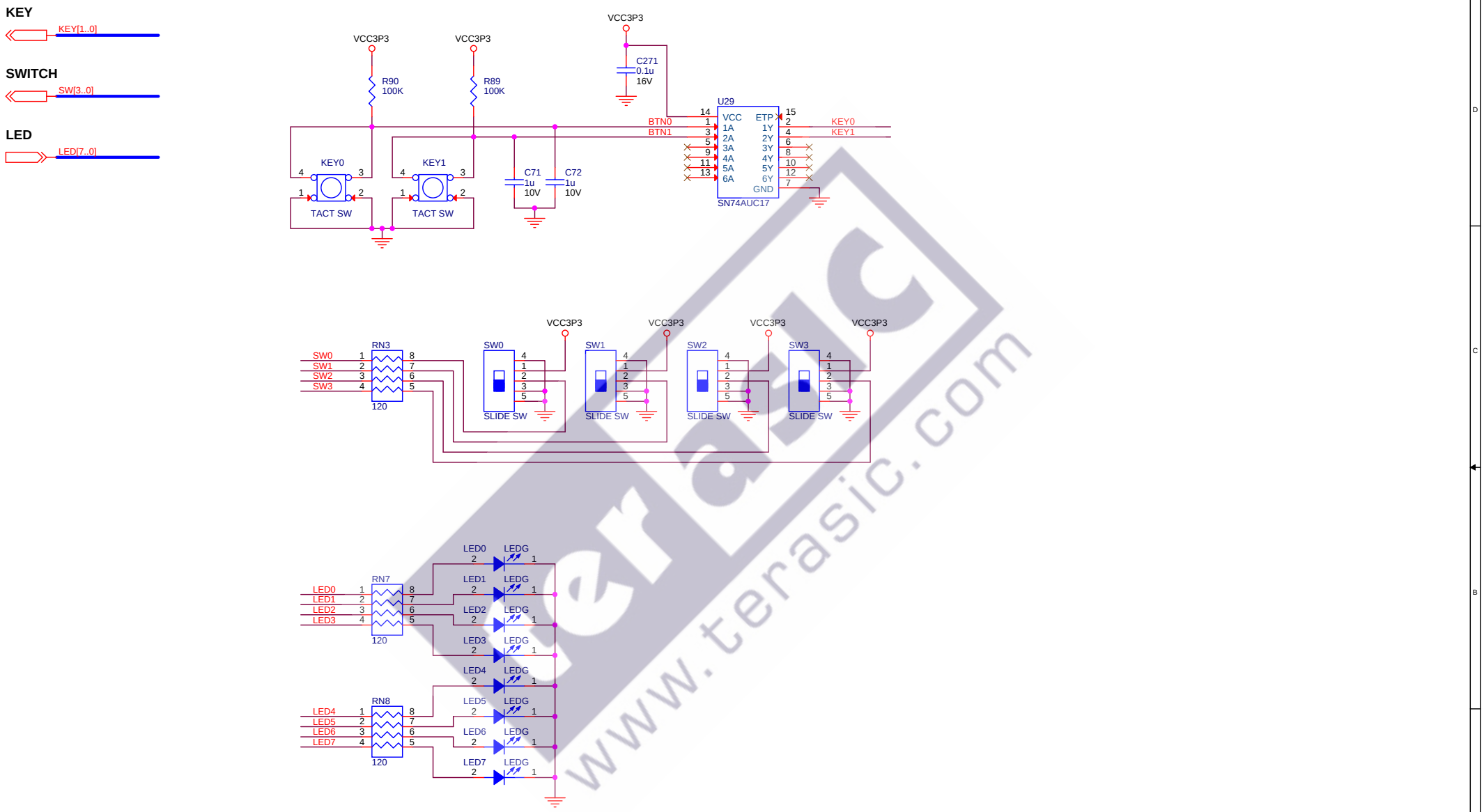

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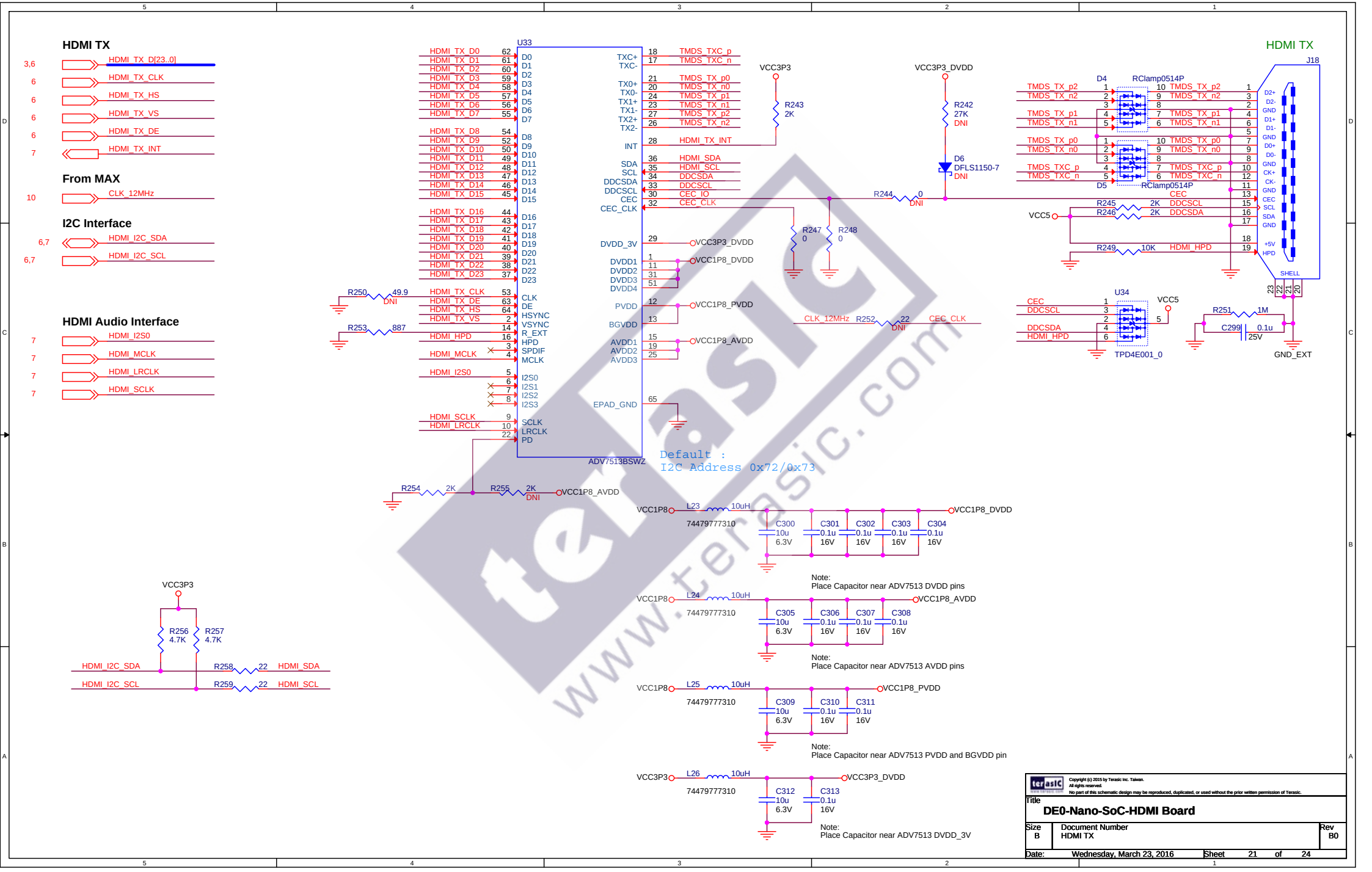
Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	FPGA : LED, KEY, SW	B0

Date: Wednesday, March 23, 2016 Sheet 20 of 24


HDMI TX
HDMI_TX_D[23..0]
HDMI_TX_CLK
HDMI_TX_HS
HDMI_TX_VS
HDMI_TX_DE
HDMI_TX_INT
From MAX
CLK_12MHz
I2C Interface
HDMI_I2C_SDA
HDMI_I2C_SCL
HDMI Audio Interface
HDMI_I2S0
HDMI_MCLK
HDMI_LRCLK
HDMI_SCLK
U33
ADV7513BSWZ
Default :
I2C Address 0x72/0x73
VCC3P3
VCC3P3_DVDD
VCC1P8_DVDD
VCC1P8_PVDD
VCC1P8_AVDD
VCC5
R243 2K
R242 27K DNI
D6 DFLS1150-7 DNI
R244 0 DNI
R247 0
R248 0
R250 49.9 DNI
R253 887
R254 2K
R255 2K DNI
R256 4.7K
R257 4.7K
R258 22
R259 22
R245 2K DDCSCL
R246 2K DDCSDA
R249 10K HDMI_HPD
R251 1M
C299 0.1u 25V
CLK_12MHz R252 22 DNI CEC_CLK
D4 RClamp0514P
D5 RClamp0514P
U34 TPD4E001_0
J18 HDMI TX
GND_EXT
L23 10uH 74479777310
C300 10u 6.3V
C301 0.1u 16V
C302 0.1u 16V
C303 0.1u 16V
C304 0.1u 16V
Note:
Place Capacitor near ADV7513 DVDD pins
L24 10uH 74479777310
C305 10u 6.3V
C306 0.1u 16V
C307 0.1u 16V
C308 0.1u 16V
Note:
Place Capacitor near ADV7513 AVDD pins
L25 10uH 74479777310
C309 10u 6.3V
C310 0.1u 16V
C311 0.1u 16V
Note:
Place Capacitor near ADV7513 PVDD and BGVDD pin
L26 10uH 74479777310
C312 10u 6.3V
C313 0.1u 16V
Note:
Place Capacitor near ADV7513 DVDD_3V
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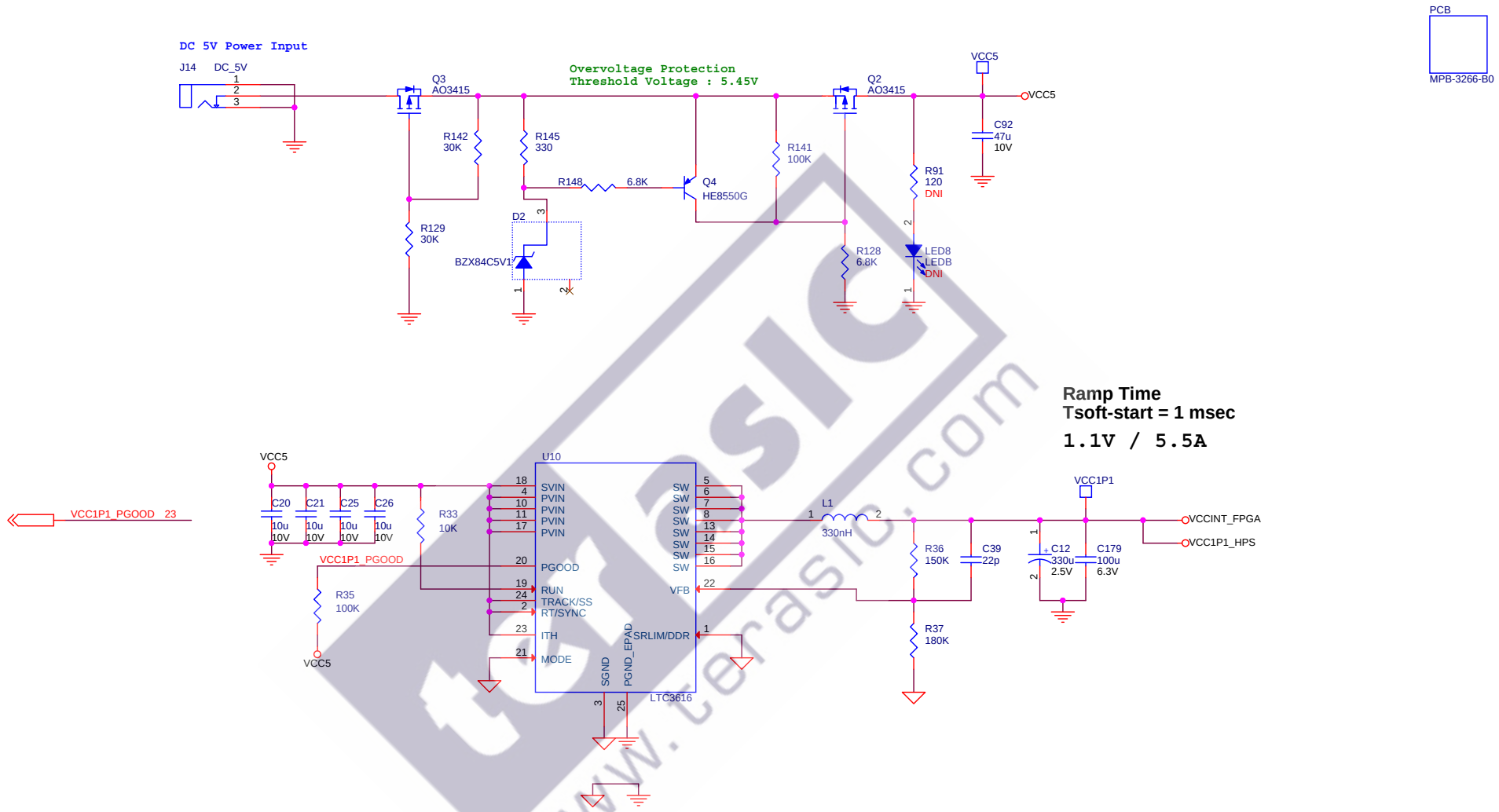
Title
DE0-Nano-SoC-HDMI Board
Size B
Document Number HDMI TX
Rev B0
Date: Wednesday, March 23, 2016
Sheet 21 of 24



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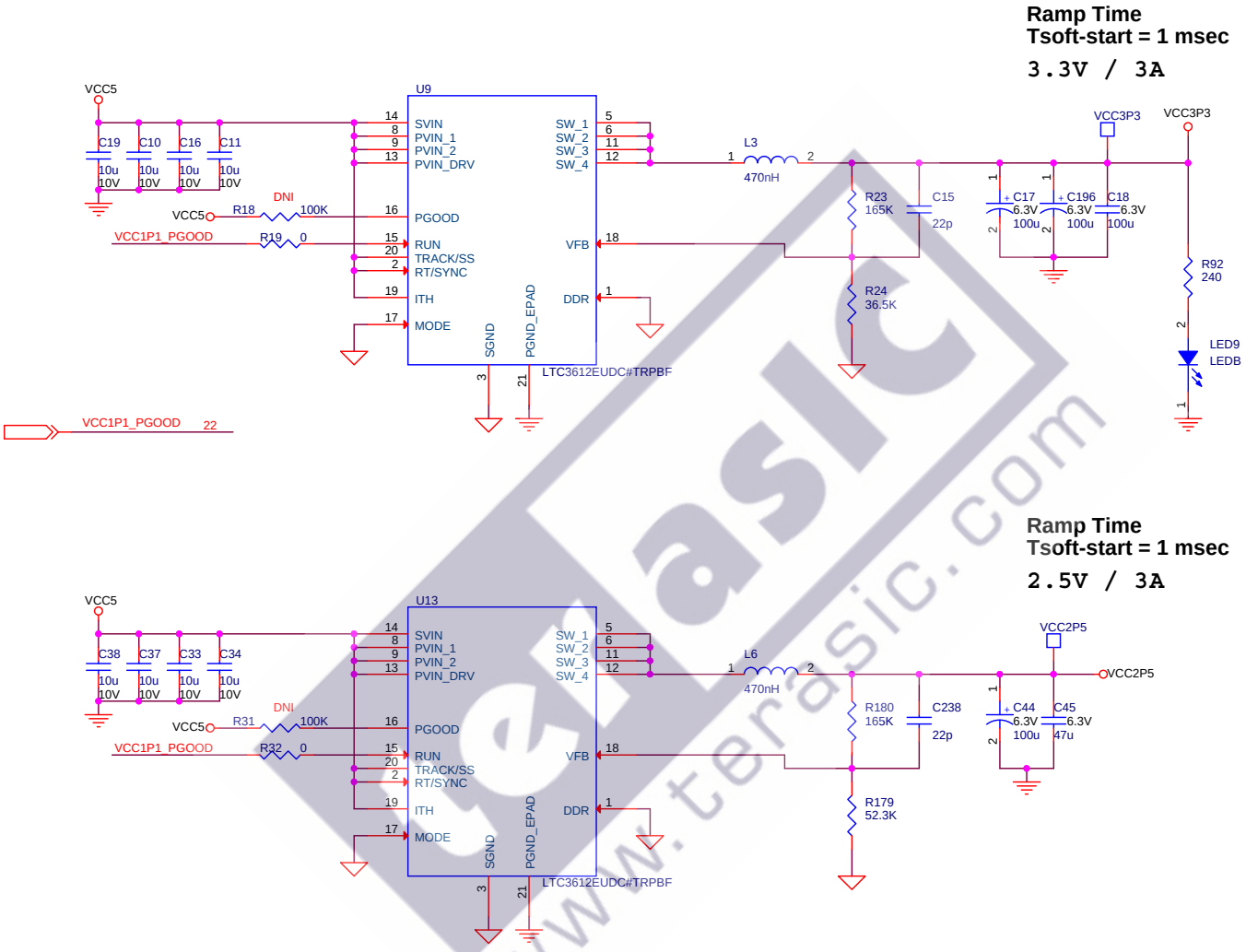
Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	Power - 1.1V, 5V	B0

Date: Thursday, March 31, 2016 Sheet 22 of 24



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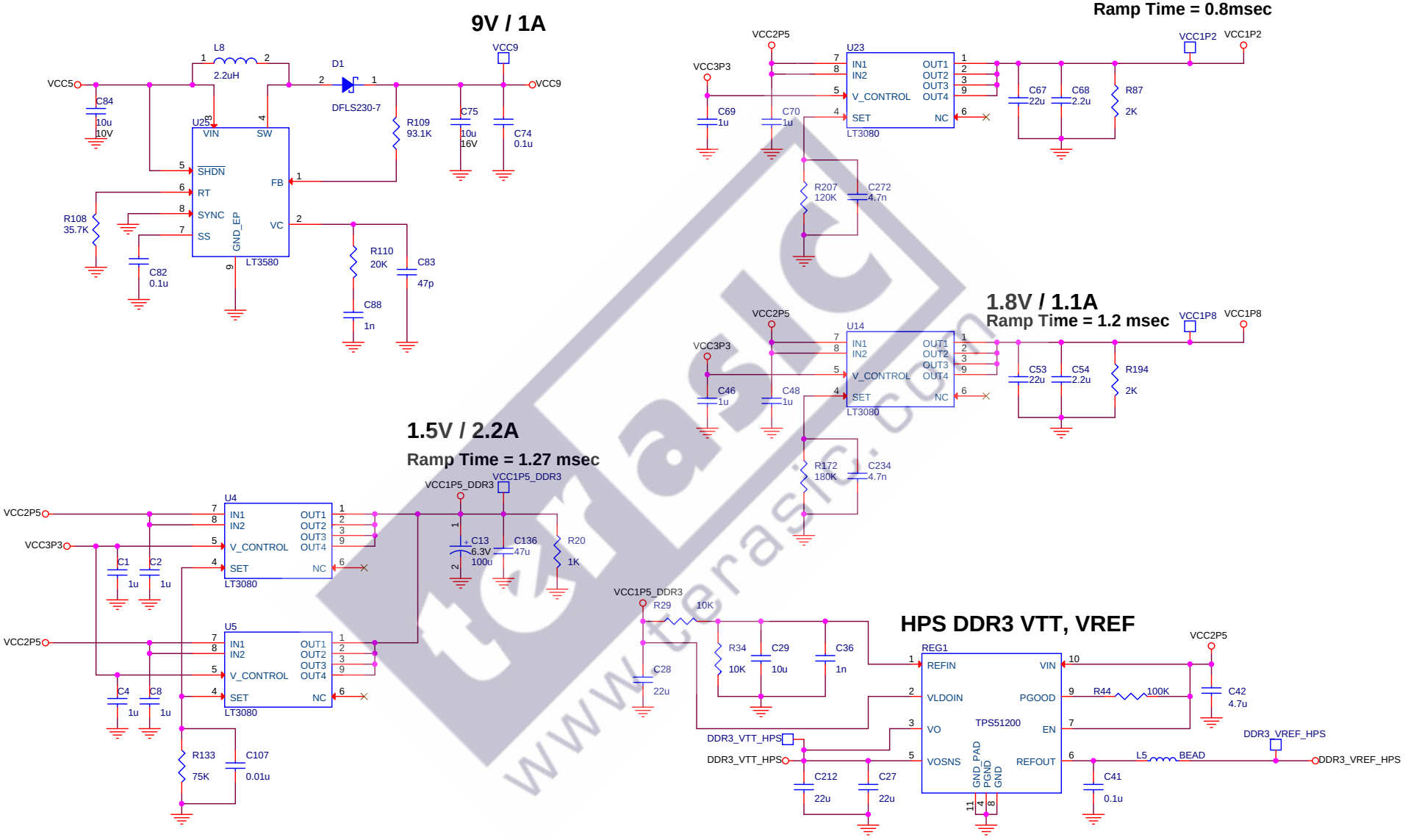
Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	Power - 2.5V, 3.3V	B0

Date: Wednesday, March 23, 2016 Sheet 23 of 24



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Title
DE0-Nano-SoC-HDMI Board

Size	Document Number	Rev
B	Power - 1.2V, 1.5V, 1.8V, 9V	B0

Date: Wednesday, March 23, 2016 Sheet 24 of 24