Cell Characterization using Spectre

1. **INVERTER:**

- **Inverter-cell18 model**

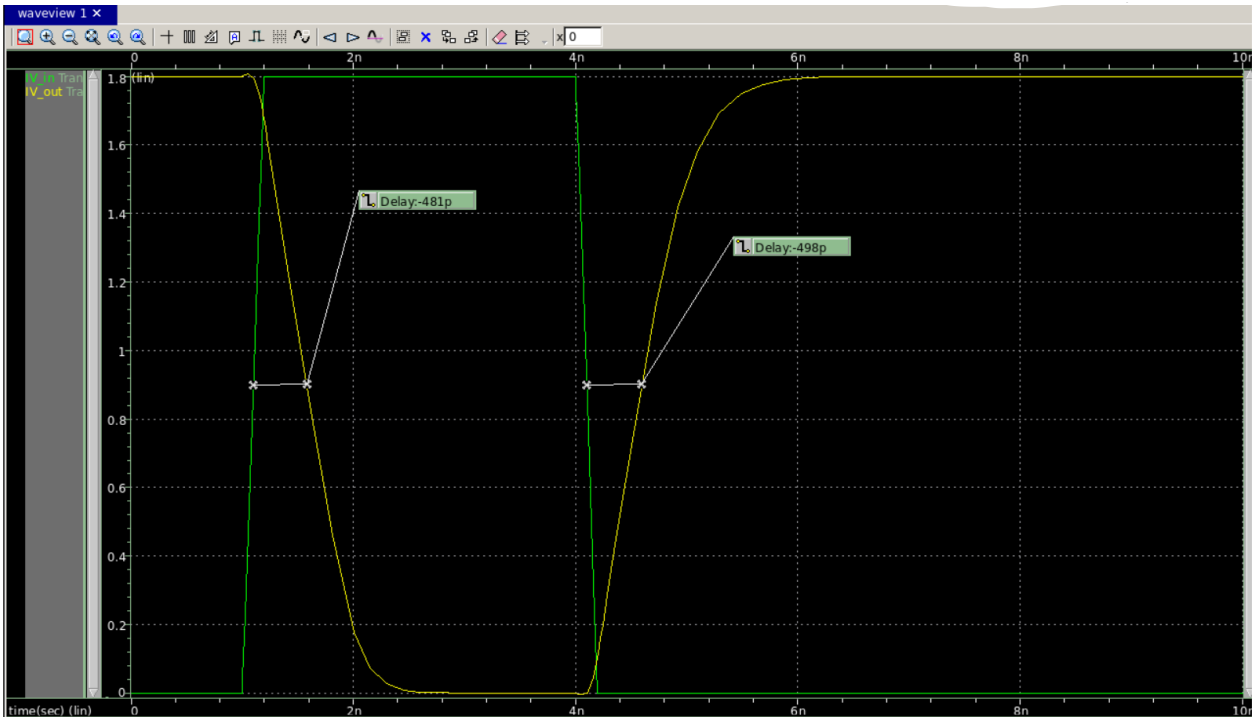
2. olympus.ece.tamu.edu (1)

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV
```

- **Delay Plot with RC**

2. olympus.ece.tamu.edu (1)

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.900u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out

~
```

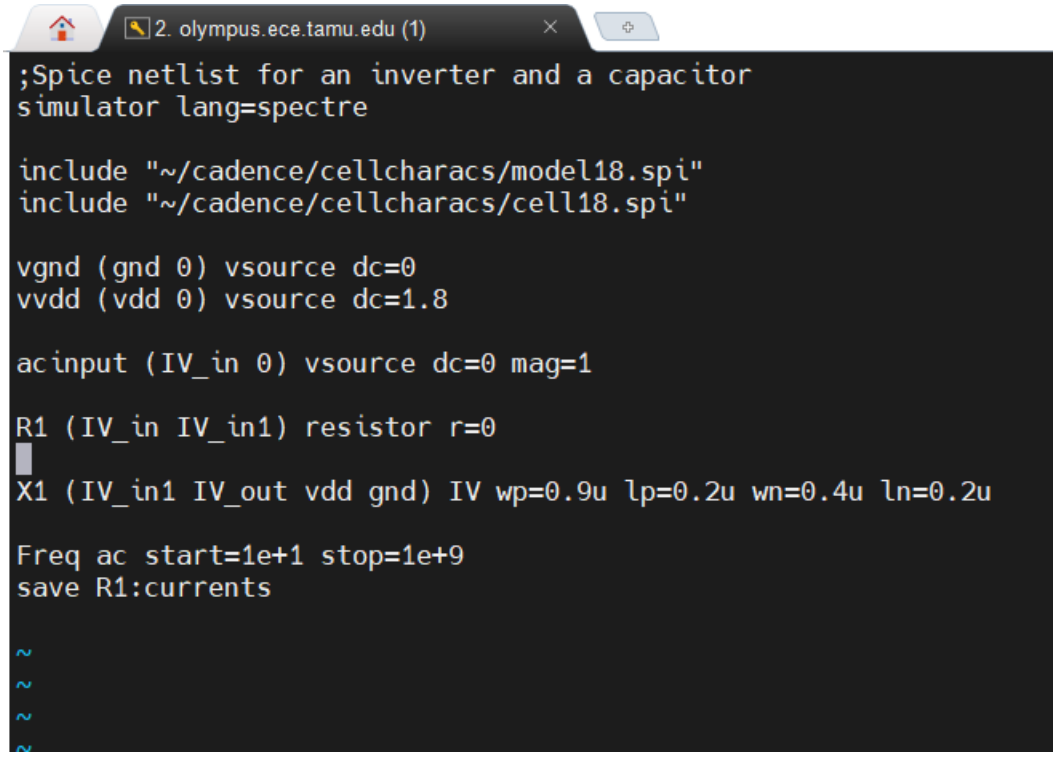


- **Delay table with Capacitance only**

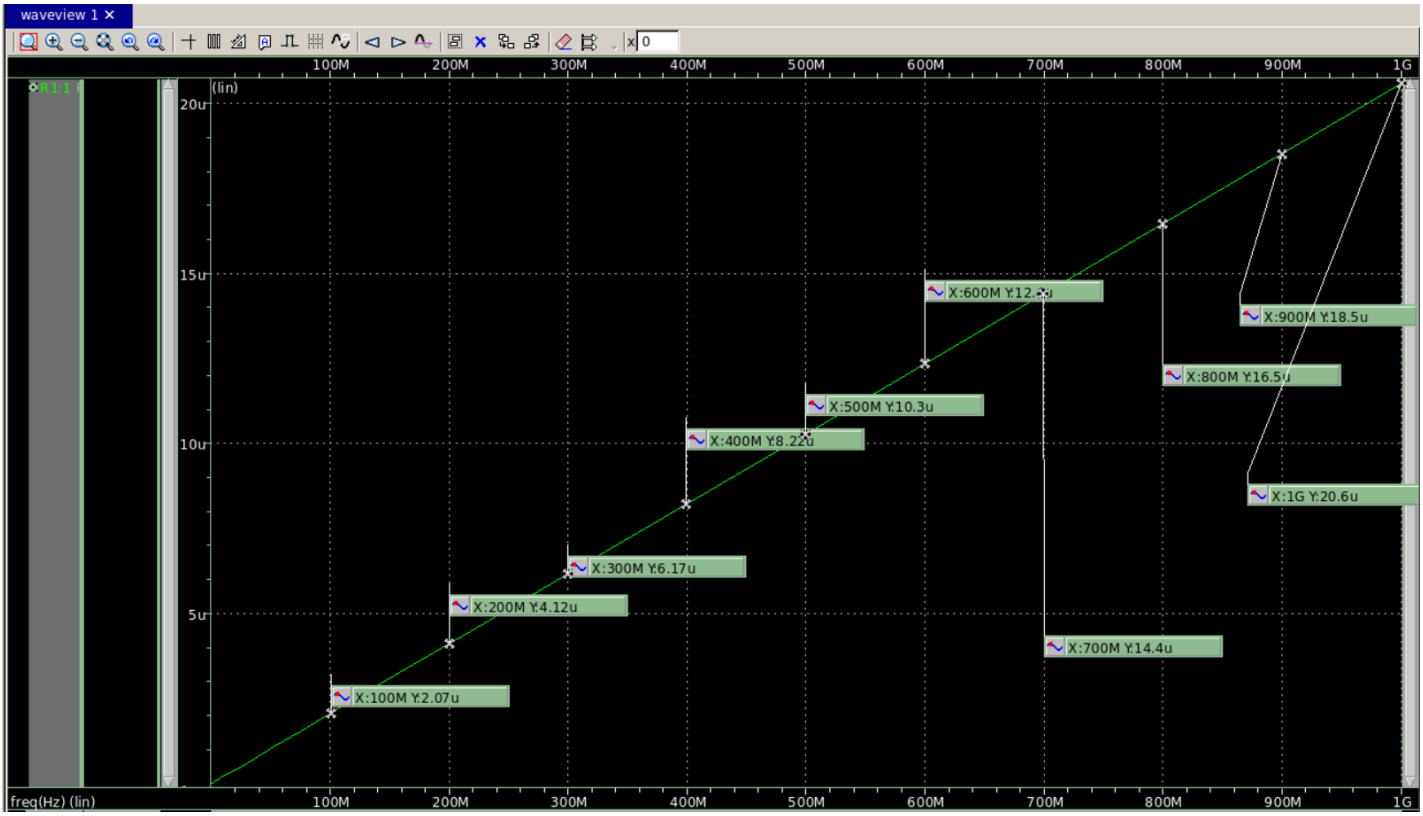
```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

;R1 (IV_out 1) resistor r=1
C1 (IV_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Load Capacitance Value(fF)	Rising Edge Delay(p)	Falling Edge Delay(p)	%error
5f	57.7	74.5	29.11611785
10f	85.8	101	17.71561772
20f	131	144	9.923664122
22f	140	153	9.285714286
30f	175	188	7.428571429
40f	219	232	5.936073059
50f	262	277	5.72519084
60f	306	321	4.901960784
65f	329	345	4.863221884
70f	351	368	4.843304843
75f	372	389	4.569892473
80f	393	410	4.325699746
88f	430	445	3.488372093
90f	439	451	2.733485194
100f	481	498	3.534303534

- **SinkCap**



- **AC PLOT**



- **Capacitance Table**

Frequency(MHz)	Current(uA)	C = (I/2pif)
100	2.07	3.29318E-15
200	4.12	3.27727E-15
300	6.17	3.27197E-15
400	8.22	3.26932E-15
500	10.3	3.27727E-15
600	12.4	3.28788E-15
700	14.4	3.27273E-15
800	16.5	3.28125E-15
900	18.5	3.2702E-15
1000	20.6	3.27727E-15
	Inveter Sink Cap	**3.27783E-15**

2) NAND

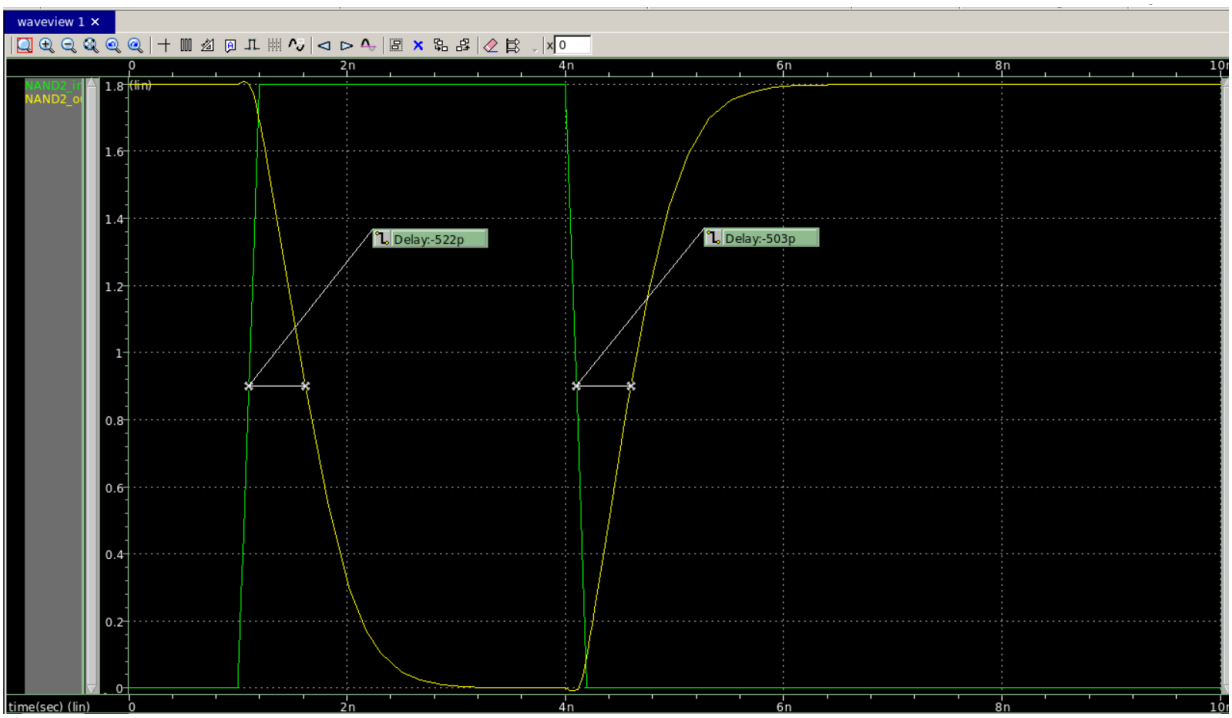
- **NAND cell18 model**

```
//Spice netlist for NAND2
simulator lang=spectre
subckt NAND2 (inputA inputB output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output inputA VDD VDD tsmc18P w=wp l=lp
        M2 output inputB VDD VDD tsmc18P w=wp l=lp
        M3 output inputA X VSS tsmc18N w=wn l=ln
        M4 X inputB VSS VSS tsmc18N w=wn l=ln

ends NAND2
```

- **Delay Plot with RC**

2. olympus.ece.tamu.edu (1)

```
;Spice netlist for an Nand2 and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_nand.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.900u lp=0.2u wn=0.45u ln=0.2u

R1 (NAND2_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```



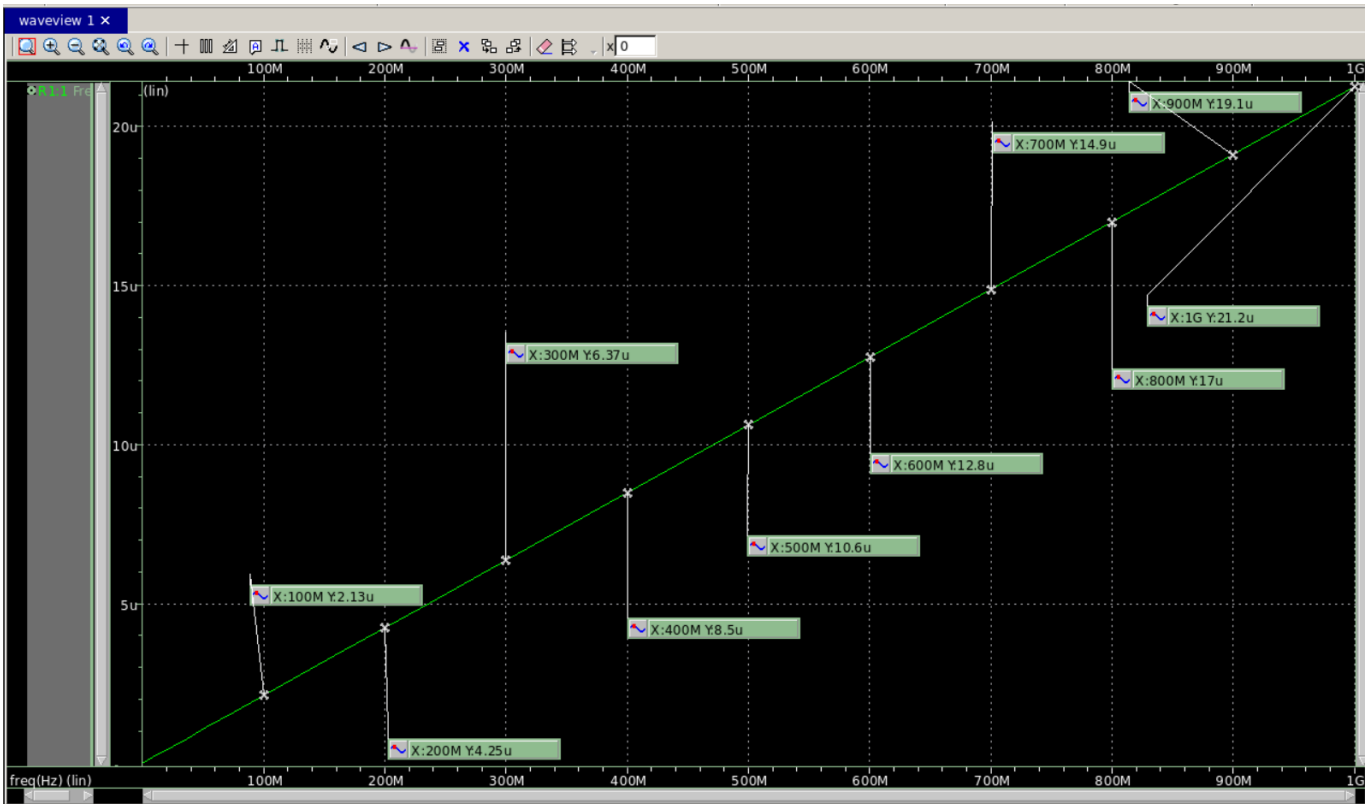
- **Delay Table(C only)**

```
;Spice netlist for an Nand2 and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_nand.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.900u lp=0.2u wn=0.45u ln=0.2u

;R1 (NAND2_out 1) resistor r=1
C1 (NAND2_out 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```

Load Capacitance Value	Rising Edge Delay	Falling Edge Delay	%error
5f	67.2	80.4	19.64285714
10f	96.1	106	10.30176899
20f	144	149	3.472222222
22f	153	159	3.921568627
30f	192	194	1.041666667
40f	240	238	0.840336134
50f	287	283	1.413427562
60f	334	326	2.45398773
65f	358	349	2.578796562
70f	384	373	2.949061662
75f	407	396	2.777777778
80f	430	414	3.8647343
88f	467	452	3.318584071
90f	476	461	3.253796095
100f	522	504	3.571428571

- **Sink Cap**

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_nand.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (NAND2_in 0) vsource dc=0 mag=1

R1 (NAND2_in NAND2_in1) resistor r=0

X1 (NAND2_in1 vdd NAND2_out vdd gnd) NAND2 wp=0.9u lp=0.2u wn=0.45u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```



Frequency(MHz)	Current(uA)	C = (I/2pif)
100	2.13	3.38864E-15
200	4.25	3.38068E-15
300	6.37	3.37803E-15
400	8.5	3.38068E-15
500	10.6	3.37273E-15
600	12.8	3.39394E-15
700	14.9	3.38636E-15
800	17	3.38068E-15
900	19.1	3.37626E-15
1000	21.2	3.37273E-15
	Sink Cap	**3.38107E-15**

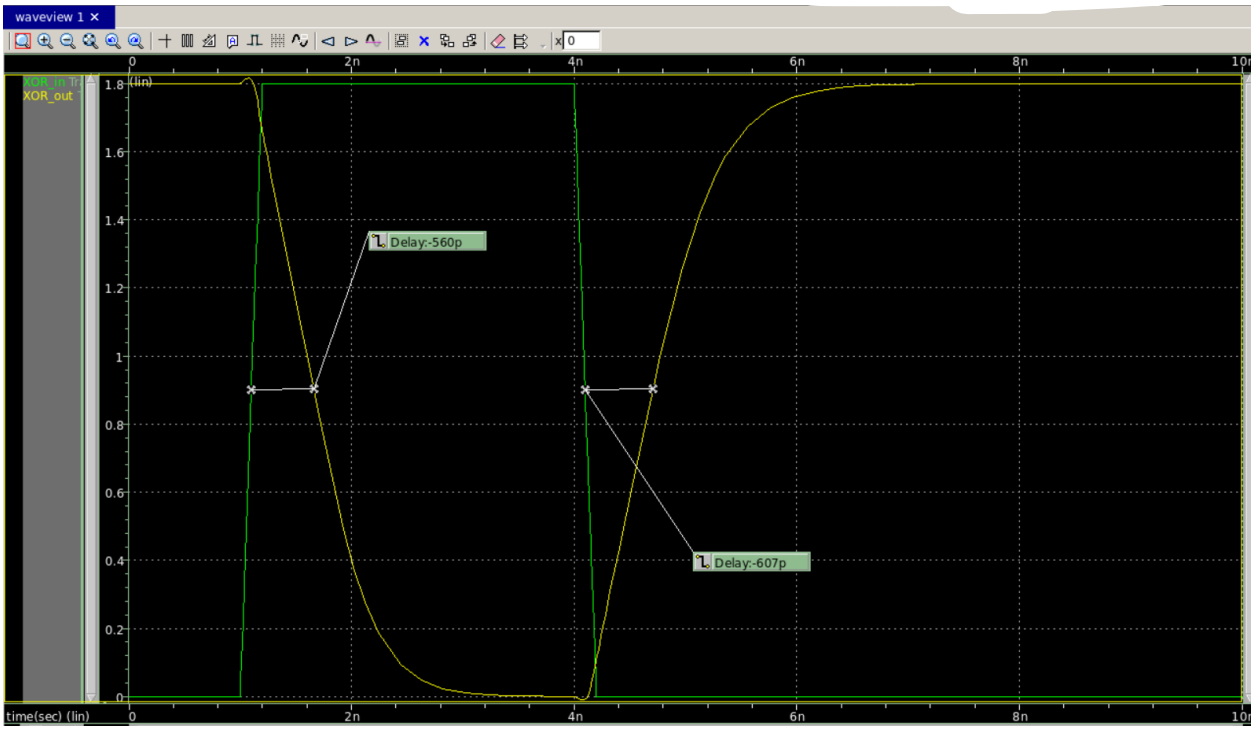
3) XOR

- **XOR cell18 model**

```
//Spice netlist for XOR
simulator lang=spectre
subckt XOR (inputA inputB output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 a inputA VDD VDD tsmc18P w=wp l=lp
        M2 a inputA VSS VSS tsmc18N w=wn l=ln
        M3 b inputB VDD VDD tsmc18P w=wp l=lp
        M4 b inputB VSS VSS tsmc18N w=wn l=ln

        M5 x1 inputB VDD VDD tsmc18P w=wp l=lp
        M6 output a x1 VDD tsmc18P w=wp l=lp
        M7 output a x2 VSS tsmc18N w=wn l=ln
        M8 x2 b VSS VSS tsmc18N w=wn l=ln

        M9 y1 b VDD VDD tsmc18P w=wp l=lp
        M10 output inputA y1 VDD tsmc18P w=wp l=lp
        M11 output inputA y2 VSS tsmc18N w=wn l=ln
        M12 y2 inputB VSS VSS tsmc18N w=wn l=ln

ends XOR
```

- **XOR-Delay with RC**

```
;Spice netlist for an Nand2 and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_xor.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR_in vdd XOR_out vdd gnd) XOR wp=1.40u lp=0.2u wn=0.4u ln=0.2u

R1 (XOR_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR_in XOR_out
```



- **Delay Table(With C)**

```
;Spice netlist for an Nand2 and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_xor.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR_in vdd XOR_out vdd gnd) XOR wp=1.4u lp=0.2u wn=0.4u ln=0.2u

;R1 (XOR_out 1) resistor r=1
C1 (XOR_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR_in XOR_out
```

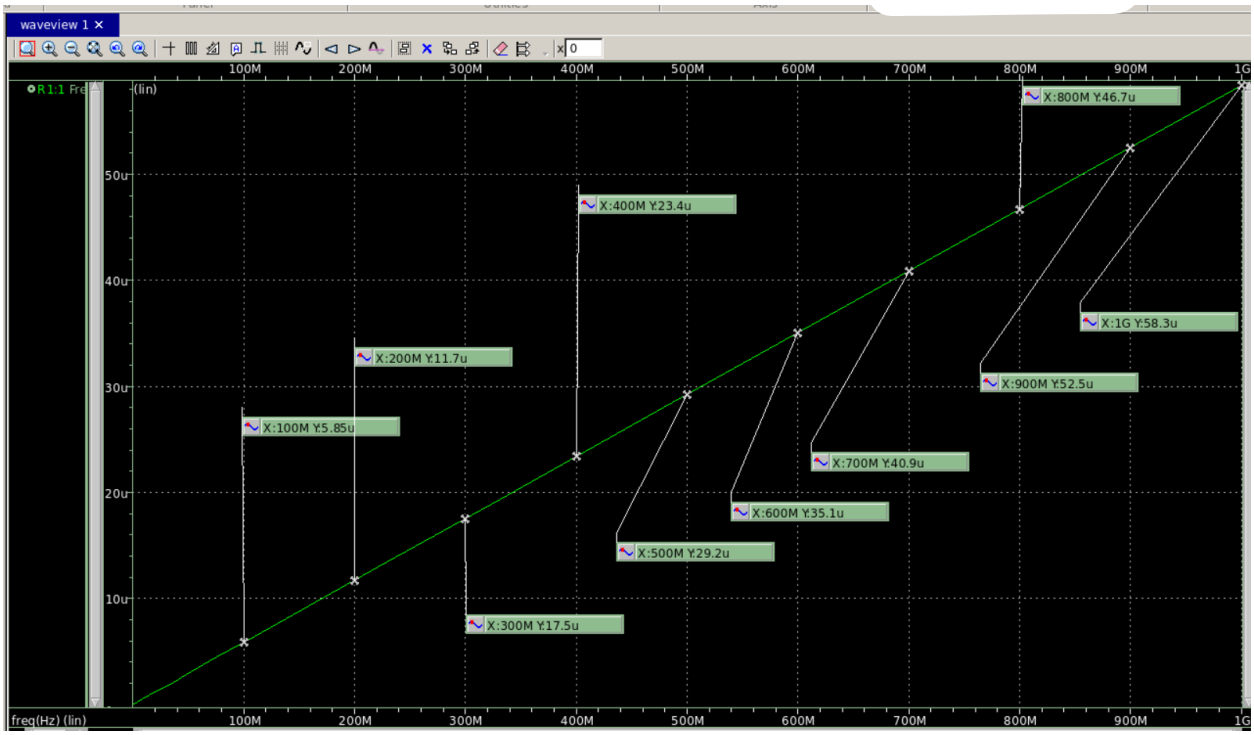
- **Delay Table**

Load Capacitance Value(fF)	Rising Edge Delay	Falling Edge Delay	%error
5f	65.7	76.5	16.43836
10f	94.1	108	14.77152
20f	147	164	11.56463
22f	157	175	11.46497
30f	199	220	10.55276
40f	251	276	9.960159
50f	303	331	9.240924
60f	355	386	8.732394
65f	381	415	8.923885
70f	406	442	8.866995
75f	432	469	8.564815
80f	457	496	8.533917
88f	499	543	8.817635
90f	509	551	8.251473
100f	560	607	8.392857

- **Sink Cap**

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18_xor.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (XOR_in 0) vsource dc=0 mag=1

R1 (XOR_in XOR_in1) resistor r=0

X1 (XOR_in1 vdd XOR_out vdd gnd) XOR wp=1.4u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

- **AC plot**



- **Capacitance Table**

Frequency(MHz)	Current(uA)	C = (I/2pif)
100	5.85	9.30682E-15
200	11.7	9.30682E-15
300	17.5	9.2803E-15
400	23.4	9.30682E-15
500	29.2	9.29091E-15
600	35.1	9.30682E-15
700	40.9	9.29545E-15
800	46.7	9.28693E-15
900	52.5	9.2803E-15
1000	58.3	9.275E-15
	Sink Cap of XOR	**9.29362E-15**