

SHIRISHA VISSOM

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EDUCATION

Texas A&M University

08/2022 – Present

Master of Science in Electrical Engineering ; GPA - 3.5/4.0

College Station, Texas, United States

Specialisation: VLSI Design.

Courses: VLSI Physical Design Automation, Parallel Computing, Computer Architecture, Advanced Digital System Design, Microprocessor System Design, Digital Integrated Circuits, VLSI Circuit Design.

M.S. Ramaiah University of Applied Sciences

08/2017 – 06/2021

Bachelor of Technology in Electronics and Communications ; CGPA - 9.11/10

Bangalore, India

Courses: Digital Logic Circuits, Microprocessors and Microcontrollers.

SKILLS

Design Tools: Schematic and Layout (Cadence Virtuoso), Digital Design(Vivado Design Suite).

EDA Tools: Synthesis (Synopsys Design Compiler), Place and Route (Cadence Innovus).

Static Timing Analysis Tools: Synopsys (Primetime), YOSYS Synthesis Tool (QFLOW).

Hardware Experience: Oscilloscope, Vector Network Analyzer, Soldering.

Languages: Python, Verilog, Perl, TCL.

Simulation Tools: MATLAB, Simulink.

EXPERIENCE

Raman Research Institute

11/2021 – 07/2022

Electrical Engineer Intern - POLIX Hardware team

Bangalore, India

This project is based on developing X-Ray Polarimeter for studying various dynamics of bright astronomical X-ray sources.

- Involved in Design of Power supply for **Charge Sensitive Pre-Amplifier and Amp-tek-PH300 chip**.
- Testing of the Amp-tek PH300 chip to determine its upper threshold voltage (9V) and lower threshold voltage (200mV).
- Implemented **timing checks and ADC calibration on digital cards**.

PROJECTS

- Design and Floorplan analysis of a Multiplier using YOSYS (QFLOW)** 03/2023
 - Synthesized an RTL netlist of a Multiplier and mapped it to standard cell components producing a Library (LIB) file.
 - Configured clock period, IO port assignments, and drive strength using a **custom Perl script**.
 - Conducted a **Pre-layout Static Timing Analysis (STA)** to obtain critical path delay of 2.5 ns.
 - Designed floorplan with height and width (400µm and 600µm), achieved Utilization Factor of 54.7%, and an Aspect Ratio of 0.66.
- Design and Synthesis of a Cruise Control Logic - Synopsys Primetime** 11/2022
 - Designed a **Finite State Machine model based Cruise Control Logic** and synthesized it in 180nm technology.
 - SDC constraints were set (Input Drive Strength, Output Capacitance Load, Clock period and Input delay) resulting in an overall cell area of 10.463mm².
 - Achieved a maximum slack path of 3.8ns and a minimum slack path of 0.13ns.
- Automatic Place and Route of Cruise Control Logic - Cadence Innovus** 11/2022
 - Utilization factor of 70% and an Aspect Ratio of 0.9 was used to perform **Place And Route** of Cruise Control Logic.
 - Analysed **SPEF** file and **optimised power routings** to minimize capacitance on critical nets in order to achieve a maximum Operating Frequency of 195 MHz.
- Characterization of D Flip-Flop - Cadence Virtuoso** 11/2022
 - Created testbench and executed post layout simulation to analyse **delay characteristics and setup time** of a D Flip-Flop.
 - Strategically **optimized logical effort and transistor sizing**, resulting in a rise delay of 0.649ns, a fall delay of 0.652ns, and achieving a rise/fall delay difference of 0.32%, (well below the design specification of 10%) and setup time of 0.28ns.
- Design of 8-bit pipelined Adder with buffered H-clock tree - Cadence Virtuoso** 10/2022
 - Designed the layout for an 8-bit Pipelined Adder, incorporating a **Buffered H-clock tree** Distribution Network.
 - Achieved a maximum delay of 1.65ns and minimum clock period of 1.93ns, indicative of a well-optimized and efficient design.
- Place and Route of 2:1 Analog Multiplexer** 09/2022
 - Created an RTL code for the 2:1 Analog Multiplexer and built its custom layout using the Sky130 library.
 - Modified the LEF file and layout dimensions, implemented a **Floorplan**, Detailed Placement, **Power Distributed Network design**, Routing, and DRC verification, resulting in a final layout of the Analog Multiplexer, achieving a macro height of 5.444 µm.

EXTRA-CURRICULAR

International Symposium Physical Design: ISPD

03/2023

On-going Research on Physical Design

Texas, United States

* Attended the three-day virtual conference on state-of-the-art research on traditional IC physical design.

Smart India Hackathon

03/2020

Demonstrated an automated Mini Cart using Trilateration and GPS

Bangalore, India

CERTIFICATIONS

- VLSI System Design (VSD) - Physical Design Flow, Static Timing Analysis, Signal Integrity, Clock Tree Synthesis - Udemy
- VSD Intern - Mixed Signal Physical Design Flow - Sky130 - Udemy
- VSD - Physical Design and Analysis using Open-Source Tools - QFLOW - Udemy
- Python - Basic to Advance - Udemy
- Basic Static Timing Analysis - Cadence