SHIRISHA VISSOM

College Station, TX - 77840 | +1 (513) 500-7767 | shirisha_2022@tamu.edu| | LinkedIn | GITHUB |

Objectives

Graduate student, with strong background in VLSI Design, actively seeking internship/Co-op opportunities starting Fall of 2023 in Physical Design and Static Timing Analysis.

Education

Texas A&M University College Station, Texas

- **M.S. in Electrical Engineering**; Specialization: VLSI Design; GPA: 3.5 Aug 2022 -May 2024
- ***Courses:*** Advanced Digital System Design, Microprocessor System Design, Digital Integrated Circuits, VLSI Circuit Design

M.S. Ramaiah University of Applied Sciences Bangalore, India

- **B.Tech. in Electronics and Communication**; GPA: 9.11 Aug 2017 - May 2021
- ***Courses:*** Digital Logic Circuits, Computer Architecture, Microprocessors and Microcontrollers

Experience

Summer Project: Texas A&M University (Ongoing) College Station, Texas
ASIC implementation for EMPT simulation May 2023-August 2023

- Involved in design of system architecture using 45nm PDK, consisting of Processor, Memory, and Matrix multiplication.
- Designing of DSP architecture using pipelining to suite faster operations and improve continuous simulations.

Raman Research Institute Bangalore, India
Electrical Engineer – POLIX Hardware team *Nov 2021 – July 2022*

- Involved in the Post-silicon **hardware integrated testing** of Analog & Digital IC cards.
- Design and testing of Power supply for Charge Sensitive Pre-Amplifier and amtek-PH300 chip.
- Implemented timing checks and ADC calibration on digital cards.

Projects

Design and Performance analysis of a Multiplier using YOSYS(QFLOW) *Mar-2023*

- Synthesized the RTL netlist using Yosys synthesis tool from Qflow
- Engineered the floorplan to the given die width and height
- Performed **Pre-layout STA** & ensured **50% utilization factor** & an **aspect ratio of 0.6.**

Design and synthesis of a Cruise Control Logic | Synopsys Primetime *Nov-2022*

- Synthesized the RTL Design with a specific library for 180nm technology to build gate-level netlist, performed Pre-layout STA and also designed the SDC constraint
- Performed the entire PD flow and analyzed the routing topology to reduce congestion
- Generated **SPEF Files** to determine the Parasitic RC of the nets for crosstalk and **signoff STA analysis**

Characterization of D Flip-Flop *Nov-2022*

- Designed the transistor level schematic and layout of a D-Flipflop using TSMC02 library(180nm)
- Implemented post layout simulation to estimate the rise and fall delays for a variance of load from 1fF-100fF
- Reduced variation in fall and rise delays by optimizing logical effort and resizing the transistors
- Determined the setup time for rising and falling transitions and delay arc of the Flip-Flop

Design of 8-bit pipelined Adder with buffered H-clock tree | Cadence Virtuoso *Oct-2022*

- Designed the layout of an 8 bit-Pipelined Adder with **Buffered H-clock tree**
- Performed **DRC and LVS checks**. H-Tree clock structure was designed to achieve close to zero clock skew
- Computed the maximum operating frequency considering the setup time, cell delay and the insertion delay of the D-flipflops

Design of a Folded Cascode Amplifier using CMFB and Biasing Circuit | Cadence Virtuoso *Dec-2022*

- Designed a **schematic and layout** for a Folded Cascode amplifier, with a biasing circuit and common mode feedback circuit
- Performed **ADEL simulations** for design optimization, to obtain graphical relation between gain, power, and phase margin

Technical Skills

Design Tools:	Schematic & Layout (Cadence Virtuoso) || Digital Design (Xilinx Zynq-7000 SOC, ISE Design Tool)
EDA Tools:	Synthesis (Synopsys Design Compiler) || Place and Route (Cadence Innovus)
Static Timing Analysis Tools:	STA (Synopsys Primetime) || (YOSYS Synthesis Tool ||QFLOW)
Simulation Tools:	NI Multisim, ModelSim, Calibre, ADEL.
Languages:	Python|| Verilog || Scripting Languages: Perl, TCL || GITHUB

Certifications

- VSD - Physical Design Flow, Static Timing Analysis, Signal Integrity, Clock Tree Synthesis *UDEMY | Mar-2023*
- VSD Intern - Mixed Signal Physical Design Flow - Sky130 *UDEMY | Mar-2023*
- VSD - Physical Design and Analysis using Open-Source Tools - Proton *UDEMY | Feb-2023*

Extra-Curricular Activities

- **International Symposium Physical Design**: ISPD 2023 *Mar-2023*
  Attended the three-day virtual conference on state-of-the-art research on traditional IC physical design
- **Smart India Hackathon - Grade A** for demonstrating an automated Mini Cart using Trilateration and GPS *Mar-2020*