Shirisha Vissom

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EDUCATION

Texas A&M University **08/2022 – Present**

Master of Science in Electrical Engineering ; GPA - 3.5/4.0 *College Station, Texas, United States*

Specialisation: VLSI Design.

Courses: Advanced Digital System Design, Microprocessor System Design, Digital Integrated Circuits, VLSI Circuit Design.

M.S. Ramaiah University of Applied Sciences **08/2017 – 06/2021**

Bachelor of Technology in Electronics and Communications ; CGPA - 9.11/10 *Bangalore, India*

Courses: Digital Logic Circuits, Computer Architecture, Microprocessors and Microcontrollers.

Major Project: Development of a Passive Radar system.

SKILLS

Design Tools: Schematic and Layout (Cadence Virtuoso), Digital Design (Xilinx Zynq-7000 SOC, ISE Design Tool)
EDA Tools: Synthesis (Synopsys Design Compiler),Place and Route (Cadence Innovus)
Static Timing Analysis Tools: Synopsys (Primetime),YOSYS Synthesis Tool(QFLOW)
Hardware Experience: Network Analyzer, Oscilloscope, Vector Network Analyzer, FPGA based implementation in Verilog, Soldering
Languages: Python,Verilog,Perl, TCL, GITHUB
Simulation Tools:: MATLAB, Simulink, Modelsim, AutoCAD, Mentor Graphics, Calibre ADEL.

EXPERIENCE

Raman Research Institute **11/2021 – 06/2022**

Electrical Engineer Intern-POLIX Hardware team *Bangalore, India*

This project is based on developing X-Ray Polarimeter for studying various dynamics of bright astronomical X-ray sources in extreme conditions.

- Involved in the Post silicon hardware **integrated testing of Analog & Digital IC cards.**
- Implemented **timing checks and ADC calibration on digital cards.**
- Design and testing of Power supply for **Charge Sensitive Pre-Amplifier and amtek-PH300 chip.**

PROJECTS

- **Place and Route of Analog I/P , 2:1 analog multiplexer** **06/2023**
  - Employed OpenLane to execute PNR for a 2:1 analog multiplexer IP.
  - Systematically modified existing IP layouts to align with OpenLane's specifications, ensuring efficient processing within the toolchain.
- **Design and Floorplan analysis of a Multiplier using YOSYS(QFLOW)** **03/2023**
  - Synthesized a RTL netlist from Qflow, designed floorplan with height and width of 400umx600um.
  - Conducted Pre-layout STA with 50% utilization and 0.6 aspect ratio.
- **Design and synthesis of a Cruise Control Logic - Synopsys Primetime** **11/2022**
  - The RTL Design was synthesized using a 180nm technology-specific library to generate a gate-level netlist. S.SDC constraints were designed, having cell area of 10463µm^2 and a register count of 20.
  - Pre-layout STA was performed, resulting in a slack of maximum path of 3.8ns and minimum path of 0.13ns.
- **Automatic place and route of Cruise Control Logic- Cadence Innovus** **11/2022**
  - Defined the floorplan with a utilization factor of 0.7 (70%) and an aspect ratio of 0.9.
  - Calculated the total wire length for detailed routing as 9328µm.
  - Generated SPEF files to evaluate the parasitic RC of nets.
- **Characterization of D Flip-Flop** **11/2022**
  - Designed transistor-level schematic and layout of a D-Flipflop using TSMC02 library (180nm)
  - Estimated rise delay (0.649ns) and fall delay (0.652ns) with a 0.32% error.
  - Optimized logical effort and transistor sizing to minimize variation and achieved a setup time of 0.28ns.
- **Design of 8-bit pipelined Adder with buffered H-clock tree - Cadence Virtuoso** **10/2022**
  - Designed the layout of an 8 bit-Pipelined Adder with Buffered H-clock tree.
  - Computed the maximum delay of 1.65ns and maximum clock period of 1.93ns

TRAINING

- Virtual training on "Digital Design and Implementation" on Xilinx Spartan 6 and Xilinx Artix 7 *Bangalore, India*
- Attended a virtual conference on Partial Reconfiguration on "Xilinx FPGA/ZYNQ SoC". *Bangalore, India*

Extra Curricular

International Symposium Physical Design: ISPD **03/2023**

On-going Research on Physical Design *Texas, United States*

∗ Attended the three-day virtual conference on state-of-the-art research on traditional IC physical design.

Smart India Hackathon **03/2020**

Demonstrated an automated Mini Cart using Trilateration and GPS *Bangalore, India*

CERTIFICATIONS

- VSD - Physical Design Flow, Static Timing Analysis, Signal Integrity, Clock Tree Synthesis
- VSD Intern - Mixed Signal Physical Design Flow - Sky130
- VSD - Physical Design and Analysis using Open-Source Tools - Proton
- Python- Basic to Advance - Udemy
- Cadence: Basic Static Timing Analysis v2.0 Exam