POKHARA UNIVERSITY

Level: Bachelor | Semester: Spring | Year : 2018
Programme: BE | Full Marks: 100
Course: Logic Circuit | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.

1. a) How does the logic system express data during computation? Differentiate between Digital and Analog system. 5
   b) Perform the conversion as indicated (any two). 5
      i. $(235)_6 = (\quad)_{\text{Excess-3}}$
      ii. $(369)_{10} = (\quad)_{2421}$
      iii. $(BCA)_{16} = (\quad)_2$
   c) Use 2's complement to subtract the following: 5
      i. $(1010)_2 - (10100)_2$
      ii. $(957)_{10} - (876)_{10}$
      iii. $(378)_{BCD} - (256)_{BCD}$
2. a) Why NAND and NOR are called Universal Gates? Construct F=AB+CD using universal gates. 7
   b) Define K-Map. Simplify the expression mentioned below using K-Map. 8
      $F(A, B, C, D) = \sum (1,3,7,10,13,15)$
      $d(A, B, C, D) = \sum (0, 2, 8)$
      Where d denotes don't care. Also implement the simplified function using NOR gates only.
3. a) Design a combinational circuit that has four inputs and two outputs one of the outputs is high when majority of inputs are high .The second output is high only when all inputs are of same type. 7
   b) Implement the following Boolean function using 16:1 Multiplexer 8
      $F(A,B,C,D,E)=\sum m(2,4,5,7,10,14,15,16,17,25,26,30,31)$
4. a) Design a 4 bit parallel adder subtractor circuit with one selection variables M and two inputs A and B. For M = 0, the circuit required to perform addition i.e. (A+B) and for M = 1, the circuit must perform subtraction (A – B) by taking 2'S complement of B. 7
   b) Explain negative edge triggered S-R flip-flop with necessary logic diagram, characteristic table, characteristic equation and waveform. 8
5. a) Design a synchronous Mod-6 counter using clocked D Flip Flop 8
   b) Define shift register. Draw diagram for parallel in serial out shift register and discuss its operation with necessary explanation. 7
6. a) Explain the process how does binary value of 4 flags in status register change with necessary diagram. 8
   b) Design a 3-bit Synchronous DOWN Counter using T flip-flop. 7
7. Write short notes on: (Any two) 2×5
   a) State Reduction and State Assignment
   b) Random Access Memory
   c) Self-complementing code