POKHARA UNIVERSITY

Level: Bachelor | Semester:Spring | Year : 2019
Programme:BE | Full Marks: 100
Course:Logic Circuits | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

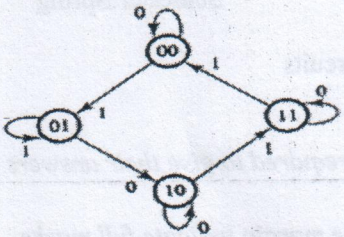
Attempt all the questions.

1. a) With characters differentiate between Digital and Analog system. 5
   b) Perform the conversion as indicated (any two). 5
      i. $(543)_6 = (\quad)_{Excess\text{-}3}$
      ii. $(708)_{10} = (\quad)_{2421}$
      iii. $(BBA)_{16} = (\quad)_2$
   c) Use 2's complement to subtract the following: 5
      i. $(1011)_2 - (10100)_2$
      ii. $(952)_{10} - (873)_{10}$
      iii. $(368)_{BCD} - (256)_{BCD}$
2. a) Prove the following Boolean expression 5
      i. $\overline{AB} + BC + \overline{A}\overline{BC} = \overline{A} + BC$
      ii. $X\overline{Y} + Y\overline{Z} + Z\overline{X} = \overline{X}Y + \overline{Y}Z + \overline{Z}X$
   b) Simplify the Boolean function **F**and don't care conditions **d** in(1) SOP (2) POSand (3) draw NAND-NAND equivalent logic. Given: 5
      F= B'CD'+A'CD+A'BC+ A'B'C'D'
      d=A'BC'D+ACD+AB'D'
   c) A Boolean function is given by $F(A,B,C,D) = \sum(0,1,2,3,10,13,14)$ and don't care condition $d(A,B,C,D) = \sum(4,7,12)$. Simplify it using K-Map and implement using NAND gate only. 5
3. a) Design a combinational circuit that converts decimal digits from 8-4-2-1 to Excess 3 8
   b) Design a combinational circuit using PLD device as PLA (4X8X4) that is used to implement full Subtract or function in which difference is represented as Di and borrow as Br. 7
4. a) Illustrate the process how does binary value of 4 flags in status registers change with necessary diagram. 8
   b) Implement the following with appropriate MUX: 7

i. $F(A,B,C)= \sum (1,4,5,6)$

ii. $F(A,B,C,D)= \sum (0,1,3,8,9,15)$

5. a) Realize the following state diagram into a circuit using SR flip-flop. 8



Describe with diagram the working and characteristics of JK flipflop.

b)Explain operation of J-K Flip-flop with its logic diagram, truth table, excitation table 7

6. a) What are shift registers? Explain Parallel in serial out and Serial in Parallel out shift register with diagrams. 7

b) Design 3 bit up counter using T flip-flop 8

2×5

7. Write short notes on: **(Any two)**

a) Computational Logic Design Procedure

b) Johnson Counter

c) Self-complementing code