GATE SOLVED PAPER - EE

ANALOG & DIGITAL ELECTRONICS

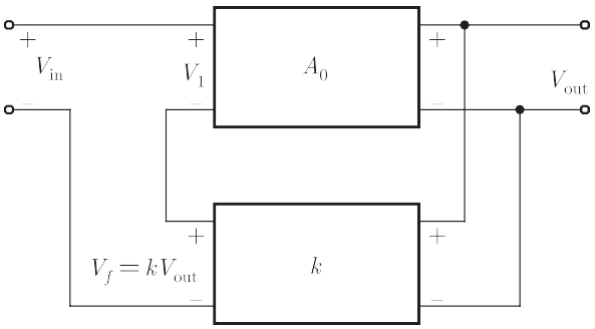
YEAR 2013 **ONE MARK**

Q. 1 A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles

(A) and AND gate (B) an OR gate

(C) an XOR gate (D) a NAND gate

Q. 2 In a voltage-voltage feedback as shown below, which one of the following statements is TRUE if the gain k is increased?



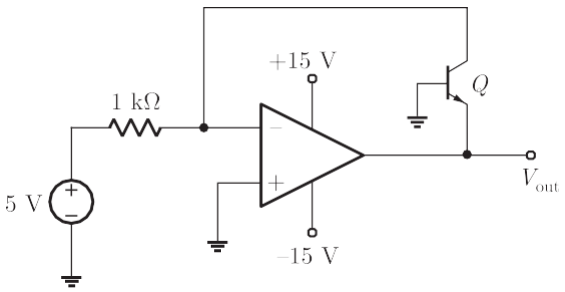
(A) The input impedance increases and output impedance decreases

(B) The input impedance increases and output impedance also increases

(C) The input impedance decreases and output impedance also decreases

(D) The input impedance decreases and output impedance increases

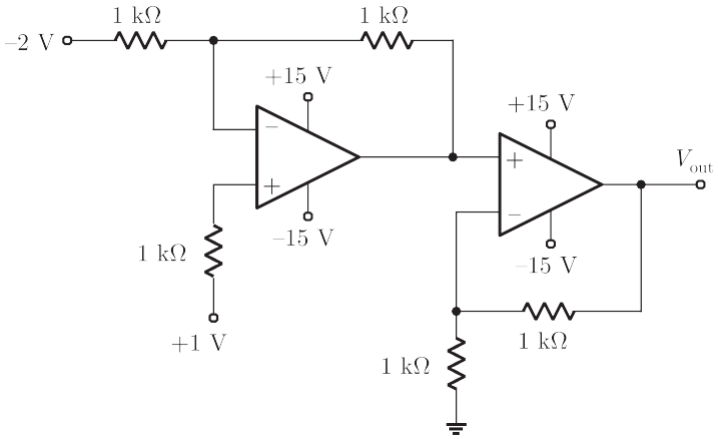
Q. 3 In the circuit shown below what is the output voltage V_{out} if a silicon transistor Q and an ideal op-amp are used?



(A) −15 V (B) −0.7 V

(C) +0.7 V (D) +15 V

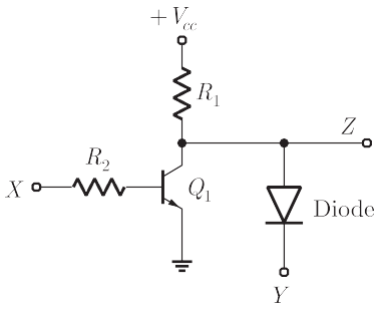
Q. 4 In the circuit shown below the op-amps are ideal. Then, V_{out} in Volts is



(A) 4 (B) 6

(C) 8 (D) 10

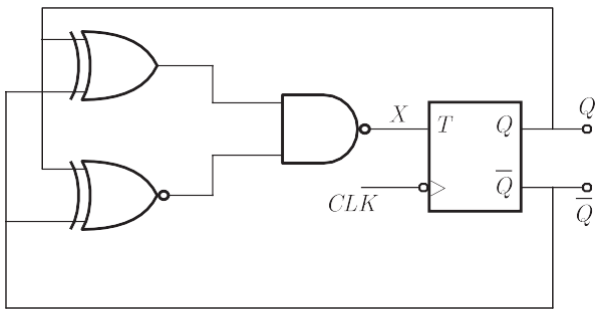
Q. 5 In the circuit shown below, Q_1 has negligible collector-to-emitter saturation voltage and the diode drops negligible voltage across it under forward bias. If V_{cc} is +5 V, X and Y are digital signals with 0 V as logic 0 and V_{cc} as logic 1, then the Boolean expression for Z is



(A) XY (B) $\overline{X}Y$

(C) $X\overline{Y}$ (D) $\overline{XY}$

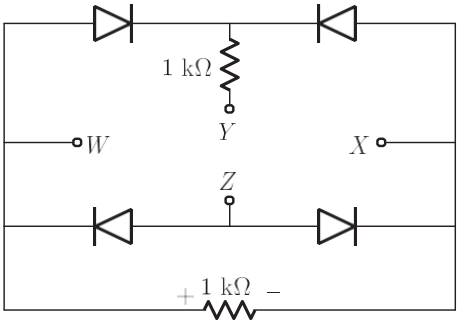
Q. 6 The clock frequency applied to the digital circuit shown in the figure below is 1 kHz. If the initial state of the output of the flip-flop is 0, then the frequency of the output waveform Q in kHz is



(A) 0.25 (B) 0.5

(C) 1 (D) 2

Q. 7 A voltage $1000 \sin wt$ Volts is applied across YZ. Assuming ideal diodes, the voltage measured across $W X$ in Volts, is



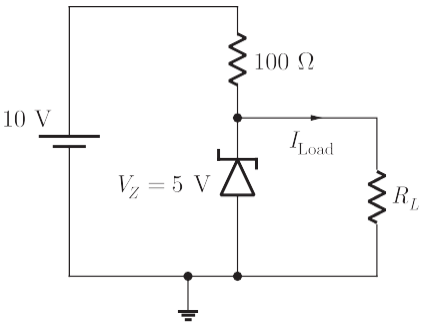
(A) $\sin wt$

(B) $-\sin wt + |\sin wt| / 2$

(C) $\sin wt - \sin wt / 2$

(D) 0 for all t

Q. 8 In the circuit shown below, the knee current of the ideal Zener dioide is10 mA . To maintain 5 V across R_L, the minimum value of R_L in W and the minimum power rating of the Zener diode in mW, respectively, are



(A) 125 and 125

(B) 125 and 250

(C) 250 and 125

(D) 250 and 250

YEAR 2012 ONE MARK

Q. 9 In the sum of products function $f(X, Y, Z) = \sum (2, 3, 4, 5)$, the prime implicants are

(A) $\overline{X}Y, X\overline{Y}$

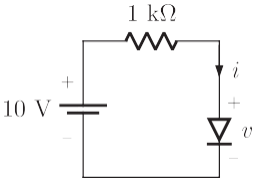
(B) $\overline{X}Y, X\overline{Y}\overline{Z}, XY\overline{Z}$

(C) $\overline{X}Y\overline{Z}, \overline{X}YZ, XY\overline{Z}$

(D) $\overline{X}Y\overline{Z}, \overline{X}YZ, X\overline{Y}\overline{Z}, XY\overline{Z}$

Q. 10 The i-v characteristics of the diode in the circuit given below are

$$i = \begin{cases} \dfrac{v - 0.7}{500} \text{ A}, & v \geq 0.7 \text{ V} \\ 0 \text{ A} & v < 0.7 \text{ V} \end{cases}$$



The current in the circuit is

(A) 10 mA (B) 9.3 mA

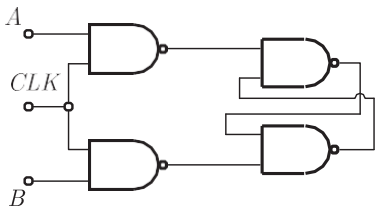
(C) 6.67 mA (D) 6.2 mA

Q. 11 The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

(A) 4 (B) 6

(C) 8 (D) 10

Q. 12 Consider the given circuit



In this circuit, the race around

(A) does not occur

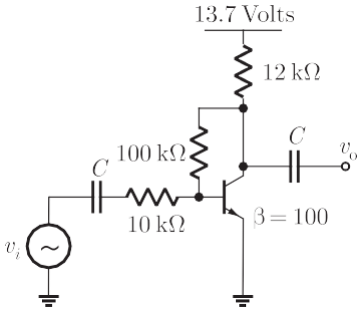
(B) occur when $CLK = 0$

(C) occur when $CLK = 1$ and $A = B = 1$

(D) occur when $CLK = 1$ and $A = B = 0$

YEAR 2012 TWO MARKS

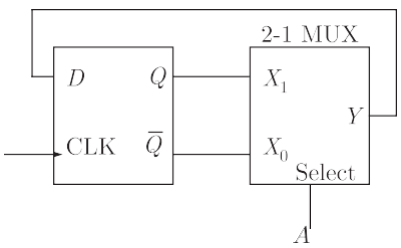
Q. 13 The voltage gain A_v of the circuit shown below is

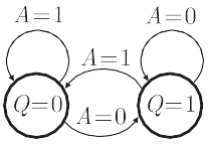


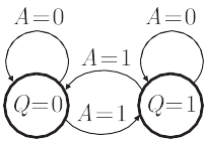
(A) $|A_v| = 200$ (B) $|A_v| = 100$

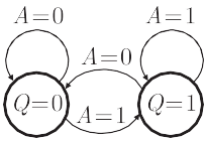
(C) $|A_v| = 20$ (D) $|A_v| = 10$

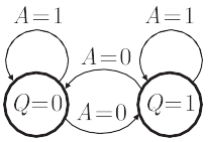
Q. 14 The state transition diagram for the logic circuit shown is



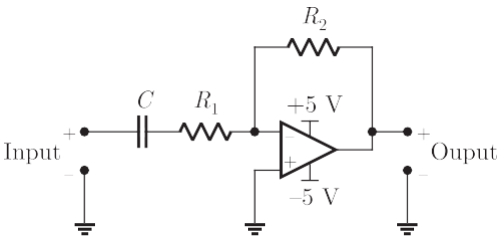
(A) 

(B) 

(C) 

(B) 

Q. 15 The circuit shown is a



(A) low pass filter with $f_{3dB} = \frac{1}{(R_1 + R_2)C}$ rad /s

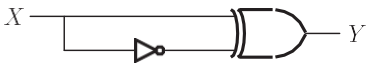
(B) high pass filter with $f_{3dB} = \frac{1}{R_1 C}$ rad /s

(C) low pass filter with $f_{3dB} = \frac{1}{R_1 C}$ rad /s

(D) high pass filter with $f_{3dB} = \frac{1}{(R_1 + R_2)C}$ rad /s

YEAR 2011 ONE MARK

Q. 16 The output Y of the logic circuit given below is



(A) 1 (B) 0

(C) X (D) X

Q. 17 A low-pass filter with a cut-off frequency of 30 Hz is cascaded with a high pass filter with a cut-off frequency of 20 Hz. The resultant system of filters will function as

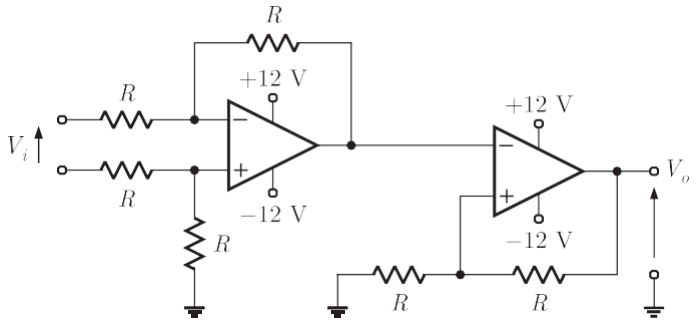
(A) an all – pass filter

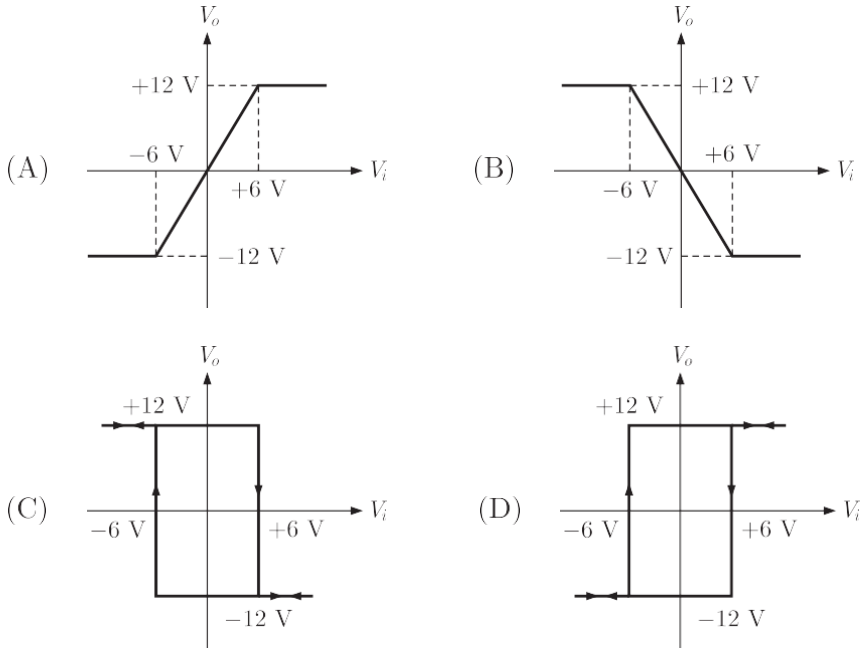
(B) an all – stop filter

(C) an band stop (band-reject) filter

(D) a band – pass filter

Q. 18 The CORRECT transfer characteristic is





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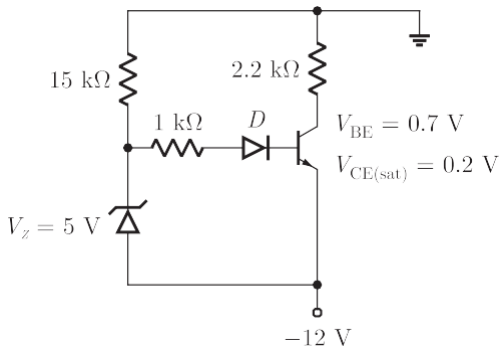
Q. 19 The transistor used in the circuit shown below has a b of 30 and I_{CBO} is negligible

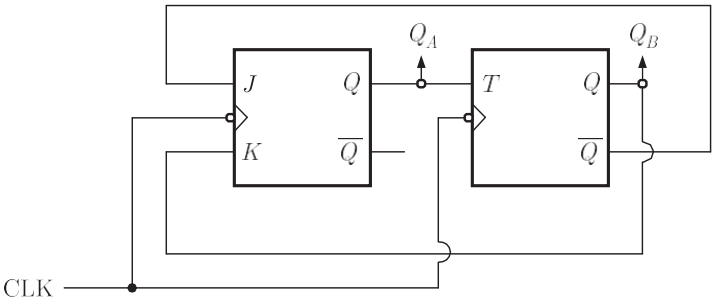


If the forward voltage drop of diode is 0.7 V, then the current through collector will be

(A) 168 mA (B) 108 mA

(C) 20.54 mA (D) 5.36 mA

Q. 20 A two bit counter circuit is shown below



It the state $Q_A\,Q_B$ of the counter at the clock time t_n is '10' then the state $Q_A\,Q_B$ of the counter at $t_n + 3$ (after three clock cycles) will be

(A) 00 (B) 01

(C) 10 (D) 11

Q. 21 A portion of the main program to call a subroutine SUB in an 8085 environment is given below.

```
LXI D, DISP
LP :  CALL SUB
LP + 3
```

It is desired that control be returned to LP + DISP + 3 when the RET instruction is executed in the subroutine. The set of instructions that precede the RET instruction in the subroutine are

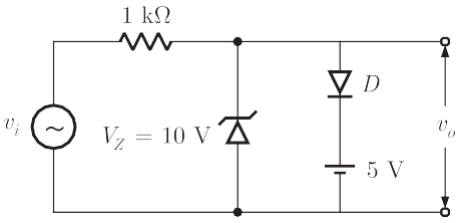
(A)
```
POP  D
DAD H
PUSH D
```

(B)
```
POP  H
DAD  D
INX  H
INX  H
INX  H
PUSH H
```

(C)
```
POP  H
DAD D
PUSH H
```

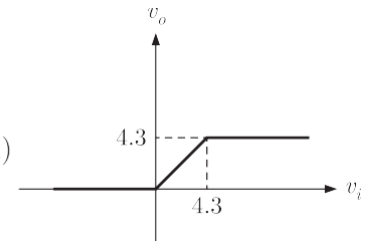
(D)
```
XTHL
INX  D
INX  D
INX  D
XTHL
```

Q. 22 A clipper circuit is shown below.

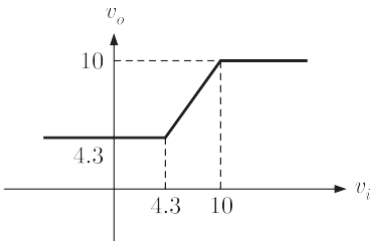


Assuming forward voltage drops of the diodes to be 0.7 V, the input-output transfer characteristics of the circuit is

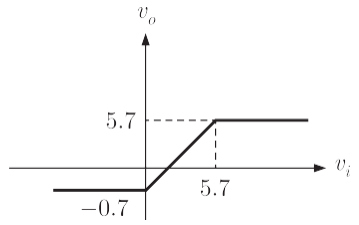
(A)



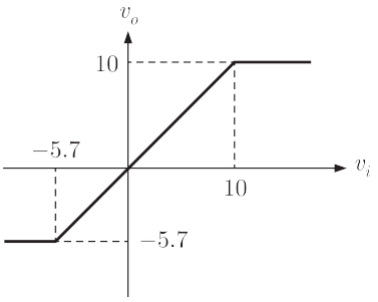
(B)



(C)



(D)



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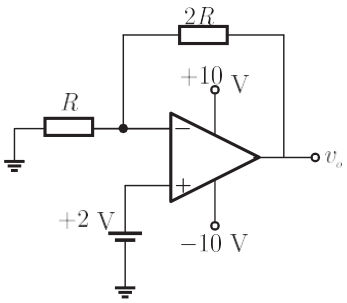
Q. 23 Given that the op-amp is ideal, the output voltage v_o is



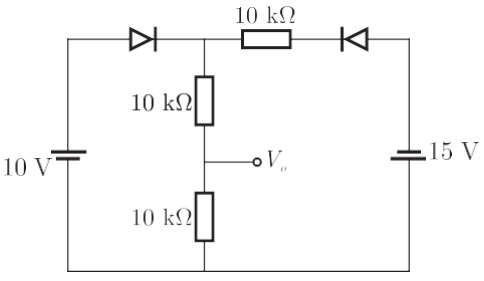
(A) 4 V

(B) 6 V

(C) 7.5 V

(D) 12.12 V

Q. 24 Assuming that the diodes in the given circuit are ideal, the voltage V_0 is



(A) 4 V

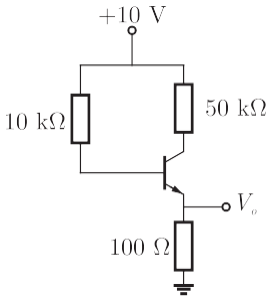
(B) 5 V

(C) 7.5 V

(D) 12.12 V

YEAR 2010 TWO MARKS

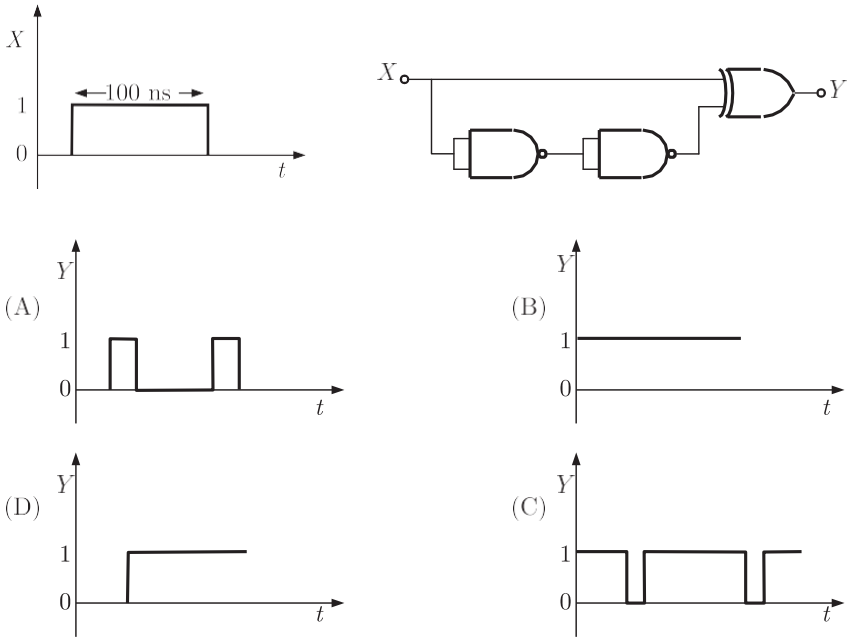
Q. 25 The transistor circuit shown uses a silicon transistor with $V_{BE} = 0.7, I_C \approx I_E$ and a dc current gain of 100. The value of V_0 is



(A) 4.65 V (B) 5 V

(C) 6.3 V (D) 7.23 V

Q. 26 The TTL circuit shown in the figure is fed with thewaveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit is



Statement For Linked Answer Questions: 27 and 28

The following Karnaugh map represents a function F .

F : X \ YZ	00	01	11	10
0	1	1	1	0
1	0	0	1	0

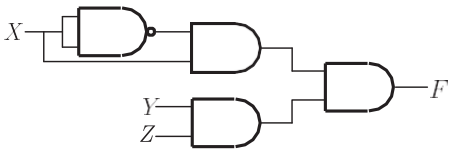
Q. 27 A minimized form of the function F is

(A) $F = XY + YZ$ *(B)* $F = XY + YZ$

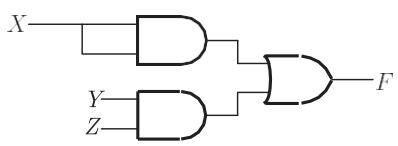
(C) $F = XY + YZ$ *(D)* $F = XY + Y\ Z$

Q. 28 Which of the following circuits is a realization of the above function F ?

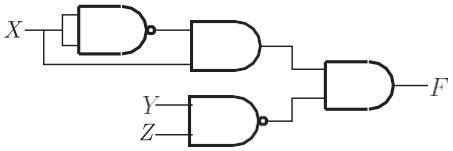
(A)



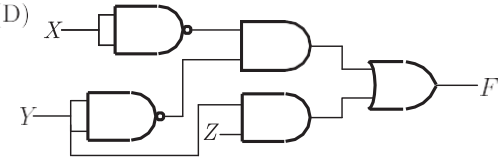
(B)



(C)



(D)



Q. 29 When a "CALL Addr" instruction is executed, the CPU carries out the following sequential operations internally :

Note: (R) means content of register R
((R)) means content of memory location pointed to by R.
PC means Program Counter
SP means Stack Pointer

(A) (SP) incremented
(PC) ← Addr
((SP)) ← (PC)

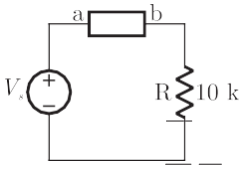
(B) (PC) ← Addr
((SP)) ← (PC)
(SP) incremented

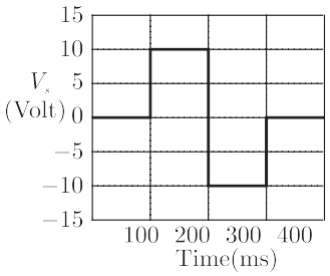
(C) (PC) ← Addr
(SP) incremented
((SP)) ← (PC)

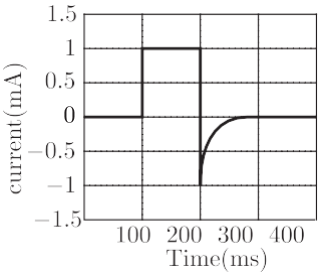
(D) ((SP)) ← (PC)
(SP) incremented
(PC) ← Addr

YEAR 2009 ONE MARK

Q. 30 The following circuit has a source voltage V_S as shown in the graph. The current through the circuit is also shown.



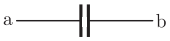




The element connected between *a* and *b* could be

(A)

(B)



(C)

(D)

Q. 31 The increasing order of speed of data access for the following device is

(I) Cache Memory

(II) CD-ROM

(III) Dynamic RAM

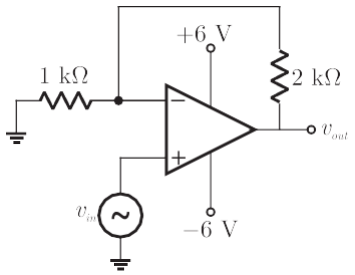
(IV) Processor Registers

(V) Magnetic Tape

(A) (V), (II), (III), (IV), (I) (B) (V), (II), (III), (I), (IV)

(C) (II), (I), (III), (IV), (V) (D) (V), (II), (I), (III), (IV)

Q. 32 The nature of feedback in the op-amp circuit shown is



(A) Current-Current feedback (B) Voltage-Voltage feedback

(C) Current-Voltage feedback (D) Voltage-Current feedback

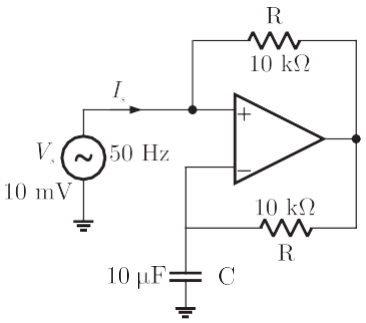
Q. 33 The complete set of only those Logic Gates designated as Universal Gates is

(A) NOT, OR and AND Gates (B) XNOR, NOR and NAND Gates

(C) NOR and NAND Gates (D) XOR, NOR and NAND Gates

YEAR 2009 TWO MARKS

Q. 34 The following circuit has R = 10 kW, C = 10 mF. The input voltage is a sinusoidal at 50 Hz with an rms value of 10 V. Under ideal conditions, the current I_s from the source is



(A) 10p mA leading by 90°
(B) 20p mA leading by 90°
(C) 10p mA leading by 90°
(D) 10p mA lagging by 90°

Q. 35 Transformer and emitter follower can both be used for impedance matching at the output of an audio amplifier. The basic relationship between the input power P_{in} and output power P_{out} in both the cases is

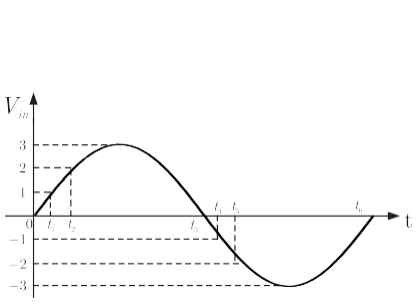
(A) $P_{in} = P_{out}$ for both transformer and emitter follower
(B) $P_{in} > P_{out}$ for both transformer and emitter follower
(C) $P_{in} < P_{out}$ for transformer and $P_{in} = P_{out}$ for emitter follower
(D) $P_{in} = P_{out}$ for transformer and $P_{in} < P_{out}$ for emitter follower

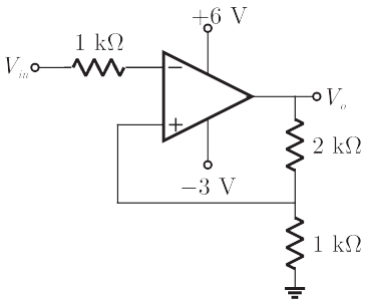
Q. 36 In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become

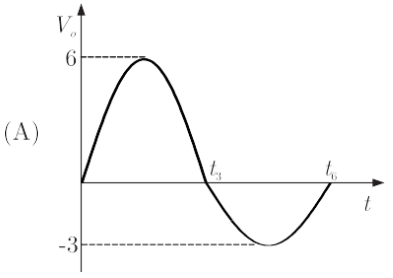
```
XRA  A
MVI  B, F0 H
SUB  B
```

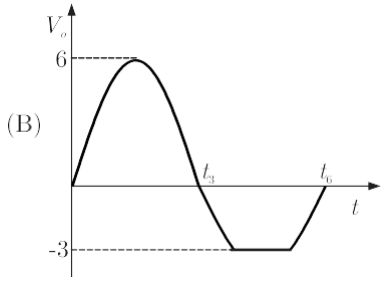
(A) 01 H
(B) 0F H
(C) F0 H
(D) 10 H

Q. 37 An ideal op-amp circuit and its input wave form as shown in the figures. The output waveform of this circuit will be

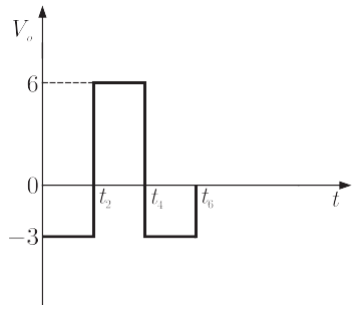




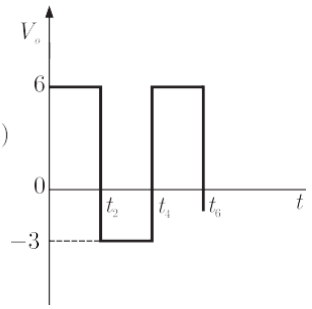




(C)



(D)

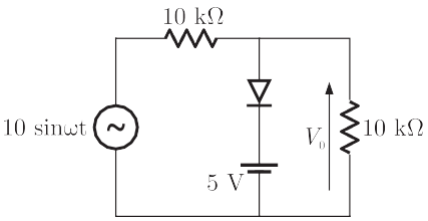


YEAR 2008 ONE MARK

Q. 38 The equivalent circuits of a diode, during forward biased and reverse biased conditions, are shown in the figure.

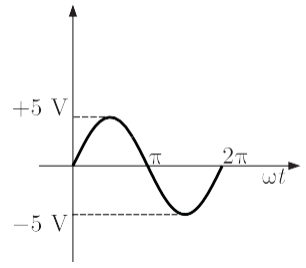
(I)

(II)

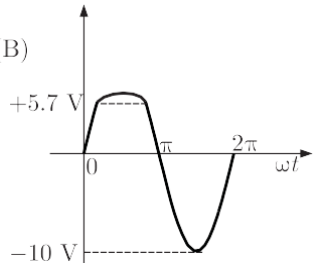


If such a diode is used in clipper circuit of figure given above, the output voltage V_0 of the circuit will be

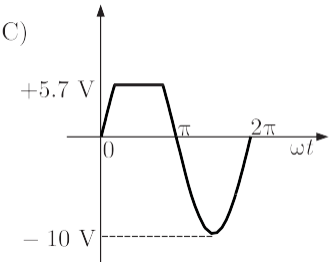
(A)



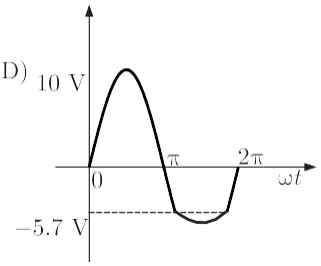
(B)



(C)

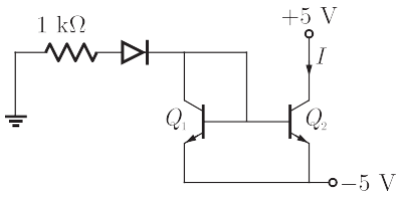


(D)



YEAR 2008 TWO MARKS

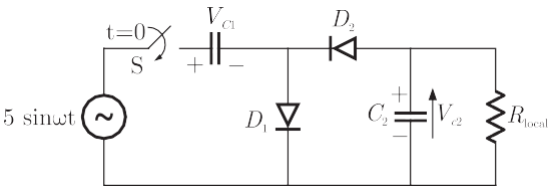
Q. 39 Two perfectly matched silicon transistor are connected as shown in the figure assuming the *b* of the transistors to be very high and the forward voltage drop in diodes to be 0.7 V, the value of current *I* is



(A) 0 mA (B) 3.6 mA

(C) 4.3 mA (D) 5.7 mA

Q. 40 In the voltage doubler circuit shown in the figure, the switch *S* ' is closed at $t = 0$. Assuming diodes D_1 and D_2 to be ideal, load resistance to be infinite and initial capacitor voltages to be zero. The steady state voltage across capacitor C_1 and C_2 will be



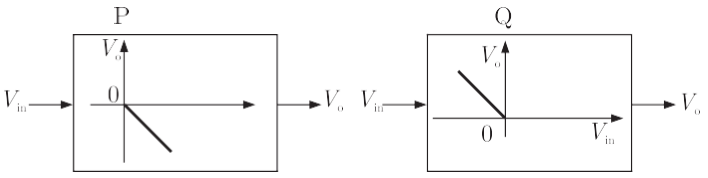
(A) V_{c1} = 10 V, V_{c2} = 5 V

(B) V_{c1} = 10 V, V_{c2} = – 5 V

(C) V_{c1} = 5 V, V_{c2} = 10 V

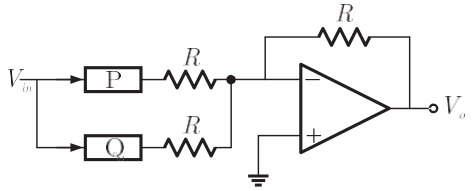
(D) V_{c1} = 5 V, V_{c2} = – 10 V

Q. 41 The block diagrams of two of half wave rectifiers are shown in the figure. The transfer characteristics of the rectifiers are also shown within the block.

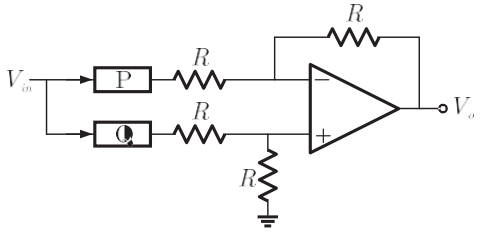


It is desired to make full wave rectifier using above two half-wave rectifiers. The resultants circuit will be

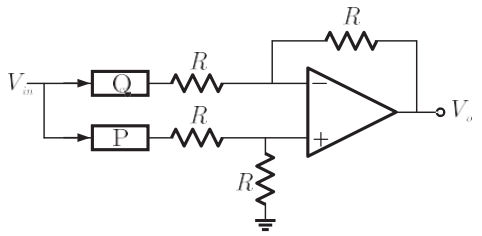
(A)



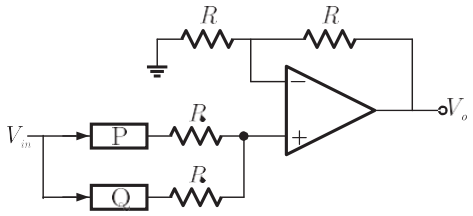
(B)



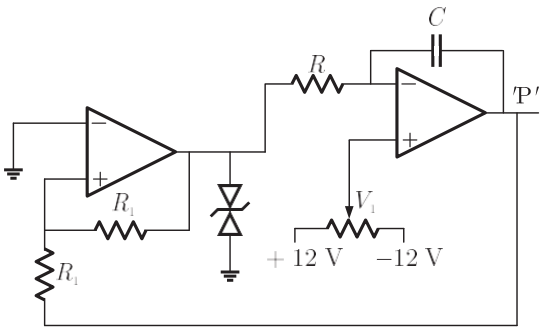
(C)



(D)

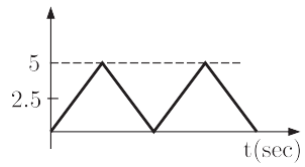


Q. 42 A waveform generator circuit using OPAMPs is shown in the figure. It produces a triangular wave at point 'P' with a peak to peak voltage of 5 V for $V_i = 0$ V.

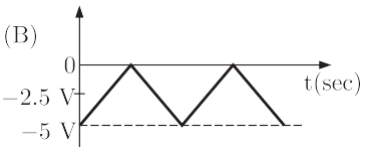


If the voltage V_i is made +2.5 V, the voltage waveform at point 'P' will become

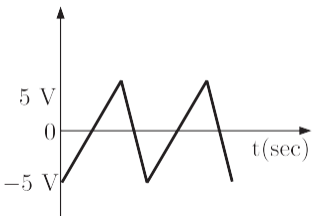
(A)



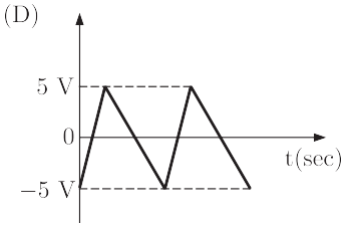
(B)



(C)

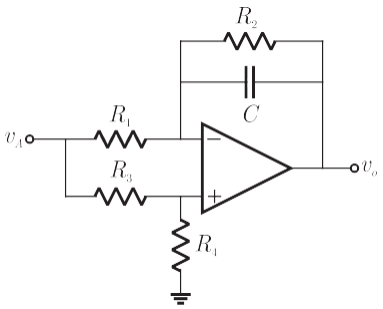


(D)



Statement for Linked Answer Questions 43 and 44

A general filter circuit is shown in the figure :



Q. 43 If $R_1 = R_2 = R_A$ and $R_3 = R_4 = R_B$, the circuit acts as a

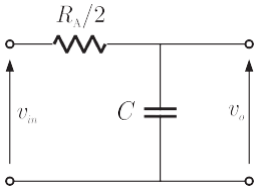
(A) all pass filter

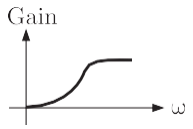
(B) band pass filter

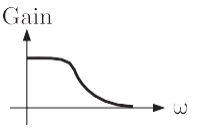
(C) high pass filter

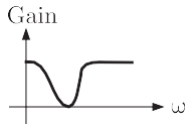
(D) low pass filter

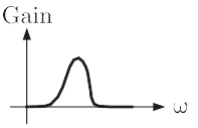
Q. 44 The output of the this filter is given to the circuit in figure : The gain v / s frequency characteristic of the output (v_o) will be



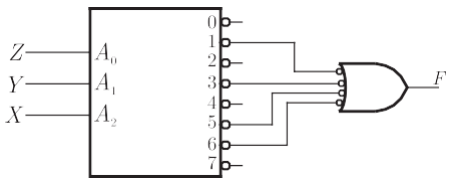
(A) 

(B) 

(C) 

(D) 

Q. 45 A 3-line to 8-line decoder, with active low outputs, is used to implement a 3-variable Boolean function as shown in the figure



The simplified form of Boolean function $F(A, B, C)$ implemented in 'Product of Sum' form will be

(A) $(X + Z)(X + Y + Z)(Y + Z)$

(B) $(X + Z)(X + Y + Z)(Y + Z)$

(C) $(X + Y + Z)(X + Y + Z)(X + Y + Z)(X + Y + Z)$

(D) $(X + Y + Z)(X + Y + Z)(X + Y + Z)(X + Y + Z)$

Q. 46 The content of some of the memory location in an 8085 accumulator based system are given below

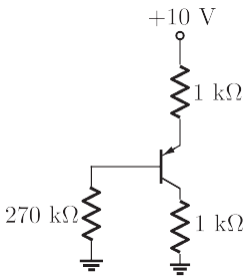
Address	Content
g	g
26FE	00
26FF	01
2700	02
2701	03
2702	04
g	g

The content of stack (SP), program counter (PC) and (H,L) are 2700 H, 2100 H and 0000 H respectively. When the following sequence of instruction are executed. 2100 H: DAD SP
2101 H: PCHL
the content of (SP) and (PC) at the end of execution will be

(A) PC = 2102 H, SP = 2700 H (B) PC = 2700 H,SP = 2700 H
(C) PC = 2800 H, SP = 26FE H (D) PC = 2A02 H,SP = 2702 H

YEAR 2007 ONE MARK

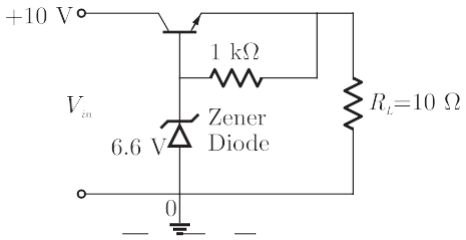
Q. 47 The common emitter forward current gain of the transistor shown is b_F = 100



The transistor is operating in

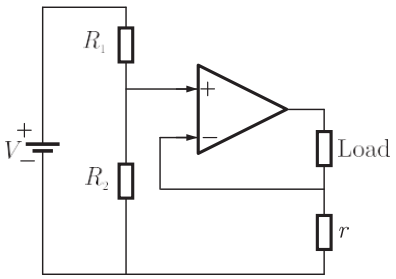
(A) Saturation region (B) Cutoff region
(C) Reverse active region (D) Forward active region

Q. 48 The three-terminal linear voltage regulator is connected to a 10 W load resistor as shown in the figure. If V_{in} is 10 V, what is the power dissipated in the transistor ?



(A) 0.6 W (B) 2.4 W
(C) 4.2 W (D) 5.4 W

Q. 49 The circuit shown in the figure is



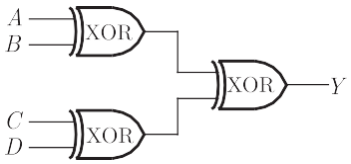
(A) a voltage source with voltage $\frac{rV}{R_1 < R_2}$

(B) a voltage source with voltage $\frac{r < R_2}{R_1} V$

(C) a current source with current $c\frac{r < R_2}{R_1 + R_2}m\frac{V}{r}$

(D) a current source with current $c\frac{R_2}{R_1 + R_2}m\frac{V}{r}$

Q. 50 *A*, *B*, *C* and *D* are input, and *Y* is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum *S* of *A*, *B*, *C*, *D* and *Y* is correct ?



(A) *S* is always with zero or odd

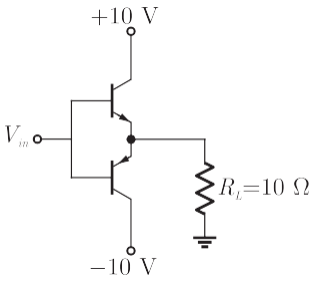
(B) *S* is always either zero or even

(C) *S* = 1 only if the sum of *A*, *B*, *C* and *D* is even

(D) *S* = 1 only if the sum of *A*, *B*, *C* and *D* is odd

YEAR 2007 TWO MARKS

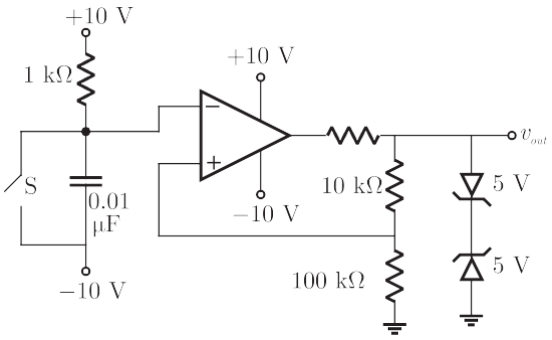
Q. 51 The input signal V_{in} shown in the figure is a 1 kHz square wave voltage that alternates between $+7$ V and -7 V with a 50% duty cycle. Both transistor have the same current gain which is large. The circuit delivers power to the load resistor R_L. What is the efficiency of this circuit for the given input ? choose the closest answer.



(A) 46% (B) 55%

(C) 63% (D) 92%

Q. 52 The switch S in the circuit of the figure is initially closed, it is opened at time $t = 0$. You may neglect the zener diode forward voltage drops. What is the behavior of v_{out} for $t > 0$?



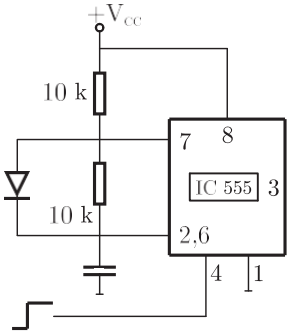
(A) It makes a transition from -5 V to $+5$ V at $t = 12.98$ ms

(B) It makes a transition from -5 V to $+5$ V at $t = 2.57$ ms

(C) It makes a transition from + 5V to -5 V at $t = 12.98$ ms

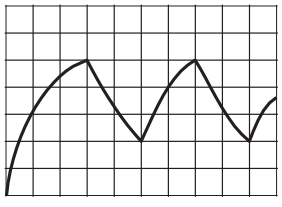
(D) It makes a transition from + 5V to -5 V at $t = 2.57$ ms

Q. 53 IC 555 in the adjacent figure is configured as an astable multi-vibrator. It is enabled to to oscillate at $t = 0$ by applying a high input to pin 4. The pin description is : 1 and 8-supply; 2-trigger; 4-reset; 6-threshold 7-discharge. The waveform appearing across the capacitor starting from $t = 0$, as observed on a storage CRO is

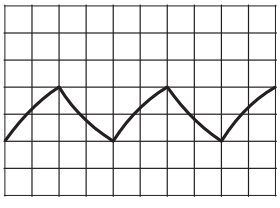


diode is forward biased during charging

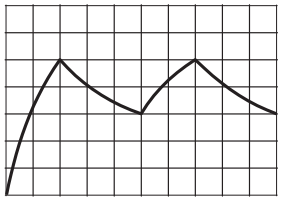
(A)



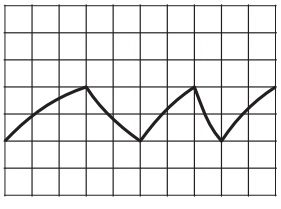
(B)



(C)



(D)



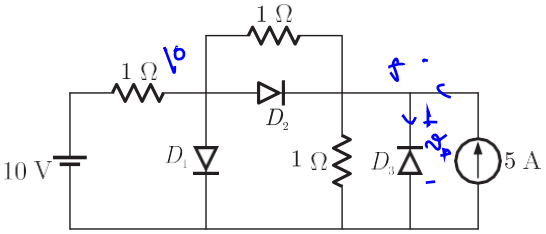
Q. 54 The Octal equivalent of HEX and number AB.CD is

(A) 253.314 (B) 253.632

(C) 526.314 (D) 526.632

YEAR 2006 ONE MARK

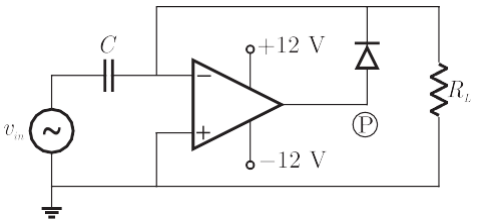
Q. 55 What are the states of the three ideal diodes of the circuit shown in figure ?

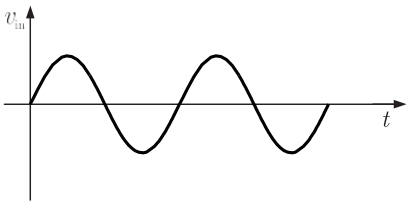


(A) D_1 ON, D_2 OFF, D_3 OFF (B) D_1 OFF, D_2 ON, D_3 OFF

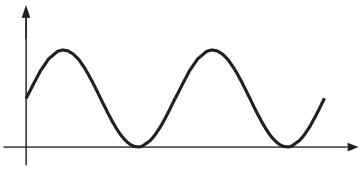
(C) D_1 ON, D_2 OFF , D_3 ON (D) D_1 OFF, D_2 ON, D_3 ON

Q. 56 For a given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure will be

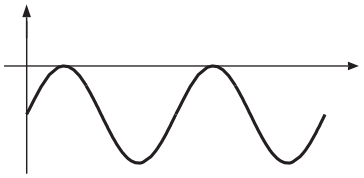




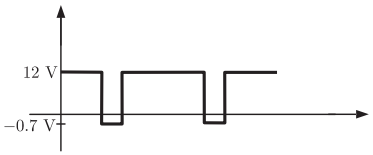
(A)



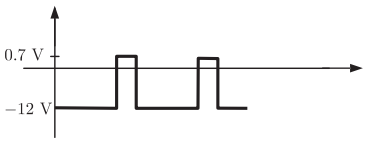
(B)



(C)

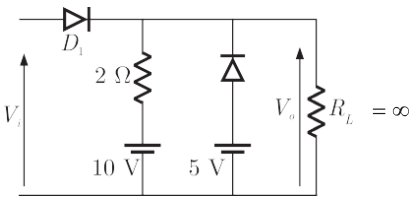


(D)

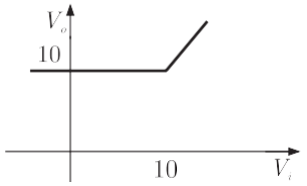


YEAR 2006 TWO MARKS

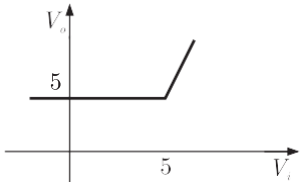
Q. 57 Assuming the diodes D_1 and D_2 of the circuit shown in figure to be ideal ones, the transfer characteristics of the circuit will be



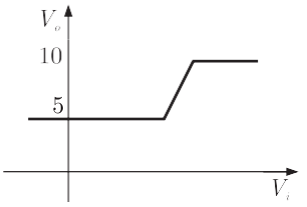
(A)



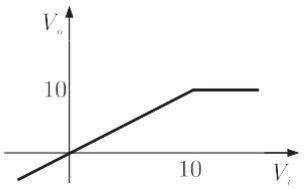
(B)



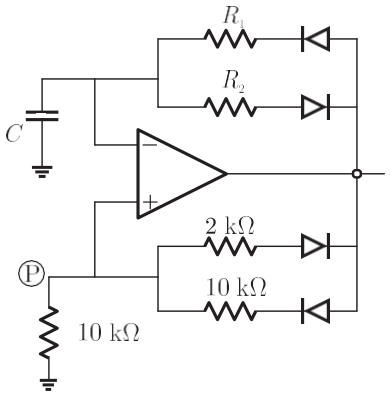
(C)



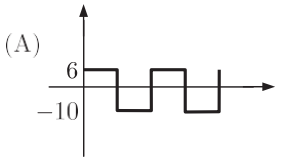
(D)



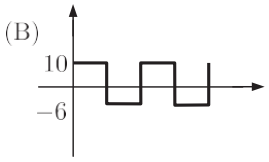
Q. 58 A relaxation oscillator is made using OPAMP as shown in figure. The supply voltages of the OPAMP are ±12 V. The voltage waveform at point P will be



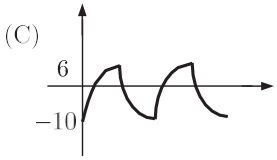
(A)



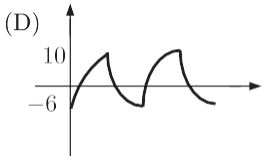
(B)



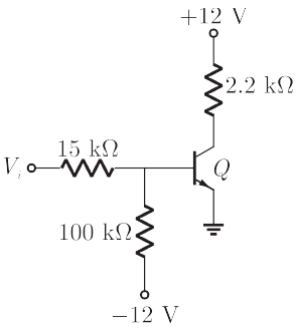
(C)



(D)



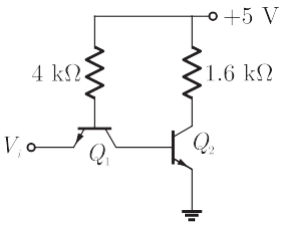
Q. 59 Consider the circuit shown in figure. If the *b* of the transistor is 30 and I_{CBO} is 20 mA and the input voltage is +5 V, the transistor would be operating in



(A) saturation region (B) active region

(C) breakdown region (D) cut-off region

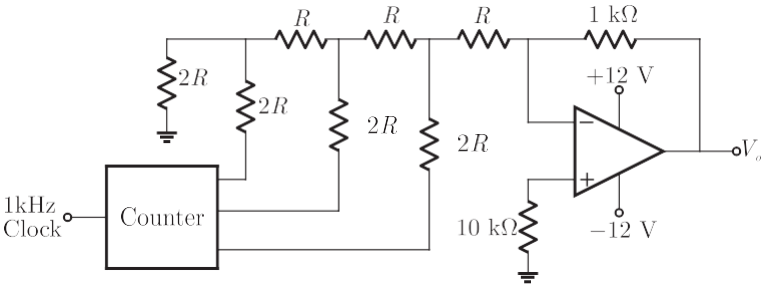
Q. 60 A TTL NOT gate circuit is shown in figure. Assuming V_{BE} = 0.7 V of both the transistors, if V_i = 3.0 V, then the states of the two transistors will be

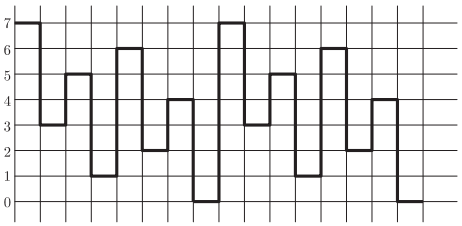


(A) Q_1 ON and Q_2 OFF (B) Q_1 reverse ON and Q_2 OFF

(C) Q_1 reverse ON and Q_2 ON(D) Q_1 OFF and Q_2 reverse ON

Q. 61 A student has made a 3-bit binary down counter and connected to the R-$2R$ ladder type DAC, [Gain $= (-1\,\text{kW}/2R)$] as shown in figure to generate a staircase waveform. The output achieved is different as shown in figure. What could be the possible cause of this error ?





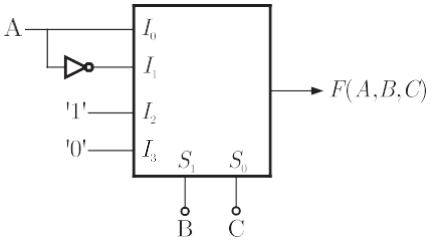
(A) The resistance values are incorrect option.

(B) The counter is not working properly

(C) The connection from the counter of DAC is not proper

(D) The R and 2R resistance are interchanged

Q. 62 A 4 # 1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function $F(A, B, C)$ implemented is



(A) $F(A,B,C) = \Sigma(1,2,4,6)$ (B) $F(A,B,C) = \Sigma(1,2,6)$

(C) $F(A,B,C) = \Sigma(2,4,5,6)$ (D) $F(A,B,C) = \Sigma(1,5,6)$

Q. 63 A software delay subroutine is written as given below :

```
DELAY :  MVI   H, 255D
         MVI   L, 255D
LOOP :   DCR   L
         JNZ   LOOP
         DCR   H
         JNZ   LOOP
```

How many times DCR L instruction will be executed ?

(A) 255 (B) 510

(C) 65025 (D) 65279

Q. 64 In an 8085 A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D,E) register pair and store the result in same location. The sequence of instruction is

(A) XCHG
INR M

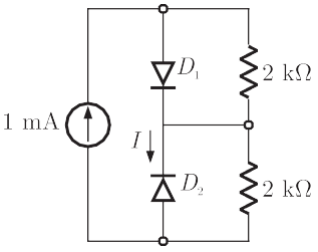
(B) XCHG
INX H

(C) INX D
XCHG

(D) INR M
XCHG

YEAR 2005 ONE MARK

Q. 65 Assume that D_1 and D_2 in figure are ideal diodes. The value of current is



(A) 0 mA (B) 0.5 mA

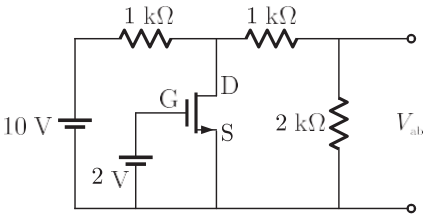
(C) 1 mA (D) 2 mA

Q. 66 The 8085 assembly language instruction that stores the content of H and L register into the memory locations 2050_H and 2051_H, respectively is

(A) SPHL 2050_H (B) SPHL 2051_H

(C) SHLD 2050_H (D) STAX 2050_H

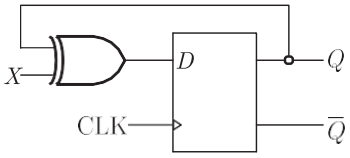
Q. 67 Assume that the N-channel MOSFET shown in the figure is ideal, and that its threshold voltage is +1.0 V the voltage V_{ab} between nodes *a* and *b* is



(A) 5 V (B) 2 V

(C) 1 V (D) 0 V

Q. 68 The digital circuit shown in the figure works as



(A) JK flip-flop

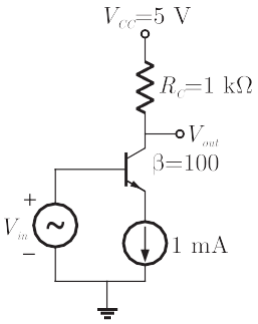
(B) Clocked RS flip-flop

(C) T flip-flop

(D) Ring counter

YEAR 2005 TWO MARKS

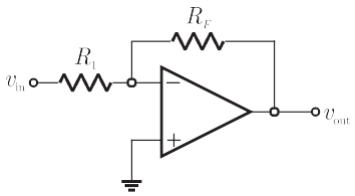
Q. 69 The common emitter amplifier shown in the figure is biased using a 1 mA ideal current source. The approximate base current value is



(A) 0 *m*A (B) 10 *m*A

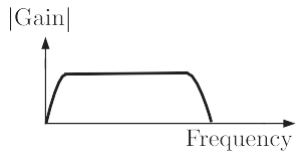
(C) 100 *m*A (D) 1000 *m*A

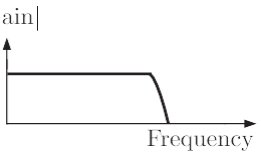
Q. 70 Consider the inverting amplifier, using an ideal operational amplifier shown in the figure. The designer wishes to realize the input resistance seen by the small-signal source to be as large as possible, while keeping the voltage gain between −10 and −25. The upper limit on R_F is 1 MW. The value of R_1 should be

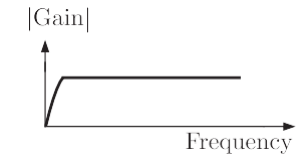


(A) Infinity
(B) 1 MW
(C) 100 kW
(D) 40 kW

Q. 71 The typical frequency response of a two-stage direct coupled voltage amplifier is as shown in figure

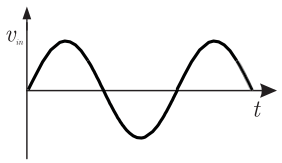
(A) 

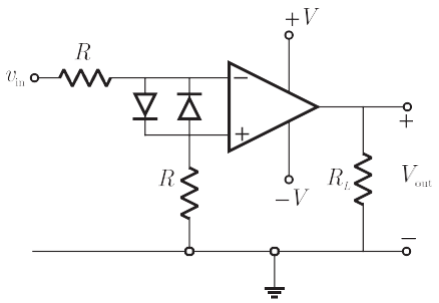
(B) 

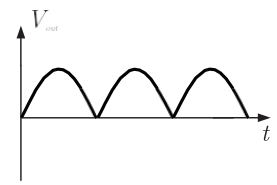
(C) 

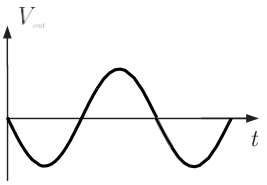
(D) 

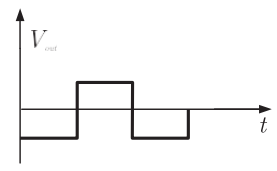
Q. 72 In the given figure, if the input is a sinusoidal signal, the output will appear as shown

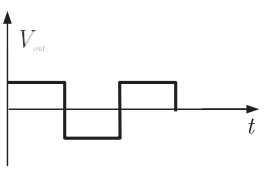




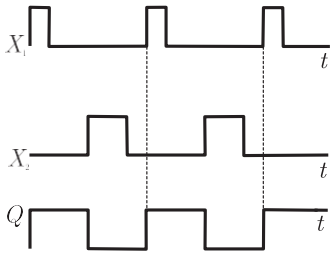
(A) 

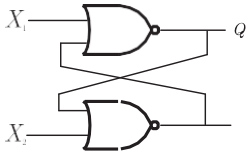
(B) 

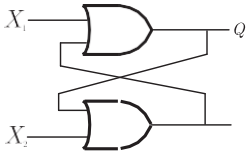
(C) 

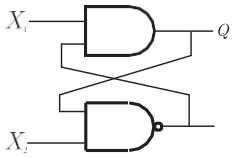
(D) 

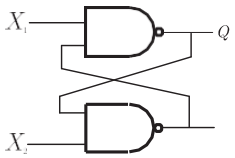
Q. 73 Select the circuit which will produce the given output Q for the input signals X_1 and X_2 given in the figure



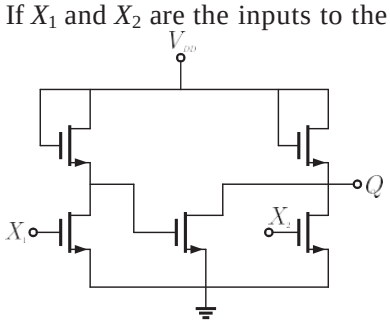
(A) 

(B) 

(C) 

(D) 

Q. 74 If X_1 and X_2 are the inputs to the circuit shown in the figure, the output Q is



(A) $\overline{X_1 + X_2}$

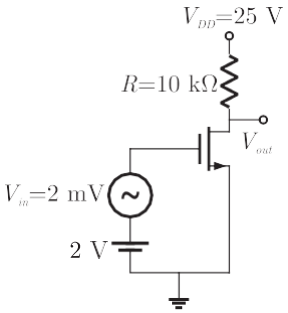
(B) $\overline{X_1 : X_2}$

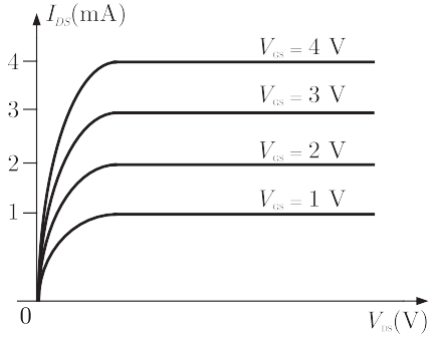
(C) $\overline{X_1} : X_2$

(D) $X_1 : \overline{X_2}$

Common Data For Q. 75 and 76

Assume that the threshold voltage of the N-channel MOSFET shown in figure is + 0.75 V. The output characteristics of the MOSFET are also shown





Q. 75 The transconductance of the MOSFET is

(A) 0.75 ms

(B) 1 ms

(C) 2 ms

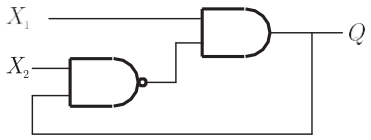
(D) 10 ms

Q. 76 The voltage gain of the amplifier is

(A) +5 (B) −7.5

(C) +10 (D) −10

Q. 77 In the figure, as long as $X_1 = 1$ and $X_2 = 1$, the output Q remains



(A) at 1

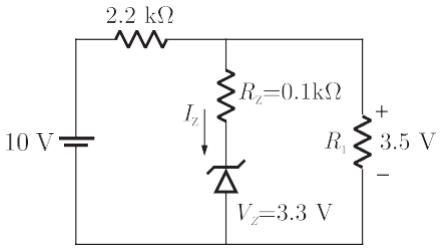
(B) at 0

(C) at its initial value

(D) unstable

YEAR 2004 ONE MARK

Q. 78 The current through the Zener diode in figure is



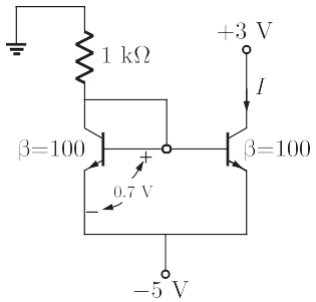
(A) 33 mA

(B) 3.3 mA

(C) 2 mA

(D) 0 mA

Q. 79 Two perfectly matched silicon transistor are connected as shown in figure. The value of the current I is



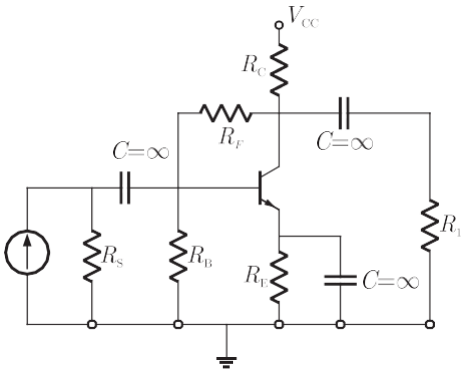
(A) 0 mA

(B) 2.3 mA

(C) 4.3 mA

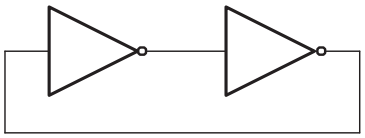
(D) 7.3 mA

Q. 80 The feedback used in the circuit shown in figure can be classified as



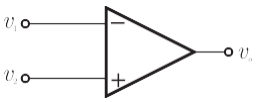
(A) shunt-series feedback
(B) shunt-shunt feedback
(C) series-shunt feedback
(D) series-series feedback

Q. 81 The digital circuit using two inverters shown in figure will act as



(A) a bistable multi-vibrator
(B) an astable multi-vibrator
(C) a monostable multi-vibrator
(D) an oscillator

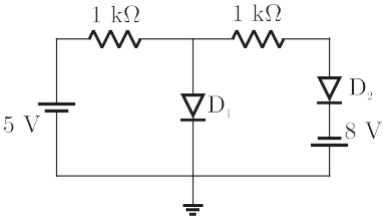
Q. 82 The voltage comparator shown in figure can be used in the analog-to-digital conversion as



(A) a 1-bit quantizer
(B) a 2-bit quantizer
(C) a 4-bit quantizer
(D) a 8-bit quantizer

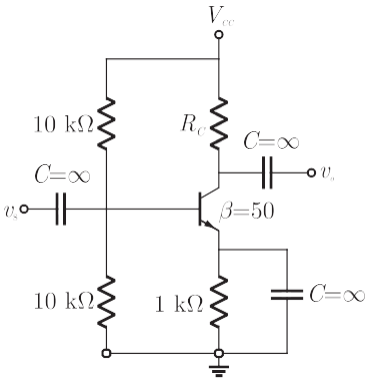
YEAR 2004 TWO MARKS

Q. 83 Assuming that the diodes are ideal in figure, the current in diode D_1 is



(A) 9 mA
(B) 5 mA
(C) 0 mA
(D) −3 mA

Q. 84 The trans-conductance g_m of the transistor shown in figure is 10 mS. The value of the input resistance R_{in} is



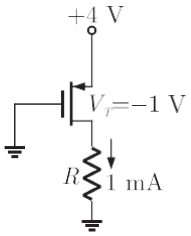
(A) 10.0 kW

(B) 8.3 kW

(C) 5.0 kW

(D) 2.5 kW

Q. 85 The value of *R* for which the PMOS transistor in figure will be biased in linear region is



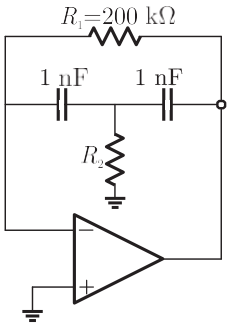
(A) 220 W

(B) 470 W

(C) 680 W

(D) 1200 W

Q. 86 In the active filter circuit shown in figure, if Q = 1, a pair of poles will be realized with w_0 equal to



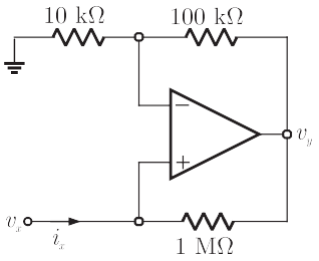
(A) 1000 rad/s

(B) 100 rad / s

(C) 10 rad/s

(D) 1 rad / s

Q. 87 The input resistance $R_{in} = v_x / i_x$ of the circuit in figure is



(A) +100 kW (B) −100 kW

(C) +1 MW (D) −1 MW

Q. 88 The simplified form of the Boolean expression $Y = (A\overline{\ }BC + D)(A\overline{\ }D + B\overline{\ }\overline{C})$ can be written as

(A) $\overline{A}\,\$\,D + \overline{B}\,\$\,\overline{C}\,\$\,D$ (B) $AD + B\,\$\,\overline{C}\,\$\,D$

(C) $(\overline{A} + D)(\overline{B}\,\$\,C + \overline{D})$ (D) $A\,\$\,\overline{D} + BC\$\,\overline{D}$

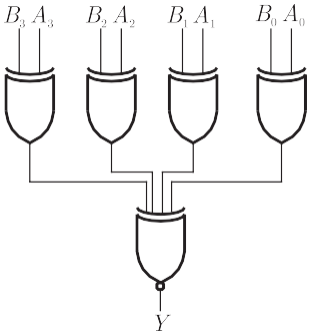
Q. 89 If the following program is executed in a microprocessor, the number of instruction cycle it will take from START to HALT is

```
START   MVI A, 14H  ;   Move 14 H to register A
SHIFT   RLC         ;   Rotate left without carry
        JNZ SHIFT   ;   Jump on non-zero to SHIFT
        HALT
```

(A) 4 (B) 8

(C) 13 (D) 16

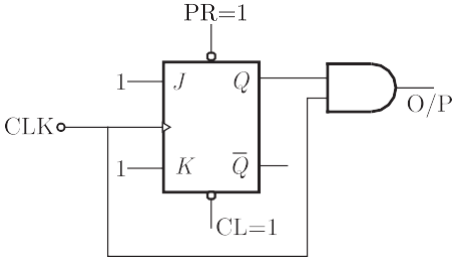
Q. 90 A digit circuit which compares two numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ is shown in figure. To get output $Y = 0$, choose one pair of correct input numbers.



(A) 1010, 1010 (B) 0101, 0101

(C) 0010, 0010 (D) 1010, 1011

Q. 91 The digital circuit shown in figure generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.



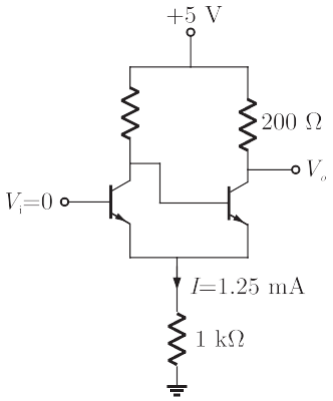
(A)

(B)

(C)

(D)

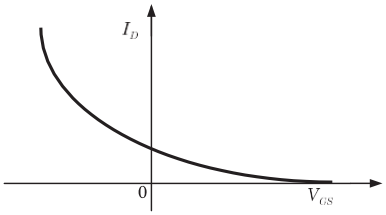
Q. 92 In the Schmitt trigger circuit shown in figure, if $V_{CE\,(sat)} = 0.1$ V, the output logic low level (V_{OL}) is



(A) 1.25 V (B) 1.35 V
(C) 2.50 V (D) 5.00 V

YEAR 2003 **ONE MARK**

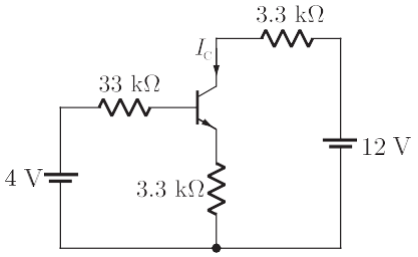
Q. 93 The variation of drain current with gate-to-source voltage ($I_D - V_{GS}$ characteristic) of a MOSFET is shown in figure. The MOSFET is



(A) an n-channel depletion mode device
(B) an n-channel enhancement mode device
(C) an p-channel depletion mode device

(D) an p-channel enhancement mode device

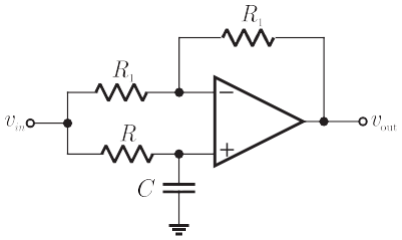
Q. 94 In the circuit of figure, assume that the transistor has h_{fe} = 99 and V_{BE} = 0.7 V. The value of collector current I_C of the transistor is approximately



(A) [3.3 / 3.3] mA (B) [3.3/(3.3+3.3)] mA

(C) [3.3 / .33] mA (D) [3.3(33 + 3.3)] mA

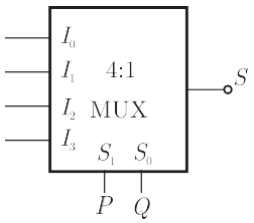
Q. 95 For the circuit of figure with an ideal operational amplifier, the maximum phase shift of the output v_{out} with reference to the input v_{in} is



(A) 0c (B) −90c

(C) +90c (D) !180c

Q. 96 Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in} . Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S ?



(A) $I_0 = I_1 = C_{in}; I_2 = I_3 = C_{in}$ *(B)* $I_0 = I_1 = C_{in}; I_2 = I_3 = C_{in}$

(C) $I_0 = I_3 = C_{in}; I_1 = I_2 = C_{in}$ *(D)* $I_0 = I_3 = C_{in}; I_1 = I_2 = C_{in}$

Q. 97 When a program is being executed in an 8085 microprocessor, its Program Counter contains

(A) the number of instructions in the current program that have already been executed

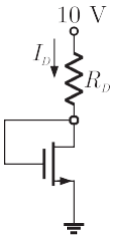
(B) the total number of instructions in the program being executed.

(C) the memory address of the instruction that is being currently executed

(D) the memory address of the instruction that is to be executed next

YEAR 2003 TWO MARKS

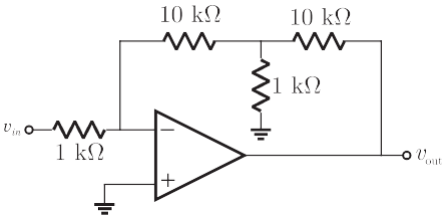
Q. 98 For the n-channel enhancement MOSFET shown in figure, the threshold voltage V_{th} = 2 V. The drain current I_D of the MOSFET is 4 mA when the drain resistance R_D is 1 kW.If the value of R_D is increased to 4 kW, drain current I_D will become



(A) 2.8 mA (B) 2.0 mA

(C) 1.4 mA (D) 1.0 mA

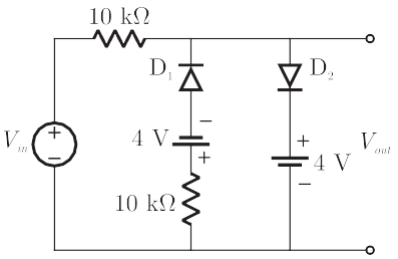
Q. 99 Assuming the operational amplifier to be ideal, the gain v_{out} / v_{in} for the circuit shown in figure is



(A) −1 (B) −20

(C) −100 (D) −120

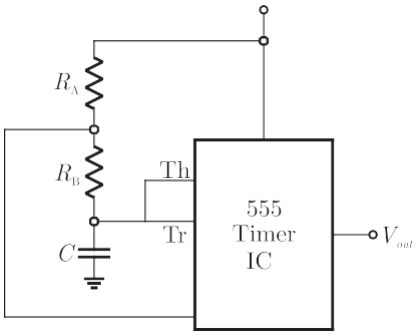
Q. 100 A voltage signal 10 sin *wt* is applied to the circuit with ideal diodes, as shown in figure, The maximum, and minimum values of the output waveform V_{out} of the circuit are respectively



(A) +10 V and −10 V (B) + 4 V and −4 V

(C) + 7 V and −4 V (D) + 4 V and −7 V

Q. 101 The circuit of figure shows a 555 Timer IC connected as an astable multi-vibrator. The value of the capacitor *C* is 10 nF. The values of the resistors R_A and R_B for a frequency of 10 kHz and a duty cycle of 0.75 for the output voltagewaveform are



(A) R_A = 3.62 kW, R_B = 3.62 kW (B) R_A = 3.62 kW, R_B = 7.25 kW

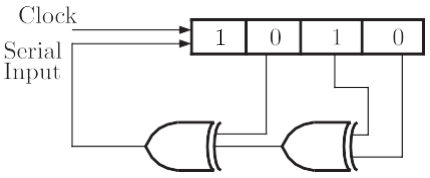
(C) R_A = 7.25 kW, R_B = 3.62 kW (D) R_A = 7.25 kW, R_B = 7.25 kW

Q. 102 The boolean expression $X\overline{Y}Z + \overline{X}Y\overline{Z} + XY\overline{Z} + X\overline{Y}\overline{Z} + XYZ$ can be simplified to

(A) $X\overline{Z} + \overline{X}Z + YZ$ (B) $XY + \overline{Y}Z + Y\overline{Z}$

(C) $\overline{X}Y + YZ + XZ$ (D) $\overline{XY} + Y\overline{Z} + \overline{X}Z$

Q. 103 The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again ?



(A) 3 (B) 7

(C) 11 (D) 15

Q. 104 An X-Y flip-flop, whose Characteristic Table is given below is to be implemented using a J-K flip flop

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q}_n$
1	1	0

(A) $J = X, K = Y$ (B) $J = X, K = Y$

(C) $J = Y, K = X$ (D) $J = Y, K = X$

Q. 105 A memory system has a total of 8 memory chips each with 12 address lines and 4 data lines, The total size of the memory system is

(A) 16 kbytes (B) 32 kbytes

(C) 48 kbytes (D) 64 kbytes

Q. 106 The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

```
LXI   H, 1FFE
MOV B,  M
INR   L
MOV A, M
ADD B
INR   L
MOV M, A
XOR A
```

On completion of the execution of the program, the result of addition is found

(A) in the register A

(B) at the memory address 1000

(C) at the memory address 1F00

(D) at the memory address 2000

****

SOLUTION

Sol. 1 Option (C) is correct.

Let A denotes the position of switch at ground floor and B denotes the position of switch at upper floor. The switch can be either in up position or down position. Following are the truth table given for different combinations of A and B

A	B	Y(Bulb)
up(1)	up(1)	OFF(0)
Down(0)	Down(0)	OFF(0)
up(1)	Down(0)	ON(1)
Down(0)	up(1)	ON(1)

When the switches A and B are both up or both down, output will be zero (i.e. Bulb will be OFF). Any of the switch changes its position leads to the ON state of bulb. Hence, from the truth table, we get

$$Y = A \oplus B$$

i.e., the XOR gate

Sol. 2 Option (A) is correct.

The i / p voltage of the system is given as

$$V_{in} = V_1 + V_f = V_1 + k V_{out}$$
$$= V_1 + k A_0 V_1 \qquad \because V_{out} = A_0 V_1$$
$$= V_1 (1 + k A_0)$$

Therefore, if k is increased then input voltage is also increased so, the input impedance increases. Now, we have

$$V_{out} = A_0 V_1$$
$$= A_0 \frac{V_{in}}{(1 + k A_0)} = \frac{A_0 V_{in}}{(1 + k A_0)}$$

Since, V_{in} is independent of k when seen from output mode, the output voltage decreases with increase in k that leads to the decrease of output impedance. Thus, input impedance increases and output impedance decreases.

Sol. 3 Option (B) is correct.

For the given ideal op-amp, negative terminal will be also ground (at zero voltage) and so, the collector terminal of the *BJT* will be at zero voltage.

i.e., $V_C = 0$ volt

The current in 1 kΩ resistor is given by

$$I = \frac{5 - 0}{1\text{k}\Omega} = 5 \text{ mA}$$

This current will flow completely through the *BJT* since, no current will flow into the ideal op-amp (I / P resistance of ideal op-amp is infinity). So, for *BJT* we have

$$V_C = 0$$

$$V_B = 0$$

$$I_C = 5 \text{ mA}$$

i.e.,the base collector junction is reverse biased (zero voltage) therefore, the collector current (I_C) can have a value only if base-emitter is forward biased.

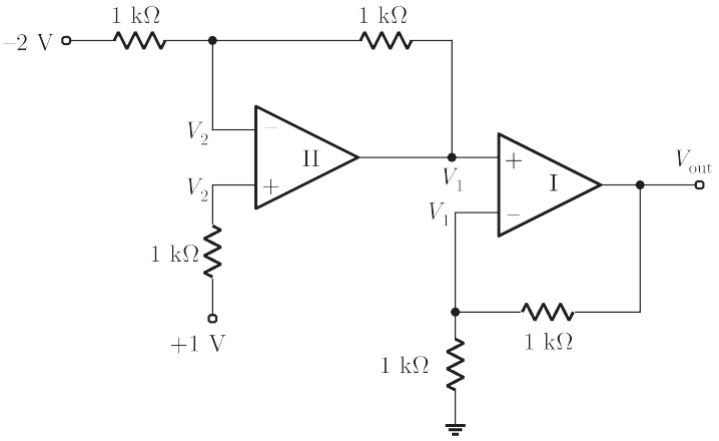
Hence,

$$V_{BE} = 0.7 \text{ volts}$$

& $V_B - V_E = 0.7$

& $0 - V_{out} = 0.7$ & $V_{out} = -0.7 \text{ volt}$

Sol. 4 Option (C) is correct.



For the given ideal op-Amps we can assume

$$V_2^- = V_2^+ = V_2 \text{ (ideal)}$$

$$V_1^+ = V_1^- = V_1 \text{ (ideal)}$$

So, by voltage division

$$V_1 = \frac{V_{out} \# 1}{2}$$

$$V_{out} = 2V_1$$

and, as the I / P current in Op-amp is always zero therefore, there will be no voltage drop across 1 KW in II op-amp

i.e., $V_2 = 1 \text{ V}$

Therefore, $\frac{V_1 - V_2}{1} = \frac{V_2 - \wedge - 2\hbar}{1}$

or, $V_1 - 1 = 1 + 2$

or, $V_1 = 4$

So,

$$V_{out} = 2V_1 = 8 \text{ volt}$$

Sol. 5 Option (B) is correct.

For the given circuit, we can make the truth table as below

X	Y	Z
0	0	0
0	1	1
1	0	0
1	1	0

Logic 0 means voltage is $v = 0$ volt and logic 1 means voltage is 5 volt

For $x = 0, y = 0$, Transistor is at cut off mode and diode is forward biased. Since, there is no drop across forward biased diode.

So, $Z = Y = 0$

For $x = 0, y = 1$, Again Transistor is in cutoff mode, and diode is forward biased. with no current flowing through resistor.

So, $Z = Y = 1$

For $x = 1, y = 0$, Transistor is in saturation mode and so, z directly connected to ground irrespective of any value of Y.

i.e., $Z = 0$ (ground)

Similarly for $X = Y = 1$

$Z = 0$ (ground)

Hence, from the obtained truth table, we get

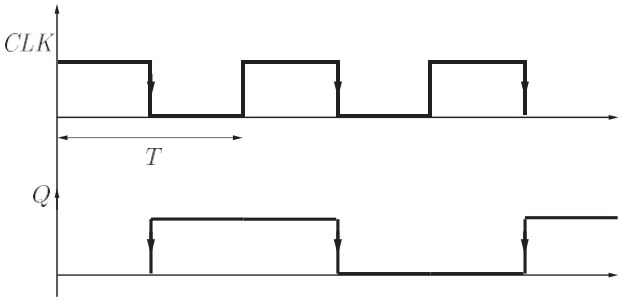
$$Z = \overline{X\,Y}$$

Sol. 6 Option (B) is correct.

From the given logic diagram, we obtain

$$X = (Q \cdot \overline{Q}) + (\overline{Q} \cdot \overline{Q}) = \overline{0} = 1$$

So, the input is always '1' at T, since, clock is – ve edge trigged therefore, at the negative edge Q changes its state as shown in waveform below



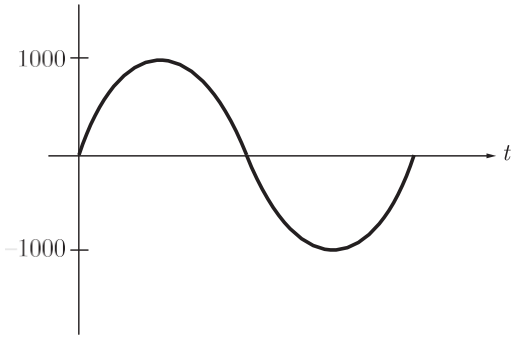
Hence, as obtained from the waveform, time period of Q is double to that of CLK I / p and so, frequency is $\frac{1}{2}$ of clock frequency

Thus, $f_Q = \frac{F_{CLK}}{2} = \frac{1}{2} = 0.5\,\text{kHz}$

Sol. 7 Option (D) is correct.

Given, the input voltage

$$V_{YZ} = 100 \sin wt$$



For + ve half cycle

$$V_{YZ} > 0$$

i.e., V_Y is a higher voltage than V_Z

So, the diode will be in cutoff region. Therefore, there will no voltage difference between X and W node.

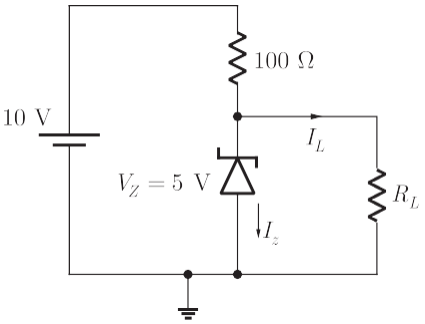
i.e., $V_{WX} = 0$

Now, for $-$ve half cycle all the four diodes will active and so, X and W terminal is short circuited

i.e., $V_{WX} = 0$

Hence, $V_{WX} = 0$ for all t

Sol. 8 Option (B) is correct.



From the circuit, we have

$$I_s = I_Z + I_L$$

or, $$I_Z = I_s - I_L \quad (1)$$

Since, voltage across zener diode is 5 V so, current through 100 W resistor is obtained as

$$I_s = \frac{10 - 5}{100} = 0.05 \text{ A}$$

Therefore, the load current is given by

$$I_L = \frac{5}{R_L}$$

Since, for proper operation, we must have

$$I_Z \geq I_{knes}$$

So, from Eq. (1), we write

$$0.05 \text{ A} - \frac{5}{R_L} \geq 10 \text{ mA}$$

$$50 \text{ mA} - \frac{5}{R_L} \geq 10 \text{ mA}$$

$$40 \text{ mA} \geq \frac{5}{R_L}$$

$$40 \times 10^{-3} \geq \frac{5}{R_L}$$

$$\frac{1}{40 \times 10^{-3}} \times \frac{R_L}{5}$$

$$\frac{5}{40 \times 10^{-3}} \times R_L$$

or, $125\ \Omega \# R_L$

Therefore, minimum value of $R_L = 125\ \Omega$

Now, we know that power rating of Zener diode is given by

$$P_R = V_Z I_{Z^{\wedge}maxh}$$

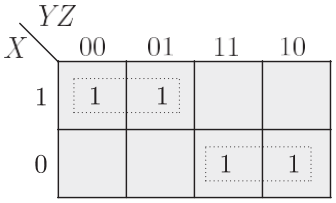
$I_{Z^{\wedge}maxh}$ is maximum current through zener diode in reverse bias. Maximum currrent through zener diode flows when load current is zero. i.e.,

$$I_{Z^{\wedge}maxh} = I_s = \frac{10-5}{100} = 0.05$$

Therefore, $P_R = 5 \# 0.05\ \text{W} = 250\ \text{mW}$

Sol. 9 Option (A) is correct.

Prime implicants are the terms that we get by solving K-map



$$F = \underbrace{XY}_{\text{prime implicants}} + \underbrace{\bar{X}Y}_{\text{prime implicants}}$$

Sol. 10 Option (D) is correct.

Let $v > 0.7$ V and diode is forward biased. Applying Kirchoff's voltage law

$$10 - i \# 1\text{k} - v = 0$$

$$10 - \left(\frac{v-0.7}{500}\right)(1000) - v = 0$$

$$10 - (v - 0.7) \# 2 - v = 0$$

$$v = \frac{11.4}{3} = 3.8\ \text{V} > 0.7 \quad \text{(Assumption is true)}$$

So, $$i = \frac{v-0.7}{500} = \frac{3.8-0.7}{500} = 6.2\ \text{mA}$$

Sol. 11 Option (B) is correct.

$Y = 1$, when $A > B$

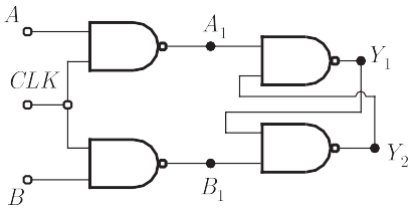
$$A = a_1 a_0,\ B = b_1 b_0$$

a_1	a_0	b_1	b_0	Y
0	1	0	0	1
1	0	0	0	1
1	0	0	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1

Total combination = 6

Sol. 12 Option (A) is correct.

The given circuit is



Condition for the race-around

It occurs when the output of the circuit (Y_1, Y_2) oscillates between '0' and '1' checking it from the options.

1. Option (A): When $CLK = 0$

Output of the NAND gate will be $A_1 = B_1 = \overline{0} = 1$. Due to these input to the next NAND gate, $Y_2 = \overline{Y_1 \cdot 1} = \overline{Y}_1$ and $Y_1 = \overline{Y_2 \cdot 1} = \overline{Y}_2$.

If $Y_1 = 0$, $Y_2 = \overline{Y_1} = 1$ and it will remain the same and doesn't oscillate.

If $Y_2 = 0$, $Y_1 = \overline{Y_2} = 1$ and it will also remain the same for the clock period. So, it won't oscillate for $CLK = 0$.

So, here race around doesn't occur for the condition $CLK = 0$.

2. Option (C): When $CLK = 1, A = B = 1$

$A_1 = B_1 = 0$ and so $Y_1 = Y_2 = 1$

And it will remain same for the clock period. So race around doesn't occur for the condition.

3. Option (D): When $CLK = 1, A = B = 0$

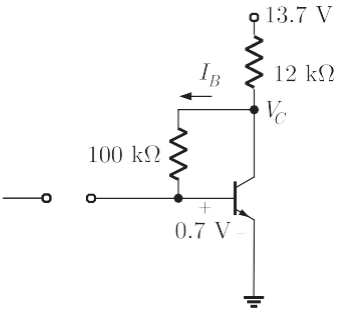
So, $A_1 = B_1 = 1$

And again as described for Option (B) race around doesn't occur for the condition.

So, Option (A) will be correct.

Sol. 13 Option (D) is correct.

DC Analysis :



Using KVL in input loop,

$$V_C - 100I_B - 0.7 = 0$$

$$V_C = 100I_B + 0.7 \quad \text{...(i)}$$

$$I_C - I_E = \frac{13.7 - V_C}{12k} = (b+1)I_B$$

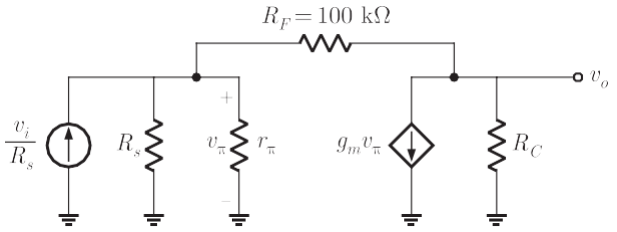
$$\frac{13.7 - V_C}{12 \# 10^3} = 100I_B \quad \text{...(ii)}$$

Solving equation (i) and (ii),

$$I_B = 0.01 \text{ mA}$$

Small Signal Analysis :

Transforming given input voltage source into equivalent current source.



This is a shunt-shunt feedback amplifier.

Given parameters,

$$r_p = \frac{V_T}{I_B} = \frac{25\ \text{mV}}{0.01\ \text{mA}} = 2.5\ \text{kW}$$

$$g_m = \frac{b}{r_p} = \frac{100}{2.5 \# 1000} = 0.04\ \text{s}$$

Writing KCL at output node

$$\frac{v_0}{R_C} + g_m v_p + \frac{v_0 - v_p}{R_F} = 0$$

$$v_0 : \frac{1}{R} + \frac{1}{R} \text{D} + v_p : g_m - \frac{1}{R} \text{D} = 0$$

Substituting R_C = 12 kW, R_F = 100 kW, g_m = 0.04 s

$$v_0 (9.33 \# 10^{-5}) + v_p (0.04) = 0$$

$$v_0 = -428.72 V_p \qquad \ldots(\text{i})$$

Writing KCL at input node

$$\frac{v_i}{R_s} = \frac{v_p}{R_s} + \frac{v_p}{r_p} + \frac{v_p - v_o}{R_F}$$

$$= v_p : \frac{1}{R} + \frac{1}{r} + \frac{1}{R} \text{D} - \frac{v_0}{R}$$

$$= v_p (5.1 \# 10^{-4}) - \frac{v_0}{R_F}$$

Substituting V_p from equation (i)

$$\frac{v_i}{R_s} = \frac{-5.1 \# 10^{-4}}{428.72} v_0 - \frac{v_0}{R_F}$$

$$\frac{v_i}{10 \# 10^3} = -1.16 \# 10^{-6} v_0 - 1 \# 10^{-5} v_0 \quad R_s = 10\ \text{kW}$$

$$\frac{v_i}{10 \# 10^3} = -1.116 \# 10^{-5}$$

$$\left| A_v = \left| \frac{v_0}{v_i} \right| \right| = \frac{1}{10 \# 10^3 \# 1.116 \# 10^{-5}} = 8.96$$

Sol. 14 Option (D) is correct.

Let Q_{n+1} is next state and Q_n is the present state. From the given below figure.

$$D = Y = A\overline{X}_0 + AX_1$$

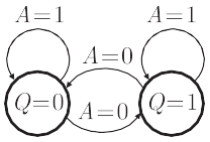
$$Q_{n+1} = D = \overline{A} X_0 + A X_1$$

$$Q_{n+1} = \overline{A}\,\overline{Q_n} + A Q_n \qquad X_0 = \overline{Q},\ X_1 = Q$$

If $A = 0$, $Q_{n+1} = \overline{Q_n}$ (toggle of previous state)

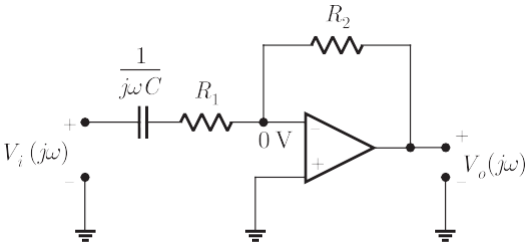
If $A = 1$, $Q_{n+1} = Q_n$

So state diagram is



Sol. 15 Option (B) is correct.

First we obtain the transfer function.



$$\frac{0 - V_i(jw)}{\frac{1}{jwC} + R_1} + \frac{0 - V_o(jw)}{R_2} = 0$$

$$\frac{V_o(jw)}{R_2} = \frac{-V_i(jw)}{\frac{1}{jwC} + R_1}$$

$$V_o(jw) = -\frac{V_i(jw)\, R_2}{R_1 - j\frac{1}{wC}}$$

At $w \to 0$ (Low frequencies), $\frac{1}{wC} \to \infty$, so $V_o = 0$

At $w \to \infty$ (higher frequencies), $\frac{1}{wC} \to 0$, so $V_o(jw) = -\frac{R_2}{R_1} V_i(jw)$

The filter passes high frequencies so it is a high pass filter.

$$H(jw) = \frac{V_o}{V_i} = \frac{-R_2}{R_1 - j\frac{1}{wC}}$$

$$|H(\infty)| = \left|\frac{-R_2}{R_1}\right| = \frac{R_2}{R_1}$$

At 3 dB frequency, gain will be $\sqrt{2}$ times of maximum gain $H(\infty)$ @

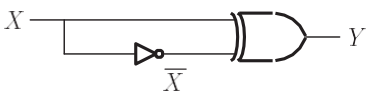
$$|H(jw_0)| = \frac{1}{\sqrt{2}} |H(\infty)|$$

So, $$\frac{R_2}{\sqrt{R_1^2 + \frac{1}{w_0^2 C^2}}} = \frac{1}{\sqrt{2}} \frac{R_2}{R_1}$$

$$2R_1^2 = R_1^2 + \frac{1}{w_0^2 C^2} \quad \& \quad R_1^2 = \frac{1}{w^2 C^2}$$

$$w_0 = \frac{1}{R_1 C}$$

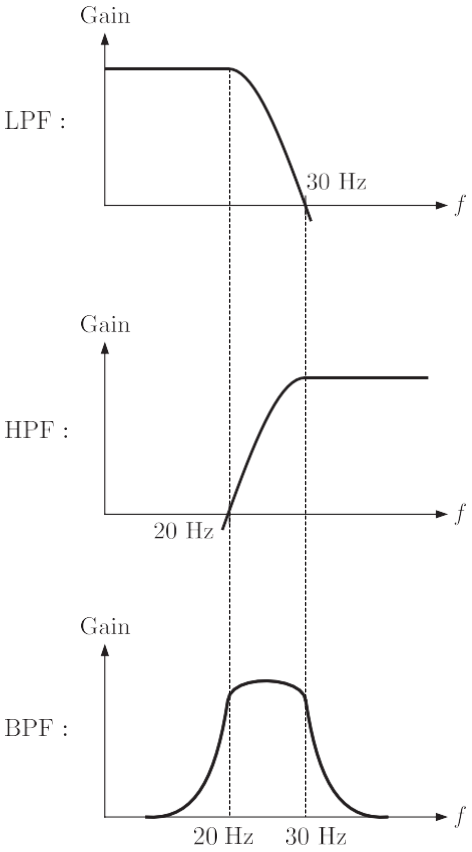
Sol. 16 Option (A) is correct.



$$Y = X \oplus \overline{X} = X\,\overline{\overline{X}} + \overline{X}X$$

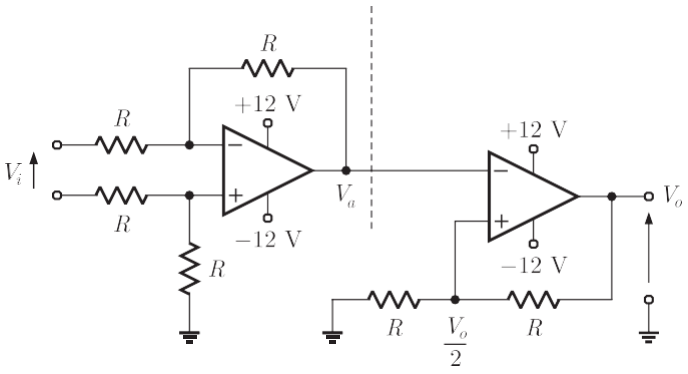
$$= XX + \overline{X}\,\overline{X} = X + \overline{X} = 1$$

Sol. 17 Option (D) is correct.



So, it will act as a Band pass filter.

Sol. 18 Option (D) is correct.



The first half of the circuit is a differential amplifier (negative feedback)

$$V_a = -(V_i)$$

Second op-amp has a positive feedback, so it acts as an schmitt trigger.

Since

$V_a = -V_i$ this is a non-inverting schmitt trigger.

Threshold value

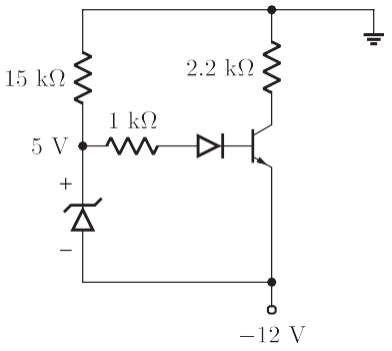
$$V_{TH} = \frac{12}{2} = 6 \text{ V}$$

$$V_{TL} = -6 \text{ V}$$

Sol. 19 Option (D) is correct.

Zener Diode is used as stabilizer.

The circuit is assumed to be as



We can see that both BE and BC Junction are forwarded biased. So the BJT is operating in saturation.

Collector current $I_C = \frac{12 - 0.2}{2.2k} = 5.36 \text{ mA}$

Note:- In saturation mode $I_C \leq bI_B$

Sol. 20 Option (C) is correct.

The characteristics equation of the JK flip-flop is

$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

Q_{n+1} is the next state

From figure it is clear that

$$J = \overline{Q_B}\,;\, K = Q_B$$

The output of JK flip flop

$$Q_{A(n+1)} = \overline{Q_B}\,\overline{Q_A} + \overline{Q_B}Q_A = \overline{Q_B}\,(\overline{Q_A} + Q_A) = \overline{Q_B}$$

Output of T flip-flop

$$Q_{B(n+1)} = \overline{Q}_A$$

Clock pulse	Q_A	Q_B	$Q_{A(n+1)}$	$Q_{B(n+1)}$
Initially(t_n)	1	0	1	0
$t_n + 1$	1	0	1	0
$t_n + 2$	1	0	1	0
$t_n + 3$	1	0	1	0

Sol. 21 Option (C) is correct.

LXI D, DISP

LP : CALL SUB

LP + 3

When CALL SUB is executed LP + 3 value is pushed(inserted) in the stack.

POP H & $HL = LP + 3$

DAD D & $HL = HL + DE$

$= LP + 3 + DE$

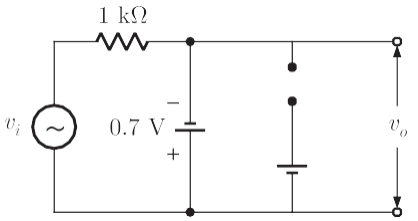
PUSH H & The last two value of the stack will be HL value i.e, $LP + DISP + 3$

Sol. 22 Option (C) is correct.

We can obtain three operating regions depending on whether the Zener and PN

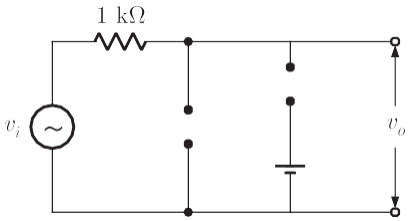
diodes are forward biased or reversed biased.

1. $v_i \# -0.7$ V, zener diode becomes forward biased and diode D will be off so the equivalent circuit looks like



The output $v_o = -0.7$ V

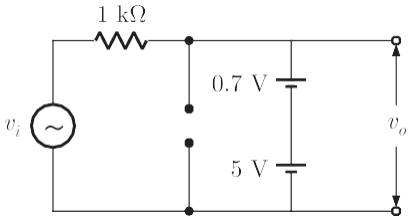
2. When $-0.7 \le v_i \# 5.7$, both zener and diode D will be off. The circuit is



Output follows input i.e $v_o = v_i$

Note that zener goes in reverse breakdown(i.e acts as a constant battery) only when difference between its p-n junction voltages exceeds 10 V.

3. When $v_i > 5.7$ V, the diode D will be forward biased and zener remains off, the equivalent circuit is



$$v_o = 5 + 0.7 = 5.7 \text{ V}$$

Sol. 23 Option (B) is correct.

Since the op-amp is ideal

$$v_+ = v_- = +2 \text{ volt}$$

By writing node equation

$$\frac{v_- - 0}{R} + \frac{v_- - v_o}{2R} = 0$$

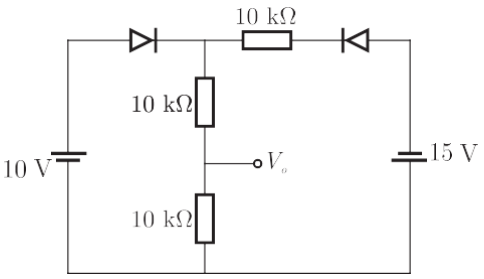
$$\frac{2}{R} + \frac{(2 - v_o)}{2R} = 0$$

$$4 + 2 - v_o = 0$$

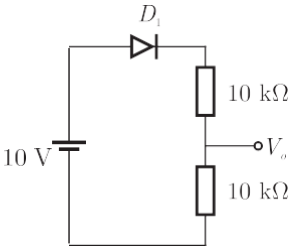
$$v_o = 6 \text{ volt}$$

Sol. 24 Option (B) is correct.

Given circuit is,



We can observe that diode D_2 is always off, whether D_1,is on or off. So equivalent circuit is.



$$V_0 = \frac{10}{10 + 10} \# 10$$

$$= 5 \text{ volt}$$

D_1 is ON in this condition and

Sol. 25 Option (A) is correct.

By writing KVL equation for input loop (Base emitter loop)

$$10 - (10\,\text{kW})\, I_B - V_{BE} - V_0 = 0 \qquad ...(1)$$

Emitter current $I_E = \frac{V_0}{100}$

$$I_C - I_E = \beta I_B$$

So,

$$\frac{V_0}{100} = 100 I_B$$

$$I_B = \frac{V_0}{10 \# 10^3}$$

Put I_B into equation (1)

$$10 - (10 \# 10^3)\frac{V_0}{10 \# 10^3} - 0.7 - V_0 = 0$$

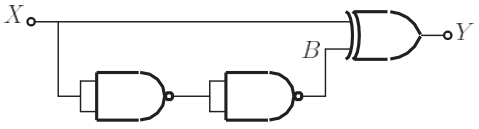
$$9.3 - 2V_0 = 0$$

&

$$V_0 = \frac{9.3}{2} = 4.65 \text{ A}$$

Sol. 26 Option (A) is correct.

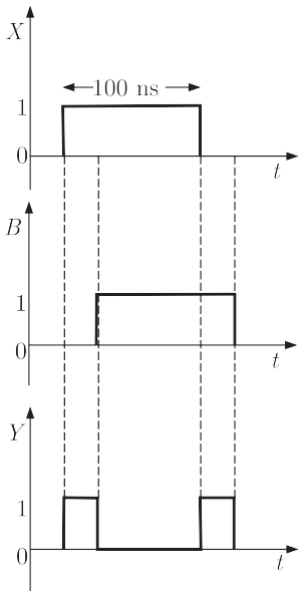
The circuit is



Output Y is written as

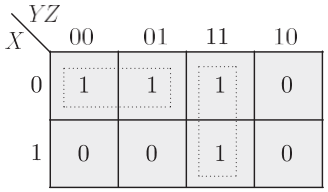
$$Y = X \oplus B$$

Since each gate has a propagation delay of 10 ns.



Sol. 27 Option (B) is correct.

Function F can be minimized by grouping of all 1's in K-map as following.

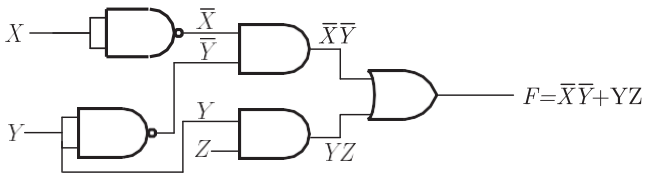


$$F = \overline{X}\,\overline{Y} + YZ$$

Sol. 28 Option (D) is correct.

Since $F = \overline{X}\,\overline{Y} + YZ$

In option (D)



Sol. 29 Option (D) is correct.

CALL, Address performs two operations

(1) PUSH PC & Save the contents of PC (Program Counter) into stack.

$$SP = SP - 2 \text{ (decrement)}$$

$$((SP)) \leftarrow (PC)$$

(2) Addr stored in PC.

$$(PC) \leftarrow Addr$$

Sol. 30 Option (A) is correct.

Figure shows current characteristic of diode during switching.

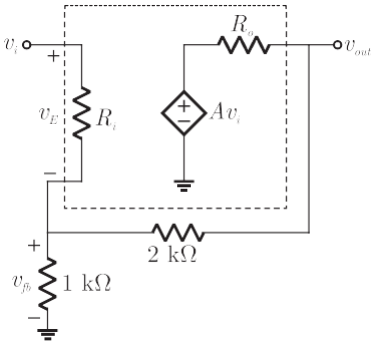
Sol. 31 Option (B) is correct.

The increasing order of speed is as following

Magnetic tape> CD-ROM> Dynamic RAM> Cache Memory> Processor register

Sol. 32 Option (B) is correct.

Equivalent circuit of given amplifier



Feedback samples output voltage and adds a negative feedback voltage (v_{fb}) to input. So, it is a voltage-voltage feedback.

Sol. 33 Option () is correct.

NOR and NAND gates considered as universal gates.

Sol. 34 Option (A) is correct.

Let voltages at positive and negative terminals of op-amp are V_+ and V_- respectively, then

$$V_+ = V_- = V_s \text{ (ideal op-amp)}$$

In the circuit we have,

$$\frac{V_- - 0}{\frac{1}{Cs}} + \frac{V_- - V_0(s)}{R} = 0$$

$$(RCs)\, V_- + V_- - V_0(s) = 0$$

$$(1 + RCs)\, V_s = V_0(s)$$

Similarly current I_s is,

$$I_s = \frac{V_s - V_0}{R}$$

$$I_s = \frac{RCs}{R} V_s$$

$$I_s = jwCV_s$$

$$I_s = |wCV_s| + +90^\circ$$

$$|I_s| = 2pf \# 10 \# 10^{-6} \# 10$$

$$|I_s| = 2 \# p \# 50 \# 10 \# 10^{-6} \# 10$$

$$|I_s| = 10p \text{ mA, leading by } 90^\circ$$

Sol. 35 Option (D) is correct.

Input and output power of a transformer is same

$$P_{in} = P_{out}$$

for emitter follower,

$$\text{voltage gain}(A_v) = 1$$

$$\text{current gain}(A_i) > 1$$

$$\text{Power}(P_{out}) = A_v A_i P_{in}$$

Since emitter follower has a high current gain so $P_{out} > P_{in}$

Sol. 36 Option (D) is correct.

For the given instruction set,

XRA A & XOR A with A & A = 0

MVI B , F0 H& B = F0 H

SUB B & $A = A - B$

A = 0 0 0 0 0 0 0 0

B = 1111 0 0 0 0

2's complement of $(-B)$ = 0 0 0 1 0 0 0 0

$A + (-B) = A - B$ = 0 0 0 1 0 0 0 0 = 10 H

Sol. 37 Option (D) is correct.

This is a schmitt trigger circuit, output can takes two states only.

V_{OH} = + 6 volt

V_{OL} = - 3 volt

Threshold voltages at non-inverting terminals of op-amp is given as

$$\frac{V_{TH} - 6}{2} + \frac{V_{TH} - 0}{1} = 0$$

$$3V_{TH} - 6 = 0$$

V_{TH} = 2 V (Upper threshold)

Similarly $$\frac{V_{TL} - (-3)}{2} + \frac{V_{TL}}{1} = 0$$

$$3V_{TL} + 3 = 0$$

V_{TL} = - 1 V (Lower threshold)

For

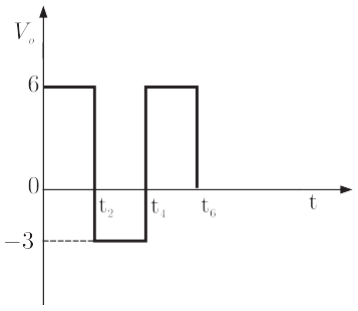
$V_{in} < 2$ Volt, $V_0 = +6$ Volt

$V_{in} > 2$ Volt, $V_0 = -3$ Volt

$V_{in} < -1$ Volt $V_0 = +6$ Volt

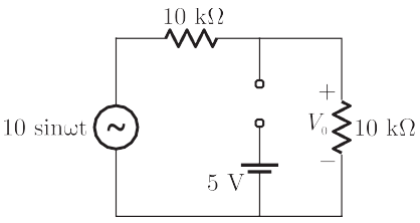
$V_{in} > -1$ Volt $V_0 = -3$ Volt

Output waveform



Sol. 38 Option (A) is correct.

Assume the diode is in reverse bias so equivalent circuit is

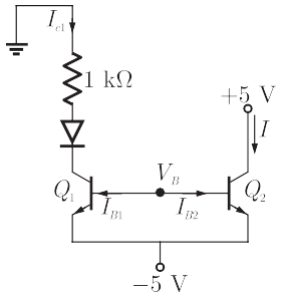


Output voltage $V_0 = \frac{10 \sin wt}{10 + 10} \# 10 = 5 \sin wt$

Due to resistor divider, voltage across diode $V_D < 0$ (always). So it in reverse bias for given input.

Output, $V_0 = 5 \sin wt$

Sol. 39 Option (C) is correct.



This is a current mirror circuit. Since b is high so $I_{C1} = I_{C2}$, $I_{B1} = I_{B2}$

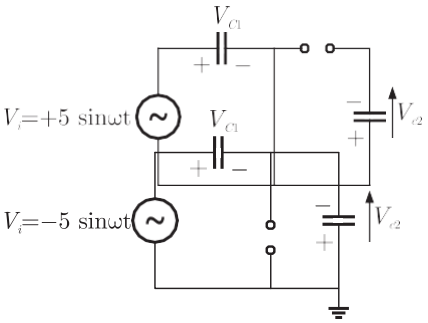
$$V_B = (-5 + 0.7) = -4.3 \text{ volt}$$

Diode D_1 is forward biased.

So, current I is, $I = I_{C2} = I_{C1} = \frac{0 - (-4.3)}{1} = 4.3$ mA

Sol. 40 Option (D) is correct.

In positive half cycle of input, diode D_1 is in forward bias and D_2 is off, the equivalent circuit is



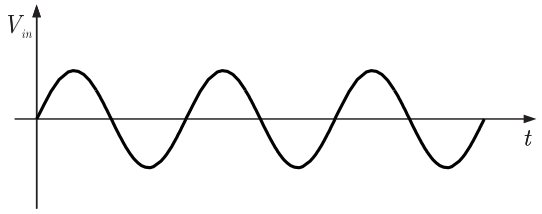
Capacitor C_1 will charge upto +5 volt. $V_{C1} = +5$ volt

In negative halt cycle diode D_1 is off and D_2 is on.

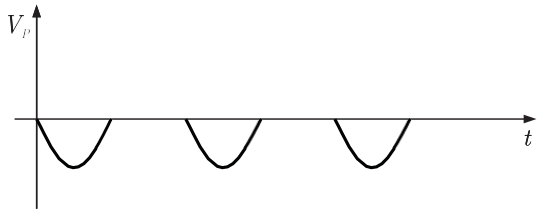
Now capacitor V_{C2} will charge upto −10 volt in opposite direction.

Sol. 41 Option () is correct.

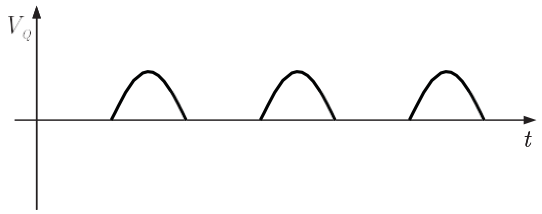
Let input V_{in} is a sine wave shown below



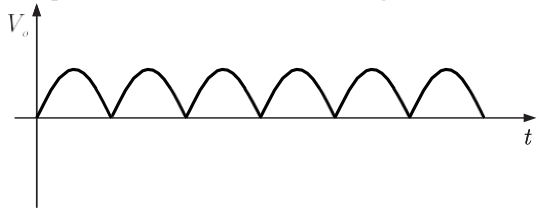
According to given transfer characteristics of rectifiers output of rectifier P is.



Similarly output of rectifier Q is



Output of a full wave rectifier is given as



To get output V_0

$V_0 = K(-V_P + V_Q)$ K – gain of op-amp

So, P should connected at inverting terminal of op-amp and Q with non-inverting terminal.

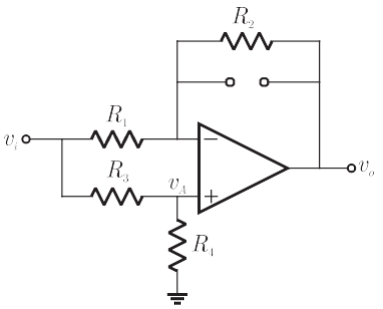
Sol. 42 Option () is correct.

Sol. 43 Option (C) is correct.

For low frequencies,

$w \to 0$, so $\frac{1}{wC} \to \infty$

Equivalent circuit is,



Applying node equation at positive and negative input terminals of op-amp.

$$\frac{v_A - v_i}{R_1} + \frac{v_A - v_o}{R_2} = 0$$

$$2v_A = v_i + v_o \,, \qquad \text{a } R_1 = R_2 = R_A$$

Similarly,

$$\frac{v_A - v_i}{R_3} + \frac{v_A - 0}{R_4} = 0$$

$$2v_A = v_{in} \,, \qquad \text{a } R_3 = R_4 = R_B$$

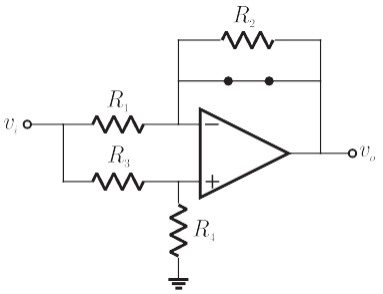
So, $v_o = 0$

It will stop low frequency signals.

For high frequencies,

w '' 3, then $\frac{1}{wC}$ '' 0

Equivalent circuit is,



Output, $v_o = v_i$

So it will pass high frequency signal.

This is a high pass filter.

Sol. 44 Option (D) is correct.

In previous solution cutoff frequency of high pass filter is given by,

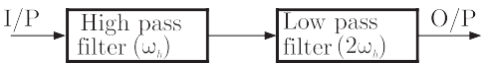
$$w_h = \frac{1}{2p\,R_A\,C}$$

Here given circuit is a low pass filter with cutoff frequency,

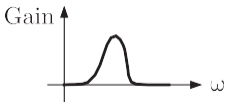
$$w_L = \frac{1}{2p\frac{R_A}{2}C} = \frac{2}{2pR_A\,C}$$

$$w_L = 2w_h$$

When both the circuits are connected together, equivalent circuit is,



So this is is Band pass filter, amplitude response is given by.

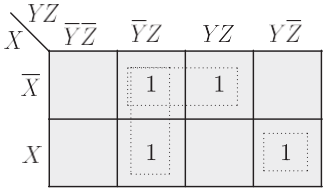


Sol. 45 Option (B) is correct.

In SOP form, F is written as

$$F = \text{Sm}(1, 3, 5, 6) = \overline{X}\,\overline{Y}\,\overline{Z} + X\overline{Y}Z + X\overline{Y}Z + XY\overline{Z}$$

Solving from K- map



$$F = \overline{X}Z + \overline{Y}Z + XY\overline{Z}$$

In POS form $F = (Y + Z)(X + Z)(\overline{X} + \overline{Y} + \overline{Z})$

Since all outputs are active low so each input in above expression is complemented

$$F = (Y + Z)(X + Z)(X + Y + Z)$$

Sol. 46 Option (B) is correct.

Given that SP = 2700 H

PC = 2100 H

HL = 0000 H

Executing given instruction set in following steps,

DAD SP & Add register pair (SP) to HL register

HL = HL + SP

HL = 0000 H + 2700 H

HL = 2700 H

PCHL & Load program counter with HL contents PC

= HL = 2700 H

So after execution contents are,

PC = 2700 H, HL = 2700 H

Sol. 47 Option (D) is correct.

If transistor is in normal active region, base current can be calculated as following,

By applying KVL for input loop,

$$10 - I_C(1\#10^3) - 0.7 - 270\#10^3 I_B = 0$$

$$bI_B + 270\,I_B = 9.3\text{ mA}, \qquad \because\ I_C = bI_B$$

$$I_B(b + 270) = 9.3\text{ mA}$$

$$I_B = \frac{9.3\text{ mA}}{270 + 100} = 0.025\text{ mA}$$

In saturation, base current is given by,

$$10 - I_C(1) - V_{CE} - I_E(1) = 0 \qquad I_C - I_E$$

$$\frac{10}{2} = I_{C\,(\text{sat})} \qquad V_{CE} - 0$$

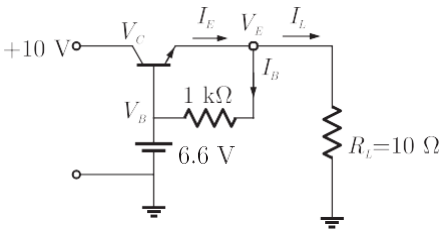
$$I_{C\,(\text{sat})} = 5\text{ mA}$$

$$I_{B\,(sat)} = \frac{I_{C\,(sat)}}{b} = \frac{5}{100} = .050 \text{ mA}$$

I_B 1 $I_{B\,(sat)}$, so transistor is in forward active region.

Sol. 48 Option (B) is correct.

In the circuit



We can analyze that the transistor is operating in active region.

$$V_{BE(ON)} = 0.6 \text{ volt}$$
$$V_B - V_E = 0.6$$
$$6.6 - V_E = 0.6$$
$$V_E = 6.6 - 0.6 = 6 \text{ volt}$$

At emitter (by applying KCL),

$$I_E = I_B + I_L$$
$$I_E = \frac{6 - 6.6}{1\,kW} + \frac{6}{10\,W} - 0.6 \text{ amp}$$

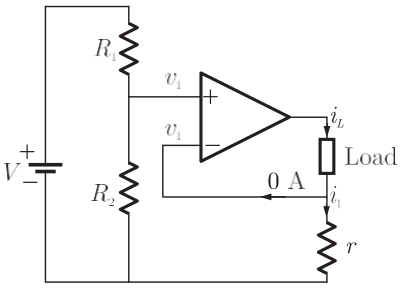
$V_{CE} = V_C - V_E = 10 - 6 = 4$ volt

Power dissipated in transistor is given by.

$$P_T = V_{CE} \# I_C = 4 \# 0.6 \quad \because I_C - I_E = 0.6 \text{ amp}$$
$$= 2.4 \text{ W}$$

Sol. 49 Option (D) is correct.

This is a voltage-to-current converter circuit. Output current depends on input voltage.



Since op-amp is ideal $v_+ = v_- = v_1$

Writing node equation.

$$\frac{v_1 - v}{R_1} + \frac{v_1 - 0}{R_2} = 0$$
$$v_1 \left(\frac{R_1 + R_2}{R_1 R_2}\right) = \frac{V}{R_1}$$
$$v_1 = V \left(\frac{R_2}{R_1 + R_2}\right)$$

Since the op-amp is ideal therefore

$$i_L = i_1 = \frac{v_1}{r} = \frac{V}{r}\left(\frac{R_2}{R_1 + R_2}\right)$$

Sol. 50 Option (D) is correct.

In the circuit output Y is given as

$$Y = [A \oplus B] \oplus [C \oplus D]$$

Output Y will be 1 if no. of 1's in the input is odd.

Sol. 51 Option () is correct.

This is a class-B amplifier whose efficiency is given as

$$\eta = \frac{\pi V_P}{4 V_{CC}}$$

where V_P '' peak value of input signal

V_{CC} '' supply voltage

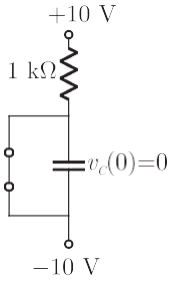
here V_P = 7 volt, V_{CC} = 10 volt

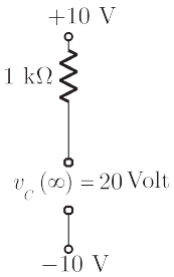
so, $$\eta = \frac{\pi}{4} \times \frac{7}{10} \times 100 = 54.95\% \approx 55\%$$

Sol. 52 Option (B) is correct.

In the circuit the capacitor starts charging from 0 V (as switch was initially closed) towards a steady state value of 20 V.

for $t < 0$ (initial) for $t \to \infty$ (steady state)





So at any time t, voltage across capacitor (i.e. at inverting terminal of op-amp) is given by

$$v_c(t) = v_c(\infty) + [v_c(0) - v_c(\infty)]\, e^{-t/RC}$$

$$v_c(t) = 20\,(1 - e^{-t/RC})$$

Voltage at positive terminal of op-amp

$$\frac{v_+ - v_{out}}{10} + \frac{v_+ - 0}{100} = 0$$

$$v_+ = \frac{10}{11} v_{out}$$

Due to zener diodes, $-5 \le v_{out} \le +5$

So, $$v_+ = \frac{10}{11}(5)\ \text{V}$$

Transistor form -5 V to $+5$ V occurs when capacitor charges upto v_+.

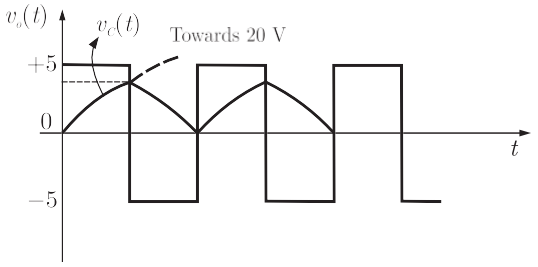
So $$20(1 - e^{-t/RC}) = \frac{10 \times 5}{11}$$

$$1 - e^{-t/RC} = \frac{5}{22}$$

$$\frac{17}{22} = e^{-t/RC}$$

$$t = RC \ln\left(\frac{22}{17}\right) = 1 \# 10^3 \# .01 \# 10^{-6} \# 0.257 = 2.57\ m\text{sec}$$

Voltage waveforms in the circuit is shown below



Sol. 53 Option (B) is correct.

In a 555 astable multi vibrator circuit, charging of capacitor occurs through resistor ($R_A + R_B$) and discharging through resistor R_B only. Time for charging and discharging is given as.

$$T_C = 0.693(R_A + R_B)C \quad = 0.693\ R_B\ C$$

But in the given circuit the diode will go in the forward bias during charging, so the capacitor will charge through resistor R_A only and discharge through R_B only.

a $$R_A = R_B$$

So $$T_C = T_D$$

Sol. 54 Option (B) is correct.

First convert the given number from hexadecimal to its binary equivalent, then binary to octal.

Hexadecimal no. AB. CD

Binary equivalent 1010 1011 1100 1101
A B C D

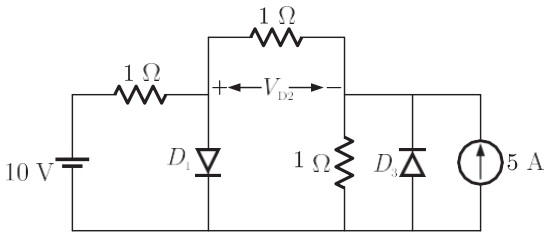
To convert in octal group three binary digits together as shown

010 101 011 100 110 100
2 5 3 4 6 4

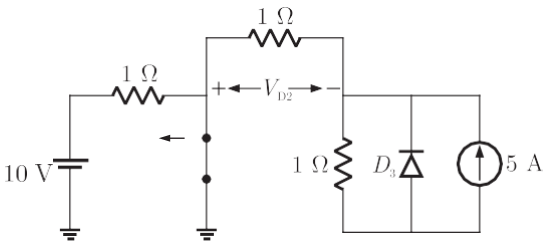
So, $$(AB.CD)_{\text{H}} = (253.632)_8$$

Sol. 55 Option (A) is correct.

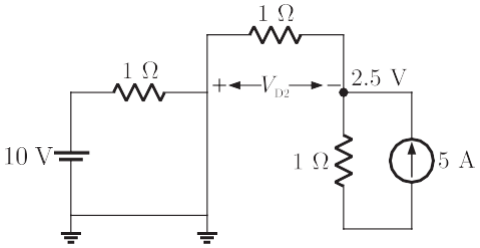
First we can check for diode D_2. Let diode D_2 is OFF then the circuit is



In the above circuit diode D_1 must be ON, as it is connected with 10 V battery now the circuit is



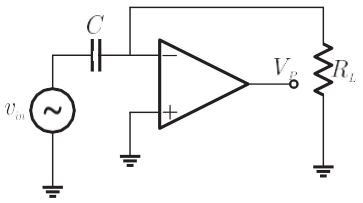
Because we assumed diode D_2 OFF so voltage across it $V_{D2} \neq 0$ and it is possible only when D_3 is off.



So, all assumptions are true.

Sol. 56 Option (D) is correct.

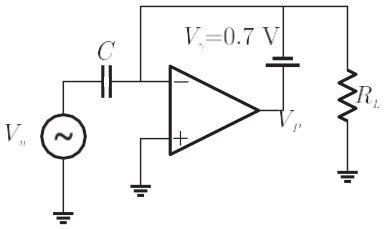
In the positive half cycle of input, Diode D_1 will be reverse biased and equivalent circuit is.



Since there is no feed back to the op-amp and op-amp has a high open loop gain so it goes in saturation. Input is applied at inverting terminal so.

$$V_P = - V_{CC} = - 12 \text{ V}$$

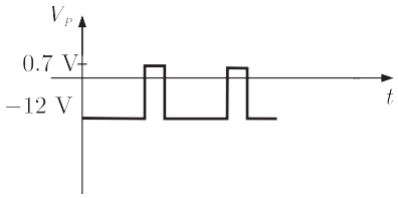
In negative half cycle of input, diode D_1 is in forward bias and equivalent circuit is shown below.



Output $V_P = V_g + V_-$

Op-amp is at virtual ground so $V_+ = V_- = 0$ and $V_P = V_g = 0.7$ V

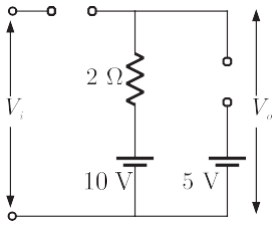
Voltage wave form at point P is



Sol. 57 Option (A) is correct.

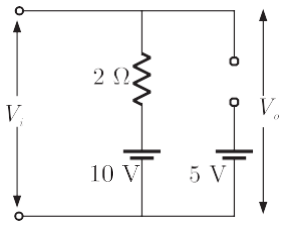
In the circuit when $V_i < 10$ V, both D_1 and D_2 are off.

So equivalent circuit is,



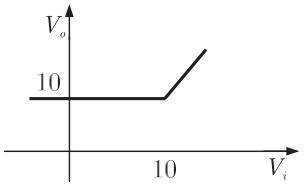
Output, $V_o = 10$ volt

When $V_i > 10$ V (D_1 is in forward bias and D_2 is off So the equivalent circuit is,



Output, $V_o = V_i$

Transfer characteristic of the circuit is



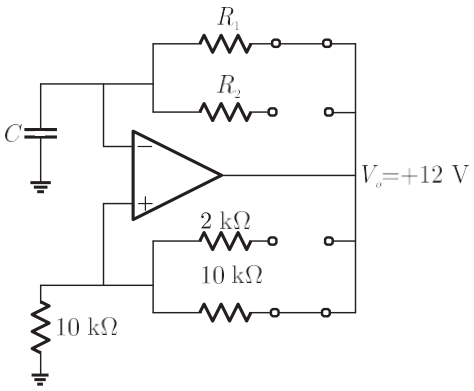
Sol. 58 Option (C) is correct.

Here output of the multi vibrator is

$$V_0 = \pm 12 \text{ volt}$$

Threshold voltage at positive terminal of op-amp can be obtained as following

When output $V_0 = +12$ V, equivalent circuit is,



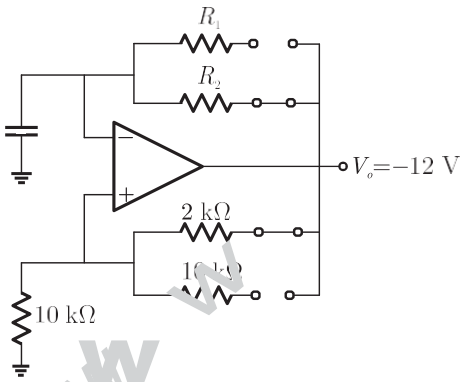
writing node equation at positive terminal of op-amp

$$\frac{V_{th}-12}{10}+\frac{V_{th}-0}{10}=0$$

V_{th} = 6 volt (Positive threshold)

So, the capacitor will charge upto 6 volt.

When output V_0 =- 12 V, the equivalent circuit is.



node equation

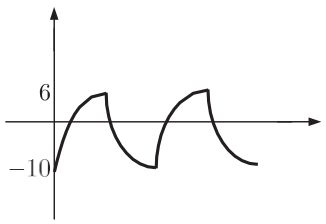
$$\frac{V_{th}+12}{2}+\frac{V_{th}-0}{10}=0$$

$$5\,V_{th}+60+V_{th}=0$$

V_{th} =- 10 volt (negative threshold)

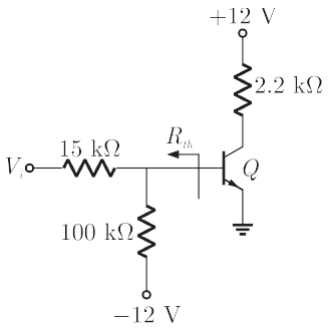
So the capacitor will discharge upto −10 volt.

At terminal P voltage waveform is.



Sol. 59 Option (B) is correct.

Assume that BJT is in active region, thevenin equivalent of input circuit is obtained as



$$\frac{V_{th} - V_i}{15} + \frac{V_{th} - (-12)}{100} = 0$$

$$20V_{th} - 20V_i + 3V_{th} + 36 = 0$$

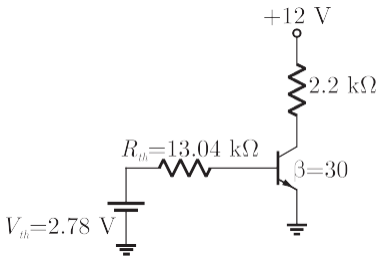
$$23V_{th} = 20 \# 5 - 36,\ V_i = 5 \text{ V}$$

$$V_{th} = 2.78 \text{ V}$$

Thevenin resistance $R_{th} = 15 \text{ KW} \,||\, 100 \text{ KW}$

$= 13.04 \text{ KW}$

So the circuit is



Writing KVL for input loop

$$2.78 - R_{th} I_B - 0.7 = 0$$

$$I_B = 0.157 \text{ mA}$$

Current in saturation is given as,

$$I_{B(\text{sat})} = \frac{I_{C(\text{sat})}}{\beta}$$

$$I_{C(\text{sat})} = \frac{12.2}{2.2} = 5.4 \text{ mA}$$

So, $$I_{B(\text{sat})} = \frac{5.45 \text{ mA}}{30} = 0.181 \text{ mA}$$

Since $I_{B(\text{sat})} > I_B$, therefore assumption is true.

Sol. 60 Option () is correct.

Sol. 61 Option () is correct.

Sol. 62 Option (A) is correct.

Function F can be obtain as,

$$F = I_0 S_1 \overline{S_0}\,\overline{} + I_1 S_1 \overline{S}_0 + I_2 S_1 \overline{S}_0 + I_3 S_1 S_0$$

$$= A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + 1 \cdot B\overline{C} + 0 \cdot BC$$

$$= A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + B\overline{C}$$

$$= A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + BC\,\overline{(A + A)}$$

$$= AB\,C + A\,BC + ABC + A\,BC$$
$$= S(1, 2, 4, 6)$$

Sol. 63 Option (A) is correct.

MVI H and MVI L stores the value 255 in H and L registers. DCR L decrements L by 1 and JNZ checks whether the value of L is zero or not. So DCR L executed 255 times till value of L becomes '0'.

Then DCR H will be executed and it goes to 'Loop' again, since L is of 8 bit so no more decrement possible and it terminates.

Sol. 64 Option (A) is correct.

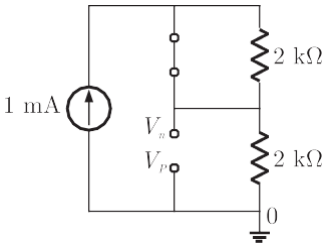
XCHG & Exchange the contain of DE register pair with HL pair So now addresses of memory locations are stored in HL pair.

INR M & Increment the contents of memory whose address is stored in HL pair.

Sol. 65 Option (A) is correct.

From the circuit we can observe that Diode D_1 must be in forward bias (since current is flowing through diode).

Let assume that D_2 is in reverse bias, so equivalent circuit is.



Voltage V_n is given by

$$V_n = 1 \# 2 = 2 \text{ Volt}$$
$$V_p = 0$$

$V_n > V_p$ (so diode is in reverse bias, assumption is true)

Current through D_2 is $I_{D2} = 0$

Sol. 66 Option (C) is correct.

SHLD transfers contain of HL pair to memory location.

SHLD 2050 & L '' M[2050H]

H ''M[2051H]

Sol. 67 Option (D) is correct.

This is a N-channel MOSFET with $V_{GS} = 2$ V

$$V_{TH} = +1 \text{ V}$$
$$V_{DS\,(\text{sat})} = V_{GS} - V_{TH}$$
$$V_{DS(\text{sat})} = 2 - 1 = 1 \text{ V}$$

Due to 10 V source $V_{DS} > V_{DS\ (\text{sat})}$ so the NMOS goes in saturation, channel conductivity is high and a high current flows through drain to source and it acts as a short circuit.

So, $V_{ab} = 0$

Sol. 68 Option (C) is correct.

Let the present state is Q(t), so input to D-flip flop is given by,

$$D = Q\,(t)\ 5\ X$$

Next state can be obtained as, $\overline{\overline{Q}}\ \overline{\overline{X}}\qquad \overline{Q}\ \overline{X}$

$$Q(t+1) = D$$
$$= Q(t) \oplus X$$
$$= Q(t)\overline{X} + \overline{Q}(t)X$$
$$= Q(t), \quad \text{if } X = 1$$

and $Q(t+1) = \overline{Q}(t), \quad \text{if } X = 0$

So the circuit behaves as a T flip flop.

Sol. 69 Option (B) is correct.

Since the transistor is operating in active region.

$$I_E = \beta I_B$$
$$I_B = \frac{I_E}{\beta} = \frac{1\ \text{mA}}{100} = 10\ \mu\text{A}$$

Sol. 70 Option (C) is correct.

Gain of the inverting amplifier is given by,

$$A_v = -\frac{R_F}{R_1} = -\frac{1 \times 10^6}{R_1}, \qquad R_F = 1\ \text{M}\Omega$$

$$R_1 = -\frac{1 \times 10^6}{A_v}$$

$A_v = -10$ to -25 so value of R_1

$$R_1 = \frac{10^6}{10} = 100\,\text{k}\Omega \qquad \text{for } A_v = -10$$

$$R_1' = \frac{10^6}{25} = 40\,\text{k}\Omega \qquad \text{for } A_v = -25$$

R_1 should be as large as possible so $R_1 = 100\ \text{k}\Omega$

Sol. 71 Option (B) is correct.

Direct coupled amplifiers or DC-coupled amplifiers provides gain at dc or very low frequency also.

Sol. 72 Option (C) is correct.

Since there is no feedback in the circuit and ideally op-amp has a very high value of open loop gain, so it goes into saturation (ouput is either $+V$ or $-V$) for small values of input.

The input is applied to negative terminal of op-amp, so in positive half cycle it saturates to $-V$ and in negative half cycle it goes to $+V$.

Sol. 73 Option (B) is correct.

From the given input output waveforms truth table for the circuit is drawn as

X_1	X_2	Q
1	0	1
0	0	1
0	1	0

In option (A), for $X_1 = 1$, $Q = 0$ so it is eliminated.

In option (C), for $X_1 = 0$, $Q = 0$ (always), so it is also eliminated.

In option (D), for $X_1 = 0$, $Q = 1$, which does not match the truth table. Only option (B) satisfies the truth table.

Sol. 74 Option (D) is correct.

In the given circuit NMOS Q_1 and Q_3 makes an inverter circuit. Q_4 and Q_5 are in

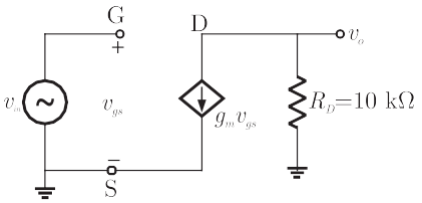
parallel works as an OR circuit and Q_2 is an output inverter.
So output is

$$Q = \overline{\overline{X_1} + X_2} = X_1.\overline{X_2}$$

Sol. 75 Option (B) is correct.
Trans-conductance of MOSFET is given by

$$g_m = \frac{2i_D}{2V_{GS}} = \frac{(2-1)\text{ mA}}{(2-1)\text{ V}} = 1\text{ mS}$$

Sol. 76 Option (D) is correct.
Voltage gain can be obtain by small signal equivalent circuit of given amplifier.



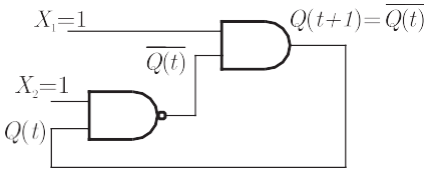
$$v_o = -g_m\, v_{gs}\, R_D$$

$$v_{gs} = v_{in}$$

So, $v_o = -\,g_m R_D v_{in}$

Voltage gain $A_v = \frac{v_o}{v_i} = -\,g_m R_D = -\,(1\text{ mS})\,(10\text{ kW}) = -\,10$

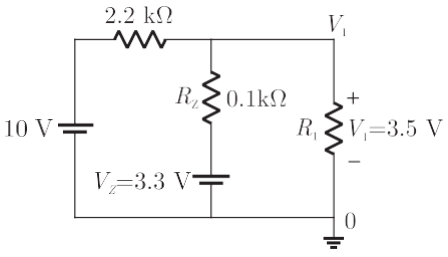
Sol. 77 Option (D) is correct.
Let $Q(t)$ is the present state then from the circuit,



So, the next state is given by

$$Q(t+1) = \overline{Q}(t) \text{ (unstable)}$$

Sol. 78 Option (C) is correct.
Given circuit,



In the circuit

$$V_1 = 3.5\text{ V (given)}$$

Current in zener is.

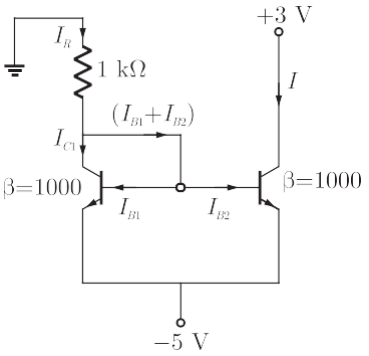
$$I_Z = \frac{V_1 - V_Z}{R_Z} = \frac{3.5 - 3.3}{0.1 \#10^3} = 2\text{ mA}$$

Sol. 79 Option (C) is correct.

This is a current mirror circuit. Since V_{BE} is the same in both devices, and transistors are perfectly matched, then

$$I_{B1} = I_{B2} \quad \text{and} \quad I_{C1} = I_{C2}$$

From the circuit we have,



$$\text{a } I_{B1} = I_{B2}$$

$$\text{a } I_{C1} = I_{C2}, I_{C2} = \text{b} I_{B2}$$

$$I_R = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2}$$

$$= I_{C2} + \frac{2I_{C2}}{b}$$

$$I_R = I_{C2}\left(1 + \frac{2}{b}\right)$$

$$I_{C2} = I = \frac{I_R}{\left(1 + \frac{2}{b}\right)}$$

I_R can be calculate as

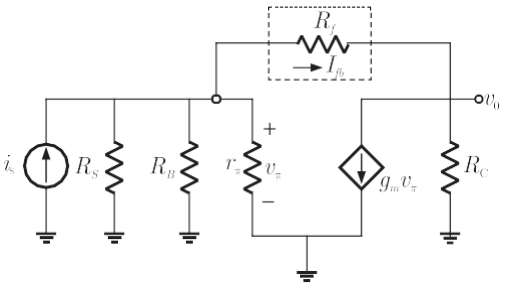
$$I_R = \frac{-5 + 0.7}{1 \# 10^3} = -4.3 \text{ mA}$$

So,

$$I = \frac{4.3}{\left(1 + \frac{2}{100}\right)} = 4.3 \text{ mA}$$

Sol. 80 Option (B) is correct.

The small signal equivalent circuit of given amplifier



Here the feedback circuit samples the output voltage and produces a feed back current I_{fb} which is in shunt with input signal. So this is a shunt-shunt feedback configuration.

Sol. 81 Option (A) is correct.

In the given circuit output is stable for both 1 or 0. So it is a bistable multi-vibrator.

Sol. 82 Option (A) is correct.

Since there are two levels ($+ V_{CC}$ *or* $- V_{CC}$) of output in the given comparator

circuit.

For an n -bit Quantizer

$$2^n = \text{No. of levels}$$

$$2^n = 2$$

$$n = 1$$

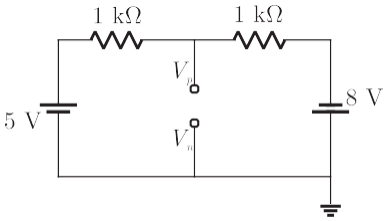
Sol. 83 Option (C) is correct.

From the circuit, we can see the that diode D_2 must be in forward Bias.

For D_1 let assume it is in reverse bias.

Voltages at p and n terminal of D_1 is given by V_p and V_n

$V_p < V_n$ (D_1 is reverse biased)



Applying node equation

$$\frac{V_p - 5}{1} + \frac{V_p + 8}{1} = 0$$

$$2V_p = -3$$

$$V_p = -1.5$$

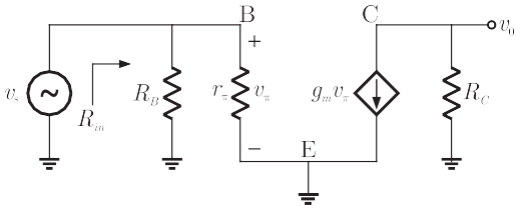
$$V_n = 0$$

$V_p < V_n$ (so the assumption is true and D_1 is in reverse bias) and current in D_1

$$I_{D1} = 0 \text{ mA}$$

Sol. 84 Option (D) is correct.

The small signal ac equivalent circuit of given amplifier is as following.



Here $R_B = (10 \text{ kW} < 10 \text{ kW}) = 5 \text{ kW}$

$$g_m = 10 \text{ ms}$$

$$a\, g_m r_p = b \;\&\; r_p = \frac{50}{10 \# 10^{-3}} = 5 \text{ kW}$$

Input resistance

$$R_{in} = R_B < r_p = 5 \text{ kW} < 5 \text{ kW} = 2.5 \text{ kW}$$

Sol. 85 Option (D) is correct.

For PMOS to be biased in non-saturation region.

$$V_{SD} < V_{SD(\text{sat})}$$

and

$$V_{SD(\text{sat})} = V_{SG} + V_T$$

$$V_{SD(sat)} = 4 - 1 \qquad \text{"a } V_{SG} = 4 - 0 = 4 \text{ volt}$$
$$= 3 \text{ Volt}$$

So, $V_{SD} < 3$

$$V_S - V_D < 3$$
$$4 - I_D R < 3$$
$$1 < I_D R$$
$$I_D R > 1, \qquad I_D = 1 \text{ mA}$$
$$R > 1000 \text{ W}$$

Sol. 86 Option () is correct.

Sol. 87 Option (B is correct.

If op-amp is ideal, no current will enter in op-amp. So current i_x is

$$i_x = \frac{v_x - v_y}{1 \# 10^6} \qquad ...(1)$$
$$v_+ = v_- = v_x \qquad \text{(ideal op-amp)}$$

$$\frac{v_x - v_y}{100 \# 10^3} + \frac{v_x - 0}{10 \# 10^3} = 0$$
$$v_x - v_y + 10 v_x = 0$$
$$11 v_x = v_y \qquad ...(2)$$

For equation (1) & (2)

$$i_x = \frac{v_x - 11 v_x}{1 \# 10^6} = - \frac{10 v_x}{10^6}$$

Input impedance of the circuit.

$$R_{in} = \frac{v_x}{i_x} = - \frac{10^6}{10} = - 100 \text{ kW}$$

Sol. 88 Option (A) is correct.

Given Boolean expression,

$$Y = (\overline{A} \$ BC + D)(\overline{A \$ D + B \$ C})$$
$$= (\overline{A} \$ BCD) + (\overline{A}BC \$ \overline{B} \$ \overline{C}) + (\overline{AD}) + \overline{B}\,\overline{C}\,\overline{D}$$
$$= \overline{A}\,BCD + \overline{AD} + \overline{B}\,\overline{C}\,\overline{D}$$
$$= \overline{AD}(BC + 1) + \overline{B}\,\overline{C}\,\overline{D} = \overline{AD} + \overline{B}\,\overline{C}\,\overline{D}$$

Sol. 89 Option (C) is correct.

The program is executed in following steps.

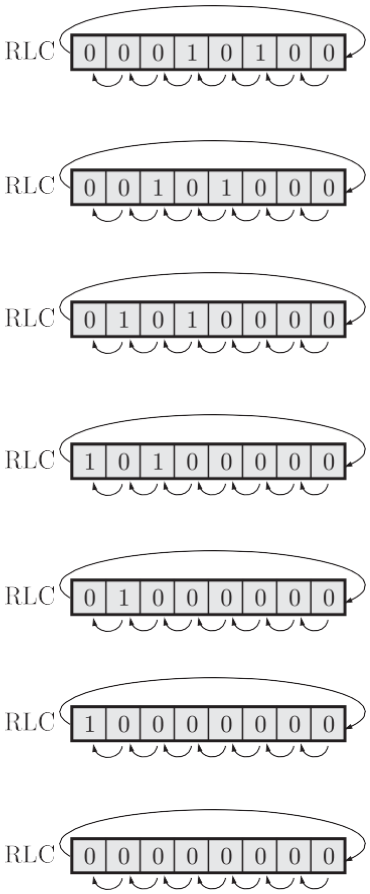
START MVI A, 14H " one instruction cycle.

RLC & rotate accumulator left without carry

RLC is executed 6 times till value of accumulator becomes zero.

JNZ, JNZ checks whether accumulator value is zero or not, it is executed 5 times.

HALT " 1-instruction cycle.



So total no. of instruction cycles are

$$n = 1 + 6 + 5 + 1 = 13$$

Sol. 90 Option (D) is correct.

In the given circuit, output is given as.

$$Y = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$$

For option (A)

$$Y = (1 \oplus 1) + (0 \oplus 0) + (1 \oplus 1) + (0 \oplus 0)$$
$$= 0 + 0 + 0 + 0 = 1$$

For option (B)

$$Y = (0 \oplus 0) + (1 \oplus 1) + (0 \oplus 0) + (1 \oplus 1)$$
$$= 0 + 0 + 0 + 0 = 1$$

For option (C)

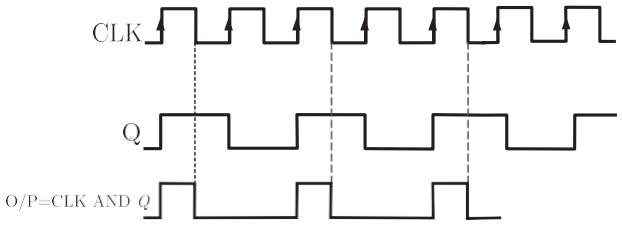
$$Y = (0 \oplus 0) + (0 \oplus 0) + (1 \oplus 1) + (0 \oplus 0)$$
$$= 0 + 0 + 0 + 0 = 1$$

For option (D)

$$Y = (1 \oplus 1) + (0 \oplus 0) + (1 \oplus 1) + (0 \oplus 1)$$
$$= 0 + 0 + 0 + 0 + 1 = 0$$

Sol. 91 Option (B) is correct.

In the given circuit, waveforms are given as,



Sol. 92 Option (B) is correct.

In the given circuit

$V_i = 0$ V

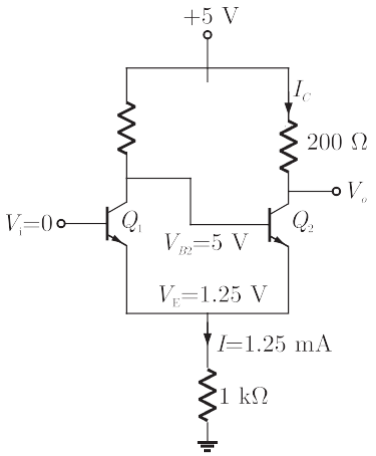
So, transistor Q_1 is in cut-off region and Q_2 is in saturation.

$$5 - I_C R_C - V_{CE(\text{sat})} - 1.25 = 0$$

$$5 - I_C R_C - 0.1 - 1.25 = 0$$

$$5 - I_C R_C = 1.35$$

$$V_0 = 1.35 \qquad \because V_0 = 5 - I_C R_C$$



Sol. 93 Option (C) is correct.

Since there exists a drain current for zero gate voltage ($V_{GS} = 0$), so it is a depletion mode device.

I_D increases for negative values of gate voltages so it is a p -type depletion mode device.

Sol. 94 Option (B) is correct.

Applying KVL in input loop,

$$4 - (33 \# 10^3)\, I_B - V_{BE} - (3.3 \# 10^3)\, I_E = 0$$

$$\because I_E = (h_{fe} + 1)\, I_B$$

$$4 - (33 \# 10^3) I_B - 0.7 - (3.3 \# 10^3)(h_{fe} + 1) I_B = 0$$

$$3.3 = [(33 \# 10^3) + (3.3 \# 10^3)(99 + 1)] I_B$$

$$I_B = \frac{3.3}{33 \# 10^3 + 3.3 \# 10^3 \# 100}$$

$$I_C = h_{fe} I_B$$

$$= \frac{99 \# 3.3}{[0.33 + 3.3] \# 100} \text{mA} = \frac{3.3}{0.33 + 3.3} \text{mA}$$

Sol. 95 Option (D) is correct.

Let the voltages at positive and negative terminals of op-amp are v_+ and v_- respectively. Then by applying nodal equations.

$$\frac{v_- - v_{in}}{R_1} + \frac{v_- - v_{out}}{R_1} = 0$$

$$2v_- = v_{in} + v_{out} \quad ..(1)$$

Similarly,

$$\frac{v_+ - v_{in}}{R} + \frac{v_+ - 0}{\left(\frac{1}{jwC}\right)} = 0$$

$$v_+ - v_{in} + v_+ (jwCR) = 0$$

$$v_+ (1 + jwCR) = V_{in} \quad ..(2)$$

By equation (1) & (2)

$$\frac{2v_{in}}{1 + jwCR} = v_{in} + v_{out} \qquad \because v_+ = v_- \text{ (ideal op-amp)}$$

$$v_{in}\left(\frac{2}{1 + jwCR} - 1\right) = v_{out}$$

$$v_{out} = v_{in}\frac{(1 - jwCR)}{1 + jwCR}$$

Phase shift in output is given by

$$\theta = \tan^{-1}(-wCR) - \tan^{-1}(wCR)$$
$$= \pi - \tan^{-1}(wCR) - \tan^{-1}(wCR)$$
$$= \pi - 2\tan^{-1}(wCR)$$

Maximum phase shift $\theta = \pi$

Sol. 96 Option (C) is correct.

In given circuit MUX implements a 1-bit full adder, so output of MUX is given by.

$$F = \text{Sum} = A \oplus Q \oplus C_{in}$$

Truth table can be obtain as.

P	Q	C_{in}	Sum
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$\text{Sum} = \overline{P}\,\overline{Q}\,C_{in} + \overline{P}Q\,\overline{C_{in}} + P\,\overline{Q}\,\overline{C_{in}} + P\,Q\,C_{in}$$

Output of MUX can be written as

$$F = \overline{P}\,\overline{Q}I_0 + \overline{P}QI_1 + P\overline{Q}I_2 + PQI_3$$

Inputs are, $I_0 = C_{in}, \quad I_1 = \overline{C_{in}}, \quad I_2 = \overline{C_{in}}, \quad I_3 = C_{in}$

Sol. 97 Option (D) is correct.

Program counter contains address of the instruction that is to be executed next.

Sol. 98 Option (A) is correct.

For a *n* -channel enhancement mode MOSFET transition point is given by,

$$V_{DS(\text{sat})} = V_{GS} - V_{TH} \qquad \because V_{TH} = 2 \text{ volt}$$

$$V_{DS\,(sat)} = V_{GS} - 2$$

From the circuit,

$$V_{DS} = V_{GS}$$

So $$V_{DS\,(sat)} = V_{DS} - 2 \;\&\; V_{DS} = V_{DS\,(sat)} + 2$$

$$V_{DS} > V_{DS\,(sat)}$$

Therefore transistor is in saturation region and current equation is given by.

$$I_D = K\,(V_{GS} - V_{TH})^2$$

$$4 = K\,(V_{GS} - 2)^2$$

V_{GS} is given by

$$V_{GS} = V_{DS} = 10 - I_D R_D = 10 - 4 \# 1 = 6 \text{ Volt}$$

So, $$4 = K(6-2)^2$$

$$K = \frac{1}{4}$$

Now R_D is increased to 4 kW, Let current is I_D' and voltages are $V_{DS}' = V_{GS}'$

Applying current equation.

$$I_D' = K\,(V_{GS}' - V_{TH})^2$$

$$I_D' = \frac{1}{4}(V_{GS}' - 2)^2$$

$$V_{GS}' = V_{DS}' = 10 - I_D' \# R_D' = 10 - 4I_D'$$

So, $$4I_D' = (10 - 4I_D' - 2)^2 = (8 - 4I_D')^2$$

$$= 16\,(2 - I_D')^2$$

$$I_D' = 4\,(4 + I_D'^2 - 4I_D')$$

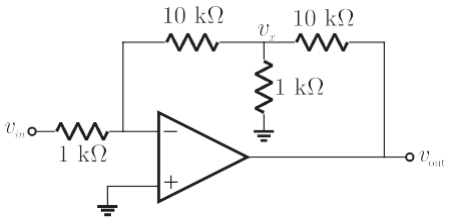
$$4I_D'^2 - 17 + 16 = 0$$

$$I_D'^2 = 2.84 \text{ mA}$$

Sol. 99 Option (D) is correct.

Let the voltages at input terminals of op-amp are v_- and v_+ respectively.

So, $v_+ = v_- = 0$ (ideal op-amp)



Applying node equation at negative terminal of op-amp,

$$\frac{0 - v_{in}}{1} + \frac{0 - v_x}{10} = 0 \qquad \ldots(1)$$

At node x

$$\frac{v_x - 0}{10} + \frac{v_x - v_{out}}{10} + \frac{v_x - 0}{1} = 0$$

$$v_x + v_x - v_{out} + 10v_x = 0$$

$$12\,v_x = v_{out}$$

$$v_x = \frac{v_{out}}{12}$$

From equation (1),

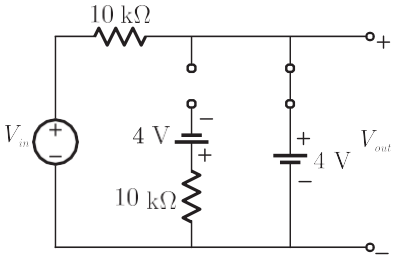
$$\frac{v_{in}}{1} + \frac{v_x}{10} = 0$$

$$v_{in} = -\frac{v_{out}}{120}$$

$$\frac{v_{out}}{v_{in}} = -120$$

Sol. 100 Option (D) is correct.

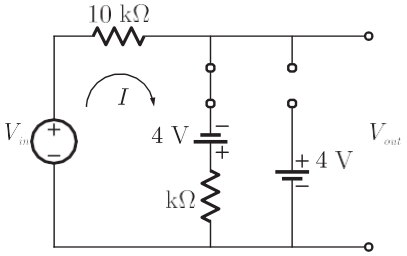
In the positive half cycle (when $V_{in} > 4$ V) diode D_2 conducts and D_1 will be off so the equivalent circuit is,



10

$$V_{out} = +4 \text{ Volt}$$

In the negative half cycle diode D_1 conducts and D_2 will be off so the circuit is,



Applying KVL

$$V_{in} - 10I + 4 - 10I = 0$$

$$\frac{V_{in} + 4}{20} = I$$

$V_{in} = -10$ V (Maximum value in negative half cycle)

So, $$I = \frac{-10+4}{20} = -\frac{3}{10} \text{ mA}$$

$$\frac{V_{in} - V_{out}}{10} = I$$

$$\frac{-10 - V_{out}}{10} = -\frac{3}{10}$$

$$V_{out} = -(10 - 3)$$

$$V_{out} = -7 \text{ volt}$$

Sol. 101 Option (C) is correct.

In the circuit, the capacitor charges through resistor ($R_A + R_B$) and discharges through R_B . Charging and discharging time is given as.

$$T_C = 0.693 (R_A + R_B) C$$

$$T_D = 0.693 R_B C$$

Frequency $$f = \frac{1}{T} = \frac{1}{T_D + T_C} = \frac{1}{0.693(R_A + 2R_B)C}$$

$$\frac{1}{0.693 (R_A + 2R_B) \# 10 \# 10^{-9}} = 10 \# 10^3$$

$$14.4 \# 10^3 = R_A + 2R_B \quad ...(1)$$

duty cycle $$= \frac{T_C}{T} = 0.75$$

$$\frac{0.693\,(R_A + R_B)\,C}{0.693\,(R_A + 2R_B)\,C} = \frac{3}{4}$$

$$4R_A + 4R_B = 3R_A + 6R_B$$

$$R_A = 2R_B \qquad ...(2)$$

From (1) and (2) $2R_A = 14.4 \# 10^3$

$$R_A = 7.21 \text{ kW}$$

and $R_B = 3.60$ kW

Sol. 102 Option (B) is correct.

Given boolean expression can be written as,

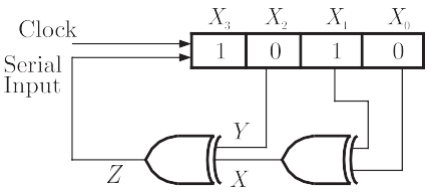
$$F = \overline{X}\,\overline{Y}\overline{Z} + \overline{X}\,\overline{Y}\,Z + XY\overline{Z} + XYZ + X\,YZ$$

$$= \overline{X}\,\overline{Y}\overline{Z} + \overline{Y}\,\overline{Z}\,(X + X) + XY\,(\overline{Z} + Z) = \overline{X}\,\overline{Y}\overline{Z} + \overline{Y}\,\overline{Z} + X\,Y$$

$$= \overline{Y}\,\overline{Z} + Y\,(X + \overline{X}\,\overline{Z}) \qquad \text{a } A + BC = (A + B)(A + C)$$

$$= \overline{Y}\,\overline{Z} + Y\,(X + \overline{X})\,(X + \overline{Z}) = \overline{Y}\,\overline{Z} + Y\,(X + \overline{Z}) = \overline{Y}\,\overline{Z} + Y\,X + YZ$$

Sol. 103 Option (B) is correct.



$$X = X_1 \oplus X_0,\ Y = X_2$$

Serial Input $Z = X \oplus Y = [X_1 \oplus X_0] \oplus X_2$

Truth table for the circuit can be obtain as.

Clock pulse	Serial Input	Shift register
Initially	1	1010
1	0	1101
2	0	0110
3	0	0011
4	1	0001
5	0	1000
6	1	0100
7	1	1010

So after 7 clock pulses contents of the shift register is 1010 again.

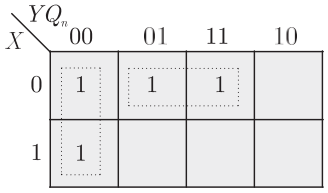
Sol. 104 Option (D) is correct.

Characteristic table of the X-Y flip flop is obtained as.

X	Y	Q_n	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1

1	0	1	0
1	1	0	0
1	1	0	0

Solving from k-map



Characteristic equation of X-Y flip flop is

$$Q_{n+1} = \overline{Y}\,\overline{Q_n} + \overline{X}Q_n$$

Characteristic equation of a J-K flip-flop is given by

$$Q_{n+1} = \overline{K}Q_n + J\overline{Q_n}$$

by comparing above two characteristic equations

$$J = \overline{Y},\ K = X$$

Sol. 105 Option (A) is correct.

Total size of the memory system is given by.

$$= (2^{12} \# 4) \# 8 \text{ bits}$$

$$= 2^{14} \# 8 \text{ bits} = 2^{14} \text{ Bytes} = 16 \text{ K bytes}$$

Sol. 106 Option (C) is correct.

Executing all the instructions one by one.

LXI H, 1FFE & H = $(1F)_H$, L = $(FE)_H$

MOV B, M & B = Memory [HL] = Memory [1FFE]

INR L & L = L + $(1)_H$ = $(FF)_H$

MOV A, M & A = Memory [HL] = Memory [1FFF]

ADD B & A = A + B

INR L & L = L + $(1)_H$ = $(FF)_H$ + $(1)_H$ = 00

MOV M, A & Memory [HL] = A

Memory [1F00] = A

XOR A & A = A XOR A = 0

So the result of addition is stored at memory address 1F00.

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