ALL INDIA 1st RANK 19 TIMES IN GATE

&

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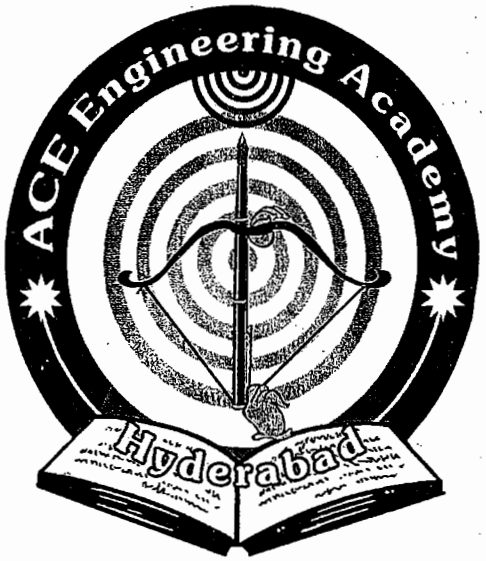

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Rohini Reddy. D

GATE – SYLLABUS

Digital Electronics & Mircroprocessors

Transistor as a switching element; Boolean algebra, simplification of Boolean functions, Karnaugh Map and application; IC Logic gates and their characteristics; IC logic families: DTL,TTL, ECL, NMOS, PMOS and CMOS gates and their comparison; Combinational logic circuits; Half adder, full adder; Digital comparator; Multiplexer; ROM and their applications. Flip – flops, R – S, J – K , D and T flip – flops; Different types of counters and registers; waveform generators. A/D & D/A converters. Semiconductor memories. Microprocessor: Architecture, Programming, Memory and I/O Interfacing.

Digital Electronics & Microprocessors

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Managing Director

Y.V. GOPALA KRISHNA MURTHY

Profile

S. V. Rao, B.Sc., B.Tech., M.E.(Digital Systems)., M.I.S.T.E., has been working for over 22 years, including the last 11 + years in the VLSI industry. Before joining the VLSI industry in 2000, he taught in the department of Electronics and Communication Engineering, MVSR Engineering College as an Associate Professor. He has also taught at the University College of Engineering, Osmania University and JNTU College of Engineering, Hyderabad and worked as a Lecturer at Deccan College of Engineering & Technology, Hyderabad.

Rao has authored a book called "Computer Fundamentals and Applications" (RPH-1994) for Diploma Course in Polytechnics in Andhra Pradesh. He has also written a paper titled "Performance Evaluation of Non-Linear Edge Detectors in Digital Image Processing" which was presented at the "International Conference on Remote Sensing" organized by JNTU, Hyderabad in December 1994. The paper was subsequently published in the International Journal for Remote Sensing in 1995.

Sri S.V. Rao's contribution in the preparation of the booklet "Digital Electronics & Microprocessor" useful for all the competitive exams in Engineering is highly appreciated, as a social responsibility towards helping the Engineering students to achieve their goals.

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The concept of counting is as old as the evolution of man on this earth. The number systems are used to quantify the magnitude of something. One way of quantifying the magnitude of something is by proportional values. This is called analog representation. The other way of representation of any quantity is numerical (Digital). There are many number systems are present. The most frequently used number systems in the applications of Digital Computers are Binary Number System, Octal Number System, Decimal Number System and Hexadecimal Number System.

Base or Radix (r) of a Number System : The Base or Radix of a number system is defined as the number of different symbols (Digits or Characters) used in that number system.

The radix of Binary number system = 2 i.e. it uses two different symbols 0 and 1 to write the number sequence.

The radix of Octal number system = 8 i.e. it uses eight different symbols 0,1,2,3,4,5,6 and 7 to write number sequence.

The radix of Decimal number system = 10 i.e. it uses ten different symbols 0,1,2,3,4,5,6,7,8 and 9 to write number sequence.

The radix of Hexadecimal number system = 16 i.e. it uses sixteen different symbols 0,1,2,3,4,5,6,7,8 ,9,A,B,C,D,E and F to write the number sequence.

The radix of Ternary number system = 3 i.e. it uses three different symbols 0,1 and 2 to write the number sequence.

To distinguish one number system from the other, the radix of the number system is used as suffix to that number.
Eg: 10_2 Binary Number ; 10_8 Octal Number ;

10_{10} Decimal Number ; 10_{16} Hexadecimal Number

Characteristics of any number system are:

1. Base or radix is equal to the number of digits in the system,
2. The largest value of digit is one (1) less than the radix, and
3. Each digit is multiplied by the base raised to the appropriate power depending upon the digit position.

The maximum value of digit in any number system is given by (r-1).
Example: maximum value of digit in decimal number system = (10 – 1) = 9.

Binary, Octal, Decimal and Hexadecimal number systems are called positional number systems.

The number system in which the weight of each digit depends on its relative position within the number, is called positional number system.

Any positional number system can be expressed as sum of products of place value and the digit value.

Eg: $756_{10} = 7 \times 10^2 + 5 \times 10^1 + 6 \times 10^0$

$156.24_8 = 1 \times 8^2 + 5 \times 8^1 + 6 \times 8^0 + 2 \times 8^{-1} + 4 \times 8^{-2}$

The place values or weights of different digits in a mixed decimal number are as follows:

$10^5\ 10^4\ 10^3\ 10^2\ 10^1\ 10^0 \bullet 10^{-1}\ 10^{-2}\ 10^{-3}\ 10^{-4}$

decimal point

The place values or weights of different digits in a mixed binary number are as follows:

$2^4\ 2^3\ 2^2\ 2^1\ 2^0 \bullet 2^{-1}\ 2^{-2}\ 2^{-3}\ 2^{-4}$

binary point

The place values or weights of different digits in a mixed octal number are as follows:

$8^4\ 8^3\ 8^2\ 8^1\ 8^0 \bullet 8^{-1}\ 8^{-2}\ 8^{-3}\ 8^{-4}$

octal point

The place values or weights of different digits in a mixed octal number are as follows:

$16^4\ 16^3\ 16^2\ 16^1\ 16^0 \bullet 16^{-1}\ 16^{-2}\ 16^{-3}\ 16^{-4}$

Hexadecimal point

Decimal to binary conversion:

(a) Integer number: Divide the given decimal number repeatedly by 2 and collect the remainders. This must continue until the integer quotient becomes zero.

Eg: 37_{10}

Quotient	Remainder
37/2	18 + 1
18/2	9 + 0
9/2	4 + 1
4/2	2 + 0
2/2	1 + 0
1/2	0 + 1

1 0 0 1 0 1

$\therefore 37_{10} = 100101_2$

Note: The conversion from decimal integer to any base-r system is similar to the above example except that division is done by r instead of 2.

(b) Fractional number: The conversion of a decimal fraction to a binary is as follows:

Eg: $0.68755_{10} = X_2$

First, 0.6875 is multiplied by 2 to give an integer and a fraction. The new fraction is multiplied by 2 to give a new integer and a new fraction. This process is continued until the fraction becomes 0 or until the number of digits has sufficient accuracy.

Integer value

Eg: 0.6875 X 2 = 1.3750 1
0.3750 X 2 = 0.7500 0
0.7500 X 2 = 1.5000 1
0.5000 X 2 = 1.0000 1
$\therefore (0.6875)_{10} = 0.1011_2$

NOTE: To convert a decimal fraction to a number expressed in base r, a similar procedure is used. Multiplication is by r instead of 2, and the coefficients found from the integers may range in value from 0 to (r-1).

The conversion of decimal number with both integer and fraction parts separately and then combining the results together.

Eg: $(41.6875)_{10} = x_2$
$41_{10} = 101001_2$ $0.6875_{10} = 0.1011$
Since $(41.6875)_{10} = 101001.1011_2$.

Eg: Convert the Decimal number to its Octal equivalent: $153_{10} = X_8$

Integer	quotient	Remainder
153/8	= 19	+1
19/8	= 2	+3
2/8	= 0	+2

$\therefore 153_{10} = 231_8$.

Eg: $(0.513)_{10} = X_8$
0.513 X 8 = 4.104
0.104 X 8 = 0.832
0.832 X 8 = 6.656
0.656 X 8 = 5.248
0.248 X 8 = 1.984
0.984X8=7.872etc.
$(0.513)_{10} = (0.406517\ldots)_8$.

Eg: Convert 253_{10} to hexadecimal
253/16 = 15 + (13 = D)
15/16 = 0 + (15 = F) $\therefore 253_{10} = FD_{16}$.

Eg: Convert the Binary number 101101_2 to decimal.
$101101 = 2^5 \times 1 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^1 + 1 \times 2^0$

$= 32 + 8 + 4 + 1 = 45$

$(101101)_2 = 45_{10}$.

Eg: Convert the Octal number 257_8 to decimal.

$257_8 = 2 \text{ X } 8^2 + 5 \text{ X } 8^1 + 7 \text{ X } 8^0 = 128 + 40 + 7 = 175_{10}$.

Eg: Convert the Hexadecimal number IAF.23 to Decimal.

$IAF.23_{16} = 1 \text{ X } 16^2 + 10 \text{ X } 16^1 + 15 \text{ X } 16^0 + 2 \text{ X } 16^{-1} + 3 \text{ X } 16^{-2} =$

BCD (Binary Coded Decimal) : In this each digit of the decimal number is represented by its four bit binary equivalent. It is also called natural BCD or 8421 code. It is a weighted code.

Excess-3 Code : This is an un weighted binary code used for decimal digits. Its code assignment is obtained from the corresponding value of BCD after the addition of 3.

BCO (Binary Coded Octal) : In this each digit of the Octal number is represented by its three bit binary equivalent.

BCH (Binary Coded Hexadecimal) : In this each digit of the hexadecimal number is represented by its four bit binary equivalent.

Decimal Digits	BCD 8421	Excess-3	Octal digits	BCO	Hexadecimal digits	BCH
0	0000	0011	0	000	0	0000
1	0001	0100	1	001	1	0001
2	0010	0101	2	010	2	0010
3	0011	0110	3	011	3	0011
4	0100	0111	4	100	4	0100
5	0101	1000	5	101	5	0101
6	0110	1001	6	110	6	0110
7	0111	1010	7	111	7	0111
8	1000	1011			8	1000
9	1001	1100			9	1100
					A	1010
					B	1011
					C	1100
					D	1101
					E	1110
					F	1111

Don't care values or unused states in BCD code are 1010, 1011, 1100, 1101, 1110, 1111.

Don't care values or unused states in excess-3 code are 0000, 0001, 0010, 1101, 1110, 1111.

The binary equivalent of a given decimal number is not equivalent to its BCD value.

Eg: $25_{10} = 11001_2$.

The BCD equivalent of decimal number 25 = 00100101 from the above example the BCD value of a given decimal number is not equivalent to its straight binary value.

The BCO (Binary Coded Octal) value of a given Octal number is exactly equal to its straight binary value. Eg: $25_8 = 21_{10} = 101101_2$

The BCO value of 25_8 is 010101.

From the above example, the BCO value of a given Octal number is same as binary equivalent of the same number.

The BCH (Binary Coded Hexadecimal) value of a given hexadecimal number is exactly equal to its straight binary.

Eg: $25_{16} = 37_{10} = 100101_2$

The BCH value of hexadecimal number $25_{16} = 00100101$.

From this example the above statement is true.

	Binary r = 2	Octal r = 8	Decimal r = 10	Hexadecimal r = 16
(r-1)'s Complement	1's	7^{th}'s	9's	15^{th}'s
r's Complement	2's	8^{th}'s	10's	16^{th}'s

Rules of Binary addition : 0 + 0 = 0; 0 + 1 = 1; 1 + 0 = 1; 1 + 1 = 1 0 (carry)

Rules of Binary subtraction: 0 – 0 = 0; 0 – 1 = 1 (Borrow 1); 1 – 0 = 1; 1 – 1 = 0.

Example: Add the two Binary numbers 101101_2.

Augend 1 0 1 1 0 1

Addend 1 0 0 1 1 1

1 1 1 1 –

Sum 1 0 1 0 1 0 0

Example: Subtract the Binary number 100111_2 from 101101_2.

Minuend: 101101

Subtracted: -100111

Difference: 000110

Example: Multiply the Binary number 1011_2 with 101_2.

Multiplicand: 1011
Multiplier: X 101

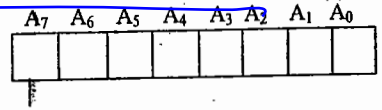
1011
0000
1011
1
Product: 110111

Example: 10011 ÷ 11

11) 10011 (110
11
11
11
01

Quotient = 110
Remainder = 1.

While storing the signed binary numbers in the internal registers of a digital computer, most significant bit position is always reserved for sign bit and the remaining bits are used for magnitude.



Sign Bit Magnitude

When the binary number is positive, the sign is represented by `0'. When the number is negative, the sign is represented by `1'.

Fixed-Point Representation and Floating Point Representation:

The representation of the decimal point (ordinary point) in a register is complicated by the fact that it is characterized by a position between two flip- flops in the register. There are two ways of specifying the position of the decimal point in a register.

(1) Fixed Point and (2) Floating Point.

The fixed point method assumes that the decimal point (or binary point) is always fixed in one position. The two positions most widely used are (1) a decimal point in the extreme left of the register to make the stored number a fraction, and (2) a decimal point in the extreme right of the register to make the stored number an integer.

Fixed point fraction Fixed point integer

The floating-point representation uses a second register to store a number that designates the position of the decimal point in the first register.

Positive numbers are stored in the registers of digital computer in sign magnitude form only.

Negative numbers can be represented in one of three possible ways.

1. Signed-magnitude representation.
2. Signed-1's complement representation.
3. Signed-2's complement representation.

Example: +9 -9
Signed –magnitude 0 0001001 (a) 1 000 1001 signed-magnitude
(b) 1 111 0110 signed-1's complement
(c) 1 111 0111 signed-2's complement

The 2's compliment of a given binary number can be formed by leaving all least significant zeros and the first non-zero digit unchanged, and then replacing 1's by 0's and 0's by 1's in all other higher significant digits.

Example: The 2's complement of 10011000_2 is 01101000.

Subtraction using 2's complement: Represent the negative numbers in signed 2's complement form, add the two numbers, including their sign bit, and discard any carry out of the most significant bit.

Since negative numbers are represented in 2's compliment form, negative results also obtained in signed 2's compliment form.

Example: 1's complement:

+6 0000110	-6 1111001	+6 0000110	- 6 1111001
+9 0001001	+9 0001001	-9 1110110	- 9 1110110
+15 0001111	+3 (1) 0000010	-3 1111100	-15 (1) 1101111
	Carry +1		Carry +1
	+3 0000011		1110000

* Example: 2's complement:

-6	1 111010	+6	0 000110	-6	1111010
+9	0 001001	-9	1 110111	-9	1110111
+3 (1)	0 000011	-3	1 111101	-15 (1)	1110001
carry				carry	

The advantage of signed 2's complement representation over the signed-1's compliment form (and the signed-magnitude form) is that it contains only one type of zero.

The range of binary integer numbers that can be accommodated in a register of length n-bits using signed-1's compliment form is given by $+(2^{n+1}-1)$ to $-(2^{n-1}-1)$ which includes both types of zero's i.e., +0 and –0. For example if n = 8, then range is +127 to –127.

The range of integer binary numbers that can be accommodated in a register of n-bits length by using signed 2 's complement representation is given by $+(2^{n-1}-1)$ to -2^{n-1} which includes only one type of zero i.e., + 0.
For example if n = 8, then range is + 127 to-128.

2's compliment form is usually chosen over 1's complement to avoid the occurrence of a negative zero. 2's compliment of zero is zero only.

The 1's complement of 1's compliment of a given number is the same number itself.

The general form of floating-point number is mr^e. Where M = Mantissa, r = base, e = exponent. Example: $+0.3574 \times 10^5$.

The Mantissa can be a fixed point fraction or fixed point integer.

Normalization: Getting non-zero digit in the most significant digit position of the mantissa is called Normalization.

If the floating point number is normalized, more number of significant digits can be stored, as a result accuracy can be improved.

A zero cannot be normalized because it does not contain a non-zero digit.

The hexadecimal code is widely used in digital systems because it is very convenient to enter binary data in a digital system using hexcode.

The parity of a digital word is used for detecting error in digital transmission.

Hollerith code is used for punched card data.

In weighted codes, each position of the number has specific weight. The decimal value of a weighted code number is the algebraic sum of the weights of those positions in which 1's appears.

Most frequently used weighted codes are 8421, 2421 code, 5211 code and 84 2'1' code.
Example: The decimal number 493 is represented in different codes as

In 8421 code : 0010 1001 0011
In 2421 code : 0100 1111 0011
In 521'1' code : 0111 1111 0101
In 842'1' code : 0100 1111 0101

Reflective Code: A code is called reflective or self complimenting if the code for 9 is the compliment for the code for 0, code for 8 is the compliment from 1 and so on. 2421, 842'1', 5211 are examples for reflected codes.

Sequential Code: A code is called sequential if each successive code is one binary number greater than its preceding code. Example: 8421

CHARACTERCODES:

An alphanumeric code is a binary code of a group of elements consisting of the ten decimal digits, the 26 letters of the alphabet, and a certain number of special symbols such as .

The total number of elements in the alphanumeric group is greater than 36. Therefore it must be coded with a minimum of six bits ($2^6 = 64$).

6-bit internal code is an alphanumeric code.

Most frequently used alphanumeric codes are
(1) ASCII (American Standard Code for Information Interchange).
(2) EBCDIC(Extended BCD Interchange Code).

ASCII is a 7-bit character code. For all practical purposes, an eight bit code is used because the eighth bit is invariably added for parity.

EBCDIC is an 8-bit character code. It uses ninth bit for parity.

When discrete information is transferred through punch cards, the alphanumeric characters use a 12-bit binary code.

Notes:

EXERCISE

1 The number system with radix 2 is known as
(a) Binary (b) Decimal (c) Octal (d) Hexadecimal

2 A group of four bits is known as
(a) bit (b) byte (c) nibble (d) word

3 The knowledge of binary number system is required for the designers of computer and other digital systems because
(a) It is easy to learn binary number system
(b) It is easy to learn Boolean algebra
(c) It is easy to use binary codes
(d) The devices used in these systems operates in binary

4 The ones complement of the binary number 10001011 is
(a) 01110100 (b) 11111111 (c) 01110101 (d) 11111110

5 The twos complement of the number 100101000 is
(a) 011010110 (b) 111111111 (c) 011010111 (d) None

6 The ones complement of ones complement of the given binary number is
(a) same binary number (b) zero (c) non-zero (d) none

7 The twos complement of the twos complement of the given binary number 1011001 is
(a) 1011000 (b) 1010110 (c) 1011001 (d) 0100111

8 The base or radix a Hexadecimal number system is
(a) 2 (b) 8 (c) 16 (d) 15

9 The number system with base or radix 8 is known as
(a) binary (b) decimal (c) octal (d) hexadecimal

10 The decimal equivalent of the binary number 101101 is
(a) 48 (b) 45 (c) 57 (d) 75

11 The decimal equivalent of the binary number 1001.0101 is
(a) 9.125 (b) 9.6125 (c) 9.3125 (d) 9.6215

12 The binary equivalent of decimal number 255 is
(a) 11111110 (b) 11111101 (c) 11111111 (d) none

13 Identify the binary number represented by the decimal number 10.625
(a) 1010.011 (b) 1010.101 (c) 1010.110 (d) none

14 The binary equivalent of the decimal number 0.6875 is
(a) 0.1010 (b) 0.1011 (c) 0.1101 (d) 0.0110

15 The octal equivalent of the decimal number 375 is
(a) 560 (b) 567 (c) 565 (d) none

16 The octal equivalent of the decimal number 27.125 is
(a) 33.23 (b) 33.28 (c) 33.1 (d) 33.01

17 The decimal equivalent of the octal number 237 is
(a) 159 (b) 165 (c) 162 (d) 160

18 The hexadecimal equivalent of the decimal number 375 is
(a) 177 (b) 17A (c) 1A0 (d) none

19 The decimal equivalent of the hexadecimal number "BEED" is
(a) 47877 (b) 48877 (c) 48777 (d) none

20 Encode the decimal number 327.87 in BCD code
(a) 0011 0010 0111. 1000 1001 (b) 0011 0010 0110. 1001 1000
(c) 0011 0010 0111. 1100 1010 (d) none

21 The decimal equivalent of the hexadecimal number 3A.2F is
(a) 58.1835 (b) 58.1385 (c) 58.23 (d) none

22 The decimal number 13 is represented in natural BCD as
(a) 1101 (b) 0001 0011 (c) 0000 1101 (d) none

23 The binary equivalent of the hexadecimal number A0B5 is
(a) 1010 0001 1011 0101 (b) 1010 0000 1010 0101
(c) 1010 0000 1011 0101 (d) none

24 The octal equivalent of the binary number 11010111 is
(a) 656 (b) 327 (c) 653 (d) D7

25 The decimal equivalent of the binary number 11010111 is
(a) 215 (b) 225 (c) 250 (d) none

26 The octal equivalent of the decimal number 215 is
(a) 327 (b) 372 (c) 237 (d) none

27 The maximum positive and negative numbers which can be represented in twos complement form using n bits are respectively
(a) $+(2^{n-1}-1), -(2^{n-1}-1)$ (b) $+(2^{n-1}-1), -2^{n-1}$
(c) $+2^{n-1}, -2^{n-1}$ (d) $+2^{n-1}, -(2^{n-1}+1)$

28 When two n-bit binary numbers are added then the sum will contain at the most
(a) n-bits (b) (n+1)-bits (c) (n+2)-bits (d) (n+ n)-bits

29 The largest positive number that can be stored in a computer that has 16-bit word length and uses twos complement arithmetic is
(a) 32 (b) 32767 (c) 32768 (d) 65536

30 The maximum positive and negative numbers that can be represented in ones complement using n-bits are respectively
(a) $+(2^{n-1}-1)$ and $-(2^{n-1}-1)$ (b) $+(2^{n-1}-1)$ and -2^{n-1}
(c) $+2^{n-1}$ and $-(2^{n-1}-1)$ (d) None of these

KEY

01. a	02. c	03. d	04. a	05. d	06. a	07. c	08. c	09. c	10. b
11. c	12. c	13. b	14. b	15. b	16. c	17. a	18. a	19. b	20. a
21. a	22. b	23. c	24. b	25. a	26. a	27. b	28. b	29. b	30. a

POINTS TO REMEMBER

→ Boolean algebra works with binary variables.

→ A Boolean algebra is an algebraic system consisting of the set {0,1}, the binary operations called OR, AND, or NOT denoted by the symbols "+", ".", and "prime".

→ Boolean algebra enables the logic designer to simplify the circuit used, achieving economy of Construction and reliability of operation.

→ Boolean algebra suggests the economic and straightforward way of describing the circuitry used in any computer system.

→ Boolean algebra is unique in the way that; it takes only two different values either 0 or 1. It does not have negative number. It does not have fraction number.

→ The basic Boolean postulates:

Logical Multiplications based on AND function.

1. 0.0 = 0
2. 0.1 = 0
3. 1.0 = 0
4. 1.1 = 1

Logical Additions based on OR function

1. 0 + 0 = 0
2. 0 + 1 = 1
3. 1 + 0 = 1
4. 1 + 1 = 1

Complement based on NOT function.

9. 0' = 1
10. 1' = 0

→ Boolean properties :

a) Properties of AND function

1. X.0 = 0
2. 0.X = 0
3. X.1 = X
4. 1.X = X

b) Properties of OR function

5. X + 0 = X
6. 0 + X = X
7. X + 1 = 1
8. 1 + X = 1

c) Combining a variable with itself or its complement

9. X.X' = 0
10. X.X = X
11. X + X = X
12. X + X' = 1
13. (X')' = X

d) Commutative laws:

14. x.y = y.x
15. x + y = y + x

e) Distributive laws:

16. x(y + z) = x.y + x.z
17. x + y.z = (x + y)(x + z)

f) Associative laws:

18. x(y.z) = (x.y)z
19. x+(y + z) = (x + y)+z

g) Absorption laws:

20. x + xy = x
21. x(x + y) = x
22. x + x'y = x + y
23. x(x' + y) = xy

h) Demorgan's laws.

24. (x + y)' = x' . y'
25. (x . y)' = x' + y'

→ In Boolean algebra '1' is called multiplicative identity and '0' is called additive identity.

→ Literal: A primed or unprimed Boolean variable is called literal. Each variable can have maximum of two literals. Example : x is a variable which can have two literals x and x'.

Proof for some important properties:

17. x+yz = (x+y)(x+z)

(x+y)(x+z) = x.x + x.z + x.y + y.z
= x + xz + xy + yz
= x(1+z)+xy+yz
= x+xy+yz since (1+z) = 1
= x(1+y) + yz = x+ yz since (1+y) = 1

22. x + x'y = x+y
x + x'y = (x+x')(x+y) = x+y.

23. x(x'+y) = xy
x(x+y) = xx' + xy = 0+ xy = xy

→ Logic Circuits can be simplified by simplifying the Boolean equation using any one of the following methods:

a) Applying Boolean properties
b) Karnaugh-map method of simplification
c) Tabulation method.

→ Boolean properties can be applied successively to minimize the given Boolean equations. But there is no guarantee that always we get minimal equation in this method.

→ 2,3 and 4 variable equations can be simplified to minimal value quickly using K-map method.

→ Tabulation method is used to minimize the equations with high order variables.

→ The properties of Boolean Algebra are useful for the simplification of Boolean equation leading to minimal gate structure.

→ Simplify the Boolean equation z = xy + x' (x + y).

xy + x'(x + y) = xy + x'.x + x'y = xy + x'y
= (x + x')y = y.

→ **Duality Principle**: The important property of Boolean algebra is the duality principle. "It states that every algebraic expression deducible from theorems of Boolean algebra remains valid if the operators and identify elements are interchanged.
Examples:

x+x = x	x.x = x	by duality
x+1 = 1	x.0 = 0	by duality
x+xy = x	x(x+y) = x	by duality
x+y = y+x	xy = yx	by duality
x + (y+z) = (x+y) + z	x(yz) = (xy)z	by duality

→ The dual of the exclusive – OR is equal to its complement.

→ A simple procedure to find the complement of a function is to take the dual of the function and complement each literal.

→ **Standard product or a minterm (m)**: Consider two binary variables x and y combined with an AND operation. Since each variable appears in direct form or in its complement form there are four possible combinations. X' Y', X' Y, XY' and XY. Each of these four AND terms is called a minterm or a standard product term.

X	Y	minterm (m)
0	0	X' Y' m_0
0	1	X'Y m_1
1	0	XY' m_2
1	1	XY m_3

→ **Standard sum or Maxterm (M):** Two binary variables x and y combined with an OR operation we will get four possible combinations X + Y, X + Y', X' + Y and X'+Y'. Each of these four OR terms is called a maxterm or a standard sum term.

X	Y	Maxterm (M)
0	0	X + Y M_0
0	1	X + Y' M_1
1	0	X' + Y M_2
1	1	X' + Y' M_3

→ Maxterm is the compliment of its corresponding Minterm and vise versa.
Eg: XY = minterm.
The compliment of minterm = (XY)' = X' + Y' = maxterm

→ **Canonical form:** Expressing the Boolean function in Standard Sum of Product form (SSOP) or Standard Product of Sums form(SPOS) is called Canonical form.

→ A Boolean function may be expressed algebraically from a given truth table by forming a minterm for each combination of the variables which produces a 1 in the function, and then taking the OR of all those terms.

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0

F (X,Y) = XY' + X' Y = Σ m(1,2). This representation is called SSOP form.

→ A Boolean function may be expressed algebraically from a given truth table by forming the maxterms for each combination of the variables which produces zero '0' in the function, and then taking the AND of all those terms.

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0

F = (X + Y)(X' + Y') = Π M(0,3).
This representation is called SPOS form.

→ If one canonical form is given it is possible to express other canonical form.
Example: The other canonical form of the equation F (X,Y,Z) = Π M(0,2,3,6) is

F (X,Y,Z) = Σ m(1,4,5,7).

→ Sum of all the minters of a given Boolean function is equal to 1.

Example: (X,Y,Z) = Σ m(0,1,2,3,4,5,6,7) = 1

→ Product of all the maxterms of a given Boolean function is equal to 0.

Example: $F(X,Y,Z) = \Pi M(0,1,2,3,4,5,6,7) = 0$.

→ Boolean functions expressed as a sum of minterms or product of maxterms are said to be in canonical form.

→ Sum of products form can be implemented by using two-level gate network NAND-NAND logic.

→ NAND-NAND realization is same as AND-OR.

→ Product of sums form can be implemented by using two-level gate network NOR-NOR logic.

→ NOR-NOR realization is same as OR-AND.

→ If the signals are propagating through two stages of gates, then it is called two level gate network.

→ **Degenerative Form:** A two level gate network is said to be degenerative if it degenerates to a single operation.

Example: AND - AND is equivalent to AND

→ **The following two level gate networks are Degenerative forms:**

AND - AND	AND
OR - OR	OR
OR - NOR	NOR
AND - NAND	NAND
NOR - NAND	OR
NAND - NOR	AND

KARNAUGH MAPS (K-maps):

→ A map is a diagram made up of squares. Each square represents either a minterm or a maxterms.

→ The number of squares in the Karnaugh map is given by 2^n where n = number of variable.

→ Two variable K-map consists of 4-cells or squares.

→ Three variable K-map consists of 8-squares or 8 cells.

→ Four variable K-map consists of 16-squares or 16 cells.

→ To maintain adjacency property Gray code sequence is used in K-maps. (Any two adjacent cells will differ by only one bit).

→ **Two variable K-map:**

Each cell represents a term of two literals.
Grouping two adjacent (pair) squares containing 1's represents a term of one literal.
Grouping four adjacent squares containing 1's represent the function =1.

X \ Y	0	1
0	X'Y'	X'Y
1	X Y'	XY

→ **Three variable K-map:**

X \ YZ	00	01	11	10

Each cell represents a term of three literals.

Grouping two adjacent cells containing 1's (Pair) represent a term of two literals.

Grouping four adjacent cells containing 1's (Quad) represent a term of one literal.

Grouping eight adjacent cells containing 1's represents the function =1.

→ **Four variable K-map:**

WX \ YZ	00	01	11	10

→ Each cell or square represents one minterm, giving a term of four literals.

→ Grouping two adjacent squares containing 1's represents a term of three literals.

→ Grouping four adjacent squares containing 1's represents a term of two literals.

→ Grouping eight adjacent squares containing 1's represents a term of one literal.

→ Grouping sixteen adjacent squares containing 1's represent the function = 1. (a term of zero literals).

→ Rules to simplify K-maps: 1.At the time of grouping the adjacent cells containing 1's always use maximum possible group. 2. All the cells containing 1's must be covered at least once in any group. 3. At the time of grouping don't care (X) values can be taken as 1's. 4. All don't care values need not be covered.

→ Tabulation method is used to simplify Boolean expressions when there are more than 5 variables.

→ In an n-variable K-map combining 8 adjacent cells containing 1's as a group will result a term of (n-3) literals.

→ In an n-variable K-map combining 8 adjacent cells containing 1's as a group will eliminate 3 variables.

Number of variables	No. of cells containing 1's grouped	No. of variables eliminated	No. of literals present in the resulting term
2	4	2	0
	2	1	1
	1	0	2
3	8	3	0
	4	2	1
	2	1	2
	1	0	3
4	16	4	0
	8	3	1
	4	2	2
	2	1	3
	1	0	4

→ Sum of Number of variables eliminated and number of literals present in the resulting term is always equal to the number of variables in the K-map.

POINTS TO REMEMBER

→ A gate is an electronic circuit with one output and one or more inputs. The output always depends on the input combinations.

→ AND, OR and NOT gates are called Basic gates.

→ NAND and NOR gates are called Universal gates, because, by using only NAND gates or by using only NOR gates we can realize any gate or any circuit.

→ Special gates are Exclusive-OR gate and Exclusive-NOR gate.

→ Exclusive-NOR (X-NOR) gate is also called inclusive-OR or gate of equivalence.

→ **There are two types of logic systems:**

(a) Positive level logic system
(b) Negative level logic system

→ **Positive level logic system(PLLS):** Out of the given two voltage levels, the more positive value is assumed as logic `1' and the other as logic `0'.

Example :

Logic '0'	Logic '1'
0V	5V
-2V	+3V
-7V	- 2V
+2V	+7V

→ **Negative level logic system (NLLS):** Out of the given two voltage levels, the more negative value is assumed as logic `1' and the other as logic `0'.

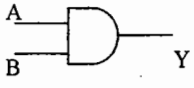
Example:

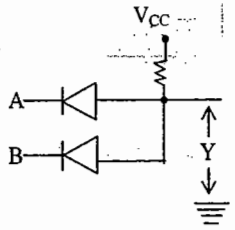
Logic '1'	Logic '0'
0V	5V
- 2V	+3V
- 7V	-2V
+ 2V	+7V

→ **AND gate :** "The output of AND gate is high if all the inputs are high." (or) "The output of AND gate is low if any one input is low or all the inputs are low."

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1





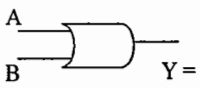
Internal Circuit diagram of AND gate with positive level logic system.

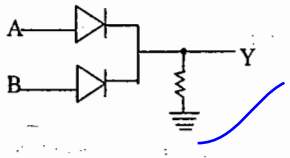
→ **OR gate** : "The output of an OR gate is high if any one input is high or all inputs are high." (or)
"The output of an OR gate is zero if all the inputs are zeros."

A	B	Y
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

Internal Circuit diagram of OR gate with positive level logic system

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1





→ The circuit, which is working as AND gate with positive level logic system, will work as OR gate with negative level logic system.

→ The circuit, which is working as OR gate with positive level logic system, will work as AND gate with negative level logic system.

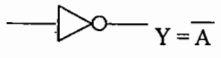
→ Truth table is also called table of combinations.

→ The number of rows in the truth table is given by 2^n where 'n' is the number of inputs to the gate.

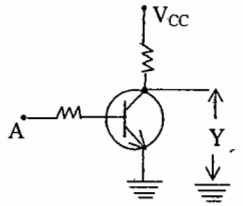
NOT gate: It is also called inverter. "The output of a NOT gate is always compliment of the input".

Truth table

A	Y
0	1
1	0



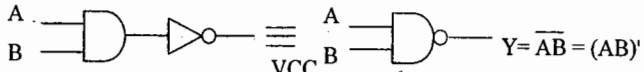
Internal Circuit



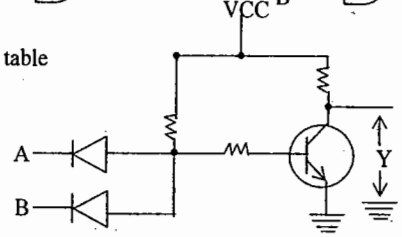
→ **NAND gate:** This is nothing but AND gate followed by NOT gate. "The output of NAND gate is high if any one input or all inputs are low."

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

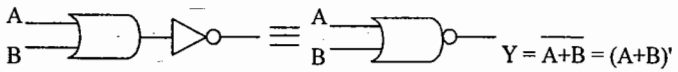


Truth table

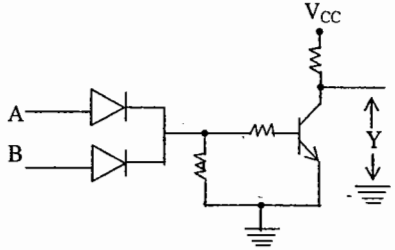


NAND with PLLS
NOR with NLLS

→ **NOR gate:** It is nothing but OR gate followed by NOT gate. " The output of NOR gate is high if all the inputs are low." (OR) "The output of NOR gate is low if any one input is high or all inputs are high."



A	B	Y
0	0	0 1
0	1	0
1	0	0
1	1	1 0

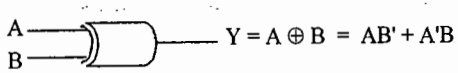


NAND with PLLS
NOR with NLLS

→ The circuit which is behaving as NAND gate with positive level logic system will behave as NOR gate with negative level logic system and vice – versa.

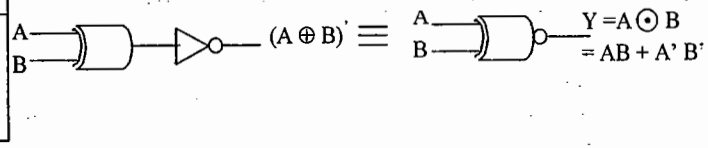
→ **Exclusive-OR gate (X-OR) :** "The output of an X-OR gate is high for odd number of high inputs."

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



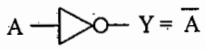
→ **Exclusive-NOR gate (X-NOR) :** It is X-OR followed by NOT. "The output is high for odd number of low inputs." (OR) "The output is high for even number of high inputs."

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

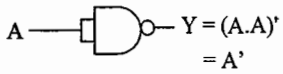


→ **Realization of Basic gates using NAND and NOR gates:**

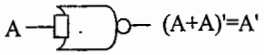
1. NOR gate

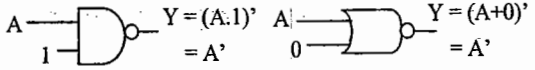


NAND

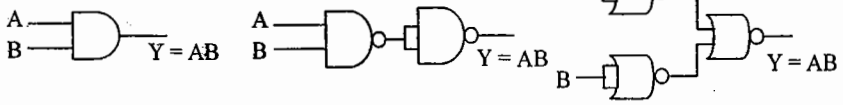


NOR

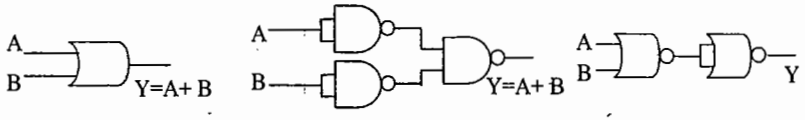




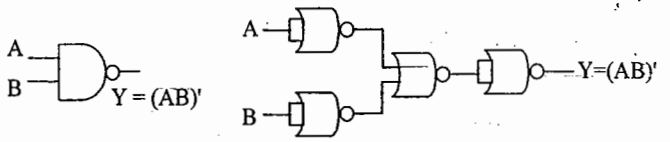
2. AND gate



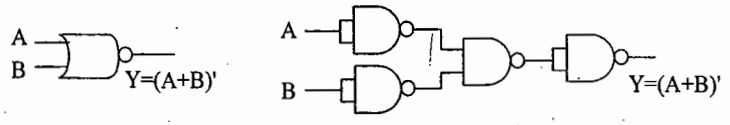
3. OR Gate



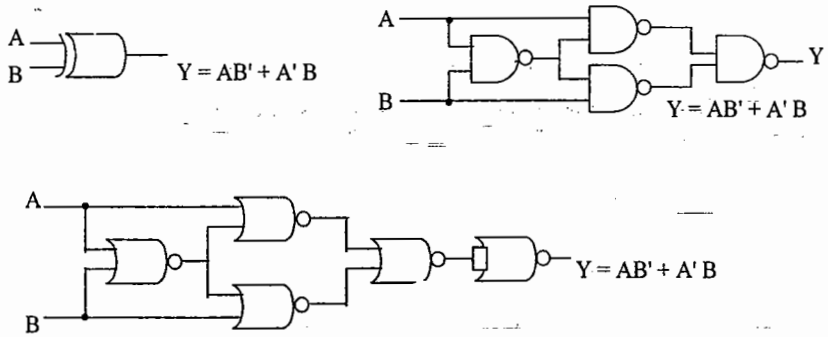
→ **Realization of NAND gate using NOR gates:**



→ **Realization of NOR gate using NAND gates:**



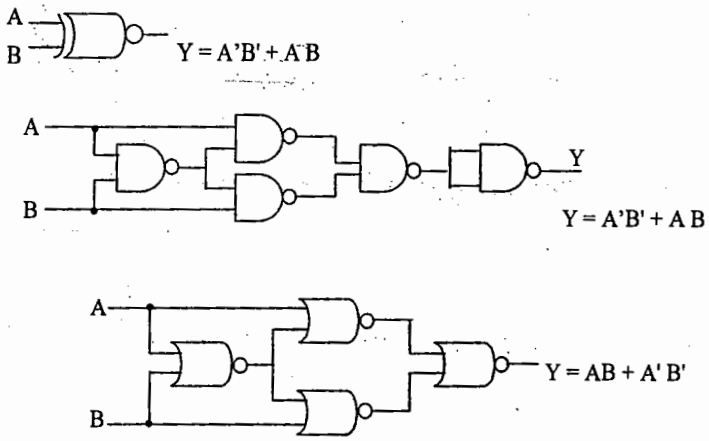
→ **Realization of X-OR gate using NAND and NOR gates:**



→ The minimum number of NAND gates required to realize X-OR gate is four.

→ The minimum number of NOR gates required to realize X-OR gate is five .

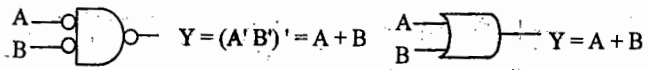
→ **Realization of X-NOR gate using NAND and NOR gates:**



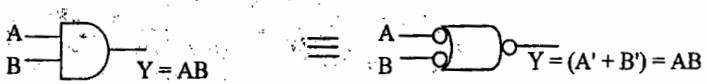
→ The minimum number of NAND gates required to realize X-NOR gate is 5.
→ The minimum number of NOR gates required to realize X-NOR gate is 4.

→ **Alternate logic gate symbols:**The alternate logic gate symbols for the standard gate symbols are obtain by interchanging AND and OR symbols, and by inverting all inputs and outputs.

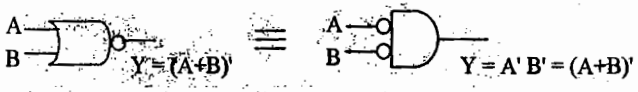
→ A bubbled NAND gate is equivalent to OR gate.



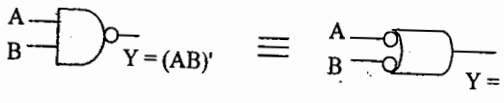
→ A bubbled NOR gate is equivalent to AND gate



* A bubbled AND gate is equivalent to NOR gate.



→ A bubbled OR gate is equivalent to NAND gate.



→ The alternate logic gate symbols for the standard gates are obtained based on Demorgan's laws only.

→ Equivalence Properties:

1. $(X \oplus Y)' = X'Y' + XY = X \odot Y$
2. $X \odot 0 = X'$
3. $X \odot 1 = X$
4. $X \odot X = 1$
5. $X \odot X' = 0$
6. $X \odot Y = X \odot Y$
7. $(X \odot Y)' = X \oplus Y$

Notes:

POINTS TO REMEMBER

→ Digital IC gates are classified not only by their logic operation, but also by the specific logic circuit family to which they belong. Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed.

→ Different types of logic gate families:

RTL Resistor transistor logic gate family.
DCTL Direct coupled Transistor Logic gate family.
RCTL Resistor capacitor transistor logic.
DTL Diode Transistor logic gate family.
TTL Transistor Logic gate family.
IIL Integrated injection Logic.
HTL High Threshold Logic.
ECL Emitter coupled logic.
MOS Metal Oxide Semi-conductor.
CMOS Complementary Metal Oxide Semi-conductor.

→ HTL is a modified form of DTL and IIL is a modified form of DCTL.

→ Because of high package density MOS and I^2L logic gate families are used for Large Scale integration (LSI) functions.

→ TTL, ECL and CMOS are used for Medium Scale Integration (MSI) or Small Scale Integration (SSI).

→ Each logic gate family is identified with a series number. For example TTL family ICs are available in 74/54 series. CMOS IC's usually designated with 4000 series and ECL family with 10000 series.

→ RTL, DTL, ECL and I^2L Logic families uses bipolar transistors. Hence these families are called bipolar logic gate families.

→ MOS and CMOS families uses unipolar transistors called Metal-Oxide Semiconductor Field- effect Transistors (MOSFETs). Hence these families are called unipolar logic gate families.

→ **Fan-out:** "The number of standard loads that the output of the gate can drive without disturbing its normal operation".

→ **Fan-in:** "The maximum number of inputs that can be applied to the logic gate".

→ **Power dissipation:** "The power consumed per gate".

→ **Propagation Delay:** "The average transition delay time for the signal to propagate from input to output when the signals change in value".

→ **Noise Margin:** "It is the limit of a noise voltage which may be present without impairing the proper operation of the circuit"

→ **Figure of Merit:** The product of propagation delay time and power dissipation is known as figure of merit of performance of a gate. Normally minimum value is desired.

→ **Logic Swing:** The difference between the two output voltages (V_{OH}-V_{OL}) is known as the logic swing of the circuit.

→ **Noise Immunity:** "The ability to with stand variations in the input levels".

→ **Saturation logic:** A form of logic gates in which one output state is the saturation voltage level of the transistor. Example: RTL, DTL, TTL.

→ **Unsaturated logic or Current Mode Logic:** A form at logic with transistors operated outside the saturation region. Example: CML or ECL.

→ ECL has ultra-fast switching speed and low logic swing.

→ The temperature range of 74-series of TTL logic gate family is 0^0 C to 70^0 C. This series of IC's is used for commercial applications.

→ The temperature range of 54-series of TTL logic gate family is -55^0 C to 125^0 C. This series of IC's is used for Military applications.

→ **Voltage parameters of the digital IC:**

High level input voltage, V_{IH}: This is the minimum input voltage which is recognized by the gate as logic 1.

Low level input voltage, V_{IL}: This is the maximum input voltage which is recognized by the gate as logic 0.

High-level output voltage, V_{OH}: This is the minimum voltage available at the output corresponding to logic 1.

Low-level output voltage, V_{OL}: This is the maximum voltage available at the output corresponding to the logic 0.

→ The number of various functions available in a logic family is known as the breadth of the logic family.

→ When the outputs of logic gates are connected together additional logic functions are performed. This is known as wired logic.

→ When the outputs are available in complemented as well as uncomplemented form it is referred to as complementary outputs. This eliminates the need of using additional inverters.

→ **Passive pull-up:** In a bipolar logic circuit, a resistance R_C used in the collector circuit of the output transistor is known as passive pull-up.

→ **Active pull-up:** In a bipolar logic circuit a BJT and diode circuit used in the collector circuit of the output transistor instead of R_C is known as active pull-up. This facility is available is TTL family.

→ The advantages of active pull-up over passive-pull up are increased speed of operation and reduced power dissipation.

→ Open collector output: In a bipolar logic circuit if nothing is connected at the collector of the output transistor and this collector terminal is available as IC pin, it is known as open-collector output.

→ Tri-state logic: In the tri-state logic, in addition to low impedance 0 and 1 there is a third state known as the high-impedance state. When the gate is disabled it is in the third state.

→ In TTL logic gate family three different types of output configurations are available: they are Open collector output type, Totem-pole output type and tri-state output type.

→ The advantages of open-collector output type are wired-logic can be performed and loads other than the normal gates can be used.

→ The tri-state logic devices are used in bus oriented systems.

→ If any input of TTL circuit is left floating, it will function as if it is connected to logic 1 level.

→ The supply voltage range of 74-series is 5 ± 0.25V and for 54-series is 5 ± 0.5V.

→ Negative supply is preferred in ECL family because, the effect of noise present in the supply line is reduced considerably and any accidental short-circuiting of output to ground will not damage the gate.

→ MOS logic is mainly used for LSI and VLSI applications because the silicon chip area required for fabrication of a MOS device is very small.

→ The fan-out of MOS logic gates is very high because of their high input impedance.

→ If any unused input terminal of a MOS gate is left unconnected, a large voltage may get induced at the unconnected input which may damage the gate.

→ Different versions available in TTL logic gate family.

- 74/54 L : Low-power
- 74/54 H : High-power/ High-speed
- 74/54 LS : Low-power Schottky
- 74/54 S : Schottky
- 74/54 AS : Advanced Schottky
- 74/54 ALS : Advanced Low-power Schottky.

→ The supply voltage required for ECL logic family is $-5.2\text{V} \pm 10\%$.

→ Comparison of Different Logic Gate families:

	DTL	TTL	ECL	CMOS	p-MOS
Fan-out	8	10	25	50	20
Propagation Delay	30n sec.	10 nsec.	4 nsec.	70 nsec.	300 sec
Power Dissipation	8mw	10mw	40mw	0.01mw.	0.2 – 10 mw
Noise Margin (min.)	700mV	400mV	200mV	300mV	150mV

→ Fastest logic gate family is ECL. It is also called Current Mode Logic.

→ Slowest Logic gate family is CMOS.

→ The logic gate family, which consumes less power CMOS.

→ The logic gate family, which consumes more power ECL.

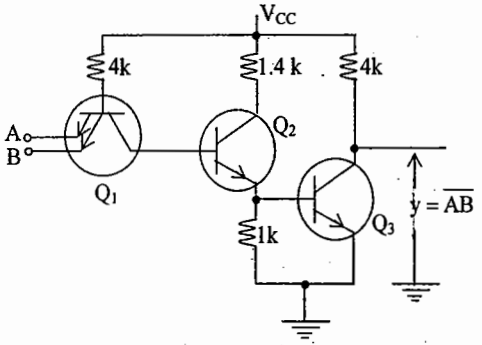
→ The logic gate family, which is having highest fan out CMOS.

→ In CMOS circuits n-MOS transistor conducts if the gate to source voltage is more positive where as p-MOS conducts if gate to source voltage is more negative.

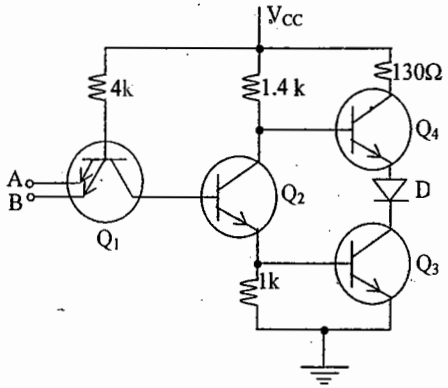
→ NMOS is faster than PMOS.

→ In tristate logic in addition to two low impedance outputs 0 and 1, there is third state known as high Impedance State.

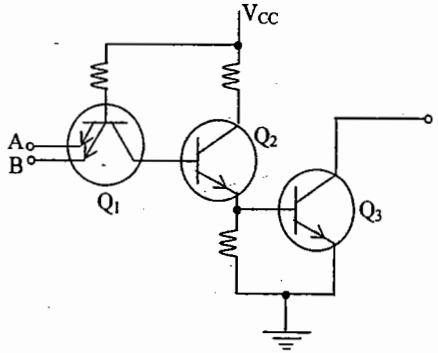
→ Standard 2 input TTL NAND gate



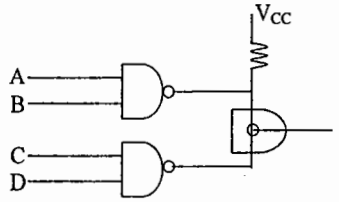
- 2 – input NAND gate with Totem-pole output configuration



- The Dido de 'D' is used to keep the transistor Q4 in OFF stats when Q3 is in ON State.
- 2 – input NAND gate with open collector output configuration.

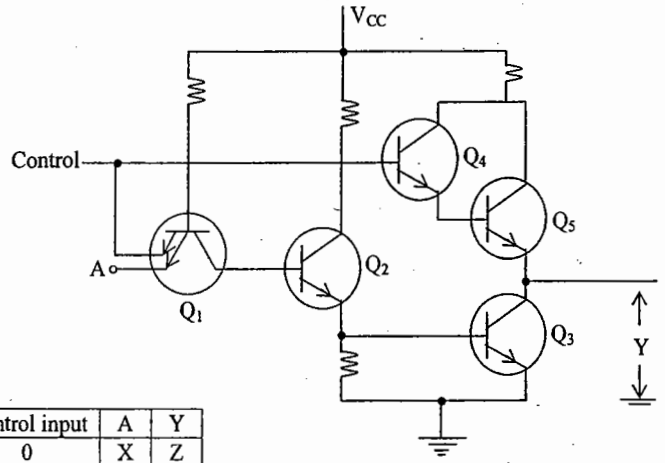


- Gates with open collector output can be used for wired – AND operation.



$Y = \overline{AB} \cdot \overline{CD} = \overline{(AB + CD)}$

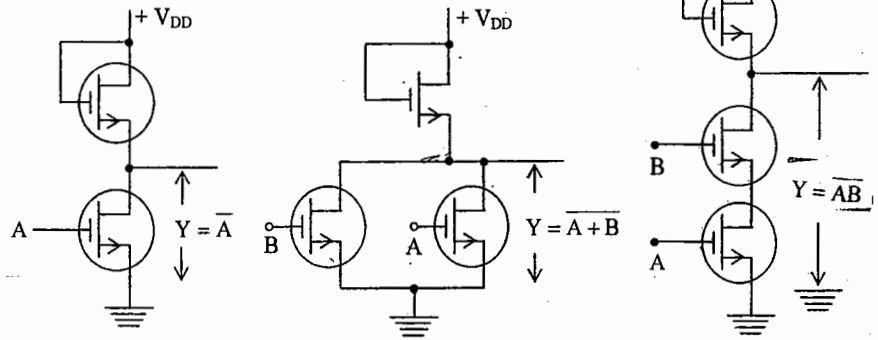
- Wired – AND operation is equivalent to AND – OR – INVERT
- Tristate output configuration – TTL circuit.



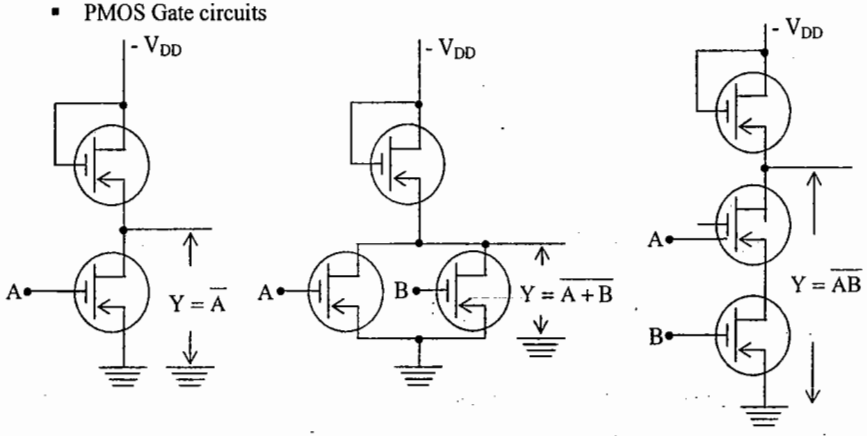
Tristate invertor

Control input	A	Y
0	X	Z
1	0	1
1	1	0

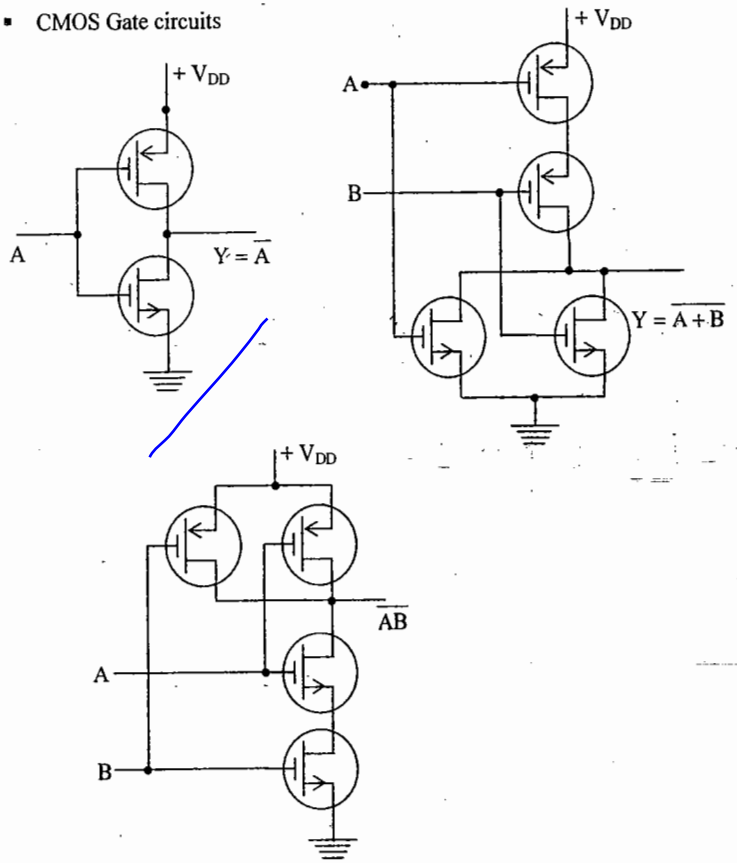
- NMOS Gate circuits



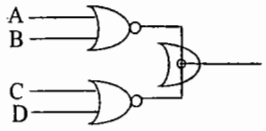
- PMOS Gate circuits



- CMOS Gate circuits



- Similar to open collector output in TTL, open emitter outputs are available in ECL. The outputs of two or more ECL gates can be connected to get additional logic without using additional hardware. Wired – OR operation is possible with ECL ckts.



$$\left(\overline{A+B}+\overline{C+D}\right)=\overline{(A+B)(C+D)}$$

- Wired – OR operation is equivalent to OR – AND – INVERT
- If any input of an ECL gate is left unconnected, the corresponding E – B junction will not be conducting. Hence it acts as if a logical 0 level voltage is applied to that input. i.e In ECL ICs, all unconnected/ floating inputs are treated as logical OS.

Notes:

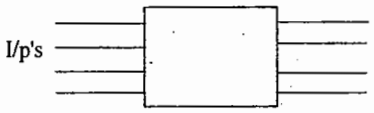
POINTS TO REMEMBER:

→ Digital circuits can be classified into two types :

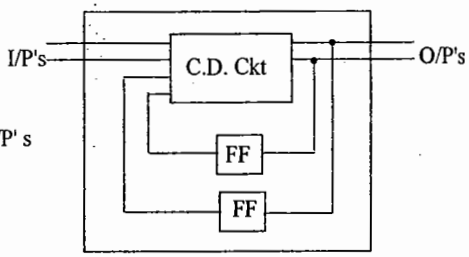
1. Combinational digital circuits and
2. Sequential digital circuits.

→ **Combinational Digital Circuits :** In these circuits "the outputs at any instant of time depends on the inputs present at that instant only."

→ For the design of Combinational digital circuits Basic gates (AND, OR, NOT) or universal gates (NAND, NOR) are used.
Examples for combinational digital circuits are Half adder, Full adder, Half subtractor, Full subtractor, Code converter, Decoder, Multiplexer, Demultiplexer, Encoder, ROM, etc.



Combinational Digital Circuit



Sequential Digital Circuit

→ **Sequential Digital Circuits** : The outputs at any instant of time not only depends on the present inputs but also on the previous inputs or outputs.
For the design of these circuits in addition to gates we need one more element flip-flop.

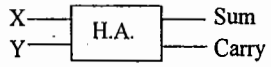
→ Examples for sequential digital circuits are Registers, Shift register, Counters etc.

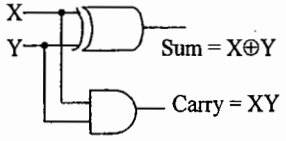
→ **Half adder:** A combinational circuit that performs the addition of two bits is called a half-adder. It consists of two inputs and two outputs.

X	Y	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Sum = X ⊕ Y= XY' + X' Y

Carry = XY



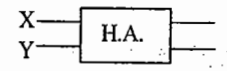


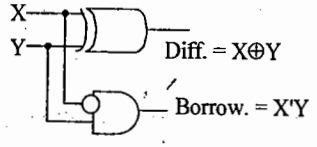
→ **Half Subtractor** : It is a Combinational circuit that subtracts two bits and produces their difference. It also has an output to specify if a '1' has been borrowed.

X	Y	Borrow	Diff
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Diff = X ⊕ Y= XY' + X' Y

Borrow = X'Y



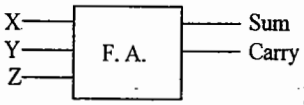


→ Half adder can be converted into half subtractor with an additional inverter.
→ Quarter Adder/Subtractor: The sum output of Half adder is called Quarter adder. The difference output of Half subtractor is called Quarter subtractor.
→ Quarter Adder/Subtractor is same as two input XOR gate.

→ **Full adder** : It performs the addition of three bits (two significant bits and a previous carry) and generates sum and carry.

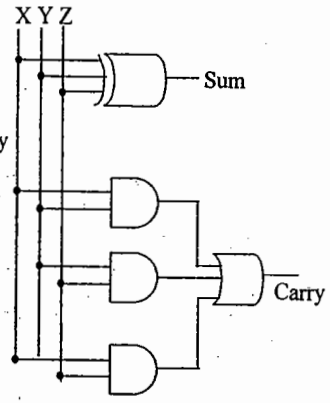
Truth Table

X	Y	Z	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

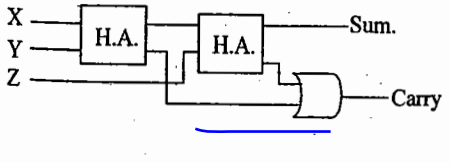


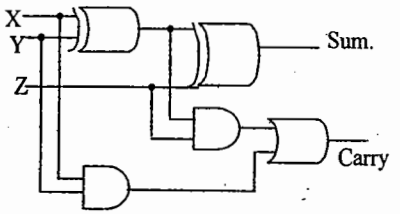
Sum = X ⊕ Y ⊕ Z

Carry = XY + YZ + ZX



→ Full adder can be implemented by using two half adders and an OR gate.

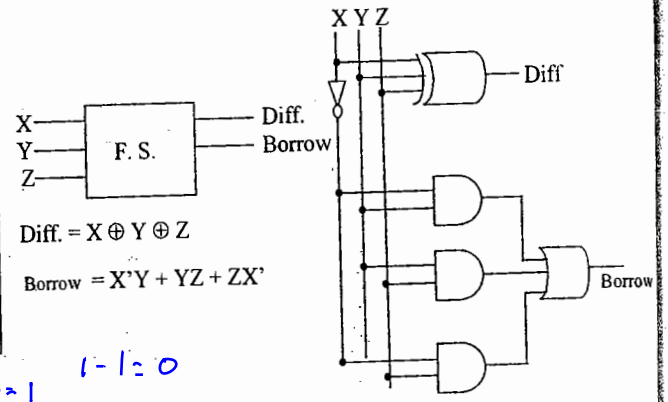




→ **Full subtractor:** It subtracts one bit from the other by taking previous borrow into account and generates difference and borrow.

Truth Table

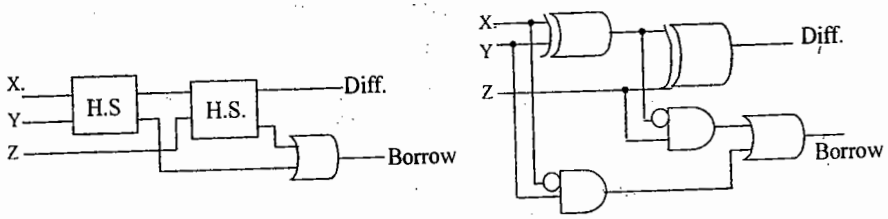
X	Y	Z	Borrow	Diff.
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Diff. = X ⊕ Y ⊕ Z

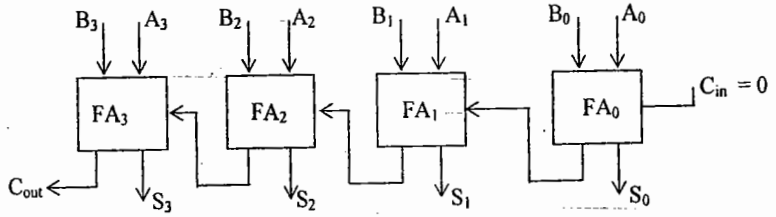
Borrow = X'Y + YZ + ZX'

Full subtractor can be implemented by using two half-subtractors and an OR gate.

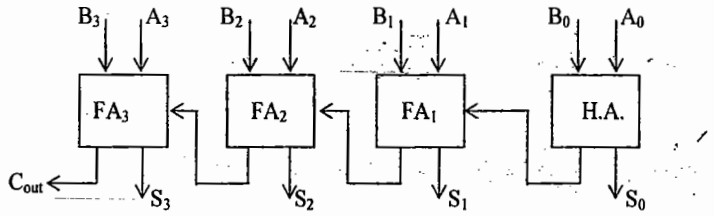


→ Four bit binary parallel adder can be constructed by using three full adders and one half adder or by using four full adders with input carry for least significant bit full adder is zero.

→ Four bit binary parallel adder shown in figure is also called as Ripple carry adder.



(OR)



→ Carry Look-Ahead adder is faster than ripple carry adder.

→ Full adder is an example for 1-bit adder.

→ **Decoder :** A decoder is a logic circuit that converts an n-bit binary input code into M (2^n) output lines such that each output line will be activated for only one of the possible combinations of inputs.

(OR)

A decoder is a Combinational circuit that converts binary information from 'n' input lines to a maximum of 2^n unique output lines.

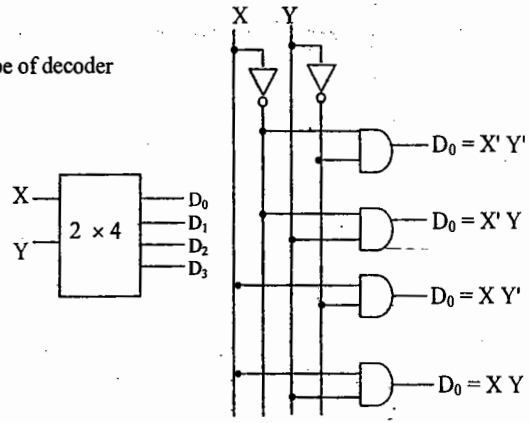
Eg : 2 X 4 line Decoder (it is also called one of four line decoder).

→ Decoders are available in two different types of output forms: (1) Active high output type decoders and (2) active low output type of decoders.

→ Active high output type of decoders are constructed with AND gates and active low output type of decoders are constructed with NAND gates.

Truth table of active high output type of decoder

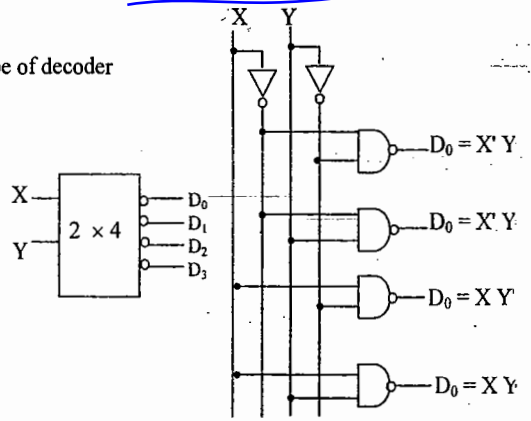
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



→ Activate low output type of decoders will give the output low for given input combination and all other outputs are high.

Truth table of active high output type of decoder

X	Y	D_0	D_1	D_2	D_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0



→ 3 to 8 line decoder is also called Binary-to-Octal decoder or converter. It is also called 1-of-8 decoder, because only one of the 8 outputs is activated at a time.

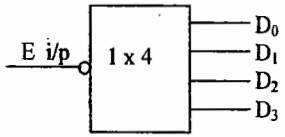
→ Decoders are widely used in the memory system of a computer, where they respond to the address code input from the CPU to activate the memory storage location specified by the address code.

→ Decoders are also used to convert binary data to a form suitable for displaying on decimal read outs.

→ Decoders can be used to implement combinational circuits, Boolean functions etc.

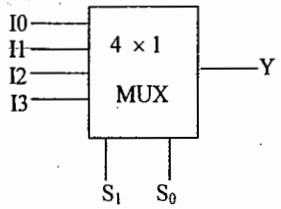
→ **Demultiplexer:** A decoder with enable input acts as a demultiplexer. "A demultiplexer is a circuit that receives information on a single line and transmits that information on one of 2^n possible output lines. The selection of specific output line is controlled by the bit values of 'n' selection lines.

E	A	B	D	D	D	D
1	X	X	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	I	0	0	0	1



Multiplexer: Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. "A digital multiplexer is a combinational circuit that selects binary information from one of many inputs lines and direct it a single output line. The selection of a particular line is controlled by a set of selection lines. Normally, there are 2^n input lines and 'n' selection lines whose bit combinations determine which input is selected."

Truth table



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

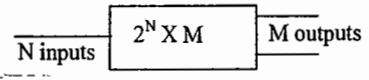
→ Multiplexers can be used for the implementation of Boolean functions, combinational circuits. They can also used for parallel to serial conversion.

→ Multiplexer is also called data selector or universal element.

→ All three variable Boolean equations can be implemented by using 8x1 multiplexer without using any additional gates. Some but not all three variable Boolean equations can also be implemented with 4x1 mux without using any additional gates.

→ **Encoder** : A decoder identifies a particular code present at the input terminals of the circuit. The inverse process is called Encoding. "An Encoder has number of inputs (2^n) one and only one of which is in the high state or active, and an n-bit code is generated upon which of the inputs is excited.

→ **ROM (Read Only Memory) :** ROM is nothing but the combination of decoder and Encoder. It is a semi-conductor memory and which is a permanent memory. ROM can also be defined as a Simple Code conversion unit.



→ The memory which is constructed by using only gates is ROM.

POINTS TO REMEMBER:

→ Two cross coupled inverters will form a basic latch which can store one bit of information.

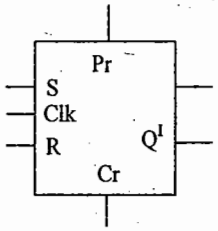
→ Flip-Flops : Flip-Flop is also called Bistable multivibrator or binary. It can store one bit of information.

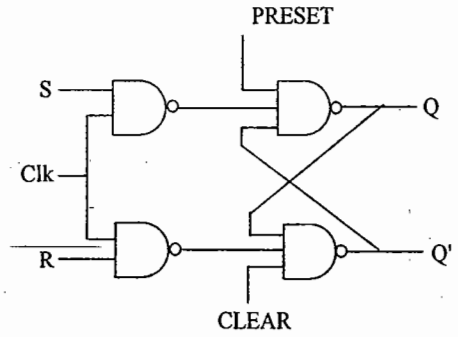
→ In a flip-flop one output is always complement of the other output.

→ Flip-Flop has two stable states.

→ **Clocked S-R Flip-flop :** It is called Set-Reset Flip-Flop.

S_n	R_n	Q_{n+1}	
0	0	Q_n	No change
0	1	0	Reset
1	0	1	Set
1	1	*	





→ N_1 and N_2 from a basic latch. N_3 and N_4 are called Steering gates or Control gates, because they are used to control the outputs.

→ S and R inputs are called synchronous inputs. Preset (Pr) and Clear (Cr) inputs are called direct inputs or asynchronous inputs.

→ The output of the flip-flop changes only during the clock pulse. In between clock pulses the output of the flip-flop does not change.

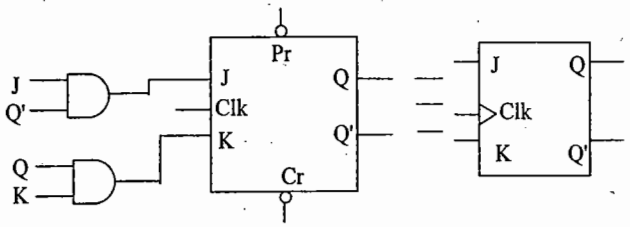
→ During normal operation of the flip-flop, preset and clear inputs must be always high.

→ The disadvantage of S-R flip-flop is S = 1, R = 1 output can not be determined. This can be eliminated in j-k flip-flop.

→ S - R flip-flop can be converted to j - k flip-flop by using the two equation S = JQ' and R = KQ.

Truth table

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\dot{Q}'_n$



→ Race around problem is present in the j-k flip-flop, when both J = K = 1.

→ Toggling the output more than once during the clock pulse is called Race around Problem

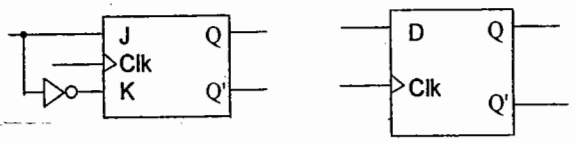
→ The Race around problem in J-K flip-flop can be eliminated by using edge triggered flip - flop or Master slave J-K flip-flop or by using the clock signal whose pulse width is less than or equal to the propagation delay of flip-flop.

→ Master-slave flip-flop is a cascading of two J-K flip-flops Positive or direct clock pulses are applied to master and these are inverted and applied to the slave flip-flop.

→ **D-flip-flop** : It is also called a Delay flip-flop. By connecting an inverter in between J and K input terminals, D flip-flop is obtained. K always receives the compliment of J.

Truth table

D	Q_{n+1}
0	0
1	1

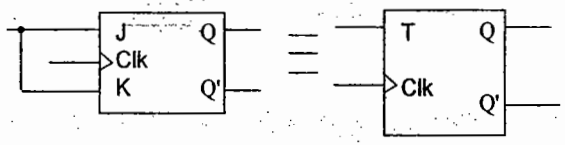


→ D flip-flop is a binary used to provide delay. The bit on the D line is transferred to the output at the next clock pulse.

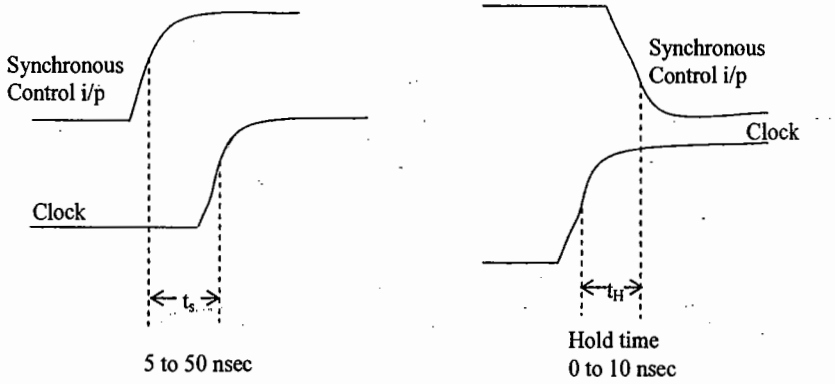
* **T flip-flop :** J K flip-flop can be converted into T-flip-flop by connecting J and K input terminals to a common point. If T = 1, then $Q_{n+1} = Q_n$. This unit changes state of the output with each clock pulse and hence it acts as a toggle switch.

Truth table

T	Q_{n+1}
0	Q_n
1	Q_n'



If X KHz clock signal is applied to a T flip-flop when T = 1, then the output (Q) signal frequency is given by X/2 KHz. Thus it acts as a frequency divider.



Setup Time (t_s) : Time interval immediately preceding the active transition of clock signal during which the control input must be maintained at the proper level.

Hold Time (t_H) : The time interval immediately following the active transition of the clock signal during which the synchronous control input must be maintained at the proper level.

Registers and Shift Registers :

→ A register is a group of flip-flops used to store binary information. An n-bit register can store n - bit information.

→ A register which is able to shift the information either from left to right or from left to right is called a shift register.

→ Shift register can perform four different operations.

1. Serial input - Parallel output.
2. Serial input - Serial output
3. Parallel input - Parallel output
4. Parallel input - Serial output.

→ **Universal Shift Register :** A register which is able to shift the information form left to right or from right to left and which can perform all four operations is called universal shift register.

→ **Applications of Shift registers :**

1. Serial to parallel conversion (It is also called spatial to temporal code conversion)
2. Parallel to serial conversion (It is also called temporal to spatial code conversion)
3. Sequence generator.
4. Multiplication and Division.
5. Ring counter and Twisted ring counter.
6. Digital delay line (serial input and serial output operations

→ Left shift operation is nothing but multiplied by 2.

Eg : Q_3 Q_2 Q_1 Q_0

0 1 0 1 = 5

1 0 1 0 = 10

Shift left by n-positions is equivalent to multiplication by 2^n.

→ If least significant bit = 0, then right shift operation by one position is same as Division by 2.

Eg: Q_3 Q_2 Q_1 Q_0

1 0 1 0 = 10

0 1 0 1 = 5

If L.S.B = 1, then right shift operation gives integer division by 2.

Eg: Q_3 Q_2 Q_1 Q_0

0 1 0 1 = 5

0 0 0 0 = 2 (instead of 2.5)

→ **Ring Counter** : Shift register can be used as ring counter when Q_0 output terminal is connected to serial input terminal.

→ An n-bit ring counter can have "n" different output states. It can count n-clock pulses.

→ **Twisted Ring counter** : It is also called Johnson's Ring counter. It is formed when Q_0' output terminal is connected to the serial input terminal of the shift register.

→ An n-bit twisted ring counter can have maximum of 2n different output states.

COUNTERS :

The Counter is driven by a clock signal and can be used to count the number of clock cycles. Counter is nothing but a frequency divider circuit.

→ Two types of counters are available :
1. Synchronous. 2. Asynchronous.

→ Synchronous counters are also called parallel counters. In this type of counters the clock pulses are simultaneously applied to all the flip-flops.

→ Asynchronous counters are also called Ripple or serial counters. In this type of counters the output of one flip-flop is connected to the clock input of next flip-flop and so on.

→ A counter having n-flip-flops can have 2^n output states i.e. it can count 2^n clock pulses (0 to 2^n-1).

→ The largest binary number that can be represented by an n-bit counter has a decimal equivalent of (2^n-1). Example.: n = 3, then $2^n - 1 = 2^3 - 1 = 7$.

→ A counter can be made to count either in the up mode or in the down mode.

→ Synchronous counters are faster than asynchronous counters.

→ The modulus of a counter is the total number of states through which the counter can progress. For example mod-8 counter is having 8 different states (000 to 111).

→ The output signal frequency of Mod-n counter is $1/n^{th}$ of the input clock frequency. Hence that counter is also called ÷ n counter.

→ The number of flip-flops (n) required to construct Mod N counter can be obtained from the following formula:

$$2^{n-1} < N \leq 2^n.$$

→ A decade counter is also called Mod- 10 or ÷10 counter requires 4 flip-flops.

→ Any binary counter can be a modulus counter where as the modulus counter need not be a binary counter.

→ Six flip-flops are required to construct mod-60 counter.

POINTS TO REMEMBER:

→ The digital computer memory can be classified into two types: Primary memory or main memory and Secondary memory or Auxiliary memory.

→ Primary memory or main memory: The memory, which is directly accessible to the CPU, is called main memory. Eg: ROM, RAM.

→ Secondary memory or Auxiliary memory: The memory, which is not directly accessible to the CPU, is called secondary memory. Eg: Hard disk, Floppy disk, Magnetic tape etc.

→ Primary memories are semiconductor memories. They are available in the form of integrated circuits with different memory capacities.

→ The capacity of a memory IC is represented by 2^nxm, where '2^n' represents number of memory locations available and 'm' represents number of bits stored in each memory location. Eg: 2^{10} x 8 = 1024 x 8.

→ The number of address bits required to identify 2^n memory locations are "n".
Eg: to identify one out of 1024 (2^{10}) memory locations, 10-adress bits are required.

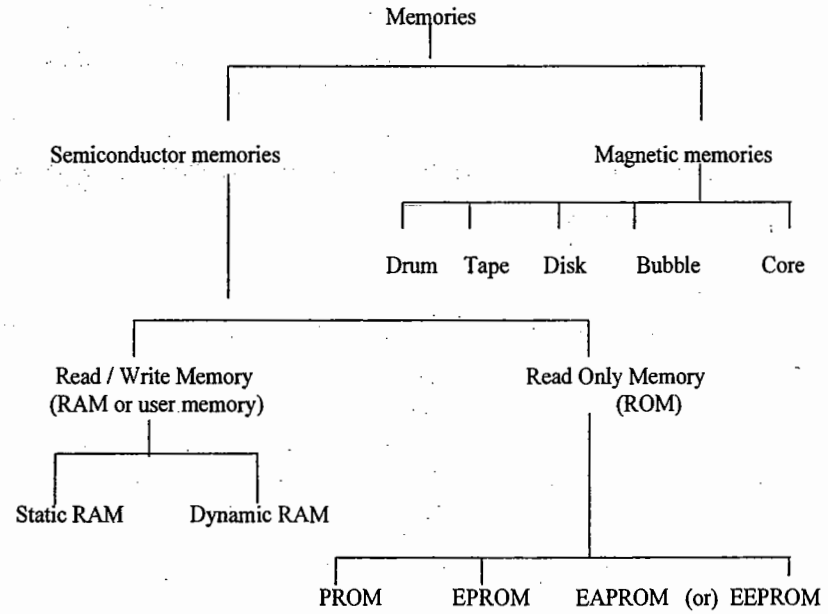
→ Assigning addresses for different memory locations of a memory IC is called memory mapping.

→ To increase the bit capacity or length of each memory location, the memory ICs are connected in parallel and the corresponding memory location of each IC must be selected simultaneously.
Eg: 1024 X 8 memory capacity can be obtained by using four memory ICs of memory capacity 1024 X 2.

→ To increase the number or memory locations (i.e. explanation of memory), the memory ICs are connected such that at any time only one memory IC must be selected.
Eg: To get 4kX8 memory capacity, it is required to use four 1kX8 memory ICs, and at any time one of four memory ICs can be selected using a decoder.

→ The number of memory Ics of capacity 1kX4 required to construct a memory of capacity 8k X 8 are 16.(i.e.16 memory Ics of 1kX4 capacity are required to construct 8kX8 memory).

Types of memories:-



Memory device parameters or characteristics:

→ Access time: The access time of a memory is defined as the time required to access a memory location for reading or writing.

→ The access time of a magnetic drum is defined as the sum of seek time and transfer time.

→ **Access rate:** It is defined as the reciprocal of access time. It is measured in words per second.

→ Access time depends on the physical characteristics of the storage medium, and also on the type of access mechanism used.

→ **Access models**: An important property of a memory device is the order or sequence in which information can be accessed.

→ **Random Access**: It the access time is independent of position of the memory location, then it is called random-access mode. I.e. The access time of every memory location is same. Eg: ROM, CAM (content addressable memory)

→ **Sequential Access**: A memory in which the locations can be accessed in a sequence only is referred to as a sequential memory. Ex: Magnetic tape, magnetic bubble

→ Some memory devices such as magnetic disks or drums contain a large number of independent rotating tracks. If each track has its own read-write head, the tracks may be accessed randomly, although access within each track is serial. In such cases the access mode is same times called semi random or direct access.

→ **Alterability:** The method used to write information into a memory may not be irreversible, in that once information has been written, it can not be alterable while the memory is in use i.e. on-line.

→ Memory whose contents can not be altered on-line are called ROM's.

→ ROMs whose contents can be changed are called PROM's.

→ Memories in which reading or writing can be done on-line are called R/W Memories.

→ **Volatile memory**: In this type of memory, the stored information is dependent on power supply i.e. the stored information will remains as it is as long as power is applied Eg: RAM.

→ **Non-volatile memory**: In this type of memory, the stored information is independent of power supply. I.e. the stored information will present as it is even if the power fails.
Eg: ROM, PROM, EPROM, EEPROM etc.

PROM: Programmable Read Only Memory
EPROM: Erasable programmable Read Only Memory
EPROM or EPROM: Electrically Erasable Programmable Read Only Memory
EAPROM: Electrically Alterable Programmable Read Only Memory

→ Static RAM (SRAM): In this type of memory binary information is stored in terms of voltage. SRAMs stores ones and zeros using conventional Flip-plops.

→ Dynamic RAM (DRAM): In this type of memory, binary information is stored in terms of charge on the capacitor. The memory cells of DRAMs are basically charge storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted as logical 1 or 0.

→ Because of the leakage property of the capacitor, DRAMs require periodic charge refreshing to maintain data storage.

→ The package density is more in the case of DRAMs. But additional hardware is required for memory refresh operation.

→ SRAMs Consume more power when compared to RAMs. SRAMS an faster than DRAMs.

→ Destructive Read Out Memory: The memory is known as destructive Read Out (DRO) memory if the reading method destroys its contents. For such memories each read operation must be followed by write operation to restore the contents. Ex. Magnetic Core.

→ Non-destructive Read Out (NDRO): It is called NDRO if the reading operation does not change its contents. Ex: Magnetic tapes, disks, RAMs, ROMs, etc.

→ Semiconductor technologies used for fabrication of memories are
(a) Bipolar and (b) Unipolar (i.e. MOS)

→ CCD (charge coupled Device) is a volatile memory and sequential access-type.

→ Low cost and high access rates are desirable memory characteristics.

→ By changing the hardware logic used for the chip selection of memory IC, it is possible to change the memory mapping.

Notes:

→ Digital to analog conversions needed in digital data processing requires insulation of digital information to an equivalent analog information.

→ Digital to analog converters, may be used to translate the output of a digital system into an analog form for the purpose of driving a pen recorder or for a cathode ray oscilloscope.

→ The D/A converter is commonly referred to as a decoding device, since it is used to decode the digital signals into proportional voltage or current signals for an entry into an analog system.

→ D/A converter converts digital information into corresponding analog signals.

→ There are two types of DAC' s are available
a) Binary weighted resistors type of DAC and
b) R –2 R ladder type of DAC

→ The R – 2R ladder type of DAC is superior type of DAC.

→ Binary weighted resistors type of DAC has many drawbacks.

→ When the number of input bits is large, the resistors used for LSB has to be very large value.

→ Each resistor required in the network is of different value, as such the resistors used are to be chosen from wide range of values.

→ If each higher bit resistor is not exactly half of the previous bit resistor, the step size will change.

→ The advantage of R – 2R ladder type of DAC over Binary weighted resistor type of DAC
a) Better linearity and
b) It requires only two different types of resistors with values R and 2R.

→ **A Linearity :** A D/A converter is said to be ideally or perfectly linear, if it gives equal increments in the analog output voltage for equal increments in the numerical value of the digital value.

→ **D/A Resolution :** It is defined as the smallest change in the analog output voltage corresponding to a change of one bit in the digital input.

→ The percentage resolution of an n – bit DAC is given by $\frac{1}{2^n - 1} \times 100$

→ The resolution of an n – bit DAC with a range of output voltage from 0 to V volts is given by $\frac{V}{2^n - 1}$ Volts

→ **Settling time of DAC :** It is defined as the time required for the analog output voltage to reach and stay within a specified limit, after application of a digital input.

→ **Monotonicity :** A DAC is said to be monotonic if its output voltage increases regularly as its binary digital input signals is increased from one value to the next value. Output wave form should be perfectly staircase with no downward steps, as input is increased for a proper monotonic DAC.

→ The accuracy of a D/A converter is a measure of the difference between the actual analog output voltage and what the output should be in the ideal case.

→ An analog to digital converter ADC converts analog voltages into the corresponding digital code.

→ An ADC usually considered as an encoder.

→ The conversion time ADC is the time required for conversion of one analog sample to corresponding digital code.

→ Different types of ADC's are available :

→ Simultaneous ADC or parallel comparator of Flash type of ADC

→ Counter type of ADC or pulse width type of ADC

→ Integrator type of ADC or single slope of ADC

→ Dual slope integrator ADC

→ Successive approximation type ADC etc.

→ Flash type of ADC is the fastest type of ADC

→ An n – bit Flash type of ADC requires $2^n - 1$ comparators.

→ Counter type of ADC uses linear search and successive approximation type of ADC uses binary search.

→ Ring counter is used in successive approximation type of ADC.

→ **ADC Resolution :** It is defined as the change in the input voltage required for a one – bit change in the output.

→ An ADC having an analog range of -V/2 to + V/2 and n – bit digital output has a resolution of $V/(2^n - 1)$ volts.

→ Dual slope ADC is more accurate.

→ Flash type of ADC requires no counter.

→ Counter type of ADC and Successive approximation type of ADC used DAC.

Notes:

ACE EDUCATIONAL ACADEMY

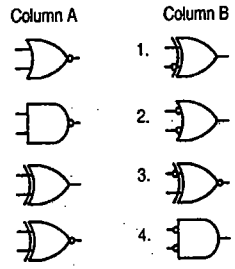
DIGITAL ELECTRONICS

GATE Examination Questions

Electronics & Communication Engineering

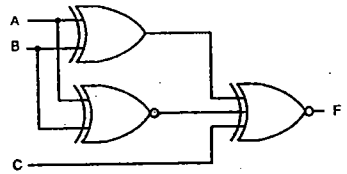
GATE-2010

1. Match the logic gates in **Column A** with their equivalents in **Column B**



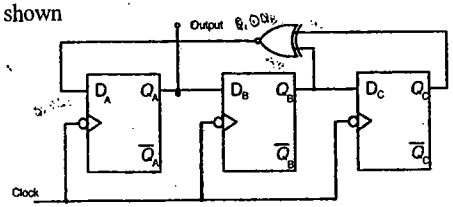
(a) P-2, Q-4, R-1, S-3 (b) P-4, Q-2, R-1, S-3
(c) P-2, Q-4, R-3, S-1 (d) P-4, Q-2, R-3, S-1

2. For the output F to be 1 in the logic circuit shown, the input combination should be



(a) A = 1, B = 1, C = 0 (b) A = 1, B = 0, C = 0
(c) A = 0, B = 1, C = 0 (d) A = 0, B = 0, C = 1

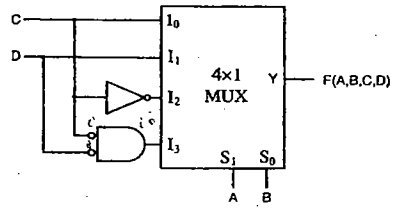
3. Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown



(a) 0010111 (b) 0001011
(c) 0101111 (d) 0110100

Notes:

4. The Boolean function realized by the logic circuit shown is



(a) F = ∑m(0,1,3,5,9,10,14) (b) F = ∑m(2,3,5,7,8,12,13)
(c) F = ∑m(1,2,4,5,11,14,15) (d) F = ∑m(2,3,5,7,8,9,12)

GATE-2009

5. The full forms of the abbreviations TTL and CMOS in reference to logic families are

(a) Triple Transistor Logic and Chop Metal Oxide Semiconductor
(b) Tristate Transistor Logic and Chip Metal Oxide Semiconductor
(c) Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
(d) Tristate Transistor Logic and Complementary Metal Oxide Silicon

6. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is
(a) non – maskable and non – vectored
(b) maskable and non – vectored
(c) non – maskable and vectored
(d) maskable and vectored

7. If $\overline{X} = 1$ in the logic equation
$[\overline{X} + Z\{\overline{Y} + (\overline{Z} + X\overline{Y})\}]\{X + Z(X + Y)\} = 1$, then

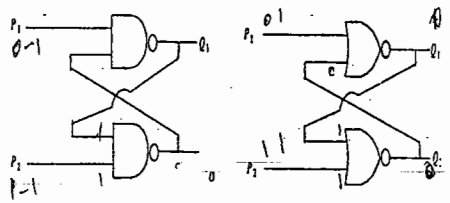
(a) Y = Z (b) $Y = \overline{Z}$ (c) Z = 1 (d) Z = 0

8. What are the minimum number of 2 to 1 multiplexers required to generate a 2- input AND gate and a 2- input XOR gate?

(a) 1 and 2 (b) 1 and 3
(c) 1 and 1 (d) 2 and 2

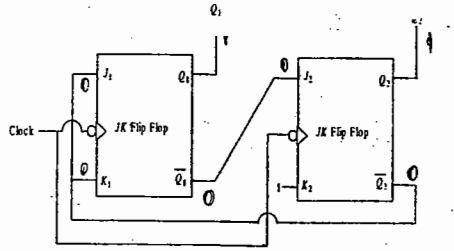
Notes:

9. Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1 , 1). The corresponding stable outputs (Q_1, Q_2) are



(a) NAND : first (0, 1) then (0,1)
NOR : first (1, 0) then (0,0)
(b) NAND : first (1, 0) then (1, 0)
NOR : first (1, 0) then (1,0)
(c) NAND : first (1, 0) then (1, 0)
NOR : first (1, 0) then (0,0)
(d) NAND : first (1, 0) then (1, 1)
NOR : first (0, 1) then (0,1)

10. What are the counting states (Q_1, Q_2) for the counter shown in the figure below?

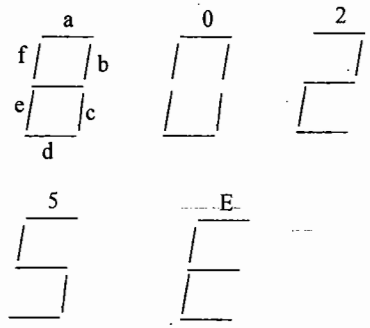


(a) 11, 10, 00, 11, 10,...
(b) 01, 10, 11, 00, 01,...
(c) 00, 11, 01, 10, 00,...
(d) 01, 10, 00, 01, 10,...

Statement for Linked Answer Questions 11 and 12.
Two products are sold from a vending machine, which has two push buttons P_1 and P_2. When a bottom pressed, the price of the corresponding product is displayed in a 7 – segment display
If no buttons are pressed,'0' is displayed, signifying'Rs.0'.
If only P_1 is pressed, '2' is displayed, signifying 'Rs.2'
If only P_2 is pressed, '5' is displayed, signifying 'Rs.5'.
If both P_1 and P_2 are pressed, 'E' is displayed, signifying 'Error'

Notes:

The names of the segments in the 7 – segment display, and the glow of the display for '0' , '2', '5' and 'E' are shown below.



Consider
(i) push button pressed/not pressed is equivalent to logic 1/0 respectively
(ii) a segment glowing / not glowing in the display is equivalent to logic 1 / 0 respectively.

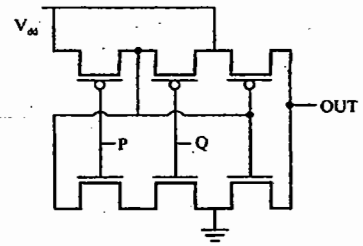
11. If segments a to g are considered as functions of P_1 and P_2, then which of the following is correct?
(a) $g = \overline{P_1} + P_2$, d = c + e
(b) $g = \overline{P_1} + P_2$, d = c + e
(c) $g = \overline{P_1} + P_2$, e = b + c
(d) $g = P_1 + P_2$, e = b + c

12. What are the minimum numbers of NOT gates and 2 – input OR gates required to design the logic of driver for this 7 – segment display?

(a) 3 NOT and 4 OR (b) 2 NOT and 4 OR
(c) 1 NOT and 3 OR (d) 2 NOT and 3 OR

GATE-2008

13. The logic function implemented by the following circuit at the terminal OUT is

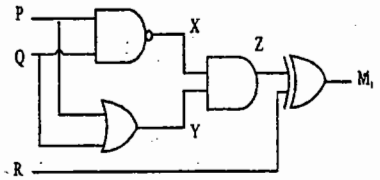


(a) P NOR Q (b) P NAND Q
(c) P OR Q (d) P AND Q

Notes:

14. The two numbers represented in signed 2's complement form are P = 11101101 and Q = 11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is
(a)100000111 (b) 00000111 (c) 11111001 (d) 111111001

15. Which of the following Boolean Expressions correctly represents the relation between P, Q, R and M_1?



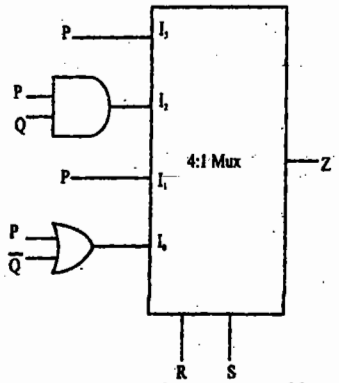
(a) M_1 = (PR OR Q) XOR R

(b) M_1 = (PR AND Q) XOR R

(c) M_1 = (PR NOR Q) XOR R

(d) M_1 = (PR XOR Q) XOR R

16. For the circuit shown in the following figure I_0 –I_3 are inputs to the 4:1 multiplexer. R (MSB) and S are control bits.



The output Z can be represented by

(a) $PQ + P\overline{Q}S + \overline{Q}\,\overline{R}\,\overline{S}$

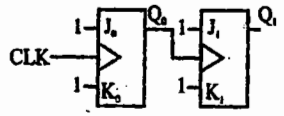
(b) $P\overline{Q} + PQ\overline{R} + \overline{P}\,\overline{Q}\,\overline{S}$

(c) $P\overline{Q}\,\overline{R} + \overline{P}QR + PQRS + \overline{Q}\,\overline{R}\,\overline{S}$

(d) $PQ\overline{R} + PQR\overline{S} + P\overline{Q}\,\overline{R}S + \overline{Q}\,\overline{R}\,\overline{S}$

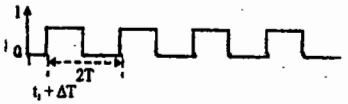
Notes:

17. For each of the positive edge-triggered J-K flip flop used in the following figure, the propagation delay in ΔT

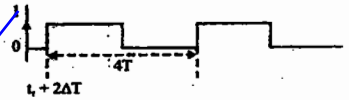


Which of the following waveforms correctly represents the output at Q_1

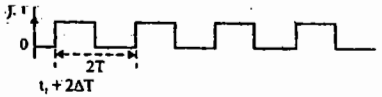
(a)



(b)

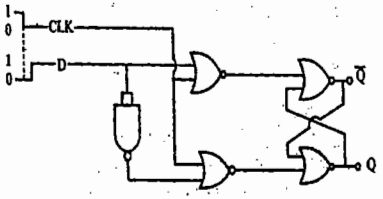


(c)



(d)

18. For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible.



Which of the following statements is true?

(a) Q goes to 1 a the CLK transition and stays at 1.

(b) Q goes to 0 at the CLK transition and stays at 0

(c) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1

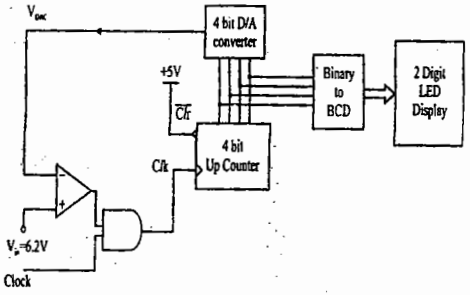
(d) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

Notes:

Statement for linked answer questions

In the following circuit, the comparator output is logic "1" if V1>V2 and is logic "0" otherwise, the D/A conversion is done as per the relation.

$V_{DAC} \sum_{n=0}^{3} 2^{n-1} b_n$ Volts, where b_3 (MSB), b_2, b_1 b_0 (LSB) _ are the counter outputs. The counter starts from the clear state.



19. The stable reading of the Led displays is
(a) 06 (b) 07 (c) 12 (d) 13

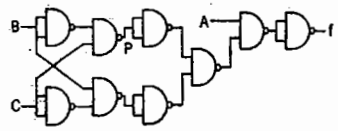
20. The magnitude of the error between V_{DAC} and V_{in} at steady state in volts is

(a) 0.2 (b) 0.3
(c) 0.5 (d) 1.0

GATE-2007

21. X=01110 and Y = 11001 are two 5- bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is
(a) 100111 (b) 001000
(c) 000111 (d) 101001

22. The point P in the following figure is struck-at-1. The output f will be



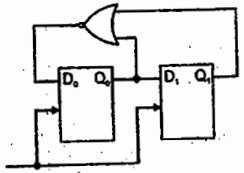
(a) $\overline{AB\overline{C}}$ (b) $\overline{A}$ (c) $AB\overline{C}$ (d) A

Notes:

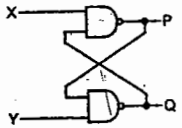
23. The Boolean function Y=AB+CD is to b realized using only 2-input NAND gates. The minimum number of gates required is
(a) 2 (b) 3 (c) 4 (d) 5

24. The Boolean expression $Y=\overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D}$ can be minimized to
(a) $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,\overline{C} + A\,\overline{C}\,D$
(b) $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D$
(c) $Y = \overline{A}\,B\,C\,\overline{D} + \overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D$
(d) $Y = \overline{A}\,B\,C\,\overline{D} + \overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D}$

25. For the circuit shown, the counter state (O_1 O_0) follows the sequence
(a) 00, 01,10,11,00
(b) 00, 01,10,00,01
(c) 00, 01,11,00,01
(d) 11, 10,11,00,10

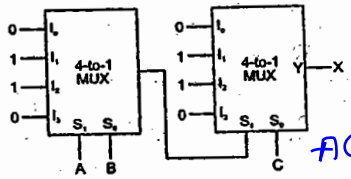


26. The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequences indicated below:
X = 0, Y = 1; X = 0,Y = 0; X = 1,Y = 1
The corresponding stable P,Q outputs will be



(a) P=1, Q=0; P=1, Q=0; P=1,Q=0 or P=0, Q=1
(b) P=1, Q=0; P=0, Q=1; P=0,Q=1; P=0, Q=1
(c) P=1, Q=0; P=1, Q=1; P=1,Q=0 or P=0, Q=1
(d) P=1, Q=0; P=1, Q=1; P=1,Q=1

27. In the following circuit, X is given by

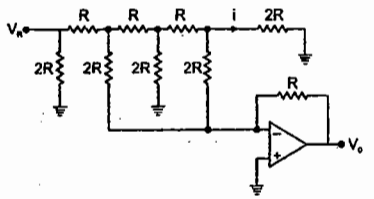


(a) $X = A\,B\,C + \overline{A}\,B\,\overline{C} + \overline{A}\,\overline{B}\,C + ABC$
(b) $Y = \overline{A}\,BC + A\overline{B}C + A\,B\overline{C} + A\,\overline{B}\,\overline{C}$
(c) $X = A\,B + B\,C + A\,C$
(d) $X = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}$

Notes:

Statement for linked answer questions:

In the Digital-to-Analog converter circuit shown in the figure below, $V_R = 10$ V and $R = 10$ kΩ



28. The current is

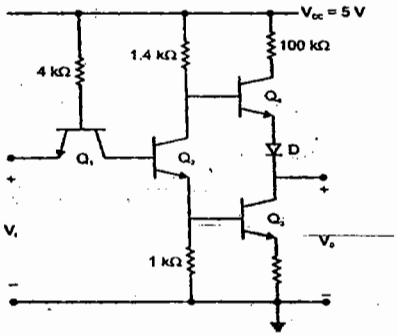
(a) 31.25 μA (b) 62.5 μA (c) 125 μA (d) 250 μA

29. The Voltage V_0 is

(a) -0.781 V (b) -1.562 V

(c) -3.125 V (d) -6.250 V

30. The Circuit diagram of a standard TTL NOT gate is shown in the figure, When $V_I = 2.5$ V, the modes of operation of the transistors will be



(a) Q_1: reverse active; Q_2: normal active; Q_3 saturation; Q_4 : cut-off

(b) Q_1: reverse active; Q_2: saturation; Q_3 saturation; Q_4: cut-off

(b) Q_1 : normal active; Q_2 :cut-off; ; Q_3: cut-off; Q_4 : saturation

(c) Q_1 :saturation ; Q_2 : saturation; ; Q_3 saturation; Q_4 : normal active

Notes:

GATE-2006

31. The number of product terms in the minimized SOP expression obtained through the following K-map is (where,"d" denotes don't care states)

(a) 2 (b) 3

(c) 4 (d) 5

1	0	0	1
0	D	0	0
0	0	d	1
1	0	0	1

32. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this numbering system, the BCP code 100010011001 corresponds to the following number is base-5 system

(a) 423 (b) 1324 (c) 2201 (d) 4231

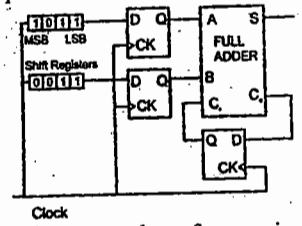
33. For the circuit shown in the figure below, two 4-buit parallel in-serial-out shift registers loaded with the data shown are used to feed the data to a full adder, initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs of the full adder should be

(a) S=0 $C_0 = 0$

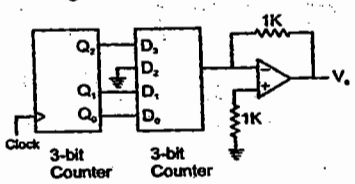
(b) S=0 $C_0 = 1$

(c) S=1 $C_0 = 0$

(d) S=1 $C_0 = 1$

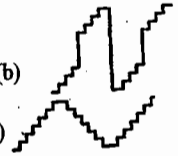


34. A 4 bit D/A convertor is connected to a free-running 3-bit UP counter, as shown in the following figure, which of the following waveforms will be observed at V_0?



In the figure shown above, the ground has been shown by the symbol

(a) 

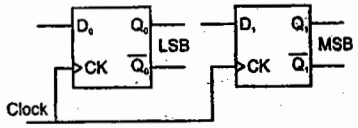
(b) 

(c) 

(d)

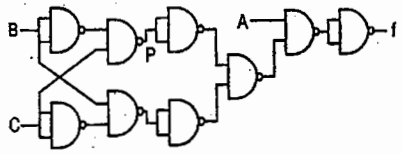
Notes:

35. Two D-flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following $Q_1\ Q_0$ sequence $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$
The inputs D_0 and D_1 respectively should be connected as



(a) $\overline{Q}_1$ and Q_0 (b) $\overline{Q}_0$ and Q_1
(c) $\overline{Q}_1 Q_0$ and $Q_1 \overline{Q}_0$ (d) $\overline{Q}_1\ \overline{Q}_0$ and $Q_1 Q_0$

36. The point P in the following figure is struck-at-1. The output f will be

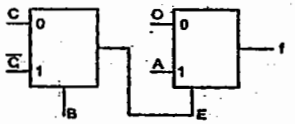


(a) $\overline{A\overline{B}\overline{C}}$ (b) $\overline{A}$ (c) $AB\overline{C}$ (d) A

GATE-2005

37. Decimal 43 is Hexadecimal and BCD number system is respectively
(a) B2, 01000011
(b) 2B, 01000011
(c) 2B, 00110100
(d) B2, 01000100

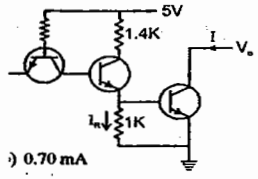
38. The Boolean function f implemented in the figure using two input multiplexers is



(a) $A\overline{B}C + AB\overline{C}$ (b) $ABC + A\overline{B}\overline{C}$
(c) $\overline{A}BC + \overline{A}\overline{B}\overline{C}$ (d) $\overline{A}BC + \overline{A}B\overline{C}$

Notes:

39. The transistors used in apportion of the TTL gate shown in the figure have a β=100. The base-emitter voltage of is 0.7 V for a transistor in active region and 0.75V for a transistor in saturation. If the sink current I=1 mA and the output is at logic 0, then the current I_R will b equal to



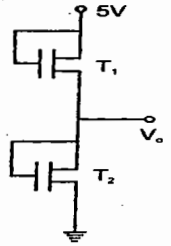
(a) 0.65 mA (b) 0.70 mA
(c) 0.75 mA (d) 1.00 mA

40. The Boolean expression for the truth table shown is

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(a) $\overline{B}\ (A + \overline{C})\ (\overline{A} + \overline{C})$ (b) B (A + C) (A + C)
(c) $\overline{B}$ (A + C) $(\overline{A} + \overline{C})$ (d) B (A + C) (A + C)

41. Both transistors T_1 and T_2 show in the figure, have a threshold voltage of 1 Volts. The device parameters K_1 and K_2 of T_1 and T_2 are, respectively, 36 $\mu A/V^2$. the output voltage V_0 is

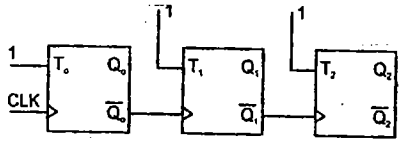


(a) 1V (b) 2V (c) 3V (d) 4 V

Notes:

42. The present output Q_n of an edge triggered JK flip-flop is logic o. If J=1, then Q_{n+1}
(a) cannot be determined (b) will be logic 0
(c) will b logic 1 (d) will race around

43. The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2\ Q_1\ Q_0 = 011$, then its next state ($Q_2\ Q_1\ Q_0$) will be

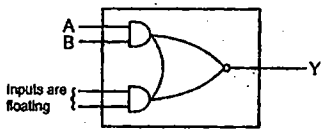


(a) 010 (b) 100 (c) 111 (d) 101

GATE-2004

44. The range of singed decimal numbers that can be represented by 6-bit 1's complement number is
(a) -31 to +31 (b) -63 to +63
(c) -64 to +63 (d) -32 to +31

45. The figure shown the internal schematic of a TTL AND-OR-Invert (AOI) gate. For the inputs shown in the figure, the output Y is



(a) 0 (b) 1 (c) AB (d) $\overline{AB}$

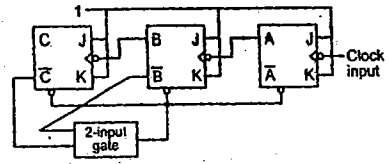
46. The minimum number of 2-to-1 multiplexers required to realize 4-to-1 multiplexer is
(a) 1 (b) 2 (c) 3 (d) 4

47. The Boolean expression $AC+B\overline{C}$ is equivalent to
(a) $\overline{A}C + B\overline{C} + AC$
(b) $\overline{B}C + A\overline{C} + B\overline{C} + \overline{A}C\overline{B}$
(c) $AC + B\overline{C} + \overline{B}C + A\overline{B}C$
(d) $ABC + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}C$

48. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?
(a) 25, 9 and 57 respectively (b) -6, -6 and -6 respectively
(c) -7, -7 and -7 respectively (d) -25, -9 and -57

Notes:

49. In the module -6 ripple counter shown in the figure, the output of the 2-input gate is used to clear the J-K flip-f;p[s/

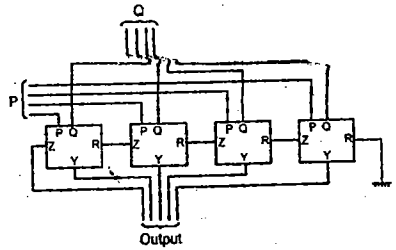


The 2-input gate is
(a) a NAND gate (b) a NOR gate
(c) an OR gate (d) an AND gate

50. A Boolean function f of two variable *x* and *y* is defined as follows: f(0,0) = f(0,1) = f(111) =1; f(1,0) = 0
Assuming complements of x and y are not available, a minimum cost solution for realizing f using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of)
(a) 1 unit (b) 4 unit (c) 3 unit (d) 2 unit

GATE-2003

51. The circuits shown in the figure has 4 boxes each described by inputs P, Q, R and outputs Y, Z with
$Y = P \oplus Q \oplus R;\ Z = RQ + \overline{P}R + Q\overline{P}$



(a) 4 bit adder giving P + Q
(b) 4 bit subtractor giving P – Q
(c) 4 bit subtractor giving Q – P
(d) 4 bit adder giving P + Q + R

52. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then
(a) R = 10ns, S=40ns (b) R=40ns, S=10ns
(c) R=10 ns, S=30 ns (d) R=30 ns, S=10 ns

Notes:

53. If the functions W, X, Y and Z are as follows:

$W = R + \overline{PQ} + \overline{RS}$

$X = PQ\overline{RS} + \overline{PQ}RS + \overline{PQ}\overline{RS}$

$Y = RS + \overline{PR + P\overline{Q} + \overline{P}.\overline{Q}}$

$Z = R+S+\overline{PQ+\overline{P}.\overline{Q}.R+P\overline{Q}.\overline{S}}$

Then

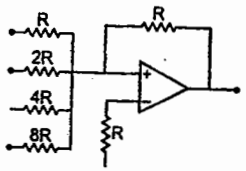
(a) W = Z, $X=\overline{Z}$ (b) W = Z, X=Y
(c) W = Y (d) W = $Y=\overline{Z}$

54. The DTL, TTL, ECL and CMOS and families of digital ICs are compared in the following 4 columns

	(P)	(Q)	(R)	(S)
Fanout is minimum	DTL	DTL	TTL	CMOS
Power consumption	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

The correct column is
(a) P (b) Q (c) R (d) S

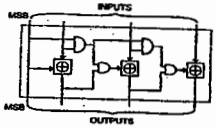
55. The circuit shown in the figure is a 4 bit DAC



The input bits 0 and 1 are represented by 0 and 5 V respectively. The OP AMP is ideal, but all the resistances and the 5 V inputs have a tolerance of ±10%. The specification (rounded to the nearest multiple of 5%) for the tolerance of the DAC is

(a) ±35% (b) ±20% (c) ±10% (d) ±5%

56. . The circuit shown in the figure Converts

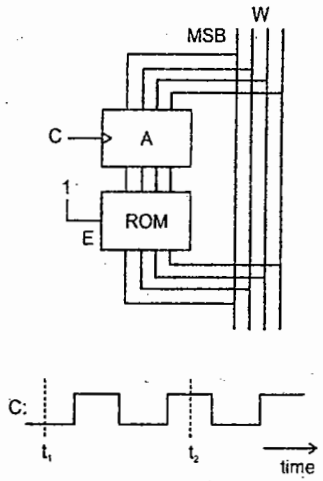


(a) BCD to binary code (b) Binary to excess – 3 code
(c) Excess -3 to Gray code (d) Gray to Binary code

Notes:

57. In the circuit shown in the figure, A parallel-in, parallel-out 4 bit register, which load at the rising edge of the clock C. The input lines are connected to a 4 bit bus, W. Its output acts as the input to a 16X4 Rom whose output is floating when the enable input E is 0.A partial table of the contents of the ROM is as follows:

Address	0	2	4	6	8	10	11	14
Data	0011	1111	0100	1010	1011	1000	0010	1000



The clock to the register is shown, and the data on the W bus at time t_1 is 0110. The data on the bus at time T_2 is
(a) 1111 (b) 1011 (c) 1000 (d) 0010

GATE-2002

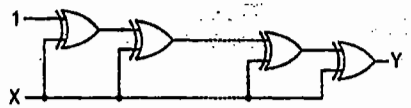
58. 4-bit 2's complement representation of a decimal number is 1000, the number is
(a) +8 (b) 0 (c) -7 (d) -8

59. Te number of comparators required in a 3-bit comparator type ADC is

(a) 2 (b) 3 (c)7 (d) 8

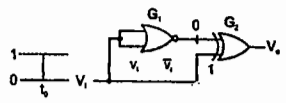
Notes:

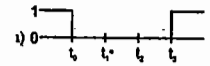
60. If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is X, then the output Y is equal to

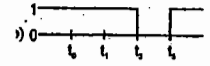


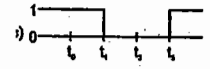
(a) 0 (b) 1 (c) $\overline{X}$ (d) X

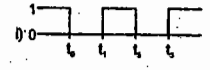
61. . The gates G_1 and G_2 in the figure have propagation delay of 10 nsec and 20 nec respectively. If the input V_1 makes an abrupt change from logic 0 to 1 at time $t=t_0$ then the output wave from V_0 is



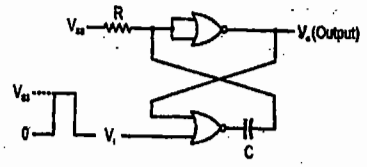
(a) 

(b) 

(c) 

(d) 

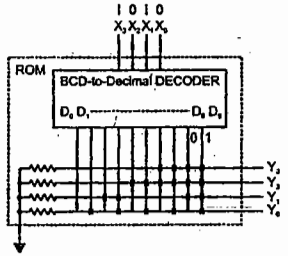
62. The circuit in the figure has two CMOS NOR-gates, This circuit functions as a:



(a) Flip-Flop (b) Schmitt trigger
(c) Monostable multivibrator
(d) Astable multivibrator

Notes:

63. If the input X_3, X_2, X_1, X_0 to the ROM in the figure are 8 4 2 1 BCD numbers, then the outputs Y_3, Y_2, Y_1, Y_0 are

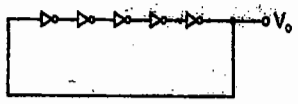


(a) gray code numbers (b) 2 4 2 1 BCD numbers
(c) excess-3 code numbers (d) none of the above

GATE-2001

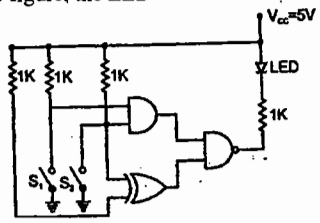
64. The 2's complement representation of -17 is
(a) 101110 (b) 101111 (c) 111110 (d) 110001

65. For the ring oscillator shown in the figure ,the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output?



(a) 10MHz (b) 100MHz (c) 1 GHz (d) 2 GHz

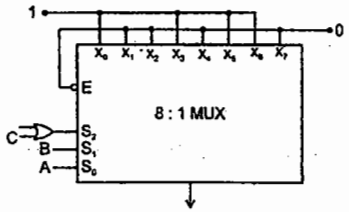
66. In the figure, the LED



(a) emits light when both S_1 and S_2 are closed.
(b) emits light when both S_1 and S_2 are open.
(c) emits light when only of S_1 and S_2 is closed.
(d) does not emit light, irrespective of the switch positions

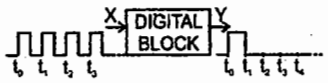
Notes:

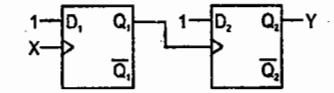
67. In the TTL circuit in the figure, S_2 to S_0 are select lines and X_7 to X_0 are input lines, S0 and X0 are LSBs. The output Y is

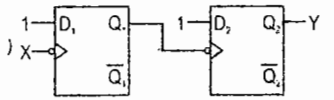


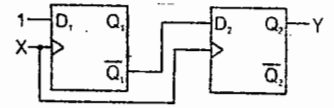
(a) indeterminate (b) AB'+A'B
(c) A+B (d) C(A+B) C(A+B)

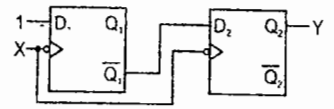
68. The digital block in the figure is realized using two positive edge triggered D-flip-flops. Assume that for T<T0, Q1=Q2=0. The circuit in the digital block is given by:



(a)


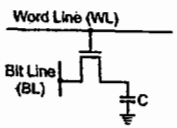
(b)


(c)


(d)


69. In the DRAM cell in the figure, the V1 of the NMOSFET is 1V. For the following three combinations of WL and BL voltages

(a) 5V; 3V; 7V
(b) 4V; 3V; 4V
(c) 5V; 5V; 5V
(d) 4V; 4V; 4V

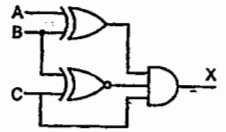


Notes:

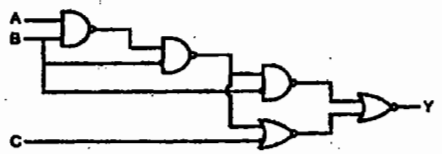
GATE-2000

70. For the logic circuit shown in the figure, the required input condition (A, B, C) to make the output (x) =1 is

(a) 1, 0, 1
(b) 0, 0, 1
(c) 1, 1, 1
(d) 0, 1, 1

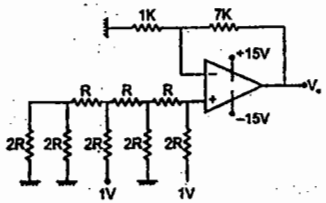


71. For the logic circuit shown in the figure, the simplified Boolean expression for the output Y is



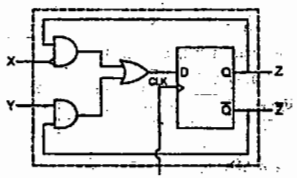
(a)A+B+C (b) A (c) B (d) C

72. For the 4 bit DAC shown in the figure, the output voltage V_0 is



(a).10 V (b) 5V (c) 4 V (d) 8V

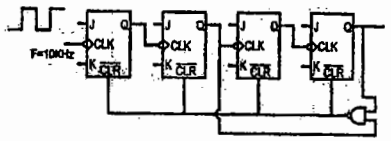
73. A sequential circuit using D Flip-Flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is



(a) S-R Flip – Flop with inputs X=R and Y=S
(b) S-R Flip-Flop with inputs X =S and Y=R
(c) J-K Flip-Flop with inputs X=J and Y=K
(d) J-K Flip-Flop with inputs X = K and Y=J

Notes:

74. In the figure, the J and K inputs of all the four Flip-Flops are made high The frequency of the signal at output Y is



(a) 0.833 KHz (b) 1.0 KHz
(c) 0.91KHz (d) 0.77KHz

Note:

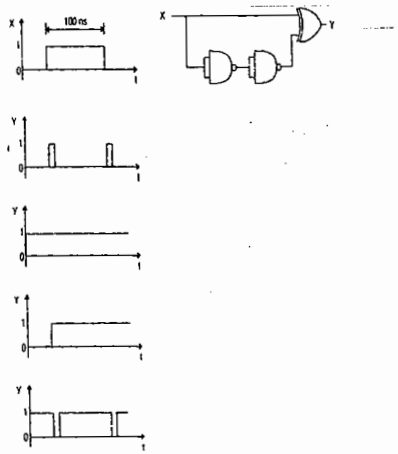
KEY

1.d	2.d	3.d	4.d	5.c	6.c	7.d	8.a
9.c	10.a	11.b	12.d	13.b	14.b	15.d	16.a
17.b	18.c	19.	20.	21.c	22.d	23.b	24.d
25. b	26.c	27.a	28.	29.	30.b	31.a	32.c
33.d	34.b	35.a	36.d	37.b	38.a	39.c	40.a
41.c	42.c	43.b	44.b	45.a	46.c	47.d	48.c
49.c	50.d	51.b	52.b	53.a	54.b	55.a	56.a
57.b	58.d	59.c	60.b	61.b	62.c	63.b	64.b
65.c	66.d	67.b	68.a	69.b	70.d	71.b	72.b
73.d	74.b						

Electrical Engineering

GATE-2010

1. The TTL circuit shown in the figure is fed with the waveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit



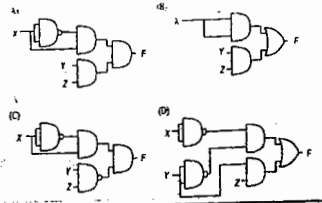
Linked Answer Questions

Statements for linked Answer questions 2 and 3
The following Karnaugh map represents a function F.

F	yz 00	01	11	10
x 0	1	1	1	0
1	0	0	1	0

2. A minimized form of the function F is
(A) $F = XY + YZ$ (b) $F = \overline{X}\overline{Y} + YZ$
(C) $F = X\overline{Y} + \overline{Y}Z$ (d) $F = \overline{X}\overline{Y} + \overline{Y}Z$

3. Which of the following circuits is a realization of the above function F?



Notes:

Notes :

GATE – 2009

4. The increasing order of speed of data access for the following devices is

i. Cache Memory

ii. CD-ROM

iii. Dynamic RAM

iv. Processor Registers

v. Magnetic Tape

(A) (v), (ii), (iii), (iv), (i)

(B) (v), (ii), (iii), (i), (iv)

(C) (ii), (i), (iii), (iv), (v)

(D) (v), (ii), (i), (iii), (iv)

5. The complete set of only those Logic Gates designated as Universal Gates is

(A) NOT, OR and AND Gates

(B) XNOR, NOR and NAND Gates

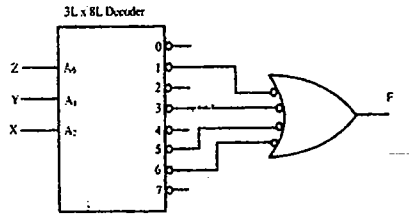
(C) NOR and NAND Gates

(D) XOR, NOR and NAND Gates

Notes :

GATE – 2008

06. A 3 line to 8 line decoder, with active low outputs, is used to implement a 3-variable Boolean function as shown in the figure.



The simplified form of Boolean function F(X, Y, Z) implemented in 'Product of Sum' form will be

(A) $(X+Z).(\overline{X}+\overline{Y}+\overline{Z}).(Y+Z)$

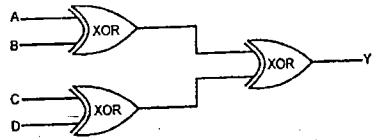
(B) $(\overline{X}+\overline{Z}).(X+Y+Z).(\overline{Y}+\overline{Z})$

(C) $(\overline{X}+\overline{Y}+Z).(\overline{X}+Y+Z).(X+\overline{Y}+Z).(X+Y+\overline{Z})$

(D) $(\overline{X}+\overline{Y}+\overline{Z}).(\overline{X}+Y+\overline{Z}).(X+Y+Z).(X+\overline{Y}+\overline{Z})$

GATE – 2007

07. A, B, C and D are input bits, and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct?



(A) S is always either zero or odd

(B) S is always either zero or even

(C) S = 1 only if the sum of A, B, C and D is even

(D) S = 1 only if the sum of A, B C and D is odd

GATE – 2006

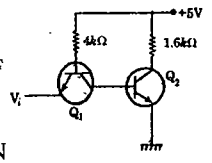
08. A TTL NOT gate circuit is shown in figure. Assuming V_{BE} = 0.7 V of both the transistors, if V_i = 3.0 V, then the states of the two transistors, will be

(A) Q_1 ON and Q_2 OFF

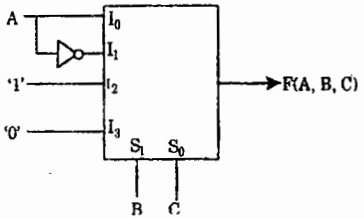
(B) Q_1 reverse ON and Q_2 OFF

(C) Q_1 reverse ON and Q_2 ON

(D) Q_1 OFF and Q_2 reverse ON



09. A 4 x 1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function F(A, B, C) implemented is



(A) $F(A, B, C) = \Sigma(1, 2, 4, 6)$

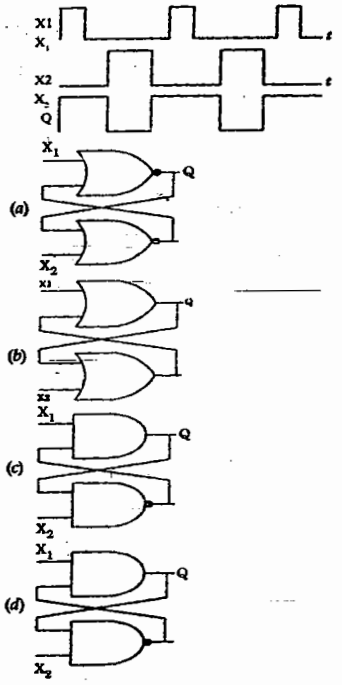
(B) $F(A, B, C) = \Sigma(1, 2, 6)$

(C) $F(A, B, C) = \Sigma(2, 4, 5, 6)$

(D) $F(A, B, C) = \Sigma(1, 5, 6)$

GATE – 2005

10. Select the circuit which will produce the given output Q for the input signals X_1 and X_2 given in the figure.

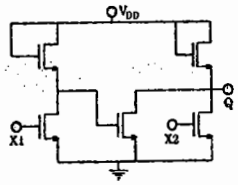


Notes :

11. A digital-to-analog converter with a full-scale output voltage of 3.5 V has a resolution close to 14 m V. Its bit size is

(A) 4 (B) 8 (C) 16 (D) 32

12. If X_1 and X_2 are the inputs to the circuit shown in the figure, the output Q is



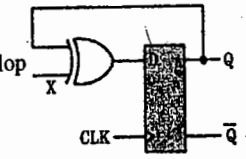
(A) $\overline{X_1 + X_2}$

(B) $\overline{X_1 \bullet X_2}$

(C) $\overline{X_1} \bullet X_2$

(D) $X_1 \bullet \overline{X_2}$

13. The digital circuit shown in the figure works as a



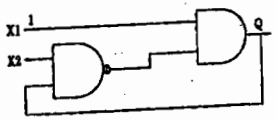
(A) JK flip-flop

(B) Clocked RS flip-flop

(C) T flip-flop

(D) Ring counter

14. In the figure, as long as $X_1 = 1$ and $X_2 = 1$, the output Q remains



(A) at 1

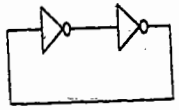
(B) at 0

(C) at its initial value

(D) unstable

GATE – 2004

15. The digital circuit using two inverters shown in fig. will act as



(A) a bistable multi-vibrator

(B) an astable multi-vibrator

(C) a monostable multi-vibrator

(D) an oscillator

16. The simplified form of the Boolean expression $Y = (\overline{A}.BC + D)(\overline{A}.D + \overline{B}.\overline{C})$ can be written as

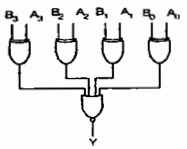
(A) $\overline{A}.D + \overline{B}.\overline{C}.D$ (B) $AD + B.\overline{C}.D$

(C) $(\overline{A} + D)(\overline{B}.C + \overline{D})$ (D) $A.\overline{D} + BC.\overline{D}$

Notes :

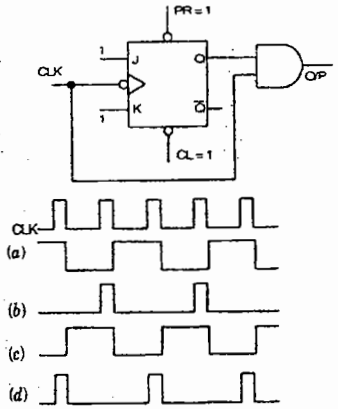
17. A digital circuit which compares two numbers $A_3\ A_2\ A_1\ A_0$, $B_3\ B_2\ B_1\ B_0$ is shown in fig. To get output Y= 0, choose one pair of correct input numbers.

(A) 1010, 1010
(B) 0101, 0101
(C) 0010, 0010
(D) 0010, 1011



Notes :

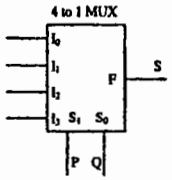
18. The digital circuit shown in fig. generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.



GATE – 2003

19. Fig. shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in}. Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S?

(A) $I_0 = I_1 = C_{in}; I_2 = I_3 = \overline{C}_{in}$
(B) $I_0 = I_1 = \overline{C}_{in}; I_2 = I_3 = C_{in}$
(C) $I_0 = I_3 = C_{in}; I_1 = I_2 = \overline{C}_{in}$
(D) $I_0 = I_3 = \overline{C}_{in}; I_1 = I_2 = C_{in}$

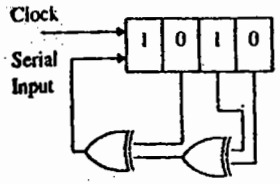


20. The Boolean expression
$\overline{X}Y\overline{Z} + \overline{X}\overline{Y}Z + XY\overline{Z} + X\overline{Y}Z + XYZ$
can be simplified to

(A) $X\overline{Z} + \overline{X}Z + YZ$ (B) $XZ + \overline{Y}Z + Y\overline{Z}$
(C) $\overline{X}Y + YZ + XZ$ (D) $\overline{X}\overline{Y} + Y\overline{Z} + \overline{X}Z$

21. The shift register shown in fig. is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how may clock pulses will the content of the shift register become 1010 again?

(A) 3
(B) 7
(C) 11
(D) 15



Notes :

22. An X-Y flip flop, whose Characteristic Table is given below is to be implemented using a J-K flip flop

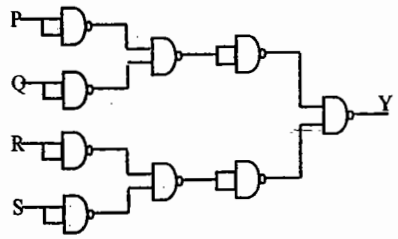
X	Y	Q_{n+1}
0	0	1
0	1	Q'_n
1	0	Q_n
1	1	0

This can be done by making

(A) $J = X, K = \overline{Y}$ (B) $J = \overline{X}, K = Y$
(C) $J = Y, K = \overline{X}$ (D) $J = \overline{Y}, K = X$

GATE – 2002

23. For the circuit shown in Fig. P2.10, the Boolean expression for the output Y in terms of inputs P, Q, R and S is



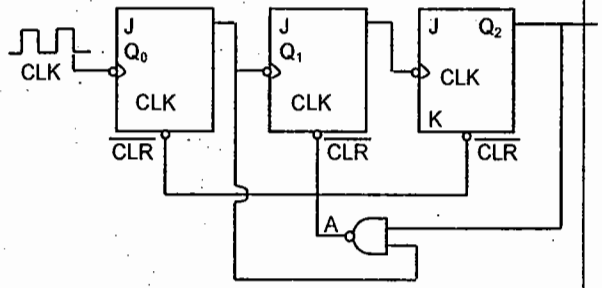
(A) $\overline{P} + \overline{Q} + \overline{R} + \overline{S}$ (B) P + Q + R + S
(C) $(\overline{P} + \overline{Q})(\overline{R} + \overline{S})$ (D) (P + Q)(R + S)

24. The ripple counter shown in fig. is made up of negative edge triggered J-K flip-flops. The signal levels at J and K inputs of all the flip-flops are maintained at logic1. Assume that all outputs are cleared just prior to applying the clock signal.

(A) create a table of Q_0, Q_1, Q_2 and A in the format given below for 10 successive input cycles of the clock CLK1.
(B) Determine the module number of the counter.
(C) Modify the circuit of fig. to create a modulo-6 counter using the same components used in the figure.

Format for (a):

CLK1	Q_2	Q_1	Q_0	A

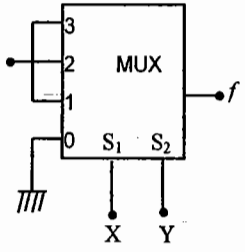


Notes :

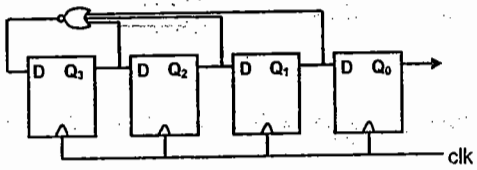
GATE – 2001

25. The output f of the 4-to-1 MUX shown in fig. is

(A) $\overline{xy} + x$
(B) $x + y$
(C) $\overline{x} + \overline{y}$
(D) $xy + \overline{x}$



26. For the ring counter shown in fig. find the steady state sequence if the initial state of the counter is 1110(i.e., Q_3 Q_2 Q_1 Q_0 = 1110). Determine the MOD number of the counter.



Notes :

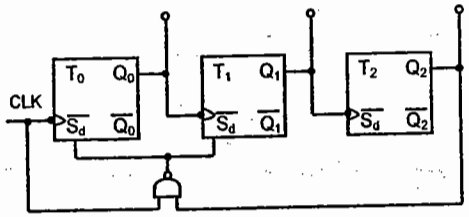
GATE – 2000

27. The minimal product-of-sums function described by the K-map given in Fig.P2.4.

(A) A'C'
(B) A' + C'
(C) A + C
(D) AC

C \ AB	00	01	11	00
0	1	1	ϕ	0
1	0	0	ϕ	0

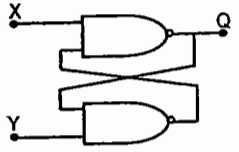
28. The counter shown in fig. is initially in state $Q_2 = 0$, $Q_1 = 1$, $Q_0 = 0$. With reference to the CLK input, draw waveforms for Q_2, Q_1, Q_0 and P for the next three CLK cycles.



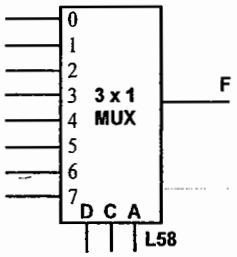
GATE – 1999

29. For a flip-flop formed from two NAND gates as shown in Figure. The unusable state corresponds to

(A) X = 0, Y = 0
(B) X = 0, Y = 1
(C) X = 1, Y = 0
(D) X = 1, Y = ∞



30. The logic function F = AC + ABD + ACD is to be realized using an 8 to 1 multiplexer shown in the figure, using A, C and D as control inputs.



(a) Indicate the inputs to be applied at the terminals 0 to 7.
(b) Can the function be realize using a 4 to 1 multiplexer?

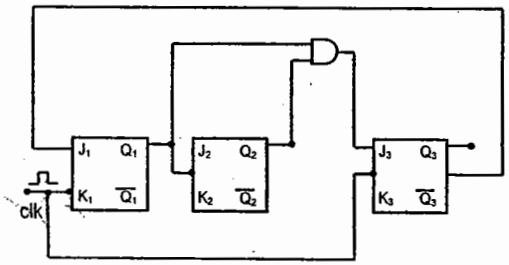
GATE – 1998

31. The open collector outputs of two 2-inputs NAND gates are connected to a common pull up resistor. If the input to the gates are P, Q and R, S respectively, the output is equal to

(A) $\overline{P.Q}.\overline{R.S}$. (B) $\overline{PQ}+\overline{RS}$
(C) P.Q+R.S (D) P.Q.R.S

32. In standard TTL gates, the totem pole output stage is primarily used to
(A) increase the noise margin of the gate
(B) decrease the output switching delay
(C) facilitate a wired OR logic connection
(D) increase the output impedance of the circuit

33. (a) Construct the truth table for the circuit given in Figure Q_1, Q_2 and Q_3 are outputs and the clock pulses are the inputs. Unused J,K inputs are assumed to be at logic. All flip flops are reset at power ON.
(b) Sketch the output waveforms at Q_1, Q_2 and Q_3.
(c) What function does this circuit perform.



Notes :

GATE – 1997

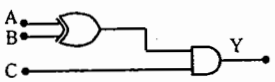
34. A 3-input 2-output priority encoder has the following truth table where X's indicate don't care conditions. Realize the logic using NAND gates and inverters.

W_2	W_1	W_0	Y_1	Y_0
0	0	0	0	0
0	0	1	0	0
0	1	X	1	0
1	X	X	1	1

GATE – 1996

35. The Boolean expression for the output of the logic circuit shown in Figure. is

(A) $Y=\overline{A}\,\overline{B}+AB+\overline{C}$
(B) $Y=\overline{A}\,\overline{B}+AB+\overline{C}$
(C) $Y=\overline{A}\,B+\overline{A}B+C$
(D) $Y=\overline{A}B+\overline{A}\,\overline{B}+\overline{C}$



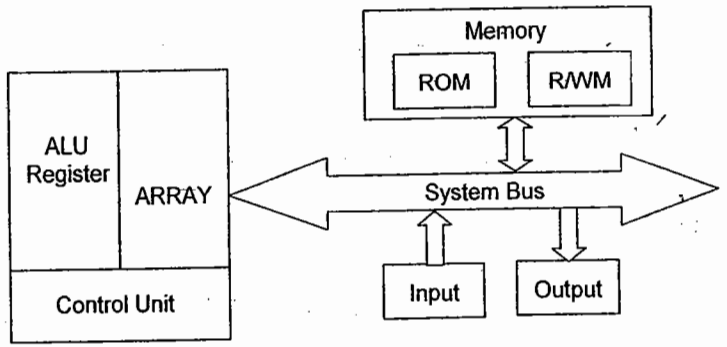
KEY

1.a	2.b	3.d	4.a	5.c	6.d	7.d	8.c
9.a	10.d	11.b	12.c	13.c	14.d	15.c	16.a
17.d	18.b	19.c	20.b	21.b	22.b	23.b	24.---
25.b	26.---	27.a	28.---	29.d	30.---	31.b	32.b
33.---	34.---	35.b					

BASICS:

- **Digital Computer:** A programmable machine that processes binary data. It is traditionally represented by five blocks: Arithmetic Logic Unit (ALU), Control Unit, Memory, Input Unit and Output Unit.
- **Central Processing Unit (CPU) :** The group of circuits that processes data and provides control signals and timing. It includes ALU, Control Unit and a group of registers.
- **ALU:** The group of circuits that performs arithmetic and logic operations. The ALU is a part of CPU.
- **Control Unit:** The group of circuits that provides timing and signals to all operations in the computer and controls the data flow.
- **Memory:** A medium that stores binary information.
- **Input:** It is a device that transfers information from the outside world to the computer.
- **Output:** It is a device that transfers information from the computer to the outside world.
- **Microprocessor**: A Microprocessor is a semiconductor device which is manufactured by using LSI or VLSI technology, which includes ALU, Control Unit and a group of Registers in a single Integrated circuit.
- **Micro controller:** It is a device that includes microprocessor, memory, and simple I/O Interface logic on a single chip, fabricated using VLSI technology.
- **Bit:** Binary Digit.
- **Nibble:** A group of four bits is called a nibble.
- **Byte:** A group of eight bits is called a byte.
- **Word:** A group of bits the computer recognizes and processes at a time.
- **Instruction:** A command in binary that is recognized and executed by the computer to accomplish a task.
- **Mnemonic Instruction:** A meaningful combination of letters used to suggest the operation of an instruction.
- **Bus:** A group of wires or lines used to transfer bits between the microprocessor and other components of the computer system. Or a path used to carry signals, such as connection between memory and the CPU in a digital computer.

- **Microcomputer:** A digital computer having a microprocessor as its Central Processing Unit is called Microcomputer. A microprocessor combined with memory, an input device and an output device forms a microcomputer



- **Bit capacity of a microprocessor:** It is defined as the number of bits it can process at a time in parallel. For example 8-bit microprocessor can perform all 8-bit operations.
- In general the internal architecture of the microprocessor depends on the bit capacity of the microprocessor.
- The system bus of the microcomputer consists of three types of buses: Address Bus, Data Bus and Control Bus.
- **Address Bus:** A group of lines that are used to send a memory address or a device address from the Microprocessor Unit (MPU) to the memory or the peripheral. The address bus is always unidirectional. Address always goes out of the microprocessor.
- The addressing capacity of any microprocessor is given by 2^n, where 'n' is nothing but the number of address lines available in the microprocessor.
- **Data Bus:** A group of lines used to transfer data between the MPU and peripherals (or memory). The data bus is always bi-directional.
- In general the width of the data bus is equal to the bit capacity of the microprocessor.
- In general the internal architecture of the microprocessor depends on the data bus width.
- **Control Bus:** The single lines that are generated by the MPU to provide timing of various operations.
- Intel Corporation introduced the first microprocessor in 1971. Its bit capacity was 4.

Some of the example microprocessors are given below:

Name	Word Length Memory	Addressing Capacity	Number Of Pins	Number Of Transistors
4004	4 – bit	640 bytes	16	2300
8008	8 - bit	16 KB	18	3500
8080	8 - bit	64 KB	40	6000
8085	8 – bit	64 KB	40	
8086	16 – bit	1 MB	40	29,000
8088	8/16 bit	1 MB	40	
80186	16 – bit	1 MB	68	
80286	16 – bit	16 MB real, 4 GB virtual	68	1,34,000
80386	32 – bit	4 GB real, 64 TB virtual	132 PGA	2,75,000
80486	32 – bit	4 GB real, 64 TB virtual	168 PGA	1,200,000
Pentium	64 – bit	4 GB real	273 PGA	3.1 Million
Pentium Pro	64 – bit	64 GB real		5.5 Million
Pentium - II	64 – bit	64 GB real		7.5 Million
6800	8 – bit	64 KB	40	
6809	8 – bit	64 KB	40	
68000	16 – bit	16 MB	64	
68020	32 – bit	4 GB	169 PGA	2,00,000
68030	32 – bit	4 GB	169 PGA	
68040	32 – bit	4 GB		
Z – 80	8 – bit	64 KB	40	
Z – 800	8 – bit	500 KB		
Z – 8000	16 – bit	64 KB	48	

- All IBM Personal computers use 8088 microprocessor as CPU.
- Virtual memory concept was first introduced in 80286 microprocessor.
- 8088 microprocessor has external 8-bit data path and all internal operations are of 16-bit.
- The microprocessors primarily perform four operations: Memory Read, Memory Write, I/O Read and I/O Write. For each operation it generates the appropriate control signal.

8085 Microprocessor

- It is a 40 pin IC, requires +5V single power supply.
- Address Bus width of 8085 is 16 – bit. Its addressing capacity is $2^{16} = 65,536 = 64K$ (1K = 1024)
- Low order address Bus $A_0 – A_7$ is multiplexed with data bus $D_0 – D_7$
- Maximum clock frequency of 8085 microprocessor is 3.07 MHz.
- 8085 microprocessor is having on chip clock generation facility
- Crystal frequency of 8085 processor is 6.144 MHz. It is always double to that of clock frequency.
- Clock frequency of 8085 is always half of the crystal frequency.
- Theoretical value of clock frequency is 3 MHz and Crystal frequency is 6 MHz.
- 8085 microprocessor is having 74 basic Instructions with 246 opcodes.
- It supports five hardware Interrupts and eight software Interrupts.
- Hardware Interrupts: TRAP RST 7.5, RST 6.5, RST 5.5 and INTR.

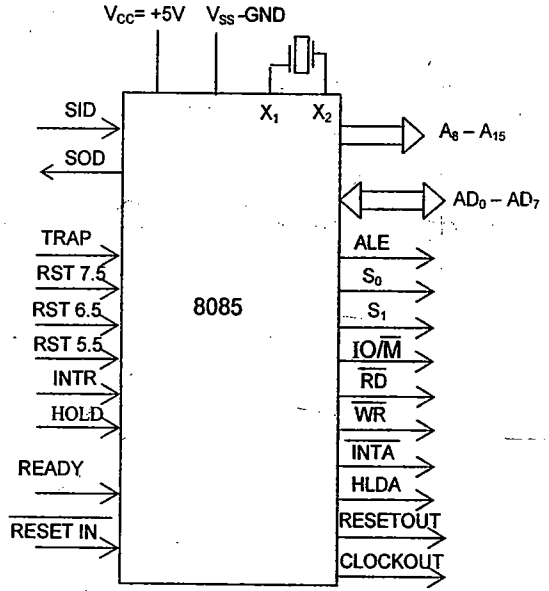
TRAP
RST 7.5
RST 6.5
RST 5.5
INTR ↓

- TRAP is also called RST 4.5. TRAP is high priority interrupt and INTR is least priority Interrupt.
- Software Interrupts: RST n (RST : Restart) Where n = 0 to 7
- Lengths of 8085 instructions vary from one to three bytes.
- 8085 supports five status flags: Sign (S), Zero (Z), Auxiliary Carry (Ac), Parity (P) and Carry (CY).

- 8085 Microprocessor consists of two 16 – bit address register: Program Counter (PC) and Stack Pointer register (SP).
- PC always holds address of next memory location to be accessed.
- SP always holds address of the top of the stack.
- 8085 consists of six 8 – bit general purpose registers which are accessible to the programmer: B, C, D, E, H and L.
- Based on requirement six 8 – bit general purpose registers can be used as three register pairs: BC, DE and HL.
- 8085 also contains an 8 – bit processor register called Accumulator 'A'.
- Range of addresses generated by 8085 Microprocessor : 0000H to FFFFH
- The number of Machine cycles required to execute an 8085 instruction varies from one to five.

Signal description of 8085:

- All the available (40) signals of 8085 can be classified into six groups: (1). Power supply & Frequency signals (2) Serial IO ports (3) Address Bus (4) Data Bus (5) Interrupts and externally initiated (6) Status, Control & Acknowledge signals



- Pair of signals used for Serial I/O communication: SID & SOD
- Pair of Instructions used for Serial I/O Communication: SIM & RIM

- ALE (Address Latch Enable) signal is used to latch low order 8 – bit address present on $AD_0 – AD_7$ into external latches
- S_1, S_0 and $IO/\overline{M}$ signals are called status signals
- $\overline{RD}$ and $\overline{WR}$ signals are control signals
- HOLD and HLDA signals are used for DMA (Direct Memory Access) operation.
- READY signal is used by the microprocessor to communicate with slow operating peripherals
- $\overline{RESET\ IN}$ is chip reset which is active low signal
- RESETOUT signal is used to connect to RESET IN of other interfacing circuits used in microprocessor based system
- CLOCKOUT of 8085 will be connected to CLOCK IN of other interfacing circuits used in micro based systems to synchronize the operation with 8085
- 8085 uses S_0 and S_1 signals to indicate the current status of the processor.

S_1	S_0	Status
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

- Getting / reading an instruction code from Memory into the processor is called opcode fetch.
- By Combining the status signal $IO/\overline{M}$ with control signals $\overline{RD}$ and $\overline{WR}$ we can generate four different signals

$IO/\overline{M}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	1	$\overline{MEMR}$
0	1	0	$\overline{MEMW}$
1	0	1	$\overline{IOR}$
1	1	0	$\overline{IOW}$

- DMA is having highest priority over all the interrupts
- Hardware interrupts are of two types: 1. Vectored Interrupts and 2. Non – Vectored Interrupts
- RST 7.5, RST 6.5, RST 5.5, RST 4.5 (TRAP) are called hardware vectored interrupts

- The vectored address corresponds to each of the HW vectored interrupts are given below

TRAP (RST 4.5) ---------- 0024 H
RST 5.5 ---------- 002C H
RST 6.5 ---------- 0034 H
RST 7.5 ---------- 003C H

- INTR is a non vectored interrupt
- TRAP is a Non – Maskable Interrupt. It is always in enable condition
- RST 7.5, RST 6.5, RST 5.5, INTR are called maskable interrupts. These interrupts can be disabled by the execution of "DI" instruction can be re - enabled by the execution of "EI" instruction.
- RST 7.5, RST 6.5, RST 5.5, interrupts can be masked or unmasked by using SIM (Set Interrupt Mask) instruction
- TRAP is a non maskable vectored interrupt
- RST 7.5, RST 6.5, RST 5.5 are called Mask able Vectored interrupts
- INTR is a maskable non vectored interrupt
- RST 7.5 is edge triggered
- RST 6.5, RST 5.5, INTR are level triggered
- TRAP is both level and edge triggered
- Vectored addresses corresponds to the SW interrupts

RST 0 ----- 0000 H
RST 1 ----- 0008 H
RST 2 ----- 0010 H
RST 3 ----- 0018 H
RST 4 ----- 0020 H
RST 5 ----- 0028 H
RST 6 ----- 0030 H
RST 7 ----- 0038 H

Interrupts	Type	Instruction	Hardware	Trigger	Vector
TRAP	Nonmaskable	Independent of EI & DI	No external Hardware	Level & Edge sensitive	0024
RST 7.5	Maskable	Controlled by EI & DI Unmasked by SIM	No external Hardware	Edge sensitive	003C
RST 6.5	Maskable	Controlled by EI & DI Unmasked by SIM	No external Hardware	Level sensitive	0034
RST 5.5	Maskable	Controlled by EI & DI Unmasked by SIM	No external Hardware	Level sensitive	002C
INTR	Maskable	Controlled by EI & DI	RST Code from external Hardware	Level sensitive	0000 To 0038

- SIM instruction is used for serial output data operation as well as to mask or un mask different maskable vectored Interrupts
- RIM instruction is used for serial input data operation as well as to read the status of different Maskable Vectored interrupts
- The Accumulator register (A) is also called processor register
- 8085 is having 8 – bit flag register which is also called status register

Flags register

The ALU includes five flip-flops that are set or reset according to data conditions in the accumulator and other registers. The flags are affected by the arithmetic and logic operations in the ALU. The flags generally reflect data conditions in the accumulator. The structure of flags register is shown below. It consists of five flags namely Sign flag (s), Zero flag (z), Auxiliary Carry flag (Ac), Parity flag (p) and Carry flag (CY).

S	Z	X	Ac	X	P	X	Cy

Sign flag: In case of arithmetic operations with signed numbers, the most significant bit D7 is reserved to indicate sign information, and the remaining seven bits are used to represent the magnitude of the number. After the execution of an arithmetic or logic operation, the MSB of the result (usually in the accumulator) is copied into sign flag. S =1 indicates result is negative,
S = 0 indicates result is positive.

***Zero flag*:** Z =1 if the ALU operation results in zero. Z=0 if the result is not zero.

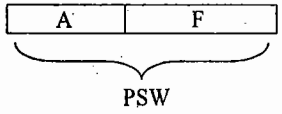
Auxiliary carry flag: In an arithmetic operation, the carry obtained from D_3 to D_4 bit position is called Auxiliary carry. This flag is used only internally for BCD operation and is not available for the programmer to change the sequence of a program with a jump instruction.

Parity flag: After ALU operation, the result has an even number of 1's then P=1 otherwise P=0.

Carry flag: If an arithmetic operation results in a carry, the carry flag is set i.e. CY=1 Otherwise it is reset. The carry flag also serves as a barrow flag for subtraction.

Note: Among the five flags, the Ac flag is used internally for BCD arithmetic; the instruction set does not include any conditional jump instructions based on this flag.

➢ Accumulator register content and status register content together is called PSW (Program Status Word or processor status word)



➢ Instruction set of 8085 Microprocessor can be classified based on their operation and length of instruction

Classification Based on operation:

❖ **Data transfer instructions:** These instructions are used to transfer data from register to register, register to memory or from memory to register. No flags will be affected for these instructions. r_1, r_2, r can be any one out of B, C, D, E, H, L, A and r_p can be any one out of three register pairs BC, DE & HL.

MOV r_1, r_2	$(r_1) \leftarrow (r_2)$
MOV r, M	$(r) \leftarrow (M)$ or $(r) \leftarrow ((HL))$
MOV M, r	$(M) \leftarrow (r)$ or $((HL)) \leftarrow (r)$
MVI (r/M), d_8	$(r/M) \leftarrow (8-bit\ data)\ d_8$
L XI r_p, 16 – bit	$r_p \leftarrow 16-bit$ r_p = BC, DE, HL or SP
LAD 16 – bit address	
STA 16 – bit address	
LHLD 16 – bit address	
SHLD 16 – bit address	
LDAX r_p / STAX r_p	r_p can be either BC or DE pair only
XCHG	(HL) ↔ (DE)
PCHL	(PC) ← (HL)

❖ **Arithmetic Instructions:** This group consists of addition, subtraction, increment and decrement operations. 8085 microprocessor does not support multiplication and division instructions

ADD r	$(A) \leftarrow (A) + (A)$	
ADD M	$(A) \leftarrow (A) + (M)$	
ADI d8	$(A) \leftarrow (A) + d8$	
ADC r	$(A) \leftarrow (A) + (r) + Cy$	
ADC M	$(A) \leftarrow (A) + (M) + Cy$	
ACI d8	$(A) \leftarrow (A) + d8 + Cy$	
SUB r	$(A) \leftarrow (A) - (r)$	
SUB M	$(A) \leftarrow (A) - (M)$	
SUI d8	$(A) \leftarrow (A) - d8$	
SBB r	$(A) \leftarrow (A) - (r) - Cy$	
SBB M	$(A) \leftarrow (A) - (M) - Cy$	
SBI d8	$(A) \leftarrow (A) - d8 - Cy$	
INR r	$(r) \leftarrow (r) + 1$	
INR M	$(M) \leftarrow (M) + 1$	
INX r_p	$(r_p) \leftarrow (r_p) + 1$	(r_p = BC, DE, HL or SP)
DCR r	$(r) \leftarrow (r) - 1$	
DCR M	$(M) \leftarrow (M) - 1$	
DCX r_p	$(r_p) \leftarrow (r_p) - 1$	(r_p = BC, DE, HL or SP)
DAD r_p	$(HL) \leftarrow (HL) + (r_p)$	r_p = BC, DE, HL or SP
DAA		

➢ In 8085, the service of AC flag is used by only one instruction. It is DAA.

➢ For INX and DCX instructions no flags affected

➢ Following table shows the list of flags affected for different instructions

Instruction	S	Z	Ac	P	Cy
INR, DCR	Yes	Yes	Yes	Yes	No
DAD	No	No	No	No	Yes
ADD, ADC, SUB, SBB, DAA	Yes	Yes	Yes	Yes	Yes

❖ **Logical Instructions:** This group consists of AND, OR, NOT, XOR, Compare and Rotate operations

ORA r	(A) ⟵ (A) V (r)
ORA M	(A) ⟵ (A) V (M)
ORI d8	(A) ⟵ (A) V d8
ANA r	(A) ⟵ (A) Λ(r)
ANA M	(A) ⟵ (A) Λ(M)
ANI d8	(A) ⟵ (A) Λd8
XRA r	(A) ⟵ (A) ∀ (r)
XRA M	(A) ⟵ (A) ∀ (M)
XRI d8	(A) ⟵ (A) ∀ d8
CMP r	(A) ⋛ (r)
CMP M	(A) ⋛ (M)
CPI d8	(A) ⋛ d8
CMA	(A) ⟵ (Ā)
CMC	Cy ⟵ Cy
STC	Cy ⟵ 1
RLC	Rotate accumulator left
RAL	Rotate Accumulator left through carry
RRC	Rotate accumulator right
RAR	Rotate Accumulator right through carry

M points to memory location address Bit in the pair

The result of the comparison is shown by setting the flags of the PSW as follows:
if (A) < (reg/mem): carry flag is set
if (A) = (reg/mem): zero flag is set
if (A) > (reg/mem): carry and zero flags are reset

➢ Following table shows how flags affected for different logical instructions

Instruction	S	Z	Ac	P	Cy
ANA	Yes	Yes	1	Yes	0
ORA, XRA	Yes	Yes	0	Yes	0
RLC, RRC, RAL, RAR, STC,CMC	No	No	No	No	Yes
CMP, CPI	Yes	Yes	Yes	Yes	Yes

❖ **Branch Instructions:** These are also called program control transfer instructions. These are two types: Un conditional branch and Conditional Branch instructions

➢ No flags will be affected for branch instructions

➢ **Unconditional Branch Instructions:**

JMP 16 – bit address
CALL 16 – bit address
RET
RST n (n = 0 to 7)
PCHL

➢ PCHL is one byte equivalent of three byte JMP Instruction
➢ RST n is one byte equivalent of three byte CALL instruction

➢ **Conditional branch instruction:**

Jump Instructions	Call Instructions	Return Instruction	Condition
J Z 16 – bit addr	CZ 16 – bit addr	RZ	If Z = 1
JNZ 16 – bit addr	CNZ 16 – bit addr	RNZ	If Z = 0
JC 16 – bit addr	CC 16 – bit addr	RC	If Cy = 1
JNC16 – bit addr	CNC 16 – bit addr	RNC	If Cy = 0
JP 16 – bit addr	CP 16 – bit addr	RP	If S = 0
JM 16 – bit addr	CM 16 – bit addr	RM	If S = 1
JPO 16 – bit addr	CPO 16 – bit addr	RPO	If P = 0
JPE 16 – bit addr	CPE 16 – bit addr	RPE	If P = 1

❖ **Machine Control, Stack and IO related Instructions:** No flags affected for these instructions.

➢ **Machine Control**: EI, DI, SIM, RIM, NOP, HLT

➢ **Stack related:** PUSH r_p (r_p = BC, DE, HL)
PUSH PSW
POP r_p
POP PSW
LXI SP, 16 – bit addr
SPHL

➢ **IO Related:** IN 8 – bit Port address
OUT 8 – bit Port address

Classification of Instructions as per their length

➢ According to the length of instruction, the 8085 instructions can be classified into three groups :

1. **One byte or One- word instructions**: This type of instruction requires one memory location to store in memory. The one byte instructions include both Op code and Operand in the same byte. Eg: MOV A, C , ADD B , CMA etc.

2. **Two byte or Two-word instructions:** This type of instruction requires two memory locations to store in memory. In a two byte instruction, the first byte specifies the operation code and the second byte specifies the operand.
Eg: MVI A,45 H , ADI 36 H , SUI 78 H, ORI 67 H, XRI 9A H etc.

3. **Three byte or Three-word instructions**: This type of instruction requires three memory locations to store in the memory. In three byte instruction, the first byte specifies the Op code, and the following two bytes specify the 16-bit address or data.
   Eg: JMP 2500 H, STA 4509 H, LDA 3456 H, LXI H,2345 H etc.

One byte instructions can be recognized as follows:

a) Data transfer instructions that copy the contents from one register (or memory) into another register (or memory) are one-byte instructions. Eg: MOV

b) Arithmetic/logic instructions without the ending letter 'I' are one byte.
   Eg: ADD, SUB, ORA

Two byte instructions can be recognized as follows:

a) Instructions that load or manipulate 8-bit data directly are 2-byte instructions.
   Eg: MVI, ADI, SUI, SBI, IN, OUT, ORI, XRI, ANI etc.

b) All three letter instructions with ending letter 'I' (except LXI) are two byte instructions.

- The instructions that load 16 bits or refer to memory addresses are 3-byte instructions.
  Eg: LXI, JMP, Conditional Jumps, CALL, Conditional Calls, STA, LDA, LHLD, SHLD .
- Whenever PUSH instruction is executed SP register content is decremented by 2.
- Whenever POP instruction is executed SP register content is incremented by 2
- When CALL instruction (conditional or unconditional) or RST instruction is executed, SP register content is decremented by 2, because current content of PC will be pushed automatically on to top two locations of the stack.
- When RET instruction (Conditional or Unconditional) is executed, SP register content is incremented by 2, because µp retrieves top two locations of the stack and loaded into PC

- **COMPARISION OF PUSH AND POP INSTRUCTIONS WITH CALL AND RET INSTRUCTIONS**

The instructions PUSH and POP are similar to the instructions CALL and RET. The Similarities and differences are as follows:

PUSH and POP	CALL and RET
The programmer uses the instructions PUSH to save the contents of register Specified register pair on the stack	When CALL is executed, the microprocessor automatically stores the 16-bit address of the instruction next to CALL on the stack.
When PUSH is executed, the stack pointer register is decremented by two	When CALL is executed, the stack pointer register is decremented by two
The instruction POP transfers the contents of the top two locations of the stack to the specified register pair.	The instruction RET transfers the contents of the top two locations of the stack to Program counter
When the instruction POP is executed the stack pointer is incremented by two	When the instruction RET is executed, the stack pointer is incremented by two
There are no conditional PUSH and POP instructions.	In addition to the unconditional CALL and RET instructions, there are eight conditional CALL and RETURN instructions

- **Addressing Modes:**

The way in which the operand information is specified in the instruction code is called addressing mode. The 8085 microprocessor supports five addressing modes.

1. **Implied or Implicit or Inherent addressing mode:** There are certain instructions which operate on the content of the accumulator. Such instructions do not require the address of the operand.
   Eg: CMA, STC, RLC, RRC, RAL, RAR etc.

2. **Direct addressing mode**: In this mode the address of the operand (data) is given in the instruction itself. Eg: STA, LDA, SHLD, LHLD, IN, OUT etc.

3. **Register addressing mode:** In this mode the operands are in the general purpose registers. The operation code specifies the address of the register in addition to the operation to be performed.
   Eg: MOV A,B; ADDB; SUB C; ORA B; etc.

4. **Register Indirect addressing mode:** In this mode the address of the operand is specified by a register pair. Eg: LXI , STAX, LDAX etc.

5. **Immediate addressing mode:** In this mode the operand is specified in the instruction itself. Eg: MVI, ADI, LXI, ORI, SUI, SBI, ACI, XRI, ANI etc.

- Each instruction cycle of the 8085 microprocessor can be divided into a few basic operations called machine cycles, and each machine cycle can be divided into T-states.
- **Machine cycle**: It is defined as the time required to complete the operation of accessing either memory or I/O. In the 8085, the machine cycle may consist of three to six T-states.
- T-state is defined as one sub-division of the operation performed in one clock-period.
- The time required to complete the execution of an instruction is called instruction cycle.
- The 8085 instruction cycle consists of one to five machine cycles or one to five operations.
- The first machine cycle of 8085 consists of four to six T-states and all other subsequent machine cycles consist of three T-states only.
- Read or write signal is generated at the beginning of T2 and will be completed before the end of T3 in every machine cycle.
- Types of machine cycles of 8085 : Op Code fetch cycle, Memory read cycle, Memory write cycle, I/O read cycle, I/O write cycle, Interrupt acknowledge machine cycle and Bus idle machine cycle.
- The first machine cycle of each instruction cycle is always OpCode fetch machine cycle.
- In 8085, CALL instruction is the lengthy instruction which takes 18-T states and the shortest instruction takes only 4-T states (Ex: MOV A,B).
- First machine cycle with four T – states is essential for each and every instruction. Other machine cycles depends on operation of the instruction.
- ALE signal is generated during T1 state of each machine cycle.
- Machine cycle format is given below:

M1						M2			M3			M4			M5		
T1	T2	T3	T4	T5	T6	T1	T2	T3	T1	T2	T3	T1	T2	T3	T1	T2	T3

- **Mapping:** Assigning addresses to I/O devices or memory locations is called mapping.
- **Memory mapping**: Assigning address to memory locations is called memory mapping.
- Memory mapping can be changed by changing the hardware logic used for the chip selection.
- To interface a memory chip with the 8085, the necessary low-order address lines of the 8085 address bus are connected to the address lines of the memory chip. The high-order address lines are decoded to generate CS (chip select) signal to enable the chip.

- **Absolute decoding:** In this decoding all the address lines which are not used for memory chip to identify a memory register must be decoded; thus, chip select can be asserted by only one address.
- **Linear decoding:** In this decoding technique, one address line is used for CS, and others are left don't care. This technique reduces hardware, but generates multiple addresses resulting in fold back memory space.

- **I/O devices can be connected to microprocessor in two different techniques.**

1. Memory mapped I/O technique and
2. I/O mapped or Peripheral mapped I/O technique.

Memory mapped I/O technique:

- In memory mapped I/O, the I/O devices are also treated as memory locations, under that assumption they will be given 16- bit address.
- In memory mapped I/O, microprocessor uses memory related instructions to communicate with I/O devices. Eg: STA, LDA, MOV A,M; MOV M,A etc.
- In memory mapped I/O, $\overline{MEMR}$ and $\overline{MEMW}$ control signals are used to activate I/O devices.
- In memory mapped I/O, the entire memory map is shared by memory locations and I/O devices. One address can be used only once. This technique is used in a system where the number of I/O devices are less.
- The maximum numbers of I/O devices that can be connected to microprocessor in this technique are 65536.

I/O mapped I/O technique:

- In this technique the I/O devices are identified by the microprocessor with separate 8-bit port address.
- This technique uses separate control signals ($\overline{IOR}$ and $\overline{IOW}$) to activate I/O devices and separate instructions (IN and OUT) to communicate with I/O devices.
- In this technique I/O mapping is independent of memory mapping. Same address can be used to identify input device and output device.

- This technique is used in a system where number of I/O devices are more. By using this method a maximum of 256 input devices and 256 output devices can be connected to the processor (total of 512 I/O devices).

Interfacing: Designing hardware circuit and writing software instructions to enable the microprocessor to communicate with peripheral devices is called interfacing. And the hardware circuit is called the interfacing device.

- There are two basic types of interfacing devices are available.
  1. Non-programmable interfacing devices and
  2. Programmable interfacing devices.

Non-programmable interfacing devices: Once the microprocessor based system is designed it is not possible to program this type of devices. Examples: 8212- Non-programmable I/O port, 74LS245- bi-directional buffers, 74LS373 – transparent latches etc.

Programmable interfacing devices: Writing a specific word, called the control word, according to the internal logic, can program a programmable interfacing device.

1. 8155 - Programmable Peripheral Interfacing (PPI) device with 256 bytes RAM and 16-bit timer/counter. It is a general purpose interfacing device i.e. it can be used to interface variety of I/O devices to the microprocessor.
2. 8255 - PPI it is also called programmable interface adapter (PIA). It consists of three 8-bit ports.
3. 8253 - Programmable Interval Timer. It can work in six different modes.

   Mode 0 – Interrupt on terminal count
   Mode 1 – Programmable one shot
   Mode 2 – Rate generator
   Mode 3 – Square wave generator
   Mode 4 – Software Triggered strobe
   Mode 5 – Hardware Triggered strobe.

4. 8251 – Programmable communication interfacing device. It is also called USART (Universal Synchronous Asynchronous receiver transmitter).
5. 8257 – Programmable DMA (Direct Memory Access) controller, DMA transfer is an I/O technique used commonly for high speed data transfer. The 8257 is a four channel DMA controller.

6. 8259 – Programmable Interrupt Controller (PIC). It is equivalent to providing eight INTR pins on 8085 microprocessor. By using nine 8259 IC's it is possible to connect a maximum of 64 I/O devices to the microprocessor with interrupt driven data transfer mode.
7. 8272 – Programmable Floppy disk controller.
8. 8275 – Programmable CRT controller.
9. 8279 – Programmable keyboard and display interfacing device. By using this it is possible to connect sixteen seven segment displays and sixty four keys (8 x 8 matrix) to the microprocessor.

Notes:

Prctice Test

1 An 8-bit microprocessor signifies that it has
(a) 8-bit address bus
(b) 8-bit controller
(c) 8-interrupt lines
(d) 8-bit data bus

2 Which of the following microprocessor is not an 8-bit microprocessor?
(a) 8085 (b) Z-80
(c) 68000 (d) 6502

3 Which of the following microprocessor has a 16-bit data bus?
(a) 8085 (b) Z-80
(c) 68000 (d) 6502

4 A microcomputer consists of
(a) a microprocessor (b) memory
(c) I/O devices
(d) all of the above

5 A microprocessor consists of
(a) ALU (b) Control unit
(c) array of registers
(d) all of the above

6 The address bus of any microprocessor is always
(a) Unidirectional
(b) Bi-directional
(c) Either unidirectional or bi-directional
(d) None

7 The data bus of any microprocessor is always
(a) Unidirectional
(b) bi-directional
(c) Either unidirectional or bi-directional
(d) None

8 The multiplexing of address bus and data buses is used in
(a) all the microprocessors
(b) depends on the internal architecture
(c) never multiplexed
(d) none of these

9 The multiplexing of address bus and data buses is used in microprocessors
(a) To reduce speed of operation
(b) To increase the number of pins
(c) To reduce the number of pins on IC
(d) To improve the operation

10 The multiplexing of address bus and data buses in microprocessors
(a) reduces the speed of the processor
(b) increases the speed of the processor
(c) multiplexing is independent of speed
(d) none of these

11 The address bus width of a microprocessor which is capable of addressing 64K bytes of memory is
(a) 8 (b) 12
(c) 16 (d) 20

12 The data bus width of a microprocessor which is capable of addressing 1M bytes of memory is
(a) 16 (b) 8
(c) 20 (d) can not be predicated

13 An 8-bit microprocessor can have ------- address lines.
(a) 8 (b)16 (c) 20
(d) can not be predicated

14 A number of 1-bit registers used in microprocessors to indicate certain conditions are usually referred to as
(a) Shift registers (b) flags
(c) latches (d) counters

15 A microprocessor has an 8-bit Op Code. The maximum possible number of OpCodes for this microprocessor will be
(a) 256 (b) 64
(c) 8 (d) 16

16 The Program Counter in a microprocessor always holds
a) the number of programs being executed on the microprocessor
b) the number of instructions being executed on the microprocessor
c) the number of interrupts handled by the microprocessor
d) the address of the next instruction to be fetched.

17 The word size of 8085 microprocessor is
(a) 4-bit (b) 8-bit
(c) 16-bit (d) 20-bit

18 How many 16-bit special purpose registers are present in the 8085 microprocessor?
(a) 8 (b) 6
(c) 2 (d) 16

19 The Stack Pointer register in a microprocessor
a) counts the number of programs being executing on the microprocessor
b) counts the number of instructions being executing on the microprocessor
c) keeps the address of the next instruction to be fetched
d) holds the address of the top of the stack

20 The number of status flags present in 8085 microprocessor are
(a) 8 (b) 16
(c) 5 (d) 10

21 The number of hardware interrupts present in 8085 microprocessor are
(a) 5 (b) 8
(c) 10 (d) 16

22 Which of the following statements is false?
(a) A microprocessor has bi-directional address bus
(b) A microprocessor has a unidirectional address bus
(c) A microprocessor has a bi-directional data bus
(d) A microprocessor has an ALU

23 Identify the non-maskable interrupt from the following
(a) RST 7.5 (b) RST 6.5
(c) RST 5.5 (d) RST 4.5

24 In microprocessor based systems DMA refers to
a) direct memory access for the microprocessor
b) direct memory access for the user
c) direct memory access for the I/O devices
d) none of the above

25 The interrupt facility is provided in microprocessor to
a) change the sequence of instructions being executed
b) stop the microprocessor when desired
c) stop the microprocessor when it starts malfunctioning
d) keep a control on the working of the microprocessor

26 A microprocessor differentiates between op code, data/address at any time by
(a) the sequence in which memory contents are fetched by it
(b) Its internal registers
(c) the stack pointer
(d) the program counter

27 A microprocessor without the interrupt facility
a) is best suited for a process control system
b) is not useful for a process control system
c) can not be used for DMA operation
d) can not be interfaced with any I/O device

28 In microprocessor based systems I/O ports are used to interface
(a) The I/O devices and memory chips
(b) the I/P device only
(c) The O/P devices only
(d) all the I/O devices

29 The stack pointer
(a) Resides in RAM
(b) resides in microprocessor
(c) Resides in ROM
(d) may be in RAM or ROM

30 In a microprocessor based system, the stack is always in
(a) Microprocessor (b) RAM
(c) ROM (d) EPROM

31 The instruction set of a microprocessor
(a) Is specified by the manufacturers
(b) is specified by the user
(c) Can not be changed by the user
(d) is stored inside the microprocessor

32 An 8085 microprocessor uses a crystal of frequency 6.25 MHz. The T state value is
(a) 340ns (b) 640ns
(c) 960ns (d) 1280ns

33 In an 8085 microprocessor based system, the contents of SP are 1000H. PUSH B instruction will transfer the contents of registers B and C respectively for memory locations
(a) 0FFFH and 0FFEH
(b) 0FFE H and 0FFF H
(c) 1000H and OFFFH
(d) 1000 H and 1001 H

34 In an 8085 microprocessor based system, the contents of SP are 2000H. POPH instruction will transfer the contents of memory location
(a) 2001H and 2002H to H and L registers respectively
(b) 2001H and 2000H to H and L registers respectively
(c) 2000H and 1FFFH to H and L registers respectively
(d) 2000H and 1999H to H and L registers respectively

35 PUSH B instruction in 8085 microprocessor causes
a) the contents of register B only to be copied in the stack
b) the contents of register B and C to be copied in the stack
c) the contents of registers B and C to be transferred in the stack and the registers get cleared
d) registers B and C to be cleared.

36 SUB A instruction in 8085
(A) resets carry and sign flags
(b) resets zero and parity flags
(c) sets zero and sign flags
(d) sets zero and carry flags

37 In 8085 microprocessor, let the accumulator contains the value 0AH and register C contains the value 05H. After CMPC instruction is executed, the
(a) zero and carry flags will be set
(b) zero and carry flags will be reset
(c) zero flag will be set and the carry flag will be reset
(d) zero flag will be reset and the carry flag will be set

38 When an 8085 microprocessor is reset, the address bus contains
(a) 0000H (b) 002CH
(c) 0043H (d) 003CH

39 Which of the data transfer is not possible in microprocessor
(a) memory to accumulator
(b) accumulator to memory
(c) memory to memory
(d) I/O device to accumulator

40 In 8085 microprocessor, in response to RST 7.5 interrupts the execution is transferred to memory location
(a) 0000H (b) 002CH
(c) 0034H (d) 003CH

41 In 8085 microprocessor, which of the following statements is false?
(a) there is a pin available for serial input
(b) there is a pin available for serial output
(c) serial I/O is possible through RIM and SIM instructions
(d) serial I/O is not possible

42 EPROM s are preferred for storing programs while developing new microprocessor based system because of their
(a) non-volatile characteristic
(b) erasable and programmable characteristic
(c) random access characteristic
(d) all the above characteristics

43 When any data transfer instruction, for transfer of data between memory and microprocessor, is executed the condition flags are
(a) not affected (b) always set
(c) always reset
(d) affected indicating specific conditions

44 Let the contents of the accumulator and register B be 00000100 and 01000000 respectively before execution of instruction SUB B. The contents of the accumulator after the execution of this instruction will be
(a) 00000100 (b) 01000000
(c) 11000100 (d) 010001000

45 Let the contents of register C be 00000000 before DCR C is executed. The contents of C after the execution of this instruction will be
(a) 00000000 (b) 11111111
(c) 00000001 (d) None

46 In an 8085 microprocessor based system the maximum possible number input/output devices can be connected using I/O mapped I/O technique is given by
(a) 64 (b) 512
(c) 256 (d) 65536

47 cycle-sealing mode of DMA operation involves
(a) DMA controller taking over the address, data, and control buses while a block of data is transfer between memory and I/O device .
(b) While the microprocessor is executing a program an interface circuit takes over control of address, data, control buses when not in use by microprocessor
(c) Data transfer takes place between the I/O device and memory during every alternate clock cycle
(d) The DMA control waiting for the microprocessor to finish execution of the program and then takes over the buses

48 Which of the following is not true during the execution of an interrupt service routine, which does not contain any EI instructions
(a) the microprocessor can be interrupted by a non-maskable interrupt
(b) the microprocessor can not be interrupted by any interrupt
(c) the microprocessor can not be interrupted by any masksble interrupt
(d) all interrupts except the non-maskable interrupt are disable

49 The reasons for the presence of ALE pin in 8085, but not in 6800 is that
(a) 8085 uses I/O mapped I/O, whereas 6800 uses memory mapped I/O
(b) 8085 has 5 interrupts lines, whereas 6800 has only two
(c) 8085 has multiplexed bus, whereas 6800 does not have
(d) None

50 Which of the following interrupt is both level and edge sensitive?
(a) RST 5.5 (b) INTR
(c) RST 7.5 (d) TRAP

51 The addressing mode used in the instruction PUSH B is
(a) direct (b) register
(c) register indirect
(d) immediate

52 On receiving an interrupt from an I/O device, the CPU
(a) halts for a predetermined time
(b) hands over control of address bus and data bus to the interrupting device
(c) branches off to the interrupt service routine immediately
(d) branches off to the interrupt service routine after completion of the current Instruction

53 The ALE line of an 8085 microprocessor is used to
(a) latch the output of an I/O instruction into an external latch
(b) deactivate the chip-select signal from memory devices
(c) latch the 8-bit of address lines AD7-AD0 into an external latch
(d) find the interrupt enable status of the TRAP interrupt

54 What is the execution time for the instruction, "STA ADDR", in an 8085 microprocessor if the clock frequency is 3 MHz ?
(a) 4329ns (b) 3975ns
(c) 3115ns (d) 3960ns

55 The first operation performed in INTEL 8085 after RESET is
(a) instruction fetch from location 0000H
(b) memory read from the location 0000H
(c) instruction fetch from location 8000H
(d) stack initialization

56 After the execution of CMP A instruction
(a) ZF is set and CY is reset
(b) ZF is set and CY is unchanged
(c) ZF is reset and CY is set
(d) ZF is reset and CY is unchanged

57 The 8085 microprocessor will enter into INA cycle after the recognition
(a) any interrupt
(b) TRAP only
(c) INTR only
(d) RST 7.5, 6.5, and 5.5 only

58 Which of the following lists the interrupts in decreasing priority?
(a) TRAP, RST 5.5, RST 6.5, RST 7.5, INTR
(b) INTR, TRAP, RST 7.5, RST 6.5, RST 5.5
(c) TRAP, RST 7.5, RST 6.5, RST 5.5, INTR
(d) RST 7.5, RST 6.5, RST 5.5, TRAP, INTR

59 The interrupt vector address for TRAP is
(a) 0000H (b) 0024H
(c) 0018H (d) 002CH

60 In order to reset carry without affecting accumulator content, one has to use
(a) SUB A (b) XRA A
(c) ORA A (d) CMC

61 Maximum number of I/O devices that can be addressed by INTEL 8085 is
(a) 65,536 (b) 255
(c) 512 (d) 256

62 The microprocessor may be made to exit from HALT state by asserting
(a) RESTART
(b) any of the five interrupts lines
(c) READY line
(d) a (or) b (or) HOLD line

63 The 8085 microprocessor enters into bus idle machine cycle whenever
(a) INTR interrupt is recognized
(b) RST X.5 is recognized
(c) DAD rp instruction is executed
(d) none of the above

64 In order to complement the lower order nibble of the accumulator, one can use
(a) ANI 0FH (b) XRI OF
(c) ORI 0FH (d) CMA

65 During OPCODE fetch the state of S0 and S1 is
(a) 00 (b) 01
(c) 10 (d) 11

66 After RESET 8255 will be in
(a) mode 0, all ports are input
(b) mode 0, all ports are output
(c) mode 2
(d) unchanged condition

67 The microprocessor issues ALE during first T-state of
(a) fetch cycle only
(b) memory READ cycle only
(c) memory WRITE cycle only
(d) every machine cycle

68 The data lines of 8085 processor are multiplexed with
(a) higher order address lines
(b) lower order address lines
(c) status lines
(d) none of the above

69 RST 3 instruction will cause the processor to branch to the location
(a) 0000H (b) 0018H
(c) 0024H (d) 8018H

70 Which of the following instruction will never affect the zero flag?
(a) DCR reg (b) ORA reg.
(c) DCX rp. (d) XRA reg.

71 The content of the A15-A8 (higher order address lines) while executing "IN addr." instruction are
(a) same as the contents of A7-A0
(b) irrelevant
(c) all bits reset (i.e. 00H)
(d) all bits set (i.e. FFH)

72 Which of the following peripheral ICs is used to interface keyboard and display?
(a) 8251 (b) 8279
(c) 8259 (d) 8253

73 The only interrupt which is edge-triggered is
(a) INTR (b) TRAP
(c) RST 7.5 (d) RST 5.5

74 Which one of the following instruction may be used to clear the accumulator content (i.e. A = 00H) irrespective of its initial value?
(a) CLR A (b) ORA A
(c) SUB A (d) MOV A,00H

75 The execution of RST n instruction causes the stack pointer to
(a) increment by two
(b) decrement by two
(c) remain unaffected
(d) none of the above

76 The stack is nothing but a set of
(a) reserved ROM address space
(b) reserved RAM address space
(c) reserved I/O address space
(d) none of the above

77 S0 and S1 pins are used for
(a) serial communication
(b) indicating the processor's status
(c) acknowledging the interrupt
(d) none of the above

78 Pick out the matching pair
(a) READY; RIM
(b) HOLD; DMA
(c) SID; SIM
(d) S0, S1; wait status

79 In order to save accumulator value onto the stack, which of the following instructions may be used
(a) PUSH PSW (b) PUSH A
(c) PUSH SP (d) POP PSW

80 A single instruction to clear the lower 4 bits of the accumulator in 8085 assembly language is
(a) XRI OFH (b) ANI FOH
(c) XRI FOH (d) ANI OFH

81 In a vectored interrupt
(a) the branch address is assigned to a fixed location in memory
(b) the interrupting source supplies the branch information to the processor through an interrupt vector
(c) the branch address is obtained from a register in the processor (d) none

82 A sequence of two instructions that multiplies the contents of the DE register pair by 2 and stores the result in the HL register pair(in 8085 assembly language) is
(a) XCHG and DAD B
(b) XTHL and DAD H
(c) PCHL and DAD D
(d) XCHG and DAD H

83 Identify key board and display interfacing device from the following
(a) 8255 (b) 8253
(c) 8279 (d) 8155

84 Identify the programmable interval timer from the following
(a) 8255 (b) 8253
(c) 8279 (d) 8275

85 Identify the communication interfacing device from the following
(a) 8155 (b) 8255
(c) 8251 (d) 8257

86 Identify the programmable DMA controller from the following
(a) 8257 (b) 8253
(c) 8251 (d) 8279

87 Pick up the programmable interrupt controller from the following
(a) 8279 (b) 8259
(c) 8257 (d) 8275

88 Identify the non-programmable interfacing device from the following
(a) 8295 (b) 8257
(c) 8212 (d) 8255

89 The maximum number of seven segment displays that can be connected to 8279 is
(a) 12 (b) 14 (c) 16 (d) 8

90 Using one 8259 IC is equivalent to providing _____ INTR pins on 8085
(a) 16 b) 12 (c) 8 (c) None

91 Total number of modes the 8253 can work
(a) 4 (b) 6 (c) 8 (d) 12

92 Maximum of how many devices can be connected simultaneously to the microprocessor via 8257 in DMA data transfer mode?
(a) 4 (b) 6 (c) 8 (d) 10

93 A microprocessor with a 12-bit address bus will be able to access
(a) 1K bytes (b) 4K bytes
(c) 8K bytes (d) 10K bytes

94 The frequency of the driving network connected between pins 1 and 2 of 8085 chip is
(a) twice the desired frequency
(b) equal to the desired frequency
(c) four times the desired frequency
(d) none of the above

95 A high on RESET OUT signifies that
(a) all the registers of the CPU are being reset.
(b) all the registers and counters are being reset.
(c) all the registers and counters are being reset and this signal can be used to reset external support chip
(d) processing can begin when this signal goes high.

96 READY signal in 8085 is useful when the CPU communicates with
(a) a slow peripheral device
(b) a fast peripheral device
(c) a DMA chip
(d) a PPI

97 Which of the following task is not performed by an assembler
(a) providing storage allocation
(b) creating a table of labels etc.
(c) doing assembly time arithmetic
(d) translate a program written in high level language to machine code program.

98 PSW stand for
(a) accumulator contents
(b) flag byte
(c) accumulator and flags register contents
(d) none of these

99 During the DMA transfer the processor (check the incorrect answer)
(a) continues its normal operation
(b) suspends its normal operations
(c) needs to initiate read (write) command
(d) needs to check if the input/output device is ready for data transfer

100 In 8085, interrupts except TRAP are disabled (check the incorrect statement) by
(a) a DI instruction
(b) a system reset
(c) Acknowledgement of a previous interrupt
(d) none of these

KEY

1.d	2.c	3.c	4.d	5.d	6.a
7.b	8.b	9.c	10.a	11.c	12.d
13.d	14.b	15.b	16.d	17.b	18.c
19.d	20.c	21.a	22.a	23.d	24.c
25.a	26.a	27.b	28.d	29.b	30.b
31.a	32.a	33.a	34.b	35.b	36.a
37.b	38.a	39.c	40.d	41.d	42.d
43.a	44.c	45.b	46.b	47.b	48.b
49.c	50.d	51.c	52.d	53.c	54.a
55.a	56.a	57.c	58.c	59.b	60.c
61.d	62.d	63.b	64.b	65.d	66.a
67.d	68.b	69.b	70.c	71.a	72.b
73.c	74.c	75.b	76.b	77.b	78.d
79.a	80.b	81.a	82.d	83.c	84.b
85.c	86.a	87.b	88.c	89.c	90.c
91.b	92.a	93.b	94.a	95.c	96.a
97.d	98.c	99.a	100.a		

MICROPROCESSORS
GATE Examination Questions

Electronics & Communication Engineering

GATE- 2009 (ECE)

Q1. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such interrupt is
(a) non-maskable and non-vectored
(b) maskable and non-vectored
(c) non-maskable and vectored
(d) maskable and vectored

GATE- 2008 (ECE)

Q2. An 8085 executes the following instructions

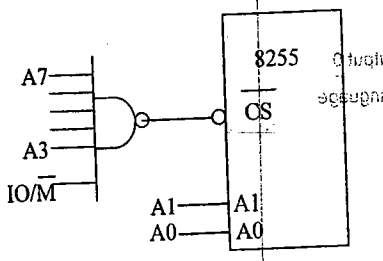
```
2710  LXI H,30A0
2713  DAD H
2714  PCHL
```

All addresses and contents are in Hex. Let PC be the contents of the program counter and HL be the contents of the HL register pair just after executing PCHL. Which of the following statements is in correct?

(a) PC = 2715 H, HL = 30A0 H
(b) PC = 30A0 H, HL = 2715 H
(c) PC = 6140 H, HL = 6140 H
(d) PC = 6140 H, HL = 2715 H

GATE- 2007 (ECE) – 2 marks each

Q3. An 8255 chip is interfaced to an 8085 microprocessor system as an I/O mapped I/O as shown in the figure. The address lines A0 and A1 of the 8085 are used by 8255 chip to decoded internally its three ports and Control register. The address lines A3 to A7 as well as the signal are used for address decoding. The range of addresses for which the 8255 chip would get selected is



(a) F8 H - FB H (b) F8 H - FC H
(c) F8 H – FF H (d) F0 H – F7 H

Notes:

Statements for linked questions Q4 and Q5.

An 8085 assembly language program is given below

```
Line1: MVI A, B5 H
   2: MVI B, 0E H
   3: XRI  69 H
   4: ADD B
   5: ANI 9B H
   6: CPI 9F H
   7: STA 3010 H
   8: HLT
```

Q4. The content of the accumulator just after execution of the ADD instruction in line 4 will be

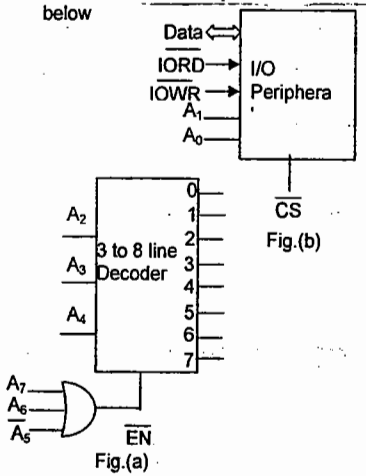
(a) C3 H (b) EA H (c) DC H (d) 69 H

Q5. After execution of line 7 of the program, the status of the CY and Z flags will be

(a) CY = 0, Z = 0 (b) CY = 0, Z = 1
(c) CY = 1, Z = 0 (d) CY = 1, Z = 1

GATE- 2006 (ECE) – 2 marks each

Q6. An I/O Peripheral device shown in figure (b) is interfaced to an 8085 microprocessor. To select I/O device in the I/O address range D4 H to D7 H, its chip-select (CS) should be connected to the output of the decoder shown in figure (a) below



(a) output 7 (b) output 5 (c) output 2 (d) output 0

Q7. Following is the segment of an 8085 assembly language program

```
        LXI SP, EFFF H
        CALL 3000 H
3000 LXI H, 3CF4 H
        PUSH PSW
        SPHL
        POP PSW
        RET
```

On completion of RET execution, the contents of SP is

(a) 3CF0 H (b) 3CF8 H (c) EFFD H (d) EFFF H

Notes:

(SP) ← EFFF H

(HL) ← 3CF4 H

[SP] ← 3CF4 H

POP PSW

(SP) ← (SP)+2
← 3CF6 H

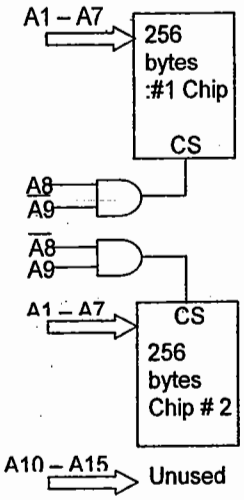
RET

(SP) ← (SP)+2

(SP) ← 3CF8 H

GATE- 2005 (ECE) – 2 marks each

Q8. What memory address range is NOT represented by Chip#1 and Chip#2 in the figure. A0–A15 in this figure are address lines and CS means chip select.



(a) 0100 – 02FF H (b) 1500 – 16FF H
(c) F900 – FAFF H (d) F800 - F9FF H

Statements for linked questions Q8 and Q9.

Consider an 8085 Microprocessor system

Q9. The following program starts at 0100 H

```
0100 LXI SP, 00FF H
0103 LXI H, 0107 H
0106 MVI A, 20 H
0109 SUB M
```

The contents of accumulator when the program counter reaches 0109 H is

(a) 20 H (b) 02 H
(c) 00 H (d) FF H

Q10. If in addition following code exists from 0109 H onwards,

```
ORI 40 H
ADD M
```

What will be the result in the accumulator after the last instruction is executed?

(a) 40 H (b) 20 H
(c) 60 H (d) 42 H

Notes:

0100 LXI SP
0101 FF
0102 00
0103 LXI H
0104 07H
0105 01H
0106 MVI A
0107 20H ← (HL)
0109 SUB M
010A

so A = 20 H

A ← (A) - [HL]
= 20H - 20H

0109 ORI
010A 40
010B ADD M
010C

[HL] ←
↓
20H

ADD M

40H
+ 20H
A 60H

GATE- 2004 (ECE) – 2 marks each Notes:

Q11. The 8255 Programmable Peripheral Interfaces is used as described below.

(I) An A/D converter is interfaced to a microprocessor through an 8255. the conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be strobed into PortA.

(II) Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals.

The appropriate modes of operation of the 8255 for (I) and (II) would be

(a) Mode 0 for (I) and Mode1 for (II)
(b) Mode 1 for (I) and Mode2 for (II)
(c) Mode 2 for (I) and Mode0 for (II)
(d) Mode 2 for (I) and Mode1 for (II)

Q12. The Number of memory cycles required to execute the following 8085 instructions

(I) LDA 3000H (II) LXI D, F0F1 H would be

(a) 2 for (I) and 2 for (II) (b) 4 for (I) and 3 for (II)
(c) 3 for (I) and 3 for (II) (d) 3 for (I) and 4 for (II)

Q13. Consider the sequence of 8085 instructions given below.

```
LXI H, 9258 H
MOV A,M
CMA
MOV M,A
```

Which one of the following is performed by this sequence?

(a) Contents of location 9258 are moved to the accumulator
(b) Contents of the location 9258 are compared with the contents of accumulator
(c) Contents of location 9258 are complemented and stored in location 9258
(d) Contents of location 5892 are complemented and stored in location 5892.

Q14. It is desired to multiply the numbers 0A H by 0B H and store the result in the accumulator. The numbers are available in registers B and C respectively. A part of the 8085 program for this purpose is given below:

```
      MVI A, 00 H
Loop : ————————
       ————————
       ————————
       HLT
```

The sequence of instructions to complete the program would be

(a) JNZ, Loop
ADD B
DCR C

(b) ADD B
JNZ Loop
DCR C

(c) DCR C
JNZ Loop
ADD B

(d) ADD B
DCR C
JNZ Loop

GATE- 2003 (ECE) – 2 marks each Notes:

Q15. In an 8085 microprocessor, the instruction CMP B has been executed while the content of the accumulator is less than that of register B. As a result

(a) Carry Flag will be set but Zero flag will be reset
(b) Carry Flag will be reset but Zero flag will be set
(c) Both Carry Flag and Zero flag will be reset
(d) Both Carry Flag and Zero flag will be set

GATE- 2002 (ECE) – 2 marks each

Q16. Consider the following assembly language program:

```
        MVI   B, 87 H
        MOV   A, B
START:  JMP   NEXT
        MVI   B, 00H
        XRA   B
        OUT   PORT1
        HLT
NEXT:   XRA   B
        JP    START
        OUT   PORT2
        HLT
```

The execution of the above program in an 8085 microprocessor will result in

a) An output of 87H at PORT1

b) An output 87H at PORT 2

c) Infinite looping of the program execution with accumulator data remaining at 00H

d) Infinite looping of the program execution with accumulator data alternating between 00 H and 87 H

Q17. An 8085 microprocessor operating at 5 MHz clock frequency executes the following routine. **— 5 marks**

```
START: MOV A, B
       OUT 55 H
       DCR B
       STA FFF8 H
       JMP START
```

(a) Determine the total number of machine cycles required to execute this routine till the JMP instruction is executed for the first time.

(b) Determine the time interval between two consecutive MEMW Signals

(c) If the external logic controls the READY line so that three WAIT states are introduced in the I/O WRITE machine cycle, determine the time interval between two consecutive MEMW signals.

GATE- 2001 (ECE)

Q18. An 8085 microprocessor based system uses a 4K x 8 bit RAM whose starting address is AA00 H. The address of the last byte in this RAM is **--- 1 mark**

(a) 0FFF H (b) 1000 H (c) B9FF H (d) BA00 H

Q19. Consider the following sequence of instructions for an 8085 microprocessor based system **---- 5 marks**

Memory Address	Instructions
FF00	MVI A, FF H
FF02	INRA
FF03	JC FF0C H
FF06	ORI A8 H
FF08	JM FF15 H
FF0B	XRA A
FF0C	OUT PORT1
FF0E	HLT
FF10	XRI FF H
FF12	OUT PORT2
FF14	HLT
FF15	MVI A, FF H
FF17	ADI 02 H
FF19	RAL
FF1A	JZ FF23 H
FF1D	JC FF10 H
FF20	JNC FF12 H
FF23	CMA
FF24	OUT PORT3
FF26	HLT

(a) if the program execution begins at the location FF00 H, write down the sequence of instructions which are actually executed till a HLT instruction. (Assume all flags are initially reset).

(b) Which of the three ports will be loaded with data, and what is the bit pattern of the data?

Q22. a) The program and machine code for an 8085 microprocessor are given by

```
3E      MVI   A, C3
C3
00      NOP
80      ADD   B
3D      DCR   A
C2      JNZ   800A
0A
80
C3      JMP   800C
0C
80
D3      OUT   10
10
76      HLT
```

The starting address of the above program is 7FFF H. What would happen if it is executed from 8000 H?

Notes:

GATE- 2000 (ECE)

Q20. In an 8085 microprocessor RST6 instruction transfers the program execution to the following location: **--- 1mark**

(a) 0030 H (b) 0024 H (c) 0048 H (d) 0060 H

Q21. The contents of Register (B) and Accumulator (A) of 8085 microprocessor are 49 H and 3AH respectively. The contents of A and the status of carry flag (CY) and sign flag (S) after executing SUB B instructions are **---- 1 mark**

a) A = F1 H, CY = 1, S = 1
b) A = 0F H, CY = 1, S = 1
c) A = F0 H, CY = 0, S = 0
d) A = 1F H, CY = 1, S = 1

(b) For the instructions given below, how many memory operations (read / write) are performed during the execution in an 8085 μP?
(I) Call 2000 H
(II) LDA 2000 H

(c) Write an instruction which takes the minimum possible time to clear the accumulator of the 8085. **---- 5 marks**

GATE- 1999 (ECE)

Q23. If CS = A_{15} A_{14} A_{13} is used as the chip select logic of a 4 K RAM in an 8085 system, then its memory range will be

(a) 3000 H – 3 FFF H (b) 7000 H – 7 FFF H
(c) 0000 H to 0FFF and 1000 to 1 FFF H
(d) 6000 H – 6FFF H and 7000 H – 7FFF H

Q24. An 8085 assembly language program is given below:

```
        MVIC, 03 H
        LXI H, 2000H
        MOV A, M
        DCR C
LOOP1:  INX H
        MOV B, M
        CMP B
        JNC LOOP2
        MOV A, B
LOOP2:  DCR C
        JNZ LOOP1
        STA 2100 H
        HLT
```

Contents of the memory locations 2000 H to 2002 H are:
2000 : 18 H; 2001 : 10 H; 2002 : 2BH
a) What does the above program do ?
b) At the end of the program, what will be

* the contents of the registers A, B, C, H and L ?
* the condition of the carry and zero flags ?
* the contents of the memory locations 2000H, 2001 H, 2002 H, 2100 H.

--- 5 marks

Notes:

GATE- 1998 (ECE)

Q25. An instruction used to set the carry Flag in a computer can be classified as
(a) data transfer (b) arithmetic
(c) logical (d) program control

GATE- 1997 (ECE)

Q26. In an 8085 μ P system, the RST instruction will cause an interrupt
(a) only if an interrupt service routine is not being executed
(b) only if a bit in the interrupt mask is made 0
(c) only if interrupts have been enabled by an EI instruction
(d) None of the above

Q27. The following instructions have been executed by an 8085μP

ADDRESS	INSTRUCTION
6010	LXI H, 8A 79 H
6013	MOV A, L
6014	ADD H
6015	DAA
6016	MOV H, A
6017	PCHL

From which address will the next instruction be fetched?
(a) 6019 (b) 6379
(c) 6979 (d) None of the above

Q28. An 8085 microprocessor uses a 2 MHz crystal. Find the time taken by it to execute the following delay subroutine, inclusive of the call instruction in the calling program.

Calling Program: ————————
————————
CALL DELAY
————————
————————

```
DELAY: PUSH PSW
       MVI A, 64 H
LOOP:  NOP
       DCR A
       JNZ LOOP
       POP PSW
       RET
```

You are given that a CALL instruction takes 18 cycles of the system clock, PUSH requires 12 cycles and a conditional jump takes 10 cycles if the jump is taken and 7 cycles if it is not. All other instructions used above take (3n+1) clock cycles, where n is the number of accesses to the memory, inclusive of the opcode fetch. — 5 marks

Notes:

GATE- 1996 (ECE)

Q29. The following sequence of instructions is executed by an 8085 microprocessor:

```
1000   LXI SP,27 FF
1003   CALL1006
1006   POP H
```

The contents of the stack pointer (SP) and the HL, register pair on completion of execution of these instructions are
a) SP = 27 FF, HL = 1003 b) SP = 27 FD, HL = 1003
c) SP = 27 FF, HL = 1006 d) SP = 27 FD, HL = 1006

GATE- 1995 (ECE) – 1 mark each

Q30. When a CPU is interrupted, it
a) stops execution of instructions
b) acknowledges interrupt and branches to subroutine
c) acknowledges interrupt and continues
d) acknowledges interrupt and waits for the next instruction from the interrupting device

Q31. A DMA transfer implies
(a) direct transfer of data between memory and accumulator
(b) direct transfer of data between memory and I/O devices without the use of microprocessor
(c) transfer of data exclusively within microprocessor registers
(d) A fast transfer of data between microprocessor and I/O devices

Q32. An "Assembler" for a microprocessor is used for
(a) assembly of processors in a production line
(b) creation of new programs using different modules
(c) translation of a program from assembly language to a machine language
(d) translation of a higher level language into English text.

GATE- 1993 (ECE) – 1 mark each

Q33. In a microprocessor, the address of the next instruction to be executed, is stored in
a) stack pointer b) address latch
c) Program counter d) general purpose register

KEY

01. d	02. c	03. c	04. b	05. c	06. b	07.d	08. d
09. c	10. c	11. b	12. b	13. c	14. d	15. a	16. c
17.	18. b	19.	20. a	21. a	22.	23. c	24.
25. b	26.c	27.c	28.	29. c	30. b	31. b	32.c
33. a							

Notes:

ACE EDUCATIONAL ACADEMY

MICROPROCESSORS

GATE Examination Questions

Electrical Engineering

GATE- 2009 (EEE)

Q01. In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become ---2 marks

```
XRA A
MVI B,F0 H
SUB B
```

(a) 01 H (b) 0F H (c) F0 H (d) 10 H

GATE- 2008 (EEE)

Q02. An input device is interfaced with Intel 8085 microprocessor as memory mapped I/O. The Address of the device is 2500H. In order to input data from the device to accumulator, the sequence of instructions will be

(a) LXI H, 2500H
MOV A, M

(b) LXI H, 2500H
MOV M, A

(c) LHLD 2500 H
MOV A, M

(d) LHLD 2500H
MOV M, A ----1 mark

Q03. The contents (in Hexadecimal) of some of the memory locations in an 8085 based system are given below

Address	Contents
..	..
26FE	00
26FF	01
2700	02
2701	03
2702	04
..	..

The contents of stack pointer (SP), program counter (PC) and (H, L) are 2700H, 2100 H and 0000H respectively. When the following sequence of instructions are executed,

```
2100 H: DAD SP
2101H: PCHL
```

the contents of (SP) and (PC) at the end of execution will be

(a) (PC)=2102H, (SP)=2700H (b) (PC)=2700H, (SP)=2700H
(c) (PC)=2800H, (SP)=26FEH (d) (PC)=2A02H, (SP)=2702H

GATE- 2007 (EEE)

Q04. Which one of the following statements regarding the INT (interrupt) and the BRQ (bus request) pins in a CPU is true? ---- 2 marks

(a) The BRQ pin is sampled after every instruction cycle, but the INT is sampled after every machine cycle
(b) Both INT and BRQ are sampled after every machine cycle
(c) The INT pin is sampled after every instruction cycle, but the BRQ is sampled after every machine cycle
(d) Both INT and BRQ are sampled after every instruction cycle

Notes:

GATE- 2006 (EEE)

Q05. A software delay subroutine is written as given below:

```
DELAY: MVI H, 255D
       MVI L, 255D
LOOP:  DCR L
       JNZ LOOP
       DCR H
       JNZ LOOP
```

How many times DCR L instruction will be executed?

(a) 255 (b) 510 (c) 65025 (d) 65279 ---- 2 marks

Q06. In an 8085 A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D,E) register pair and store the result in same location. The sequence of instructions is ---- 2 marks

(a) XCHG
INR M

(b) XCHG
INX H

(c) INX M
XCHG

(d) INR M
XCHG

GATE- 2005 (EEE)

Q07. The 8085 assembly language instruction that stores the content of H and L registers into the memory locations 2050H and 2051H respectively is ---- 1 mark

(a) SPHL 2050 H (b) SPHL 2051 H
(c) SHLD 2050 H (d) STAX 2050 H

GATE- 2004 (EEE)

Q08. If the following program is executed in a microprocessor, the number of instruction cycles it will take from START to HALT is

```
START: MVI A, 14 H
SHIFT: RLC
       JNZ SHIFT
       HLT
```

(a) 4 (b) 8 (c) 13 (d) 16

GATE- 2003 (EEE) – each 2 marks

Q09. A memory system has a total of 8 memory chips, each with 12 address lines and 4 data lines. The total size of the memory system is

(a) 16 Kbytes (b) 32 Kbytes
(c) 48 Kbytes (d) 64Kbytes

Q10. The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

```
LXI H, 1FFE
MOV B,M
INR L
MOV A, M
ADD B
INR L
MOV M, A
XRA A
```

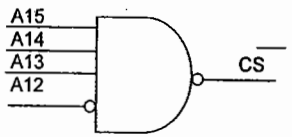
On completion of the execution of the program, the result of addition is found

(a) in the register A (b) at the memory address 1000
(c) at the memory address 1F00
(d) at the memory address 2000

Notes:

GATE- 2002 (EEE)

Q11. The logic circuit used to generate the active low chip select (CS) by an 8085 microprocessor to address a peripheral is shown in fig. The peripheral will respond to addresses in the range —— 2 marks



(a) E000 – EFFF (b) 000E – FFFE
(c) 1000 – FFFF (d) 0001 – FFF1

GATE- 2001 (EEE)- 2 marks

Q12. An Intel 8085 processor is executing the program given below.

```
    MVI A, 10 H
    MVI B, 10 H
BACK :NOP
    ADD B
    RLC
    JNC BACK
    HLT
```

The number of times that the operation NOP will be executed is equal to
(a) 1 (b) 2 (c) 3 (d) 4

GATE- 2000 (EEE) -- 1 mark

Q13. Which one of the following is not a vectored interrupt?
(a) TRAP (b) INTR (c) RST 7.5 (d) RST 3

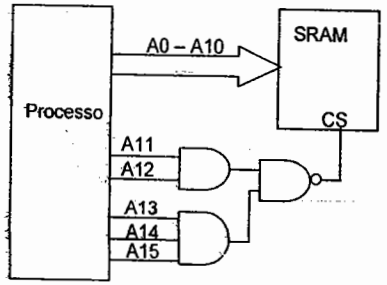
GATE- 1999 & 1998 (EEE)

Nil

GATE- 1997 (EEE)

Q14. In a microprocessor, the address of the next instruction to be executed, is stored in —— 1 mark
(a) stack pointer (b) address latch
(c) program counter (d) general purpose register

Q15. The range of addresses for which the memory chip shown in figure will be selected is from —— to ——. —— 2 marks



Notes:

GATE- 1996 (EEE)

Q16. In an 8085 microprocessor, the following instructions may result in change of accumulator contents and change in status flags. Choose the correct match for each instruction

(a) ANA r (P) A = No change; Cy = 1; Ac = No change
(b) XRA r (Q) A = No change; Cy = 1; Ac = 1
(c) CMP r (R) A = No change; Cy = 1; Ac = 0
(S) A = No change; Cy = 1; Ac = 0
(T) A = No change; Cy = 1; Ac = 0 —— 2 marks

GATE- 1995 (EEE)

Q17. In an 8085 microprocessor, after the execution of XRA A instruction

(a)the carry flag is set
(b) the accumulator contains FF H
(c) the zero flag is set
(d) the accumulator contents are shifted left by one bit

GATE- 1994 (EEE) – 1 mark

Q18. The content of the accumulator in an 8085 microprocessor is altered after the execution of the instruction.
(a) CMP C (b) CPI 3A (c) ANI 5C (d) ORA A

GATE- 1993 (EEE) -- 1 mark

Q19. Three devices A, B & C have to be connected to a 8085 microprocessor. Device A has highest priority and device C has the lowest priority. In this context which of the following is correct assignment of interrupt inputs?
(a) uses TRAP , B uses RST 5.5 and C uses RST 6.5
(b)A uses RST 7.5 , B uses RST 6.5 and C uses RST 5.5
(c)A uses RST 5.5 , B uses RST 6.5 and C uses RST 7.5
(d)A uses RST 5.5 , B uses RST 6.5 and C uses TRAP

GATE- 2009 (EI)

Q20. Consider a system consisting of a microprocessor, memory, and peripheral devices connected by a common bus. During DMA data transfer, the microprocessor —— 1 marks
(a) only reads from the bus
(b) only writes to the bus
(c) both reads from and writes to the bus
(d) neither reads from nor writes to the bus

Notes:

Q21. The following is an assembly language program for 8085 microprocessor: —2 marks

Address	Instruction Code	Mnemonic
1000 H	3E, 06	MVI A, 06 H
1002 H	C6, 70	ADI 70 H
1004 H	32, 07, 10	STA 1007 H
1007 H	AF	XRA A
1008 H	76	HLT

(a) 00 H (b) 06 H (c) 70 H (d) 76 H

GATE- 2008 (EI)

Q22. A 2K x 8 bit RAM is interfaced to an 8-bit microprocessor. If the address of the first memory location in the RAM is 0800 H, the address of the last memory location will be ----1 mark

(a) 1000H (b) 0FFFH
(c) 4800 H (d) 47FF H

Q23. A part of the program written for an 8085 microprocessor is shown below. When the program execution reaches LOOP2, the value of register C will be ---- 2 marks

```
        SUB A
        MOV C,A
LOOP1 : INR A
        DAA
        JC LOOP2
        INR C
        JNC LOOP1
LOOP2 : NOP
```

(a) 63 H (b) 64 H (c) 99 H (d) 100 H

GATE- 2007 (EI)

Q24. A snapshot of the address, data and control buses of an 8085 microprocessor executing a program is given below: - 2 marks

Address	2020 H
Data	24 H
IO/M'	Logic High
RD'	Logic High
WR'	Logic Low

The assembly language instruction being executed is
(a) IN 24 H (b) IN 20 H
(c) OUT 24 H (d) OUT 20 H

Notes:

Q25. 8-bit signed integers in 2's complement form are read into the accumulator of an 8085 microprocessor from an I/O port using the following assembly language program segment with symbolic addresses.

```
BEGIN: IN PORT
       RAL
       JNC BEGIN
       RAR
END:   HLT
```

This program
(a) halts upon reading a negative number
(b) halts upon reading a positive number
(c) halts upon reading a zero
(d) never halts ---- 2 marks

GATE- 2006 (EI)

Q26. A memory mapped I/O device has an address of 00F0H. which of the following 8085 instruction outputs the content of the accumulator to the I/O device? ---- 1 marks

(a) LXI H, 00F0H
MOV M, A

(b) LXI H, 00F0H
OUT M

(c) LXI H, 00F0H
OUT F0H

(d) LXI H, 00F0H
MOV A,M

Q27. An 8085 assembly language program is given as follows. The execution time of each instruction is given against the instruction in terms of T-state. ---2 marks

Instruction	T-state
MVI B, 0A H	7T
LOOP: MVI C, 05 H	7T
DCR C	4T
DCR B	4T
JNZ LOOP	10T/7T

The execution time of the program in terms of T-states is
(a) 247 T (b) 250 T (c) 254 T (d) 257 T

GATE- 2005 (EI)

Q28. The time period of a square ware in the audio frequency range is measured using an 8085 microprocessor by feeding the square wave to one of the four interrupts, namely, RST 7.5, RST 6.5, RST 5.5 or INT. The algorithm used starts a timer at the beginning of a time period, stops the timer at the beginning of the next time period and reads the timer values for time measurement. Which of the following interrupts should be selected for this application?
(a) INTR (b) RST 5.5 (c) RTS 6.5 (d) RST 7.5

Q29. An 8-bit microcontroller has an external RAM is in the memory map from 8000 H to 9FFF H. The number of bytes this RAM can store is
(a) 8193 (b) 8191 (c) 8192 (d) 8000

Q30. In an 8085 microprocessor, which one of the following is the correct sequence of the machine cycles for the execution of the DCR M instruction? --- 1 mark
(a) op-code fetch
(b) op-code fetch, memory read, memory write
(c) op-code fetch, memory read
(d) op-code fetch, memory write, memory write

Notes:

Q31. A microprocessor has an instruction XOR (r1,r2), which performs an exclusive OR operation of registers r1, r2 and stores the result in r1. After the following instructions are executed which one of the following is true?

```
XOR ( r2, r1)
XOR ( r1, r2)
XOR ( r2, r1)
```

(a) the contents of r1 is half sum of r1 and r2
(b) the contents of r2 is half sum of r1 and r2
(c) the contents of r1 and r2 remains unaltered
(d) the contents of r1 and r2 are swapped — 1 mark

Q32. In an 8085 microprocessor the value of Stack Pointer (SP) is 2010H and that of DE pair is 1234H before the following code is executed. The value of the DE register pair after the following code is executed is —2 marks

```
LXI H, 0000H
PUSH H
PUSH H
POP B
DAD SP
XCHG
```

(a) 200E H (b) 200C H (c) 2010 H (d) 1234 H

GATE- 2004 (EI)

Q33. The vectored address corresponding to the software interrupt RST 7 in 8085 microprocessor is —1 mark
(a) 0017 H (b) 0027 H (c) 0038 H (d) 0700 H

Q34. The following 8085 instructions are executed sequentially. — 2 marks

```
XRA A
MOV L, A
MOV H, L
INH H
DAD H
```

After execution, the content of HL register pair is
(a) 0000 H (b) 0101 H (c) 0001 H (d) 0002 H

GATE- 2003 (EI)

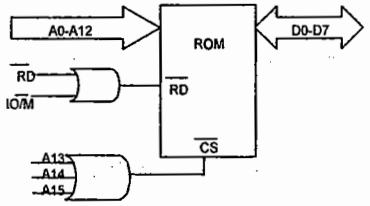
Q35. Some of the pins of an 8085 CPU and their functions are listed below. Identify the correct answer that matches the pins to their respective functions —— 1 mark

P. RST 7.5	1. Selects IO or memory
Q. HOLD	2. Demuxes address and data bus
R. IO/M'	3. Is a vectored interrupt
S. ALE	4. Facilitates DMA operation
	5. Is a clock
	6. Selects BCD mode operation

(a) P-3, Q-2, R-1, S-4 (b) P-4, Q-1, R-5, S-3
(c) P-3, Q-4, R-1, S-2 (d) P-2, Q-3, R-6, S-1

Notes:

Q36. A ROM is interfaced to an 8085 CPU as indicated in figure below. The address range occupied by the ROM is —— 2 marks



(a) 0000 - 0FFF H (b) 0000 – 1FFF H
(c) 0000 – 2FFF H (d) 8000 – 9FFF H

Q37. In an 8085 system containing 8KB of ROM and 8KB of RAM, the ROM is selected when A15 is 0 and RAM is selected when A15 is 1. A13 and A14 are unused. The CPU executed the following program —— 2 marks

```
MVI A, 00 H
STA 8080 H
DCR A
STA C080 H
RET
```

The content of memory location 8080 H after the execution of the RET instruction is
(a) FF H (b) FE H (c) 01 H (d) 00 H

GATE- 2002 (EI)

Q38. In an INTEL 8085 microprocessor the address bus and data bus are --1 mark
(a) Non multiplexed (b) Multiplexed
(c) Duplicated (d) Same as control bus

Q39. In an 8085 based system the subroutine TEST given below is called by another program. When the processor returns from the subroutine TEST, the value in the accumulator will be

```
TEST: MVI A, 00 H
      CALL TESK
TESK: INR A
      RET
```

(a) 01 H (b) 02 H (c) 20 H (d) FF H

Q40. A minimal microcomputer system is constructed using INTEL 8085 microprocessor, an 8156 RAM and an 8355 ROM. The chip enable CE of 8156 and chip enable CE of 8355 are connected to the address line A12 of 8085. The address of port A of the 8156 chip is — 2 marks

(a) 21 H (b) 12 H (c) 11 H (d) 20 H

Notes:

Q41. The 14-bit timer of 8156 is loaded with the counter value of 07D0 H. the timer input is connected to a clock with a frequency of 800 KHz. The timer is programmed to produce a continuous signature wave output. The frequency of the square wave output is
--- 2 marks

(a) 400 KHz (b) 800 KHz
(c) 400 Hz (d) 2000 KHz

Notes:

GATE- 2001 (EI)

Q42. In a microprocessor with 16 address and 12 data lines, the maximum number of opcodes is ---- 1 mark
(a) 2^6 (b) 2^8 (c) 2^{12} (d) 2^{16}

Q43. An m-bit microprocessor has m-bit — 1 mark
(a) flag register (b) instructions register
(c) data registers (d) program counter

Q44. In 8085 microprocessor, CY flag may be set by the instruction ---- 1 mark
(a) SUB (b) INX (c) CMA (d) ANA

Q45. Microprocessor 8085 regains control of the bus ---- 1 mark
(a) immediately after HOLD goes low
(b) immediately after HOLD goes high
(c) after half-clock cycle after HLDA goes low
(d) after half-clock cycle after HLDA goes high

GATE- 2000 (EI)

Q46. Find the correct match among the following pair in the context of an 8085 microprocessor: ----- 1 mark

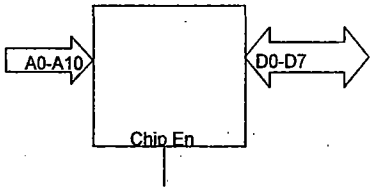
P. DAA	1. Program control transfer instruction
Q. LXI	2. Data movement Instruction
R. RST	3. Interrupt instruction
S. JMP	4. Arithmetic Instruction

(a) P-4, Q-2, R-3, S-1
(b) P-3, Q-2, R-1, S-4
(c) P-1, Q-2, R-3, S-4
(d) P-4, Q-3, R-2, S-1

Q47. In an 8085 microprocessor, the Stack Pointer (SP) and Program Counter (PC) register contain the number the number F000 and 2400 in Hex respectively. The contents of the register after execution of the instruction CALL E0000 would be ----- 1 mark

(a) PC : F003 SP : 2400
(b) PC : E000 SP : 2400
(c) PC : E000 SP : EFFE
(d) PC : E000 SP : 23FE

Q48. 2K bytes of ROM have to be interfaced to an 8085 microprocessor using one EEPROM chip. The relevant pins of the EEPROM are shown in fig. The address space assigned to the ROM chip in hex is C000-C7FF H.
– 5 Marks
(a) Show how the address and data lines of the 8085 are to be connected to those of the EEPROM chip.
(b) Design the address decoding circuit whose output is to be connected to the chip enable pin of the EEPROM chip using only 2-input AND gate and inverters.



Notes:

GATE- 1999 (EI) --Nil

GATE- 1998 (EI)

Q49. Identify software interrupt instruction in 8085 microprocessor ---- 1 mark
(a) INT (b) RST 5 (c) RST 7.5 (d) RST 6.5

GATE- 1997 (EI)

Q50. The stack pointer in a microprocessor is a register containing ---- 1 mark
(a) the address of the next operand
(b) the current size of the stack
(c) the address of the top of the stack
(d) the address for storing the result of arithmetic operation

GATE- 1994 (EI)

Q51. The contents of the Stack memory in a microprocessor system are retrieved on first-in-first out basis. (True or False) -- 1 mark

Q52. The program counter of 8-bit microprocessor is always a 8-bit register. (True or False) — 1 mark

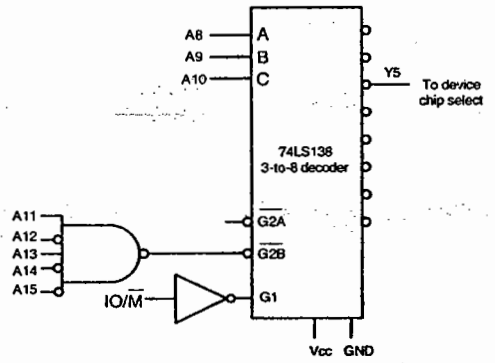
GATE- 2010 (ECE)

Q53. For the 8085 assembly language program given below, the content of the accumulator after the execution of the program is —— 2 Marks

```
3000 MVI  A, 45 H
     3002 MOV  B,A
     3003  STC
     3004  CMC
     3005  RAR
     3006  XRA  B
```

(a) 00 H (b) 45 H (c) 67 H (d) E7 H

Q54. In the circuit shown, the device connected to Y5 can have address in the range



(a) 2000 - 20FF (b) 2D00 -- 2DFF
(c) 2E00 -- 2EFF (d) FD00 – FDFF

GATE- 2010 (EEE)

Q55. When a "CALL Addr" instruction is executed, the CPU carries out the following sequential operations internally:
Note: (R) means content of register R —— 1 Marks
((R)) means contents of memory location pointed to by R
PC means Program Counter
SP means Stack Pointer

(a) (SP) incremented
(PC) ← Address
((SP)) ← (PC)

(b) (PC) ← Address
((SP)) ← (PC)
(SP) ← incremented

(c) (PC) ← Address
(SP) incremented
((SP)) ← (PC)

(d) ((SP)) ← (PC)
(SP) incremented
(PC) ← Address

GATE- 2010 (EI)

Q56. The subroutine SBX given below is executed by an 8085 processor. The value in the accumulator immediately after execution of the subroutine will be: —— 1 Marks

```
SBX: MVI A,99 H
     ADI 11 H
     MOV C, A
     RET
```

(a) 00 H (b) 11 H (c) 99 H (d) AA H

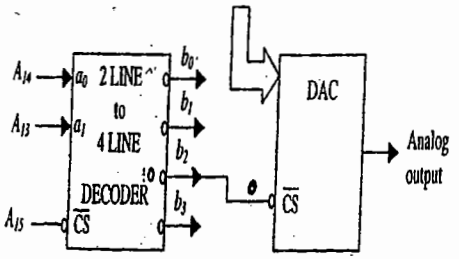
Notes:

Q57. In an 8085 processor, the main program calls the subroutine SUB 1 given below. When the program returns to the main program after executing SUB 1, the value in the accumulator is ——— 2 Marks

Address	Opcode	Mnemonic
2000	3E, 00	SUB1: MVI A, 00 H
2002	CD, 05, 20	CALL SUB2
2005	3C	SUB2: INR A
2006	C9	RET

(a) 00 H (b) 01 H (c) 02 H (d) 03 H

Q58. An 8-bit DAC is interfaced with a microprocessor having 16 address lines (A0, ...A15) as shown in the figure. A possible valid address for this DAC is



(a) 3000 H (b) 4FFF H (c) AFFF H (d) C000 H

KEY

01.d	02. c	03. b	04.c	05.d	06.a	07.c	08.
09.a	10.c	11.a	12.c	13. b	14.c	15.	16.
17.c	18.c	19.b	20.d	21. d	22. b	23.	24.b
25. a	26.a	27.c	28.d	29.c	30. b	31.d	32.a
33.c	34.d	35.c	36.b	37.a	38.b	39.b	40.
41.	42.c	43.c	44.a	45. a	46. a	47.c	48.
49.b	50.c	51.False		52. False		53.d	54.b
55.d	56.d	57.c	58.c				

Notes:

PUBLIC SECTOR EXAMINATION QUESTIONS (DIGITAL ELECTRONICS) - 2009

01. A 5 bit DAC has a current output. For a digital input of 10100, an output current of 10 mA is produced. What will be the output current for a digital input of 11101? **(ISRO)**

(a) 14.5 mA (b) = 10 mA (c) = 100 mA (d) Not possible to calculate

02. If a counter having 10 FFs is initially at 0, what count will it hold after 2060 pulses? **(ISRO)**

(a) 000 000 1100 (b) 000 001 1100
(c) 000 001 1000 (d) 000 000 1110

03. A certain JK FF has t_{pd} = 12 ns. The largest MOD counter that can be constructed from such FFs and still operate up to 10 MHz is **(ISRO)**

(a) 16 (b) 256 (c) 8 (d) 128

04. A 12 bit ADC is operating with a 1 μs clock period and the total conversion time is seen to be 14 μs. The ADC must be of **(ISRO)**

(a) Flash type (b) Counting type
(c) Integrating type (d) Successive Approximation type

05. Which of the following types of devices is not field programmable? **(ISRO)**

(a) FPGA (b) ASIC (c) CPLD (d) PLD

06. Which is the correct order of different process steps for a typical FPGA design? **(ISRO)**

(a) Functional simulation, Synthesis, Place & Route, Timing Verification
(b) Functional simulation, Timing Verification, Synthesis, Place & Route
(c) Timing Verification, Synthesis, Functional simulation, Place & Route
(d) Synthesis, Functional simulation, Timing Verification, Place & Route

07. The theoretical dividing line between Reduced Instruction Set computing (RISC) microprocessor and Complex Instructions Set Computing (CISC) microprocessor is **(ISRO)**

(a) Instruction execution rate to be one instruction per clock cycle
(b) Number of address and data lines
(c) Number of pins in the chip
(d) None of the above

08. Which of the following technology results in least power dissipation? **(ISRO)**

(a) CMOS (b) ECL (c) TTL (d) NMOS

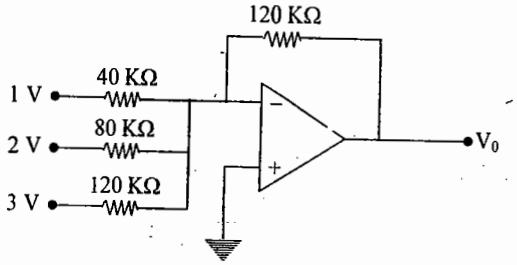
09. The greatest negative number which can be stored in a computer that has 8-bit word length and uses 2's complement arithmetic is **(ISRO)**

(a) – 256 (b) – 255 (c) – 128 (d) – 127

10. Which of the following ADCs uses over sampling in its operation **(ISRO)**

(a) Sigma-delta ADC (b) Counter ramp converter
(c) Successive Approximation Register ADC (d) Flash Converter

11.



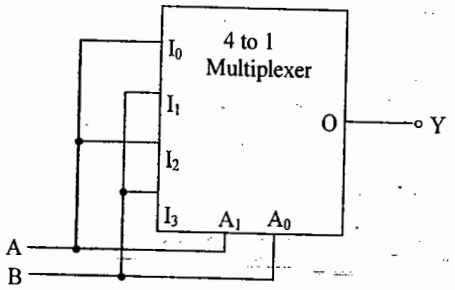
In the circuit shown in the above figure, the value of output V_0 is **(ISRO)**

(a) + 6 V (b) – 9 V (c) – 6 V (d) + 9 V

12. In the logic equation $A(A+\overline{B}\overline{C}+C)+\overline{B}(\overline{C}+\overline{A}+BC)(A+\overline{B}C+A\overline{C})=1$, if $C=\overline{A}$ then **(DRDO)**

(a) A + B = 1 (b) $\overline{A}$ + B = 1 (c) A + $\overline{B}$ = 1 (d) A = 1

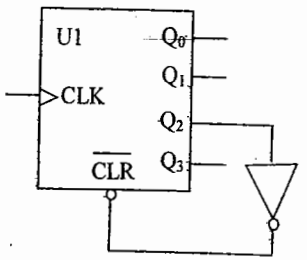
13. A gate having two inputs (A, B) and one output (Y) is implemented using a 4-to-1 multiplexer as shown in Fig. A_1(MSB) and A_0 are the control bits and $I_0 - I_3$ are the inputs to the multiplexer. The gate is **(DRDO)**



(a) NAND (b) NOR (c) XOR (d) OR

14. In Fig. U1 is a 4-bit binary synchronous counter with synchronous clear. Q_0 is the LSB and Q_3 is the MSB of the output. **(DRDO)**

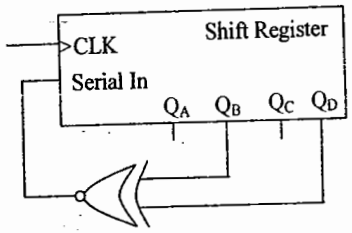
The circuit shown in Fig. represents a
(a) mod 2 counter
(b) mod 3 counter
(c) mod 4 counter
(d) mod 5 counter



15. An increase in the value of the hold capacitor in a sample-and-hold circuit results in **(DRDO)**

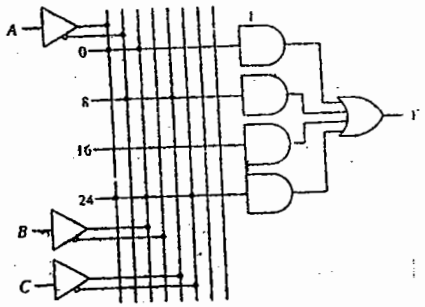
(a) decrease in the acquisition time and decrease in the droop rate
(b) decrease in the acquisition time and increase in the droop rate
(c) increase in the acquisition time and increase in the droop rate
(d) increase in the acquisition time and decrease in the droop rate

16. A 4-bit serial-in-parallel-out shift register is used with a feedback as shown in Fig. The shifting sequence is $Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$. **(DRDO)**



If the output is 0000 initially, the output repeats after
(a) 4 clock cycles (b) 6 clock cycles (c) 15 clock cycles (d) 16 clock cycles

17. Fig. shows a section of a Programmable Logic Device (PLD). **(DRDO)**



The Boolean expression implemented in the PLD is
(a) $AC + AB + \bar{A}B\bar{C}$ (b) $A\bar{C} + \bar{A}B + AB\bar{C}$
(c) $AB + \bar{A}C + A\bar{B}C$ (d) $AB + \bar{A}C + AB\bar{C}$

18. For an 8-bit digital-to-analog converter having reference voltage of 8 V, the least significant 4 bits of the input are grounded and the most significant 4 bits are driven by 4 bit data from a binary counter. The maximum obtainable peak-to-peak amplitude of a waveform at the output of the digital-to-analog converter is **(DRDO)**
(a) 4 V (b) 6 V (c) 7.2 V (d) 7.5 V

19. Which one of the following Boolean expressions is **NOT** correct? **(JTO)**
(a) $\overline{x+y} = \bar{x}\bar{y}$ (b) $\overline{\bar{x}+y} = \bar{x}\,\bar{y}$
(c) $\overline{\bar{x}\,\bar{y}} = \bar{x}+\bar{y}$ (d) $\overline{\bar{x}+\bar{y}} = \bar{x}\,\bar{y}$

20. A Boolean function can be expressed **(JTO)**
(a) as sum of maxterms or product of minterms
(b) as product of maxterms or sum of minterms
(c) partly as product of maxterms and partly as sum of minterms
(d) partly as sum of maxterms and partly as product of minterms

21. Among the following logic families, the one having the lowest power dissipation and highest noise margin is **(JTO)**
(a) Schottky TTL (b) TTL (c) ECL (d) CMOS

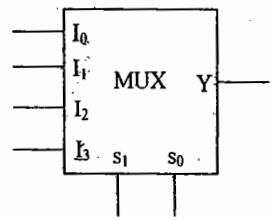
22. The Characteristic equation of a level triggered T flip-flop, with T as input and Q as output is **(JTO)**
(a) $Q(n+1) = T\bar{Q} + \bar{T}Q$ (b) $Q(n+1) = \bar{T}$
(c) $Q(n+1) = Q$ (d) $Q(n+1) = TQ + \bar{T}\,\bar{Q}$

23. A Combinational circuit accepts a 2 bit binary number and outputs its square in binary. To design this circuit using a ROM, the minimum size of ROM required is **(JTO)**
(a) 2 × 2 (b) 4 × 2 (c) 4 × 4 (d) 8 × 4

24. For the truth table given in Figure, the minimized Boolean expression is **(JTO)**
(a) $p = xyz + \bar{x}y\bar{z} + x\bar{y}\bar{z} + \bar{x}\bar{y}z$
(b) $p = \overline{x \oplus y \oplus z}$
(c) $p = x\overline{(y \oplus z)} + x(y \oplus z)$
(d) $p = x \oplus \bar{y} \oplus z$

Input			Output
x	y	z	p
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

25. The Boolean function $F(A, B, C) = \prod(0, 2, 4, 7)$ is to be implemented using a 4 × 1 multiplexer shown in figure. Which one of the following choices of inputs to multiplexer will realize the Boolean function? **(JTO)**



(a) $(I_0, I_1, I_2, I_3, s_1, s_0) = (1, 0, \bar{A}, A, C, B)$
(b) $(I_0, I_1, I_2, I_3, s_1, s_0) = (1, 0, \bar{A}, A, B, C)$
(c) $(I_0, I_1, I_2, I_3, s_1, s_0) = (0, 1, \bar{A}, A, C, B)$
(d) $(I_0, I_1, I_2, I_3, s_1, s_0) = (0, 1, A, \bar{A}, B, C)$

26. An edge triggered synchronous binary counter is provided with a clock (CLK) and control inputs: active low clear ($\overline{CLR}$), active high load (L) and active high count (C). The correct matching combination between Column A and Column B is **(JTO)**

Column A	Column B
1. (CLK, $\overline{CLR}$, L, C) = (↑, 1, 1, X)	P. No change
2. (CLK, $\overline{CLR}$, L, C) = (↑, 1, 0, 1)	Q. Load inputs
3. (CLK, $\overline{CLR}$, L, C) = (X, 0, X, X)	R. Count next binary state
4. (CLK, $\overline{CLR}$, L, C) = (X, 1, 0, 0)	S. Clear outputs

Where X = don't care.

(a) 1-Q, 2-R, 3-S, 4-P (b) 1-P, 2-Q, 3-R, 4-S
(c) 1-Q, 2-R, 3-P, 4-S (d) 1-P, 2-Q, 3-S, 4-R

27. A 5-bit serial adder is implemented using two 5-bit shift registers, a full adder and a D flip-flop. The two binary words to be added are 11011 and 11011. The sum of the two numbers is stored in one of the shift registers and the carry in the D flip-flop. Assuming that the D flip-flop is set initially, the content of the sum shift register and the D flip-flop, respectively, are **(JTO)**

(a) 10111 and 0 (b) 11011 and 1 (c) 11101 and 0 (d) 10111 and 1

28. The Boolean expression $(A + B)\,\overline{(A + B)}$ is equivalent to a two-input **(EEE- JTO)**

(a) NAND gate (b) NOR gate (c) X-OR gate (d) X-NOR gate

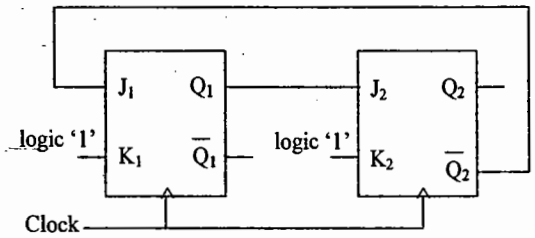
29. The minimum number of MOS transistors required to make a dynamic RAM cell is **(EEE- JTO)**

(a) 1 (b) 2 (c) 3 (d) 4

30. How many minimum number of NOR gates are required to realize a two-input X-OR gate? **(EEE- JTO)**

(a) 2 (b) 3 (c) 4 (d) 5

31. The sequential circuit shown in Fig. will act as a **(EEE- JTO)**



(a) Mod – 1 counter (b) Mod – 2 counter
(c) Mod – 3 counter (d) Mod – 4 counter

32. The total number of Boolean functions that can be constructed for n Boolean variables is **(DRDO-CSE)**

(a) n (b) 2^n (c) $(2^n)^n$ (d) $2^{(2^n)}$

33. Consider two 4-bit numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ and the expression $x_i = A_i B_i + \overline{A_i}\,\overline{B_i}$ for i = 0, 1, 2, 3. The expression $A_3\overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$ evaluates to 1 if **(DRDO-CSE)**

(a) A = B (b) A ≠ B (c) A > B (d) A < B

34. An odd function involving three Boolean variables is **(DRDO-CSE)**

(a) $\Sigma(1, 3, 5, 7)$ (b) $\Sigma(0, 2, 4, 6)$
(c) $\Sigma(1, 2, 4, 7)$ (d) $\Sigma(0, 3, 5, 6)$

35. How many 2-to-4-line decoders with enable input are needed to construct a 4-to-16-line decoder? **(DRDO-CSE)**

(a) 4 (b) 5 (c) 6 (d) 8

36. The function $f(A, B, C, D) = \Sigma(5, 7, 9, 11, 13, 15)$ is independent of variable(s) **(DRDO-CSE)**

(a) B (b) C (c) A and C (d) D

37. $(3527)_8$ is equivalent to **(DRDO-CSE)**

(a) $(757)_{16}$ (b) $(1879)_{10}$ (c) $(131113)_4$ (d) All of these

38. How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after 1001100111? **(DRDO-CSE)**

(a) 3 (b) 4 (c) 6 (d) 10

39. An 8 x 1 multiplexer has input A, B and C connected to the selection input s_2, s_1 and s_0 respectively. The data input I_0 to I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ and $I_6 = \overline{D}$. The Boolean function that the multiplexer implements is **(DRDO-CSE)**

(a) $f(A, B, C, D) = \Sigma(1, 6, 7, 9, 10, 11, 12)$
(b) $f(A, B, C, D) = \Sigma(0, 3, 4, 5, 11, 12)$
(c) $f(A,B, C, D) = \Sigma(1, 3, 5, 7, 9, 11, 13, 15)$
(d) $f(A, B, C, D) = \Sigma(0, 1, 3, 4, 5, 6, 12)$

40. The Characteristic equation of T flip-flop is given by **(ISRO)**

(a) $Q(n+1) = T\overline{Q} + \overline{T}Q$ (b) $Q(n+1) = \overline{T}$
(c) $Q(n+1) = Q$ (d) $Q(n+1) = TQ + \overline{T}\,\overline{Q}$

41. A Melay state machine's output depends on

(a) State and outputs (b) Inputs
(c) State (d) State and inputs

KEY

1. A	2. A	3. C	4. D	5. B	6. D	7. A	8. A	9. C	10. A
11. B	12. C	13. D	14. C	15.	16. B	17.	18. D	19. D	20. B
21. D	22. A	23. B	24. B	25. D	26. A	27. D	28. C	29. A	30. D
31. C	32. D	33. C	34. C	35. B	36. B	37. D	38. B	39.A	40. A
41. D									

PUBLIC SECTOR EXAMINATION QUESTIONS (MICROPROCESSOR) – 2009

01. A micro controller differs from a microprocessor in terms of **(ISRO)**

(a) I/O interfaces and instruction decoding
(b) Memory configuration and I/O interfaces
(c) Data bus width and clock speed
(d) Memory configuration and instruction decoding

02. An 8-bit microcontroller has an external RAM with the memory map from 8000H to 9FFFH. The number of bytes this RAM can store is **(ISRO)**

(a) 8193 (b) 8192 (c) 8191 (d) 8000

03. Consider the following program for 8085 **(ISRO)**

```
      XRA A
      LXI B, 0007H
LOOP: DCX B
      JNZ LOOP
```

The loop will be executed
(a) 8 times (b) once (c) 7 times (d) infinite times

04. Which one of the following statements about the 8085 is TRUE? **(DRDO)**

(a) Only accumulator can be loaded with an 8-bit number in a single instruction.
(b) The processor can be interrupted even after it executes HLT instruction.
(c) When HOLD input is activated, the processor can execute register-to-register instructions.
(d) The program and data memories are separate.

05. The contents of the HL register pair after the execution of the following program on the 8085 are **(DRDO)**

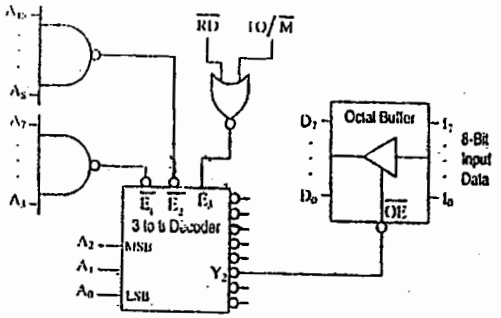
```
LXI H, 2095H
LXI B, 8FBFH
PUSH B
XTHL
POPH
HLT
```

(a) 2095H (b) 20BFH (c) 8F95H (d) 8FBFH

06. When the 8085 receives an interrupt on its INTR pin, **(DRDO)**

(a) the program is directly transferred to a fixed call location
(b) 8085 waits till an interrupt acknowledgement is received and transfers program to a fixed call location
(c) the call location is determined by an external device
(d) the program is transferred to a call location indicated by HL register pair

07. The Fig. shows an interfacing circuit for the 8085 microprocessor to read an 8-bit data from an external device. **(DRDO)**



The appropriate instruction for reading the data is

(a) MVI A, FAH (b) IN FAH (c) IN FFFAH (d) LDA FFFAH

08. In a 8085 microprocessor system, the active low chip select $(\overline{CS})$ signal is generated by passing address lines A_{15}, ..., A_{10} through a 6 inputs NAND gate. For selecting the address range CC00 to CFFF, the inputs to the NAND gate are **(JTO)**

(a) $A_{10}, A_{11}, \overline{A_{12}}, \overline{A_{13}}, A_{14}, A_{15}$ (b) $\overline{A_{10}}, \overline{A_{11}}, A_{12}, A_{13}, \overline{A_{14}}, \overline{A_{15}}$

(c) $A_{10}, A_{11}, \overline{A_{12}}, A_{13}, A_{14}, A_{15}$ (d) $A_{10}, A_{11}, A_{12}, A_{13}, A_{14}, A_{15}$

09. In the context of 8085 microprocessor, the correct matching combination between Column A and Column B is **(JTO)**

Column A	Column B
P. ALE	1. Rotate accumulator left
Q. PSW	2. Compare with accumulator
R. CMA	3. Program status word
S. RLC	4. Address latch enable
	5. Program stack word
	6. Arithmetic logic enabled
	7. Complement accumulator
	8. Rotate accumulator left through carry

(a) P-6, Q-5, R-2, S-8 (b) P-4, Q-3, R-2, S-8

(c) P-4, Q-5, R-7, S-1 (d) P-6, Q-5, R-7, S-1

10. A 8085 microprocessor program uses all available Jump instructions, each only once. For this program, the total memory (in Bytes) occupied by the Jump instructions is **(JTO)**

(a) 30 (b) 27 (c) 24 (d) 18

11. The content of the memory location 2068 H after the execution of the following 8085 program is **(JTO)**

```
LHIB  2070H
MVI   A, 8FH
MVI   C, 68H
SUB   C
ANI   0FH
STAX  B
HLT
```

(a) 04 H (b) 07 H (c) 09 H (d) 0F H

12. An arithmetic operation in the 8085 microprocessor sets the sign and parity flags. The contents of the accumulator after the execution of the operation can be **(ELECTRICAL JTO)**

(a) 1011 0100 (b) 0010 1101 (c) 1010 1101 (d) 0110 0111

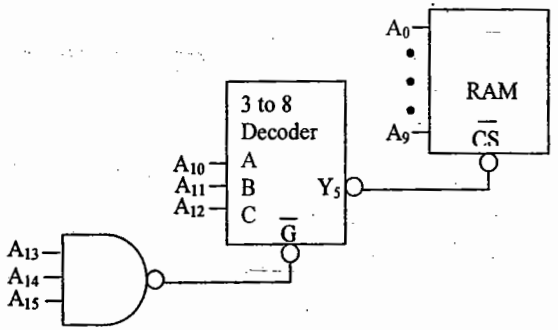
13. An instruction of the 8085 microprocessor that requires both memory read and memory write machine cycles is **(ELECTRICAL JTO)**

(a) MVI M, 8F (b) LHLD 8088 (c) RST 1 (d) ADD M

14. The duration of one T-state in the 8085 microprocessor that uses a crystal of 5.00 MHz is **(ELECTRICAL JTO)**

(a) 0.2 μs (b) 0.4 μs (c) 2.5 μs (d) 5.0 μs

15. The range of the address of the RAM which is interfaced to a microprocessor as shown in fig. is **(ELECTRICAL JTO)**



(a) 1400 – 17FF (b) E400 – EFFF

(c) F000 – FFFF (d) F400 – F7FF

16. After the execution of the following program in the 8085 microprocessor, the contents of

the accumulator are (ELECTRICAL JTO)

Address	Code	Mnemonics
203A	3E 20	MVI A, 20H
203C	2A, 3A 20	LHLD 203AH
203F	86	ADD M
2040	76	HLT

(a) 20H (b) 40H (c) 5EH (d) 7CH

17. The size of address bus of a microprocessor is 20 bits and the size of data bus is 8 bits. What is the maximum number of RAM chips of size 64 K × 4 that can be connected to this microprocessor? (DRDO- CSE)
(a) 8 (b) 16 (c) 24 (d) 32

18. Static RAM (DRDO- CSE)
(a) is a volatile memory
(b) is a non-volatile memory
(c) needs refreshing to retain the value
(d) contains static information, i.e., cannot be modified

19. Pick up the correct pair in which the first element refers to the addressing modes with minimum operand fetching time and the second one refers to the addressing modes with maximum operand fetching time. (DRDO-CSE)
(a) Register direct and memory indirect.
(b) Register direct and indexed indirect.
(c) Immediate and indexed indirect.
(d) Immediate and indexed.

20. While an instruction is executed, the Program Counter (PC) should contain the address of (DRDO-CSE)
(a) the current instruction (b) the next sequential instruction
(c) the operand (d) the previous instruction

21. A memory system of size 16 K bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. Then the number of such chips required to design the memory system is (ISRO)
(a) 2 (b) 4 (c) 8 (d) 16

22. Number of address lines required to address 8 k bytes of memory is (JTO)
(a) 13 (b) 14 (c) 15 (d) 16

KEY

1. A 2. B 3. B 4. B 5. A 6. C 7. D 8. A 9. C 10. B 11. B

12. A 13. A 14. B 15. D 16. B 17. D 18. A 19. A 20. B 21. C 22. A

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