EE Dept, IIT Bombay
Academic Year: 2024-2025, Semester II (Spring)

Course: MS101 Makerspace
EE Lecture 10

Transistors

Topics: (1) Transistor Basics, (2) BJT, (3) MOSFET, (4) Switches Using Transistors, (5) Logic Gates Using MOSFETs.

Reference: AS Sedra, KC Smith, TC Carusone, & V Gaudet, Microelectronic Circuits, 8th ed., Oxford University Press, 2020. Chs. 1, 2, 11, 13, 15.

1. Transistor Basics

Transistor

A transistor is a semiconductor device with three terminals, used in analog & digital applications.

It is mostly used as a ‘two-port device’ with one terminal common between the input and output ports.

Commonly used transistors

- Bipolar Junction Transistor (BJT)
- Metal Oxide Field Effect Transistor (MOSFET)

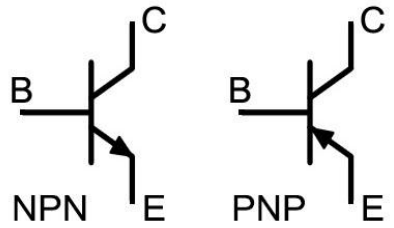
Both types are available as discrete devices and are used in analog and digital ICs.

Bipolar Junction Transistor (BJT): symbol & model

Types: NPN, PNP

Terminals: Emitter (E), Base (B), Collector (C)

Circuit symbol

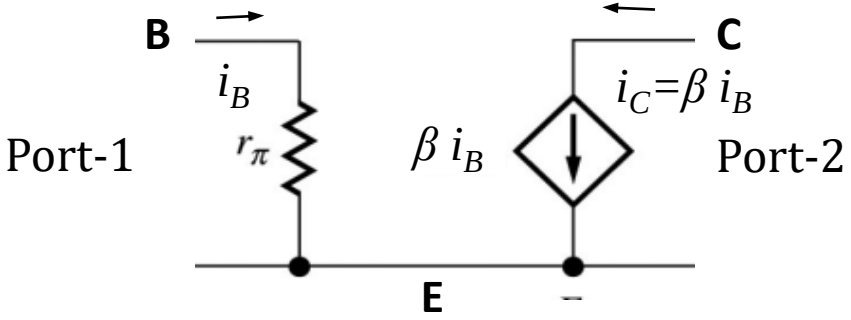


Two-port configurations with one terminal common between the input & output ports

- Common emitter (CE)
- Common base (CB)
- Common collector (CC)

Simplified small-signal model for CE configuration
(current-controlled current source)

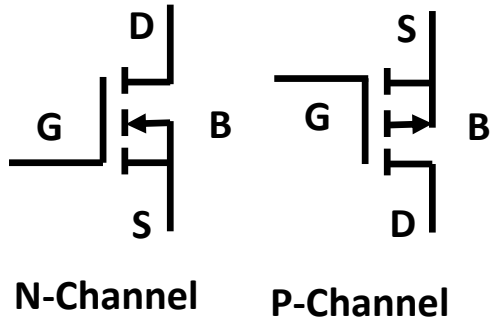
- Input: base current i_B
- Output: collector current $i_C = \beta i_B$
- β: Current gain



Metal Oxide Field Effect Transistor (MOSFET): symbol & model

Types
- N-channel enhancement mode
- P-channel enhancement mode
- N-channel depletion mode
- P-channel depletion mode

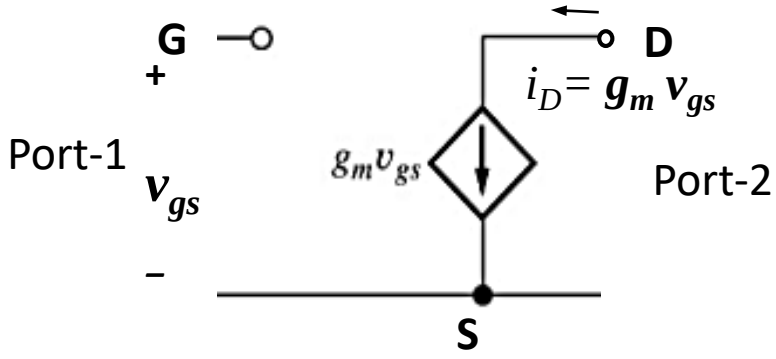
Circuit symbol (enhancement mode) with B-S shorted



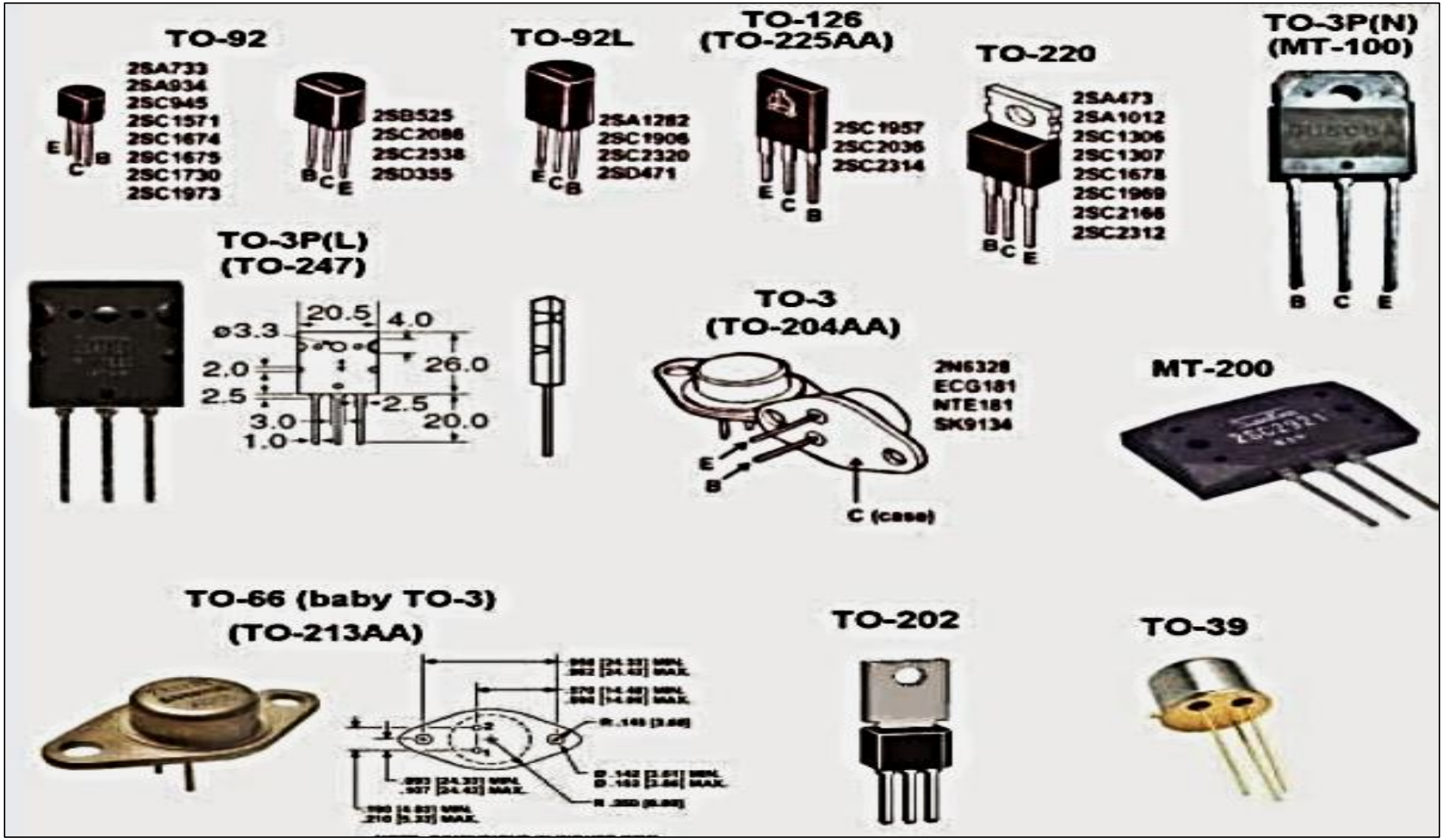
Terminals: Source (S), Gate (G), Drain (D), Substrate / Body (B)

Two-port configurations with one terminal common between the input & output ports
- Common source (CS)
- Common gate (CG)
- Common drain (CD)

Simplified small-signal model for CS configuration
(voltage-controlled current source)
- Input: gate-source voltage v_{GS}
- Output: drain current $i_D = g_m v_{GS}$
- g_m: trans-conductance
- $i_G \approx 0 \Rightarrow$ Almost no power from the input source.



Some commercially available discrete transistor packages



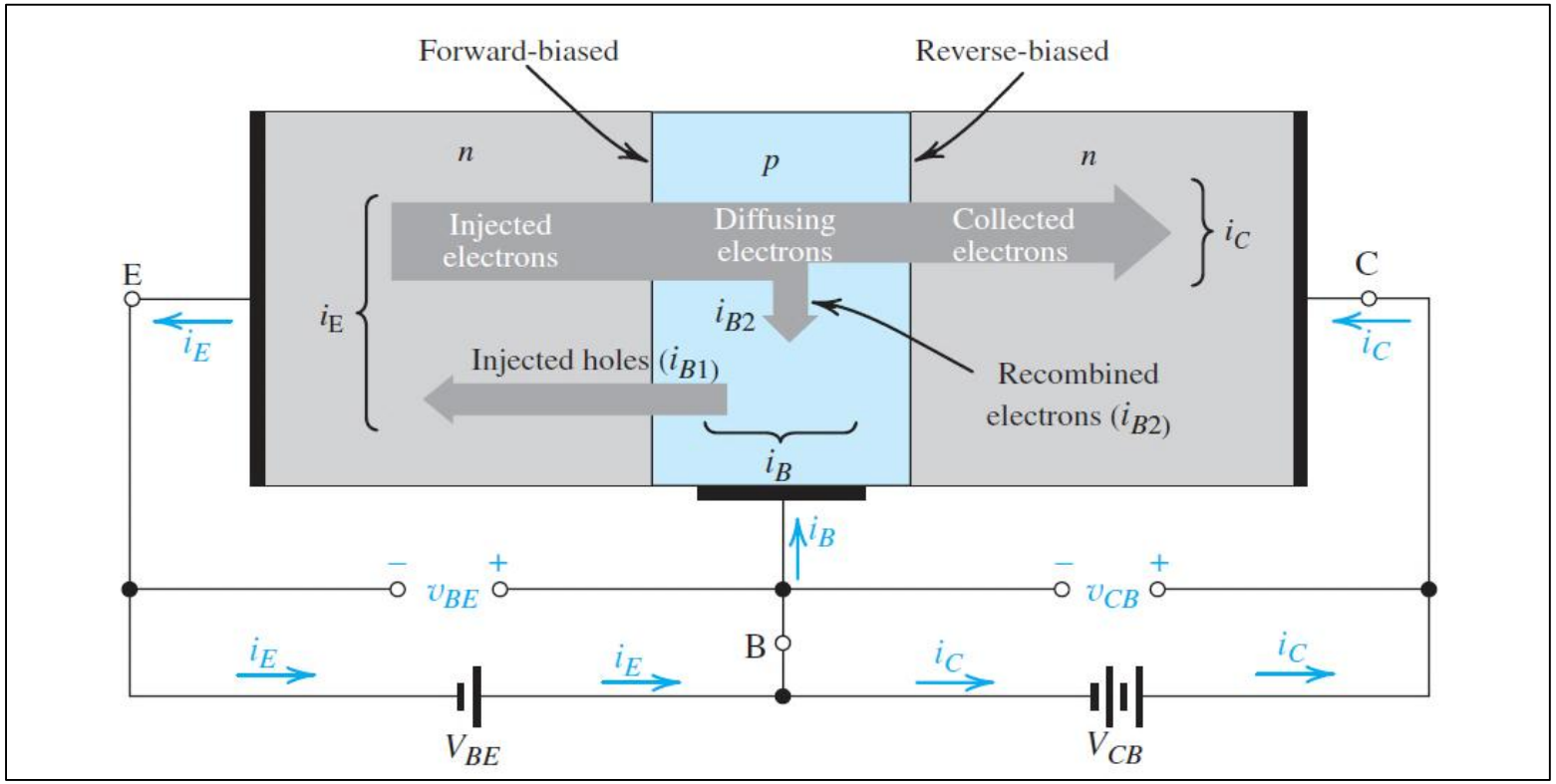
2. Bipolar Junction Transistor (BJT)

NPN transistor

Emitter (E): heavily doped N region

Base (B) : very thin P region

Collector (C): lightly doped N region



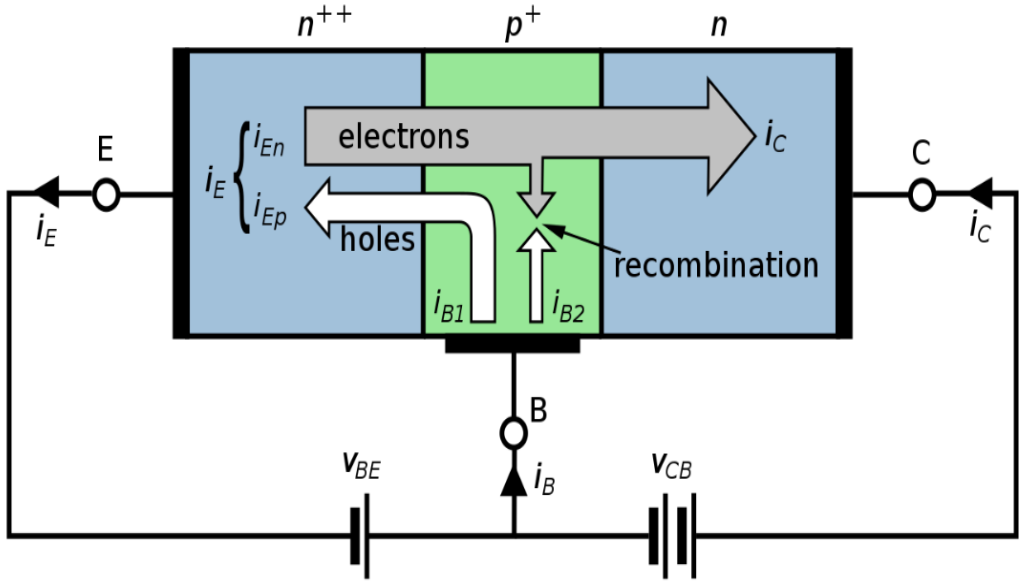
Active mode operation

- BE junction is forward biased.
- BC junction is reversed biased.

Source: Fig 6.3:-Sedra A S, Smith K C, "Microelectronic Circuits", Oxford University Press, 7Ed. ISBN: 9780199339136

Active mode operation: a cricket analogy

- The emitter is the bowler who shoots balls (electrons) toward the base.
- The base is the batsman, a tail-ender who swings away but connects with only 1-2% of the incoming balls (electrons).
- Most of the balls (electrons) are collected by the wicketkeeper (collector).



Current relations

KCL: $I_E = I_B + I_C$

Transistor action

$\Delta I_C = \alpha \Delta I_E \quad (\alpha \approx 0.90 - 0.99)$

$\Delta I_C = \beta \Delta I_B$

$I_C = \beta I_B$ is used as an approximate relation.

Relation between α & β

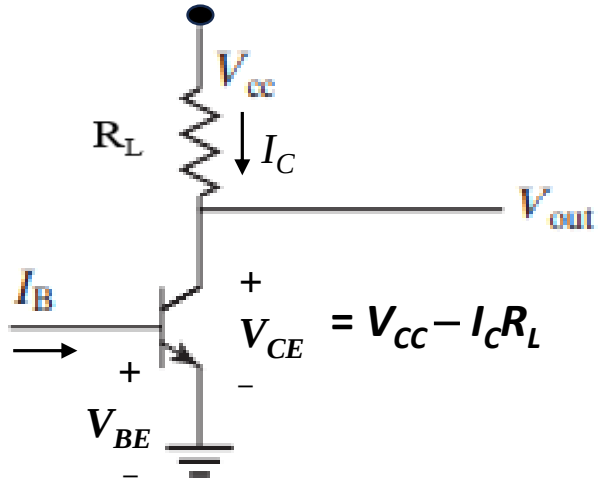
$\Delta I_E = \Delta I_B + \Delta I_C \Rightarrow \Delta I_B = \Delta I_E - \Delta I_C = (1/\alpha - 1)\, \Delta I_C$

$\Rightarrow \Delta I_C = \alpha/(1-\alpha)\, \Delta I_B = \beta\, \Delta I_B$

$\Rightarrow \beta = \alpha/(1-\alpha)$

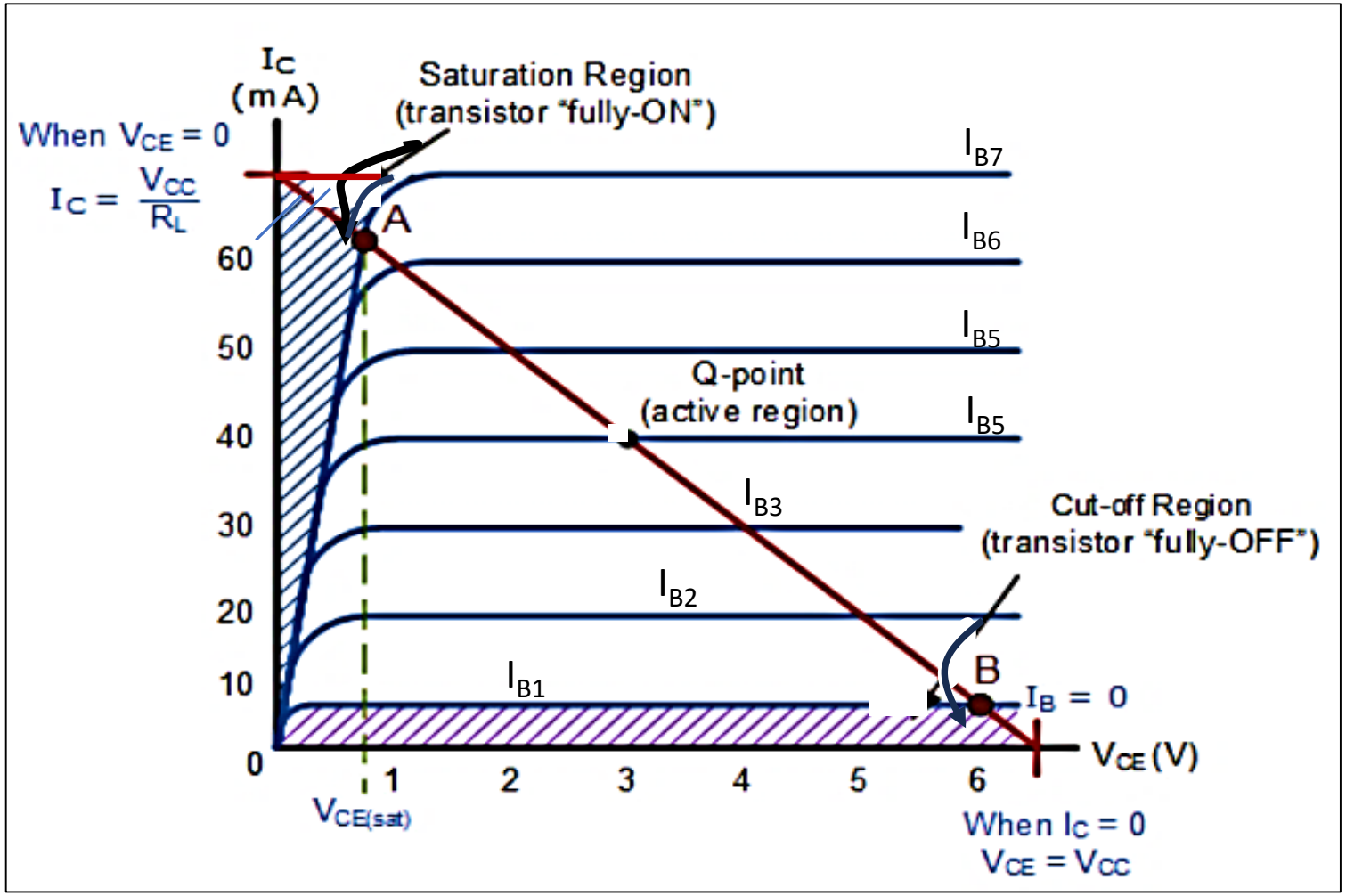
Example: $\alpha = 0.98 \Rightarrow \beta = 0.98/0.02 = 49$

NPN transistor characteristics: I_C vs V_{CE}



Operation states

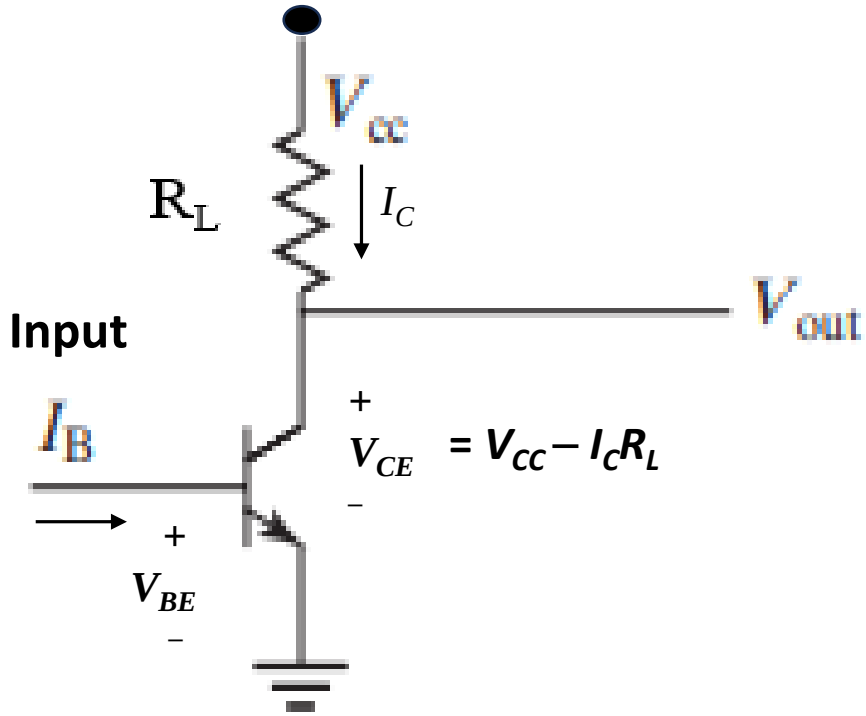
- Active: Forward biased BE junction, reverse biased BC junction.
- ON (saturation): Forward biased BE & BC junctions. High I_B, High I_C, Low V_{CE}.
- OFF (cutoff): Reverse biased BE & BC junctions. $I_B \approx 0$, $I_C \approx 0$, High V_{CE}.



Typical 'V_{CE} - I_C' characteristics ($I_{B1} < I_{B2} < I_{B3} < I_{B4} < I_{B5} < I_{B6} < I_{B7}$).
Operating points for switching action: A (on) & B (off).

NPN transistor as a switch

Common emitter (CE) configuration
- Control input on the base side
- Load on the collector side
- ON / OFF control by changing the base current I_B



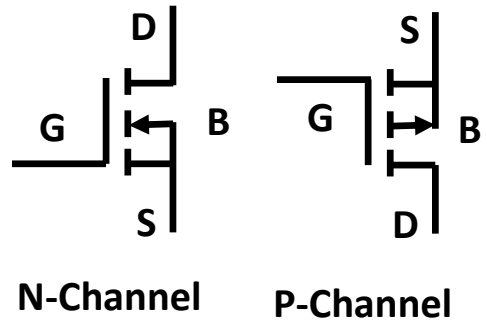
OFF: $V_{BE} < V_\gamma$
BE junction cutin voltage: $V_\gamma \approx 0.5$ V
$I_B \approx 0.\ I_C \approx 0.\ V_{CE} \approx V_{CC}$
$V_{BC} < 0$

Heavily ON: $I_B > I_C/\beta$
$V_{BE} = V_{BES}, V_{CE} = V_{CES}$
Saturation voltages: $V_{BES} \approx 0.8$ V, $V_{CES} \approx 0.2$ V)
$I_C = (V_{CC} - V_{CES})/R_L$
$V_{BC} > 0$

3. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Types
- N-channel enhancement-mode
- P-channel enhancement-mode
- N-channel depletion-mode
- P-channel depletion-mode

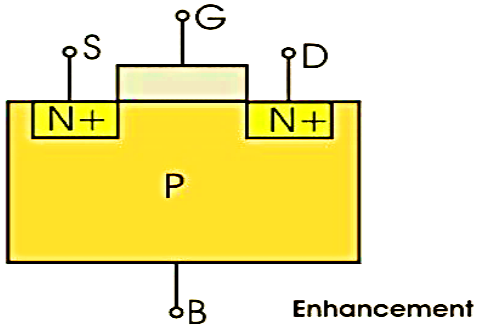
Enhancement-mode device symbols
(B-S usually shorted in switching & logic circuits)



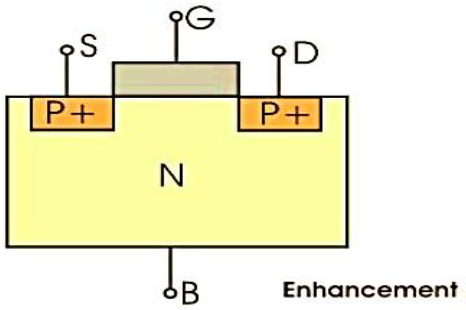
Terminals: Source (S), Gate (G), Drain (D), Substrate / Body (B)

Commonly used MOSFETs: N-channel & P-channel enhancement-mode

N-channel enhancement-mode MOSFET

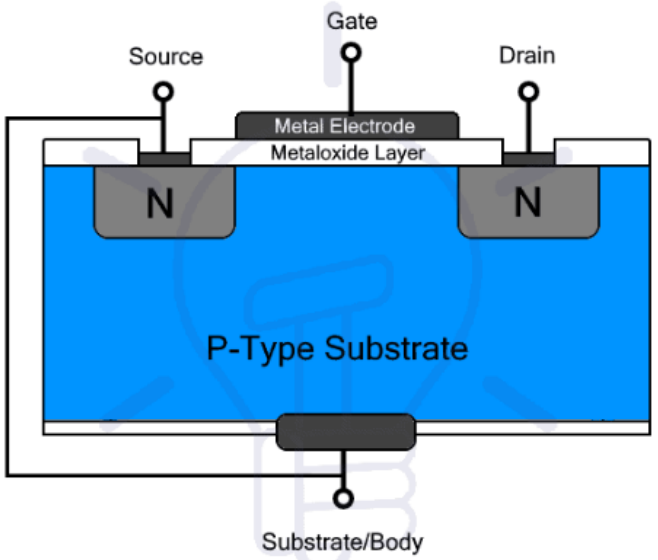


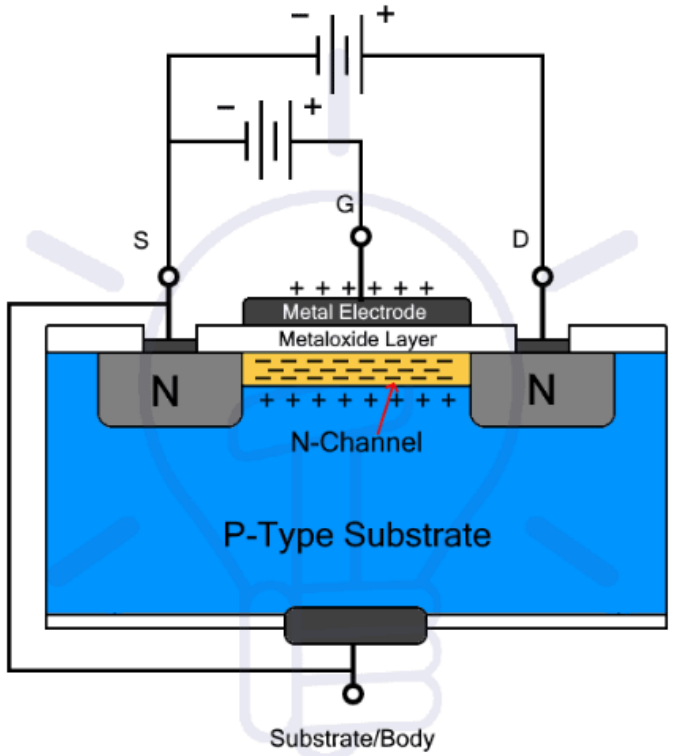
P-channel enhancement-mode MOSFET



Operation: Voltage-controlled current source device. Gate-source voltage (V_{GS}) controls drain current (I_D).
Nearly zero gate current (I_G) $\Rightarrow$ Almost no power taken from the input source.

N-channel enhancement-mode MOSFET operation

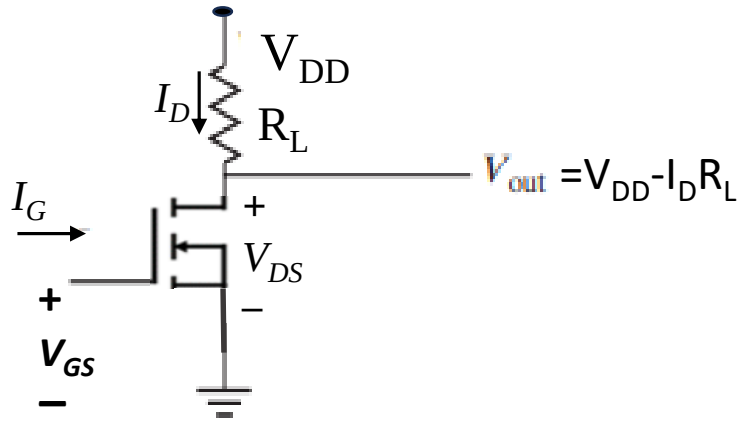




- The D & S terminals are interchangeable, with $V_{DS} > 0$.
- No D-S channel is available at $V_{GS} = 0$.
- For N-channel, the D-S channel is formed for $V_{GS} > V_T$ (threshold voltage >0)
- OFF-state: $V_{GS} < V_T$. Very high resistance for drain-source current flow.
- ON-state: $V_{GS} > V_T$ +a few V. Low resistance for drain-source current flow.

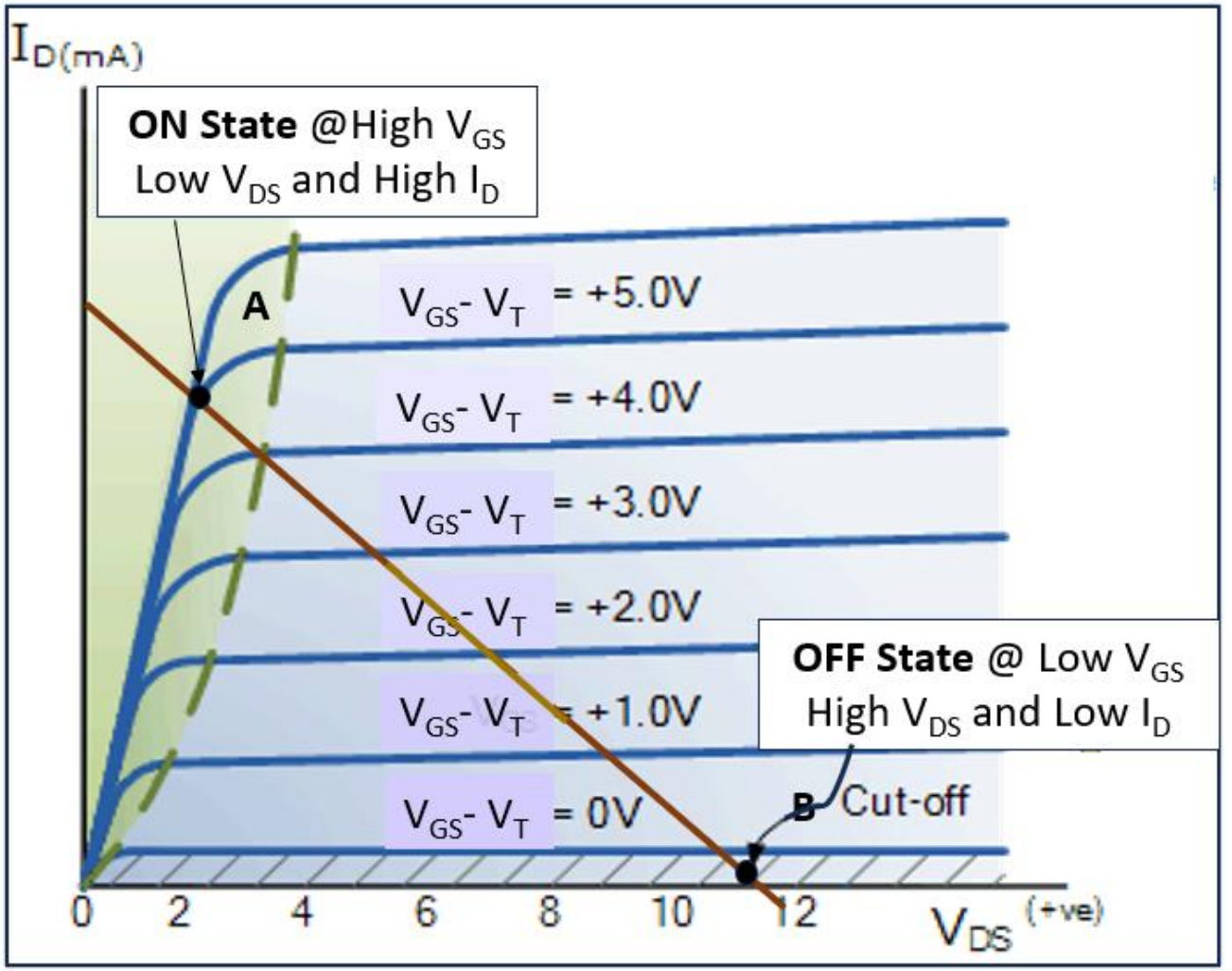
MOSFET Type	Condition for Switching
N-channel Enhancement	OFF for $V_{GS} < V_T$ (0.6 to 1 V)
P-channel Enhancement	OFF for $V_{GS} > V_T$ (−1.0 to 0.6 V)

N-channel enhancement-mode MOSFET characteristics: I_D vs V_{DS}



- $V_{DS} > 0$. D-S conduction starts when the N-channel is formed between the D & S terminals.
- V_T is the minimum value of V_{GS} for the channel formation. Channel is formed for $V_{GS} > V_T$. Channel resistance decreases as V_{GS} increases further.
- OFF state: $V_{GS} < V_T$. $I_G \approx 0$. $I_D \approx 0$. $V_{DS} \approx V_{DD}$
- ON state: $V_{GS} > V_T$ + a few V

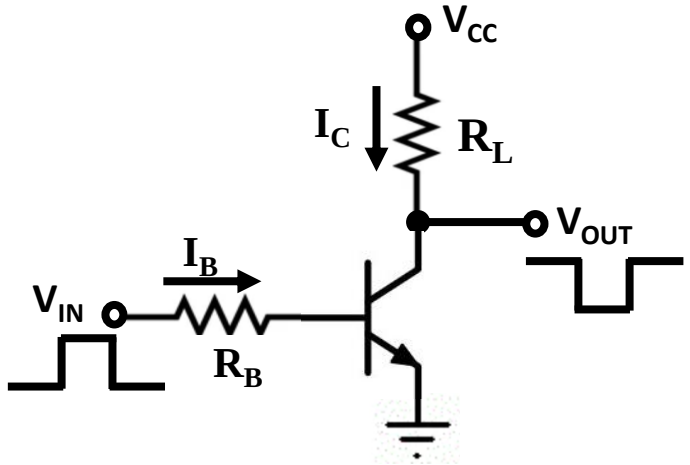
$$I_G \approx 0.\ V_{DS} \approx 0.\ I_D \approx V_{DD} / R_L$$



Typical 'V_{DS}-I_D' characteristics for N channel Enhancement mode MOSFET
A & B: operating points for switching action

4. Switches Using Transistors

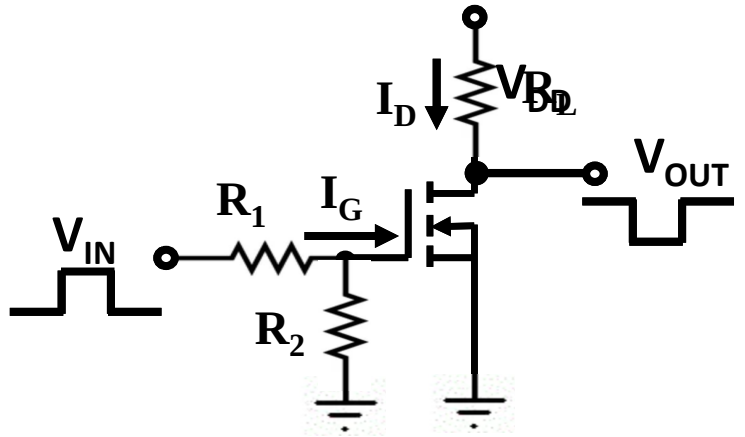
BJT switch with Vin as control



BJT switch for load R_L connected to +ve supply end (V_{CC})

- Control input V_{in}
- NPN BJT in common-emitter (CE) configuration
- R_B for limiting I_B
- OFF: $I_B \approx 0$ (V_{in} = low)
- ON: $I_B > I_C/\beta$ (V_{in} = high)

MOSFET switch with Vin as control

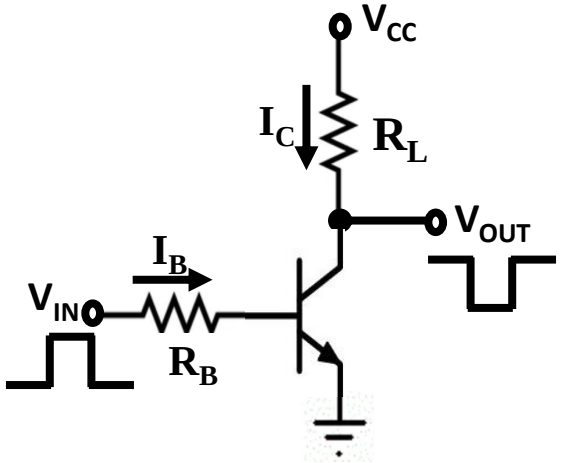


MOSFET switch for load connected to +ve supply end (V_{DD})

- Control input V_{in}
- N-channel MOSFET in common-source (CS) configuration
- R_1 and R_2 for voltage attenuation, if V_{in}-peak is large
- OFF: $V_{GS} < V_T$ (V_{in} = low)
- ON: $V_{GS} > V_T$ + a few V (V_{in} = high)

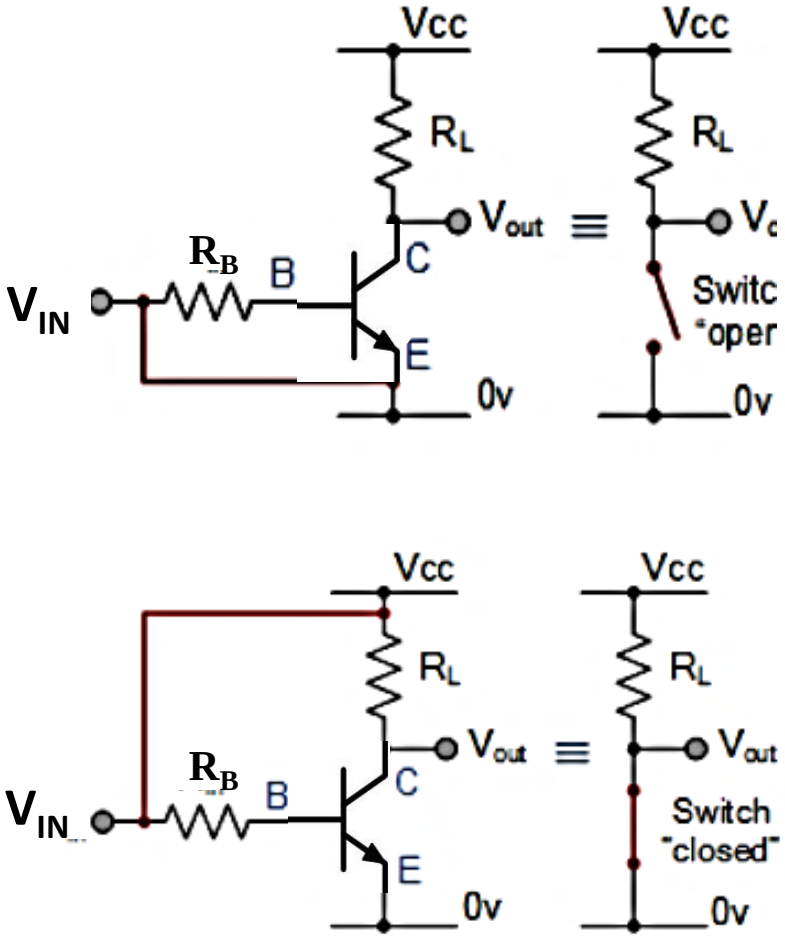
For load R_L connected to –ve supply end, we use PNP BJT in CE configuration or P-channel MOSFET in CS configuration.

NPN BJT Switch Operation



NPN BJT switch

Control input Vin, with binary levels 0 & V_{CC}



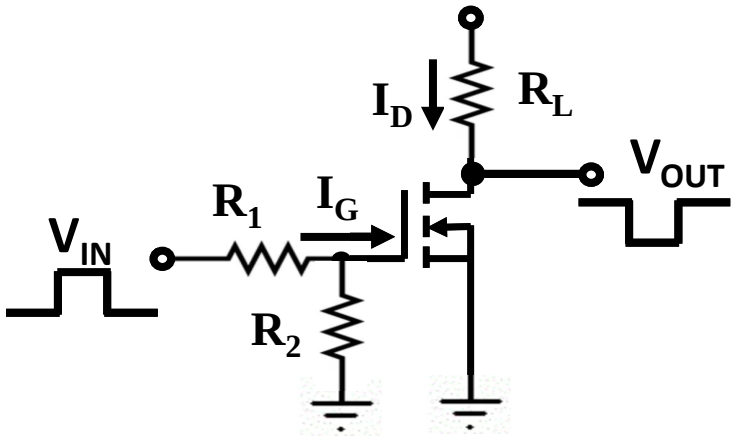
(a) $V_{IN} = 0$

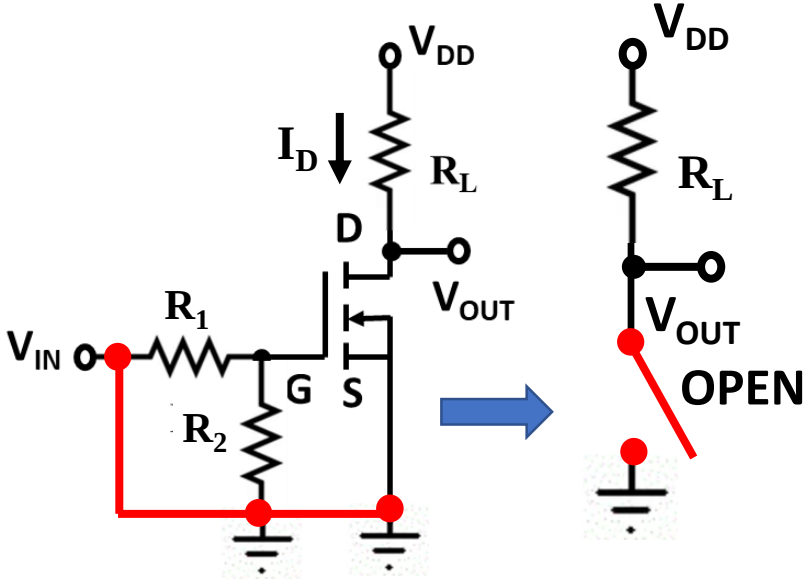
- $V_{BE} = 0 < 0.5$ V.
- BJT operates as open switch.
  $I_B \approx 0$. $V_{CE} \approx V_{CC}$. $I_C \approx 0$.
- BE junction is not forward biased.
- BC junction is reverse biased.

(b) $V_{IN} = V_{CC}$

- BE junction is forward biased. I_B is limited by R_B. V_{BE} reaches saturation value V_{BES} (≈ 0.8 V).
- Collector voltage drops until BC junction gets forward biased. V_{CE} reaches saturation value V_{CES} (≈ 0.2 V).
- BJT operates as closed switch.
- $V_{BE} = 0.8$ V. $V_{out} = V_{CES} = 0.2$ V.
  $I_B = (V_{CC} - 0.8) / R_B$.
  $I_C = (V_{CC} - V_{CES}) / R_L$.

N-channel MOSFET Switch Operation





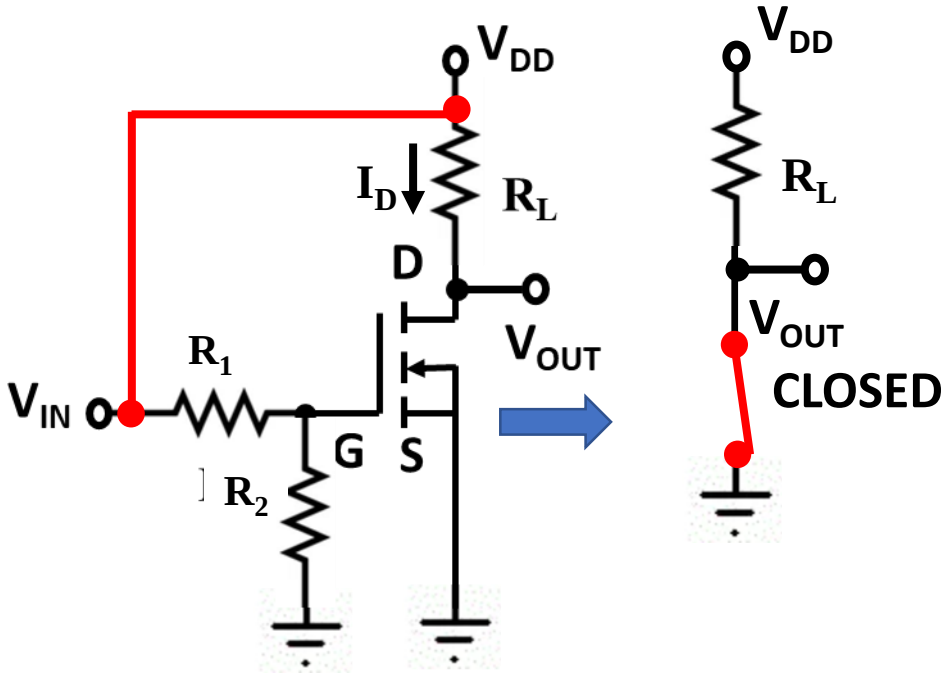
Let $V_{DD} = 12$ V, $V_T = 2$ V, $R_1 = 0$, $R_2 = \infty$.

(a) $V_{in} = 0$
- $V_{GS} = 0 < V_T$.
- MOSFET operates as open switch.

$I_G \approx 0$
$V_{DS} \approx V_{DD}$
$I_D \approx 0$.

N-channel MOSFET switch

Control input V_{IN}, with binary levels 0 & V_{DD}. Usually R_1 is short and R_2 is open.

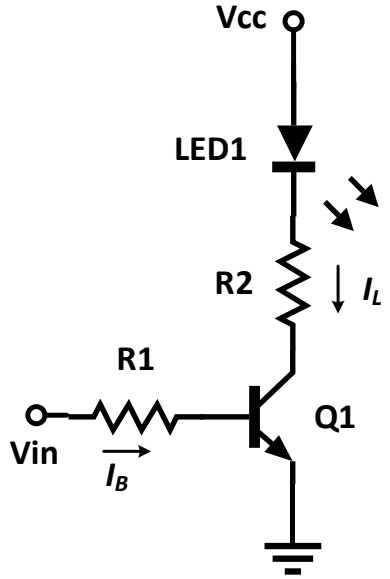


(b) $V_{in} = V_{DD}$
- $V_{GS} = 12$ V $> V_T$.
- MOSFET operates as closed switch.

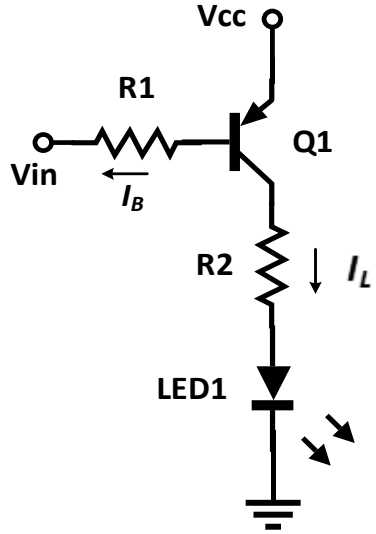
$I_G \approx 0$
$V_{DS} \approx 0$
$I_D = V_{DD}/R_L$

NPN and PNP BJT Switches for LED Control

NPN switch for load connected to +ve supply end (Vcc)



PNP switch for load connected to –ve supply end (GND)



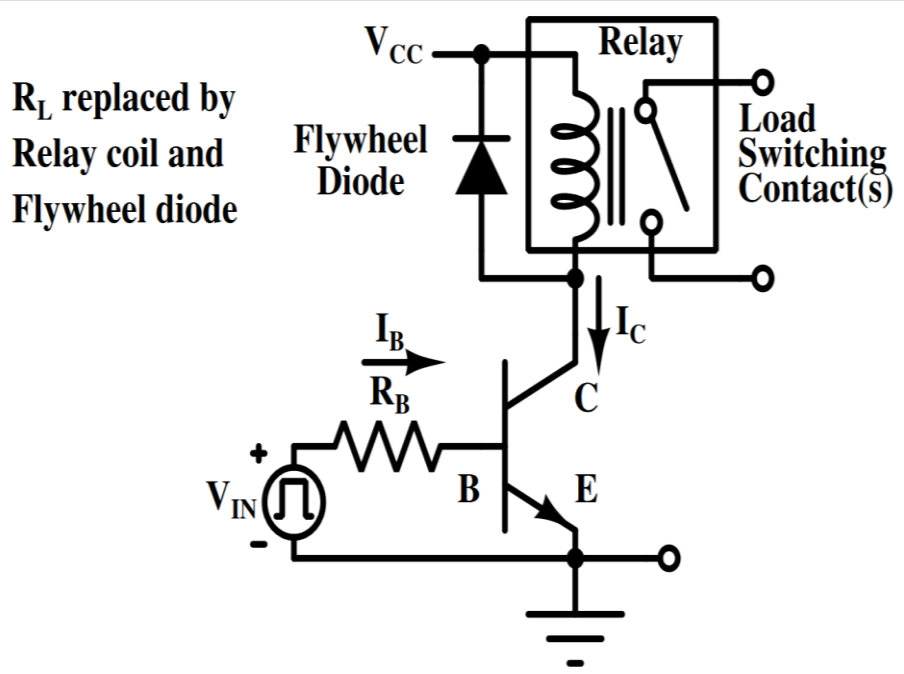
Given: $V_{cc} = 5$ V. V_{in} (LED off) = 0 V. V_{in} (LED on) = 5 V.
$\beta > 50$. I_L (full brightness) = 10 mA. LED voltage drop = 2 V.

$I_L = (V_{CC} - V_{LED} - V_{CES})/R_2 = (5-2-0.2)/R_2 > 10$ mA
$\Rightarrow R_2 < 2.8/10\ \text{k}\Omega = 280\ \Omega$.
Let $R_2 = 270\ \Omega$. $\Rightarrow I_L = 10.3$ mA.
$I_B = [(V_{in})_{\text{high}} - V_{BES} - 0]/R_1 > I_L/\beta_{\min}$
$\Rightarrow (5-0.8-0)/R_1 > 10.3/50 \Rightarrow R_1 < 20.38\ \text{k}\Omega$.
Let $R_1 = 18\ \text{k}\Omega$.

Given: $V_{cc} = 5$ V. V_{in} (LED off) = 5 V. V_{in} (LED on) = 0 V.
$\beta > 50$. I_L (full brightness) = 10 mA. LED voltage drop = 2 V.

$I_L = [V_{CC} - V_{ECS} - V_{LED}]/R_2 = [5 - 0.2 - 2]/R_2 > 10$ mA
$\Rightarrow R_2 < 2.8/10\ \text{k}\Omega = 280\ \Omega$.
Let $R_2 = 270\ \Omega$, $\Rightarrow I_L = 10.3$ mA.
$I_B = [V_{CC} - V_{EBS} - (V_{in})_{\text{low}}]/R_1 > I_L/\beta_{\min}$
$\Rightarrow (5 - 0.8 - 0)/R_1 > 10.3/50 \Rightarrow R_1 < 20.38\ \text{k}\Omega$.
Let $R_1 = 18\ \text{k}\Omega$.

BJT Switch for Electromagentic Relay Control

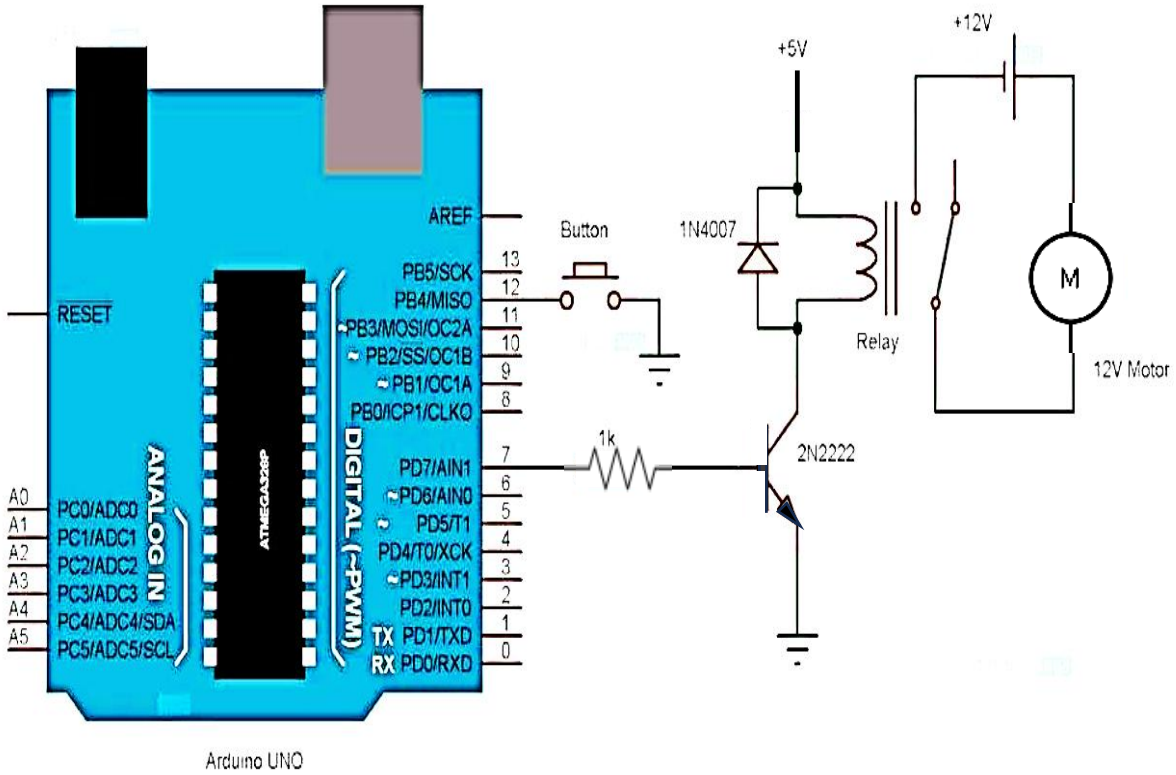


Relay Symbols

- Relay is used for switching loads with large voltage & current and for electrical isolation of the control circuit from the load voltage.
- The relay coil has a resistance and an inductance. It is activated if the coil current is above a certain threshold.
- Turning off the coil current generates a large voltage at its lower end (i.e. collector terminal). To protect the transistor from high VCE, "flywheel diode" is used. When the transistor is turned off, the diode turns on, limiting V_{CE} to $V_{CC} + V_D$. The coil current slowly decays to zero.

- NPN transistor for relay connected to +ve supply.
- The relay coil current (I_C) is switched by controlling the transistor base current (I_B). Transistor current Gain $\beta = I_C / I_B$.
- Load switching contacts of the relay switch the load with large voltage & current.
- The relay control circuit is electrically isolated from the load.

Relay Switching Using Micro-Controller (Arduino)



Arduino Relay Control Circuit Diagram

Example
Control of a relay with 'Arduino' digital output pin PD7 and NPN transistor 2N2222.

Relay coil current = 60 mA.
Transistor $\beta_{min} = 30$.

Set the pin PD7 to 'Hi'. It will put the transistor in ON state, allowing current to flow through the relay coil making the relay ON.
$I_B >$ Relay current / $\beta_{min} = 2$ mA.

Diode is connected in parallel with the relay coil to avoid sudden change of current in it and thereby to avoid large voltage at the transistor's collector terminal.

Source: https://www.electronicshub.org/arduino-relay-control/

5. Logic Gates Using MOSFETs

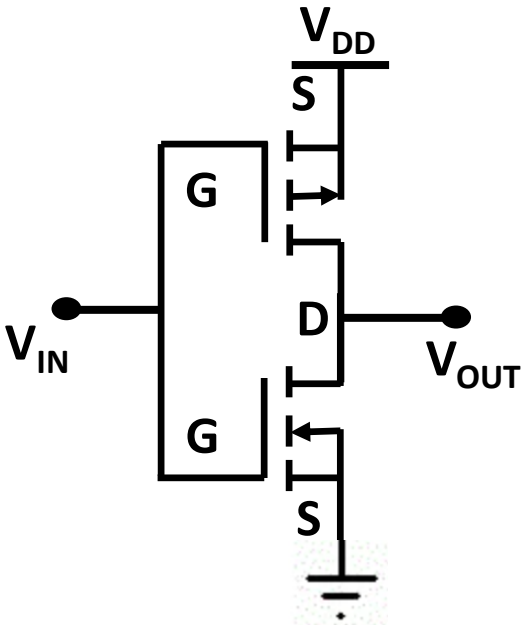
Complementary Metal Oxide Semiconductor (CMOS) Circuits

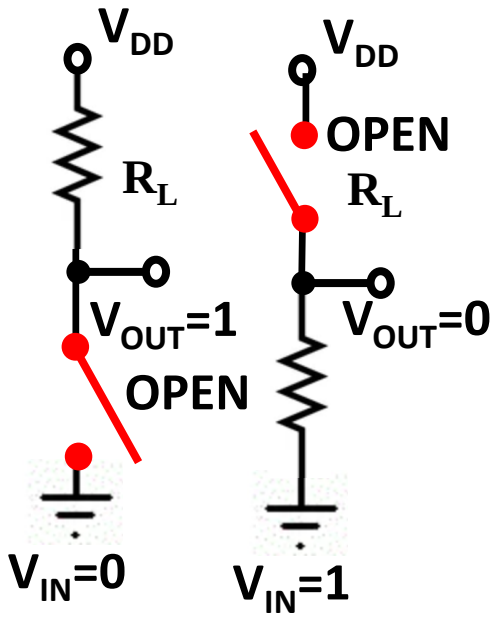
1. Combination of N-channel and P-channel MOSFETs
2. Usually same gate signal goes to N-channel and its complementary P-channel transistors for logic circuits
3. Negligible steady-state power consumption in CMOS digital circuits

Some CMOS Logic Gates

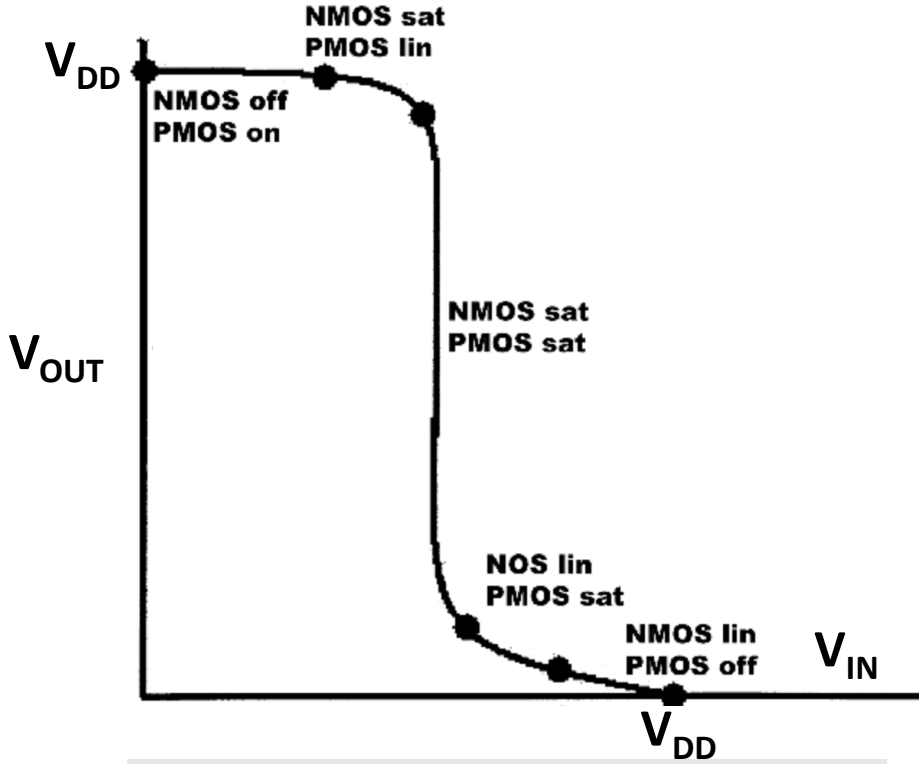
- CMOS Inverter
- CMOS NAND Gate – Universal gate
- CMOS NOR Gate – Universal Gate
- CMOS Tri-state Inverter

CMOS Inverter



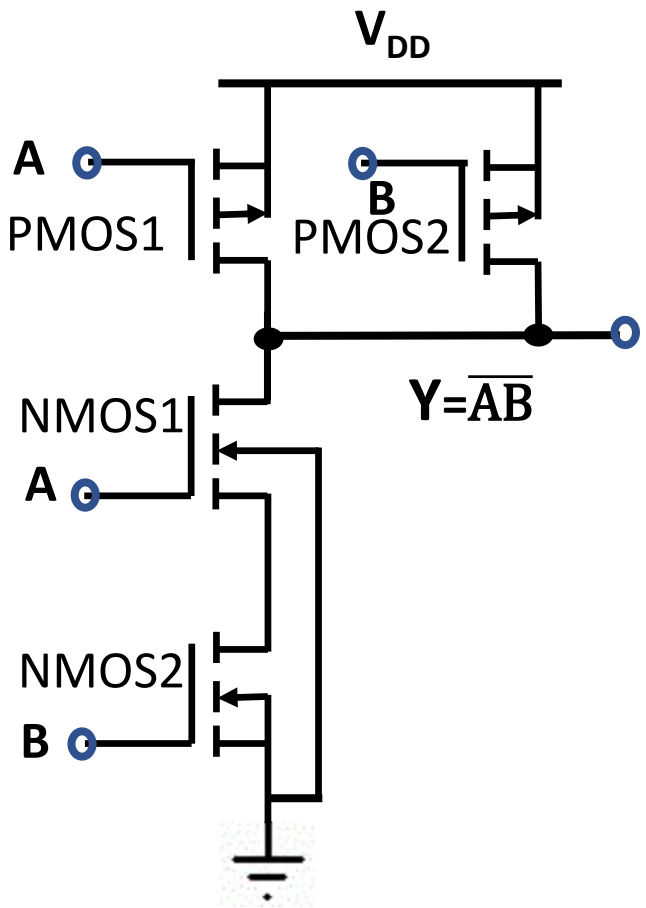


Ideal Digital Operation



Practical Inverter Characteristics

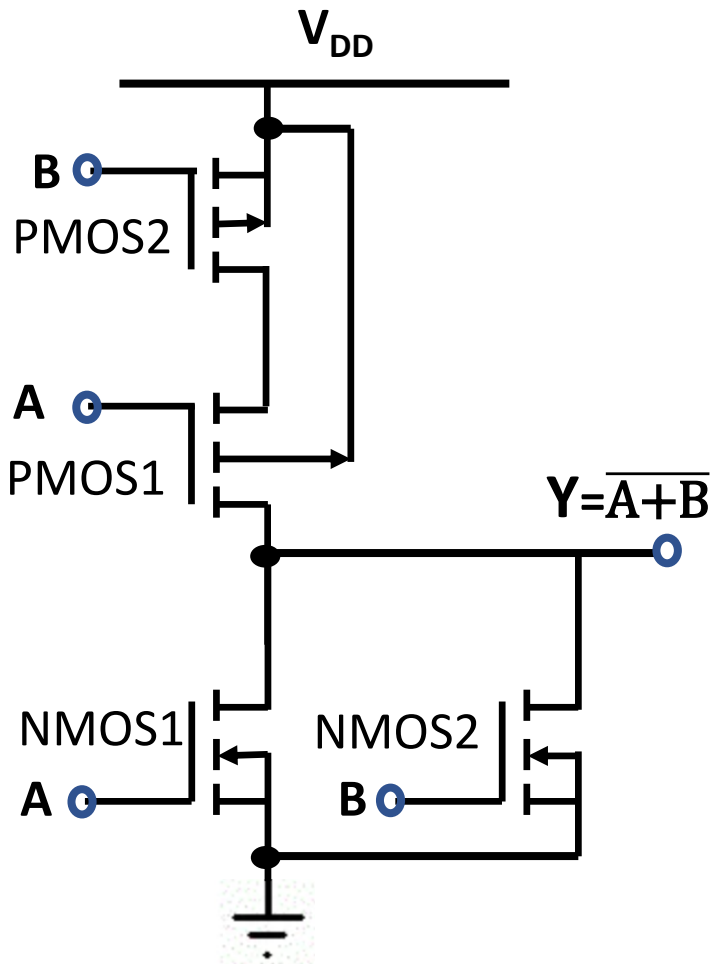
CMOS 2-Input NAND Gate



TRUTH TABLE **STATE OF THE TRANSISTORS**

A	B	Y	NMOS1	PMOS1	NMOS2	PMOS2
0	0	1	OFF	ON	OFF	ON
0	1	1	OFF	ON	ON	OFF
1	0	1	ON	OFF	OFF	ON
1	1	0	ON	OFF	ON	OFF

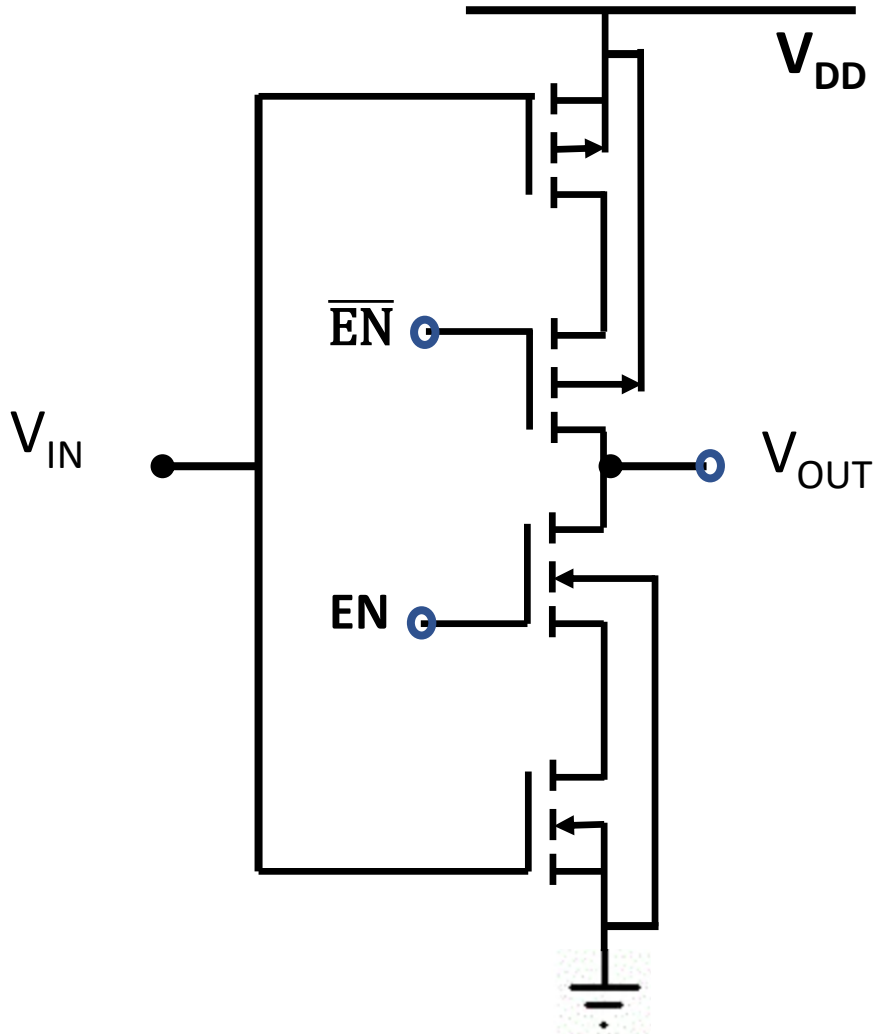
CMOS 2-Input NOR GATE



TRUTH TABLE **STATE OF THE TRANSISTORS**

A	B	Y	NMOS1	PMOS1	NMOS2	PMOS2
0	0	1	OFF	ON	OFF	ON
0	1	0	OFF	ON	ON	OFF
1	0	0	ON	OFF	OFF	ON
1	1	0	ON	OFF	ON	OFF

CMOS Tri-state Inverter



- When EN=1, $V_{OUT} = \overline{V_{IN}}$
- When EN=0, V_{OUT} is in the high impedance state

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