SHISHU Assigment 5 REG : 2020CA089

Q1. A CPU generates 32-bit virtual - - - of 128 page - - - - - - Find the minimum size of the TLB tag?

virtual memory would not be very effective if every memory address had to be translated by looking up the associated physical page in memory. The Solution is to catch cache the recent translations in a Translation Lookaside Buffer (TLB).

size of a page = 4KB = 2^12 means 12 offset bits CPU generated 32-bit virtual address.

Total number of bits needed to address a page frame = 32 - 12 = 20

If there are 'n' cache lines in a set, the cache placement is called n-way set accociative. Since TLB is 4 way set associative and can hold total 128 (2^7) page table entries, no. of sets in cache = 2^7 / 4 = 2^5.

So, 5 bits are needed to address a set, and 15 (20-5) bits are needed for tag.

Q2 A computer uses 46-bit virtual address, 32-bit - - - - - - - - - . Each entry of T3 stores - - - - - - - . The processor used - - - - - 64 bytes. what is the minimum - - - sets in the processor cache of this computer.

Sol 1 MB 16-way set associative virtually indexed physically tagged Cache (VIPT).

The cache block size is 64 bytes.

No of blocks in 2^20/2^6 = 2^14.

No of sets is 2^14 /2^4 = 2^10.

VA (46)

tag(30), set(10), block offset(6)

In VIPT if the no. of bits of page offset = (set+ block offset) then only one page color sufficient. but we need 8 colors because the number bits where the cache set over lap index and physical page number is required. is 3 so 2^3(8)page color

Q3 A processor uses 36-bit physical addresses and 32 bit virtual addresses, with a page ―― - - - - - where the virtual address is used as follow:.

- - - -
- - -
- - -
-

The number of bits- - - - -, level page tables are respectively.

At first we have physical address of 2^36, and page size is 2^12. Hence 2^24 should be the number of pages. and you figured that right.

Since given 9 bits for 3rd level page table, i.e 2^9 and then 4 bytes per entry ; so 2^11 . Now 2^36/2^11 would given 2^25, Hence 25 bit (25 bit at second level table).

Now again given 9 bits for second level page table, so the same logic applies again. 2^36 / 2^11. Which agin is 2^25. (25 bits at fist lavel table).

hence the answer must be 25, 25, 24.

Q4 The memory access time is 1 nanosecond - - - - . What is the avg memory access time in executing the sequence of instructions?

Sol

Read Operation :

$T_1 = 1\ ns$, $T_2 = 5\ ns$ and $H_1 = 0.9$

Read instructions = 100 + 60 = 160

Write operation

$T_1 = 2ns$, $T_2 = 10\ ns$ and $H_1 = 0.9$

Write instructions = 40

Formula

$T_{avg} = H_1 T_1 + (1 - H_1) T_2$

Calculation

Read operation :

$T_{avg} = 1 \times 0.9 + (1 - 0.9) \times 5$

$\therefore T_{avg} = 1.4$

Write Operation

$T_{avg} = 2 \times 0.9 + (1 - 0.9) \times 10$

$\therefore T_{avg} = 2.8\ ns$

Average access time $= \frac{1.4 \times 160 + 2.8 \times 40}{160 + 40} = \frac{336}{200}$

$\therefore T_{avg} = 1.68$

Average access time $= \frac{360}{200} = 1.8$ ns

Q5

Sol

The possibilities are

TLB Hit * Cache Hit +

TLB Hit * Cache Miss +

TLB Miss * Cache Hit +

TLB Miss * Cache Miss

$= 0.96 * 0.9 * 2 + 0.96 * 0.1 * 12 + 0.04 * 0.9 * 22$
$+ 0.04 * 0.1 * 32$

$= 3.8$

approx ; 4