EE610A Analog VLSI Circuits
Project Report

Course: EE610A Analog VLSI Circuits

Project: Differential Amplifier Design

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1. Abstract

This report presents the design and simulation of a single-stage differential amplifier using a pMOS input stage for a non-inverting amplifier configuration. The goal was to achieve a loop gain ≥ 40 dB, bandwidth ≥ 25 MHz, and CMRR ≥ 80 dB using Cadence Virtuoso and 45nm GPDK. This report details the design approach, theoretical calculations, simulation results, and temperature performance from 0°C to 70°C.

2. Design Specifications

Parameter	Value
Input Stage	pMOS
VDD	1.8 V
Load Capacitance (CL)	20 pF
Minimum Loop Gain	40 dB
Minimum Bandwidth	25 MHz
Minimum CMRR	80 dB

3. Design Approach

3.1 Determining Transconductance (gm)

Using the unity-gain bandwidth relation:

f_unity = gm / (2π * CL)

Given:
- CL = 20 pF
- Required –3 dB bandwidth ≥ 25 MHz

We compute:
gm = 2π × 25 MHz × 20 pF ≈ 6.28 mS

Hence, **gm ≥ 6.28** mS is required for the input differential pair.

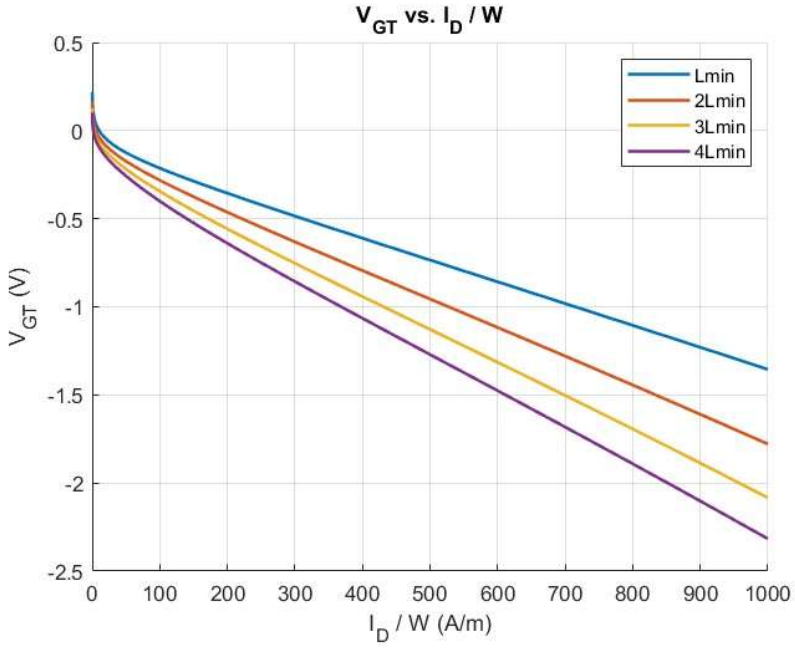
3.2 Using Lookup Tables for Parameter Selection

DC simulations were performed in Cadence ADE to extract gm, gds, ID, and V_GT. These were exported to CSV and plotted externally.

Graphs were analyzed to select points with high gm, good gm/gds (intrinsic gain), and moderate V_ov.

Graphs for PMOS were attached;

NMOS were evaluated



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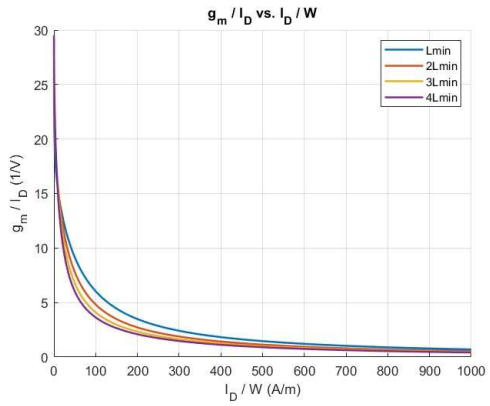
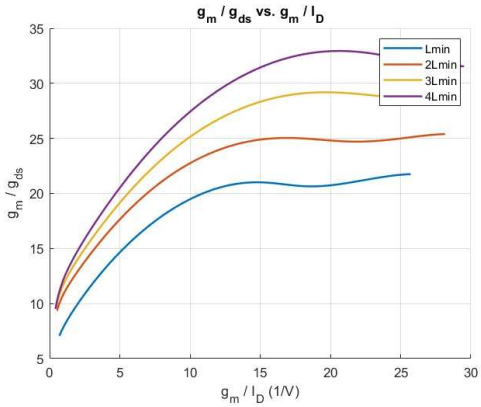
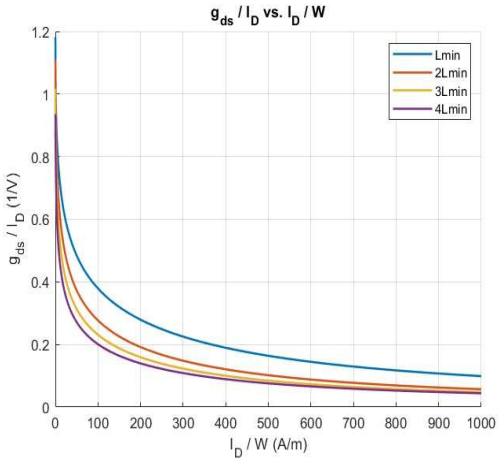
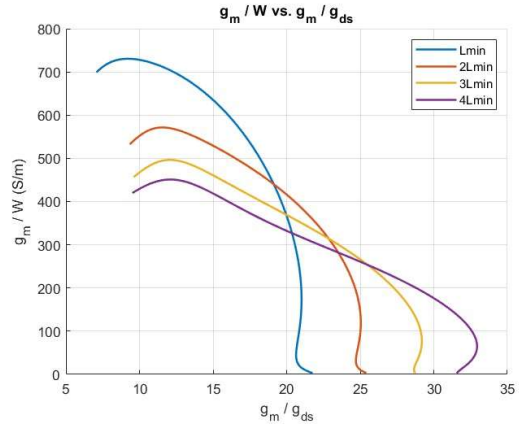
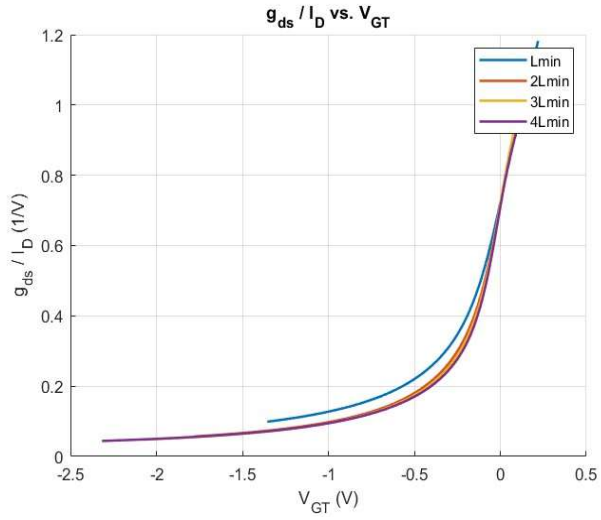










3.3 Loop Gain and Intrinsic Gain Requirement

In a negative feedback system:

Loop Gain = A_DM × β

For β = 0.5 and Loop Gain > 100:
A_DM > 200

A_DM = gm × (r_o1 || r_o2)
Assuming r_o1 = r_o2 ⇒ A_DM = gm × r_o / 2 ⇒ gm/gds > =400

This was infeasible with a basic differential pair. Thus, we chose a cascode configuration.

3.4 Cascode Configuration

For cascode:
A_DM ≈ gm × (gm × r_o)^2

Target: gm/gds ≥ 30, gm ≈ 8 mS

gm-ID plots helped determine ID, V_ov, and W/L ratios.
Bias voltages and gate voltages were set accordingly.

3.5 Biasing and Sizing Strategy

Using gm-ID and V_ov plots, we sized PMOS inputs for higher gm without increasing current. Biasing ensured cascode transistors remained in saturation.

3.6 Sizing of Other Transistors

Transistors PM4–PM7 (PMOS) and NM0–NM3 (NMOS) were sized using the required gm and ID from graphs.

3.7 CMRR Consideration

To achieve high CMRR:

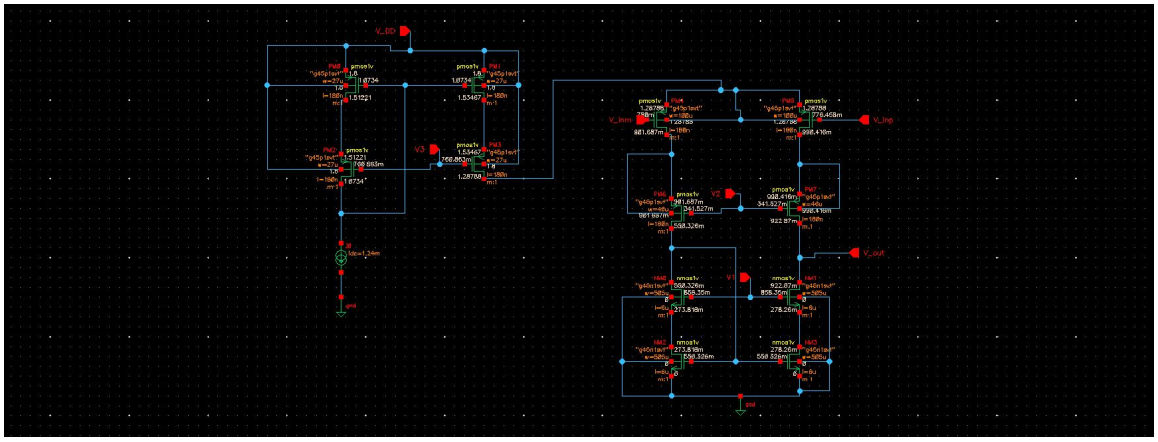
CMRR = A_DM / A_CM ≈ gm / gds

A_CM is approximately 1/(2*gmp*Rx) where Rx is output resistance of tail current source cascade configuration

Rx = gm * r01 * r02

Tail current source was cascoded. PM0–PM3 were sized carefully to maintain common-mode rejection and bias.

4. Schematic Diagram



5. Temperature Sweep Analysis

Temperature (° C)	Loop Gain (dB)	Bandwidth (MHz)	CMRR (dB)
0	42.382	29.75	90.4176
27	41.6892	27	88.6211
50	40.9641	25.8	86.5148
70	40.2076	24.49	84.33

6. DC Operating Point Results

Extracted from Cadence simulation (ADE → Results → Print → DC Operating Point):

Transistor	W/L (μm/μm)	gm (mS)	gds (μS)	Vov (V)	Cgs (fF)	Cgd (fF)
PM0	27 / 0.18	6.09	1.29m	-0.299	-53.7	-5.95
PM1	27 / 0.18	6.04	1.33m	-0.299	-53.69	-5.99
PM2	27 / 0.18	6.78	530.69	-0.288	-52.97	-5.45

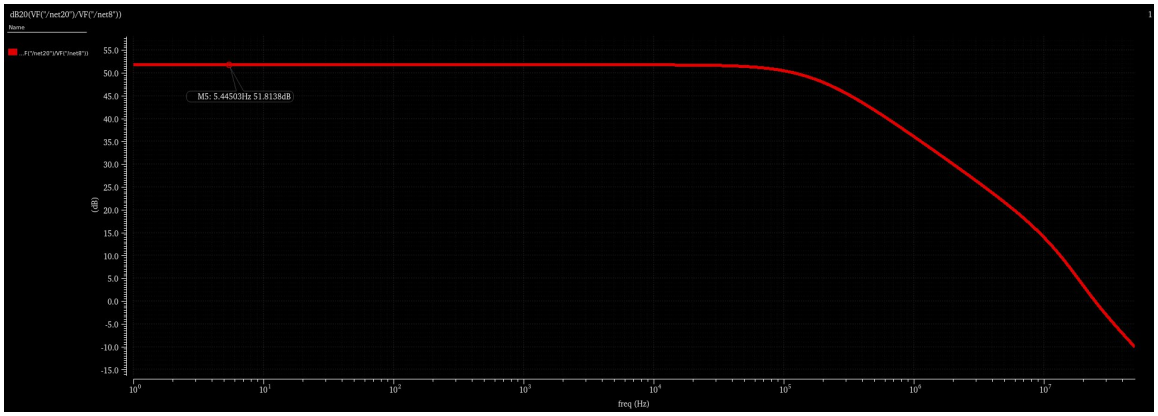
Transistor	W/L (µm/µm)	gm (mS)	gds (µS)	Vov (V)	Cgs (fF)	Cgd (fF)
PM3	27 / 0.18	6.54	700	-0.293	-53	-5.57
PM4	100 / 0.18	9.79	474.13	-0.088	-155	-20.37
PM5	100 / 0.18	9.79	473.33	-0.088	-155.184	-20.37
PM6	46 / 0.18	7.32	333.578	-0.135	-79.42	-9.2
PM7	46 / 0.18	7.32	329	-0.134	-79.38	-9.2
NM0	505 / 6	5.61	154.35	0.189	-28.81p	-720
NM1	505 / 6	5.61	162	0.189	-28.81p	-780
NM2	505 / 6	5.53	177.61	0.194	-29.53p	-795
NM3	505 / 6	5.53	177.82	0.194	-29.53p	-797

7. Simulation Results

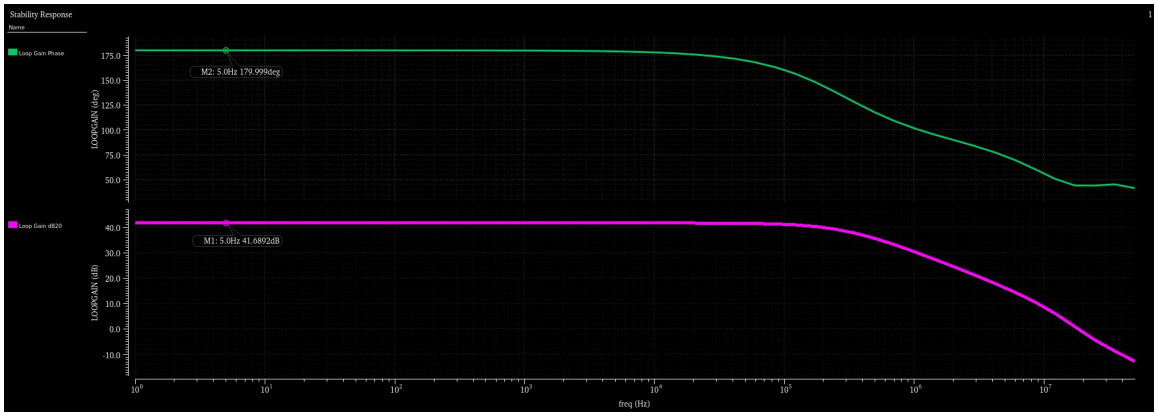
Include plots for:

- Open-loop gain and phase

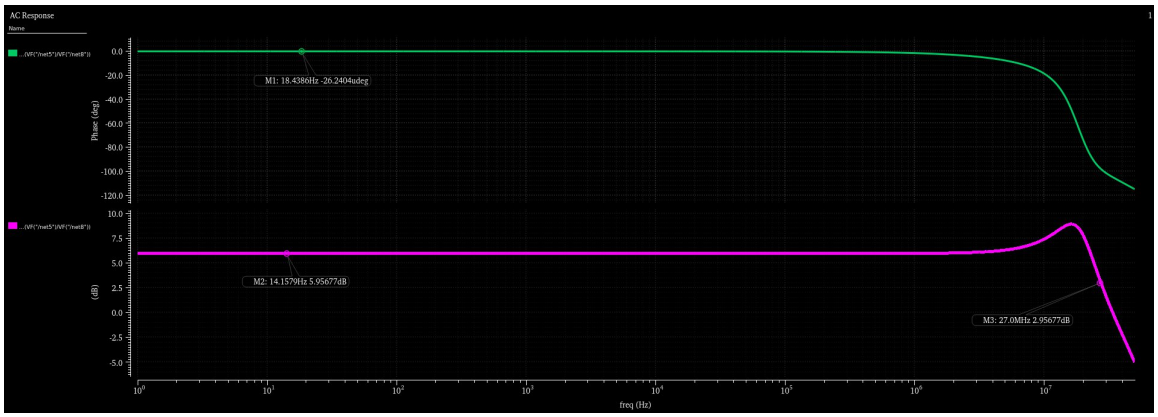
Adm Plot



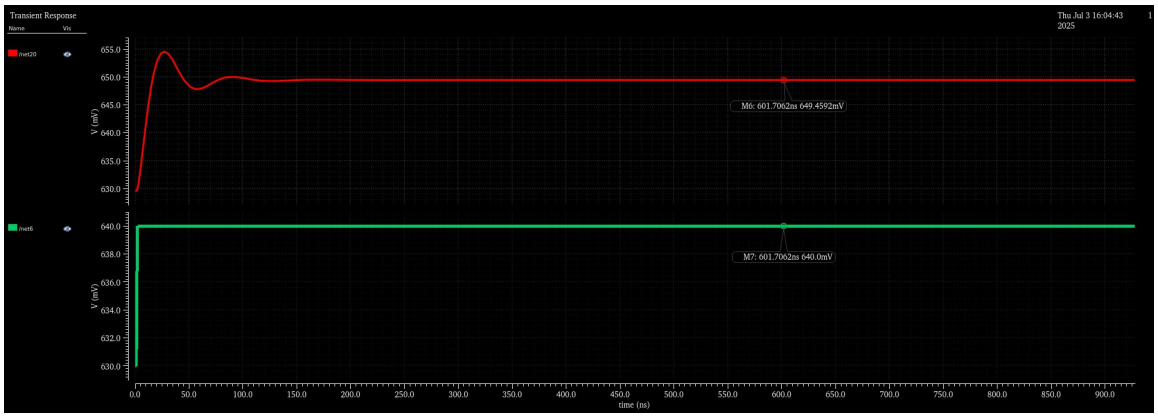
Loop gain and phase



- Closed-loop gain and phase



- Transient response with step input



Steady-State Error Analysis

A step input of **10 mV (0.01 V)** was applied with Vbias of 630mV to the non-inverting amplifier. The output settled at:

$V_{out,ss}=649.4593\ mV$

The bias voltage was **640 mV**, so the actual output step is:

$\Delta V_{out}=649.4593\ mV-640\ mV=\mathbf{9.4593\ mV}$

Since the expected ideal output step is **10 mV**, the **simulated steady-state error** is:

$SSE_{sim}=0.01\ V-0.0094593\ V=0.0005407\ V=\mathbf{540.7\ \mu V}$

Theoretical Steady-State Error

The loop gain from simulation is:

$A_{loop}=1041.6892/20\approx121.31$

The theoretical SSE is:

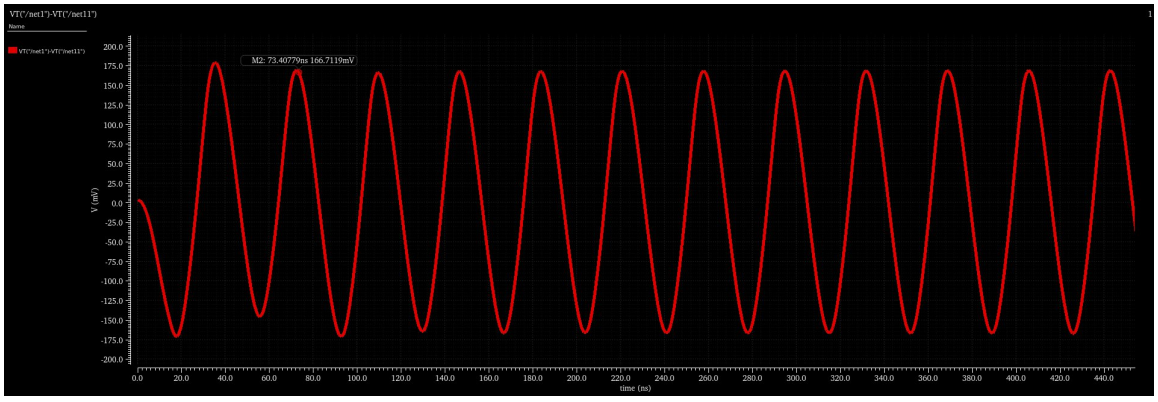
$SSE_{theoretical}=1/(1+A_{loop})=1/(1+121.31)\approx0.00818$

For a 10 mV step input:

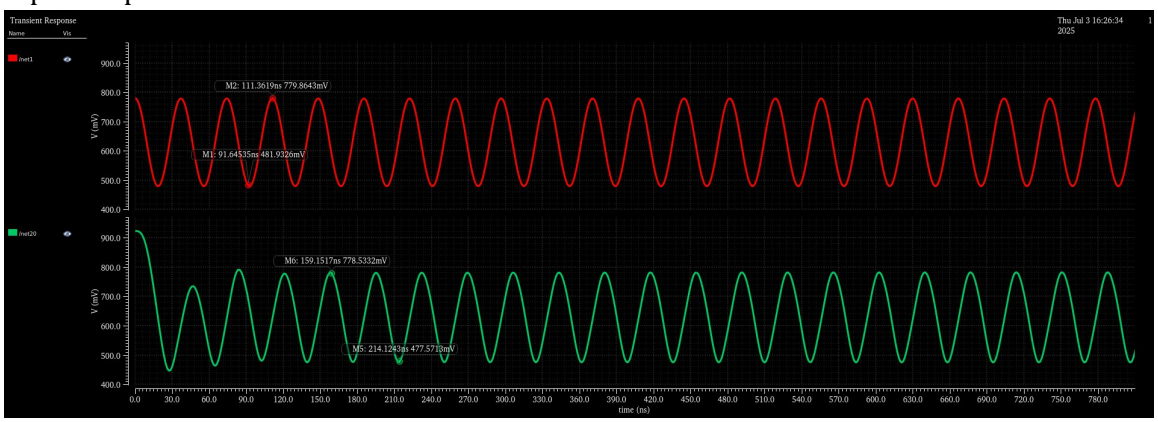
$SSE_{theoretical}=10\ mV\times0.00818\approx\mathbf{81.8\ \mu V}$

- Transient response with 150 mV cos(ωt) for ω= ω3dB

V+ - V- plot

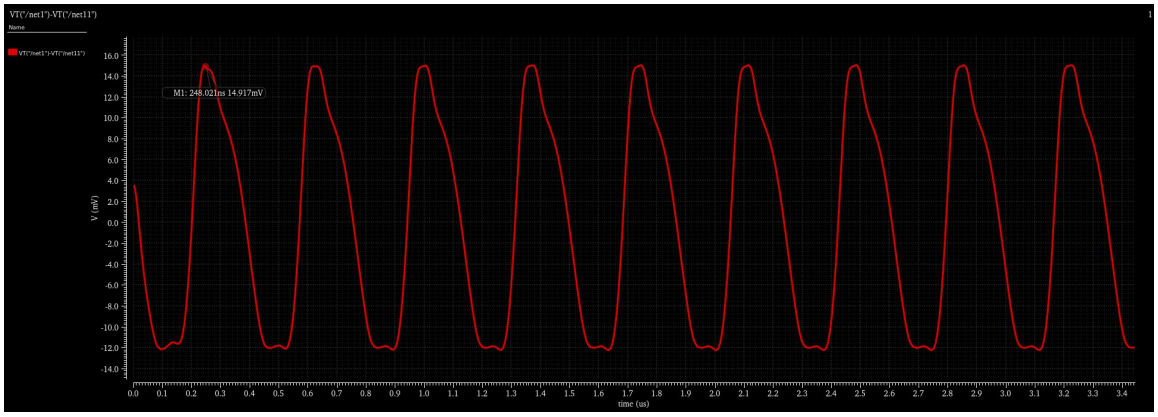


Input Output Plots

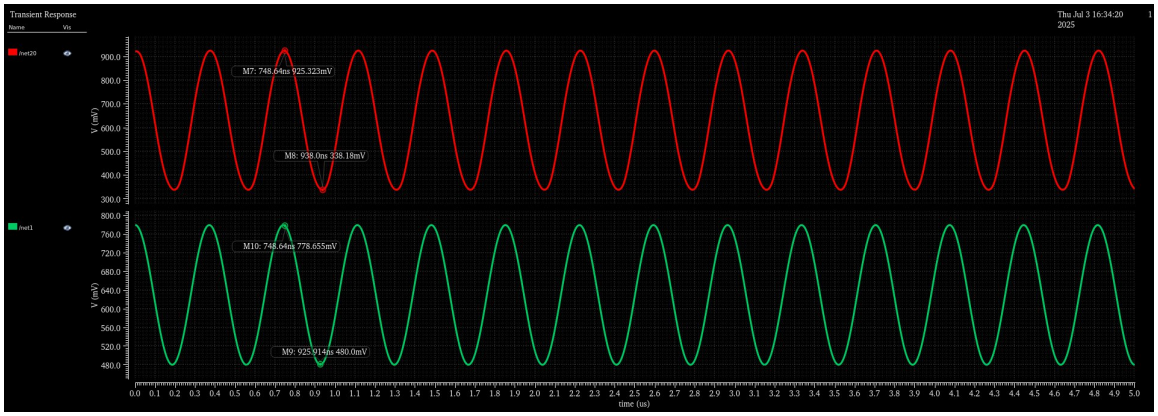


- Transient response with 150 mV cos(ωt) for ω = ω3dB/10

V+ - V- plot



Input Output Plot

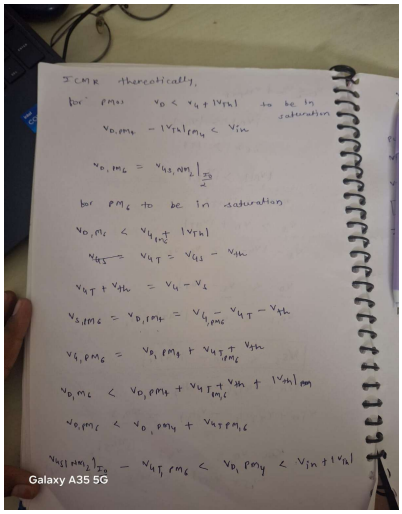


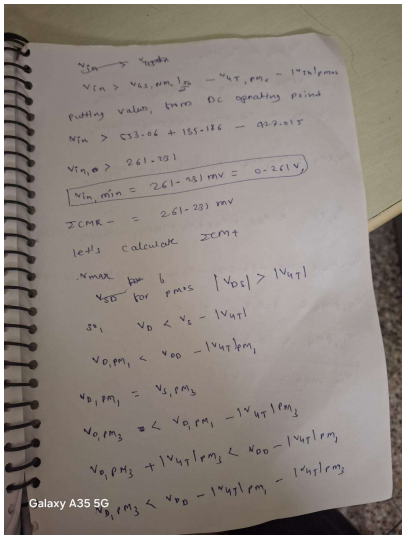
- Difference between diffamp input voltages

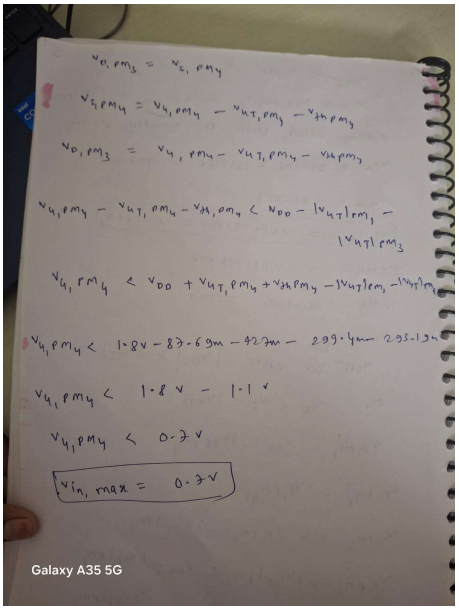
- At **ω = ω₃dB**, the peak input difference was **166.71 mV**
- At **ω = ω₃dB/10**, the peak input difference was only **14.92 mV**

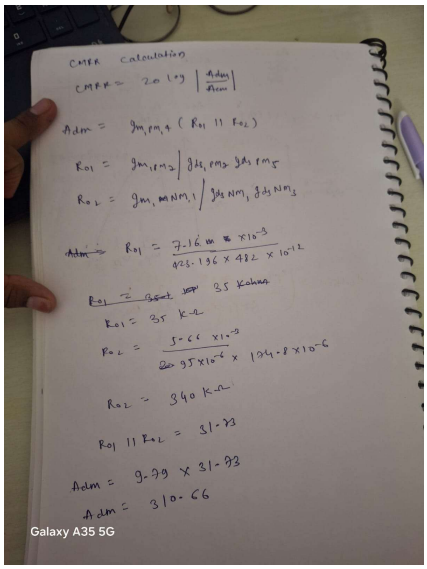
6. Theoretical Calculations

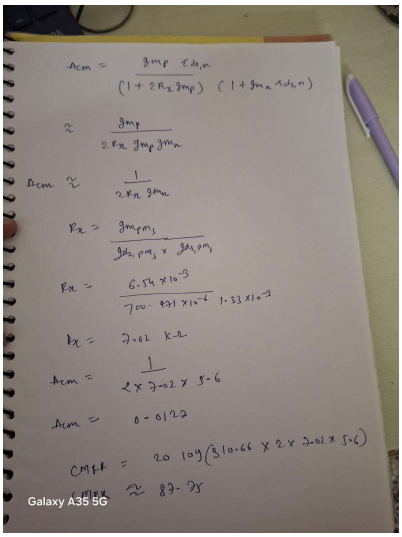
Calculate and explain: ICMR+, ICMR-, CMRR, Gain, etc., using small-signal parameters fromDC simulation.

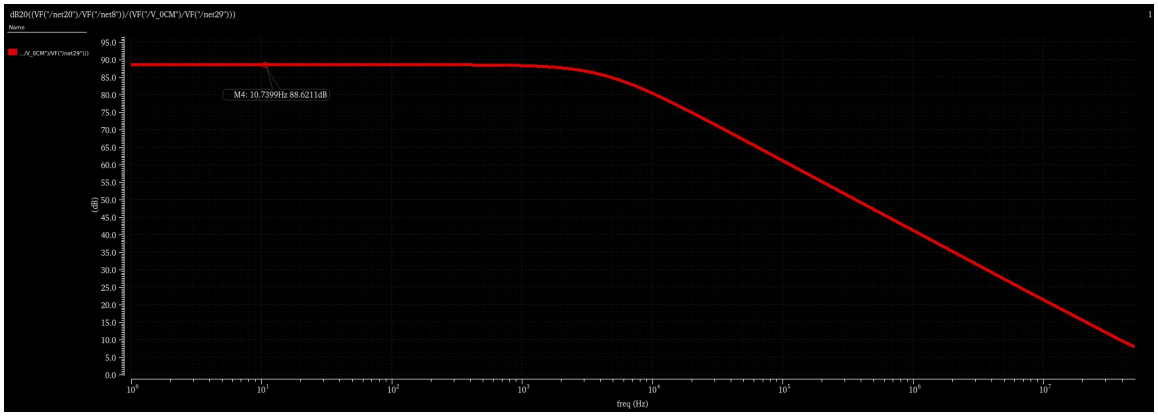












10. Conclusion

Theoretical and Simulated Results

The following parameters were computed both theoretically (using incremental parameters from DC operating point simulation) and verified through Cadence simulation.

Parameter	Theoretical Value	Simulated Value
$ICMR^+$	0.70 V	0.73 V
$ICMR^-$	0.261 V	0.49 V
CMRR	87.75 dB	88.6211 dB

11. References

EE610 Lectures

Thank You