EE610A: Analog VLSI Circuits

Simulation Assignment

Instructor: Imon Mondal, imon@iitk.ac.in

Design a single stage differential amplifier to be used in a non-inverting configuration shown in Fig. 1(a), with the following specifications. $V_{DD} = 1.8\,\text{V}$, $v_i = 150\,mV\sin(\omega t)$ The technology file is provided separately.

Roll No.	Input stage	V_{DD}	C_L	Loop gain (min)	–3dB Bandwidth of V_0/V_i (min)	CMRR(@dc)
4N	nMOS	1.8 V	10 pF	40 dB	100 MHz	80 dB
4N+1	pMOS	1.8 V	10 pF	40 dB	50 MHz	80 dB
4N+2	nMOS	1.8 V	20 pF	40 dB	50 MHz	80 dB
4N+3	pMOS	1.8 V	20 pF	40 dB	25 MHz	80 dB

A prototype schematic of the opamp is shown in Fig. 1(b). Modify it to satisfy your specification. For the pMOS input stage you will need to flip the polarities (all nMOS transistors becomes pMOS and vice-versa) of all the transistors. Other than a single master current source I_0, and voltage sources V_{DD} and V_{Bias}, all other reference voltages must be generated internally. Choose V_{Bias} to satisfy your specifications.

Try to satisfy all parameters at room temperature. However, sweep temperature from 0 to 70^o and tabulate your results.

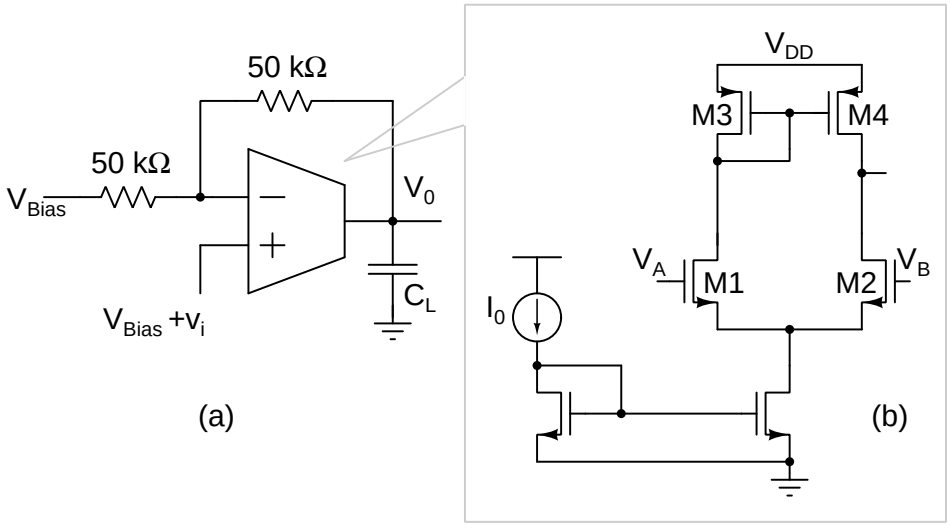

Fig. 1. (a) Top level of the opamp. (b) Prototype internal schematic (without zero cancelling resistor). (c) CMFB of first stage. (d) CMFB of second stage.

You must submit a softcopy (pdf) of the results. It must contain all the schematics with sizes of all the transistors and their g_ms (wherever relevant) clearly marked. If you plan to submit screen-shots of your schematics, ensure that all these are legible. Else, draw them with any circuit drawing tool (encouraged). Your report must contain the steps that you undertook to approach the design. Don't just dump data.

Plot the following for room temperature.

- Open loop gain and phase.
- Closed loop gain and phase (v_0/v_i); Indicate the –3 dB bandwidth.
- Transient response of the non-inverting amplifier with a 0.01 V step input at v_i. What is the steady state error? What is the theoretically evaluated steady state error?

- Transient response of the non-inverting amplifier when $v_i = 150\,mV\cos(\omega_{3dB}t)$ where ω_{3dB} is the –3dB bandwidth of the amplifier. Plot the same when $\omega = \omega_{3dB}/10$.
- The difference between the input voltages of the diffamp in Fig. 1(a) for inputs $150\,mV\cos(\omega_{3dB}t)$ and $150\,mV\cos((\omega_{3dB}/10)t)$.

Find the following theoretically and verify with simulation. For theoretical calculations use the incremental parameters that you will get from the DC operating point simulation.

- ICMR+ for the open loop diffamp.
- ICMR- for the open loop diffamp.
- CMRR for the open loop difamp.
- The difference between the input voltages of the diffamp in Fig. 1(a) for inputs $150\,mV\cos(\omega_{3dB}t)$ and $150\,mV\cos((\omega_{3dB}/10)t)$.

Tabulate g_m, g_{ds}, c_{gs}, c_{gd}, V_{ov} for all transistors.