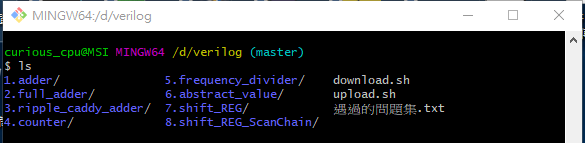
寫過的verilog、上傳與下載檔案寫成sh檔案、將遇到的問題存下來

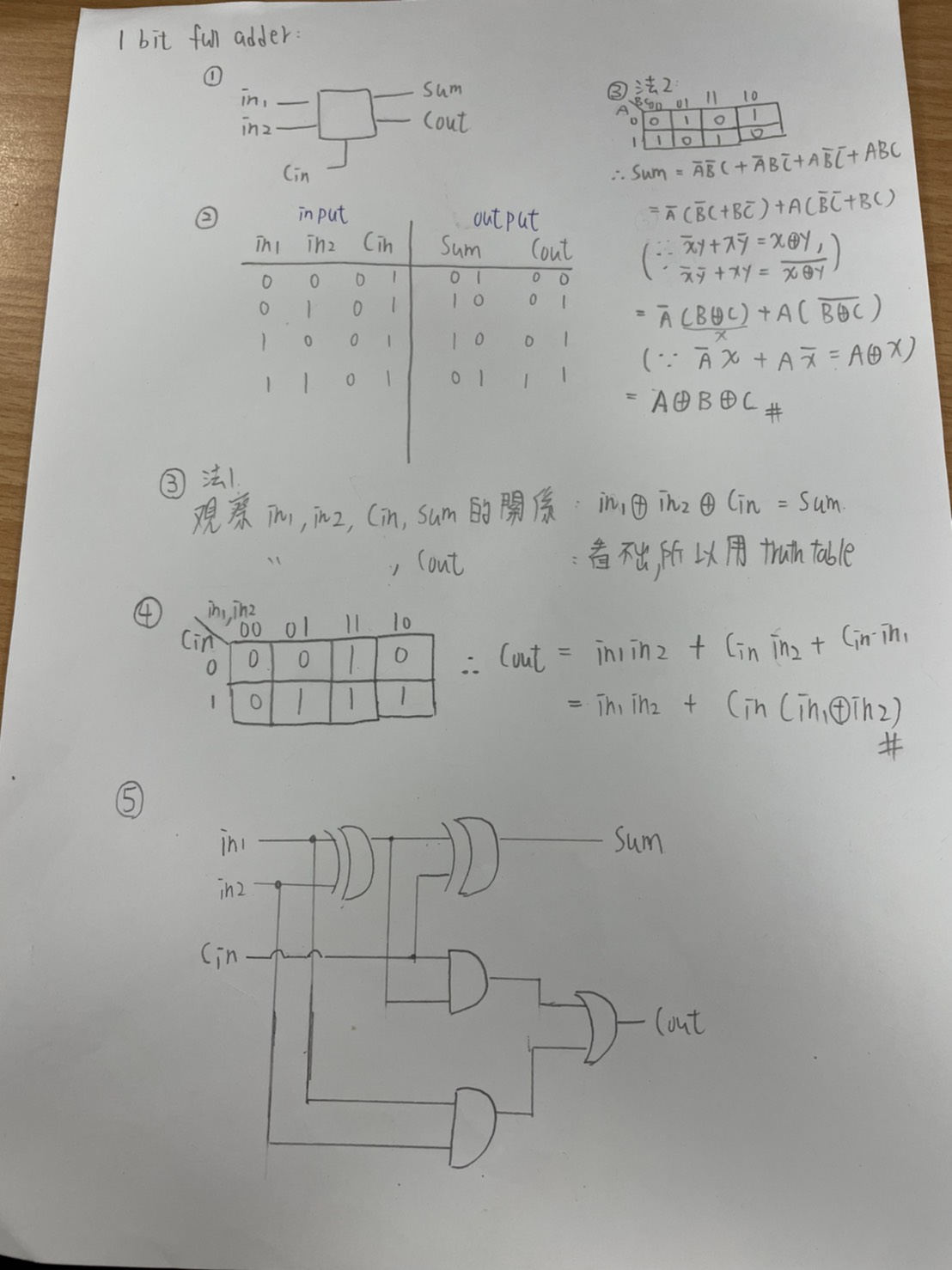


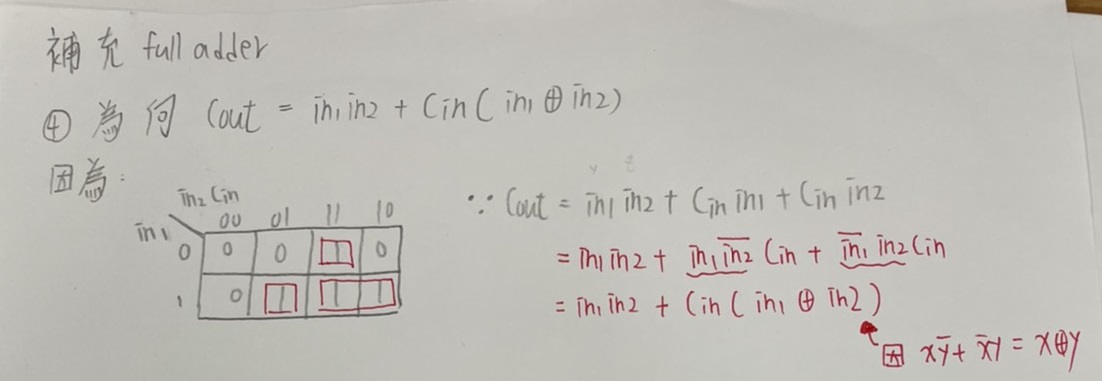
遇過的問題集

1. reg的輸出，一定要宣告成reg

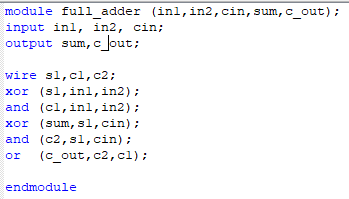
# Full\_adder 全加法器

電路圖

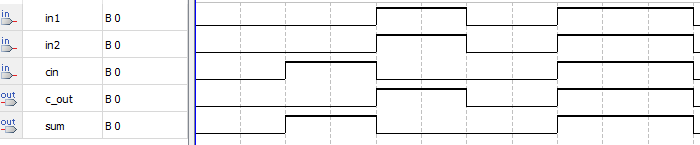




程式碼:



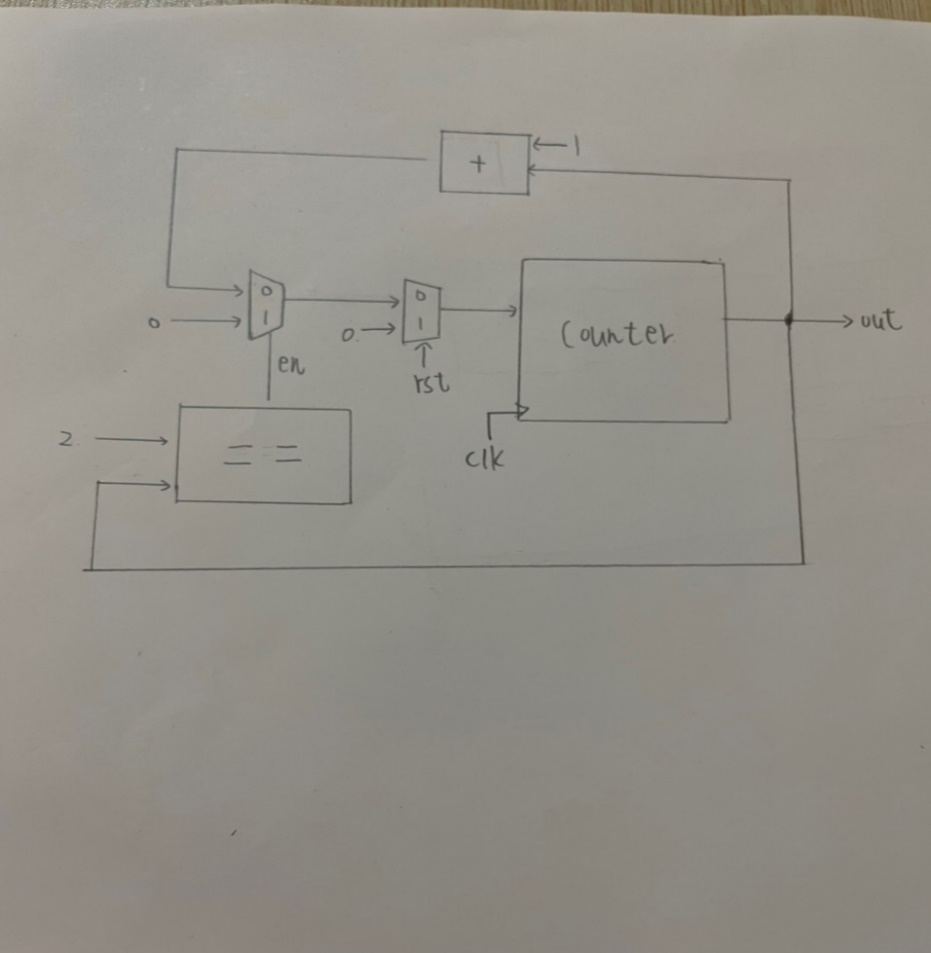
Waveform



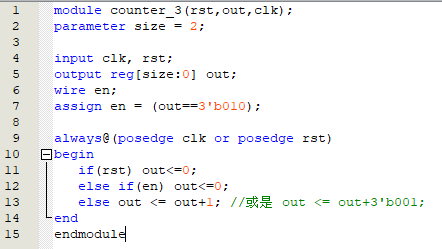
# Counter 計數器

**數3的計數器**

電路圖



程式碼



Waveform

數3次則歸0重新上數

