# SINGAPORE POLYTECHNIC
# SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

ET0104 Embedded Computer Systems Laboratory

**Laboratory 6 - Digital to Analogue, Analogue to Digital Interfacing**

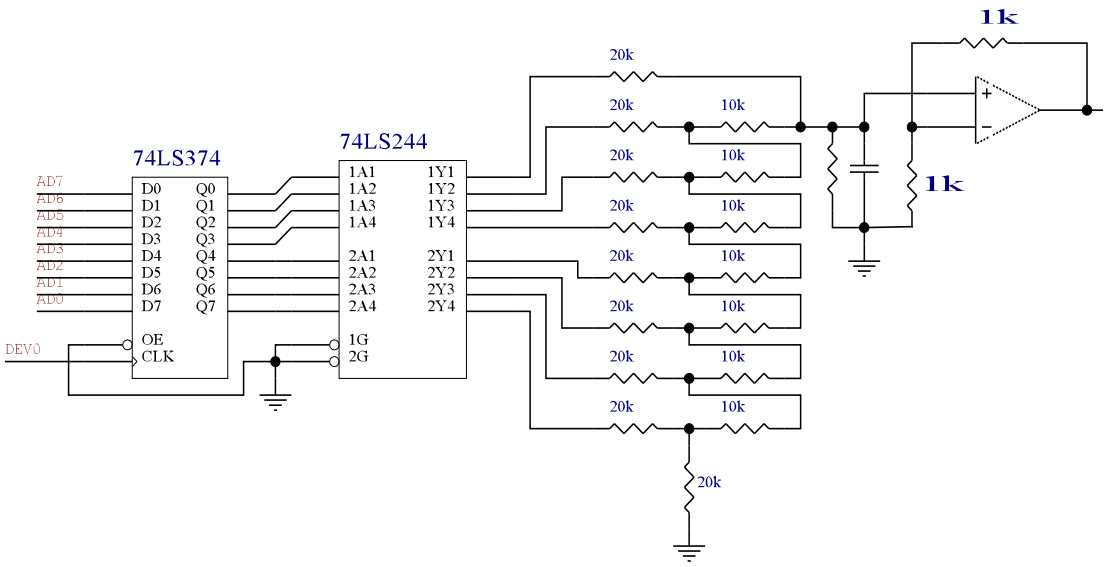
## Objectives

- To configure a latch and buffer to work with a R-2R network
- To anticipate the output of a D/A converter given various digital inputs
- To observe the working of a A/D converter

In this lab, you will use the SBC to output various values to an R-2R network.

## Digital to Analogue conversion

Digital to Analogue (D/A) interfacing allows a microcontroller to perform analogue control, as opposed to on-off control for purely digital systems. Most D/A converters are made of integrated circuits. These circuits are made up of R-2R networks anyway, with various degrees of quality in the integrated components. In this lab we are using a voltage mode converter. Note the use of the 74LS244 which increases the current drive of the 74LS373 latch. The opamp acts as a buffer and provides a gain of 2.




R-2R ladder in voltage conversion mode

First we need to find out the resolution of the D/A converter. This will help us in various calculations later. The resolution is the smallest change in the analogue output, for the

smallest change in the digital input. The following program LAB6A.C will generate a certain waveform: what is its shape?

```
#define DACPort 0x330
#define TRUE 1

unsigned char DACout;

void main()
{
      DACout = 0;
      while TRUE
      {
            _outp(DACPort, DACout);      /* DAC Port */
            DACout++;                    /* increment */
      }
}
```

To answer this, consider the smallest and largest values DACout will take.

Initial observations

Now power up the I/O Board, and load the program LAB6A.C. Run the program and this time, power on the oscilloscope and attach a probe at the connector DA_OUT, located near the top left of the board.

What is the maximum *digital* value that will be output to the R-2R circuit? _____

What is the maximum *analog* value of the wave you see? _____

What is the resolution of the D/A circuit? _____

Note that if the waveform was distorted, we should only use the linear portion.

## Generating a sine wave

Using the program LAB6B.C, we put in data and count values so we can see a sine wave at the DAC output.

We note that:

1) This hardware configuration cannot output a negative voltage. If we need to generate a sine wave, we need to add an offset to it.

2) In order to minimize the quantization error, we want the maximum value of the waveform to be reached when the maximum digital value is output.

In general, the equation of a sine wave with offset is:

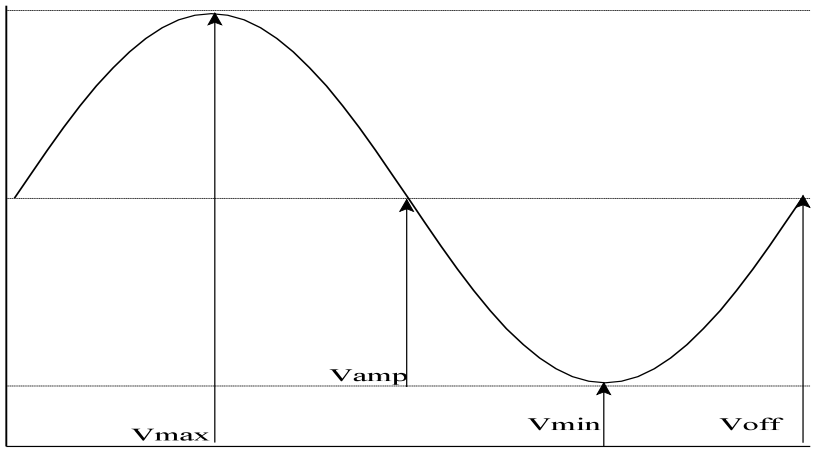
$$Vout = Voff + Vamp * \sin \theta$$

From the diagram, the value of the offset voltage,

$$Voff = (Vmax + Vmin) / 2$$

and hence the amplitude,

$$Vamp = (Vmax - Vmin) / 2$$




General equation of a sine wave with offset

For our lab, we let the minimum be zero, so the sine wave is:

$$V = (Vamp * \sin \theta) + Voff \quad \text{or;} \quad Vmax/2\ (1 + \sin \theta)$$

We have seen that the resolution ρ, is the voltage represented by one bit for the DAC. The *scale factor* $F_{scale}$ is the digital value for one volt and is the reciprocal of the resolution, 1 / ρ.

From the previous measurement, the value of $F_{scale}$ is: _____

The table below will assist you in the calculation of the necessary values for the generation of a sine wave using 12 equal intervals

| θ | 0 | 30 | 60 | 90 | 120 | 150 | 180 | 210 | 240 | 270 | 300 | 330 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| sin θ | 0 | 0.5 | 0.87 | 1 | 0.87 | 0.5 | 0 | -0.5 | -0.87 | -1 | -0.87 | -0.5 |
| $V=V_{max}/2*(1+\sin \theta)$ | | | | | | | | | | | | |
| $F_{scale} * V$ | | | | | | | | | | | | |

Substitute the calculated values into the appropriate data locations in LAB6B.C. Execute the

program and observe the output on the oscilloscope.

What would we have to change in order to obtain

i) a smoother sine wave?

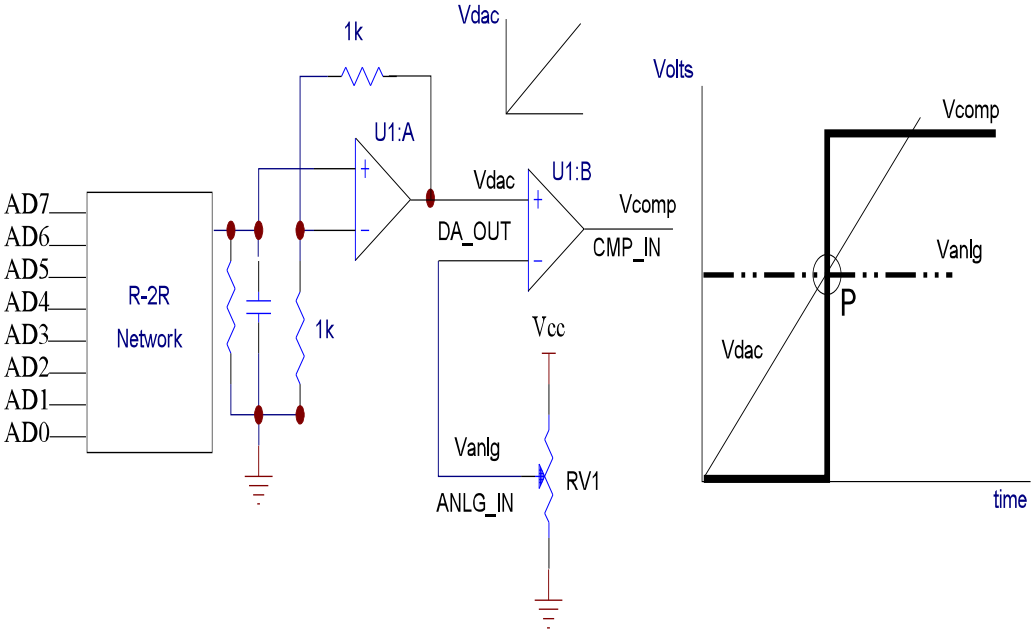
_____

ii) a higher/lower frequency waveform?

_____

## Analogue to Digital Conversion

An Analogue to Digital (A/D) converter takes analog signals and converts them into their corresponding digital representations. A/D can be implemented in many ways. For example, Counter Ramp, Successive approximation, Dual Ramp and Flash conversion. Simpler types like the Counter Ramp can be built using a DAC and feedback circuitry.




Feedback ADC

In general when using a feedback ADC, a sample of the input analog voltage, $V_{anlg}$ is taken and held at one input of the comparator, U1:B. With reference to the above diagram, the other input is connected to the output of a DAC, at U1:A. A digital value is applied at the input of the DAC. This voltage is then compared with the $V_{anlg}$. The output of the comparator $V_{comp}$ remains low until point P. This is when $V_{dac}$ equals $V_{anlg}$ and $V_{comp}$ goes high.

The Counter Ramp version of a feedback ADC works by applying a steadily increasing digital input to the DAC. The corresponding analog voltage,$V_{dac}$ is also a rising ramp as seen above. At point P, when $V_{comp}$ goes high, the input to the DAC is the digital equivalent of the analog voltage $V_{anlg}$.

Observation

To generate the ramp, we will make use of LAB6A.C again. Load the program and run it.

Set up the oscilloscope for a dual trace input, using the same scale for both channels. Observe the outputs at jumpers CMP_IN and DA_OUT. Locate these points on the I/O board. Use only CMP_IN pin 2. The CMP_IN and DA_OUT signals are actually $V_{comp}$ and $V_{dac}$, as seen in the diagram above. Sketch the waveforms below.

We can vary the voltage $V_{anlg}$ using potentiometer RV1. From the schematic diagram, the voltage range is 0 to 5 V.

Do so and note that the duty cycle of CMP_IN changes.

Performing voltage measurements

Now observe CMP_IN on the oscilloscope. It should be a pulse wave. Now adjust RV1 so the duty cycle decreases. Do this until CMP_IN *just becomes zero*.

From the schematic of the Feedback ADC before, what value of $V_{anlg}$ will cause CMP_IN to be low continuously? _____.

Verify this by using another oscilloscope probe to look at the signal $V_{anlg}$ by looking at pin ANLG_IN on the IO board.

Now vary RV1 until the signal at CMP_IN has a 50% duty cycle. Think about what the value

of $V_{anlg}$ should be and verify it.

Do this once more for a 25% duty cycle.

Can you explain why this is so?

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Assume that the processor takes t seconds to generate the digital values 0 to 255. When output to the DAC, this generate analogue voltages from 0 to $V_{FSD}$, the maximum or full scale output.

This voltage $V_{dac}$ is input to the comparator U1:B. If $V_{anlg}$ is half of $V_{FSD}$ it follows that the processor will only need t/2 seconds to reach this value. This will account for the 50% duty cycle. In this case, immediately when $V_{cmp}$ goes high, the processor will have only output the value 127, which is 255 divided by 2.

End of lab