SINGAPORE POLYTECHNIC **ET0104**

2017/2018 SEMESTER TWO EXAMINATION

Diploma in Computer Engineering
Diploma in Electrical and Electronic Engineering
3rd Year Full-Time

EMBEDDED COMPUTER SYSTEMS Time Allowed: 2 Hours

Instructions to Candidates

1. The examination rules set out on the last page of the answer booklet are to be complied with.

2. This paper consists of **THREE** sections:

   Section A - 10 Multiple Choice Questions, 2 marks each.
   Section B - 6 Short Questions, 10 marks each.
   Section C - 1 Long Question, 20 marks.

3. **ALL** questions are **COMPULSORY**.

4. All questions are to be answered in the answer booklet. Start each question in Sections B and C on a new page.

5. Fill in the Question Numbers, in the order that it was answered, in the boxes found on the front cover of the answer booklet under the column "Question Answered".

6. This paper consists of 9 pages, inclusive of data sheets.

SECTION A

MULTIPLE CHOICE QUESTIONS [2 marks each]

1. Please **tick** your answers in the **MCQ box** on the second page of the answer booklet.
2. No marks will be deducted for incorrect answers.

A1. Which one of the following is *not* the correct reason for using only 10 bits for addressing I/O in a PC/104 system?

(a) Less electronic hardware is needed for decoding.
(b) There are normally much less I/O devices than memory.
(c) The circuit board holding the electronics is smaller and cheaper to manufacture.
(d) There is less propagation delay, so there is faster access. (2 marks)

A2. The rotational speed of a stepper motor is controlled by the

(a) size of the load it is turning.
(b) pulse frequency.
(c) direction of the current in the stator coil.
(d) value of the current in the stator coil. (2 marks)

A3. Sample-and-hold circuits in analog-to-digital converters (ADCs) are used to:

(a) stabilize the value of the input analog signal during conversion.
(b) sample and hold the output of the binary counter during the conversion process.
(c) sample and hold the D/A converter staircase wave during the conversion process
(d) stabilize the internal comparator threshold voltage during conversion. (2 marks)

A4. Using Pulse Width Modulation (PWM) to generate an analogue waveform has several advantages over traditional multibit Digital to Analogue (DAC) converters. Which one of the following is not an advantage?

(a) Lower pin count.
(b) Less heat dissipated.
(c) Higher signal switching speed.
(d) Less analog filtering needed. (2 marks)

A5. Which one of the following is not true about the lower case letters `g`, `j`, `p`, `q` and `y` used in text based LCDs?

(a) They have a compressed look as compared to other characters.
(b) The uppercase versions of these letters are displayed properly.
(c) A special version of the CGROM is needed to display them correctly.
(d) To display them properly, the LCD needs to use 5x10 character size. (2 marks)

A6. In small sized embedded computers like those found in smartphones, how should an integrated graphics display be connected to the system?

(a) S-video cable.
(b) RGB cable.
(c) Direct connection to the system bus.
(d) Composite video cable. (2 marks)

A7. When designing a GUI which uses green colour to indicate an *unsuccessful* operation, which one of the following principles of user interface design does this go against ?

(a) Consistency.
(b) Efficiency.
(c) Association with human interface objects.
(d) Anthropomorphization. (2 marks)

A8. In multitasking environments, which one of the following is not suitable to be used as a synchronization object?

(a) Resource Object.
(b) Mutex Object.
(c) Semaphore Object.
(d) Event Object. (2 marks)

A9. Which one of the following is not a function of an operating system?

(a) Process user input and output.
(b) Word processing.
(c) Task management.
(d) File management. (2 marks)

A10. What will happen if an embedded system does not use a file system to access large amounts of data?

(a) Its execution time will be slower.
(b) The programs have to use global variables more.
(c) Data that is needed has to be stored within its programs.
(d) The system will cost more. (2 marks)

SECTION B [60 marks]

B1. The following questions relate to using programs written in C in an embedded system.

(a) In terms of an optimizing C compiler, what is the effect of the `volatile` keyword? (3 marks)

(b) What is the effect of the `const` keyword and what kind of data should it affect? (3 marks)

(c) What is one benefit of using global variables? (2 marks)

(d) To access an array, why is it better to use pointers rather than indexes? (2 marks)

B2. The segment of C code in Fig C initializes a LCD and then display a message. Note what needs to be written in the answer booklet.

(a) By looking at the numbered comments in the C code, the one line LCD is to be initialized. *List* down the values in hexadecimal. (3 marks)

b) After initializing, the program sends data to the LCD. Sketch the expected display. (Hint: some overwriting of data will happen!) (7 marks)

```
char warn[] = "Water at=....(M)";

lcdcmd(0x__);      /* 1. 5x7 dot font, 4-bit interface */
lcdcmd(0x__);      /* 2. turn on the display */
lcdcmd(0x__);      /* 3.DDRAM address increment/cursor shift on o/p */

lcdcmd(0x80);      /* function executes LCD COMMAND */
for (j = 0; j < 16;j++)
{
      k = warn[j];
      lcddata(k);
}
lcdcmd(0x89);      /* function executes LCD COMMAND */
lcddata(0x30);     /* function displays LCD data */
lcddata(0x2E);
lcddata(0x31);
lcddata(0x32);
```

Fig C - segment of C code

Assume that functions `lcdcmd()` and `lcddata` are available to output commands and data respectively, to the LCD.

B3. A Digital to Analogue Converter is used to generate a sine wave. For an input of 0FFH, it outputs 4V which will be the *peak to peak* voltage of the signal. One cycle of this wave is sampled at six equal time intervals.

(a) List the values needed in table form to produce this signal and sketch the output for a multibit converter. (7 marks)

(b) In order to use a single bit PWM for this waveform, sketch the resulting output before filtering. Indicate the width of the pulses as a fraction of 1. (3 marks)

B4. (a) A device that measures the water level in a tunnel comprises of a water sensor attached to a pole moved by stepper motor with a 1.8 degree step. This motor is connected to a gear which converts a rotary motion into a linear one. One revolution of the motor moves the sensor 2 centimeters. In order to move the sensor at 4 centimeters per minute, what is the time delay required between pulses sent to the motor? (4 marks)

(b) Here, the motor phases are connected to a latch so that phase A is connected to bit 0, phase B to bit 1 and so on. Using a table, write down the binary control values required to move the motor for a *two phase on* full step mode. (6 marks)

B5. As part of a system to detect water in an underground tunnel, a video based solution is proposed based on a PC/104 system. Since the tunnel has poor lighting, high colour fidelity is not needed.

(a) Suggest a suitable colour depth to be used for the video. (3 marks)

(b) Using a 640 by 480 pixel display, what is a suitable frame display rate that is a multiple or submultiple of 50 Hz? (7 marks)

B6. (a) What are the three states in which a task can exist? (4 marks)

(b) When the time-slice for a task ends, which state will it go into? (2 marks)

(c) What happens when processes and threads do not synchronize their operations together? (4 marks)

SECTION C [20 marks]

C1. A system to measure the water level in a tunnel consists of a movable platform carrying a motor which drives a water sensor vertically along a beam so as to detect new water levels. A LCD connected in 4 bit mode with backlighting will show various messages.

When the water level reaches a threshold, an alarm will sound out periodically.

A 10 button keypad allows users to customize the system.

An 8 bit DAC connected to an amplifier will give out warning sounds if the water level becomes too high.

Using a PC/104 system, design a decoding scheme for controlling the measurement system using a 74LS688 and a 74LS138 with buffers and latches. The starting address is 330_{16}.

(a) What is the minimum number of buffers and latches needed? Describe how you derive this number. (4 marks)

(b) Draw the I/O map and truth table. (7 marks)

(c) Draw a schematic diagram of the decoding circuit. (5 marks)

(d) Write the one line C code to write a variable to the motor. (4 marks)

- End of Paper -

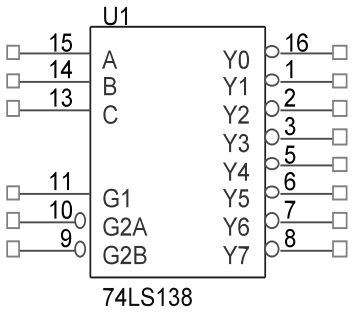
APPENDIX

LCD Instruction Table

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (when F_{cp} or f_{osc} is 250KHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears Display and returns cursor to the Home Position (Address 00)	80uS = 1.64mS
Return Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to Home Position. Returns shifted display to original position. Does not clear display	40uS = 1.6mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets DD RAM counter to increment or decrement (I/D) Specifies cursor or display shift during to Data Read or Write (S)	40uS
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets Display ON/OFF (D), cursor ON/OFF (c), and blink character at cursor position	40uS
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor or shifts the display w/o changing DD RAM contents	40uS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets data bus length (DL), # of display lines (N), and character font (F)	40uS
Set CG RAM Address	0	0	0	1	A_{CG}						Sets CG RAM address. CG RAM data is sent and received after this instruction	40uS
Set DD RAM Address	0	0	1	A_{DD}							Sets DD RAM address. DD RAM data is sent and received after this instruction	40uS
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) and address counter contents	1uS
Write Data from DD or CG RAM	1	0	Write Data								Writes data to DD or CG RAM and increments or decrements address counter (AC)	40uS
Read Data from DD or CG RAM	1	1	Read Data								Reads data from DD or CG RAM and increments or decrements address counter (AC)	40uS
I/D=1: Increment S=1: Display Shift on data entry S/C=1: Display Shift (RAM unchanged) R/L=1: Shift to the Right DL=1: 8 bits N=1: 2 Lines F=1: 5x10 Dot Font D=1: Display ON C=1: Cursor ON B=1: Blink ON BF=1: Cannot accept instruction				I/D=0: Decrements S=0: Cursor Shift on data entry S/C=0: Cursor Shift (RAM unchanged) R/L=0: Shift to the Left DL=0: 4 bits N=0: 1 Line F=0: 5x7 Dot Font D=0: Display OFF C=0: Cursor OFF B=0: Blink OFF BF=0: Can accept instruction							Definitions: DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM Address A_{DD}: DD RAM Address(Cursor Address) AC: Address Counter used for both DD and CG RAM Address	Execution Time changes when Frequency changes per the following example: If F_{CP} or f_{osc} is 27 KHz 40uS x 250/270 = 37uS

* Don't Care

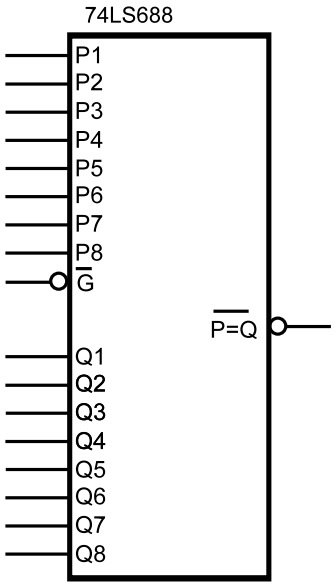
LCD Character Map



74LS138 schematic

INPUTS						OUTPUTS							
ENABLE			SELECT										
G2B	G2A	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Truth table



74LS688 schematic

Inputs		$\overline{P=Q}$
Data P,Q	Enable $\overline{G}$	
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H