SINGAPORE POLYTECHNIC **ET0104**

2018/2019 SEMESTER ONE EXAMINATION

Diploma in Computer Engineering
Diploma in Electrical and Electronic Engineering
3rd Year Full-Time

EMBEDDED COMPUTER SYSTEMS Time Allowed: 2 Hours

Instructions to Candidates

1. The examination rules set out on the last page of the answer booklet are to be complied with.

2. This paper consists of **THREE** sections:

   Section A - 10 Multiple Choice Questions, 2 marks each.
   Section B - 6 Short Questions, 10 marks each.
   Section C - 1 Long Question, 20 marks.

3. **ALL** questions are **COMPULSORY**.

4. All questions are to be answered in the answer booklet. Start each question in Sections B and C on a new page.

5. Fill in the Question Numbers, in the order that it was answered, in the boxes found on the front cover of the answer booklet under the column "Question Answered".

6. This paper consists of 9 pages, inclusive of data sheets.

SECTION A

MULTIPLE CHOICE QUESTIONS [2 marks each]

1. Please **tick** your answers in the **MCQ box** on the second page of the answer booklet.
2. No marks will be deducted for incorrect answers.

A1. When accessing Input/Output devices on a PC/104 system, what is the largest number of such devices that can be accommodated?

(a) 10.
(b) 16.
(c) 256.
(d) 1024.

(2 marks)

A2. To half step a stepper motor, how are the stator coils to be activated?

(a) Two coils on for all steps.
(b) Two coils for one step, then one coil for the next step.
(c) One coil for all steps.
(d) Three coils for one step, then two coils for the next step. (2 marks)

A3. An eight bit Parallel/Flash ADC can be thought of as comprising:

(a) resistors, encoder and 256 comparators.
(b) resistors, encoder and 8 comparators.
(c) resistors, encoder and 4 comparators.
(d) resistors, encoder and 1 comparator. (2 marks)

A4. When should a Digital to Analogue (DAC) converter be used instead of Pulse Width Modulation (PWM) to generate an analogue waveform?

(a) For lower cost.
(b) To save energy.
(c) A need for simple analog filtering.
(d) The processor runs at a lower clock speed. (2 marks)

A5. An embedded system for use in the World Cup has to display the ₽ (rouble) symbol. With reference to the LCD character chart in the datasheets provided, what should you do?

(a) Software has to store the character in DDRAM when power comes on.
(b) Construct the character, write to CGRAM when initializing.
(c) Have a manufacturer build an LCD with this symbol.
(d) Obtain the ASCII code for the rouble symbol to display it. (2 marks)

A6. Which of the following is *true* when considering the conversion from 24 bit to 8 bit colour?

(a) Conversion is necessary to display an image in real time.
(b) From the 8 bit colour, the original 24 bits can be recovered.
(c) The resulting picture may have large patchy coloured areas.
(d) Eight bit colour can only be displayed on a composite video cable. (2 marks)

A7. Which of the following is *not* a consideration factor of ergonomic guidelines for User Interface Design ?

(a) Use flashing messages.
(b) Short sequence of tasks.
(c) Consistent icons between screens.
(d) Appropriate use of visual cues.

(2 marks)

A8. When does a context switch occur?

(a) The CPU is reassigned to perform another task from its current one.
(b) When a thread needs to communicate with another thread.
(c) When a main program calls a function.
(d) The CPU has to wait on a resource.

(2 marks)

A9. Which of the following is an advantage of a process as compared to a thread?

(a) There is more memory on the heap because of better system support.
(b) Better protection between tasks if one of them has a system problem.
(c) The context switch will be faster due to less memory used.
(d) The race condition will not cause a problem here. (2 marks)

A10. For a multitasking operating system, global variables can be accessed by several tasks at a time. What are some possible consequences?

(a) The updating program can hang the system.
(b) The system runs slower due to access conflicts.
(c) The CPU can execute the modifications faster.
(d) A race condition can cause errors in updating.

(2 marks)

SECTION B [60 marks]

B1. (a) In what ways can an embedded system using the C language save on use of RAM? (6 marks)

(b) For two of the methods in (a) explain how RAM usage is minimized. (4 marks)

B2. The segment of C code initializes a LCD and then displays a message. Note what needs to be written in the answer booklet.

(a) In the C code, the numbered comments show how the two line LCD is to be initialized. *Write* these values into your answer book (3 marks)

b) After initializing, the code sends data to the LCD. Sketch the expected display in your answer booklet. (7 marks)

Assume that functions `lcdcmd()` and `lcddata` are available to output commands and data respectively, to the LCD.

```
char msg[] = "Time /No Plate  ";

lcdcmd(0x__);      /* 1.5x7 dot font, 4-bit interface */
lcdcmd(0x__);      /* 2.Turn on the display */
lcdcmd(0x__);      /* 3.DDRAM address increment/cursor shift on o/p */

lcdcmd(0x80);      /* function executes LCD COMMAND */

for (j = 0; j < 16;j++)
{
    k = msg[j];
    lcddata(k);
}
lcdcmd(0xC0);      /* function executes LCD COMMAND */
lcddata(0x31);     /* function displays LCD data */
lcddata(0x32);
lcddata(0x3A);
lcddata(0x33);
lcddata(0x30);
```

B3. A Digital to Analogue Converter is used to generate a rectified full wave voltage based on a *sine* function. For an input of 0FFH, it outputs 4.5V which will be the *peak to peak* voltage of the signal. One cycle of this wave is sampled at six equal time intervals.

(a) List the values needed in table form to produce this signal and sketch the output for an eight bit converter. (5 marks)

(b) For this wave, a frequency of 100Hz is required. Using the converter in (a), what is the time delay between samples? (2 marks)

(c) When using a single bit PWM for this waveform, sketch the resulting unfiltered output. The width of the pulses should be shown as a fraction of 1. (3 marks)

B4. (a) A four phased stepper motor with a 1.8 degree movement is connected so that phase A is connected to bit 0, phase B to bit 1 to and so on. The following control sequence in hexadecimal is sent to it at regular intervals:

0x3, 0x6, 0xC, 0x9 / 0x3, 0x6, 0xC, 0x9...(repeats)

Describe the position control method used and its advantages. (6 marks)

(b) If this sequence is used to move a car park gantry by 90 degrees, how many steps are needed? (2 marks)

(c) In order not to occupy the processor unnecessarily, what are two hardware methods to control the motor? (2 marks)

B5. A video camera is proposed as part of a system to read a number plate. The images are digitized over a PC/104 system. For this purpose, a grayscale image of 640 by 480 pixels is needed.

(a) State one difference and one similarity between grayscale and indexed colour images. (4 marks)

(b) Calculate a suitable frame display rate that is a multiple or submultiple of 25 Hz. (6 marks)

B6. (a) What are two ways a task gives way to another in a multitasking system? (2 marks)

(b) *Explain* which one of these methods can use the `Sleep()` function in the C language to achieve multitasking. (3 mark)

(c) Briefly explain what is a race condition. (2 marks)

(d) What are the three ways to prevent a race condition from happening? (3 marks)

SECTION C [20 marks]

C1. To manage certain types of a car parks, a PC/104 system will be used. It uses a camera to capture an image of a vehicle number plate and compute the number. This number is transferred as a series of 8 bit numbers. A light sensor measures the ambient light so the software can perform optimally.

A LCD connected in 4 bit mode will show the number plate read and the time, along with other messages.

The gantry movement can be considered as controlled by a stepper motor connected over 4 bits.

There are eight buttons through which users interact with the system.

Using a PC/104 system, design a decoding scheme for controlling the measurement system using a 74LS688 and a 74LS138 with buffers and latches. The starting address is 350_{16}.

(a) What is the minimum number of buffers and latches needed? Describe how you derive this number. (4 marks)

(b) Draw the I/O map and truth table. (7 marks)

(c) Draw a schematic diagram of the decoding circuit. (5 marks)

(d) Write the one line C code to read a byte from the light sensor. (4 marks)

- End of Paper -

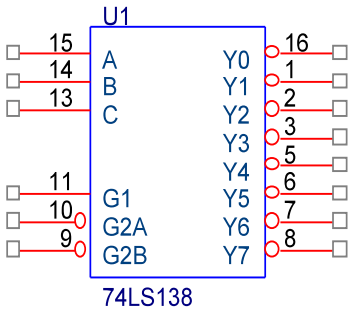
APPENDIX

LCD Instruction Table

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (when F_{cp} or f_{osc} is 250KHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears Display and returns cursor to the Home Position (Address 00)	80uS = 1.64mS
Return Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to Home Position. Returns shifted display to original position. Does not clear display	40uS = 1.6mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets DD RAM counter to increment or decrement (I/D) Specifies cursor or display shift during to Data Read or Write (S)	40uS
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets Display ON/OFF (D), cursor ON/OFF (c), and blink character at cursor position	40uS
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor or shifts the display w/o changing DD RAM contents	40uS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets data bus length (DL), # of display lines (N), and character font (F)	40uS
Set CG RAM Address	0	0	0	1	A_{CG}						Sets CG RAM address. CG RAM data is sent and received after this instruction	40uS
Set DD RAM Address	0	0	1	A_{DD}							Sets DD RAM address. DD RAM data is sent and received after this instruction	40uS
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) and address counter contents	1uS
Write Data from DD or CG RAM	1	0	Write Data								Writes data to DD or CG RAM and increments or decrements address counter (AC)	40uS
Read Data from DD or CG RAM	1	1	Read Data								Reads data from DD or CG RAM and increments or decrements address counter (AC)	40uS
I/D=1: Increment S=1: Display Shift on data entry S/C=1: Display Shift (RAM unchanged) R/L=1: Shift to the Right DL=1: 8 bits N=1: 2 Lines F=1: 5x10 Dot Font D=1: Display ON C=1: Cursor ON B=1: Blink ON BF=1: Cannot accept instruction				I/D=0: Decrements S=0: Cursor Shift on data entry S/C=0: Cursor Shift (RAM unchanged) R/L=0: Shift to the Left DL=0: 4 bits N=0: 1 Line F=0: 5x7 Dot Font D=0: Display OFF C=0: Cursor OFF B=0: Blink OFF BF=0: Can accept instruction							Definitions: DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM Address A_{DD}: DD RAM Address(Cursor Address) AC: Address Counter used for both DD and CG RAM Address	Execution Time changes when Frequency changes per the following example: If F_{CP} or f_{osc} is 27 KHz 40uS x 250/270 = 37uS

* Don't Care

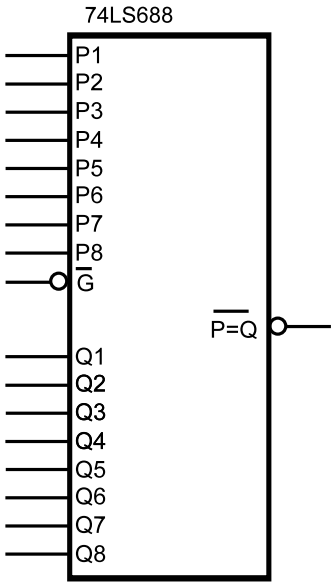
LCD Character Map



74LS138 schematic

INPUTS						OUTPUTS							
ENABLE			SELECT										
G2B	G2A	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Truth table



74LS688 schematic

Inputs		$\overline{P=Q}$
Data P,Q	Enable $\overline{G}$	
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H