Singapore Polytechnic
School of Electrical and Electronics Engineering
ET0104 Embedded Computer Systems DECC 3FT/4EO

Tutorial 2 PC Architecture

1. a)

ISA Bus width (bits) ==>	Address		Data
	Memory bits/range	I/O bits/range	
Theoretical sizes	24 bits /16 MB/0-FFFFFFh	16 bits / 64 K/0-FFFFh	16
Commonly used	20 bits /1 MB/0-FFFFFh	10 bits / 1K/0-3FFh	8

b) Theoretically, 16.67 MBytes / sec (8.33x2) but only 8.33 MB/s because 2 cycles/transfer.
c) AEN active indicates DMA controller has address bus instead of processor
d) Separate Read / Write lines for memory and I/O.
e) Memory map vs I/O map I/O - memory mapped may interfere with allocation of memory for programs. But uses more flexible addressing modes which may result in faster data transfer. I/O mapped does not have program allocation problems, but may be slower in operation.

2.

Type of memory	Use	Reason
ROM	program messages, tables	non volatile
RAM	1) data 2) temporary store photograph	1) read/write 2) fast storage
Flash (Parallel) *Device*	photograph	non volatile, erasable use available interfaces eg USB
Serial EEPROM *Chip*	Store settings	non volatile, erasable, small size, part of system

3. Main board uses mainly DRAM. Those on boards use mainly ROM and SRAM. Memory on PC/104 bus is mainly A0000H and above.

4. a) Buffer for input b) latch for output.

5. Intel processor resets to address FFFF0H. Get address of Reset routine and jumps there. Note that BIOS is F0000-FFFFFH and is nonvolatile memory.

   Motherboard designer uses BIOS routines to fetch 1st sector of secondary storage, load the 512 bytes therein to address 07C00H and executes it.