Singapore Polytechnic
School of Electrical and Electronics Engineering
ET0104 Embedded Computer Systems DECC 3FT/4EO

Tutorial 3 Address decoding with I/O devices

1. Foldover occurs when the number of address lines from the CPU is greater than the number of address lines on the memory chip. Multiple CPU addresses will access the same memory address. Eliminated by adding extra hardware to do full decoding.

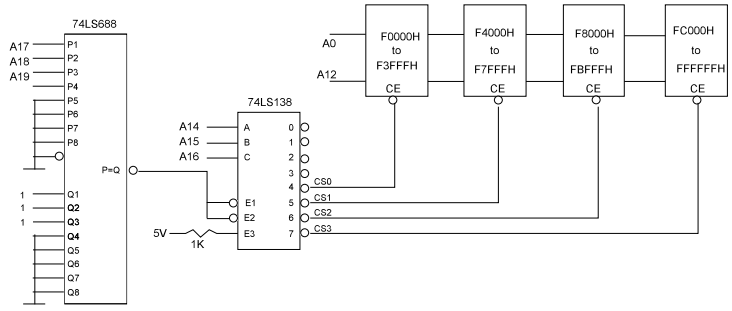
2. Highest address is FFFFFH (20 bits) - 64K is F0000H to FFFFFH.

   Memory device - 16K x 8 - A0 to A13. This device uses address pins A0 to A13.
   Each chip will take up 16384_{10} or 4000H addresses i.e. 0000-3FFFH.(2^{14} = 16384).
   4 chips.(64K/16K).

   ROM 1 - F0000H to F3FFFH
   ROM 2 - F4000H to F7FFFH
   ROM 3 - F8000H to FBFFFH
   ROM 4 - FC000H to FFFFFH

```
A19 A18 A17 A16 A15 A14 A13 A12- - - - - - A0
1   1   1   1   0   0   x------------------x F0000-F3FFFH
1   1   1   1   0   1   x------------------x F4000-F7FFFH
1   1   1   1   1   0   x------------------x F8000-FBFFFH
1   1   1   1   1   1   x------------------x FC000-FFFFFH
```

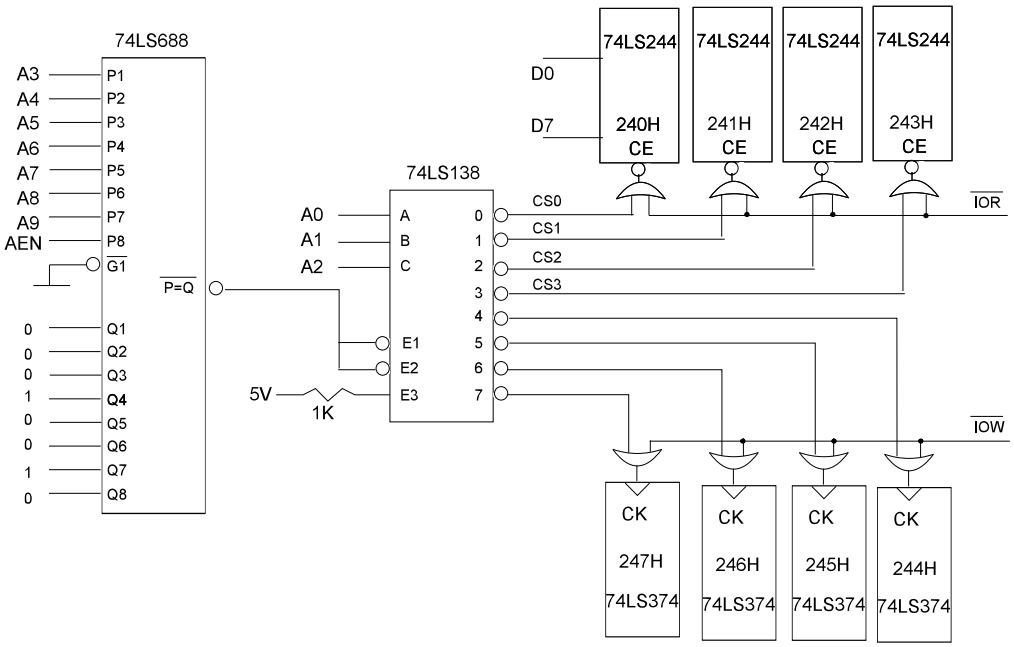
   A17-19 enabled by 74688



   Program code-so use EP/ROM

3. Other solutions possible:

```
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
1  0  0  1  0  0  0  0  0  0        240H Buffer
1  0  0  1  0  0  0  0  0  1        241H Buffer
1  0  0  1  0  0  0  0  1  0        242H Buffer
1  0  0  1  0  0  0  0  1  1        243H Buffer
1  0  0  1  0  0  0  1  0  0        244H Latch
1  0  0  1  0  0  0  1  0  1        245H Latch
1  0  0  1  0  0  0  1  1  0        246H Latch
1  0  0  1  0  0  0  1  1  1        247H Latch
```



4. 74LS688 can use a DIP switch which can be easily changed to accommodate different addresses. Otherwise have to use fixed logic gate to do the address comparison. (Please refer to lecture notes)

5. (Note: Here the differences are due to how the devices are designed. This is different from Memory vs I/O mapped I/O)

Memory devices	I/O devices (buffer/latches)
occupies several addresses - has its own address bus	occupies one address - no address bus
has 3-4 control pins - CS/WE/OE - may not need extra gate	1-2 control pins CE/Clk - requires extra gates to decode

6. 14 switches can be read by 2 buffers. Two seven segment LEDs use two latches. Thus we have 4 I/O devices and we need to do I/O decoding. Refer to I/O address map in lecture notes - select a suitable I/O address range that is NOT used by the system. EG 330H

   If there is time, proceed to do the hardware decoding.