INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN: 2278 – 0211 (Online)

Real Time Design & Implementation Of Digital Speedometer On FPGA

Aparajita Adhikary
Department of Electrical and Electronics Engineering (EEE)
Bangladesh University of Business & Technology
Shumit Saha
Department of Electronics and Communication Engineering (ECE)
Khulna University of Engineering & Technology (KUET)
Robin Sarker
Department of Electronics and Communication Engineering (ECE)
Khulna University of Engineering & Technology (KUET)

Abstract:

In this paper, a Digital Speedometer is designed and implemented using FPGA (Field Programmable Gate Array). Here, the FPGA used is Smart Fusion FPGA. It is more flexible in hardware and embedded design where need a true system-on-chip (SoC) solution FPGA devices are ideal than traditional fixed-function microcontrollers and without the excessive cost of soft processor cores on traditional FPGAs. At the inception, the speedometer is designed using Verilog Hardware Description Language. Synthesis-software algorithmically transforms the Verilog source code into a netlist, a logically-equivalent description consisting only of elementary logic primitives (AND, OR, NOT, flip-flops, etc.) that are available in a specific FPGA or VLSI technology. The designed speedometer gives lots of extra features than existing speedometers. The special addition of this speedometer is the velocity of the speedometer is accurate not only in normal times but also at exceedingly small velocities.

Key words: *Digital Speedometer; FPGA; Verilog HDL; Motor Vehicles; Embedded System .*

1.Introduction

In an automobile, an electronic instrument cluster, digital instrument panel or digital dash for short, is a set of instrumentation, including the speedometer that is displayed with a digital readout rather than with the traditional analog gauges. Many refer to it simply as a digital speedometer. Digital Speedometer implementation over FPGA is the basic concept of this paper [1]-[3].

FPGA is an innovative solution for the industrial, medical, energy, communications and military markets in diverse applications, including system management, power management, motor control, industrial networking and display [4].

In this paper, a speedometer is designed and implemented on FPGA. Here, the speedometer displays the speed of motor vehicle in km/hr. However the digital speedometer sense pulses from a sensor (which attached in vehicle wheel) and then it calculate the speed of the vehicle and display the speed in a "LCD" or "7 segment display". The features of this speedometer are given a digital readout, speed displays in km/h. It has shown more important feature is linear with change of speed like the analog speedometer. The range of speed could be measured the speedometer is 0 km/h to 999 km/hr. The extra characteristic of the speedometer can cope with decreased speed automatically whereas other speedometers appear the same velocity if the arrival of new pulse is very slow gradually.

This paper is structured as follows. Section II depicts about the methodology to be designed of system. In Section III describes the proposed architecture of the speedometer and the block of each part of this model and also analyze the simulation and synthesized results. Finally, Section IV is for conclusion.

2.Methodology

Our proposed methodology can be summarized as below:

- Step 1: In our consideration the Speedometer is designed with two counters denoted as$A$ & B. Counter A indicate previous count values and B indicate current count values.
- Step 2: When the device starts count the pulse 0 (i.e $x(0)$) then the counter A starts counting and it will continue until the arrival of next pulse. This means counter A stops counting clock when a pulse arrives. It has time between two counters for start

to arrival of the first pulse i.e. in mathematically ,counter A = x(1) – x(0) & counter B = 0.

- Step 3: After that the first pulse comes in counter B. It will be started counting until the arrival of the 2nd pulse. This means counter B has time to count between 1st and 2nd pulse i.e. B = x (2) – x (1).
- Step 4: If A>B, the speed will be gradually decreased. If B>A, then speed will be dramatically increased. In the meantime, when the 3rd pulse arrives in the counter, then B is copied in A and the time between 3rd and 2nd pulse is saved in B. We can define A = x(2) – x(1) & B = x (3) – x (2) and so on. In mathematically, for nth number of pulse it can be written that
  - Counter A = x (n – 1) – x (n – 2)
  - Counter B = x (n) – x (n – 1).
- Step 5: Record the values in 7 segment display.

The functional flow chart of the speedometer has shown in Fig.1.

2.Proposed Architechture

Fig.2 had shown the proposed architecture of digital speedometer. The whole architecture has a sensor [9] which used to sense the moving of wheel, in FPGA which is core part of the design and 7 segment display [11] to view the speed. The architectural description are given belows.

3.Sensor

In this speedometer, sensor named hall sensor is used. A hall sensor is a transducer that varies its output voltage in response to magnetic field. Hall sensors are used for proximity switching, positioning, speed detection, and current sensing applications. It has simplest form; the sensor operates as an analog transducer, directly returning voltage. With a known magnetic field, its distance from the hall plate can be determined [10].

Hall sensors are commonly used to time the speed of wheels and shafts, such as for internal combustion engine ignition timing, tachometers and anti-lock braking systems.

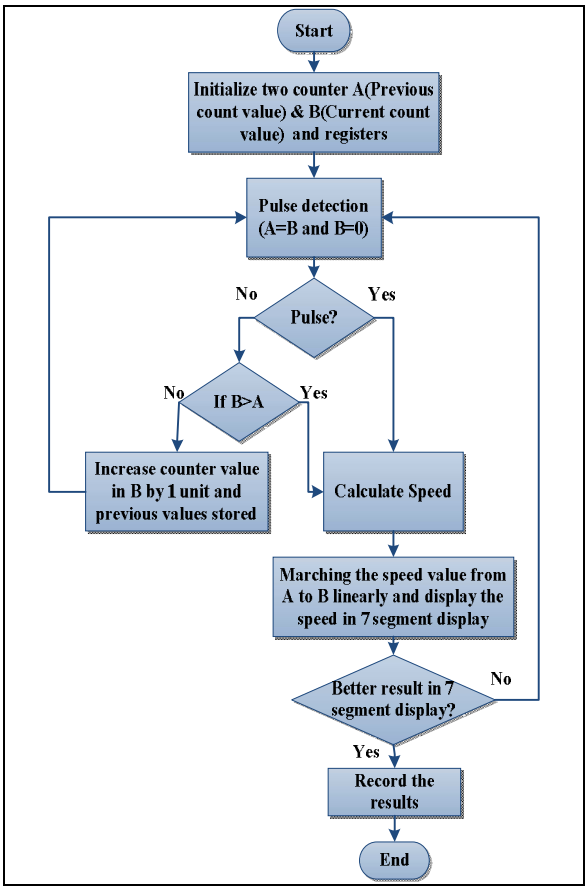

Figure 1:Functional flow chart of Speedometer

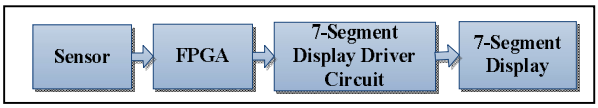

Figure 2: Block diagram of digital Speedometer

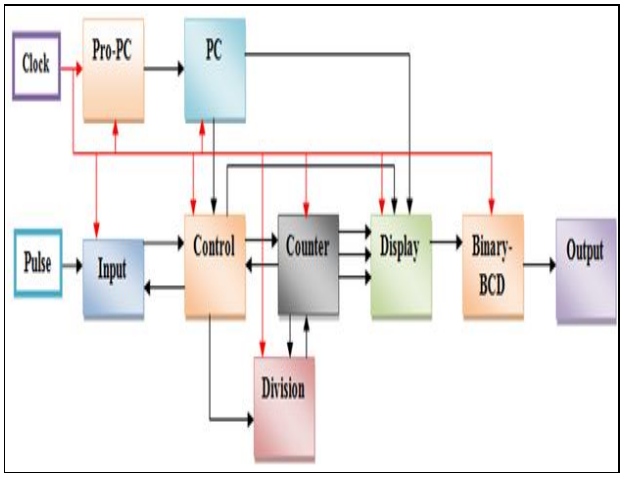

Figure 3: Block diagram of Verilog implementation

The top level design of speedometer on FPGA has shown in Fig.3. This has consisted different blocks which are described below:

Pro-Program counter (Pro-PC) : It is a kind of clock pulse generator and counter. It generates clock pulse for driving the Program counter (PC) from the main clock pulse. In this design it generates a pulse with one positive edge against four main clock pulses.Fig.4 shown of the RTL schematic diagram of Pro-PC.

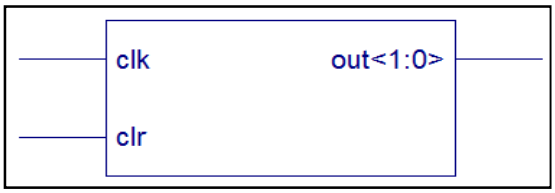

Figure 4: RTL Schematic of Pro-PC.

- Program counter (PC): It is a counter which counts the positive edge of input pulses.It comes from Pro-PC. This device drives by the control ROM.

  In Table I, the output of the Program counter (PC) is same for four main clock pulses. This will stabilize the Program counter (PC) for the main clock pulses. For this reason, Pro-Program counter (Pro-PC) is used. In Fig.5, the RTL schematic of the program counter is shown. In Fig. 5, w [1:0] is the 2 bit output which is the output of Pro-PC. The symbols defined as data_out [9:0] & control is the output port of the program counter.

Input of Pro-PC(main clk)	**Output of Pro-PC /input of PC(binary)**	**Output of PC(binary)**
0	0	0
1	01	0
0	01	0
1	10	0
0	10	0
1	11	01
0	11	01
1	0	01
0	0	01
1	01	01
0	01	01
1	10	01
0	10	01
1	11	10
0	11	10
So on…		

Table 1: Execution of PC block

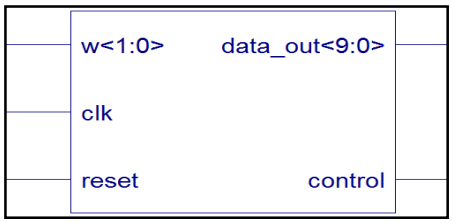

Figure 5: RTL Schematic of PC.

Control ROM: It has input from the Program Counter and 16 bit output which is called control bus. Table II, shows the full control bus structure.

Module Name	Control Bus Name (Bus number)
Input	Enable (1), Out(2)
Counter	Counter_out(3,4,5,6,7,8,9,10,11)
Division	In (12,13), Enable (16)
BCD	Reset (14)
Display	Enable (15)

Table 1: Control bus from control ROM to different module

The control bus architecture is shown including the internal structure as shown in Fig.6. It has consisted Input, Counter and PC block has bidirectional bus, other functional block Division and Display has unidirectional bus. Fig.7 shows the RTL schematic of the control ROM.

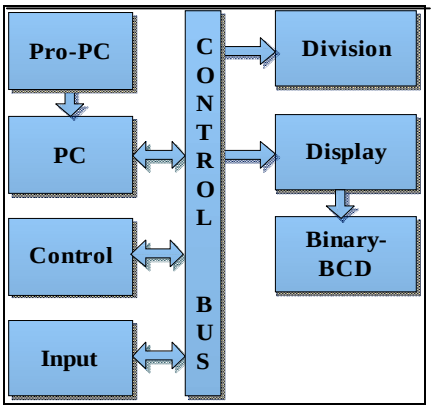

Figure 6: Block diagram of the system including control bus and internal structure.

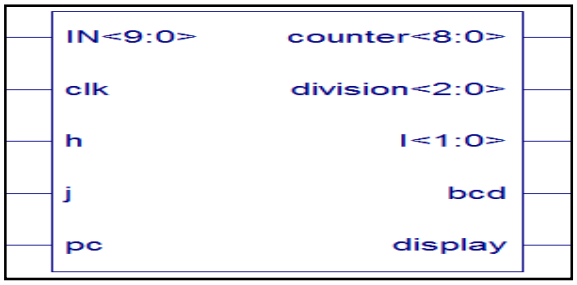

Figure 7: RTL Schematic of Control ROM.

- Division: It is a module which executes division operation of the system. Figure 8: shows the division block. Here, flag_forward and flag_backward are two signals which use to save the counts value of the program counter.

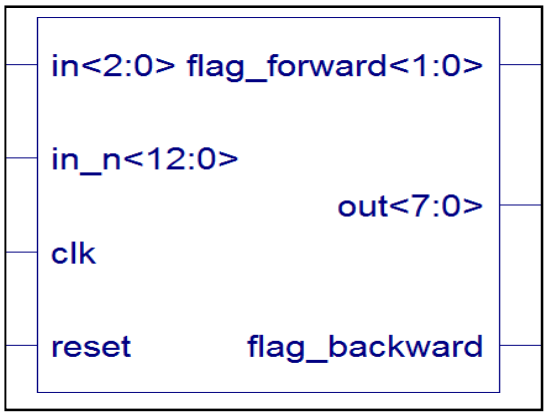

Figure 8: RTL Schematic of Division Block

- *Counter:* It counts the time between two consecutive revolutions of the wheel and store the previous count value.Fig. 8 shows the counter block. Here, control <8:0> is the input which comes from control block and division_counter<7:0> comes from division block. And the outputs are counter_division<12:0> & three counter_displays which goes to display block.

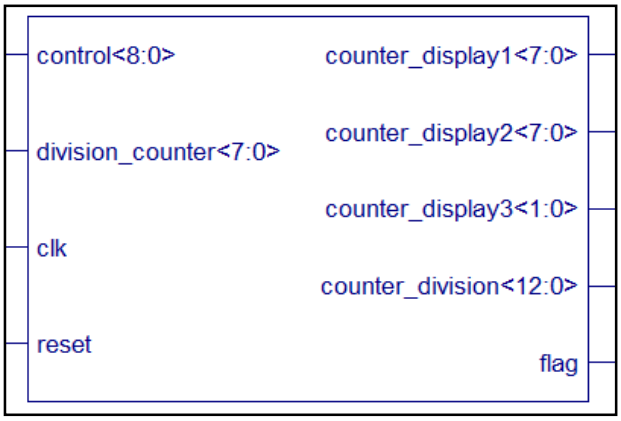

Figure 9: RTL Schematic of Counter Block.

- Display: It is a module which is responsible for marching the current speed value from previous speed value then passes the data to “Binary-BCD” module

and makes the change of speed value linearly. Fig. 10 shows the display module.

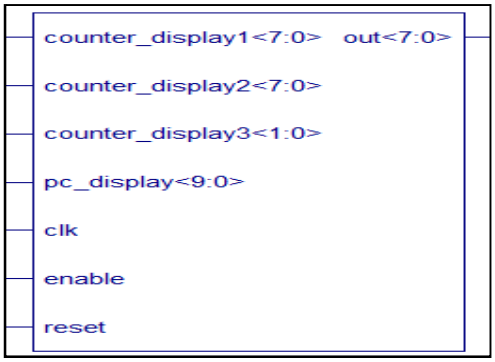

Figure 10: RTL Schematic of Display.

- Binary-BCD: It is a binary to BCD converter. In this architechture the input is 8 bit and the output goes to three switches. These three switches turns on three multiplexed seven sigment display. We have used Shift and Add-3 Algorithm.. This algorithm is given below:

  - Shift the binary number left one bit.
  - If 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column.
  - If the binary value in any of the BCD columns is 5 or greater, add 3 to that value in that BCD column.
  - Go to 1.

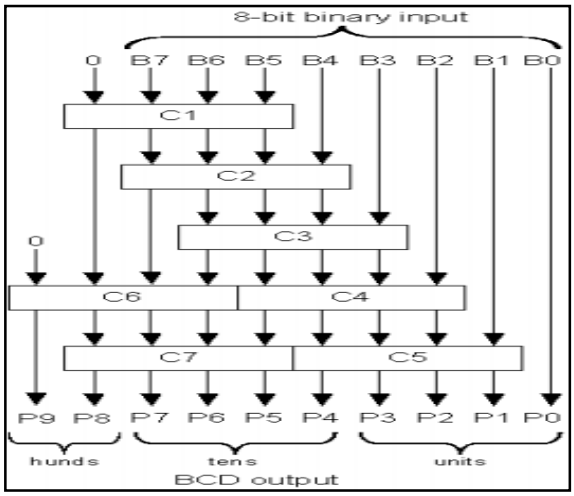

Figure 11: Functional block of Shift and Add-3 Algorithm.

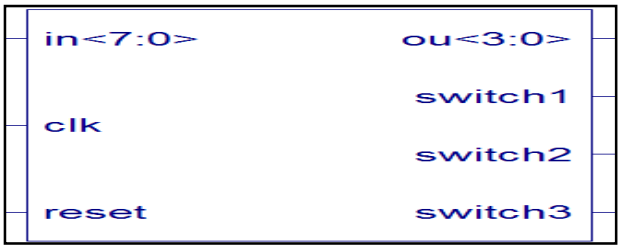

Figure 12: RTL Schematic of Binary-BCD block.

Fig. 11 shows the Functions of Shift and Add-3 Algorithm. And Fig. 12 shows the RTL Schematic of the Binary-BCD block. The top level diagram of the system has been shown in Fig.13. It's RTL schematic of the speedometer as shown in Fig.14.

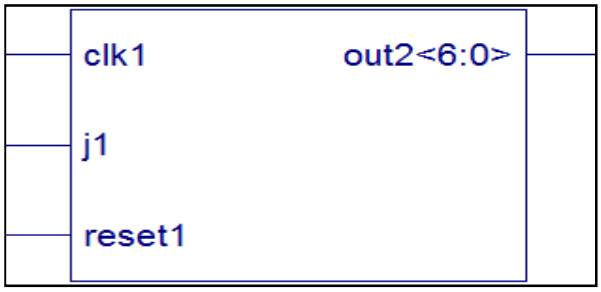

Figure 13: Top Diagram of Speedometer.

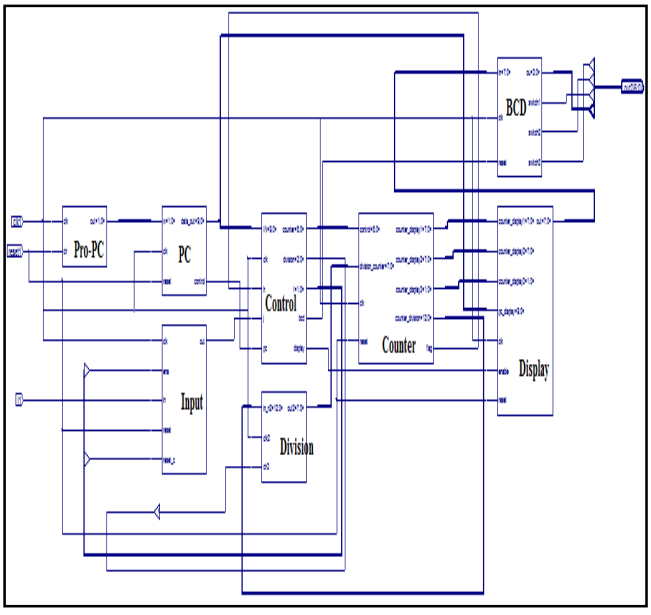

Figure 14: RTL Schematic of Speedometer.

The proposed model is loaded on XILINX FPGA board. It is implemented upon XILINX SPARTAN XC2S150 FPGA board processor. When it is implemented on FPGA board processor then the clock frequency of the processor is 1MHZ. The proposed model has the same power consumption, signal bandwidth and CMOS technology is used on the XC2S150 processor.

5.Seven Segment Display Driver

Finally, we have found the result of output is given into the multiplexed seven segment display. We have needed a seven segment display driver as shown in Fig.15. For this reason 7447 driver IC is used. It is a BCD to 7 segment decoder/driver IC. The output of the FPGA is shown in BCD format as described earlier so it can be directly fed into the 7447 IC. Here, A, B, C, D is four inputs of 7447 which are come from the FPGA module and 7447's output drives the 7 segment display.

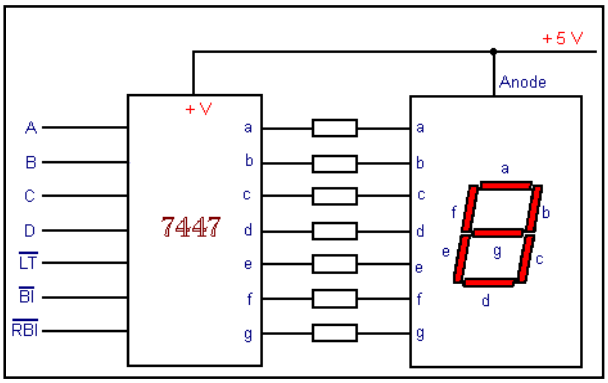

Figure 15: 7 Segment Display with Driver IC.

6.Multiplexed Seven Segment Display

The final output has also been shown in the multiplexed seven segment display. It's because the value cannot be shown in one display. So the multiplexing technique is used. It is a very common technique. Fig.16 has shown the multiplexing technique of 7 segment displays.

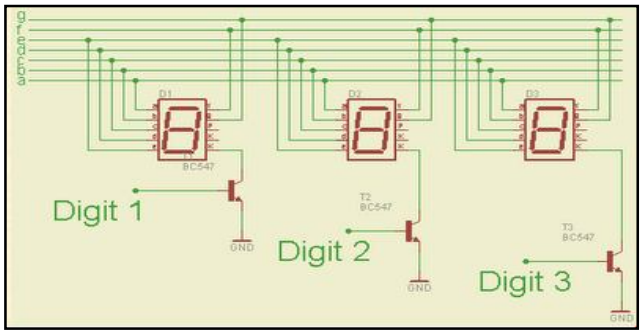

Figure 16: Multiplexing of 7 segment display

The hardware based desigened also tested and shown good performance over the basis of speed. Fig. 17 shows the pictorial view of the speedometer. From the picture ,it is seen that the wheel is moving and the multiplexed seven segment display shows the value of speed. Here, the speed is first detcted by hall sensor(not in picture) the fed this value to the smart fusion FPGA (shown in picture). Then after processing, the value of speed is shown by the displays.

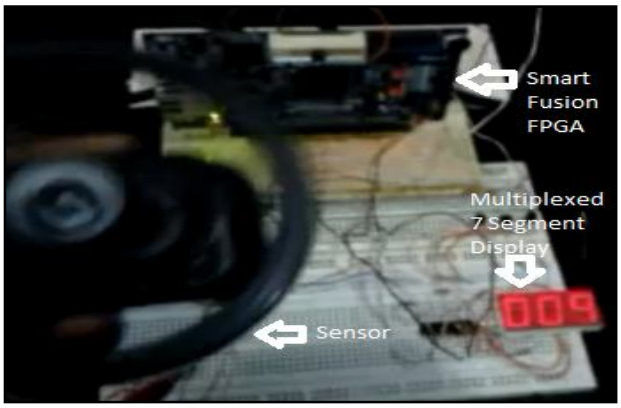

Figure 17: Implementation of Digital Speedometer.

7.Conclusion

A real time design and implementation of digital speedometer using FPGA is presented in this paper. We have used FPGA to get more flexibility result. As it is well known that FPGA device can be reprogrammed to do any logic task that can be fitted into the number of gates that it has. However FPGA based speedometer can be used in many areas. Many extra features can easily be added to this digital speedometer. Though this speedometer can be a little costly than existing speedometer in real life but this speedometer can give a large amount of features than others as described in introduction.

Moreover, this designing system not only the restraints in analogy circuit can be relaxed but also better speed and higher flexibility can be obtained using Verilog HDL than any other design technique.

8.Reference

1. N. Wadhwani, "Digital Speedometer," Electronics Projects Vol. 19, pp. 143-144.
2. T. Kaneko,T. Ohkubo, Y. Kurihara, K. Kobayashi., "Experimental study on wind-based vehicle speedometer applying the whistle principle", ICCAS-SICE, 2009, pp. 5600 - 5604.
3. J. H. Song, N. T. Thuy, S. Jin, D. Kim, J. W. Jeon, "An FPGA-based vehicle speed measurement system using an uncalibrated camera," ICCAS, 2010, pp. 1691 - 1696.
4. SmartFusion FPGA details: http://www.actel.com/FPGA/SmartFusion.
5. S. Palnitkar; "Verilog HDL.", Sunsoft Press, 1996.
6. J. Bhaskar, "VHDL primer.,3rd Edition," Pearson Education Asia Publications, 2000.
7. G. Gannot, M. Ligthart, "Verilog HDL based FPGA design," International Verilog HDL Conference, 1994, pp. 86 – 92.
8. Sheikh Md. Rabiul Islam, R. Sarker, S. Saha, A.F.M.N. Uddin, "Design of a programmable digital IIR filter based on FPGA," International Conference on Informatics, Electronics & Vision (ICIEV), 2012, pp. 716 - 721.
9. K.L. Dickinson, "An introduction to high resolution patterned magnetoresistive sensors and their application in digital tachometers," Annual Pulp and Paper Industry Technical Conference,1994, pp. 31-36.
10. J.H. Gu, C.Y. Song, S.Y. Lee, "A new velocity measurement method using linear type Hall-effect sensor for an electro-mechanical fin actuator," Annual Conference SICE, 2007, pp. 2179 – 2183.
11. Kennedy and G. Stuart, "Writing messages on 7-segment displays," *Electronic Systems News* , vol.1988, no.2, pp.6-9.
12. Sheikh Md. Rabiul Islam, A. F. M. Nokib Uddin "Design of LMS algorithm for noise canceller based on FPGA" International Institute for Science, Technology and Education (IISTE) Academic Journal Computer Engineering and Intelligent Systems (CEIS) ,December 30, 2012.Page1-12 ISSN 2222-1719 (Paper) ISSN 2222-2863 (Online).
13. Sheikh Md. Rabiul Islam, Md. Jobayer Hossain, "Gate Level Design of a Digital Clock with Asynchronous-Synchronous Logic" Global Journal of Researches in Engineering (*GJRE)*, Volume 12 Issue 4*: Page 17-22.*Apr 03, 2012 Online ISSN: 2249-4596 & Print ISSN: 0975-5861.
14. Sheikh Md. Rabiul Islam, A. F. M. Nokib Uddin, Md. Billal Hossain, Md. Imran Khan "FPGA based Heart Arrhythmia's Detection Algorithm" International Journal

of Information Technology, Issue. 4, Vol. 2, December 2012. Publisher: ACEEE, USA(a division of IDES), ISSN 2158=012X(print); ISSN 2158-0138(Online).

15. Sheikh Md. Rabiul Islam, Shumit Saha, Md. Imran Khan "FPGA Based Digital System for Detection of Dicrotic Notch in the Carotid Pulse Signal" International Journal of Information and Communication Technology Research Vol.2 No.12, December 2012. (ISSN 2223-4985)
16. Sheikh Md. Rabiul Islam, Robin Sarker, Md. Sahib Monsur Hossain "Design a digital system for detection of abnormality condition of heart from ECG waveforms" Computer and Information Technology (ICCIT), 2011 14th International Conference on , pp.24-29, 22-24 Dec. 2011, Bangladesh.