8 BIT A.L.U

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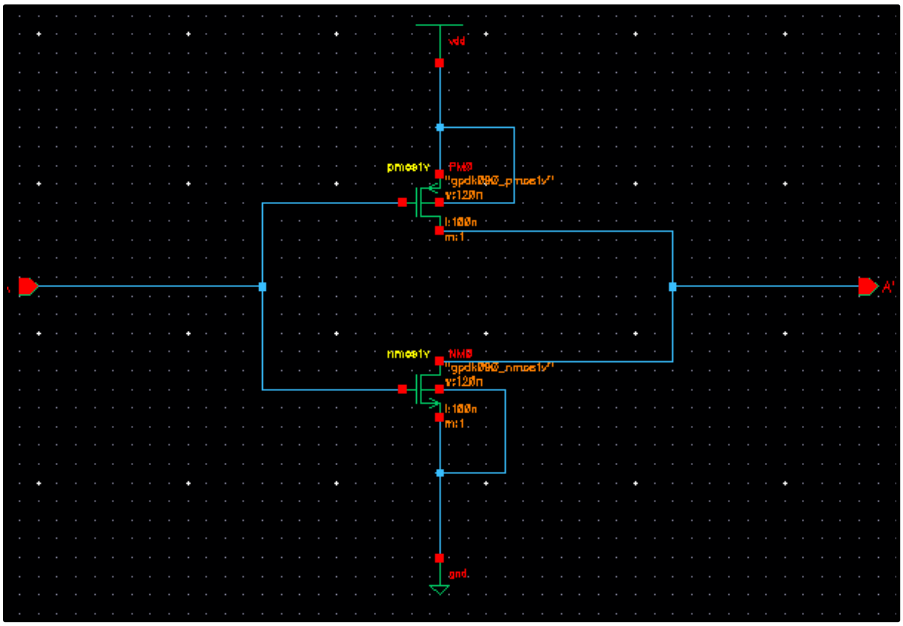
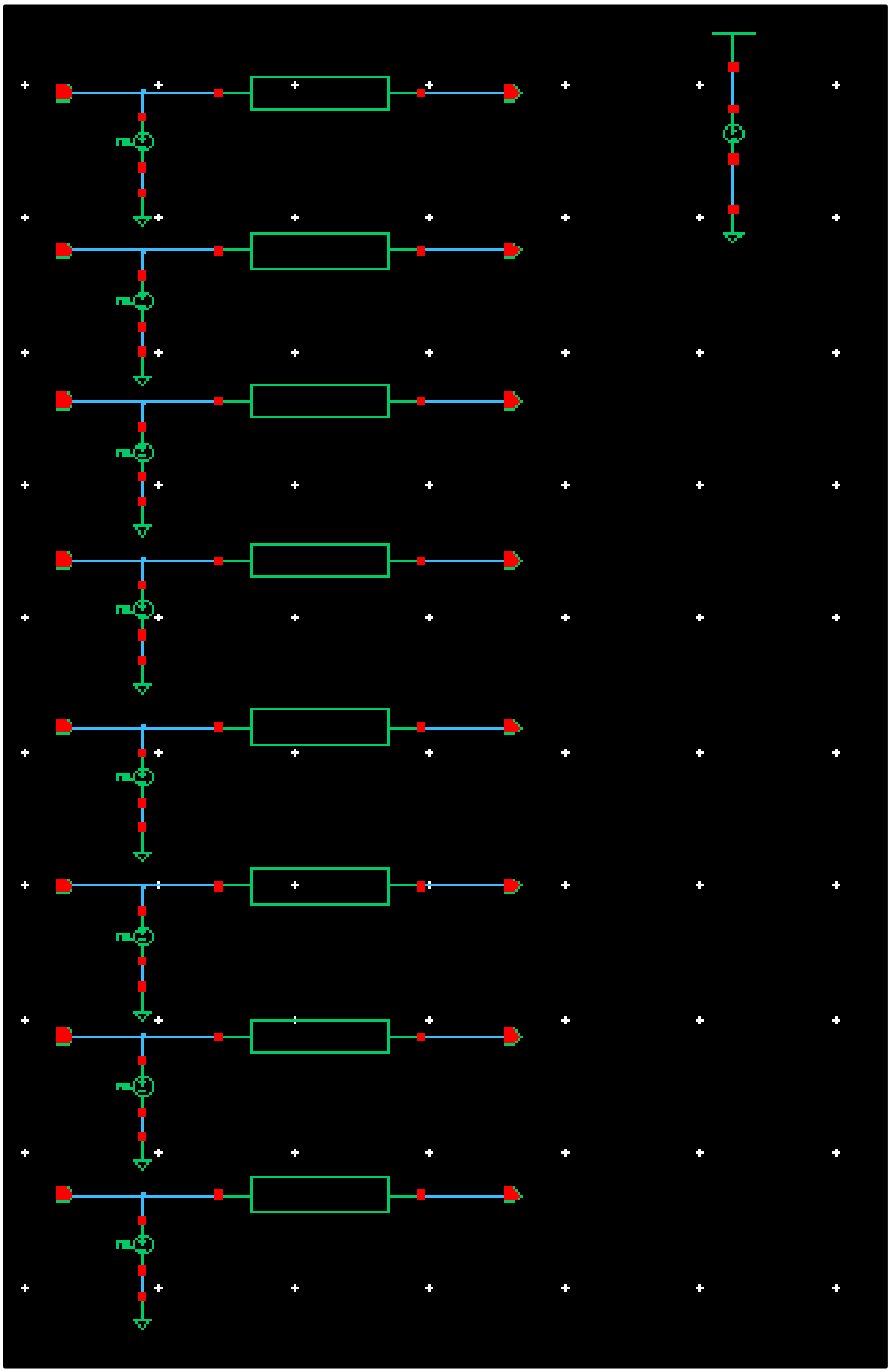
1) NOT GATE: -

❖ Schematic



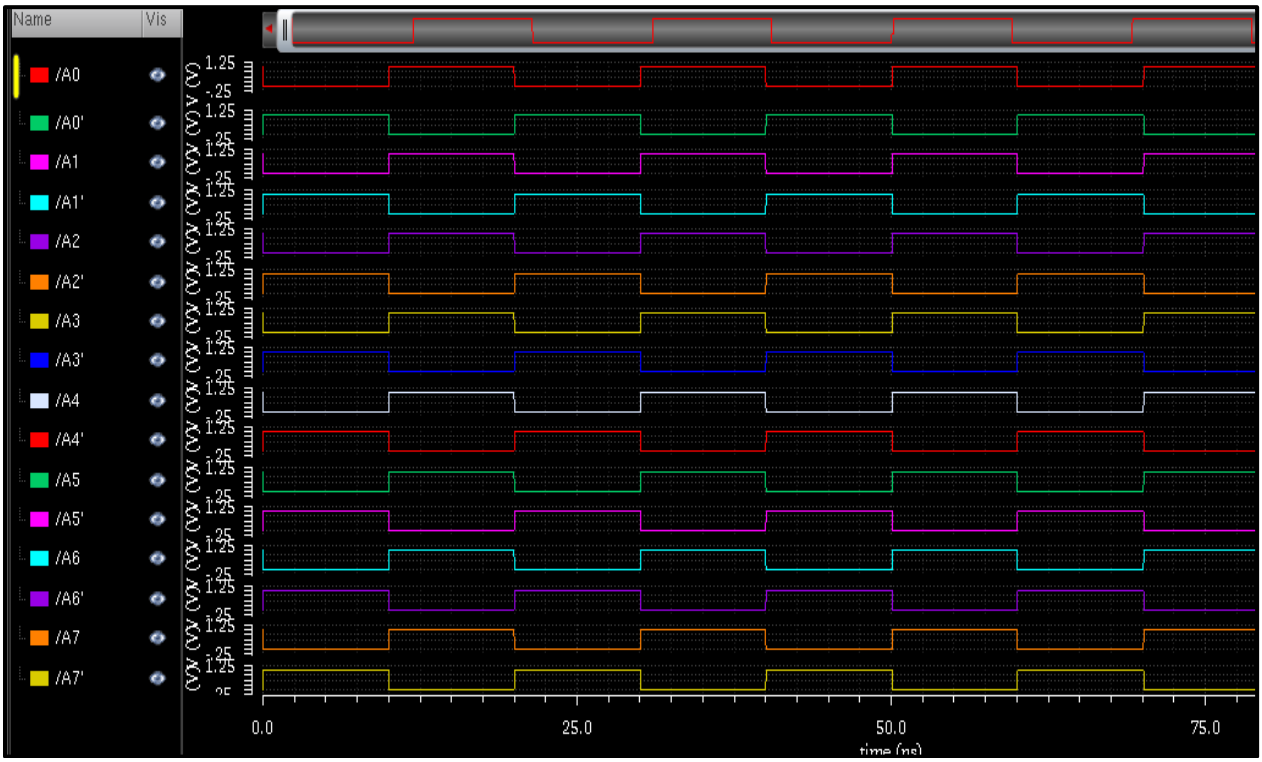
- CMOS Logic had been used in the circuit.
- Body/substrate of the MOSFET are connected to the source to avoid the body effect (either increase or decrease in threshold Voltage).

❖ Test Bench



(Test Bench – 8 Bit)

❖ Output

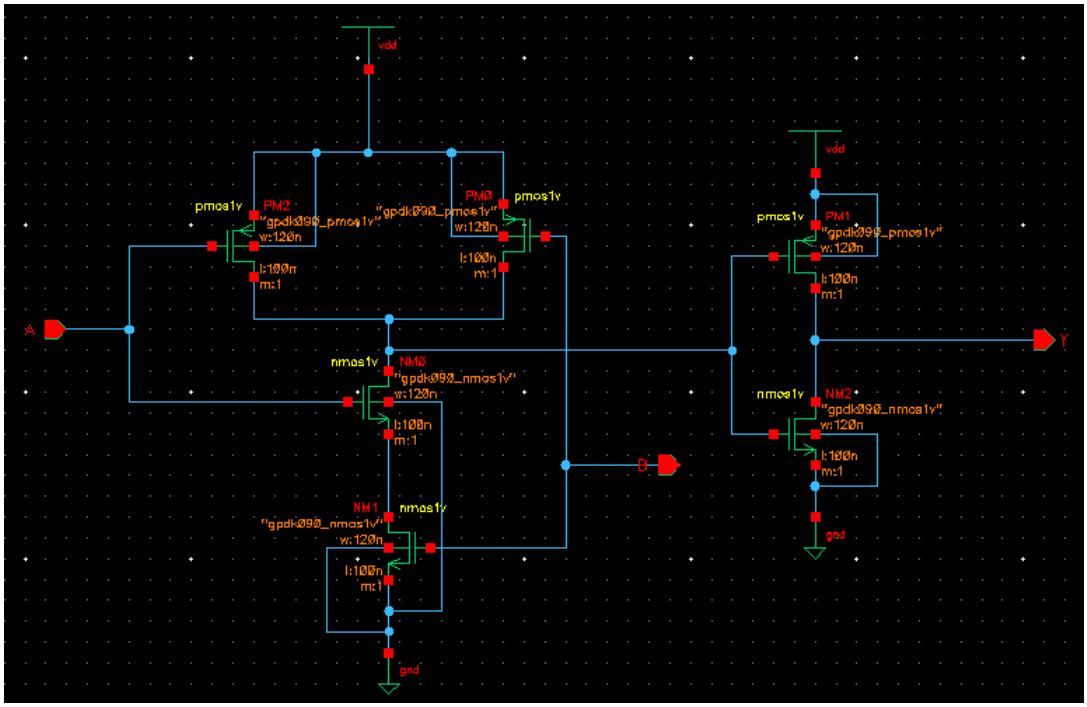


(Output – 8 Bit)

A	Pull-Up	Pull-down	A′
0	1 (Good 1)	Z	1
1	Z	0 (Good 0)	0

2) AND GATE: -

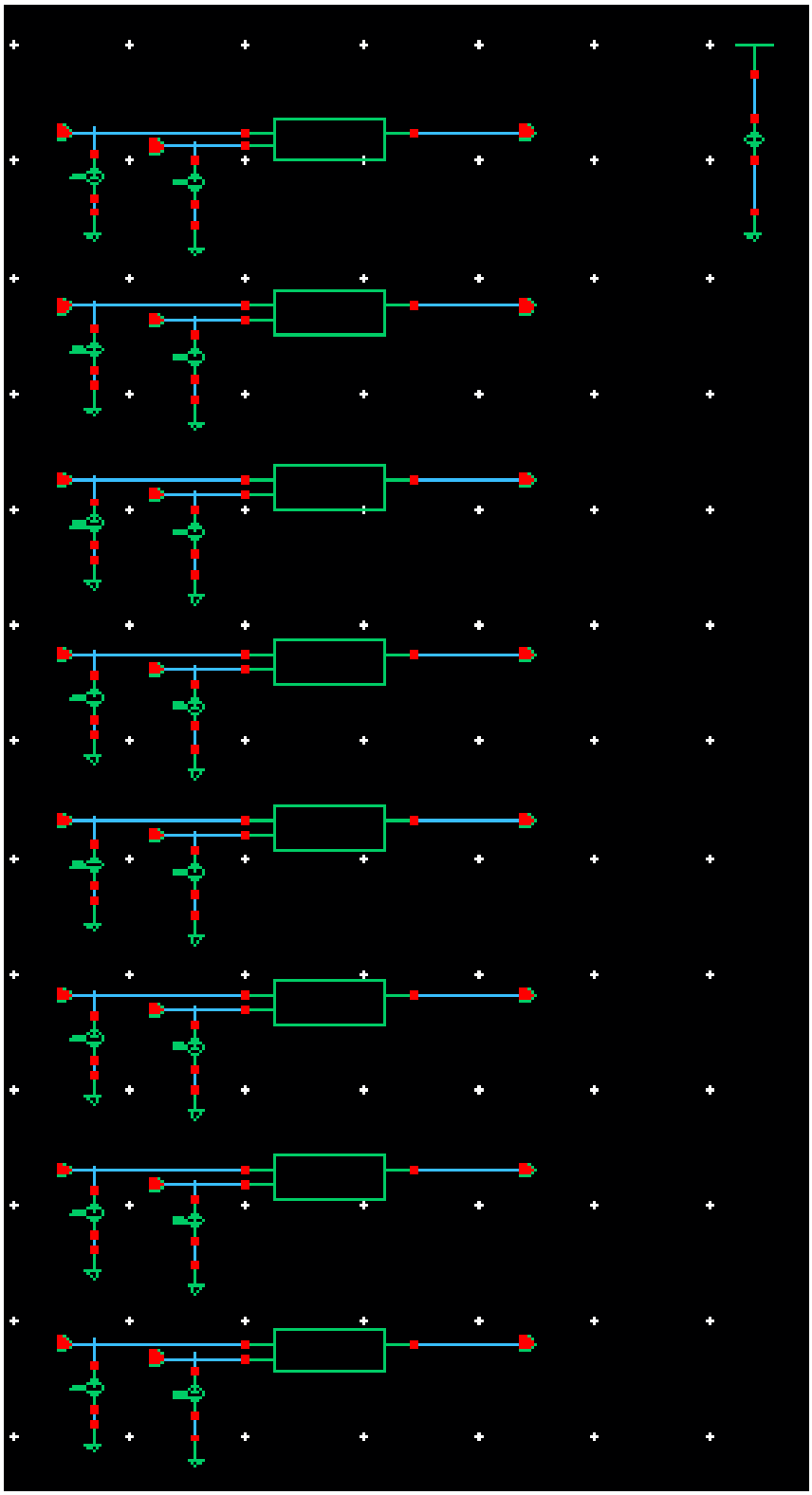
❖ Schematic



- CMOS logic had been used in the following circuit.
- AND logic had been created using the NAND and NOT logics.
- Output of NAND logic had been inverted using the NOT logic.

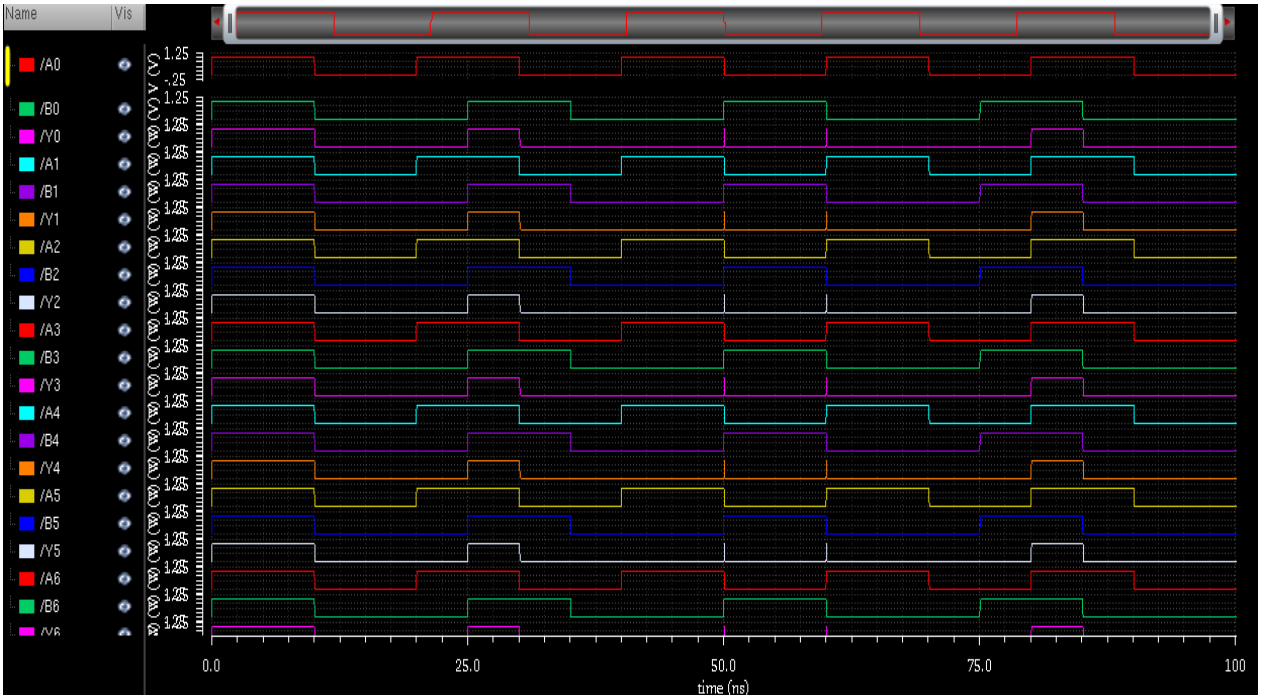
A	B	Pull-up	Pull - down	V_o (NAND)	Y
0	0	1	Z	1	0
0	1	1	Z	1	0
1	0	1	Z	1	0
1	1	Z	0	0	1

❖ Test Bench

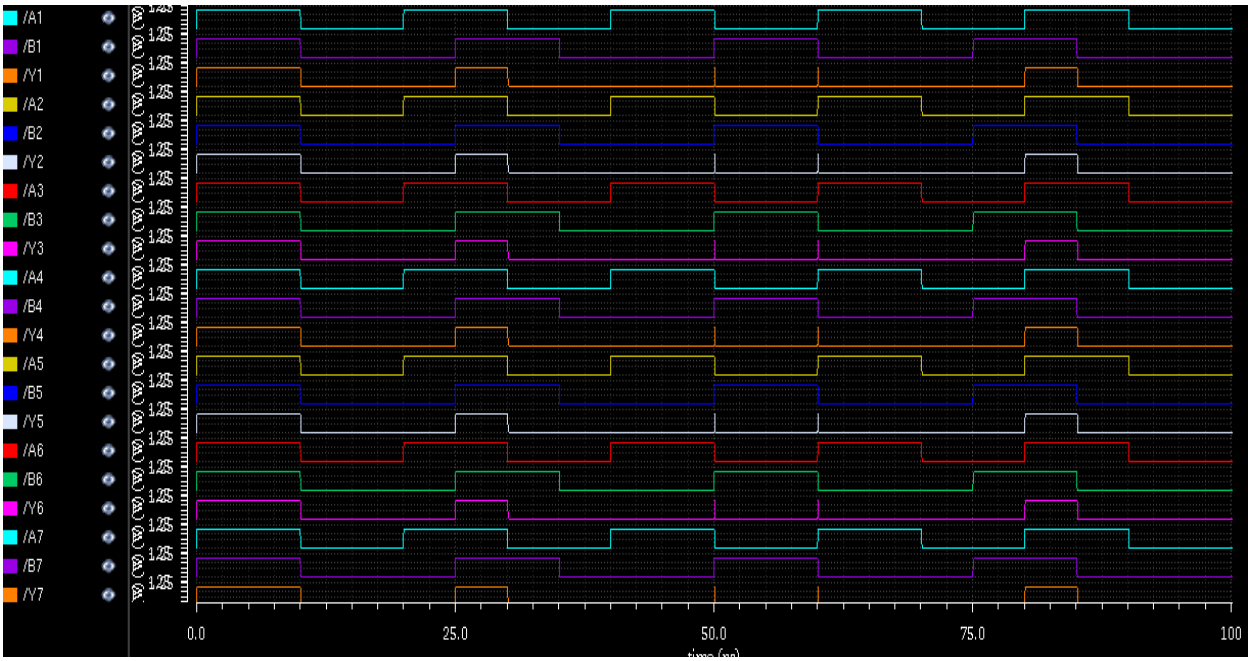


(Test Bench – 8 Bit)

❖ Output



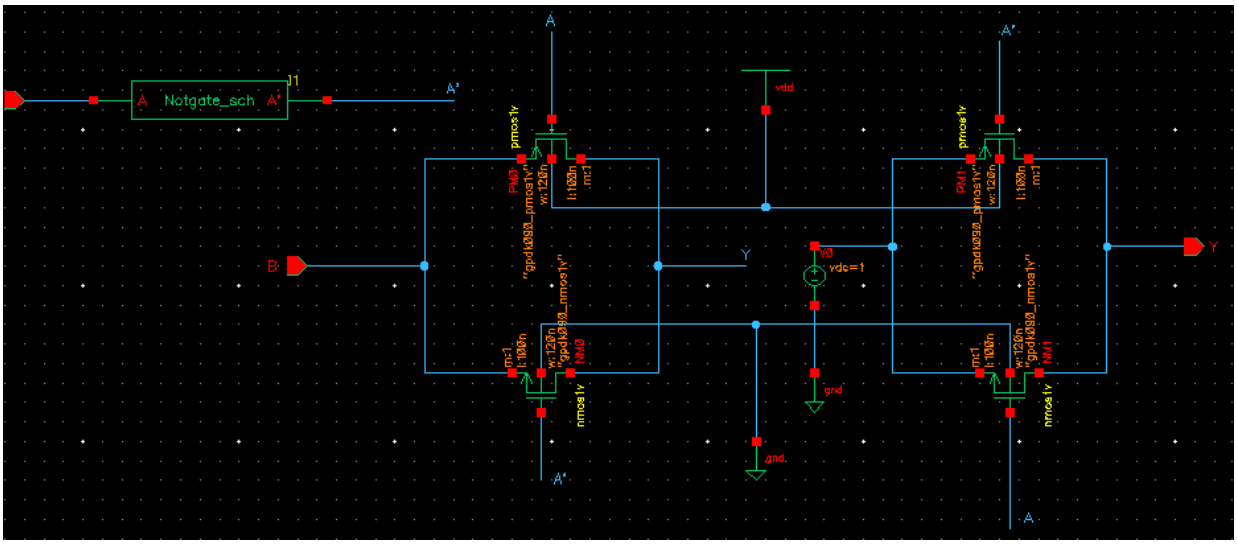
(Output – 8 Bit)



(Output – 8 Bit)

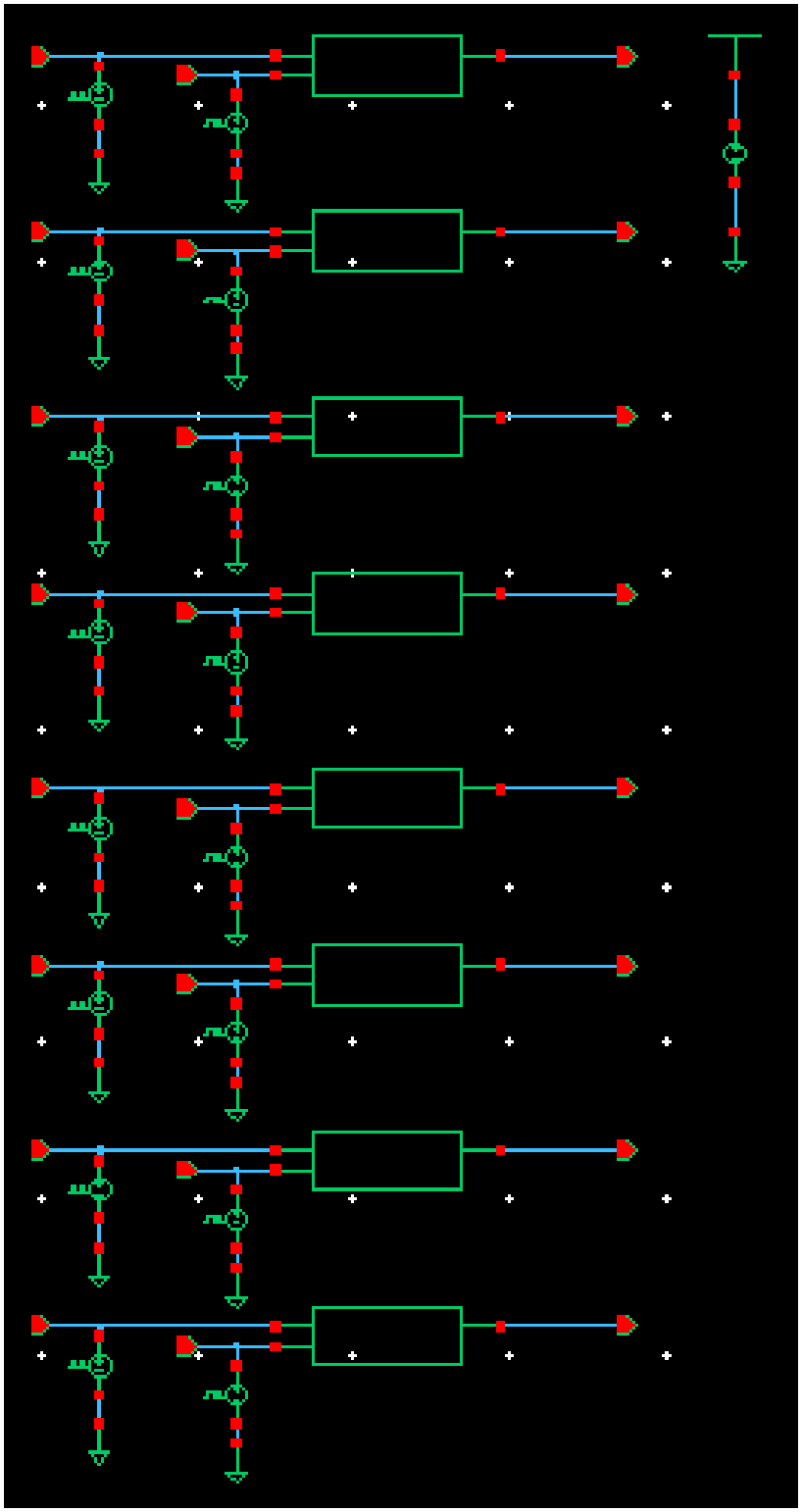
3) OR GATE: -

❖ Schematic



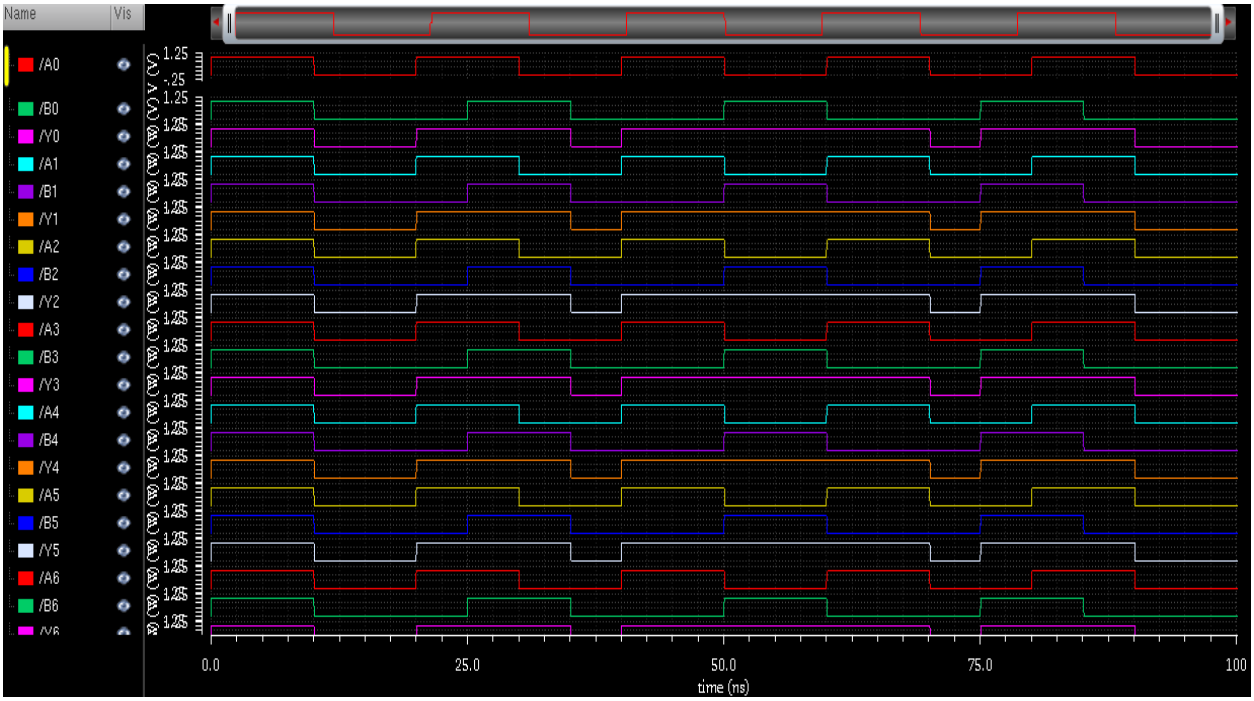
- Transmission logic had been used in the following circuit.
- Pin A is assigned as a control unit in the following circuit.
- If A=0, Y=0+B=0
- If A=1, Y=1+B=1

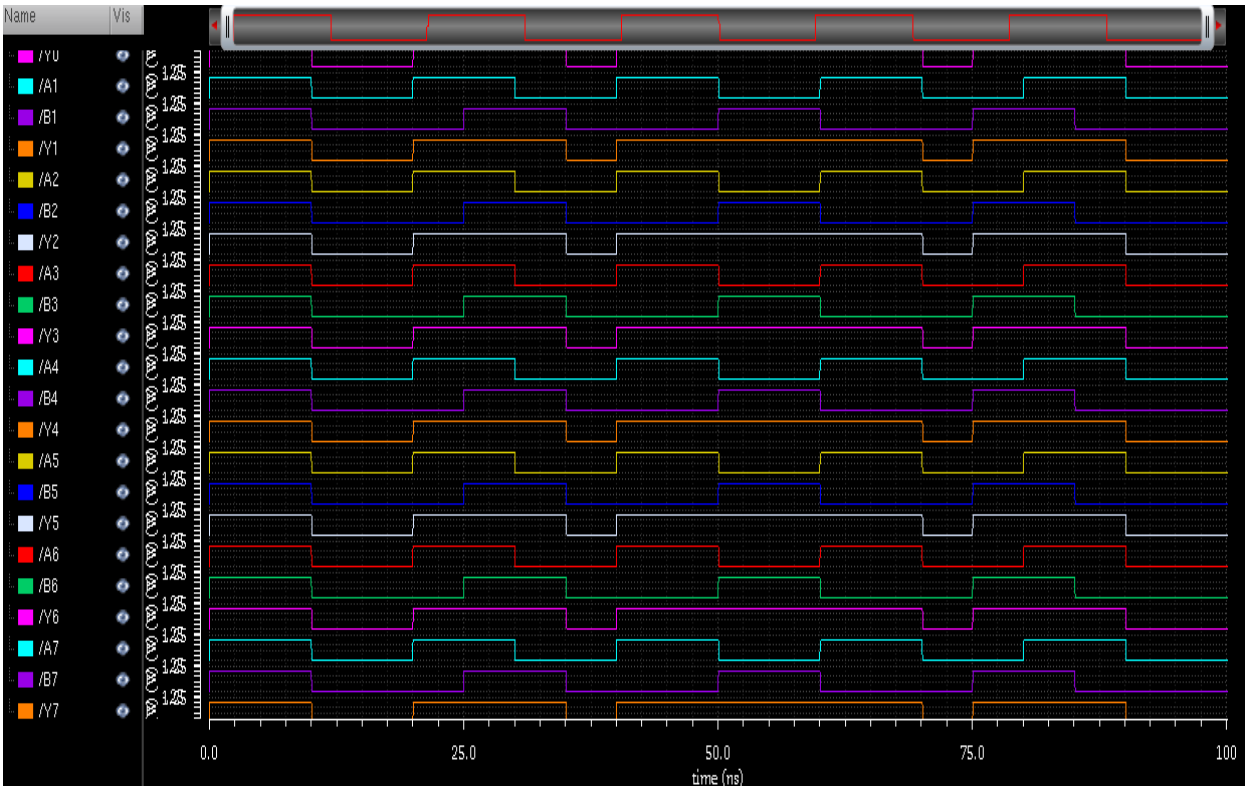
❖ Test Bench



(Test Bench – 8 Bit)

❖ Output

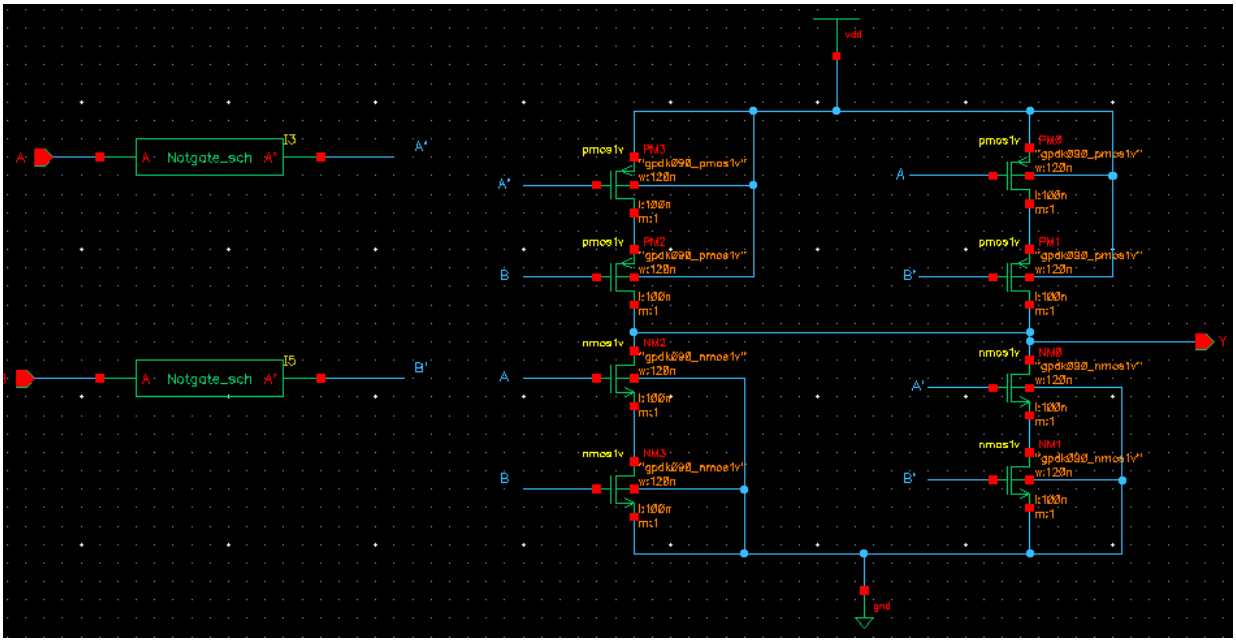




(Output – 8 Bit)

4) EX-OR GATE: -

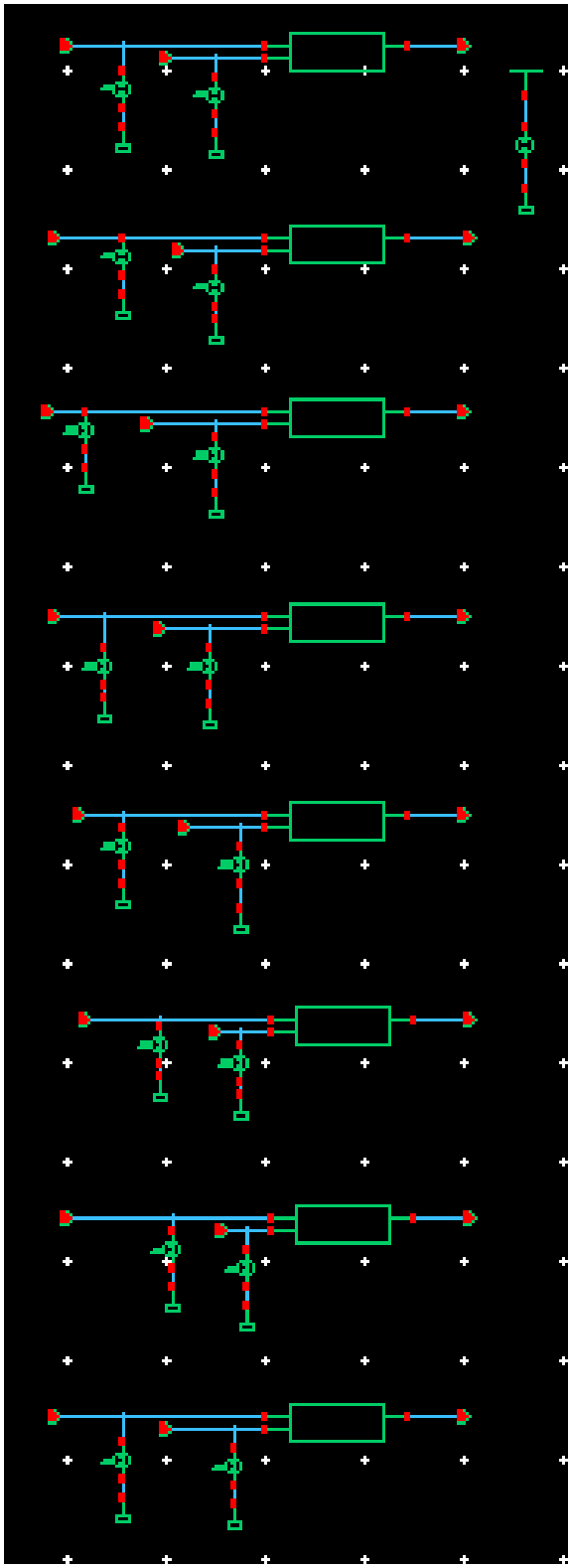
❖ Schematic



- CMOS logic had been used in the following circuit.
- XNOR logic had been created by inverting the output of XNOR logic.

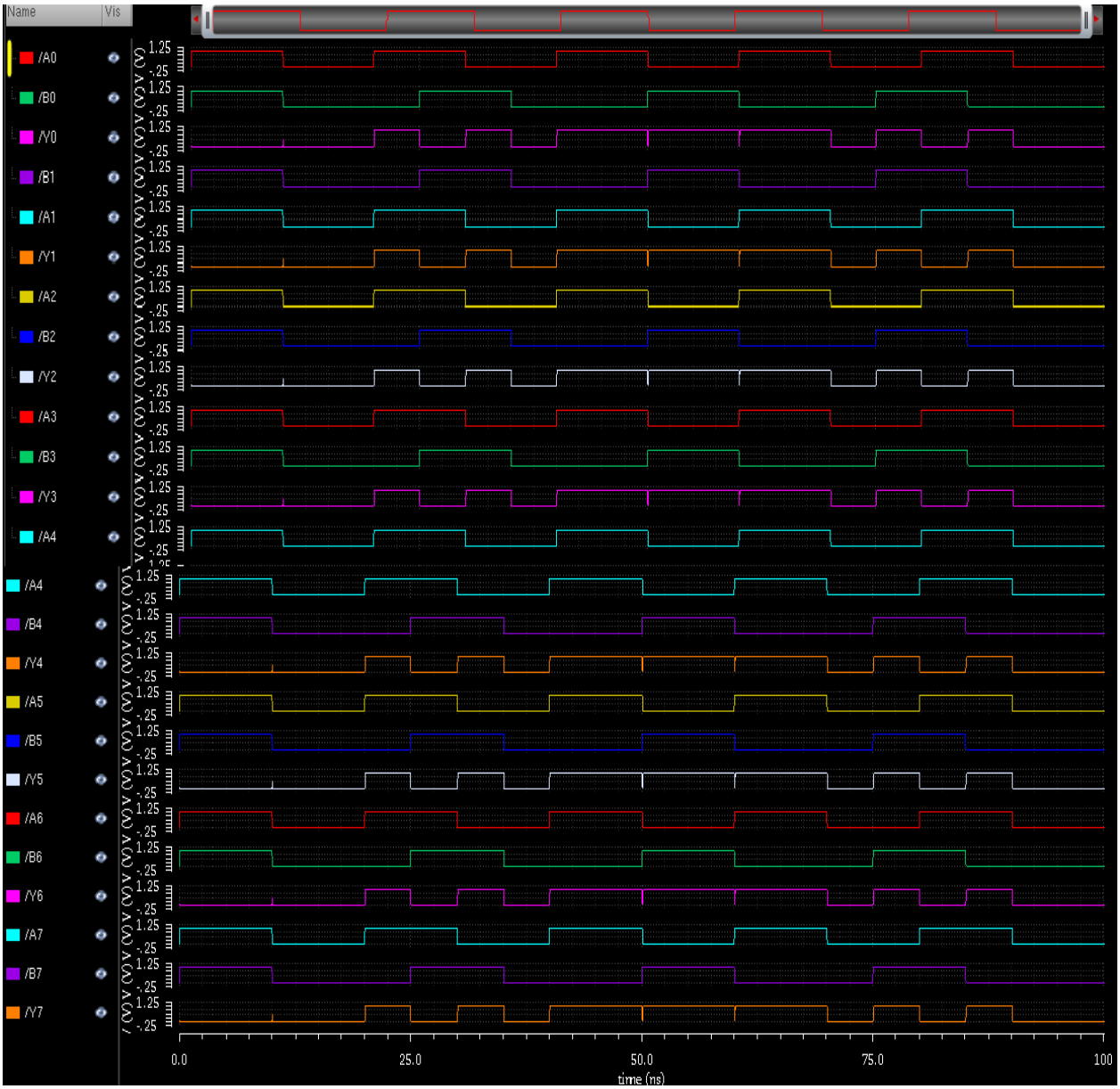
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

- ❖ Test Bench



(Test Bench – 8 Bit)

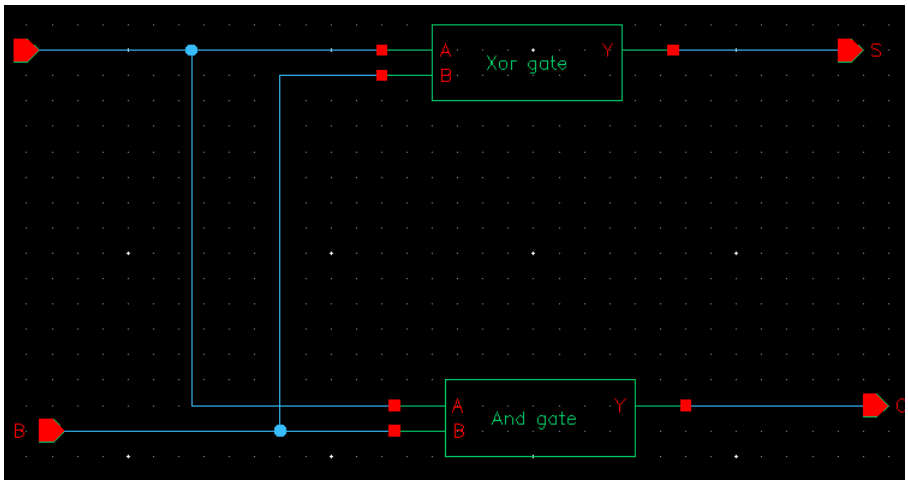
❖ Output



(Output –8 Bit)

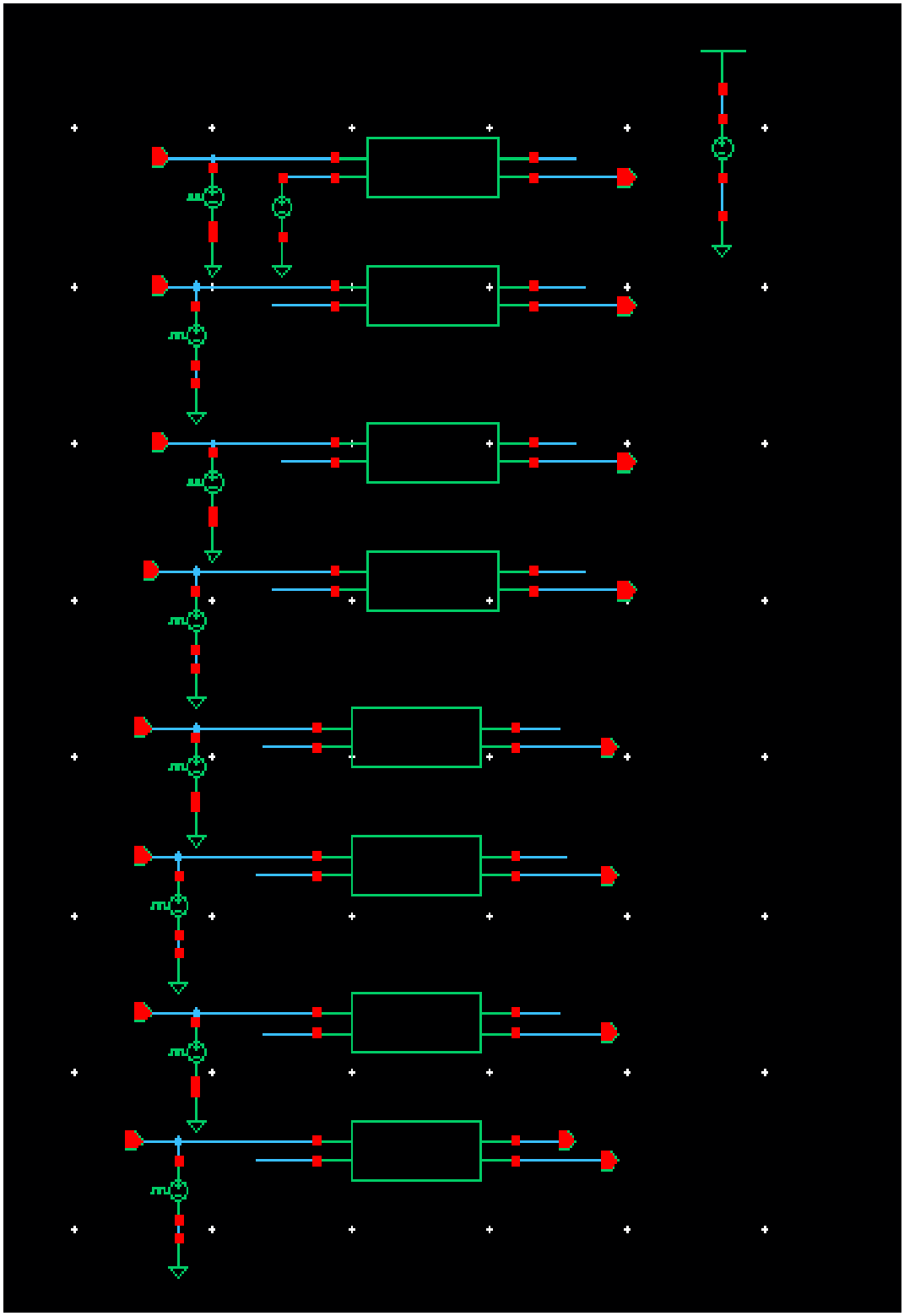
5) INCREMENT OPERATION

❖ Schematic



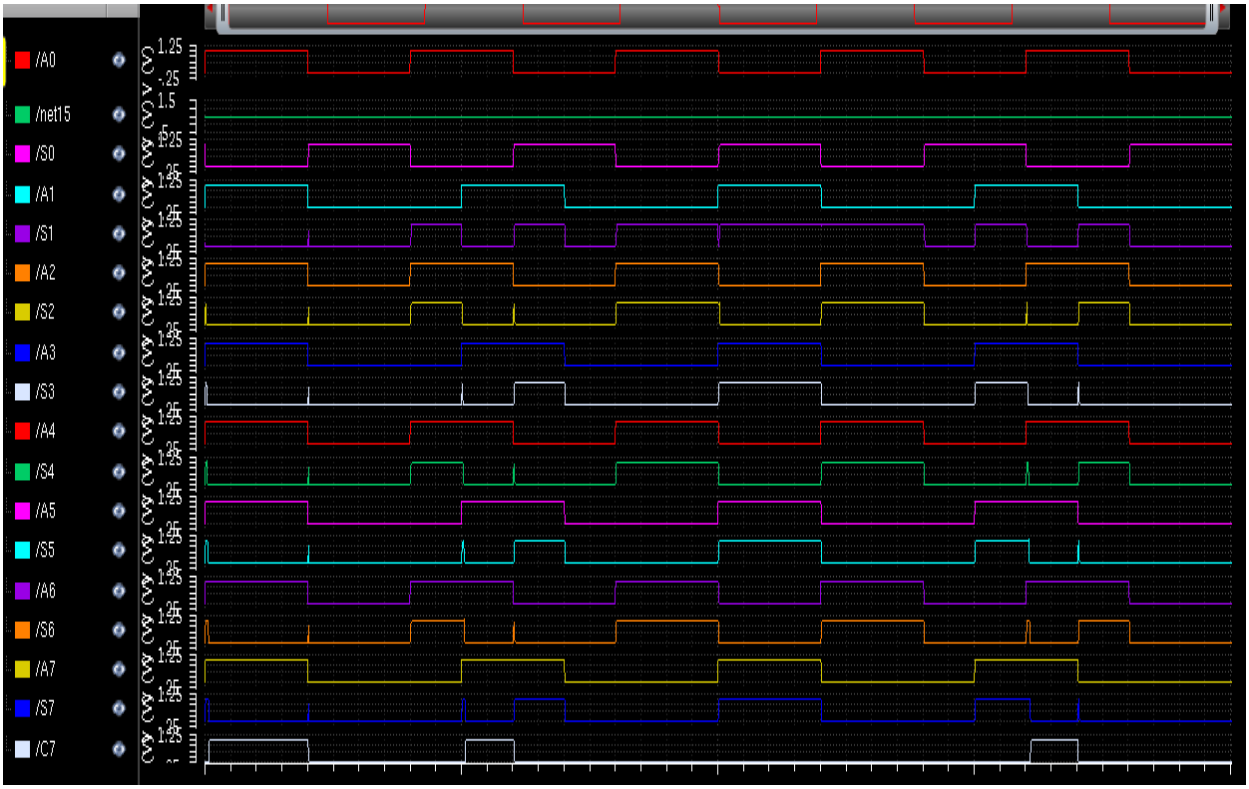
- XOR and AND gate had been used to create an Increment logic.
- Basically, a Half Adder had been created using these two gates.
- To follow an increment operation PIN B0 is set equal to 0; and the carry of each adder is transferred to PIN BX of other half adders (where X=1,2,3…...7)

❖ Test Bench



(Test Bench – 8 Bit)

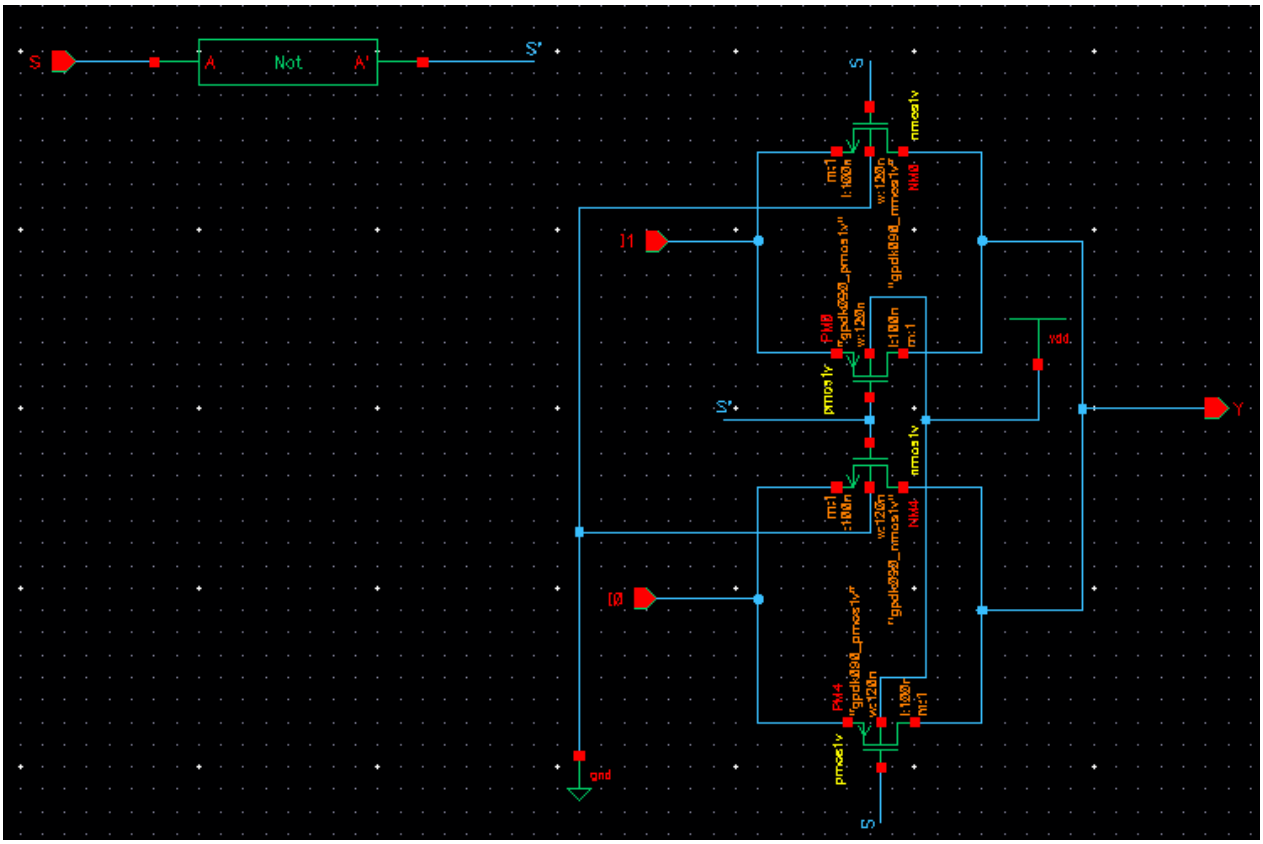
❖ Output



(Output – 8 Bit)

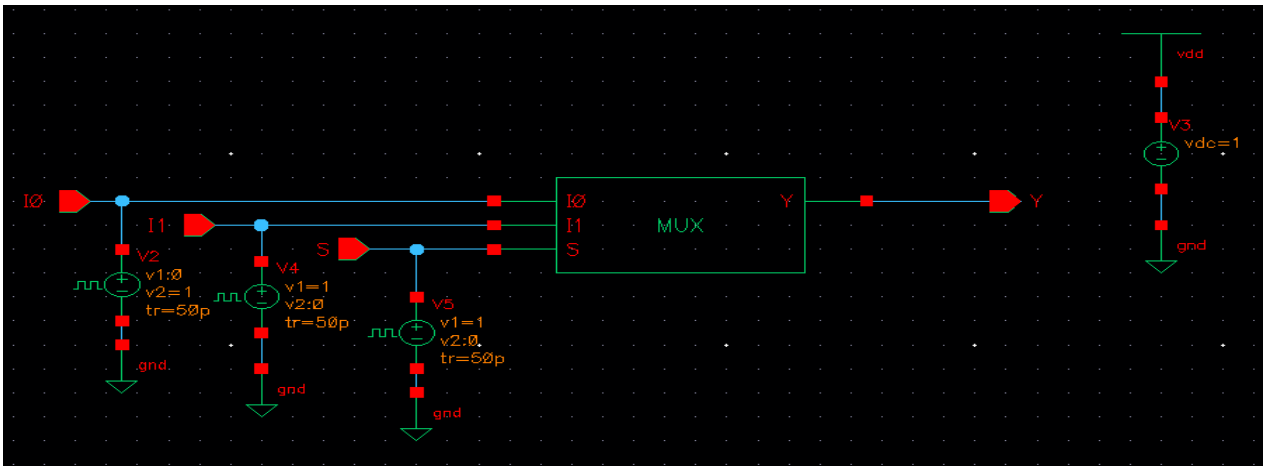
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

❖ Schematic



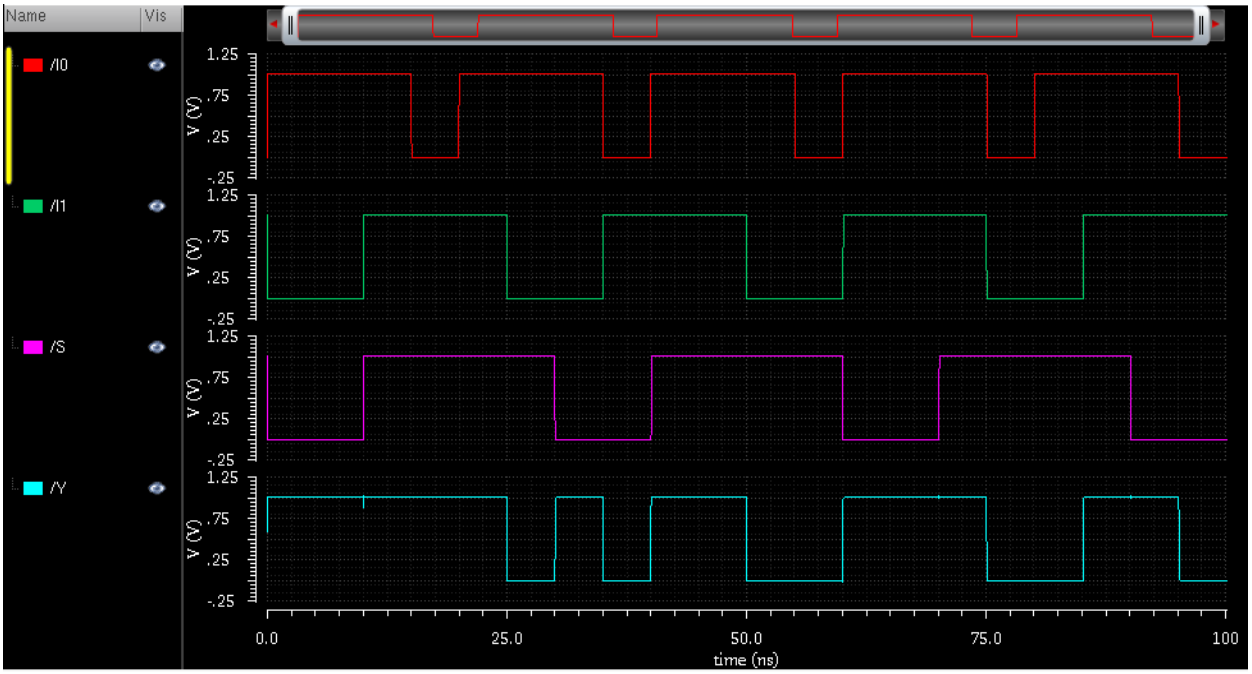
- Following logic had been created using the transmission logic.
- Select input S is assigned as a control unit.
- If S=0, Y=I0
- If S=1, Y=I1
- **Boolean Expression**: - I0S' + I1S

❖ Test Bench



(Test Bench – 1 Bit)

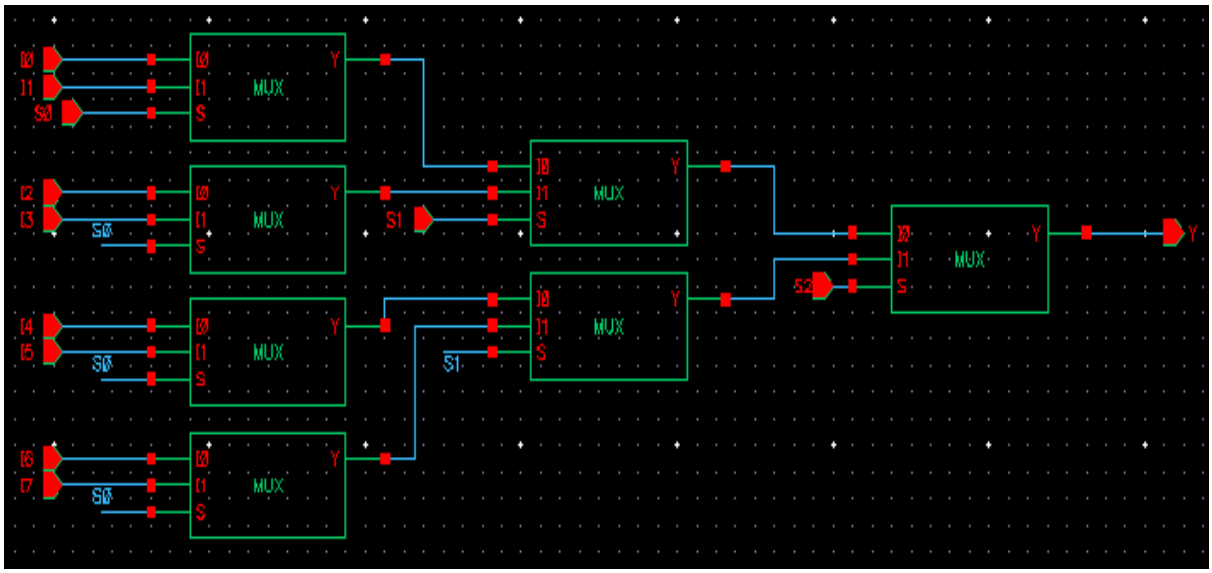
❖ Output



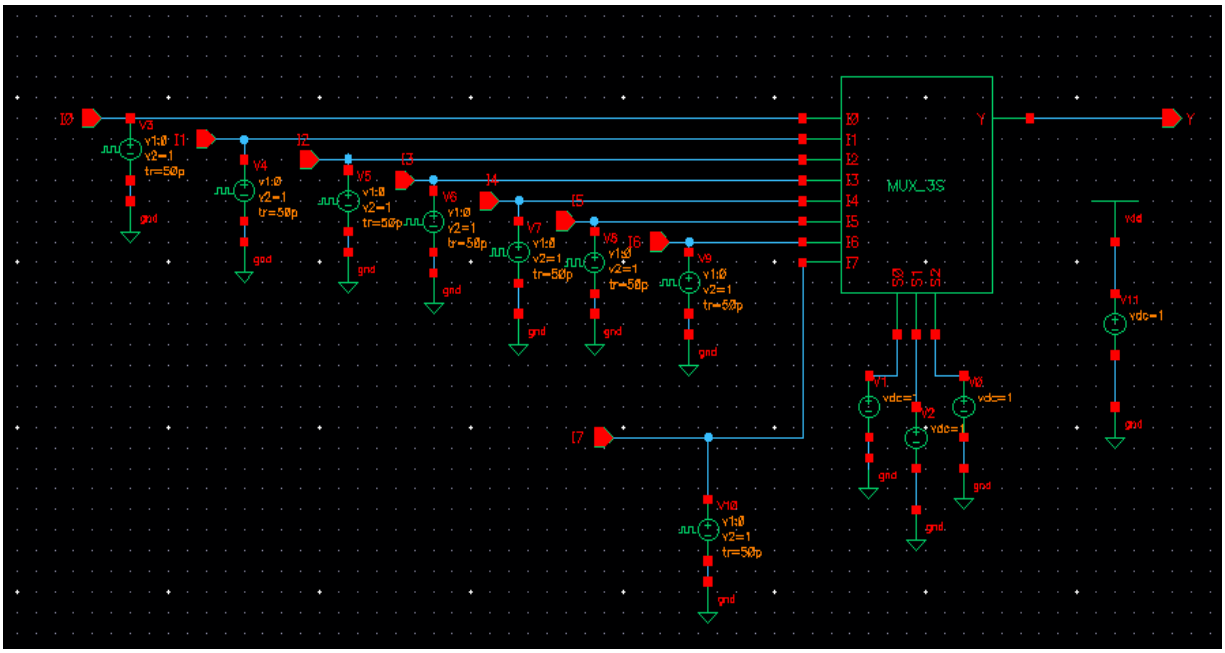
(Output – 1 Bit)

7) MUX (8:1)

- Schematic

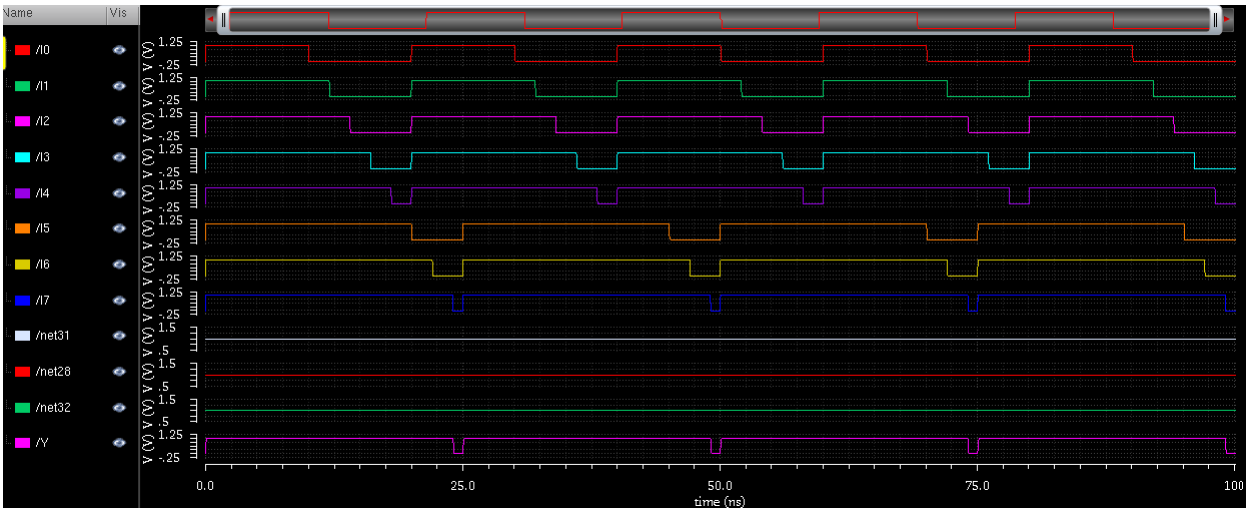


- Test Bench



(Test Bench – 8 Bit)

❖ Output

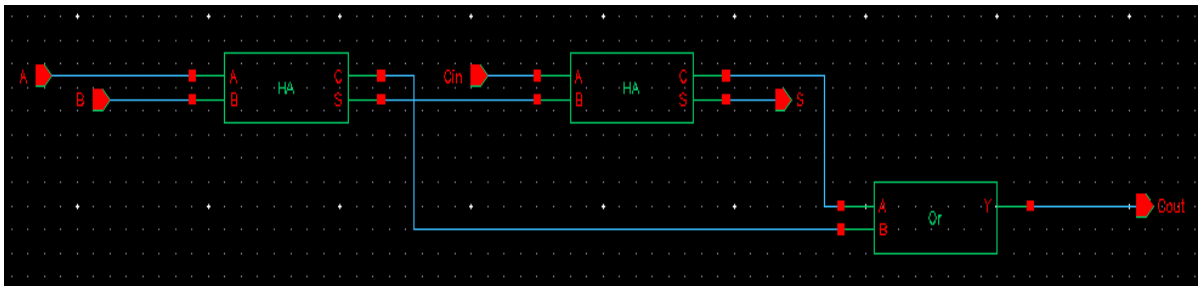


(Output – 8 Bit)
(When S2, S1, and S0 all are 1)

Here, I am showing only one output where all the select lines are set equal to 1. Rest, all the outputs could be tried as well by varying the select line inputs.

8) FULL ADDER

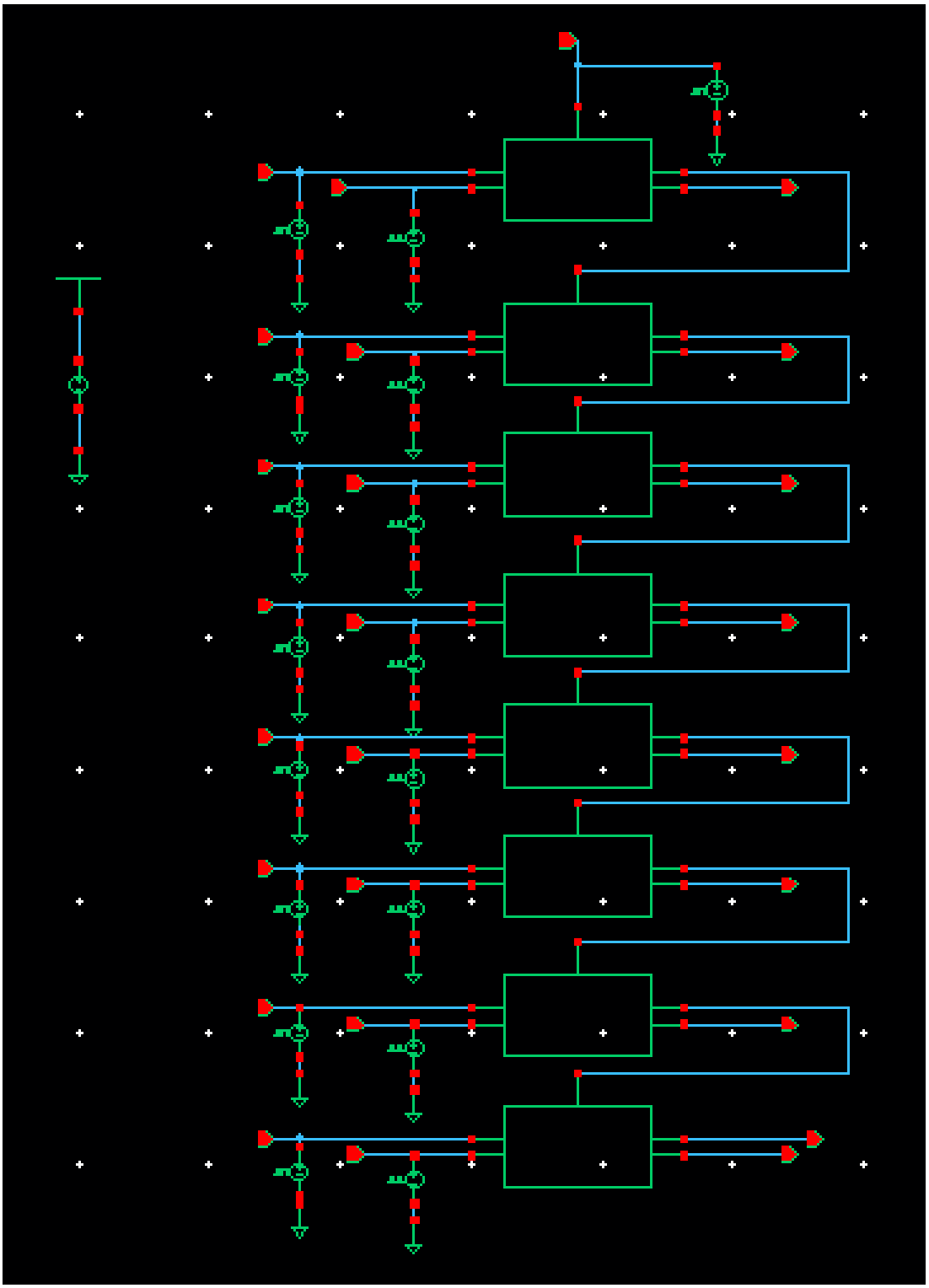
❖ Schematic



- Full Adder had been created using the two Half Adders and an OR gate.
- Pin S = XOR logic of all the 3 inputs (A, B, Cin).
- Pin Cout = Sum of all the AND logics that are formed by using 2 pins together at a time (AB, BC, CA).

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- ❖ Test Bench



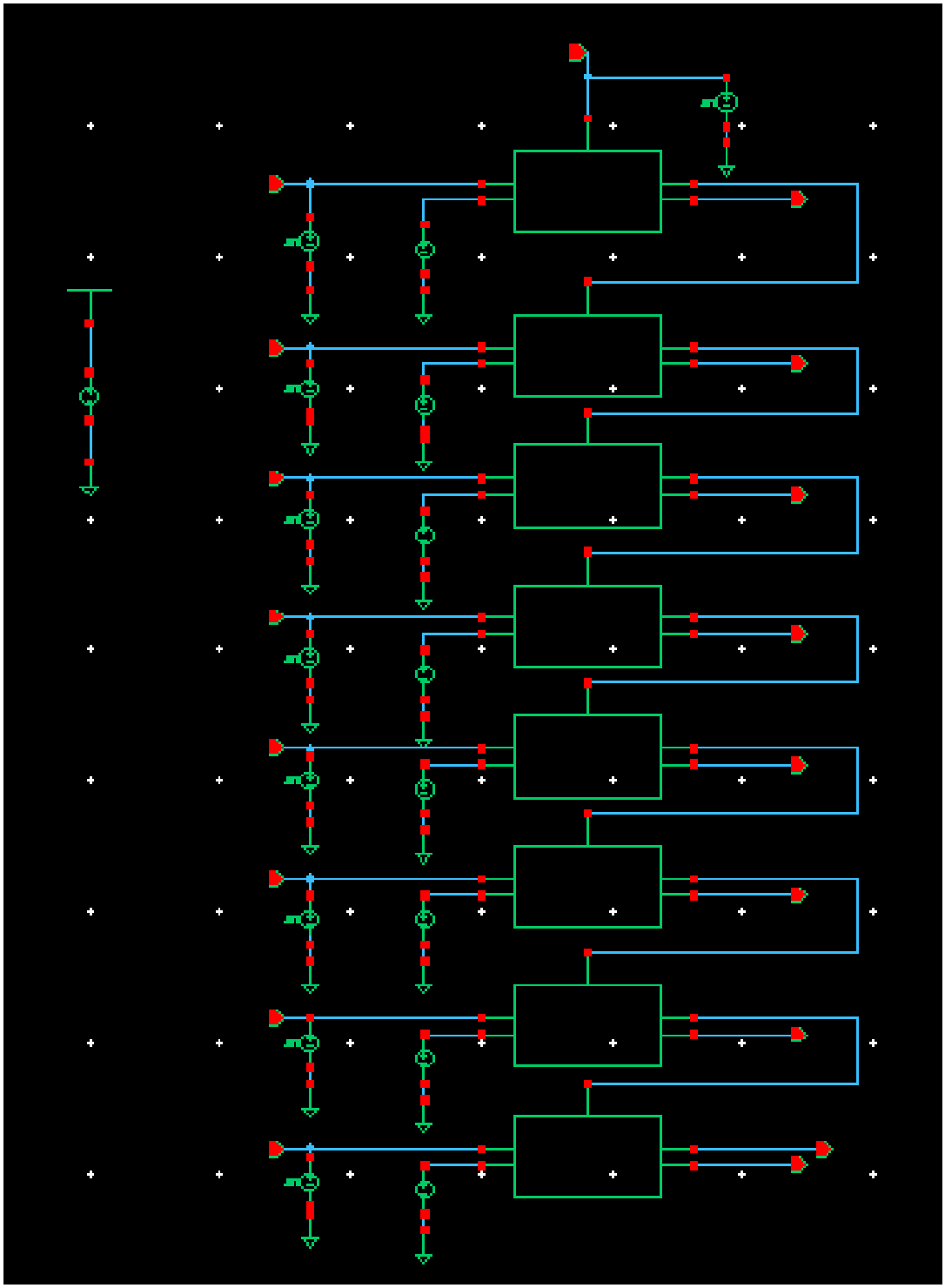
(Test Bench – 8 Bit)

❖ Output

(Output – 8 Bit)

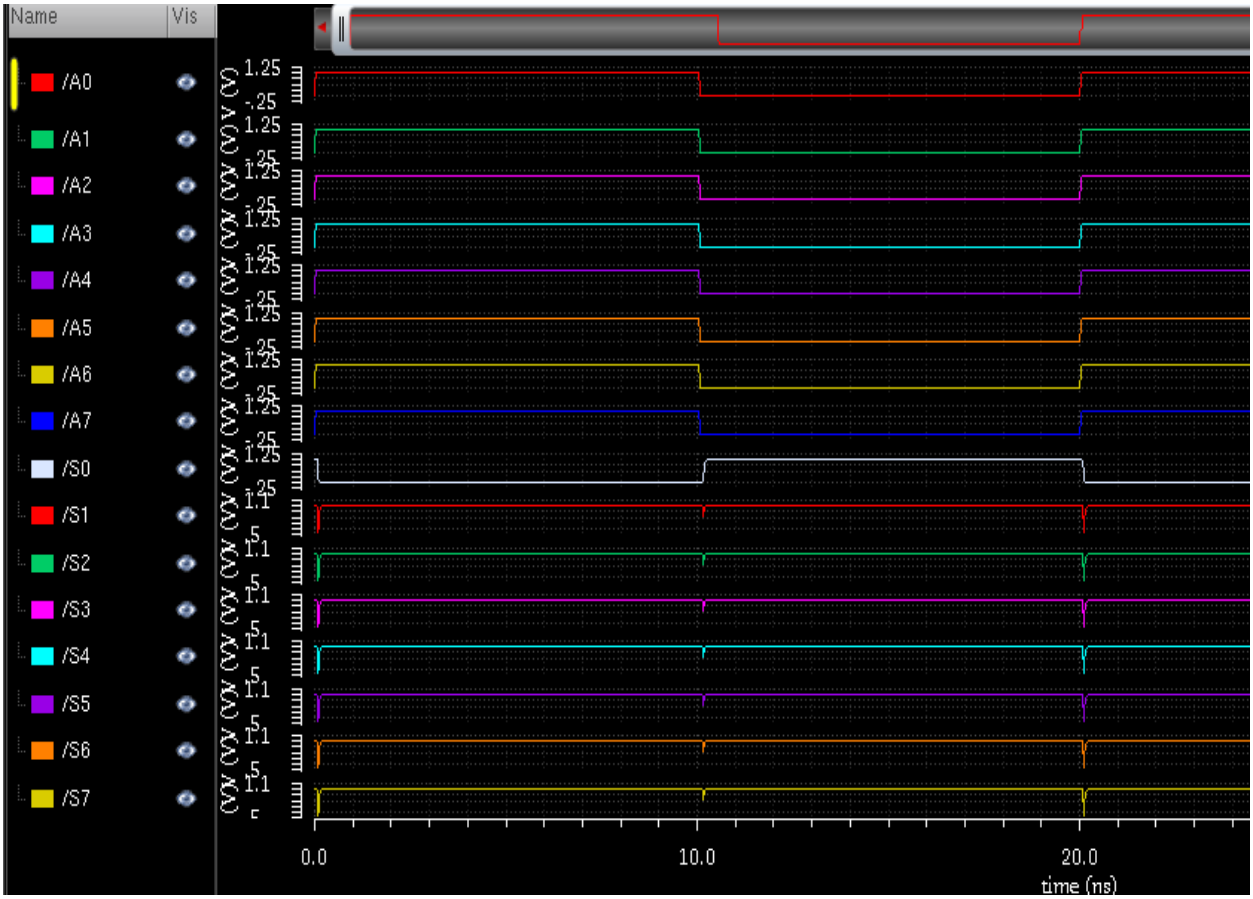
9) DECREMENT OPERATION (Designed using Full Adder Only)

- Test Bench



(Test Bench – 8 Bit)

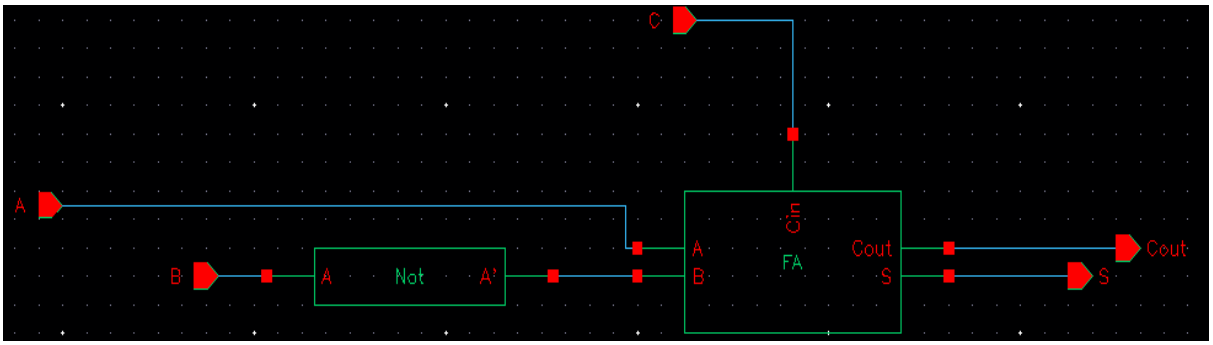
❖ Output



(Output – 8 Bit)

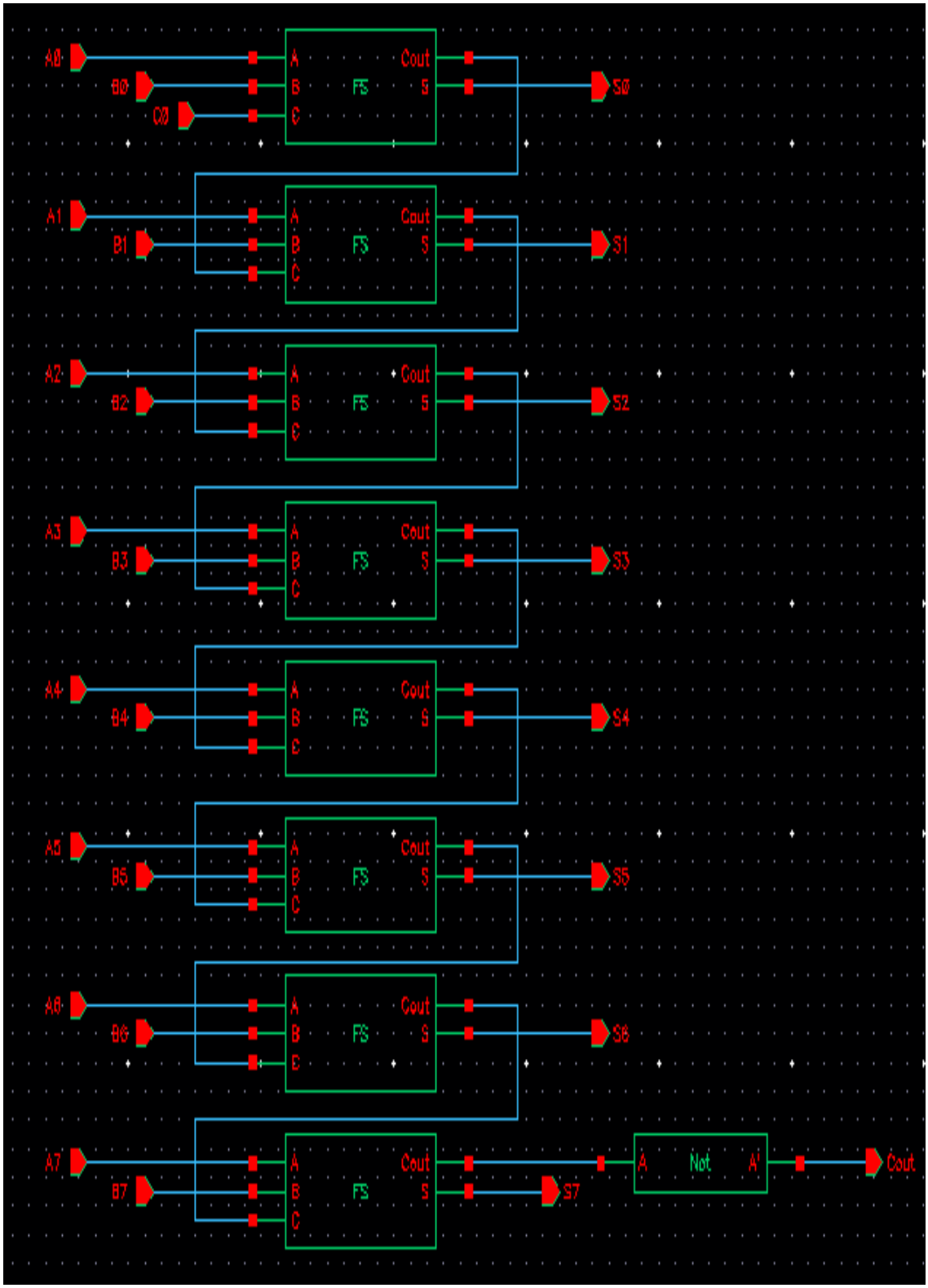
10) FULL SUBTRACTOR

❖ Schematic



- Full Subtractor had been created by complementing the input of PIN B before applying to the Full Adder.

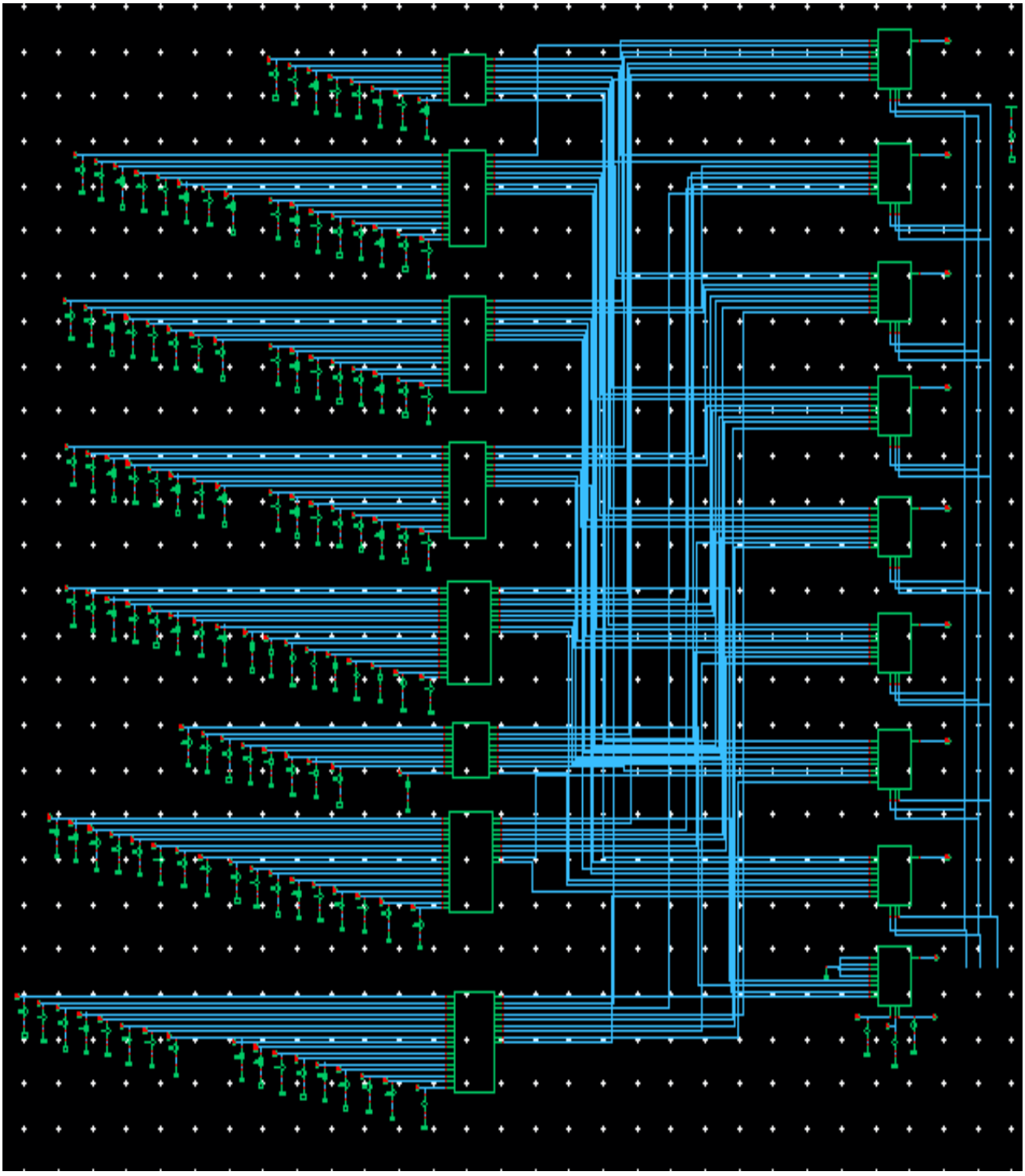
❖ Test Bench



(Test Bench – 8 Bit)

11) FINAL ALU

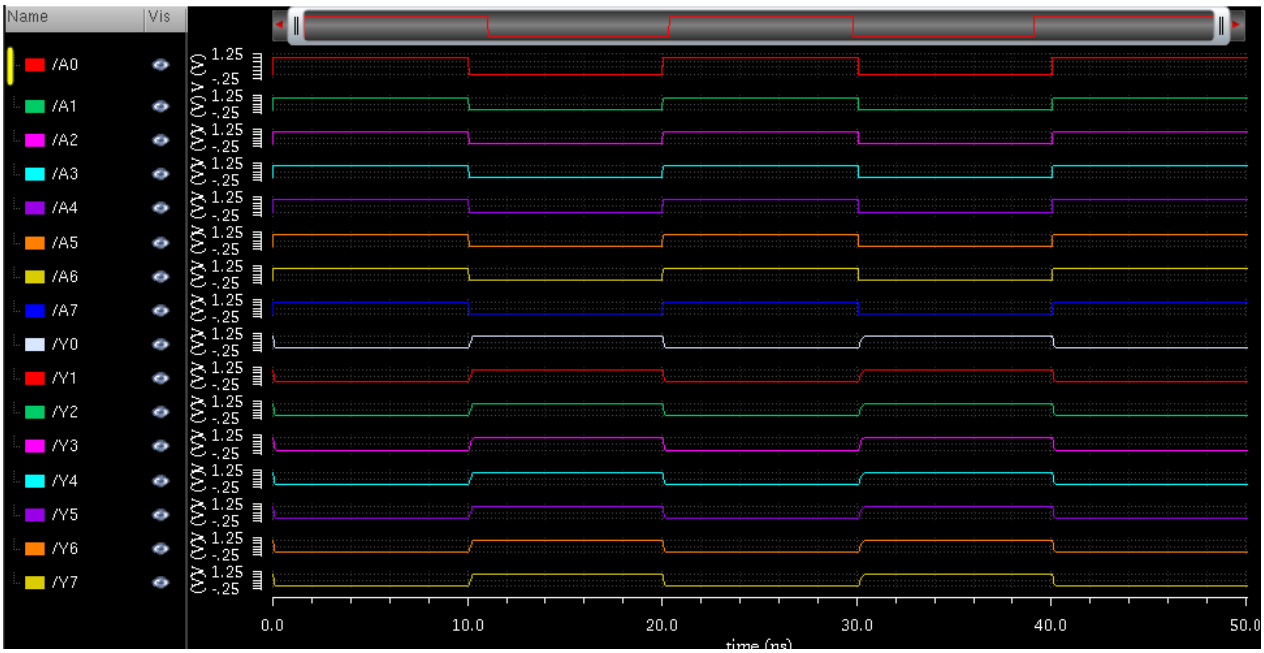
- Schematic



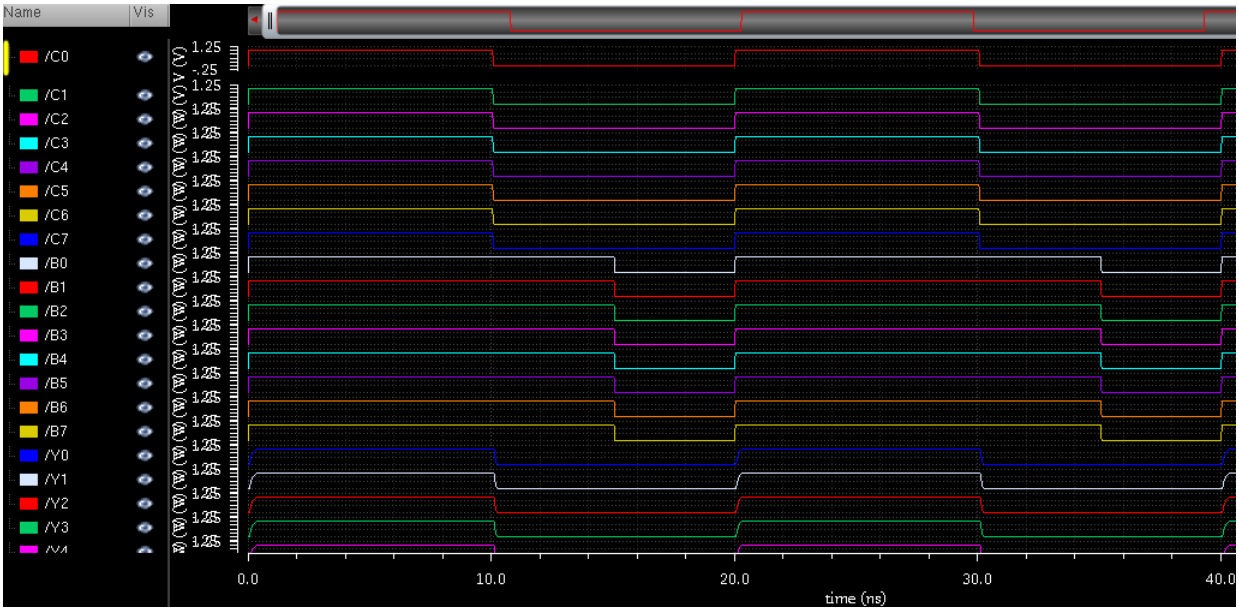
(8 BIT ALU)

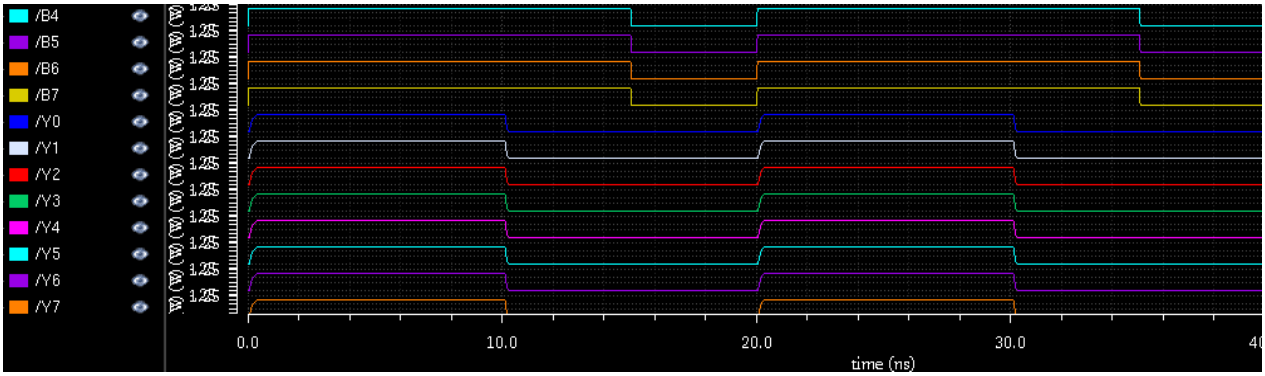
Some of the final test results are shown below: -

Case-1) When S2=S1=S0=0



Case-2) When S2=S1=0; S0=1





Case-3) When S2=1; S1=S0=0