8 BIT A.L.U

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Under the guidance of Mentor:-
Dr. Vandana Khanna

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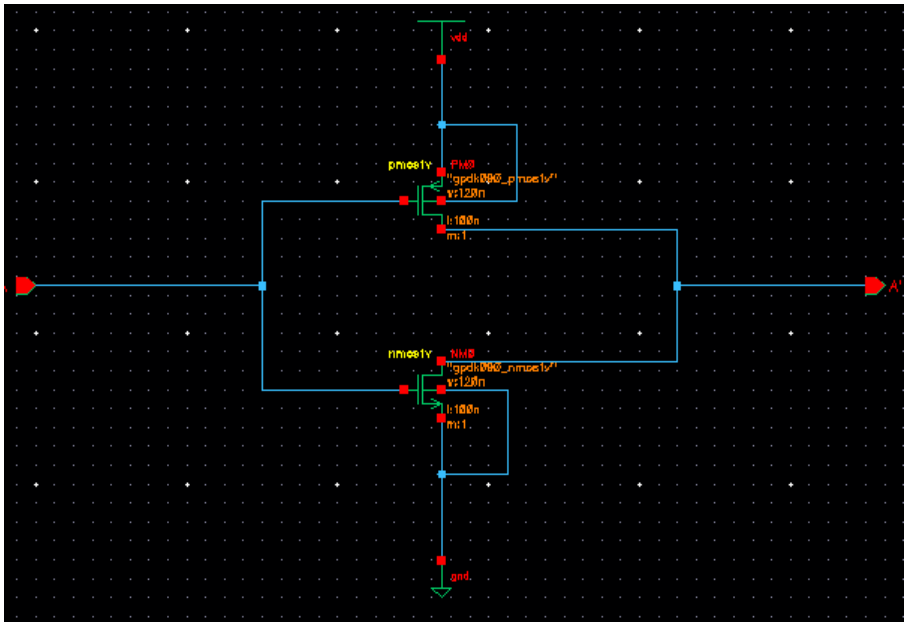
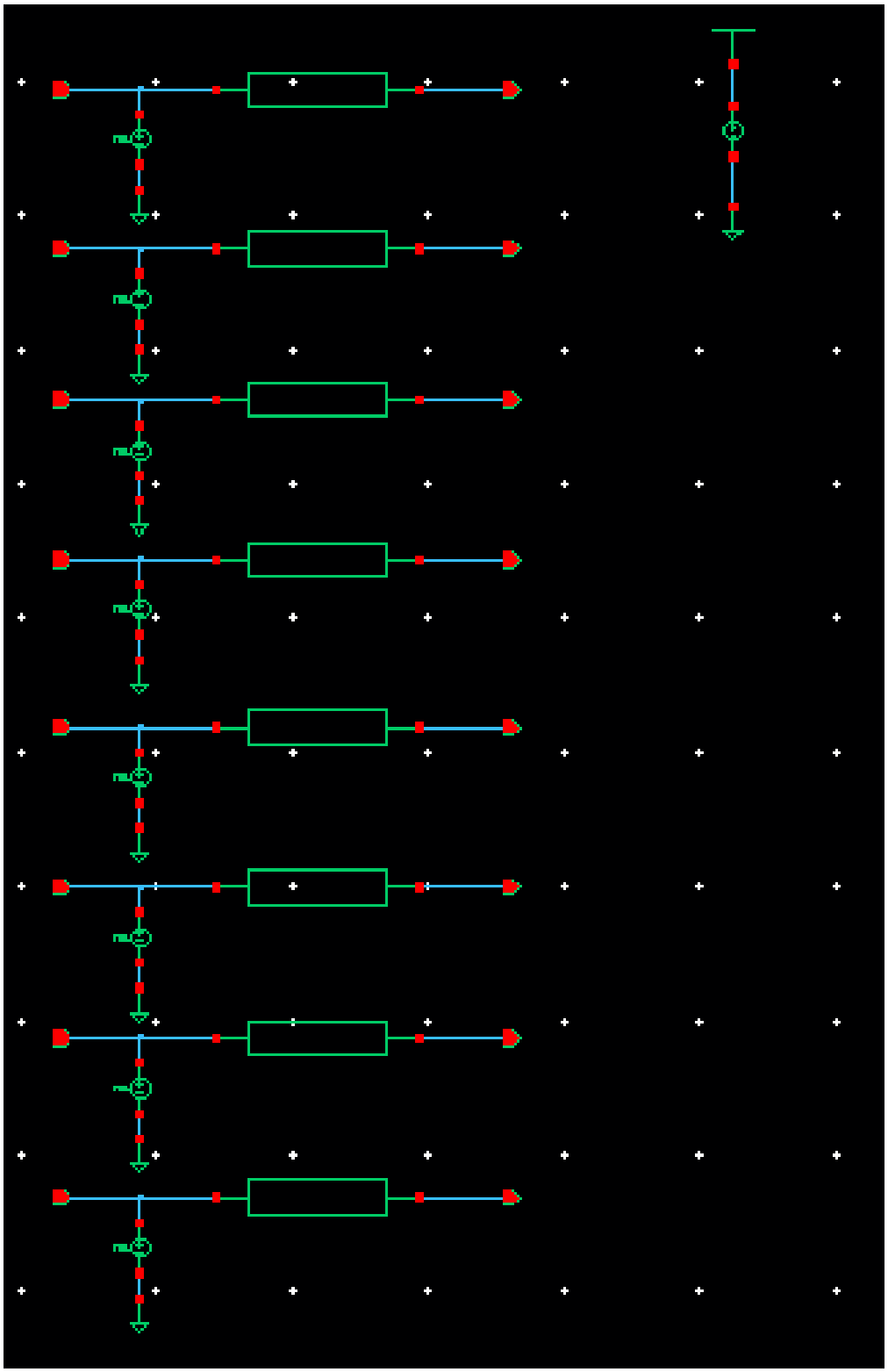
1) NOT GATE: -

❖ Schematic

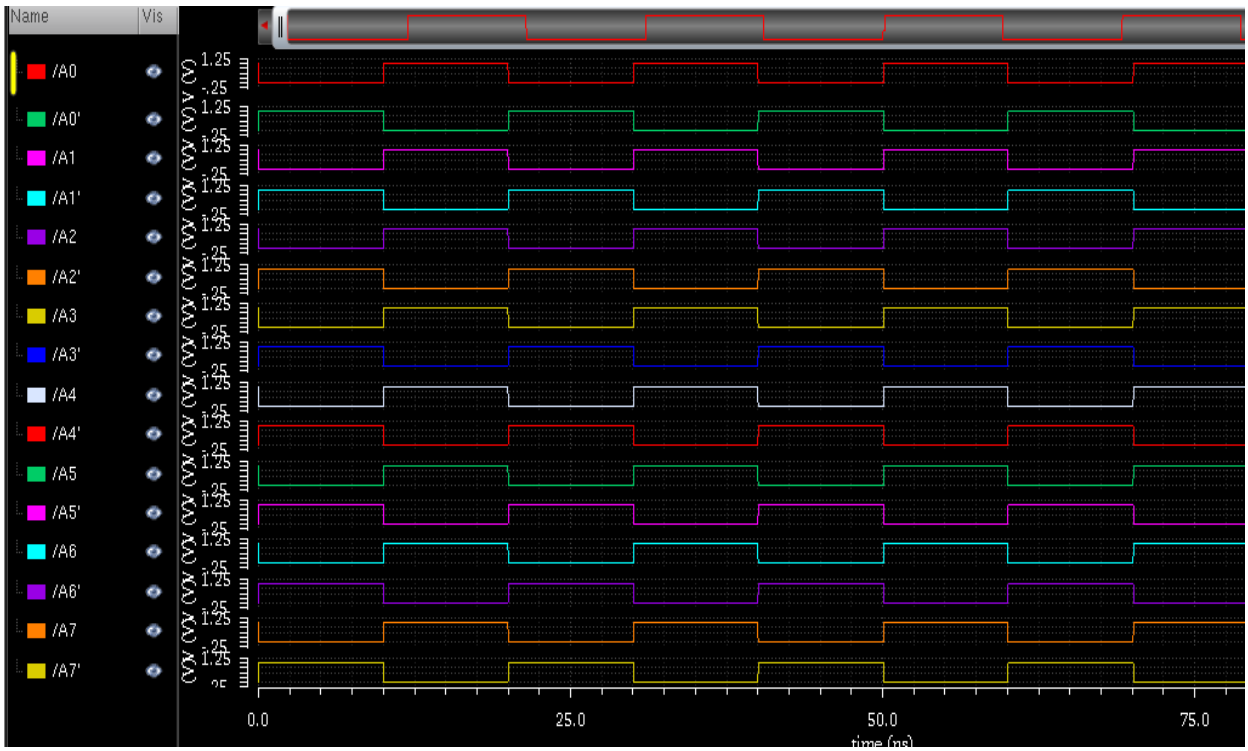


❖ Test Bench



(Test Bench – 8 Bit)

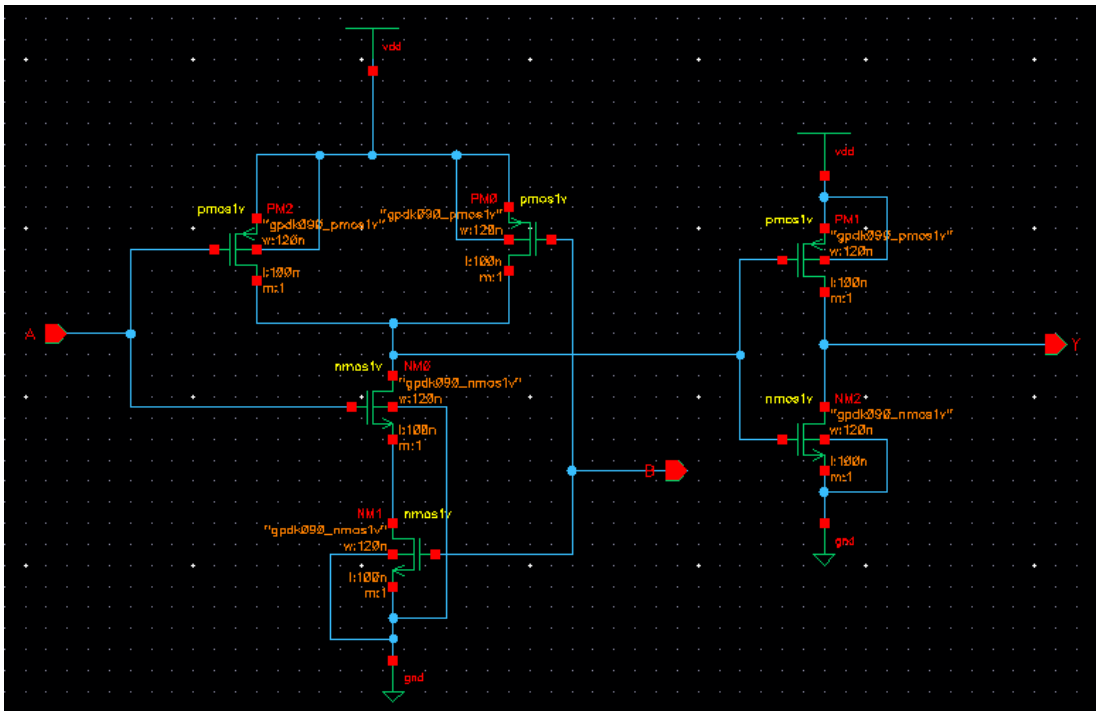
❖ Output



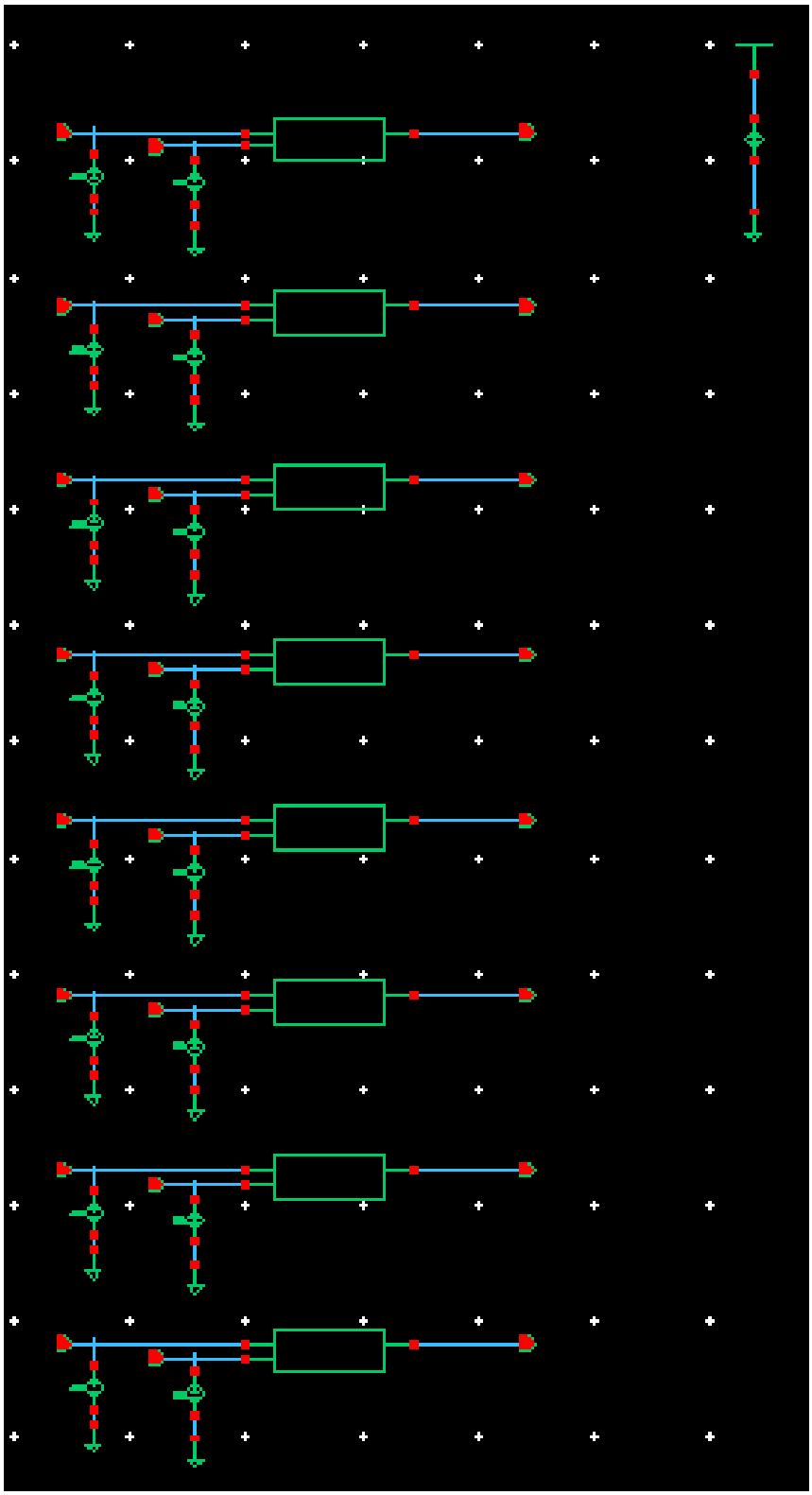
(Output – 8 Bit)

2) AND GATE: -

❖ Schematic

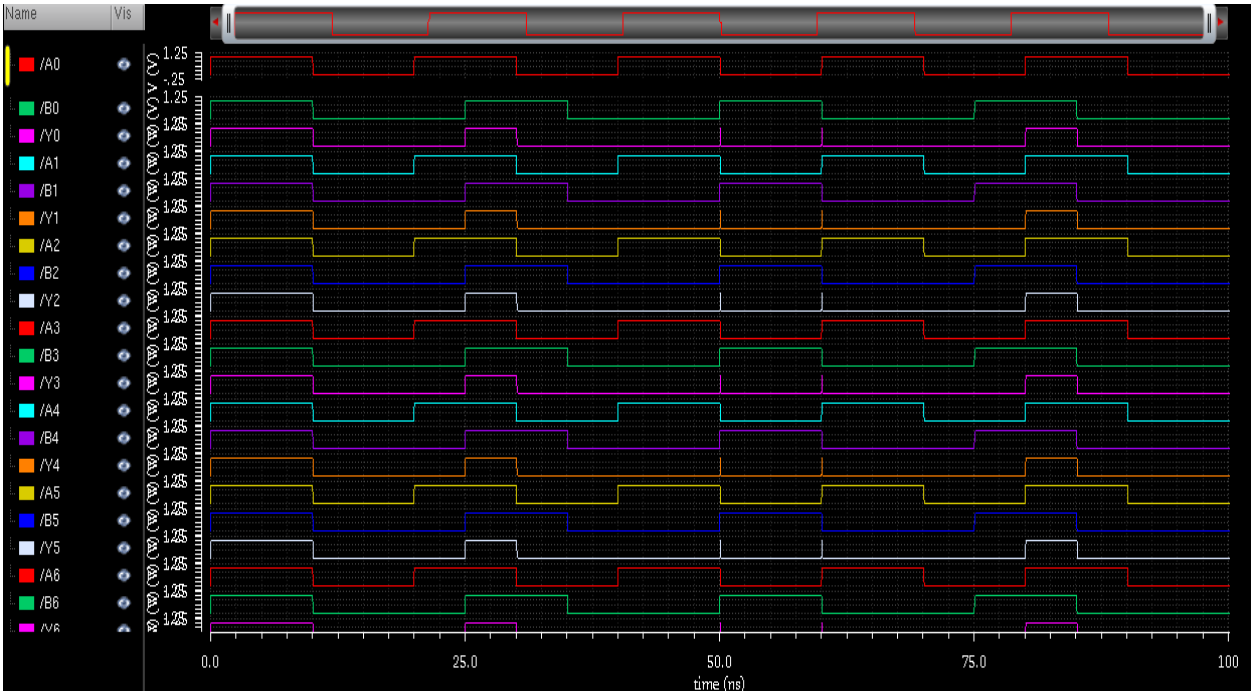


❖ Test Bench

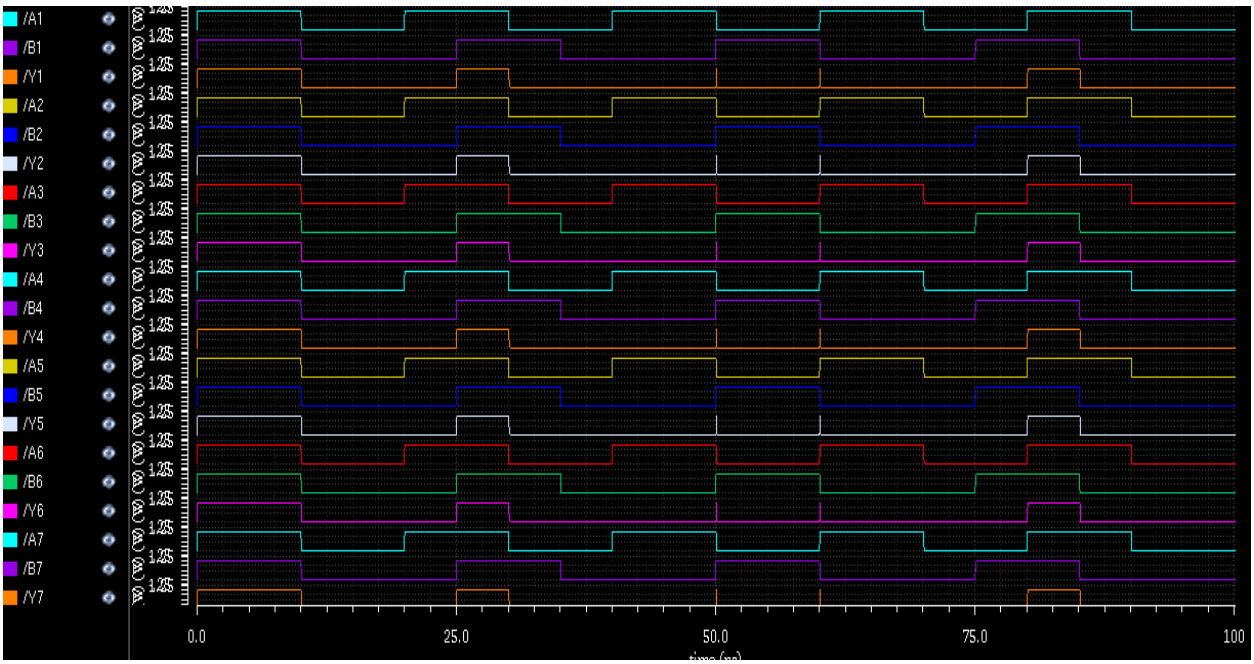


(Test Bench – 8 Bit)

❖ Output



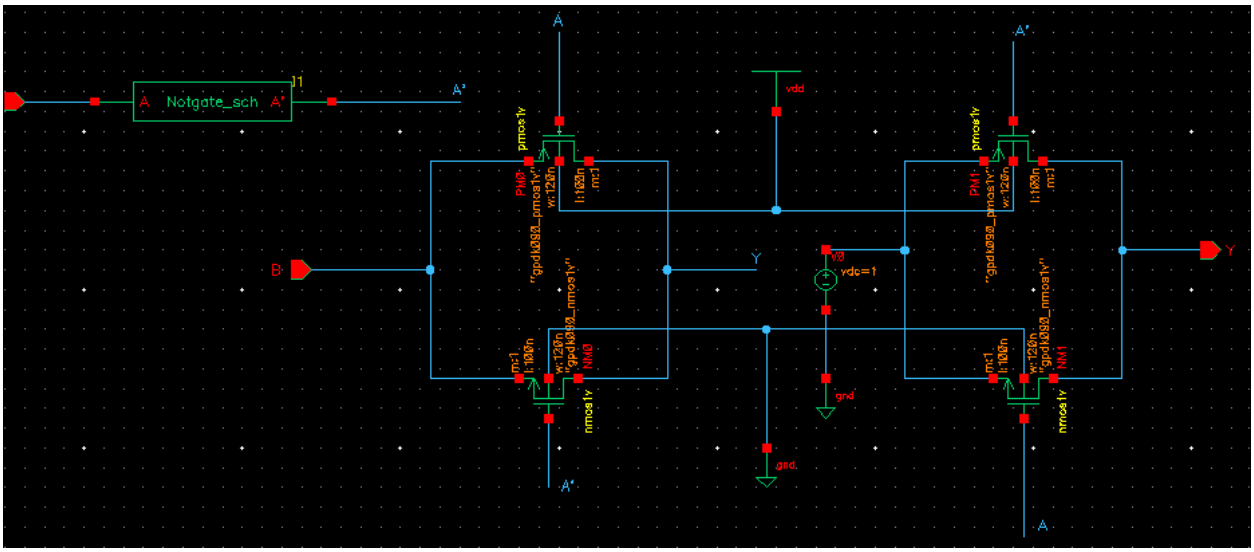
(Output – 8 Bit)



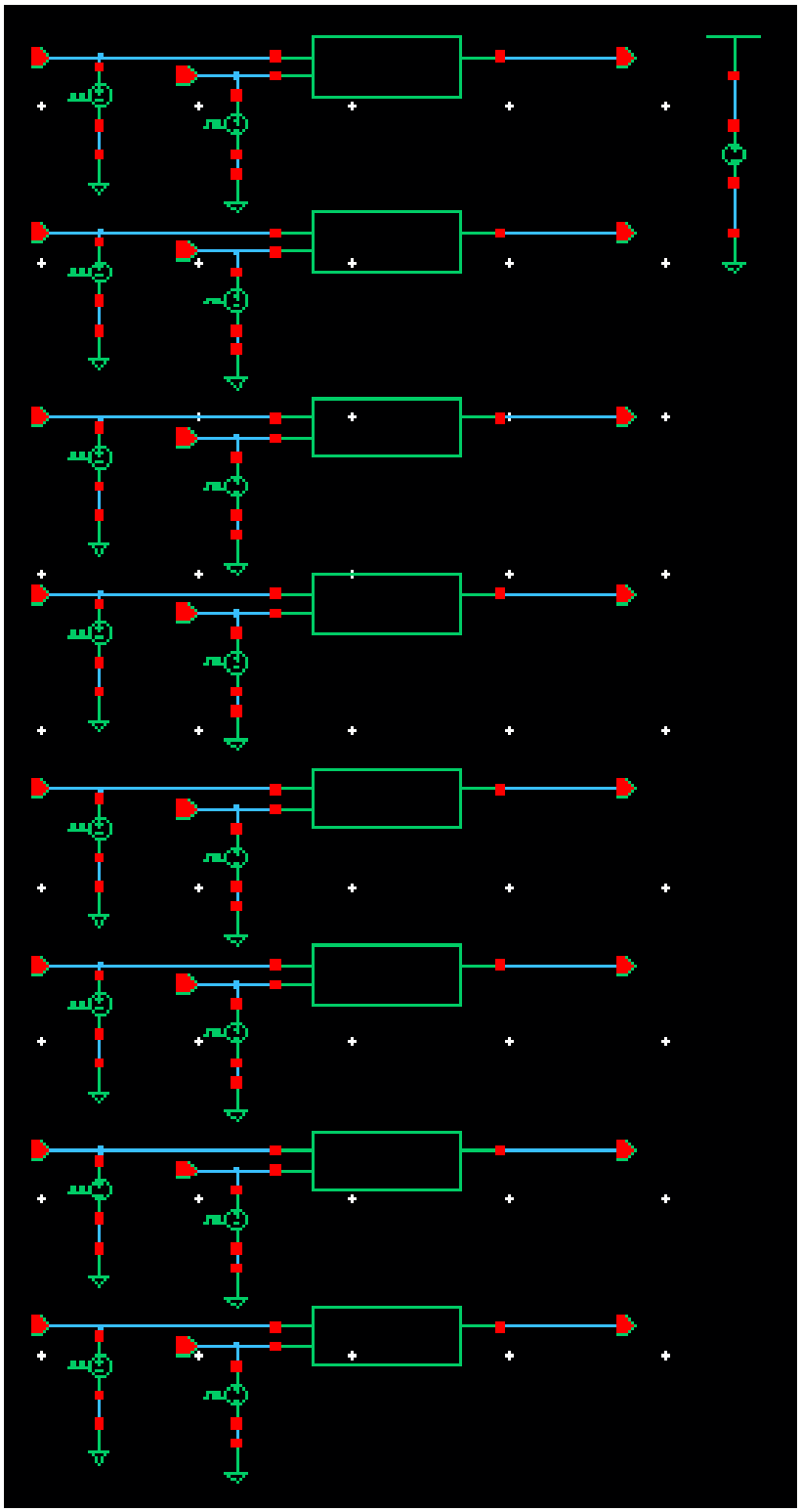
(Output – 8 Bit)

3) OR GATE: -

❖ Schematic

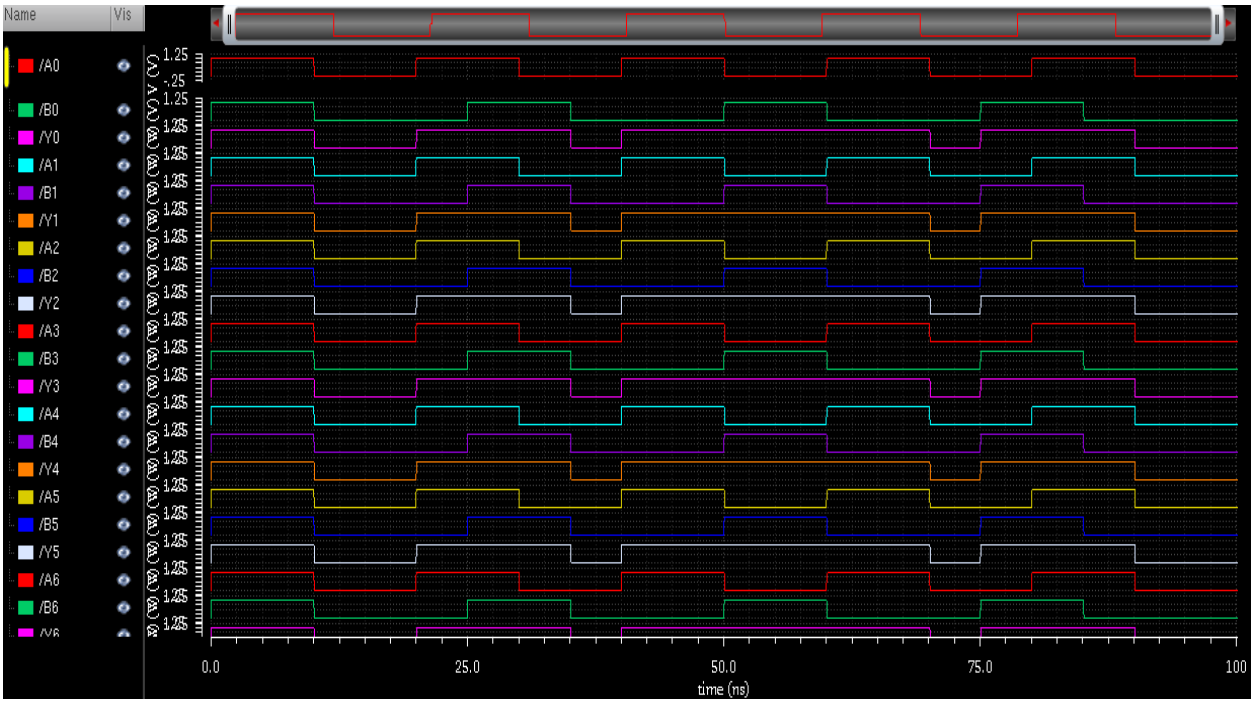


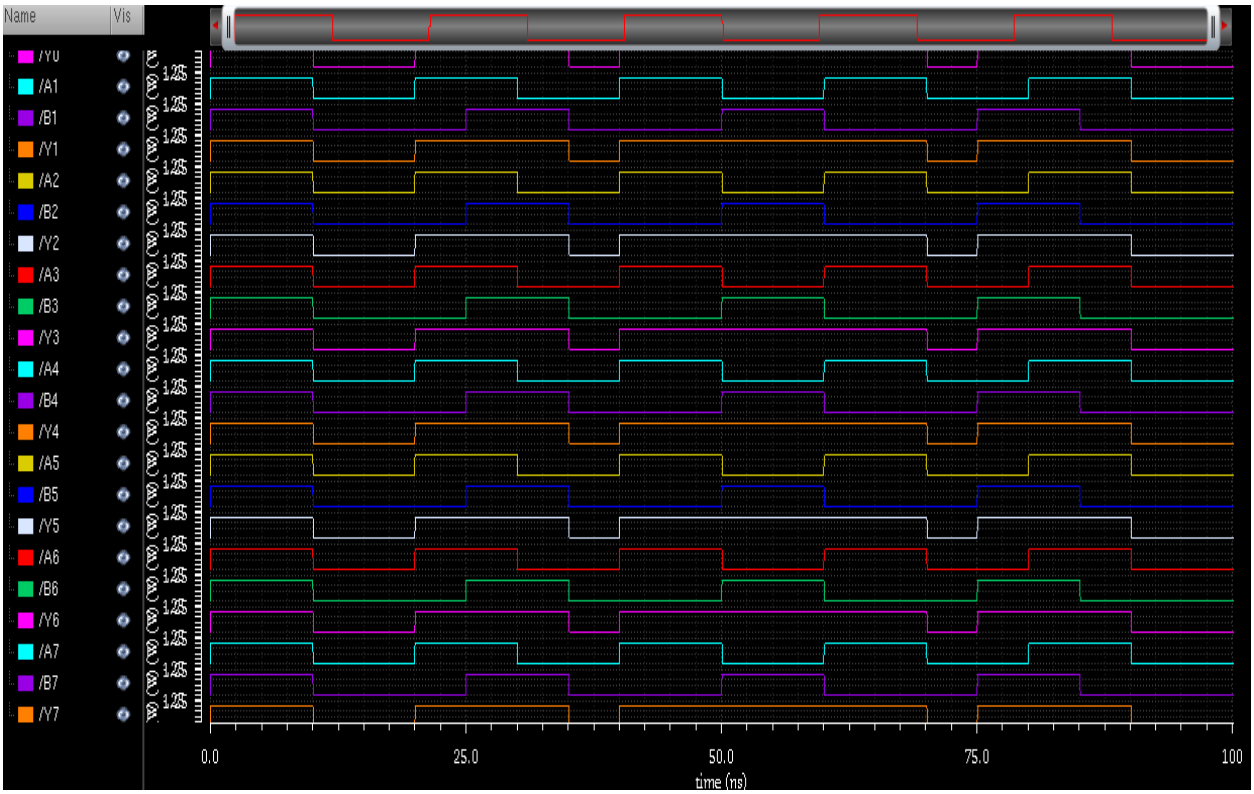
❖ Test Bench



(Test Bench – 8 Bit)

❖ Output

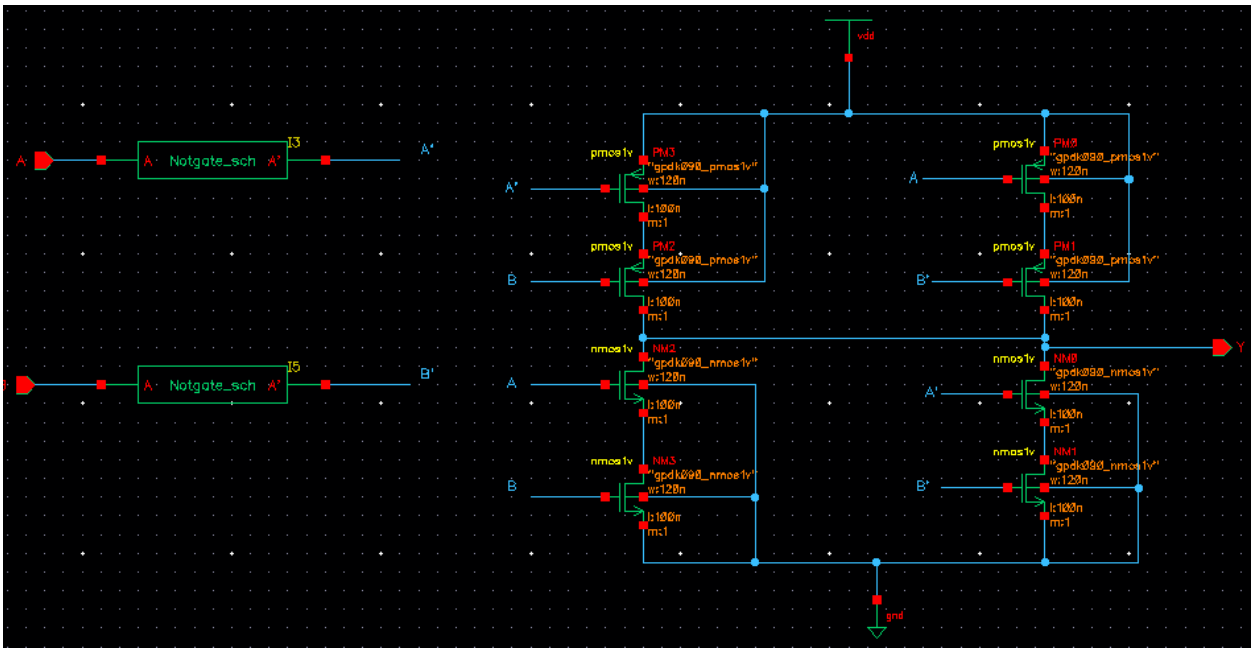




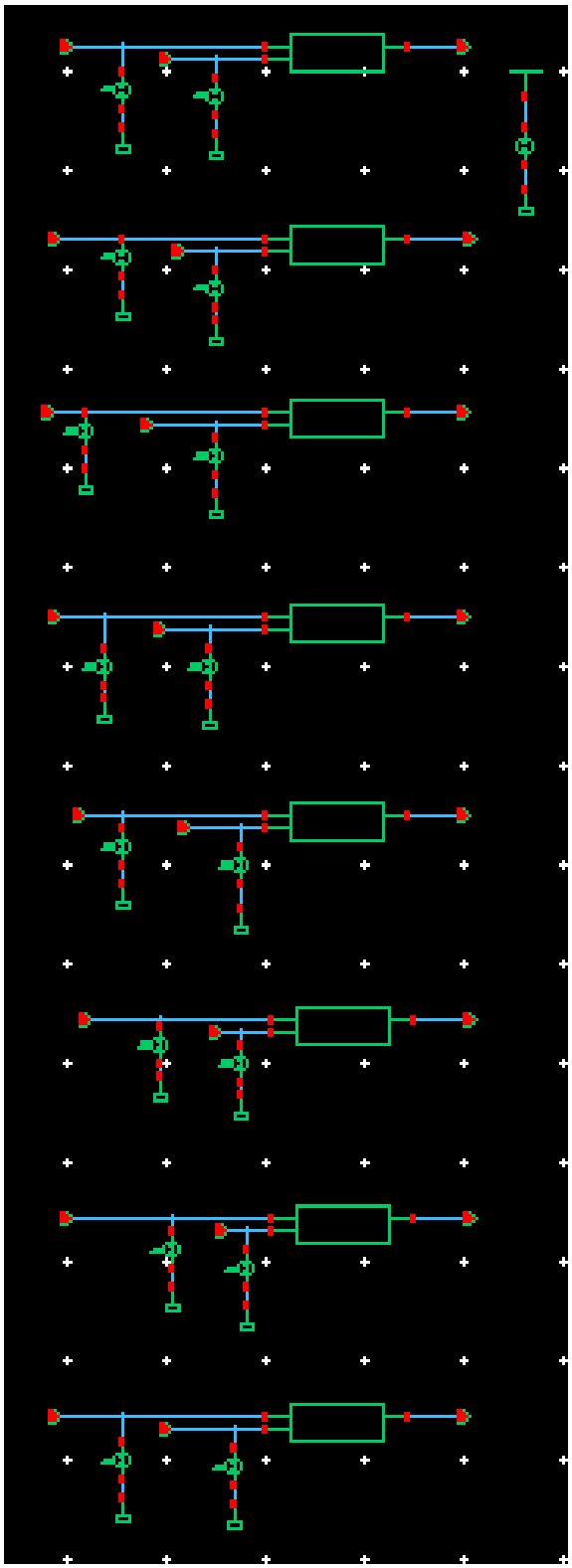
(Output – 8 Bit)

4) EX-OR GATE: -

❖ Schematic

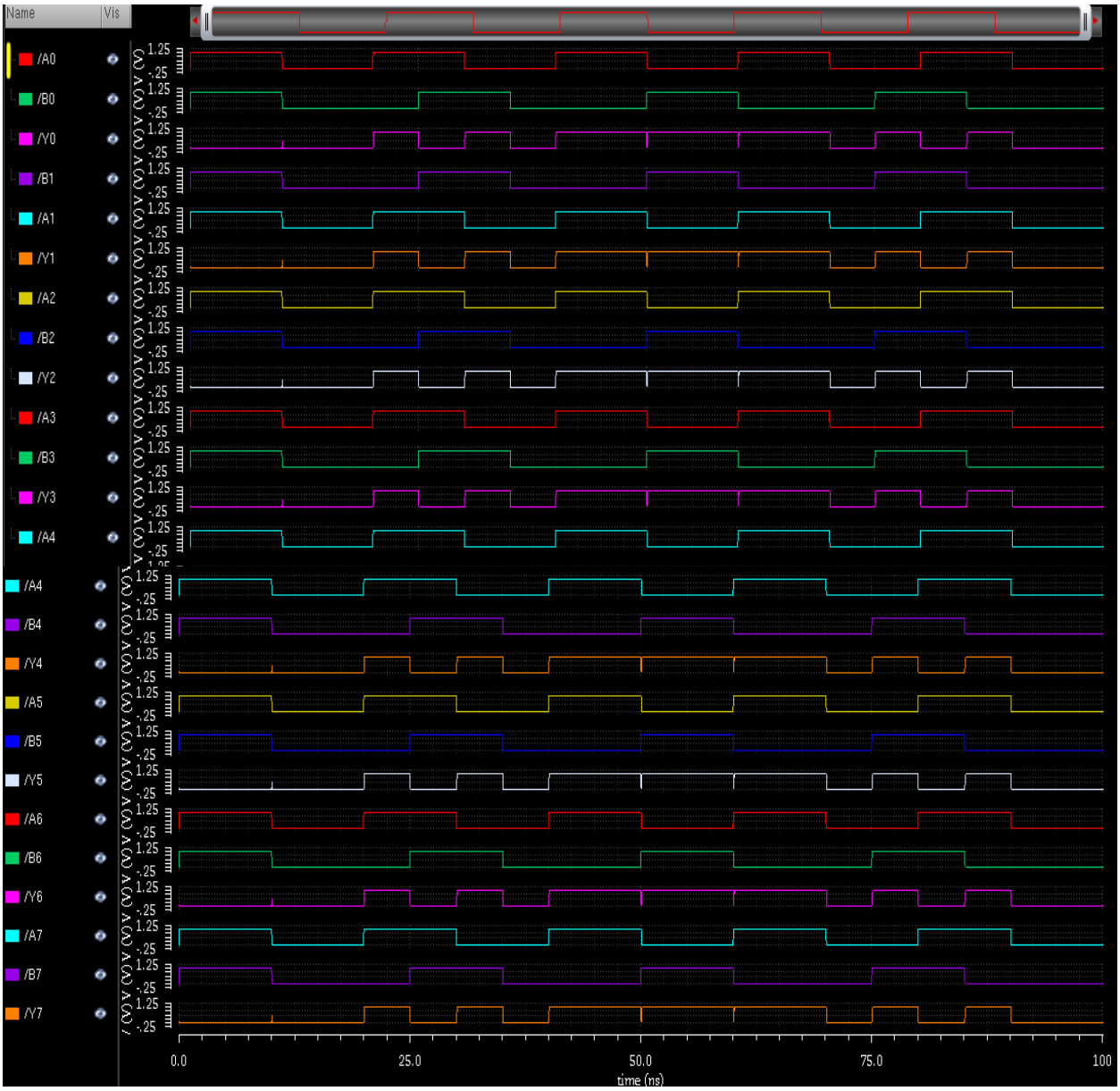


❖ Test Bench



(Test Bench – 8 Bit)

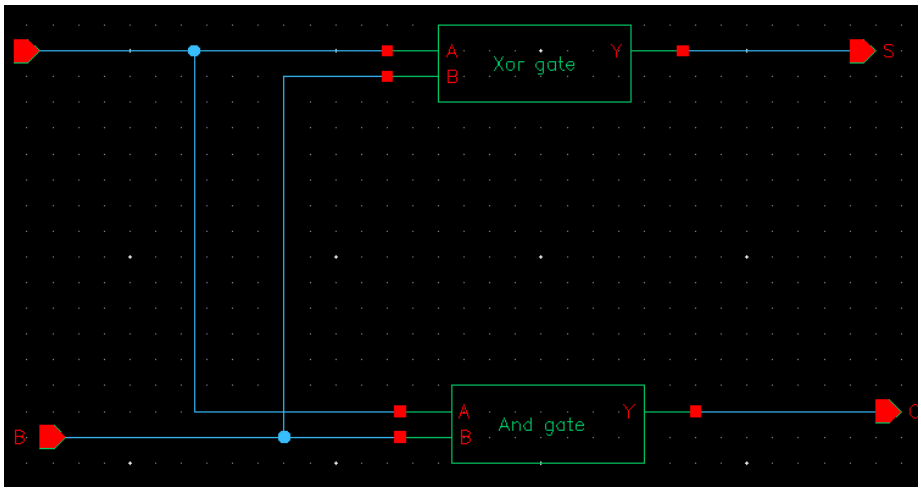
❖ Output



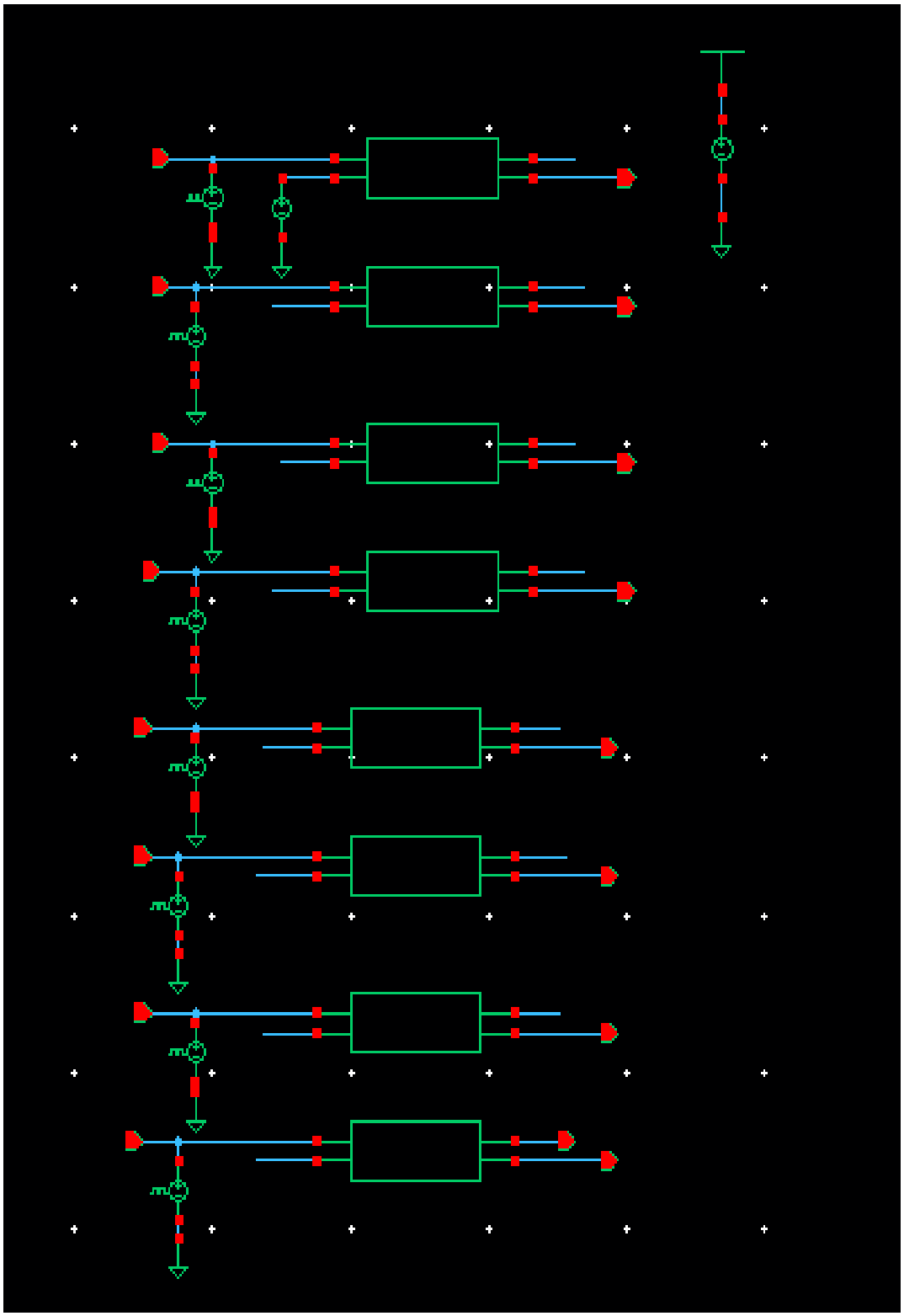
(Output –8 Bit)

5) INCREMENT OPERATION

❖ Schematic

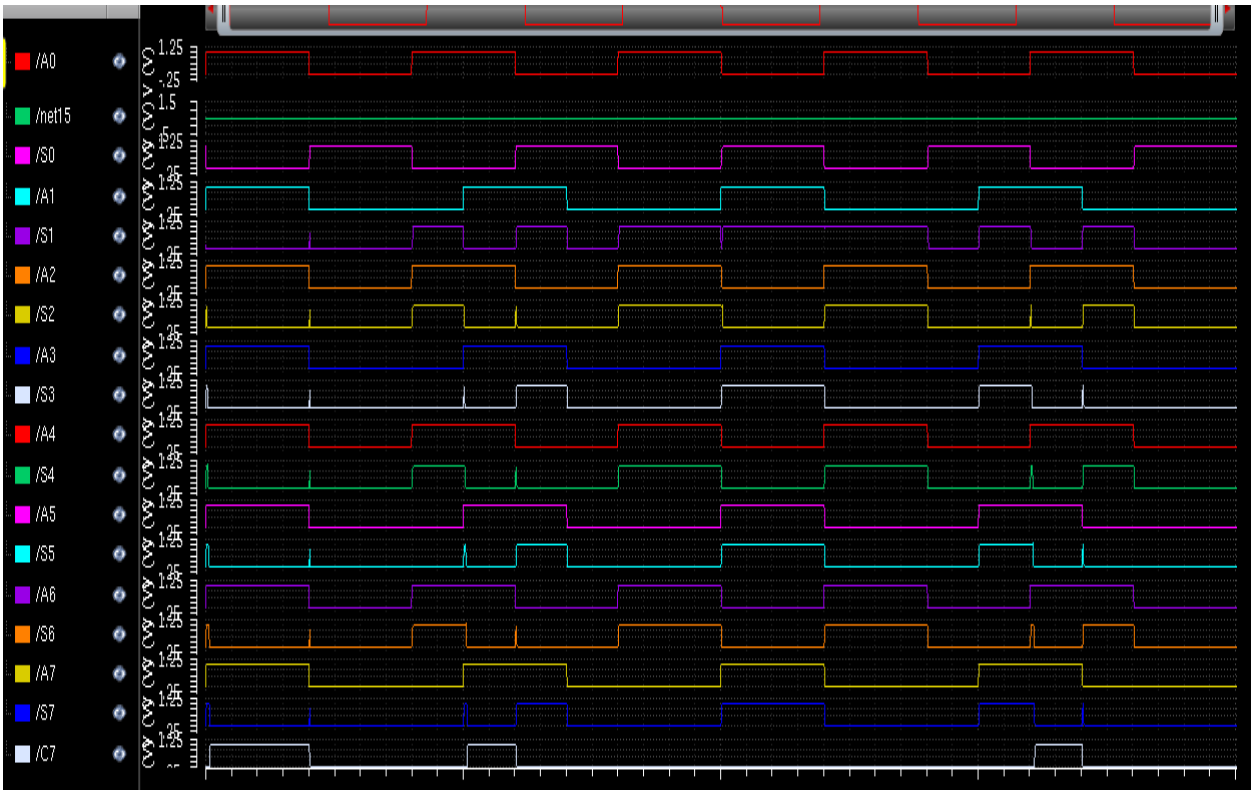


❖ Test Bench



(Test Bench – 8 Bit)

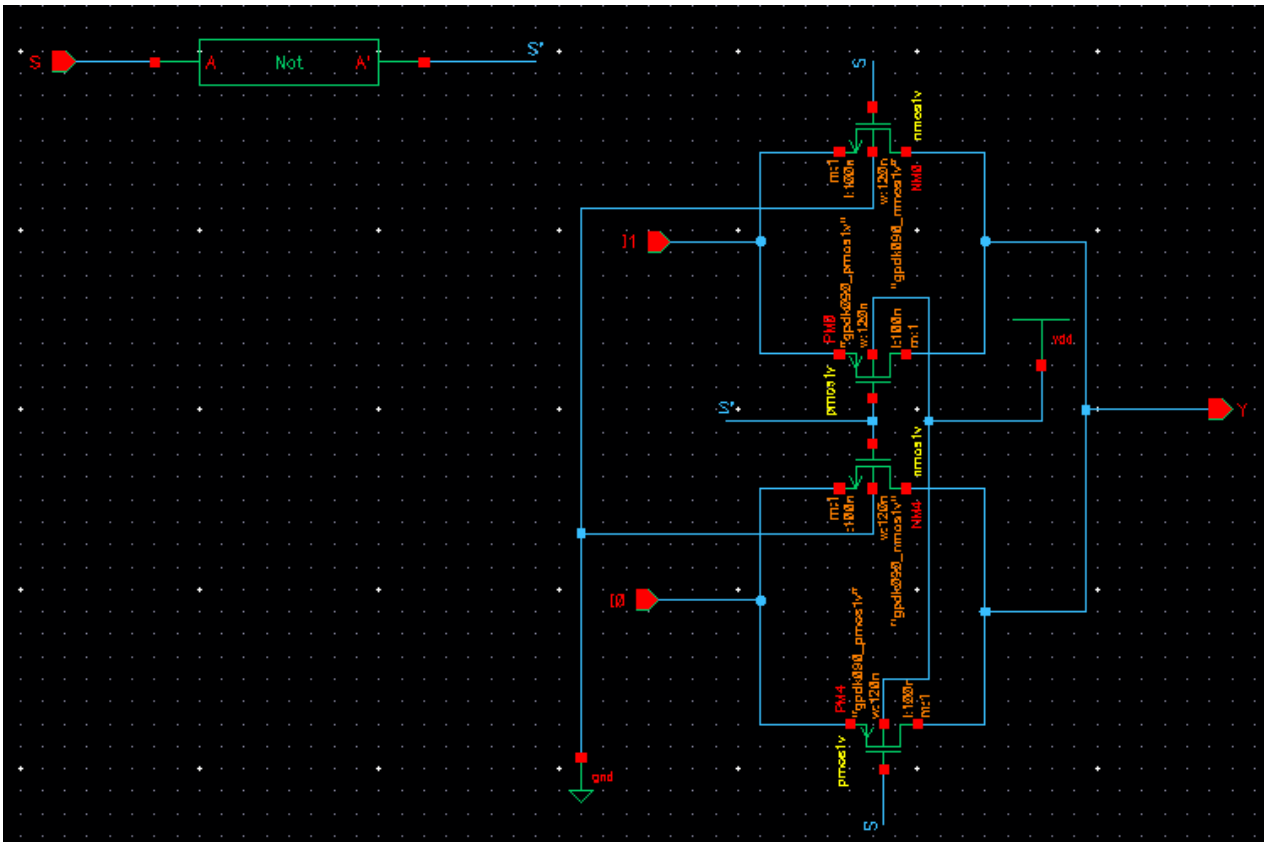
❖ Output



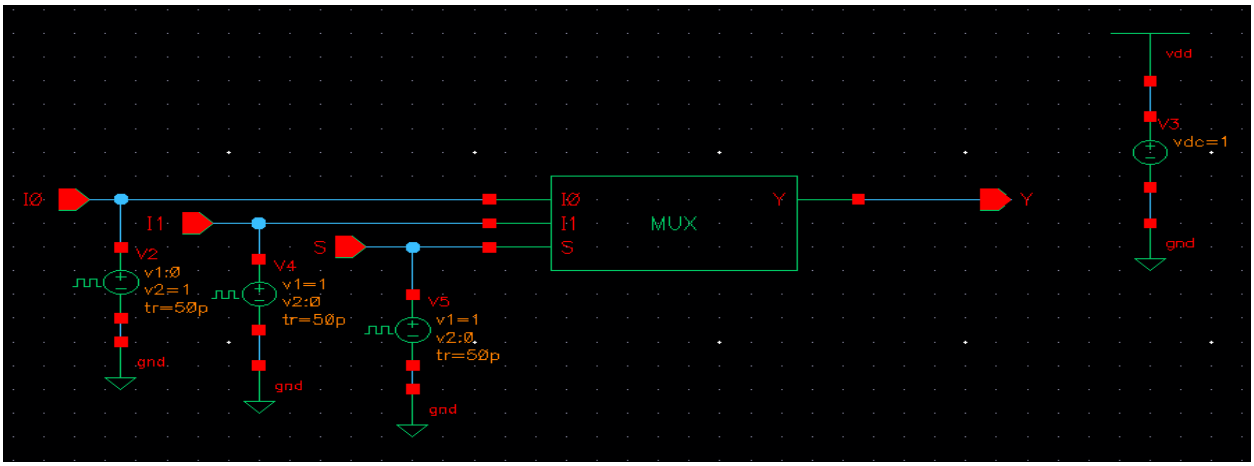
(Output – 8 Bit)

6) MUX (2:1)

❖ Schematic

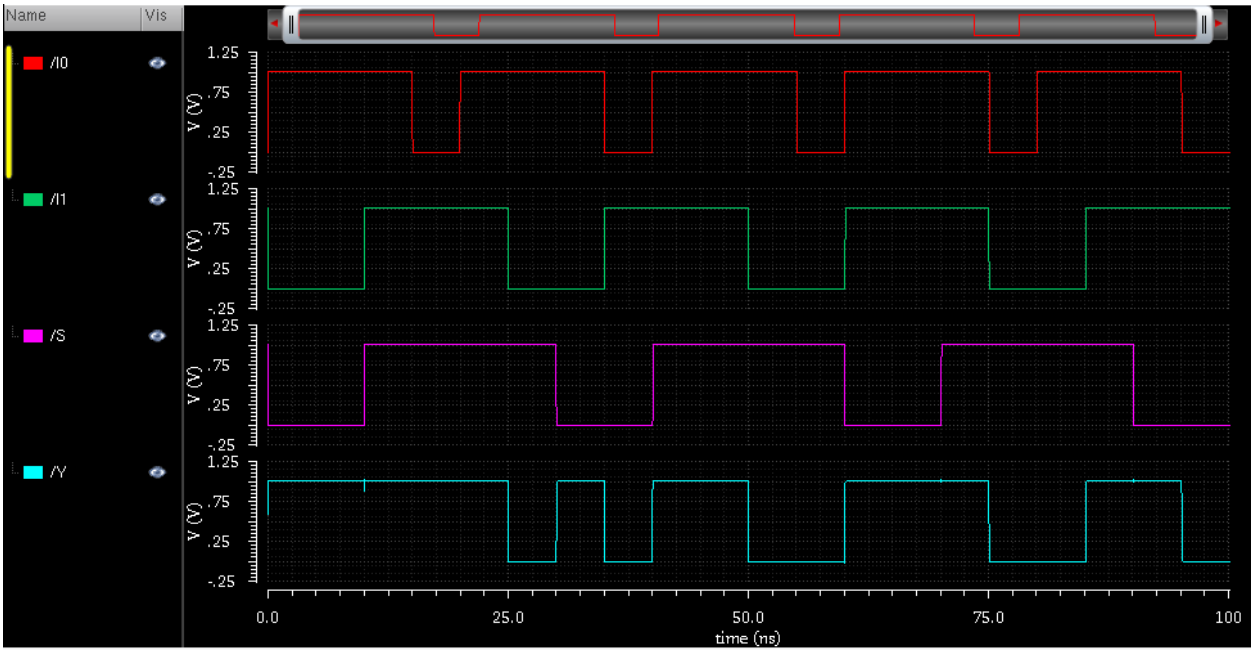


❖ Test Bench



(Test Bench – 1 Bit)

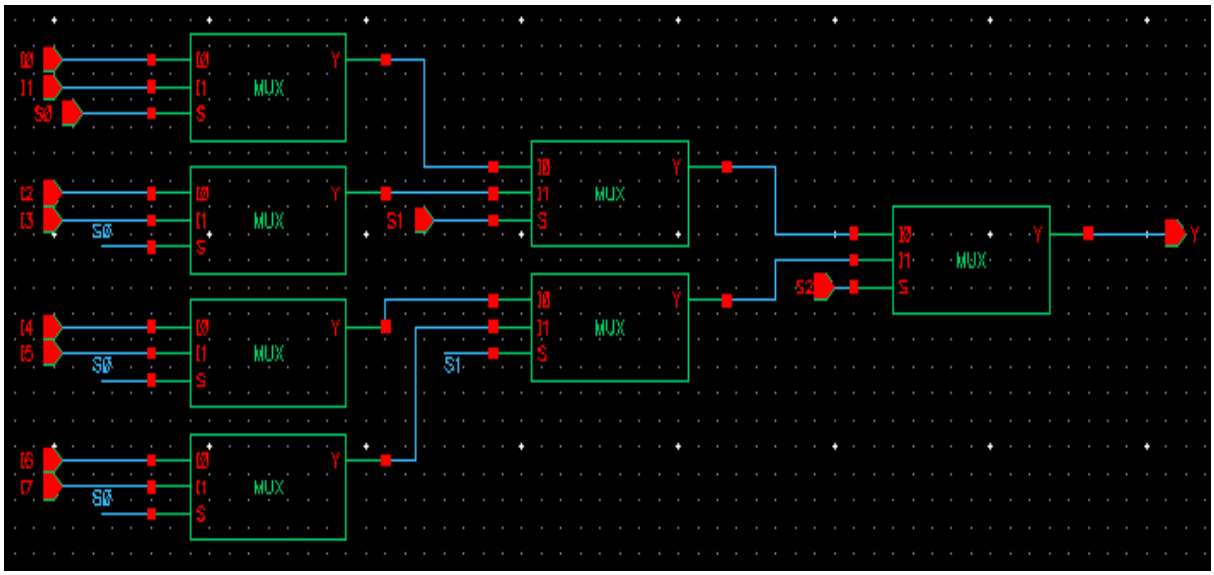
❖ Output



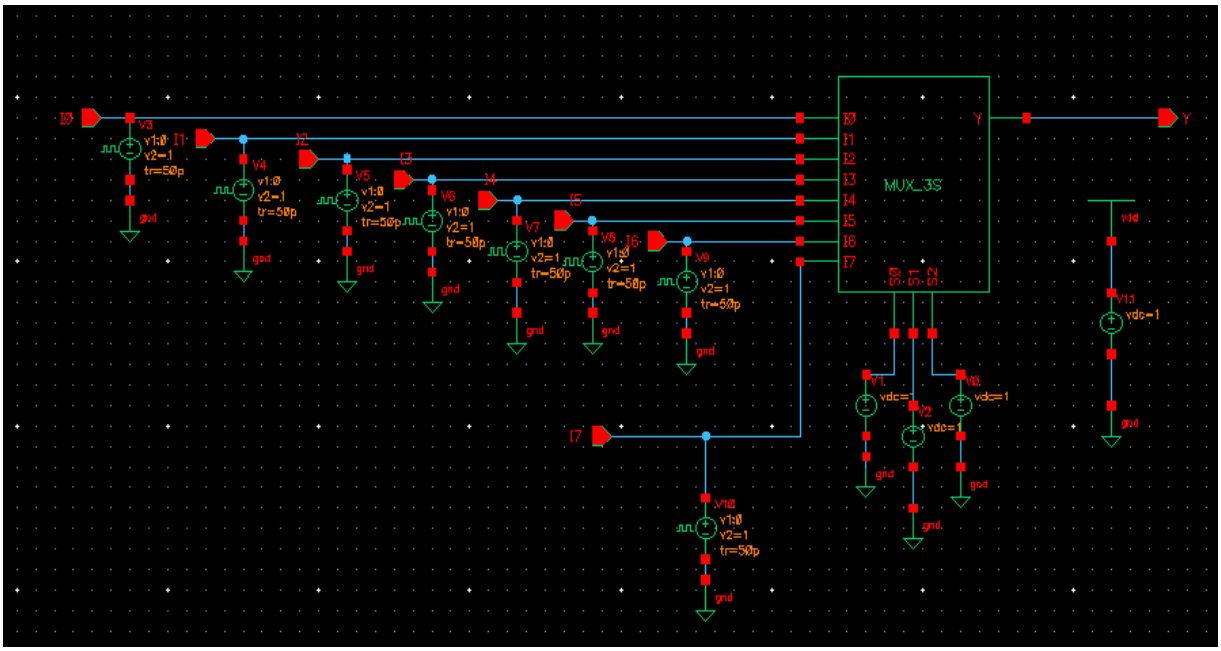
(Output – 1 Bit)

7) MUX (8:1)

❖ Schematic

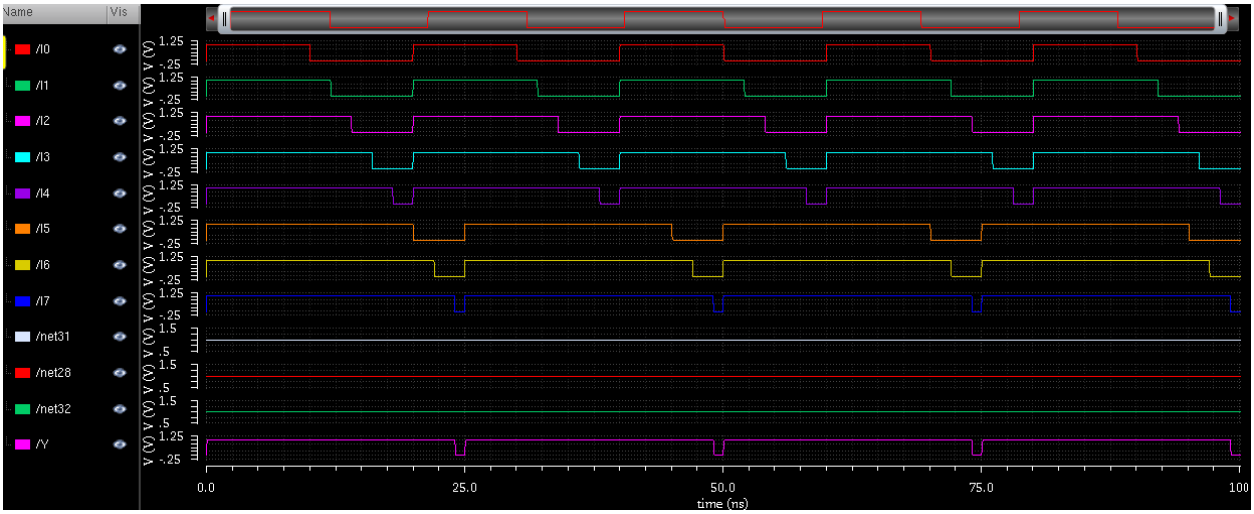


❖ Test Bench



(Test Bench – 8 Bit)

❖ Output

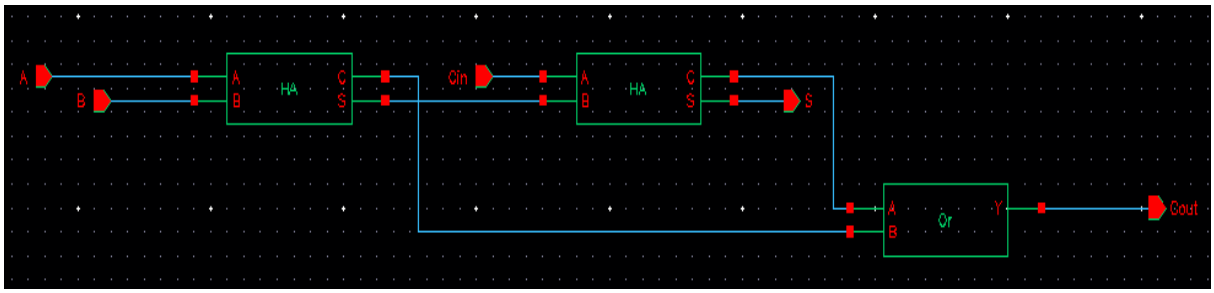


(Output – 8 Bit)

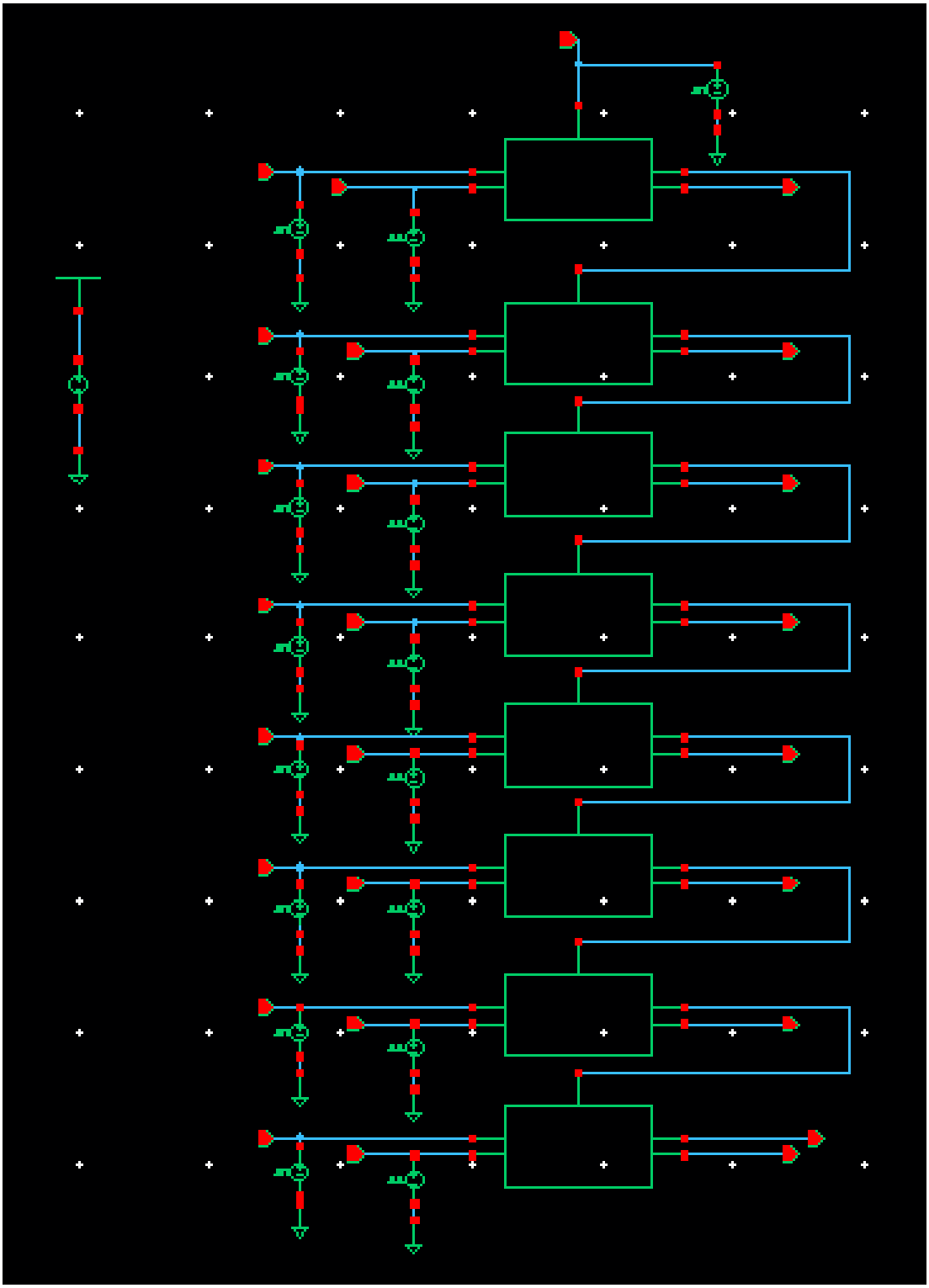
(When S2, S1, and S0 all are 1)

8) FULL ADDER

❖ Schematic

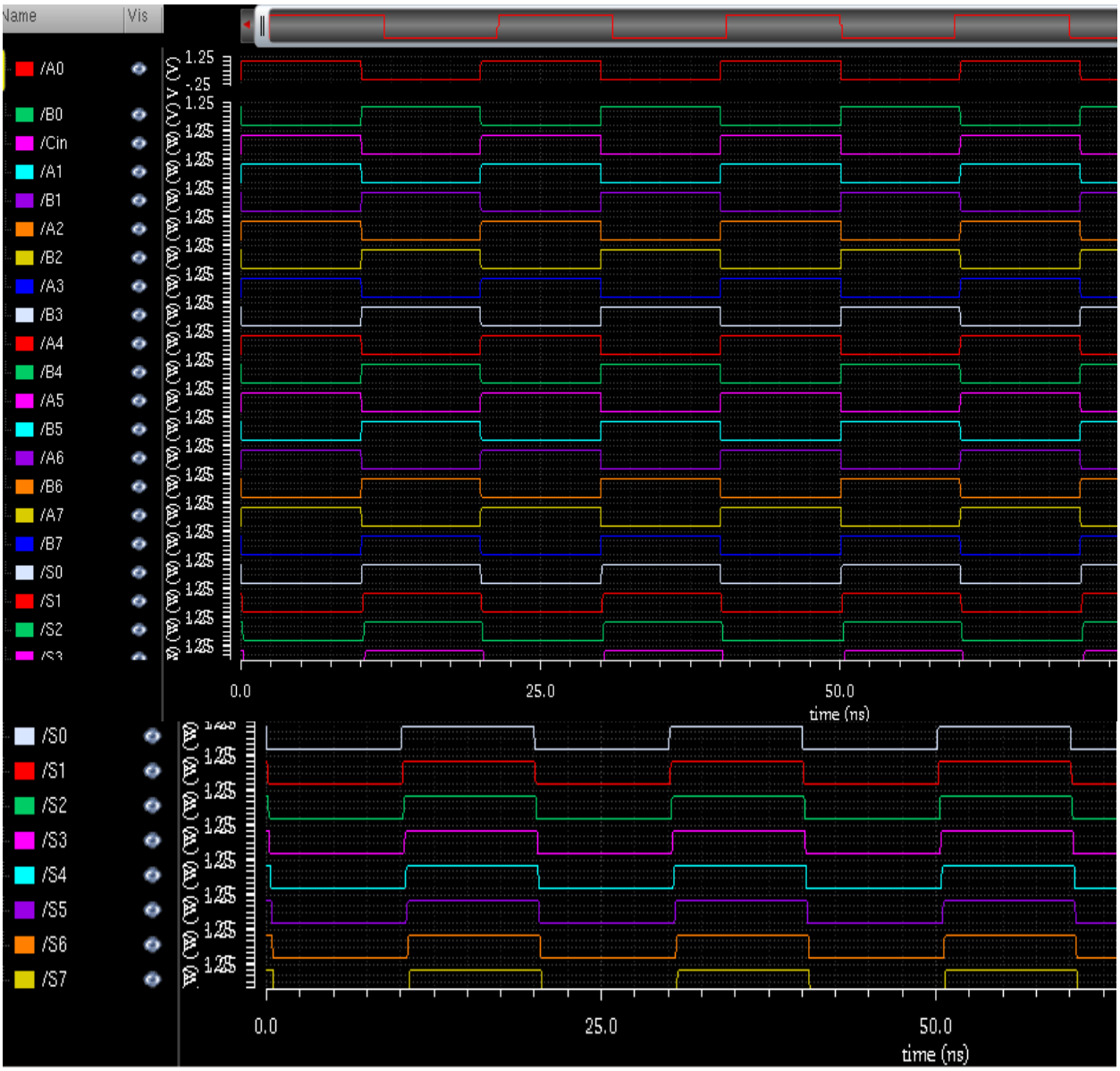


❖ Test Bench



(Test Bench – 8 Bit)

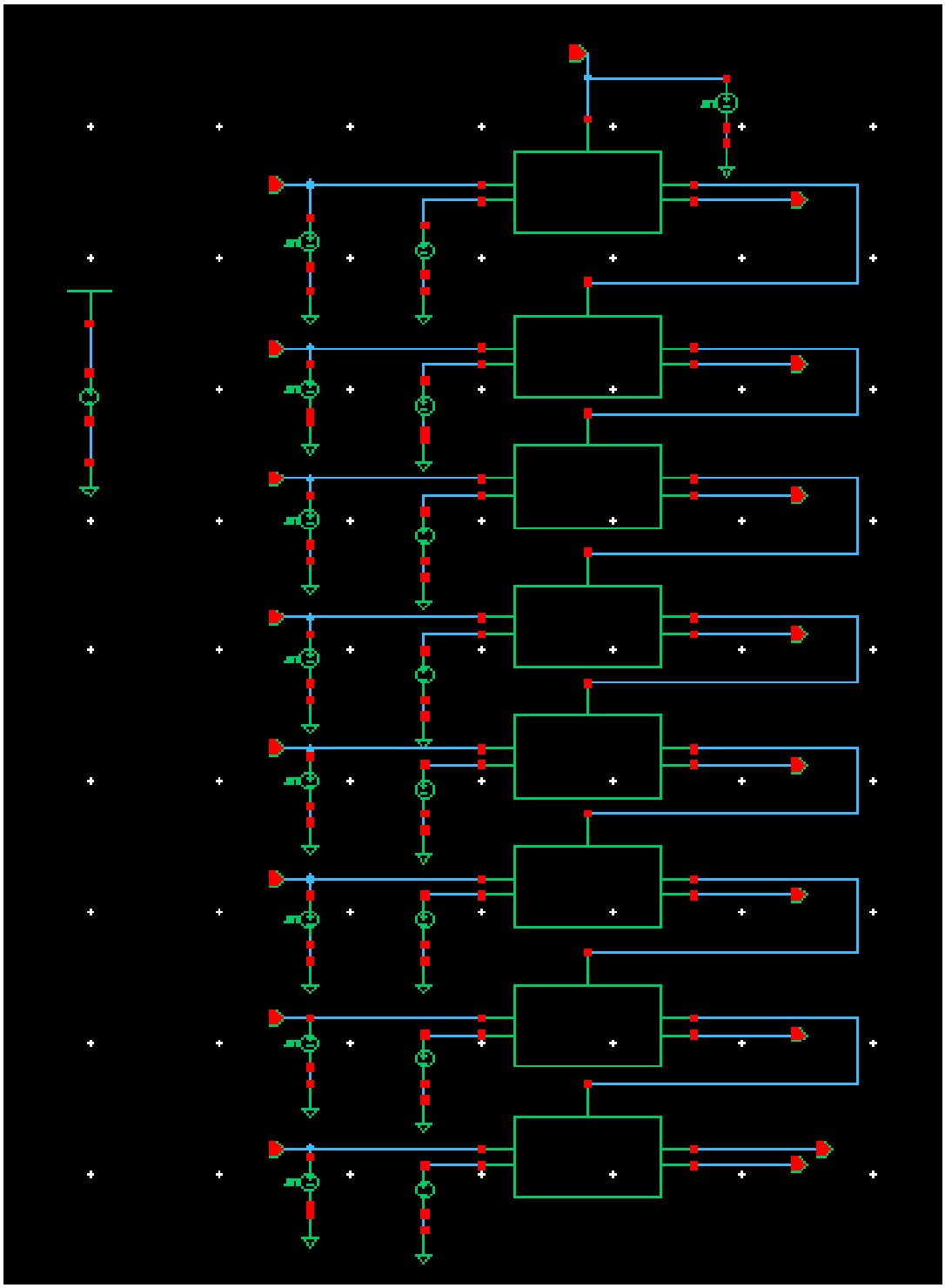
❖ Output



(Output – 8 Bit)

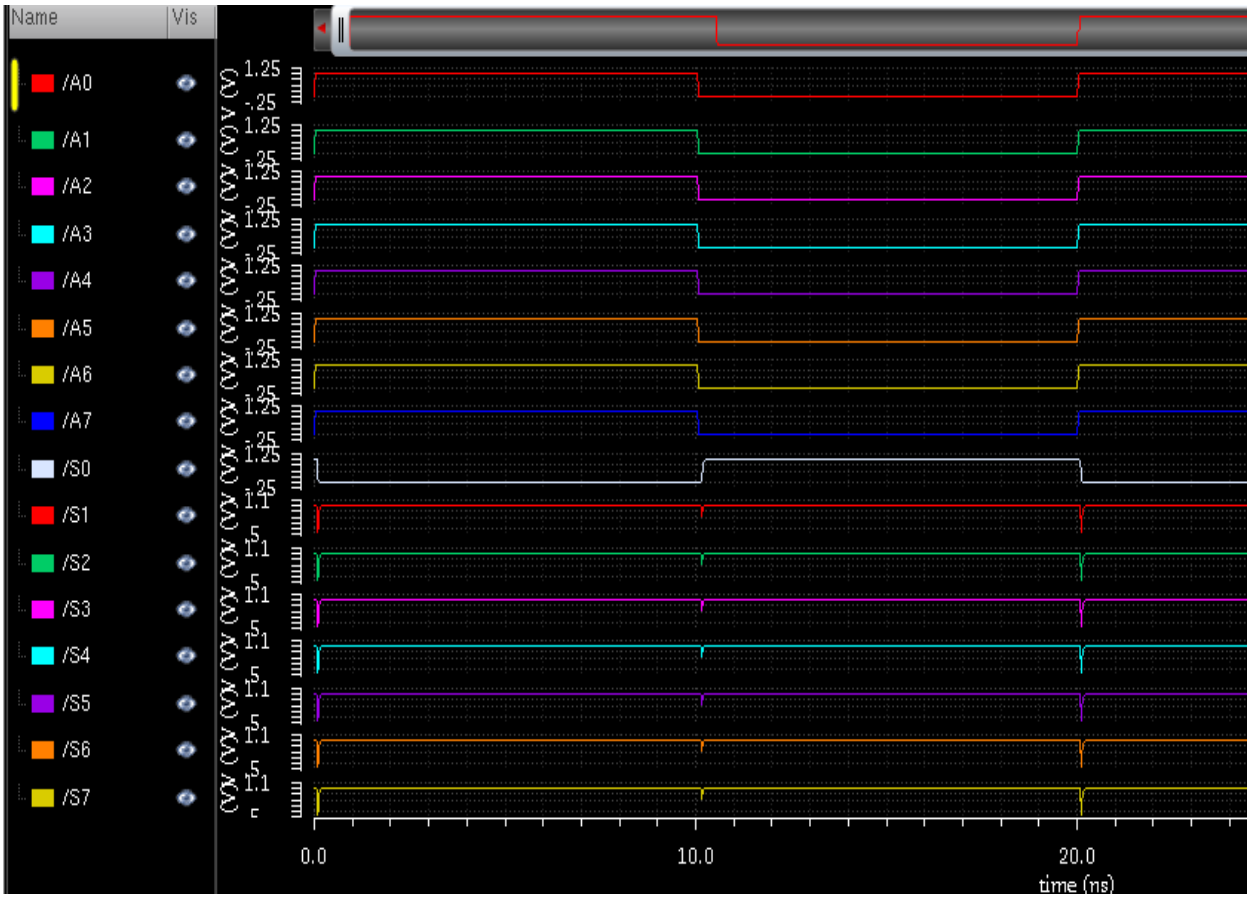
9) DECREMENT OPERATION (Designed using Full Adder Only)

❖ Test Bench



(Test Bench – 8 Bit)

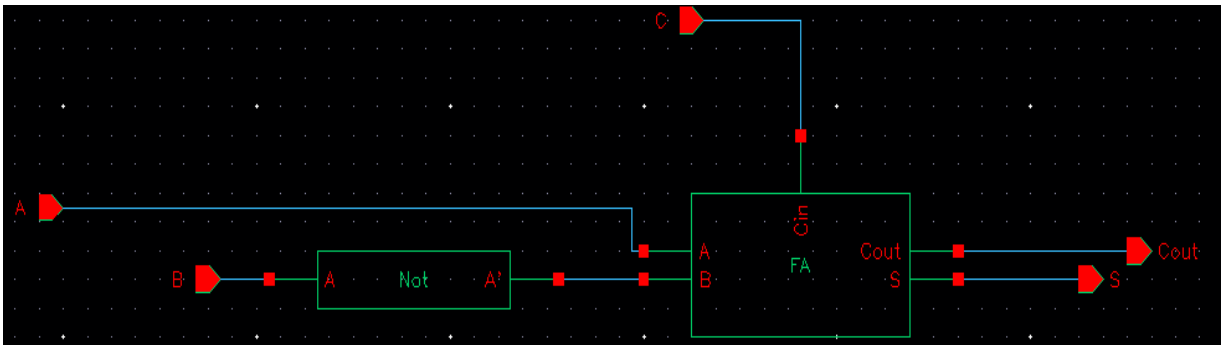
❖ Output



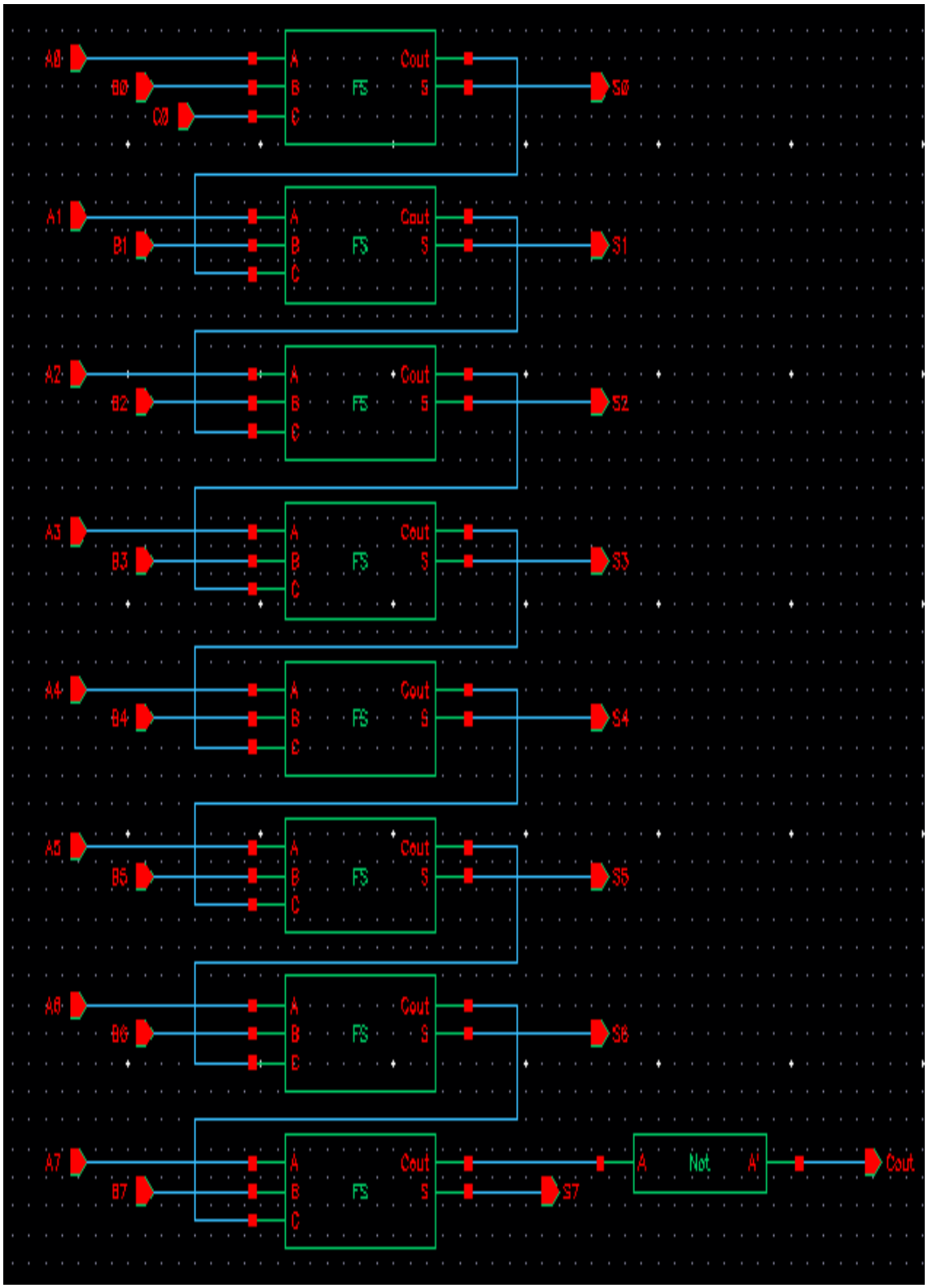
(Output – 8 Bit)

10) FULL SUBTRACTOR

❖ Schematic



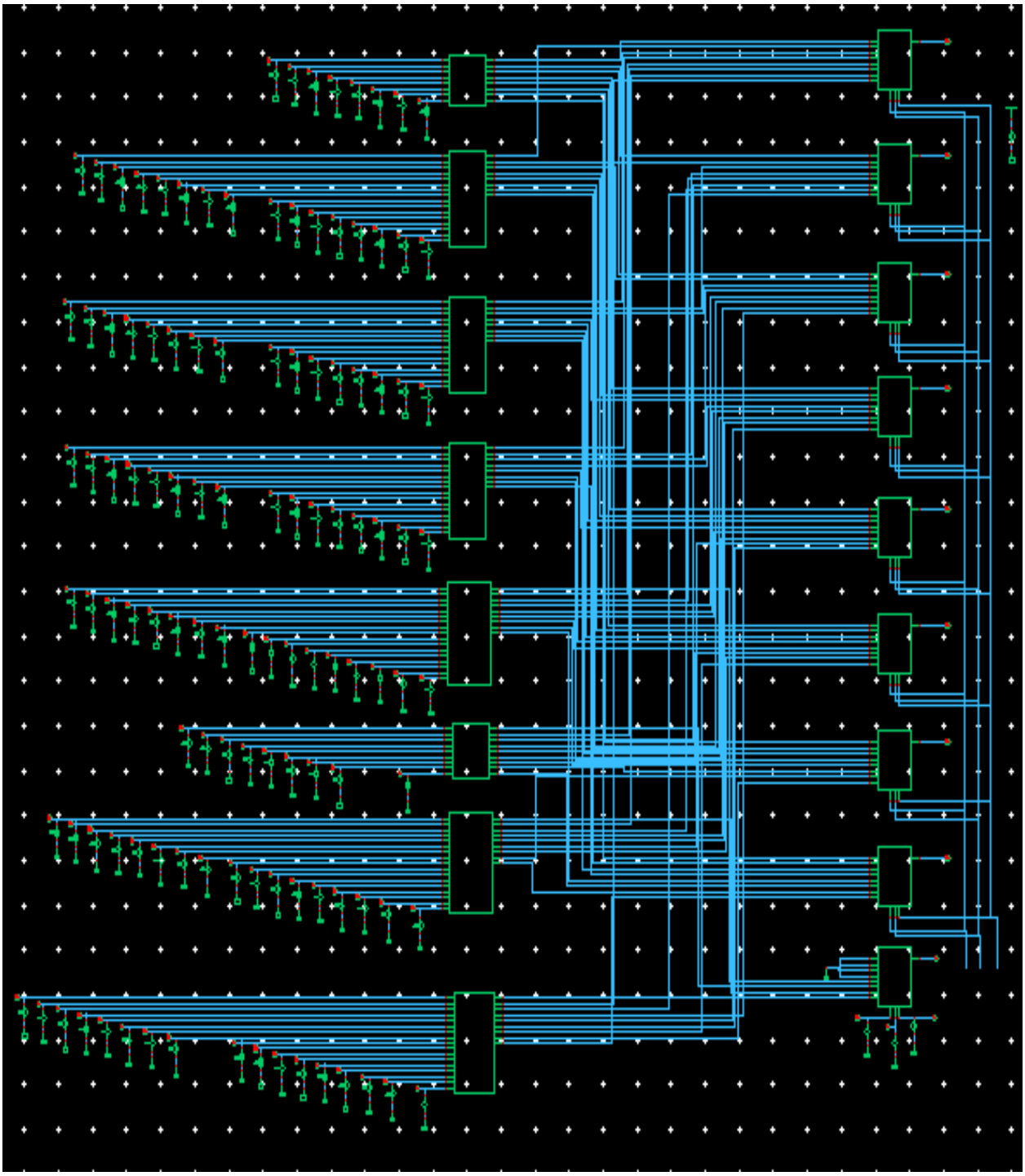
❖ Test Bench



(Test Bench – 8 Bit)

11) FINAL ALU

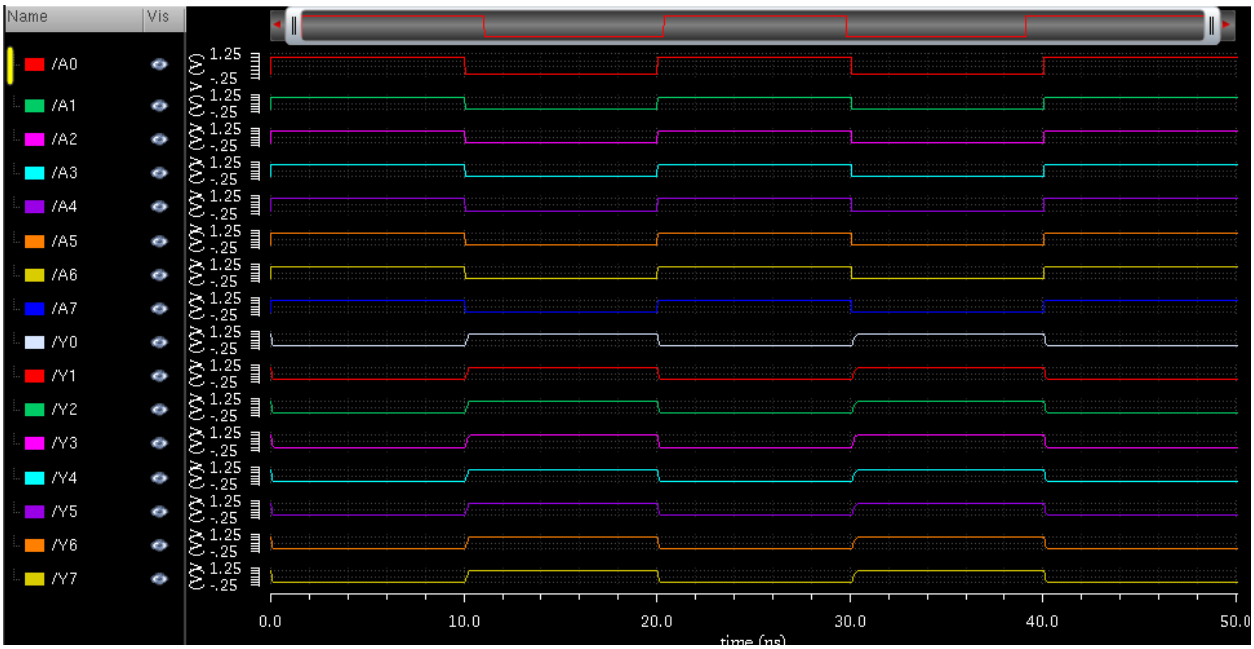
❖ Schematic



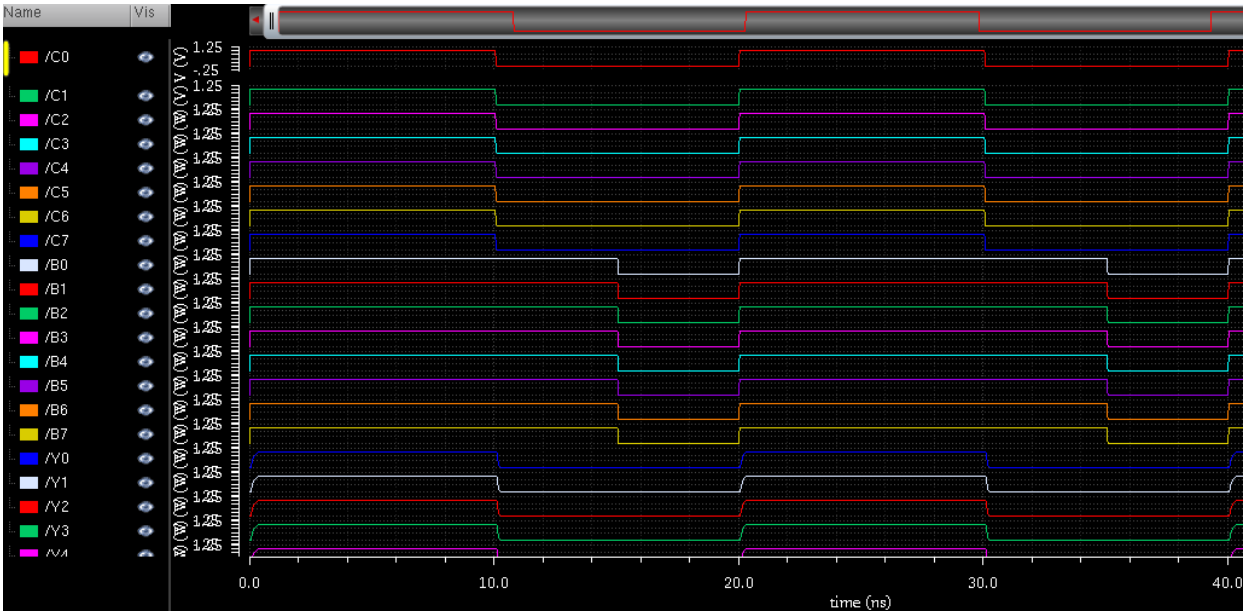
(8 BIT ALU)

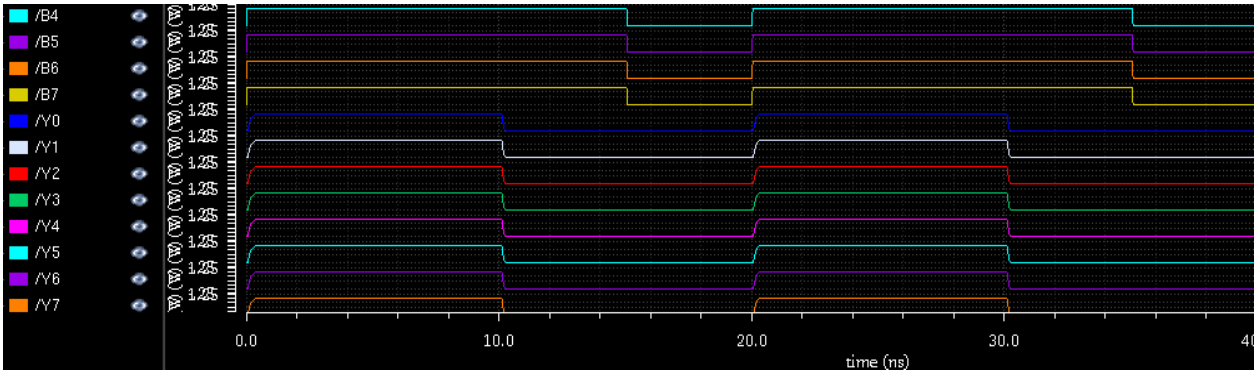
Some of the final test results are shown below: -

Case-1) When S2=S1=S0=0



Case-2) When S2=S1=0; S0=1





Case-3) When S2=1; S1=S0=0