

# Lab Assignment 1

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## Question 1

a

The circuit diagram can be seen in figure 1.

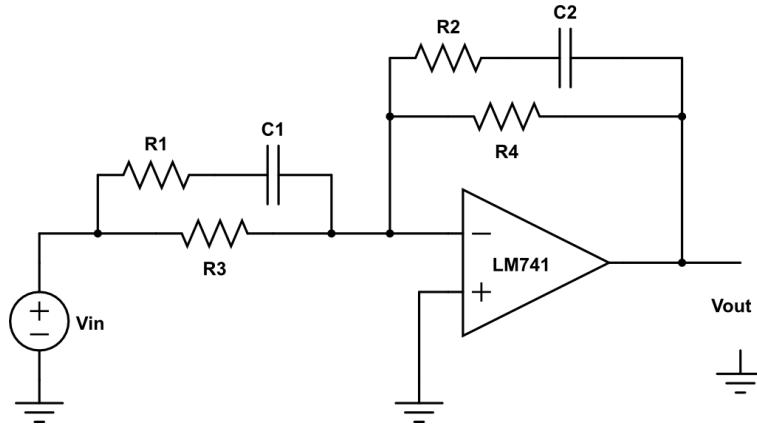


Figure 1: A lead-lag compensator circuit diagram for question 1.

b

If we consider the impedance of the group  $R_1$ ,  $C_1$  and  $R_3$  as  $Z_1$  and the impedance of the group  $R_2$ ,  $C_2$  and  $R_4$  as  $Z_2$ , we can get the circuit diagram seen in figure 2. This circuit essentially operates as an inverting amplifier and hence the relationship between the output and input is given as:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{Z_2}{Z_1}$$

Where:

$$Z_1 = \frac{R_3 * (R_1 + (1/sC_1))}{R_3 + (R_1 + (1/sC_1))} = \frac{R_3(sR_1C_1 + 1)}{s(R_1C_1 + R_3C_1) + 1}, \text{ and}$$

$$Z_2 = \frac{R_4 * (R_2 + (1/sC_2))}{R_4 + (R_2 + (1/sC_2))} = \frac{R_4(sR_2C_2 + 1)}{s(R_2C_2 + R_4C_2) + 1}$$

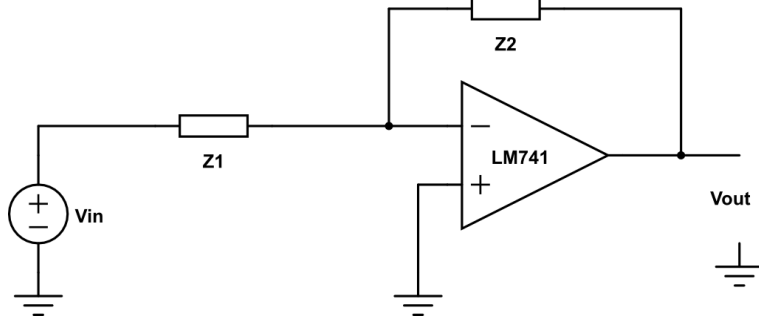


Figure 2: Simplified lead-lag compensator circuit diagram.

Thus the gain of the system can now be re-written as:

$$\begin{aligned} \frac{V_{out}(s)}{V_{in}(s)} &= -\frac{R_4(sR_2C_2 + 1)}{(s(R_2C_2 + R_4C_2) + 1)} \frac{(s(R_1C_1 + R_3C_1) + 1)}{R_3(sR_1C_1 + 1)} \\ &= -\frac{R_4}{R_3} \frac{(sR_2C_2 + 1)}{(s(R_2C_2 + R_4C_2) + 1)} \frac{(s(R_1C_1 + R_3C_1) + 1)}{(sR_1C_1 + 1)} \end{aligned}$$

We see that the op-amp operates as an inverting amplifier. In order to match the required transfer function, we need to account for the additional  $-\frac{R_4}{R_3}$  gain, which we can do by passing the output of the circuit through another inverting amplifier which has a gain of  $-\frac{R_3}{R_4}$ <sup>1</sup>. Comparing our final transfer function with what is asked in the question, we get:

$$\left(-\frac{R_4}{R_3} \times -\frac{R_3}{R_4}\right) \frac{(sR_2C_2 + 1)}{(s(R_2C_2 + R_4C_2) + 1)} \frac{(s(R_1C_1 + R_3C_1) + 1)}{(sR_1C_1 + 1)} = \frac{(1 + 0.1s)(1 + 5s)}{(1 + 0.01s)(1 + 10s)}$$

Comparing the LHS and the RHS, we see:

$$R_1C_1 = 0.01$$

$$R_2C_2 = 5$$

$$R_1C_1 + R_3C_1 = 0.01 + R_3C_1 = 0.1$$

$$\implies R_3C_1 = 0.09$$

$$R_2C_2 + R_4C_2 = 5 + R_4C_2 = 10$$

$$\implies R_4C_2 = 5$$

$$\therefore R_4 = R_2$$

**c**

While building this circuit, we made the following assumptions:

- We are using an ideal op-amp, i.e. the input impedance is infinite and the output impedance is negligible. This implies that the op-amp does not load it's input circuit and loading effects are not seen on the op-amps output terminal.
- The voltage at the non-inverting terminal is equal to the voltage at the inverting terminal.
- The open loop op-amp gain is infinite.

<sup>1</sup>For practical purposes this second op-amp is implemented in LabView as a negative gain.

- The op-amp will operate in an ideal manner when the output is not saturated above or below its supply limits.
- We used potentiometers to tune the resistors to their required value but none of the components used were ideal. For the most part we assumed the values of that the resistors were accurate and that capacitors had negligible internal resistance.

**d**

We can determine the ratings of the components by arbitrarily setting  $C_1$  and  $C_2$ . We set the capacitances because the values available to us is limited whereas we have significantly more flexibility with choosing resistances. By fixing  $C_1$  and  $C_2$  we find:

$$R_1 = \frac{0.01}{C_1}$$

$$R_2 = \frac{5}{C_2}$$

$$R_3 = \frac{0.09}{C_1}, \text{ and}$$

$$R_4 = R_2$$

We additionally see that the gain of the inverting op-amp lead-lag circuit is proportional to  $\frac{R_4}{R_3}$ . We want to limit this so that the output does not get saturated while trying to amplify the signal by a large amount. As we need to use an input amplitude of up to 2V in part (i), for a input supply of +/- 15V, we would like to limit the op-amp output to +/- 10V. Hence we want the gain,  $\frac{R_4}{R_3}, \approx 5$ .

$$\frac{R_4}{R_3} \approx 5 \implies \frac{(5/C_2)}{(0.09/C_1)} \approx 5$$

$$\therefore \frac{C_1}{C_2} = 0.09$$

For this circuit we chose  $C_1 = 2.2\mu F$ , hence ratings of the other components became:

Component Name	Component Type	Component Specification
$C_1$	Electrolytic Capacitor	$2.2\mu F$
$C_2$	Electrolytic Capacitor	$22\mu F$
$R_1$	Resistor	$454\Omega$
$R_2$	Resistor	$227K\Omega$
$R_3$	Resistor	$40.9K\Omega$
$R_4$	Resistor	$227K\Omega$

**e**

Physical implementation.

**f**

**g**

**h**

**i**

Table shows the output phase and amplitude ratios obtained when varying the input amplitude from 0.5 V to 2 V at 1Hz and 2Hz input sine waves. Theoretically we would expect the output phase and amplitude

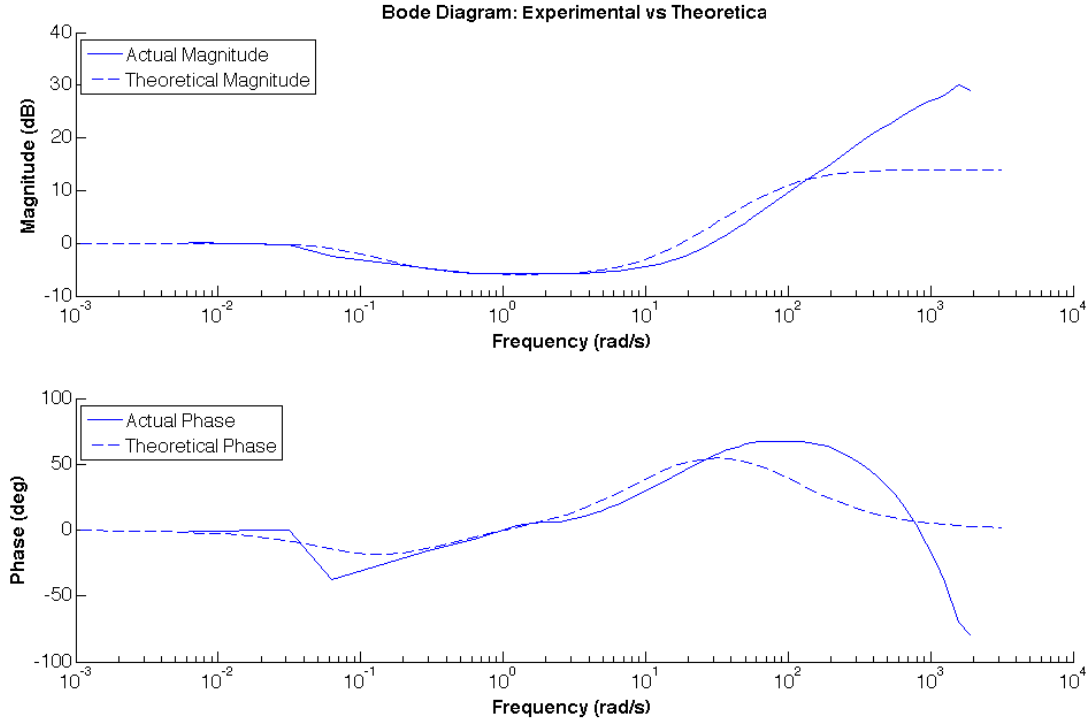


Figure 3: Bode Plot of Theoretical System and Actual System

ratio to remain constant at a given frequency for any input amplitude. The magnitude of the bode plot gives the ratio of the output to input at a particular frequency while the phase portion gives the phase at that frequency and both are independent of the input amplitude. Across different frequencies we would expect the phase and amplitude ratios to vary according to the bode plot.

Experimentally this seems to be the case at a 1Hz input, but it is not the case for the 100 Hz input. We can notice that at 1Hz the input amplitudes chosen avoid saturating the system, while the 100Hz signal saturates the system such that output can not increase with increasing input voltage. As our system inherently also has an additional gain of  $5.556^2$ , and due to the fact that we are using non-ideal op-amps that cannot output the entire input-power range, we see that the system saturates while trying to output more than 10.3 Volts.

Input Frequency (Hz)	Input Amplitude (V)	Output Phase (degrees)	Output Magnitude Ratio
1	0.5	21.0959	0.548067
1	1	19.8599	0.548165
1	2	21.1367	0.549704
100	0.5	-24.2329	4.83643
100	1	-23.8303	2.61935
100	2	-24.7609	1.23915

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<sup>2</sup>  $\frac{R_4}{R_3} = 5.556$

j

We generated the Bode Diagram by using a pair of Tone Measurement blocks to extract the amplitude and phase of the input and output signals and then subtract these phases to yield the phase difference and divide the output amplitude by the input amplitude to generate the magnitude ratio. We selected a range of frequencies running the system at each frequency and then making note of the resulting phase and amplitude ratio by hand.

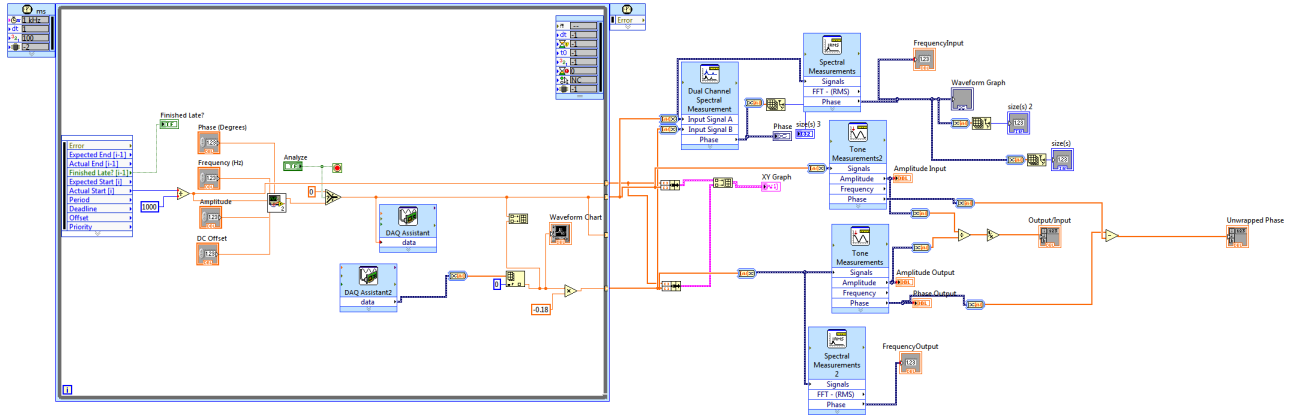


Figure 4: LabView Block Diagram for Extracting Phase and Magnitude Ratio

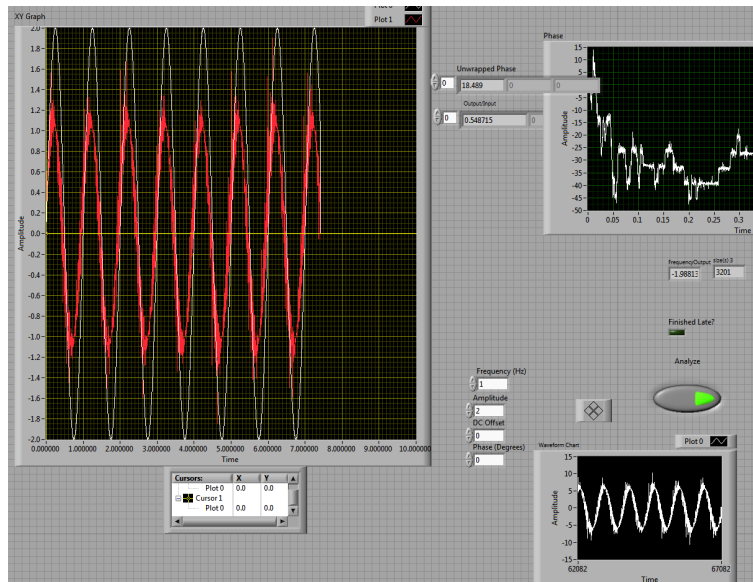


Figure 5: LabView Front Panel for extracting Phase and Magnitude Ratio

## Question 2

a

The circuit diagram can be seen in figure 6.

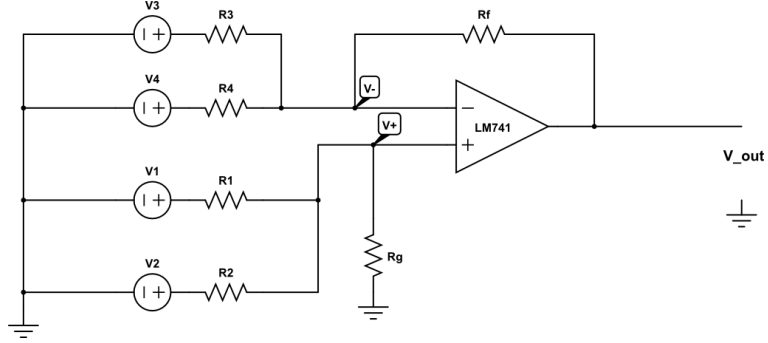


Figure 6: The required circuit diagram for question 2.

b

Circuit analysis:

At the non-inverting terminal, we effectively have a circuit represented by figure 7. We can use Kirchoff's voltage law along with the superposition theorem, we see:

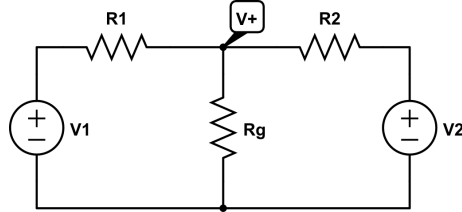


Figure 7: Equivalent circuit at the non-inverting terminal

Voltage at  $V^+$  due to  $V_1$ ,  $V_1^+$ , is given by:

$$V_1^+ = \frac{\frac{R_2 R_g}{R_2 + R_g}}{R_1 + \frac{R_2 R_g}{R_2 + R_g}} V_1$$

$$\therefore V_1^+ = \left( \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} \right) V_1$$

Similarly, voltage at  $V^+$  due to  $V_2$ ,  $V_2^+$ , is given by:

$$V_2^+ = \frac{\frac{R_1 R_g}{R_1 + R_g}}{R_2 + \frac{R_1 R_g}{R_1 + R_g}} V_2$$

$$\therefore V_2^+ = \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} V_2$$

Using the superposition theorem to recombine the values, we find that  $V^+$  is given by:

$$V^+ = V_1^+ + V_2^+$$

$$V^+ = \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} V_1 + \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} V_2$$

We can now move on to the inverting terminal of the op-amp. The corresponding equivalent circuit is shown in figure 8. Analyzing this circuit, we see that:

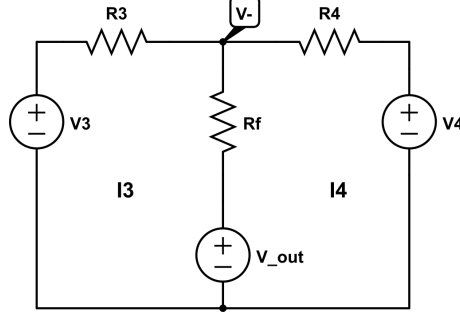


Figure 8: Equivalent circuit at the non-inverting terminal

$$I_3 R_3 = V_3 - V^-$$

$$I_4 R_4 = V_4 - V^-$$

$$V^- - V_{out} = (I_3 + I_4) R_f$$

Substituting from the above equations, we get:

$$V^- - V_{out} = \left( \frac{V_3 - V^-}{R_3} + \frac{V_4 - V^-}{R_4} \right) R_f$$

Reordering the terms, we get:

$$V_{out} = V^- - \left( \frac{V_3 - V^-}{R_3} + \frac{V_4 - V^-}{R_4} \right) R_f$$

$$\Rightarrow V_{out} = V^- \left( \frac{R_f}{R_3} + \frac{R_f}{R_4} + 1 \right) - \left( \frac{R_f}{R_3} \right) V_3 - \left( \frac{R_f}{R_4} \right) V_4$$

We also know that for an ideal op-amp,  $V^+ = V^-$ , hence we get:

$$V_{out} = \left( \frac{R_f}{R_3} + \frac{R_f}{R_4} + 1 \right) \left( \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} \right) V_1 + \left( \frac{R_f}{R_3} + \frac{R_f}{R_4} + 1 \right) \left( \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} \right) V_2 - \left( \frac{R_f}{R_3} \right) V_3 - \left( \frac{R_f}{R_4} \right) V_4$$

This is equation is the mathematical representation of the problem statement which which required  $V_{out} = a_1 V_1 + a_2 V_2 - a_3 V_3 - a_4 V_4$ , i.e. :

$$a_1 = \left( \frac{R_f}{R_3} + \frac{R_f}{R_4} + 1 \right) \left( \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} \right) = 1$$

$$a_2 = \left( \frac{R_f}{R_3} + \frac{R_f}{R_4} + 1 \right) \left( \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} \right) = 2$$

$$a_3 = \left( \frac{R_f}{R_3} \right) = 3$$

$$a_4 = \left( \frac{R_f}{R_4} \right) = 4$$

**c**

While building this circuit, we made the following assumptions:

- We are using an ideal op-amp, i.e. the input impedance is infinite and the output impedance is negligible. This implies that the op-amp does not load it's input circuit and loading effects are not seen on the op-amps output terminal.
- The voltage at the non-inverting terminal is equal to the voltage at the inverting terminal.
- The open loop op-amp gain is infinite.
- The op-amp will operate in an ideal manner when the output is not saturated above or below its supply limits.
- We used potentiometers to tune the resistors to their required value but none of the components used were ideal components. But for the most part we assumed the values of the resistors were accurate and that capacitors had negligible internal resistance.

**d**

We started by choosing  $R_f$ ,  $R_g$  and  $R_g$  to arbitrary resistances such that they were large enough to make sure that other resistances in the circuit were not small. By this we mean that the values of the other resistances were in the order of Kilo-Ohms. From section **b**, we can rewrite gains  $a_1$  and  $a_2$  in terms of  $a_3$  and  $a_4$  as follows:

$$\begin{aligned} a_1 &= (a_3 + a_4 + 1) \left( \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} \right) = 1 \\ &= (8) \left( \frac{1}{\frac{R_1}{R_g} + \frac{R_1}{R_2} + 1} \right) = 1 \end{aligned}$$

We can rewrite this as:

$$\begin{aligned} 8R_2R_g &= R_1R_2 + R_1R_g \\ \implies R_g &= \frac{R_1R_2}{7R_2 - R_1} \end{aligned}$$

Similarly for  $a_2$ , we see:

$$\begin{aligned} a_2 &= (a_3 + a_4 + 1) \left( \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} \right) = 2 \\ &= (8) \left( \frac{1}{\frac{R_2}{R_g} + \frac{R_2}{R_1} + 1} \right) = 2 \end{aligned}$$

We can re-arrange and re-write the above equations as:

$$R_g = \frac{R_1R_2}{3R_1 - R_2}$$

Equating the two equations which equal  $R_g$ , we get:

$$\frac{R_1R_2}{7R_2 - R_1} = \frac{R_1R_2}{3R_1 - R_2}$$



Thus, we get:

$$R_2 = \frac{R_1}{2}$$

Thus we arbitrarily chose  $R_f = R_g = 10\text{ K}\Omega$  and  $R_1 = 50\text{ K}\Omega$  We ended up using the following components in our circuit:

Component Name	Component Type	Component Specification
$R_f$	Resistor	9.880 $K\Omega$
$R_g$	Resistor	9.860 $K\Omega$
$R_1$	Resistor	49.3 $K\Omega$
$R_2$	Resistor	24.65 $K\Omega$
$R_3$	Resistor	3.293 $K\Omega$
$R_4$	Resistor	2.470 $K\Omega$

e

To obtain the resistances specified above we used a combination of potentiometers and fixed resistors which were assembled and then tuned to the correct resistance using a multi-meter.

f

After constructing the circuit as detailed above we began by feeding the following DC signals into our system and measuring the output to confirm its functionality. These results can be seen in table 1.

Set	V1 (VDC)	V2 (VDC)	V3 (VDC)	V4 (VDC)	Expected Vout (VDC)	Actual Vout (Avg V)
1	2	4	1	3	-5	-4.9177
2	6	4	2	1	4	4.0988
3	6	7	2	3	2	2.17

Table 1: DC inputs, Expected Output, and Actual Output

The actual voltages in table 1 were obtained by averaging the output voltage for several seconds in matlab. The inputs and outputs for Set 3 are shown in figure 9.

Our VI for generating these inputs and reading the outputs is shown in figure 10

g

After confirming that the circuit functioned correctly on DC signals we moved on to feed in AC signals and record the output. These inputs are shown in table 2.

Figure 11 shows the output for set 1 superimposed on the simulated inputs and the expected output of the system.

Figure 12 shows the output for set 2 superimposed on the simulated inputs to the system and the expected output of the system, while figure 13 shows this output within labview for confirmation.

Both figure 11 and figure 12 show a close correspondence between the actual and expected output with a few notable differences. The most obvious difference is the lag between the actual output and the expected output. When generating these graphs we assume a uniform 1 ms sampling period, which turns out to not be the case when examining real timing data. This discrepancy is the result of the system requesting a sample, since we are using on demand sampling, but not receiving the sample in time. As a consequence of this the time difference between some of the output samples are larger than 1 ms, which on a whole cause fewer than 1000 samples to be taken per second. This compresses the graph along the time axis resulting in a graph that

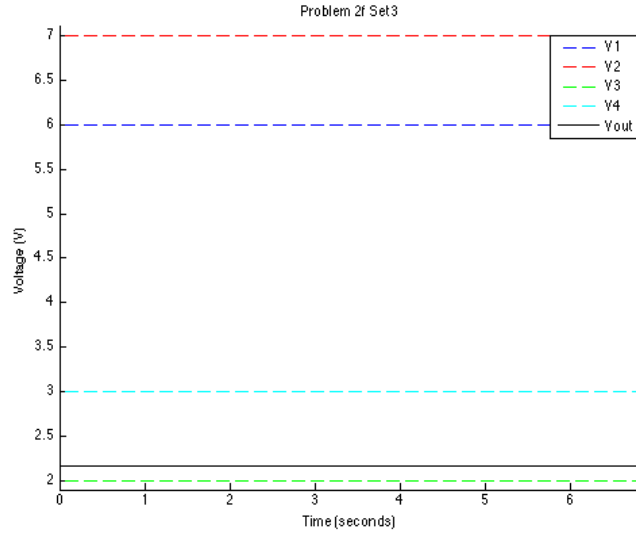


Figure 9: Set 3 Inputs and Outputs

;

Set	Set 1				Set 2			
Inputs	V1	V2	V3	V4	V1	V2	V3	V4
Amplitude (V)	3	6	0	0	0	0	2	3
Frequency (Hz)	4	4	0	0	0	0	2	2
Offset (V)	0	0	0	0	0	0	2	0
Phase (Degrees)	0	90	0	0	0	0	0	45

Table 2: Set 1 and Set 2 inputs

is out of synch with the expected results. This issue could be easily remedied by storing the sampled amplitude and the sample time and plotting the amplitude against the actual time rather than the theoretical time.

Both figure 11 and figure 12 also illustrate a saturation effect at  $\pm 11$  volts. For an ideal op-amp we would expect the output to saturate at the supply voltages which were confirmed to be  $\pm 15$  volts. However we would not expect a real op-amp, such as our LM741, to output voltages all the way up to the supply voltage, but rather within about 2 volts of the supply. But this does not explain the saturation at  $\pm 11$  volts. Examining the data sheet of our DAQ, the NI 6230 reveals a maximum input voltage of  $\pm 10$  volts. It is likely that the designers are being somewhat conservative in their estimate of input ranges, so a saturation at 11 volts is likely due to the limited range of the DAQ.

## h

The beating signal is achieved as a sinusoidal wave which has an amplitude that also varies sinusoidally. In effect, the output is  $\sin(\omega_a t) \sin(\omega_b t)$ . We can use trigonometric identities to rearrange this sinusoidal product as a sum as follows:

$$\sin(\omega_a t) \sin(\omega_b t) = \frac{\cos(\omega_a t + \omega_b t) - \cos(\omega_a t - \omega_b t)}{2}$$

We use the product-to-sum identity to break up the product of the sines into a sum of cosines. We can again rewrite the cosines in terms of sines by taking into account the phase difference.

$$\frac{\cos(\omega_a t + \omega_b t) - \cos(\omega_a t + \omega_b t)}{2} = \frac{\sin((\omega_a t + \omega_b t) + \pi/2) - \sin((\omega_a t + \omega_b t) + \pi/2)}{2}$$

This way, we can achieve a beating signal as a sum of sinusoids. For the purposes of this question, we chose  $\omega_a = 1$  and  $\omega_b = 10$ . The values for each of the output terminals is as follows:

	V1	V2	V3	V4
Amplitude (Volts)	3	0	1	0
Frequency (Hz)	-9	0	11	0
Offset (Volts)	0	0	0	0
Phase (Radians)	$\frac{\pi}{2}$	0	$\frac{\pi}{2}$	0

The required LabView screen shot can be seen in figure 14 while the graph itself may be seen in figure 15.

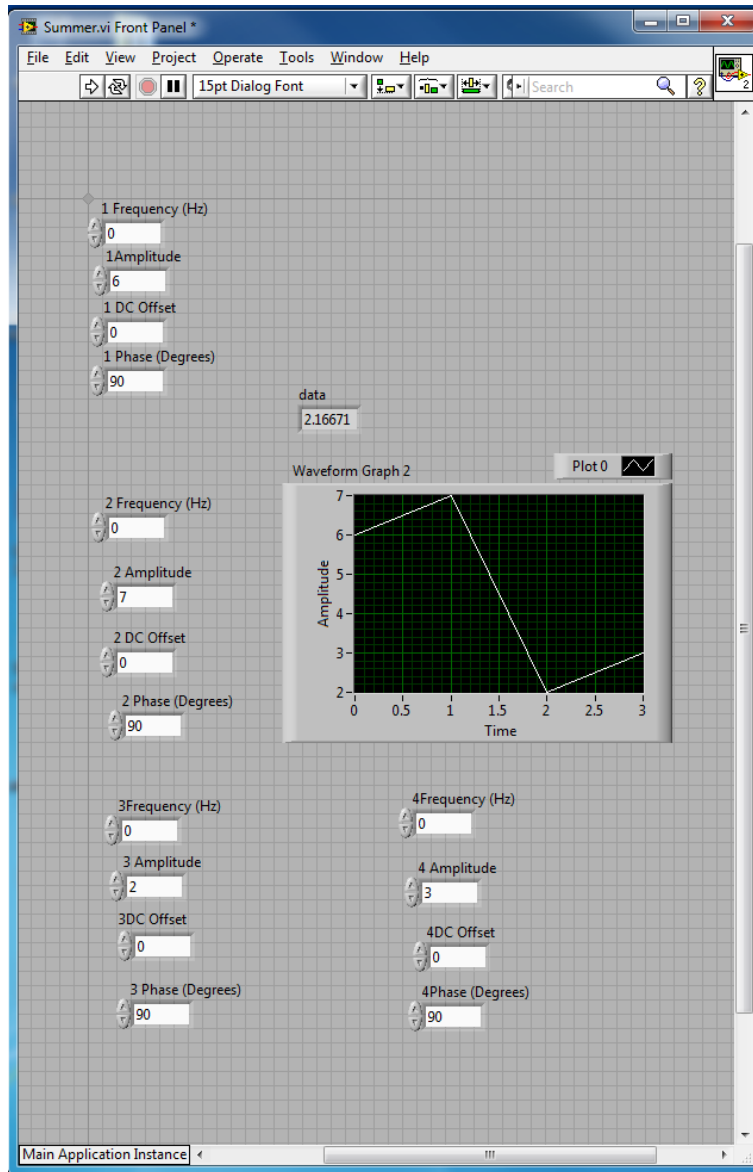


Figure 10: Set 3 VI

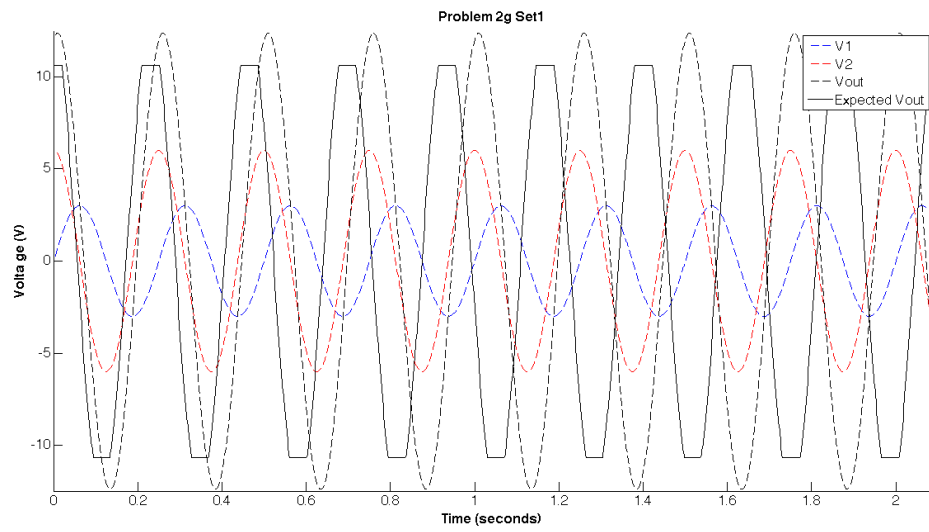


Figure 11: Set 1 Input and Output

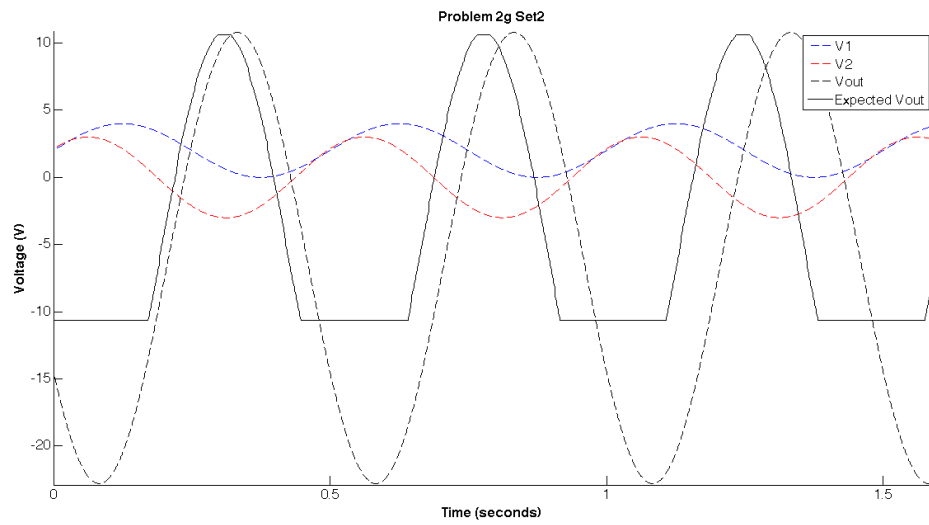


Figure 12: Set 2 Input and Output

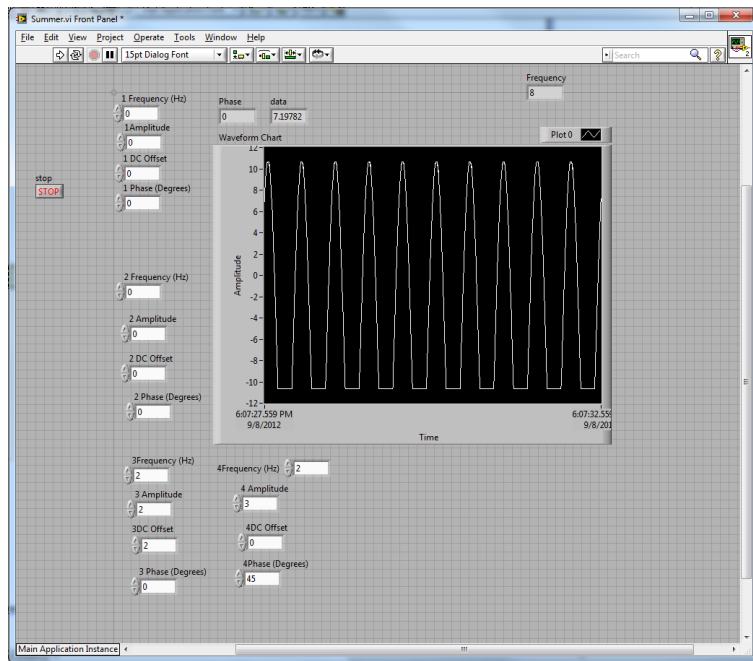


Figure 13: Set 2 Output within LabView

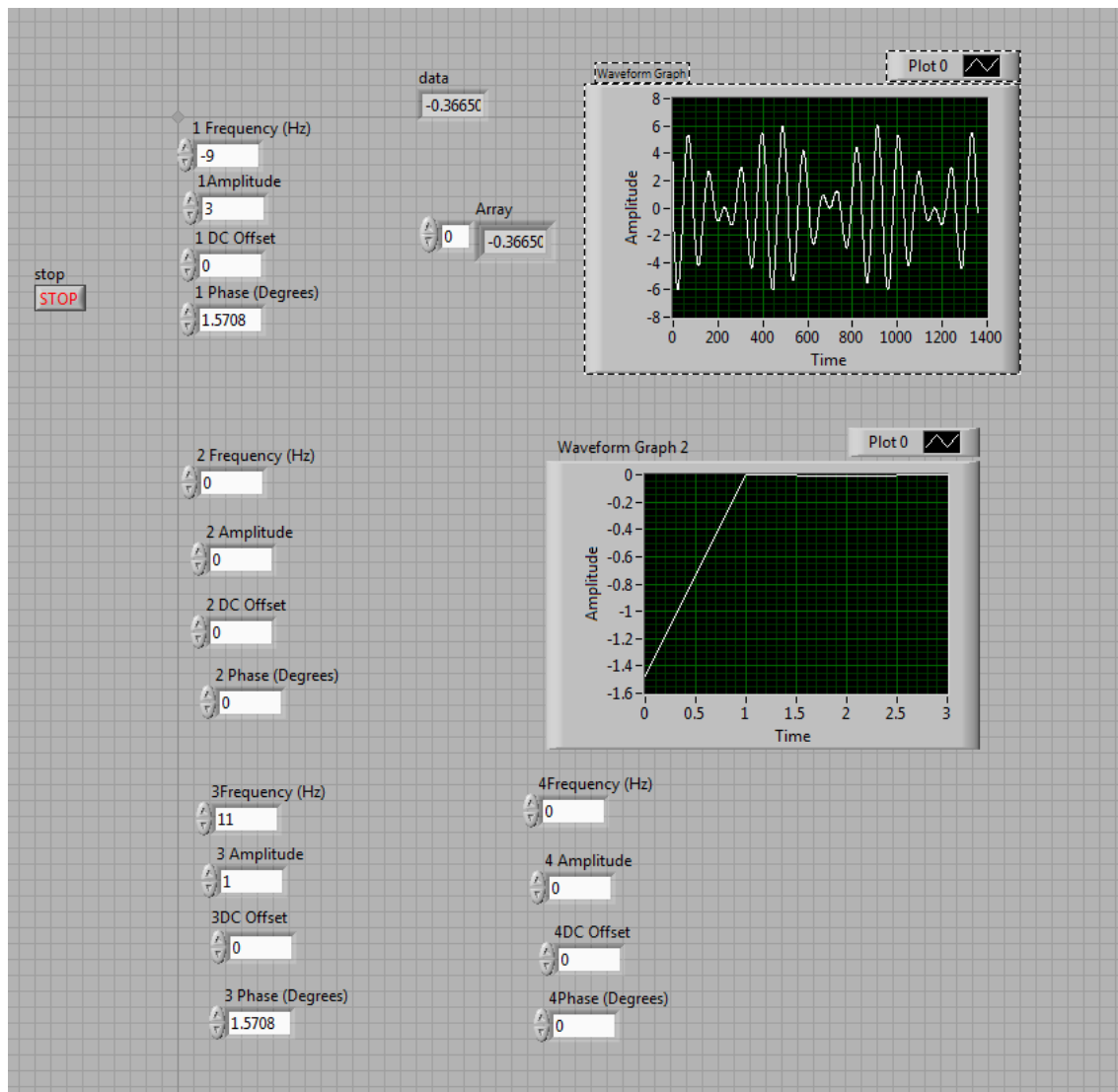


Figure 14: The LabView front-end of a system that produces  $\sin(\omega_a t_a) \sin(\omega_b t_b)$ .

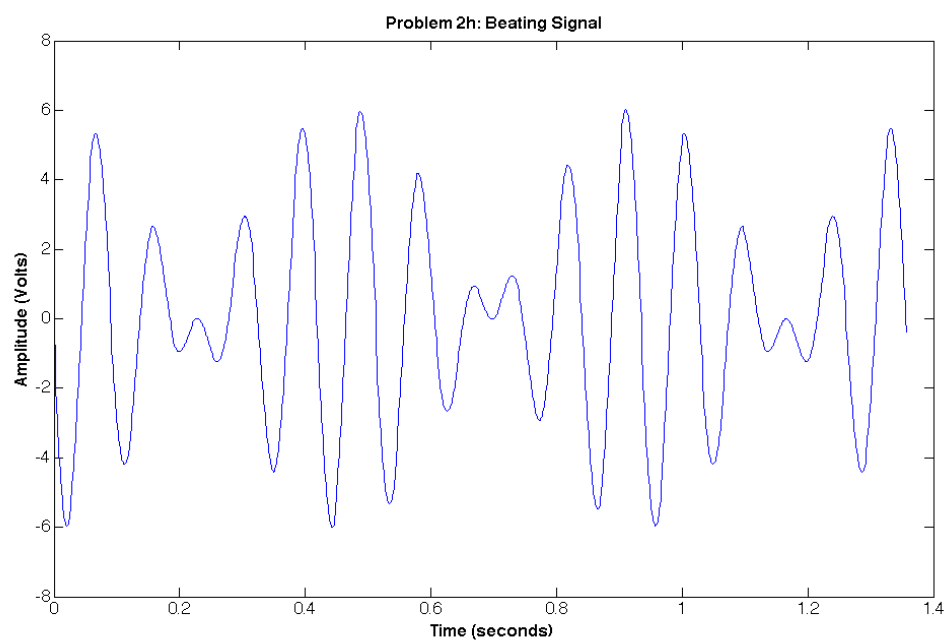


Figure 15: Problem 2h recieved signal