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EDUCATION

Veer Bahadur Singh Purvanchal University — Jaunpur, U.P., India
Bachelor of Technology (B.Tech) | Electronic & Communication Engineering *2020–2024* | Percentage: 68.32%

TRAINING & EXPERIENCE

Trainee - Fundamentals of VLSI Design
VLSI Expert Pvt. Ltd., Noida, U.P., India | July 2024 – Present

Key Learning:

- **Linux Fundamental & Scripting**: Overview of Linux operating system architecture, basic commands, shell scripting, file system navigation, environment and path variable management, and efficient text editing using *vi/vim* editor.
- **Layout Design**: Development of stick diagrams, understanding and prevention of latch-up in CMOS circuits, layout folding techniques for area optimization, and methodologies for full-custom and semi-custom VLSI design
- **Parasitic Extraction & Verification:** Understanding of Layout vs Schematic (LVS) checks, Design Rule Checking (DRC) to to ensure manufacturability, Layout Parasitic Extraction (LPE) for accurate post-layout performance analysis, and interpretation of parasitic impact on circuit behavior.
- **CMOS Design:** Understanding of MOSFET operation principles, CMOS fabrication processes, threshold voltage considerations, and scaling challenges in modern semiconductor technology.
- **Verilog HDL & Digital Modeling:** Structured modeling at gate-level, dataflow, and behavioral abstraction levels, Finite State Machine (FSM) design including Moore and Mealy models, switch-level transistor modeling, and comprehensive test bench development for functional and timing verification.
- **Physical Design & Verification:** Complete physical implementation flow, including logic synthesis (RTL to gate-level netlist), efficient floor planning for optimal area and performance, power planning and power grid design to ensure reliable power distribution, strategic placement of standard cells and macros, Clock Tree Synthesis (CTS) for balanced and low-skew clock networks, and global and detailed routing to meet timing, congestion, and design rule constraints.

Key Project:

- **Schematic & Layout Design:** Designed and simulated transistor-level layouts for PMOS, NMOS, NOT, NAND, NOR, XOR, AND, OR gates, as well as Half Adder and Full Adder using Synopsys tools. Conducted DRC, LVS, and LPE checks.
- **Verilog HDL Projects:** Developed 4-bit Full Adder, 4-bit comparator, 4-bit up-down counter, ripple carry adder, synchronous full adder, and BCD seven-segment display.
- **RTL Design:** Created and verified Verilog-based RTL for combinational and sequential circuits through comprehensive simulations.

PROJECTS

Design & Implementation of 4-Bit Arithmetic Logical Unit (ALU) using CMOS Technology

- Designed basic **CMOS** logic gates such as **AND, OR, XOR**, and components like **Multiplexers** and **Full Adders**
- Developed **1-bit** and **4-bit ALU**, complete with block diagrams and schematic verification through truth tables
- Performed performance evaluation based on complexity, **Delay**, and **Power Consumption** under various input conditions through simulation experiments
- Gained hands-on experience with industry-standard tools such as **Cadence Virtuoso**

Design and Implementation of a 16-BIT ALU, Full Subtractor & Full Adder(4-bit, 8-bit & 32-bit) from RTL to GDSII Flow

- Designed and performed logic synthesis to generate gate-level netlist using standard cell libraries
- Executed complete physical design flow including floor planning, power planning, placement, clock tree synthesis (CTS), and routing
- Successfully resolved **Design Rule Check (DRC)** and **Layout vs. Schematic (LVS)** violations to achieve a clean and verified layout
- Gained hands-on experience with industry-standard tools such **SYNOPSYS Design Compiler & IC Compiler**

TECHNICAL SKILLS

- **EDA Tools**: Cadence (Virtuoso & PSpice),Synopsys(HSpice, IC Compiler, IC Validator,Design Compiler, StarRC, SPYGLASS, Custom Compiler, Verdi)
- **Programming & Scripting Languages**: Verilog HDL,RTL Design, RTL Verification, C Programming, TCL, Shell Scripting, Linux
- **Design & Simulation**: Layout Design, Design Rule Check (DRC), Layout vs Schematic (LVS), Layout Parasitic Extraction (LPE), Standard Cell Layout
- **Digital & CMOS Design**: Digital Circuit Design, CMOS Technology, Pass Transistor

CERTIFICATIONS & TRAINING

- Certificate in Computer Concepts — NIELIT, May 2019
- VLSI Design using Cadence (Two-Week Online Training Program) — NIELIT