SHIVAKAR DUTT VERMA
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PROFILE SUMMARY

Aspiring VLSI Engineer with a foundational understanding of CMOS design, digital logic, RTL development, and verification. Proficient in using industry-standard tools such as Synopsys Verdi. Strong hands-on experience in Verilog HDL. Passionate about semiconductor technology and eager to contribute to ASIC/SoC design and verification teams.

EDUCATION

Veer Bahadur Singh Purvanchal University — Jaunpur, U.P., India
Bachelor of Technology (B.Tech) | Electronic & Communication Engineering *2020–2024* | Percentage: 68.32%

TRAINING & EXPERIENCE

Trainee - Fundamentals of VLSI Design
VLSI Expert Pvt. Ltd., Noida, U.P., India | July 2024 – Present

- **Linux Fundamental & Scripting**: Overview of Linux operating system architecture, basic commands, shell scripting, file system navigation, environment and path variable management, and efficient text editing using *vi/vim* editor.
- **Layout Design**: Development of stick diagrams, understanding and prevention of latch-up in CMOS circuits, layout folding techniques for area optimization, and methodologies for full-custom and semi-custom VLSI design
- **Parasitic Extraction & Verification:** Understanding of Layout vs Schematic (LVS) checks, Design Rule Checking (DRC) to to ensure manufacturability, Layout Parasitic Extraction (LPE) for accurate post-layout performance analysis, and interpretation of parasitic impact on circuit behavior.
- **CMOS Design:** Understanding of MOSFET operation principles, CMOS fabrication processes, threshold voltage considerations, and scaling challenges in modern semiconductor technology.
- **Digital Electronics:** Understanding of Boolean expressions, logic gates, flip-flops, counters, multiplexers, and binary representation.
- **Verilog HDL & Digital Modeling:** Structured modeling at gate-level, dataflow, and behavioral abstraction levels, Finite State Machine (FSM) design including Moore and Mealy models, switch-level transistor modeling, and comprehensive test bench development for functional and timing verification.
- **RTL Design & Verification:** Developed and simulated various combinational and sequential logic modules using Verilog HDL.
- **Logic Synthesis:** Conversion of RTL code to gate-level netlists using standard cell libraries.

PROJECTS

Design & Implementation of 4-Bit Arithmetic Logical Unit (ALU) using CMOS Technology

- Designed basic **CMOS** logic gates such as **AND, OR, XOR**, and components like **Multiplexers** and **Full Adders**
- Developed **1-bit** and **4-bit ALU**, complete with block diagrams and schematic verification through truth tables
- Performed performance evaluation based on complexity, **Delay**, and **Power Consumption** under various input conditions through simulation experiments
- Gained hands-on experience with industry-standard tools such as **Cadence Virtuoso**

Design and Devoloped of a 16-BIT ALU, Counter, Full Subtractor & Full Adder(4-bit, 8-bit & 32-bit) from RTL

- Implemented RTL architecture using modular, reusable, and synthesizable code following best hardware design practices.
- Performed functional simulation and **RTL verification** using testbenches to ensure correctness of logic under various input scenarios.
- Conducted logic synthesis using **standard cell libraries** to generate gate-level netlists, optimizing for area and timing.
- Debugged and analyzed waveform outputs using **Synopsys Verdi**, resolving functional and timing issues during simulation.

TECHNICAL SKILLS

- **EDA Tools**: Cadence (Virtuoso & PSpice),Synopsys(HSpice, IC Compiler, IC Validator,Design Compiler, StarRC, SPYGLASS, Custom Compiler, Verdi)
- **Programming & Scripting Languages**: Verilog HDL,RTL Design, RTL Verification, C Programming, TCL, Shell Scripting, Linux
- **Design & Simulation**: Layout Design, Design Rule Check (DRC), Layout vs Schematic (LVS), Layout Parasitic Extraction (LPE), Standard Cell Layout
- **Digital & CMOS Design**: Digital Circuit Design, CMOS Technology, Pass Transistor

CERTIFICATIONS & TRAINING

- Certificate in Computer Concepts — NIELIT, May 2019
- VLSI Design using Cadence (Two-Week Online Training Program) — NIELIT