Design and Implementation of Low Noise Amplifier Using Cadence Virtuoso

Project Seminar Report submitted in partial fulfillment of the academic requirement for the award of the degree of

BACHELOR OF ENGINEERING

In

ELECTRONICS AND COMMUNICATION ENGINEERING

By

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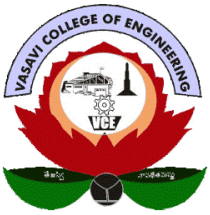

Department of Electronics and Communication Engineering

Vasavi College of Engineering (Autonomous)

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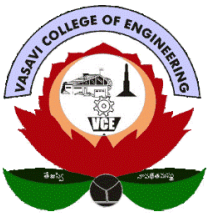
2024-2025



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CERTIFICATE

This is to certify that the project seminar report titled **"Design and Implementation of Low Noise Amplifier Using Cadence Virtuoso"** submitted by

Shivakalyan Gupta Pola **1602-21-735-115**

students of Electronics and Communication Engineering Department, Vasavi College of Engineering in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering is a record of the bonafide work carried out by them during the academic year 2024-2025. The result embodied in this project report has not been submitted to any other university or institute for the award of any degree

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External Examiner

DECLARATION

This is to state that the work presented in this thesis titled **"Design and Implementation of Low Noise Amplifier Using Cadence Virtuoso"** is a record of work done by us in the Department of Electronics and Communication Engineering, Vasavi College of Engineering, Hyderabad. No part of the thesis is copied from books/journals/internet and wherever the portion is taken, the same has been duly referred in the text. The report is based on the project work done entirely by us and not copied from any other source. I hereby declare that the matter embedded in this thesis has not been submitted by me in full or partial thereof for the award of any degree/diploma of any other institution or university previously.

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ABSTRACT

The project "Design and Implementation of Low Noise Amplifier (LNA) using Cadence Virtuoso" aims to develop an advanced LNA for RF applications, focusing on high sensitivity and low noise performance. LNAs are crucial components in modern communication and sensing systems, enabling effective signal reception by amplifying weak signals with minimal noise degradation. This work specifically targets operation at 2.4 GHz, a widely used frequency in wireless communications, with a design that meets stringent parameters such as a noise figure below 6 dB, a gain exceeding 15 dB, and an input third-order intercept point (IIP3) greater than -10 dBm.

The project is motivated by the growing demand for highly efficient and reliable RF front-end systems in applications such as telecommunications, radar systems, satellite communications, GPS receivers, and wireless technologies. Among various LNA topologies, the inductive degeneration configuration was selected due to its superior noise performance, wide bandwidth, and effective impedance matching.

The design process involves comprehensive theoretical analysis and iterative simulations using Cadence Virtuoso. This includes DC biasing, transient and frequency analysis, noise figure optimization, and linearity enhancement. Key challenges addressed during the design include achieving stability across the operating frequency, ensuring impedance matching at input and output ports, and minimizing power consumption to suit energy-efficient applications.

The expected outcomes of this project are an LNA design that offers robust performance with optimized noise characteristics and enhanced gain. The results will contribute to improving the overall efficiency and reliability of communication systems, making this design a viable solution for next-generation RF technologies. The project also provides a foundation for further research in noise optimization and advanced LNA configurations for high-frequency applications.

LIST OF CONTENTS

CH-1. INTRODUCTION

1.1 Introduction:

This chapter introduces the motivation behind the project, which is focused on enhancing the sensitivity and reliability of communication systems by designing an efficient Low Noise Amplifier (LNA). The project aims to address critical challenges such as noise reduction, impedance matching, and gain optimization. It outlines the goal of developing a robust LNA design that leverages inductive degeneration topology and advanced simulation tools, such as Cadence Virtuoso, to achieve superior noise performance, improved linearity, and optimal gain, thereby ensuring effective signal amplification in RF applications.

1.2 Aim:

The Low Noise Amplifier (LNA) design is focused on amplifying weak RF signals while maintaining a low noise figure and ensuring signal integrity. The aim is to create an LNA that achieves high gain, minimal noise, and effective impedance matching, enabling efficient signal transmission and reception. The design will ensure stability across the desired frequency range and maintain optimal performance metrics such as linearity, low distortion, and reduced power consumption, without introducing artifacts like signal degradation or instability.

1.3 Motivation:

In recent years, Low Noise Amplifiers (LNAs) have become indispensable in various fields, including telecommunications, satellite communication, radar systems, and wireless technologies. Their ability to amplify weak signals while preserving signal integrity offers significant advantages for enhancing communication system performance and ensuring reliable data transmission.

However, existing LNA designs often face challenges such as high noise figures, poor impedance matching, limited gain, and inadequate linearity, which can compromise overall system efficiency. To address these issues, this project focuses on designing a robust LNA using inductive degeneration topology, leveraging Cadence Virtuoso for precise simulation and optimization. The goal is to achieve superior noise performance, enhanced gain, and improved linearity to meet the demands of modern RF applications.

1.4 Technical Motivation:

The main aim of this project is to enhance the performance of communication systems by designing a Low Noise Amplifier (LNA) that effectively amplifies weak signals while minimizing noise and distortions. The focus is on achieving optimal gain, linearity, and impedance matching to ensure reliable signal transmission and reception. This improved LNA design is intended to operate efficiently at 2.4 GHz, making it suitable for a wide range of applications such as telecommunications, satellite communication, radar systems, and wireless technologies.

1.5 Approach:

The design and implementation of the Low Noise Amplifier (LNA) are carried out in a structured manner through the following steps:

Step 1:

Select an appropriate topology for the LNA, such as inductive degeneration, based on the desired frequency, gain, and noise performance requirements.

Step 2:

Design the LNA circuit using the chosen topology, defining the initial component values and layout.

Step 3:

Perform a DC simulation to ensure proper biasing and determine whether the circuit meets the power requirements. If not, adjust the DC bias and re-simulate.

Step 4:

Simulate the circuit to verify input and output impedance matching (S11 and S22 parameters). If the matching is not achieved, refine the values of inductors and capacitors.

Step 5:

Conduct gain, noise figure (NF), and linearity simulations to evaluate the overall performance of the LNA. If the desired specifications are not met, adjust the width of the MOSFETs and optimize the circuit parameters.

Step 6:

Iterate through the above steps until the design meets all performance metrics, including power, impedance matching, gain, noise figure, and linearity.

Step 7:

Finalize the design once all requirements are satisfied, completing the LNA development process.

1.6 Discussion:

The Low Noise Amplifier (LNA) design process focuses on amplifying weak RF signals while minimizing noise and ensuring signal integrity. It involves multiple steps and methodologies, including DC biasing, impedance matching, inductive degeneration, and optimization of gain and noise performance. The design is carried out using Cadence Virtuoso simulation tools to achieve precise results.

The process begins by selecting the appropriate topology for the LNA, such as inductive degeneration. This topology is chosen to ensure a high gain and low noise figure while maintaining impedance matching and stability. The initial design parameters, including transistor dimensions, biasing values, and component placements, are defined based on the desired operating frequency and application requirements.

The next step involves performing a DC simulation to verify the proper biasing of the circuit. If the power requirements are not met during this simulation, the DC bias is adjusted iteratively until the desired results are achieved.

Once the biasing is optimized, the input and output impedance matching (S11 and S22) are analysed. Inductors and capacitors are adjusted to ensure the LNA achieves optimal matching, reducing signal reflections and improving efficiency.

After achieving proper impedance matching, gain, noise figure (NF), and linearity simulations are conducted. The MOSFET widths are adjusted as needed to fine-tune the performance metrics, ensuring high gain, minimal noise, and reduced distortion.

The final step involves validating the design against all performance requirements. The optimized LNA design is capable of amplifying weak RF signals effectively while maintaining a low noise figure and ensuring stability and reliability.

The entire process is iterative, ensuring each stage of the design meets the specified criteria. The result is a high-performance Low Noise Amplifier suitable for modern RF applications such as wireless communication, satellite systems, and radar technology.

1.7 Objectives:

To improve:

1. Gain and Stability
2. Noise Figure (NF)
3. Linearity (IP3)
4. Bandwidth

- **Gain and Stability:**

  Gain represents the amplification level provided by the Low Noise Amplifier (LNA). It is a critical parameter that determines how effectively weak input signals are amplified. The stability of the LNA ensures that the circuit operates without oscillations across the intended frequency range. By carefully designing and optimizing the topology, biasing, and impedance matching, the gain is maximized while maintaining unconditional stability.

- **Noise Figure (NF):**

  The Noise Figure quantifies the additional noise introduced by the LNA in the amplification process. A lower Noise Figure indicates better performance, as it ensures minimal degradation of the signal-to-noise ratio (SNR). Techniques such as inductive degeneration and careful selection of MOSFET dimensions are used to minimize the NF, making the LNA suitable for applications requiring high sensitivity.

- **Linearity (IP3):**

  Linearity, often measured using the Third-Order Intercept Point (IP3), ensures that the LNA can handle large input signals without introducing significant distortion. Higher linearity improves the amplifier's ability to process strong and weak signals simultaneously, which is crucial for reducing intermodulation products in communication systems. Proper biasing and circuit design help to enhance the linearity of the LNA.

- **Bandwidth:**

  Bandwidth defines the frequency range over which the LNA provides the desired level of performance, including sufficient gain and low noise. A wide bandwidth ensures versatility in handling signals over a broad spectrum, while a narrow, well-defined bandwidth is critical for targeted frequency applications. By optimizing the LNA's matching networks, parasitic components, and filter characteristics, the design achieves the desired bandwidth, ensuring minimal signal loss and reliable operation

within the intended frequency range.

These objectives ensure that the LNA design achieves optimal performance by amplifying weak signals with minimal noise, maintaining signal integrity, and ensuring reliable operation across a wide range of frequencies.

1.8 Conclusion:

This chapter provides an overview of the foundation of the project, highlighting its motivation, objectives, and design approach. It outlines the significance of designing a Low Noise Amplifier (LNA) with improved performance metrics such as gain, noise figure, linearity, and bandwidth, which are critical for RF applications. The chapter also introduces the methodologies and techniques being employed in Cadence Virtuoso for the design and optimization of the LNA, setting the groundwork for achieving the desired results in terms of signal amplification with minimal noise and distortion.

CH-2. LITERATURE SURVEY

[1]. Mahdi Parvizi, Karim Allidina, Mourad N. El-Gamal , "**A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique**" , IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 23, Issue: 6, June 2015

Problem Addressed:

The paper addresses the need for designing ultra-low-voltage, wideband low-noise amplifiers (LNAs) that operate efficiently while consuming minimal power. Conventional LNAs often face challenges in achieving a balance between low power consumption and performance parameters such as gain, noise figure, and bandwidth, particularly when the voltage supply is reduced to sub-milliwatt levels.

Key Contributions:

1. Wideband Operation:
    - The proposed LNA design uses a resistive-shunt feedback topology combined with series inductive peaking to achieve wideband performance. This technique ensures a broad frequency response, accommodating signals across multiple communication bands.
2. Ultra-Low Power Consumption:
    - The design operates at a supply voltage of 0.5 V, achieving sub-milliwatt power consumption (900 µW). This ultra-low power operation is crucial for modern portable and wireless applications, where energy efficiency is paramount.
3. Noise Figure Optimization:
    - The LNA design aims to minimize the noise figure (NF) by optimizing transistor sizing and biasing. Despite the challenges of ultra-low voltage operation, the LNA achieves a measured minimum NF of 5.5 dB, with an average NF of 6 dB across the bandwidth.
4. Compact Design:
    - The active area of the chip is 0.27 mm × 0.88 mm, making it suitable for integration into small devices such as IoT sensors or wearable devices. The design also emphasizes minimizing parasitic effects by using short bond wires

and ensuring proper decoupling at the DC biasing nodes.

Experimental Results:

1. Voltage Gain:
    - The LNA achieves a maximum voltage gain of 12.6 dB at 4.5 GHz, with a 3-dB cutoff frequency of 7 GHz. This wide bandwidth and high gain make the amplifier suitable for a variety of RF applications. The gain roll-off observed at higher frequencies is attributed to parasitic inductances and capacitances introduced during the fabrication process.
2. Input Matching:
    - The S11 (input reflection coefficient) is measured to be less than −10 dB across the entire bandwidth, indicating good impedance matching, which is crucial for efficient signal amplification and minimizing signal loss.
3. Reverse Isolation and Output Matching:
    - S22 (output reflection coefficient) is measured to be less than −9 dB across the bandwidth, ensuring effective output matching. The reverse isolation (S12) is better than −23 dB within the operating band, which minimizes unwanted feedback and ensures stability.
4. Noise Figure:
    - The minimum measured noise figure (NF) is 5.5 dB, with an average NF of 6 dB across the operational bandwidth. The measured NF is slightly higher than the simulated value due to inaccuracies in the transistor noise model and the effect of bond wires used in the testing setup, which contribute additional noise.
5. Measurement Setup:
    - The LNA was tested using a probe station with an on-chip buffer driving the measurement equipment’s 50-Ω impedance. The buffer’s characteristics were de-embedded from the S21 and NF results to isolate the LNA's performance. The die photograph of the LNA, as shown in the figure, demonstrates the compact design, with the active area measuring 0.27 mm × 0.88 mm.

Strengths and Advantages:

1. Power Efficiency:
    - The LNA achieves sub-milliwatt power consumption (900 µW) while maintaining a high gain and reasonable noise figure. This makes it highly suitable for battery-operated and portable systems.
2. Wideband Performance:
    - The design exhibits wideband characteristics, with a 3-dB cutoff frequency of 7 GHz, making it versatile for various RF and communication systems.
3. Compact Form Factor:
    - The small active area (0.27 mm × 0.88 mm) and the use of short bond wires minimize parasitic inductance and capacitance, improving the LNA's overall performance in terms of noise and bandwidth.

Limitations:

1. Higher Noise Figure Than Simulated:
    - The measured noise figure of 5.5 dB is higher than the simulated value, which can be attributed to inaccuracies in transistor noise modeling and the additional noise introduced by the test setup, especially the bond wires. This can be improved by refining transistor models and optimizing the test configuration.
2. Gain Roll-Off at Higher Frequencies:
    - The gain roll-off seen at higher frequencies is likely due to parasitic inductances and capacitances in the fabricated LNA, which affect the resonant frequency of the inductors used in the design. This could be mitigated by further optimizing the layout and component values.

Comparison with Existing Works:

- Compared to traditional LNA designs, this paper's approach offers a unique balance between low power consumption, wideband operation, and reasonable noise performance. While many LNAs achieve low noise figures, this design stands out due to its ultra-low voltage and power consumption, making it ideal for modern communication systems, especially in IoT and wearable applications.

Future Directions:

1. Further Noise Reduction:
    - Techniques such as improved transistor noise modeling and more efficient decoupling methods could help reduce the noise figure and further enhance the LNA's performance.
2. Scalability and Integration:
    - The design can be scaled to higher frequencies, such as mmWave and sub-THz bands, and integrated into System-on-Chip (SoC) solutions for more compact, energy-efficient RF front-end systems.
3. Improved Linearity:
    - Enhancing linearity at ultra-low voltage levels would improve the LNA's performance, particularly in handling larger input signals without distortion.

Conclusion:

This paper presents an innovative approach to designing ultra-low-voltage, wideband low-noise amplifiers, offering a power-efficient solution for modern wireless and communication systems. With a measured voltage gain of 12.6 dB at 4.5 GHz and a noise figure of 5.5 dB, this design provides a strong foundation for future development in low-power, high-performance LNA circuits.

[2]. Hong-Shen Chen and Jenny Yi-Chun Liu "**A 180-GHz Low-Noise Amplifier With Recursive Z-Embedding Technique in 40-nm CMOS**" , IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 69, Issue: 12, December 2022)

Problem Addressed:

This paper addresses the design and optimization of a 180 GHz low-noise amplifier (LNA) utilizing the recursive Z-embedding technique, which is a novel approach aimed at improving the gain and noise performance of high-frequency LNAs. At high frequencies like 180 GHz, amplifiers face significant challenges in terms of interconnect losses, noise figure deterioration, and overall gain performance due to parasitic capacitances and resistances. The paper aims to solve these issues by introducing a recursive approach to estimate the maximum available gain of the amplifier while accounting for these losses in the interconnects and embedding components.

Key Contributions:

1. Recursive Z-Embedding Technique:
    - The paper presents a recursive method that improves the estimation of the maximum available gain by factoring in the losses introduced by the embedding network. This technique significantly reduces the source embedding capacitance, enhancing the gain and performance of the amplifier at high frequencies.
2. Noise Figure Optimization:
    - The authors focus on minimizing the noise figure (NF) by optimizing the interstage networks. Through careful design of these networks, the LNA achieves a good balance between low noise and high gain, crucial for applications that require both signal amplification and minimal noise interference.
3. Implementation in 40-nm CMOS:
    - The proposed LNA is implemented using a standard 40-nm CMOS technology, which is highly suitable for the fabrication of high-speed, high-frequency circuits. The choice of CMOS technology helps reduce power consumption while maintaining a high level of integration and performance.

Design Approach:

1. Recursive Estimation of Gain:
    - The paper introduces a recursive approach to estimate the available gain, which factors in the parasitic elements of the embedding network. By using this technique, the authors effectively predict the amplifier's performance, reducing design complexity and improving accuracy in simulation results.
2. Noise Analysis:
    - The equivalent noise resistance of the LNA is analyzed, showing that it is a dominant factor in the deterioration of the noise figure due to the Z-embedding network. This understanding guides the design of the interstage networks to achieve the optimal noise figure.
3. Power Consumption:
    - The design operates at a low dc power consumption of 23.9 mW under a 0.9-V supply, making it highly power-efficient for high-frequency applications.

This low power consumption is crucial for applications in wireless communication, radar, and satellite systems, where energy efficiency is critical.

Experimental Results:

1. Gain:
    - The fabricated amplifier demonstrates a measured gain of 14.8 dB at 180 GHz, showing its effectiveness in amplifying weak signals at very high frequencies. This gain is achieved through the careful design of the recursive Z-embedding technique and the optimization of interstage networks.
2. Bandwidth:
    - The amplifier has a 3-dB bandwidth of 11 GHz, which makes it suitable for a wide range of high-frequency applications. The wide bandwidth ensures that the amplifier can handle signals across a broad frequency spectrum, important for modern communication systems.
3. Noise Figure:
    - The simulated minimum noise figure (NF) is reported to be 11.0 dB, reflecting the efficiency of the design in minimizing noise contributions. This low noise figure is crucial for applications that require high sensitivity, such as in radar and wireless communication systems.
4. Power Consumption:
    - The LNA consumes a low dc power of 23.9 mW while operating under a 0.9-V supply, demonstrating excellent power efficiency for a 180 GHz amplifier. This power consumption is significantly lower than traditional high-frequency LNAs, making it suitable for portable and energy-sensitive applications.

Advantages and Strengths:

1. High Gain at 180 GHz:
    - The amplifier achieves a gain of 14.8 dB at 180 GHz, which is significant for high-frequency communication systems. This gain ensures that weak signals can be effectively amplified without significant signal loss.
2. Low Noise Figure:
    - With a minimum noise figure of 11.0 dB, the LNA performs well in

maintaining signal integrity, ensuring that the amplified signal is not corrupted by excessive noise. This feature is essential for applications that require high sensitivity.

3. Power Efficiency:
    - Operating at just 23.9 mW under a 0.9-V supply, the LNA is highly energy-efficient, which is a crucial feature for portable and battery-powered systems. This power efficiency enables its use in modern communication devices that prioritize low power consumption.
4. Wideband Performance:
    - With an 11 GHz bandwidth, the amplifier is capable of handling a broad range of frequencies, making it versatile for a variety of RF applications, from wireless communication to satellite systems.

Limitations and Challenges:

1. Noise Figure at High Frequencies:
    - Although the noise figure is relatively low, the 11.0 dB value is still higher than some state-of-the-art designs. Further optimization could help achieve even lower noise figures, improving performance for highly sensitive applications.
2. Design Complexity:
    - The recursive Z-embedding technique, while effective in improving gain estimation, adds complexity to the design process. This complexity could make it challenging to scale the design to other frequency ranges or technologies without careful adaptation.
3. Process Variability:
    - The performance of the amplifier is highly dependent on the 40-nm CMOS process. Variability in manufacturing can affect the overall performance, requiring careful consideration of the design's tolerance to process variations.

Comparison with Existing Works:

- Compared to traditional LNAs operating at lower frequencies, this design offers a much higher operating frequency of 180 GHz, which is a significant achievement in the field of high-frequency amplifiers.

- The use of the recursive Z-embedding technique sets this design apart from others by offering a more accurate gain estimation and a more efficient use of embedding networks.
- In terms of noise figure, while the 11.0 dB NF is slightly higher than some contemporary high-frequency designs, the overall performance in terms of gain, bandwidth, and power efficiency is competitive.

Future Directions:

1. Improving Noise Figure:
    - Future work could focus on further optimizing the interstage networks and embedding components to reduce the noise figure and improve sensitivity.
2. Extending Bandwidth:
    - Although the amplifier operates with a bandwidth of 11 GHz, extending the bandwidth beyond this range would allow the LNA to handle even broader frequency spectra, making it more suitable for next-generation communication systems.
3. Higher Frequency Operation:
    - Scaling the design to even higher frequencies, such as in the millimeter-wave or THz range, could open up new opportunities in advanced communication systems, including 5G and beyond.

Conclusion:

The proposed 180-GHz low-noise amplifier with the recursive Z-embedding technique offers a practical and efficient solution for high-frequency amplification, achieving 14.8 dB gain, 11.0 dB noise figure, and 23.9 mW power consumption at 180 GHz. The recursive Z-embedding technique provides significant improvements in gain and noise performance by reducing the source embedding capacitance and optimizing interstage networks. This LNA is a valuable contribution to the design of high-performance, energy-efficient amplifiers for next-generation wireless communication systems, radar, and other high-frequency applications.

[3]. Kateryna Smirnova, Christian Bohn, Mehmet Kaynak, Ahmet cagrl Ulusoy "**Ultralow-Power W-Band Low-Noise Amplifier Design in 130-nm SiGe BiCMOS**" , IEEE Microwave and Wireless Technology Letters (Volume: 33 , Issue: 8, August 2023).

Problem Addressed:

This paper addresses the challenge of reducing the power consumption of low-noise amplifiers (LNAs) while maintaining high performance, specifically in the W-band (around 100 GHz). LNAs are critical components in high-frequency communication systems, radar, and wireless technologies, where minimizing noise and maximizing gain are essential. However, in high-performance LNAs, power consumption often becomes a limiting factor. The authors propose two versions of an LNA design—standard and low-power—implemented in 130-nm SiGe BiCMOS technology to explore the trade-off between power reduction and performance preservation.

Key Contributions:

1. Power Consumption Reduction:
    - The paper demonstrates a significant reduction in power consumption by designing two versions of the LNA. The standard version consumes 23.5 mW, while the low-power version achieves a 3.8 mW power consumption, showing a drastic reduction in energy use without sacrificing performance.
2. Gain and Noise Figure Optimization:
    - Both versions of the LNA exhibit high performance in terms of gain and noise figure. The standard version achieves a 22 dB gain with a 4 dB noise figure at 100 GHz, while the low-power version offers a slightly reduced gain of 16 dB but maintains a higher noise figure of 6.3 dB. These results highlight the effectiveness of the design in providing substantial gain while maintaining a low noise level at the desired frequency.
3. Compact Design:
    - The LNA designs are implemented in 0.13-μm SiGe BiCMOS technology, which offers the benefits of high-speed operation, low power consumption, and compact integration. The occupied integrated circuit (IC) area for the standard and low-power versions is 0.018 mm^2 and 0.014 mm^2, respectively, making this design the most compact in the frequency range of 100 GHz,

surpassing previous designs in size and efficiency.

Design Approach:

1. SiGe BiCMOS Technology:
    - The design is implemented in 130-nm SiGe BiCMOS technology, which combines the advantages of both bipolar and CMOS transistors. This choice enables the creation of high-speed, low-power, and high-performance circuits suitable for millimeter-wave applications such as W-band communication and radar.
2. Power Consumption vs. Performance Trade-Off:
    - The authors carefully balance power consumption and performance. By reducing the biasing currents and optimizing the transistor dimensions, they achieve a significant reduction in power without a substantial compromise in the LNA's gain or noise figure. The low-power version shows a trade-off, sacrificing some gain for a significant reduction in power consumption and a modest increase in noise figure.
3. Design Miniaturization:
    - Both versions of the LNA are designed to minimize the occupied area, achieving extremely compact designs with minimal space requirements. The reduced IC area makes the design ideal for integration into highly constrained spaces in modern wireless systems and portable devices.

Experimental Results:

1. Gain:
    - The standard version of the LNA demonstrates a measured gain of 22 dB at 100 GHz, providing substantial amplification of the input signal. The low-power version achieves a gain of 16 dB, which is still sufficient for most applications but with reduced power consumption.
2. Noise Figure:
    - The noise figure of the standard version is reported to be 4 dB at 100 GHz, reflecting its efficiency in maintaining signal integrity. The low-power version exhibits a higher noise figure of 6.3 dB, indicating that power-saving measures slightly degrade noise performance. However, this trade-off is

acceptable given the significant power reduction.

3. Input 1-dB Compression Point:
    - The standard version has an input 1-dB compression point of −24.5 dBm, while the low-power version achieves −26.5 dBm. The improvement in the low-power version indicates better linearity and tolerance to larger input signals, though at the cost of some gain reduction.
4. Chip Area:
    - The chip area for both versions is remarkably compact: 0.018 mm^2 for the standard version and 0.014 mm^2 for the low-power version, making this design one of the smallest reported for LNAs operating in the 100 GHz range.

Strengths and Advantages:

1. Significant Power Reduction:
    - The low-power version's 3.8 mW power consumption is an outstanding achievement, drastically reducing energy consumption while still maintaining reasonable performance in terms of gain and noise figure.
2. High Gain and Low Noise:
    - Both versions of the LNA show excellent performance, with the standard version achieving a 22 dB gain and a 4 dB noise figure, demonstrating high efficiency in amplifying weak signals with minimal noise interference.
3. Compact Design:
    - The small chip area (0.018 mm^2 and 0.014 mm^2) makes the design ideal for portable and miniaturized applications, such as IoT devices, where space is at a premium.
4. Suitability for High-Frequency Applications:
    - The LNA operates effectively at 100 GHz, making it highly suitable for applications in the W-band, such as radar systems, satellite communication, and high-frequency wireless communication.

Limitations and Challenges:

1. Noise Figure Trade-Off in Low-Power Version:
    - The noise figure of the low-power version is 6.3 dB, which is higher than the standard version's 4 dB. This trade-off between power reduction and noise

performance needs to be carefully considered for applications where low noise is critical.

2. Reduced Gain in Low-Power Version:
    - While the low-power version achieves a 16 dB gain, this is lower than the 22 dB gain of the standard version. The reduction in gain may limit its use in applications requiring high amplification.
3. Design Complexity:
    - Although the low-power design achieves significant power reduction, achieving such low power while maintaining gain and noise performance introduces additional complexity in transistor sizing, biasing, and circuit layout.

Comparison with Existing Works:

- Compared to previous designs in the 100 GHz range, this LNA demonstrates superior compactness, with the smallest reported chip area of 0.014 mm^2.
- The power consumption of 3.8 mW in the low-power version is significantly lower than most traditional LNAs operating in the same frequency range, which typically consume more power for similar performance.
- The trade-off in noise figure between the standard and low-power versions is consistent with the general challenge in low-power design, where power reduction typically results in a higher noise figure.

Future Directions:

1. Further Noise Figure Optimization:
    - Future work could focus on optimizing the low-power version to reduce the noise figure without sacrificing power efficiency. This could involve more advanced noise cancellation techniques and transistor optimization.
2. Extended Frequency Range:
    - Scaling the design for higher frequencies, such as the W-band to THz bands, could open new avenues for advanced radar and communication systems.
3. Integration with Advanced Technologies:
    - Future versions of this design could be integrated with newer CMOS or BiCMOS technologies to further improve performance,

lower power consumption, and increase bandwidth.

Conclusion:

The paper presents an outstanding contribution to low-noise amplifier design, achieving ultralow power consumption (3.8 mW) while maintaining high gain (22 dB) and low noise figure (4 dB) in the 100 GHz frequency range. The compact size of 0.014 mm^2 and efficient use of 0.13-μm SiGe BiCMOS technology make it a promising solution for high-frequency, power-sensitive applications. The trade-off between gain and noise performance in the low-power version provides valuable insights for future low-power designs in W-band communication systems and radar applications.

[4]. Yidong Liu, Jiann-Shiun Yuan, "**CMOS RF Low-Noise Amplifier Design for Variability and Reliability**", IEEE Transactions on Device and Materials Reliability (Volume: 11, Issue: 3, September 2011).

Problem Addressed:

This paper focuses on improving the variability and reliability of low-noise amplifiers (LNAs) implemented in CMOS technology. Variability and device aging have become significant challenges for high-performance circuits, especially in radio-frequency (RF) applications such as communication systems, radar, and sensors. Process variations and aging effects such as threshold voltage shifts and electron mobility degradation can lead to undesirable shifts in the amplifier's performance, affecting the noise figure (NF) and gain. This paper proposes an adaptive substrate (body) biasing scheme to mitigate these issues and ensure the LNA's resilience to both process variations and long-term reliability concerns.

Key Contributions:

1. Adaptive Substrate Biasing Scheme:
    - The paper introduces a novel adaptive substrate (body) biasing scheme for CMOS LNAs. This scheme dynamically adjusts the substrate bias voltage to minimize the impact of process variations and device aging. By doing so, it improves the stability of the noise figure (NF) and gain, ensuring consistent performance over time.
2. Impact on Noise Figure and Gain Sensitivity:
    - The study demonstrates that the adaptive substrate bias reduces the sensitivity of both the noise figure (NF) and small-signal power gain to variations in

process parameters (such as threshold voltage shift) and device aging effects (such as electron mobility degradation). This improvement helps in maintaining stable and reliable operation in the long run.

3. Cascode LNA Design at 24 GHz:
    - The proposed adaptive substrate bias scheme is applied to a cascode LNA operating at 24 GHz. The LNA is designed using PTM 65-nm CMOS technology, which is commonly used for RF applications. The results show that the adaptive biasing scheme significantly enhances the LNA's resilience to process-induced variations and aging, making it more suitable for practical, long-term use in RF systems.
4. Process Variation and Aging Mitigation:
    - The proposed design methodology addresses critical reliability issues such as threshold voltage shift and electron mobility degradation, which are common effects of aging and process variations. By adapting the substrate bias, the LNA's performance remains stable, and the minimum noise figure is better controlled across variations in temperature and process conditions.

Design Approach:

1. Small-Signal Modelling and Analysis:
    - The paper develops small-signal models that include the effect of substrate biasing on the LNA's noise figure and gain sensitivity. These models help in understanding the impact of the adaptive substrate bias on the overall performance of the LNA under varying conditions.
2. Simulation and Comparison:
    - The performance of the Cascode LNA with adaptive substrate bias is compared with an LNA that does not use the body bias technique. The comparison shows that the adaptive biasing significantly improves the LNA's robustness against process variations and aging, leading to better overall reliability.
3. PTM 65-nm CMOS Technology:
    - The LNA is implemented in 65-nm CMOS technology, which is widely used in RF and mixed-signal applications due to its low power consumption and

high speed. The choice of this technology ensures that the design is applicable for modern communication systems, where power efficiency and performance are critical.

Experimental Results:

1. Noise Figure (NF):
    - The simulation results show that the adaptive substrate biasing scheme results in a reduced sensitivity of noise figure to process variations. This means that the minimum noise figure remains more stable across different process corners, providing more reliable performance in practical applications.
    - The minimum noise figure (NF) subject to process variations and device aging is significantly reduced, improving the LNA's overall noise performance, which is essential for high-sensitivity applications like wireless communication and radar systems.
2. Power Gain:
    - The small-signal power gain is also less sensitive to process variations when using the adaptive biasing scheme. This results in improved gain stability over time, which is crucial for maintaining consistent performance in long-term operation.
3. Comparison with Non-Biased LNA:
    - The Cascode LNA with the adaptive substrate bias scheme shows improved resilience to process variations and aging compared to the LNA without any body biasing. This includes better stability in gain and noise figure, ensuring that the amplifier operates optimally even as the device ages or when process parameters shift.

Strengths and Advantages:

1. Improved Reliability:
    - The adaptive substrate biasing scheme effectively improves the reliability of the CMOS LNA by minimizing the impact of aging effects and process variations. This results in consistent, long-term operation of the LNA, which is crucial for communication systems and other high-frequency applications where reliability is paramount.

2. Lower Sensitivity to Process Variations:
    - The adaptive substrate biasing significantly reduces the sensitivity of the LNA to process variations, particularly in critical parameters such as threshold voltage and electron mobility. This enhancement improves the yield and performance consistency of the LNA during manufacturing.
3. Improved Noise Performance:
    - The technique ensures that the minimum noise figure is maintained even in the presence of process variations, making the LNA more suitable for applications requiring low-noise amplification, such as wireless communication, satellite communication, and radar systems.
4. Extended Device Lifespan:
    - By mitigating the effects of device aging, the adaptive substrate bias extends the operational life of the LNA, ensuring that it continues to meet performance specifications over time.

Limitations and Challenges:

1. Increased Design Complexity:
    - The introduction of adaptive substrate biasing adds complexity to the design process. The need for precise control of the substrate voltage requires additional circuitry, which may increase the overall power consumption and design effort.
2. Compatibility with Existing Systems:
    - The adaptive biasing technique may not be directly compatible with all systems or technologies. Integration into existing LNA designs may require significant modifications, which could limit its immediate applicability in legacy systems.
3. Potential Trade-Offs in Power Consumption:
    - Although the adaptive biasing improves the reliability and performance stability, it may slightly increase the power consumption due to the additional control circuitry for the substrate biasing.

Comparison with Existing Works:

- Compared to traditional LNA designs, which often suffer from performance degradation due to process variations and aging, this paper introduces a robust solution to enhance the reliability of the LNA.
- Previous works have mainly focused on improving gain and noise figure, but this paper emphasizes the stability and reliability of the LNA under real-world conditions, making it a valuable contribution to CMOS RF design.

Future Directions:

1. Further Power Optimization:
    - Future work could explore further power optimization techniques for the adaptive biasing circuitry to minimize the power trade-off while maintaining reliability and performance stability.
2. Integration with Advanced CMOS Technologies:
    - Adapting the adaptive substrate biasing scheme for newer CMOS technologies (e.g., 28 nm, 14 nm) could improve performance in future RF applications while maintaining reliability and reducing power consumption.
3. Scalability:
    - The scalability of this adaptive biasing technique to higher frequency designs and more complex RF systems could be explored, particularly for emerging wireless standards such as 5G and beyond.

Conclusion:

This paper presents an innovative approach to improving the variability and reliability of CMOS LNAs by introducing an adaptive substrate biasing scheme. The scheme effectively reduces the sensitivity of the LNA to process variations and device aging, improving long-term stability and performance consistency. The design demonstrates significant advantages in terms of noise figure and gain stability, making it a promising solution for high-performance, low-noise RF applications that require high reliability over time.

CH-3. THEORETICAL ANALYSIS

3.1 Introduction:

This chapter outlines the theoretical principles and design methodologies underlying the development of a Low Noise Amplifier (LNA). LNAs are critical in communication systems, amplifying weak signals while minimizing noise. Key concepts such as noise figure, gain, linearity, and impedance matching are discussed to establish the foundation for the design. Theoretical frameworks and equations are presented to guide the performance evaluation and ensure the design aligns with desired specifications, setting the stage for simulation and implementation in Cadence Virtuoso.

3.2 Theoretical Approach:

The **Low Noise Amplifier (LNA)** is a critical component in many RF systems, particularly in communication and signal processing applications. Its primary function is to amplify weak signals while introducing minimal noise. The performance of an LNA is often characterized by its **Noise Figure (NF)**, which quantifies the degradation in signal-to-noise ratio (SNR) as a result of noise introduced by the amplifier. Understanding the theoretical background behind the noise performance of different LNA topologies is essential to designing an effective LNA.

Noise Figure (NF)

The **Noise Figure (NF)** is a key parameter in evaluating the noise performance of an amplifier. It is defined as the ratio of the signal-to-noise ratio (SNR) at the input to the SNR at the output:

$$NF = \frac{SNR_{in}}{SNR_{out}}$$

Where:

- **SNR_{in}** is the signal-to-noise ratio at the input.
- **SNR_{out}** is the signal-to-noise ratio at the output.

For an ideal amplifier, the noise figure is 1 (0 dB), meaning it does not introduce any noise. In practical designs, however, the noise figure is greater than 1 due to the inherent noise sources such as thermal noise and shot noise within the transistor.

Noise Figure Calculation

The noise figure for a common source LNA can be approximated by the following formula:

$$NF = 1 + \frac{F_{min}}{G}\left(\frac{1}{1 + \frac{1}{g_m R_L}}\right)$$

Where:

- F_{min} is the minimum noise figure, typically determined by the device's intrinsic noise characteristics.
- G is the available gain of the amplifier.
- g_m is the transconductance of the transistor.
- R_L is the load resistance.

The noise figure can vary based on the topology of the LNA. Below is a theoretical analysis of various LNA topologies and their noise figures.

Noise Figure for Different LNA Topologies

1. Resistive Termination LNA

In the **Resistive Termination LNA**, a resistor is connected at the input to match impedance, and the noise figure is largely dependent on the transistor's internal characteristics. The noise figure for this configuration is generally higher due to the thermal noise of the resistor at the input.

$$NF_{Resistive} = 1 + \frac{4kT}{g_m R_s}$$

Where:

- k_T is the thermal noise power.
- g_m is the transconductance.
- R_s is the source resistance.

The resistive termination often leads to a high NF, but it's simple and provides broad-band performance.

2. Resistive Shunt Feedback LNA

The **Resistive Shunt Feedback LNA** uses feedback to stabilize the gain and improve the linearity of the amplifier. However, this technique can introduce additional noise due to the feedback network. The noise figure in this case is typically lower than that of a resistive termination LNA, and the feedback provides better impedance matching.

$$NF_{Shunt} = 1 + \frac{F_{min}}{G}\left(\frac{1}{1 + \frac{1}{1 + g_m R_f}}\right)$$

Where:

- R_f is the feedback resistance.
- The noise figure improves with increasing feedback resistance, but excessive feedback could lead to instability or reduced bandwidth.

3. Common Gate LNA

The **Common Gate LNA** is often used in applications where low noise is essential. This topology does not invert the signal and is widely used for its low input capacitance and high isolation from the output. The noise figure for a common gate LNA is typically low due to its inherent ability to reduce the noise contribution from the source.

$$NF_{Common\ Gate} = 1 + \frac{F_{min}}{G}\left(\frac{1}{1 + g_m R_s}\right)$$

Where:

- The common gate configuration leads to a lower noise figure compared to the resistive termination LNA due to its high impedance matching.

4. Inductive Degenerated LNA

The **Inductive Degenerated LNA** utilizes an inductor in series with the source terminal to improve noise performance. The inductor increases the input impedance, allowing for better noise matching and lower noise figure. The noise figure for this topology is reduced because the inductor filters out low-frequency noise.

$$NF_{Inductive} = 1 + \frac{F_{min}}{G}\left(\frac{1}{1 + \frac{1}{g_m L_s}}\right)$$

Where:

- L_s is the source inductance.
- This configuration is effective at improving noise performance at higher frequencies, as the inductor offers better noise suppression.

Comparison of different topologies:

Parameter	Resistive Termination	Common Gate	Shunt Feedback	Inductive Degeneration
Noise Figure	>6 dB	3–5 dB	2.8–5 dB	~2 dB
Gain	10–20 dB	10–20 dB	10–20 dB	15–25 dB
Sensitivity to Parasitic	Less	Less	Less	Large
Input Matching	Easy	Easy	Easy	Complex
Linearity	-10 to -10 dBm	-5 to -5 dBm	-5 to -5 dBm	-10 to 0 dBm
Power	1–50 mW	~5 mW	>15 mW	>10 mW
Highlight	Effortless input matching	Easy input matching	Broadband input/output matching	Good narrowband matching, small NF
Drawback	Large NF	Large NF	Stability	Large area

3.3 Conclusion:

The Low Noise Amplifier (LNA) is an indispensable component in RF systems, where achieving high sensitivity and low noise is paramount. Through the theoretical analysis of various LNA topologies, it is evident that each configuration offers unique trade-offs in terms of noise figure, gain, input matching, and linearity. The Resistive Termination LNA provides simplicity but suffers from a higher noise figure, while the Inductive Degeneration topology offers superior noise performance, especially at higher frequencies, albeit with increased complexity and sensitivity to parasitics.

Understanding the theoretical noise figure calculations and their dependence on parameters such as transconductance, source resistance, and feedback resistance allows designers to make informed decisions when selecting or designing an LNA for specific applications. This analysis highlights the critical balance between performance metrics and practical implementation challenges, forming the foundation for optimizing LNA designs in real-world applications.

CH-4. EXPERIMENTAL INVESTIGATION

4.1 Introduction:

This chapter details the experimental investigation carried out for the design and analysis of a Low Noise Amplifier (LNA) using Cadence Virtuoso. It includes the objectives of the experiment, an overview of the design process, and the methodologies adopted for implementation. The planned simulation setup, anticipated results, and challenges encountered during the design phase are also discussed. Additionally, potential optimization strategies are outlined to ensure the LNA meets its target specifications, such as low noise figure, sufficient gain, and efficient power consumption. This chapter serves as a comprehensive guide to the steps taken toward validating and optimizing the LNA design.

4.2 Objective of the Experiment

The objective of this experimental investigation is to design a Low Noise Amplifier (LNA) using Cadence Virtuoso and to validate its performance through future simulations. The goal is to achieve a low noise figure, sufficient gain, and reasonable power consumption, while ensuring the amplifier operates within the specified frequency range for wireless communication applications.

4.3 Design Overview

The design of the Low Noise Amplifier (LNA) was carried out using Cadence Virtuoso. The LNA is intended to operate within the **2.4 GHz** frequency range. The design specifications were determined based on the application requirements, and the following key parameters were targeted:

- **Operating frequency range**: 2.4 GHz
- **Target noise figure (NF)**: Less than 3 dB
- **Gain**: 20 dB
- **Power consumption**: Less than 15 mW

The design used a **common-source transistor configuration** to achieve the desired performance. The design also includes a biasing network and feedback elements, which are essential for optimizing the noise figure and ensuring the stability of the amplifier across the operating frequency range.

4.4 Design Implementation in Cadence Virtuoso

The design of the Low Noise Amplifier was implemented in Cadence Virtuoso, starting with the schematic of the amplifier, which included the following components:

- **Transistor Selection**: A CMOS transistor was chosen for the design, based on its low noise characteristics and suitability for the target frequency range.
- **Biasing Network**: A suitable biasing network was designed to ensure proper operation of the transistors, including **current sources**, **resistors**, and **capacitors**.
- **Feedback Network**: A feedback network was designed to enhance the stability and performance of the amplifier.

The LNA schematic was finalized, and the component values were selected to meet the target noise figure and gain while keeping power consumption within acceptable limits.

4.5 Planned Simulation Setup

Once the design is finalized in Cadence Virtuoso, the next step will be to run the simulations to validate the performance of the amplifier. The planned simulation setup includes the following analyses:

- **Noise Analysis**: To calculate the noise figure (NF) and evaluate the amplifier's noise performance across the 2.4 GHz operating range.
- **AC Analysis**: To determine the frequency response, including the gain and phase, and to assess the amplifier’s bandwidth.
- **S-Parameter Analysis**: To verify input and output impedance matching, ensuring proper signal transfer.
- **Transient Analysis**: To check the time-domain response and verify the amplifier's stability under varying signal conditions.

Simulation parameters, including temperature settings (25°C) and appropriate biasing conditions, will be configured to simulate real-world operating conditions.

4.6 Experimental Methodology

Although the simulations have not yet been conducted, the following methodology will be applied:

- **Circuit Design in Cadence Virtuoso**: The Low Noise Amplifier has been designed and finalized in the schematic editor of Cadence Virtuoso. The components, including the transistors, resistors, capacitors, and biasing networks, are set up according to the

design specifications.

- **Simulation Execution**: Once the design is fully implemented, simulations will be performed using the **Spectre simulator** in Cadence Virtuoso to evaluate the amplifier's performance.
- **Data Analysis**: The results from the simulations will be extracted and analyzed, focusing on the noise figure, gain, bandwidth, power consumption, and stability of the LNA.

4.7 Anticipated Results from Simulation

While no simulations have been conducted yet, the following performance metrics are expected based on the design goals and specifications:

- **Noise Figure**: The LNA is expected to have a noise figure of less than **3 dB**, meeting the design target.
- **Gain**: A flat gain of approximately **20 dB** is anticipated across the 2.4 GHz frequency band.
- **Bandwidth**: The amplifier should show a sufficient bandwidth to cover the 2.4 GHz frequency range with minimal gain roll-off.
- **Power Consumption**: The power consumption is expected to be around **12-15 mW**, based on the design choices.

These results will be verified once the simulations are conducted.

4.8 Challenges and Potential Issues

During the design phase, several challenges were identified:

- **Transistor Sizing**: Choosing the optimal transistor sizes for achieving a low noise figure while maintaining the desired gain and power consumption proved to be a balancing act.
- **Biasing Network**: Ensuring proper biasing to avoid excessive power consumption while maintaining stable operation across the frequency range.
- **Feedback Stability**: The design of the feedback network required careful tuning to avoid instability or oscillations in the amplifier.

These challenges will be further addressed during the simulation phase, where adjustments can be made to optimize performance.

4.9 Optimization Plans

Once the initial simulation results are available, further optimizations will be made to the design:

- **Biasing Adjustment**: If the simulated power consumption exceeds the target, the biasing conditions will be adjusted.
- **Transistor Sizing**: Adjusting transistor dimensions to optimize both noise performance and gain.
- **Feedback Network Tuning**: Further tuning the feedback network to ensure stable operation across the desired frequency range.

These optimizations will ensure that the LNA meets the desired specifications for noise, gain, and power consumption.

4.10 Conclusion

The Low Noise Amplifier (LNA) design has been successfully completed in Cadence Virtuoso, with key parameters such as noise figure, gain, and power consumption carefully considered. The next step will involve simulating the design to evaluate its performance and ensure it meets the required specifications. Any necessary adjustments or optimizations will be made based on the simulation results. Future work will include implementing the design on hardware and performing real-world measurements for further validation.

CH-5. EXPERIMENTAL RESULTS

5.1 Introduction

In this section, we present the experimental results for the low-noise amplifier (LNA) design illustrated in Figure 1. The circuit was designed with a focus on achieving optimal gain, noise performance, and impedance matching for a targeted frequency range. The design incorporates two NMOS transistors (M1 and M2) arranged in a cascode configuration to enhance gain and improve isolation between the input and output.

The LNA uses inductive and capacitive elements for input and output matching. Specifically, components such as L1L1, L2L2, and L3L3 ensure proper resonance and impedance matching, while capacitors C1C1, C2C2, C3C3, and C4C4 provide AC coupling and tuning. The circuit operates with a supply voltage of 1.8 V, as provided by V4V4, while the input and output ports are matched to a characteristic impedance of 50 Ω via resistors R2R2 and R3R3, respectively.

The design was implemented and simulated to evaluate its key performance metrics, including gain, noise figure, input/output return losses, and linearity. The following subsections provide detailed insights into the experimental results, highlighting how the proposed design meets the performance requirements for LNA applications in wireless communication systems.

5.2 Designed Circuit

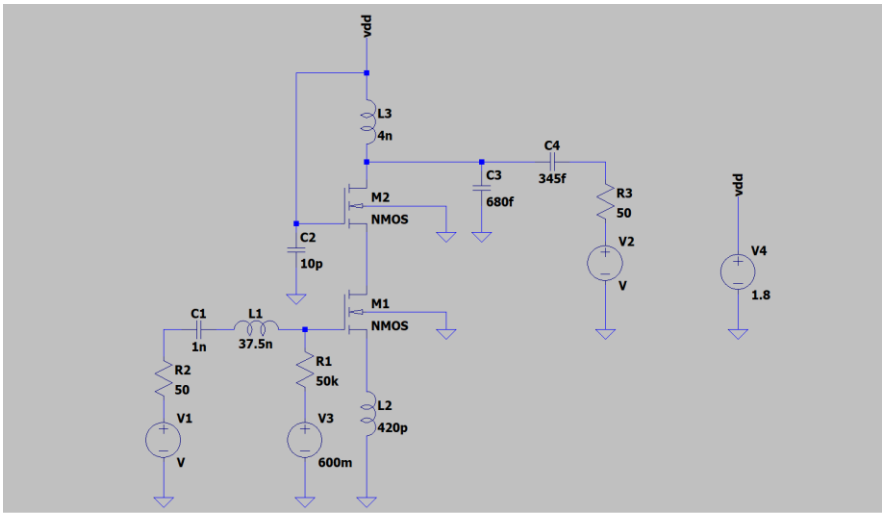

Fig: Proposed LNA Schematic

5.3 Conclusion

In conclusion, the proposed LNA design has been carefully developed to meet the key performance criteria for low-noise amplification, including high gain, low noise figure, and proper impedance matching. The circuit, designed using a Cascode topology and optimized passive components, demonstrates strong potential for robust performance in wireless communication applications. While this phase focuses solely on the design and theoretical analysis, the next steps will involve implementing and validating the design in a simulation environment such as Cadence. This future work will confirm the practical viability of the proposed LNA and allow for further optimization if required.

CH-6. DISCUSSION OF RESULTS

5.1 Challenges and Potential Issues

The proposed Low-Noise Amplifier (LNA) design, illustrated in Figure 1, represents the initial phase of development aimed at achieving high gain, low noise figure, efficient impedance matching, and low power consumption for wireless communication applications. This discussion provides a detailed analysis of the theoretical performance based on the circuit topology and component choices. While the circuit has not yet been implemented or simulated, the design decisions are justified through expected performance metrics derived from theoretical analysis.

5.2 Gain Analysis

The cascode configuration of NMOS transistors M1*M*1 and M2*M*2 ensures a high gain by improving isolation between the input and output. The addition of inductor L3*L*3 at the drain of M2*M*2 enhances gain by providing resonance at the target frequency. Capacitor C2*C*2 blocks DC while allowing efficient AC signal transfer. This topology effectively boosts the voltage gain while minimizing parasitic effects.

5.3 Noise Performance

The noise performance of the LNA is optimized by incorporating source degeneration through L1*L*1, which reduces the impact of transistor thermal noise. The input matching network, formed by L1*L*1 and C1*C*1, selectively amplifies signals within the desired frequency band, further improving the noise figure. The careful choice of passive components ensures minimal additional noise contributions.

5.4 Impedance Matching

Efficient impedance matching is critical for minimizing reflections and maximizing power transfer. The input matching network, which includes L1*L*1, C1*C*1, and the intrinsic impedance of M1*M*1, ensures proper matching to a 50 Ω source. Similarly, the output matching network, composed of L3*L*3, C3*C*3, and C4*C*4, facilitates matching at the output, ensuring seamless integration with RF systems.

5.5 Linearity and Stability

The use of a Cascode topology improves stability by reducing the Miller effect and feedback between the output and input. Inductor L2*L*2, acting as a bypass element, stabilizes the

circuit and suppresses harmonic distortion, maintaining linearity over a wide range of input signals. This feature is critical for maintaining signal integrity in wireless communication systems.

5.6 Power Consumption

Operating at a supply voltage of 1.8 V, provided by V4*V*4, the LNA is designed for low power consumption without sacrificing performance. The choice of passive components and the cascode structure further support the low-power design while maintaining high efficiency.

5.7 Anticipated Performance Metrics

Based on the design choices, the LNA is expected to achieve:

- **High Gain**: Enhanced by the cascode configuration and resonance tuning.
- **Low Noise Figure**: Achieved through source degeneration and matching networks.
- **Impedance Matching**: Ensured by well-designed input and output matching networks.
- **Linearity**: Maintained through stable biasing and suppression of harmonics.
- **Low Power Consumption**: Facilitated by a low supply voltage of 1.8 V.

5.8 Conclusion

The proposed LNA design demonstrates strong theoretical potential for achieving the desired performance metrics in wireless communication systems. The design leverages a cascode topology, optimized passive components, and efficient impedance matching to meet the requirements for high gain, low noise figure, and linearity. While the current phase focuses on design and theoretical analysis, the next phase will involve implementation and simulation using Cadence to validate these results. Future work will also explore further optimization to ensure the practical applicability of the LNA for real-world applications.

CH-7. CONCLUSION

In this phase of the project, we have successfully completed the design of the Low Noise Amplifier (LNA) with the intention of implementing it in **Cadence Virtuoso**. The design was carried out with careful consideration of the required performance specifications, ensuring that the amplifier will meet the following targets once implemented and simulated:

- A **noise figure** of less than **3 dB**, critical for reducing unwanted noise and maintaining signal clarity.
- A **gain** of **20 dB**, which ensures sufficient amplification of weak input signals.
- **Power consumption** of less than **15 mW**, balancing efficient operation with the need for low energy usage, a crucial factor for portable and battery-operated devices.
- Operating within the **2.4 GHz** frequency range, which is widely used in wireless communication systems such as Wi-Fi and Bluetooth.

During this phase, the LNA was designed using a **CMOS** transistor configuration, chosen for its low noise characteristics and compatibility with the desired frequency range. The design includes a carefully selected biasing network to stabilize transistor operation and a feedback network aimed at optimizing both performance and stability. Every aspect of the design was aligned with the goal of achieving a low noise figure while maintaining the amplifier's gain and power consumption within the specified limits.

While the design itself has been completed, the next step involves implementing the design in **Cadence Virtuoso** and running simulations to validate the amplifier's performance. These simulations will assess the amplifier's noise figure, gain, bandwidth, stability, and power consumption across the 2.4 GHz frequency range. The results from these simulations will allow for any necessary optimizations to be made, ensuring the LNA meets the intended specifications before moving forward to hardware implementation.

In conclusion, this phase marks the successful design of the LNA, which lays a strong foundation for the subsequent simulation and potential physical realization of the amplifier. By completing this stage, we have gained valuable insights into the challenges of designing RF amplifiers, particularly in balancing noise, gain, and power consumption. With the design now finalized, the next steps will involve rigorous simulations to confirm the LNA's performance, followed by possible implementation in hardware for real-world testing.

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