**Q4. Mention the applications of diode.**

**Ans:**

The major applications of PN-Junction diode are,

1. Used as rectifiers to convert ac to dc in dc power supplies.
2. Used in clamping networks of voltage multipliers and television receivers.
3. Used in clipping circuits for wave shaping in computers, radars, radio and TV receivers etc.
4. Used in demodulation circuits.
5. Used in voltage multipliers.
6. Used as switch in digital circuits.

**Q5. What is a rectifier and list its types?**

**Ans:** Model Paper-I, Q1(a)

**Rectifier:** Rectifier is a circuit made up of one or more diodes. It converts alternating supply into pulsating D.C.

**Types of Rectifiers:** Different types of rectifiers are available for converting ac supply into pulsating D.C. They are,

1. Half wave rectifier
2. Full wave rectifier
3. Bridge rectifier.

**Q6. Define diode-resistance.**

**Ans:**

The resistance of a diode is the ratio of voltage to current. It is also defined as the reciprocal of slope at a specific bi point or operating point on *V-I* characteristic of diode. It can be expressed as,

$$R_d = \frac{\Delta V_d}{\Delta I_d}$$

Where,

$\Delta V_d$ – Change in diode voltage

$\Delta I_d$ – Change in diode current.

**Q7. What is transition capacitance and Diffusion capacitance?**

**Ans:**

**Transition Capacitance:** In reverse biased PN-junction diode, as the voltage increases the number of immobile charge carri in depletion region increases. This inturn results a capacitive effect across the junction.

Capacitance associated with the depletion region of a diode is known as transition capacitance '*CT*'. The expression f transition capacitance is,

$$C_T = \left|\frac{dQ}{dV}\right|$$

**Diffusion Capacitance:** In forward-biased PN-junction diode, the rate of change in charge with input voltage is known diffusion capacitance, *CD*.

The expression for the diffusion capacitance is,

$$C_D = \frac{dQ}{dV} = \frac{\tau I_F}{\eta V_T}$$

**Q1. What is Bipolar junction transistor and mention its types?**

**Ans:**

Bipolar Junction Transistor (BJT) or transistor is a three terminal solid state semiconductor device. It is basically a semiconductor crystal formed by joining two PN junction back to back. These junctions are arranged such that, one type of semiconductor layer (n-type or p-type) is sandwiched between two layers of the opposite type of semiconductor. The term 'bipolar' in the name indicates the involvement of both majority and minority carries in its operation.

BJTs are classified into two types as,

1. PNP
2. NPN.

**Q2. Why BJT is called as current controlled device?**

**Ans:** Model Paper-I, Q1(c)

A bipolar junction transistor is called current controlled device. Since, the output current is controlled by input current i.e., the current at output terminal depends on current at input terminal.

**Q3. Draw the common base configuration.**

**Ans:**

An NPN transistor arranged in Common Base (CB) configuration is as shown in figure below.

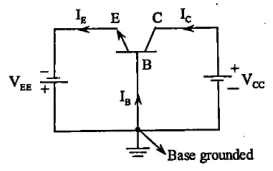



**Figure: CB Configuration**

**Q4. If a transistor has a α of 0.97, find the value of β.**

**Ans:**

Given that,

For a transistor,

Common base current gain, $\alpha = 0.97$

Common emitter current gain, $\beta = ?$

**Q8.**

**Ans**

**Q10. State few applications of Zener diode.**

**Ans:**

Applications of Zener diode are as follows,

1. Voltage regulators
2. Switches in logic circuits
3. Communication circuits
4. Voltage clampers.

**Q11. What is tunneling phenomenon?**

**Ans:**

In tunnel diode, when *P* and *N* regions are doped heavily, the depletion region becomes thin which is approximately abou 10 nm. Then there is a finite probability that electrons acquires the ability to tunnel (or) travel through from *N*-region to *P*-region. This phenomenon is known as tunneling.

**Q12. Mention some advantages and disadvantages of Tunnel Diode.**

**Ans:**

The advantages of tunnel diode are given as follows,

1. It is easy to implement and less expensive.
2. It is low power device.
3. It is a high speed device and is easy to generate.
4. It has less power consumption and is insensitive to nuclear radiations.

The disadvantages of tunnel diode are given as follows,

1. The range of operating voltage is less than 1 V.
2. There is isolation between input and output.
3. Temperature dependent
4. Voltage sensitivity.

**Q13. Mention the applications of photodiode.**

**Ans:**

Model Paper-I, Q1(b)

The applications of photodiode are,

1. Light detectors
2. Optical detector or demodulators
3. Sound track films
4. Electronic control circuits
5. Light operated switches
6. Computer punching cards and tapes
7. Encoders.

**Q14. State the disadvantages of LED.**

**Ans:**

The disadvantages of LED are as follows,

1. The light emitted from LED source is less.
2. It has large light emitting area.
3. It transmits less light energy from LED into fiber.
4. The radiation level in LED is very low.
5. The spectral width of light from LED is wide or broad.



**Q7. What is operating point?**

**Ans:** Model Paper-I, Q1(d)

The zero signal collector current and emitter - collector voltage are known as the operating point. Since the variations in the output occurs across this point, it is called operating point. Another name for this point is "Quiescent point" (or) Q-point. This is because when no signal is applied for amplification, the transistor stays at this point silently. This point is denoted by 'Q' on the DC load line.

**Q8. What is meant by biasing?**

**Ans:** Model Paper-II, Q1(c)

For the transistor to act as an amplifier it must be operated in its active region. The method of applying external voltages to operate the transistor in the active region is known as biasing. For achieving a perfect amplification in amplifier circuit proper biasing is needed.

**Q9. What is meant by stabilization.**

**Ans:** The operating point of a transistor acting as an amplifier shifts mainly with changes in $I_{CO}$, β and $V_{BE}$. The process of making the operating point independent of $I_{CO}$, β and $V_{BE}$ is known as stabilization.

**Q10. Define Stability factors of a transistor.**

**Ans:**

The rate of change of collector current ($I_C$) with respect to collector leakage current ($I_{CO}$) at constant values of $V_{BE}$ and β is called stability factor *S*.

Stability factor, $S = \frac{\partial I_C}{\partial I_{CO}}$

**Q11. List out the three stability factor.**

**Ans:**

The three stability factors of a transistor are defined as follows.

1. $S = \frac{\partial I_C}{\partial I_{CO}}$, '$I_B$' constant
2. $S' = \frac{\partial I_C}{\partial V_{BE}}$, $I_{CO}$, β are constants
3. $S'' = \frac{\partial I_C}{\partial I_B}$, $I_{CO}$, $V_{BE}$ are constants.

**Q12. What is diode compensation?**

**Ans:** Model Paper-III, Q1(d

Diode compensation is a method of stabilizing transistor circuit by replacing transistor with a diode having same temperatur characteristics.

**Q13. How thermal runaway occurs in a transistor?**

**Ans:** The general expression for collector current of a transistor circuit in active region is,

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

As the temperature increases across the collector to base junction, the reverse saturation current $I_{CBO}$ increases. It is double for every 10°C rise in temperature, which causes damage to transistor. This phenomenon is known as thermal runaway.

**Q15. Define clipper circuit and give its applications.**

**Ans:**

**Clipper Circuits**

Circuits used to clip away undesired part of a signal, below or above certain levels are called clipper circuits. They are also called slicers, amplitude selectors, voltage limiters. Though a part of the waveform is clipped, the other part remains undisturbed.

**Uses**

1. Clipping circuit are used to transmit only the required part of the signal and thus eliminates unwanted noise signals.
2. These are also used to convert sine waves into square waves.

**Q16. Classify clipper circuits based on connection of active device.**

**Ans:** Model Paper-III, Q1(b)

Depending upon the connection of active device, the clipper circuit can be classified as,

1. **Series Clipper**

In this, the active device is connected in series with the input signal. These are essentially half-wave rectifier circuits. There are two types of series clippers,

(i) Positive series clipper

(ii) Negative series clipper.

2. **Shunt Clipper**

In this, the active device is connected in shunt or in parallel with the input signal. There are two types of shunt clippers,

(i) Positive shunt clipper

(ii) Negative shunt clipper.

**Q17. What are the applications of voltage comparator?**

**Ans:**

Voltage comparators has a wide range of applications. Some of its main applications are given below.

1. **Pulse-time Modulation**

Voltage comparators are used where time modulation is needed. It produces a succession of pulses whose relative spacing reflects the input information.

2. **Phase meter**

Voltage comparators are used in phase meters to measure angle from 0 to 360°.

3. **Analog-to-Digital Converter**

Voltage comparators plays a major role as analog-to digital converter.

4. **Amplitude-distribution Analyzer**

Voltage comparators can be used as an amplitude distribution analyser, it analyze the amplitude distribution of the noise generated.

**Q18. State two disadvantages of half wave rectifier.**

**Ans:**

The disadvantages of half wave rectifier are given as follows,

1. Only one half of the input waveform reaches the output. Hence, it offers low efficiency.
2. Much more filtering is needed to eliminate harmonics of the A.C frequency from the output and produce a steady D.C voltage.



**Q14. Define the four h-parameters.**

**Ans:**

Hybrid parameters or h-parameters are used to analyse the characteristics of BJT and FET amplifiers.

The h-parameters of an amplifiers are defined as follows.

1. **Input Impedance, $h_{11}$:** It is the ratio of input voltage to input current i.e., $h_{11} = V/I_i$
2. **Output Admittance, $h_{22}$:** It is the ratio of output current to input voltage i.e., $h_{22} = I_o/V_o$
3. **Reverse Voltage Gain, $h_{12}$:** It is the ratio of input voltage to output voltage i.e., $h_{12} = V/V_o$
4. **Forward Current Gain, $h_{21}$:** It is the ratio of output current to input current i.e., $h_{21} = I_o/I_i$

**Q15. Draw the small signal model of BJT device.**

**Ans:**

The small signal model of BJT at low-frequency is illustrated in figure below.

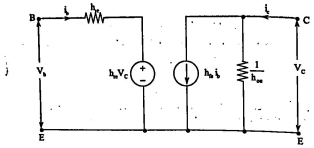



**Figure: Small-Signal Model of BJT**

**Q16. Compare the characteristics of CE, CB and CC amplifiers.**

**Ans:** Model Paper-I, Q1

The comparison between the characteristics of CE, CB and CC amplifiers is mentioned below.

| CE | CB | CC |
|---|---|---|
| 1. Current gain is high | 1. Current gain is less than one | 1. Current gain is large |
| 2. Voltage gain is high | 2. Voltage gain is very large | 2. Voltage gain is approximately one |
| 3. Power gain is also high since $A_v$ and $A_i$ are large. | 3. Power gain is nearly equal to voltage gain current gain | 3. Power gain is approximately equal to |
| 4. The phase shift in output is 180° | 4. No phase shift in output | 4. No phase shift in output |

**Q17. Why h-parameter model is not suitable for the analysis of high frequency response of the amplifier?**

**Ans:**

The h-parameter model is suitable only to analyze low frequency response of amplifiers. This analysis is carried out b neglecting the effect of shunt capacitance in the transistor due to instantaneous response to variations in input current or voltage It is not suitable for the analysis of high frequency response of the amplifier because,

(i) The values of h-parameters become complex at high frequencies.

(ii) At high frequencies the values of h-parameters change and hence it is required to analyze the transistor at each and every range of frequency. In practice, it is not possible to analyze the transistor at each and every range of frequency.

**Q18. What is cascaded amplifier?**

**Ans:** The transistor circuit which involves more than one stage (or) multiple stages of amplification is called a multistage amplifier or cascaded amplifier.

The block schematic of a multistage amplifier is shown in figure below.

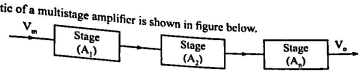



Figure : Multistage Amplifier

The overall gain of a multistage amplifier is the product of gain of individual stages.

i.e., $A = A_1 \times A_2 \times \dots A_n$

$$A = \frac{V_{o1}}{V_{in1}} \times \frac{V_{o2}}{V_{in2}} \times \dots \times \frac{V_{on}}{V_{inn}}$$

**Q19. Write down the need of cascading the amplifiers.**

**Ans:** Model Paper-III, Q1(c)

Amplification capacity of a single stage amplifier is limited and cannot meet the required specifications. A single stage amplifier uses limited transistor parameters because of which it cannot provide very high voltage and current gains and also it does not match its input impedance with the source and output impedance with the load.

In order to overcome these limitations, two or more single stage amplifiers are connected in cascade. The cascade connection of amplifiers (i.e., multistage amplifiers) provides desired amplification.

**Q20. A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB?**

**Ans:**

Given that,

The power gain of each stage in a five-stage amplifier is,

$A_{p_n} = 30, n = 1$ to 5

Total gain, $A_p = ?$

The overall gain, $A_p$ of an $n$-stage amplifier is given as,

$A_p = A_{p1} \times A_{p2} \times A_{p3} \times \dots A_{pn}$

Here, $n = 5$

$A_p = A_{p1} \times A_{p2} \times A_{p3} \times A_{p4} \times A_{p5}$

$= 30 \times 30 \times 30 \times 30 \times 30$

$A_p = 243 \times 10^5$

∴ Total gain, $A_p = 243 \times 10^5$

Gain in $dB$, $A_p = 147.71$ dB

## SHORT QUESTIONS WITH SOLUTIONS

**Q1. State the duality principle with example.**

**Ans:** Model Paper-I, Q1(g)

Duality Principle

It states that any boolean expression can be converted into another equivalent boolean expression by replacing OR operator with AND, AND operator with OR and interchanging 1 with 0 and 0 with 1.

Example

$$Y = \overline{A}B + \overline{A}B\overline{C} + \overline{A}BCD + \overline{A}B\overline{C}\,\overline{D}E$$

The dual of $Y$ is obtained by interchanging AND and OR operations as,

$$Y_D = (\overline{A} + B)(\overline{A} + B + \overline{C})(\overline{A} + B + C + D)(\overline{A} + B + \overline{C} + \overline{D} + E)$$

**Q2. State De Morgan's theorems.**

**Ans:**

For any two variables, '$A$' and '$B$' in boolean algebra, this theorem states that the complement of sum of logic variables is equal to the product of their individual complements.

i.e., $\overline{A+B} = \overline{A}.\overline{B}$

For any two variables '$A$' and '$B$' in boolean algebra this theorem states that the product of logic variables is equal to the sum of their individual complements.

i.e., $\overline{A.B} = \overline{A} + \overline{B}$

**Q3. Write the boolean algebraic laws.**

**Ans:**

The laws of boolean algebra are,

1. **Commutative Law**

This law allows changes in the order of the boolean variables.

Law 1 : Commutative law for AND

$A.B = B.A$

Law 2 : Commutative law for OR

$A + B = B + A$

2. **Associative Law**

This law allows the grouping of boolean variables.



Law 1 : Associative law for AND

$(A.B)C = A(B.C)$

Law 2 : Associative law for OR

$(A + B) + C = A + (B + C)$

3. **Distributive Law**

This law allows factoring out of expressions.

Law 1: Distributive law for AND

$A + BC = (A + B)(A + C)$

Law 2 : Distributive law for OR

$A(B + C) = AB + AC$

**Q4. Simplify the expression Z = AB + $A\overline{B}.\overline{(A\overline{C})}$?**

**Ans:** Model Paper-II, Q1(g)

The given expression is,

$Z = AB + A\overline{B}\,\overline{(A\overline{C})}$

$= AB + A\overline{B}\,\overline{(A} + \overline{\overline{C}})$ (∵ Demorgan's theorem)

$= AB + A\overline{B}\ (A + C)$

$= AB + A\overline{B}A + A\overline{B}C$

$= AB + A\overline{B} + A\overline{B}C$ (∵ $AA = A$)

$= AB + A\overline{B}\ (1 + C)$

$= AB + A\overline{B}$ (∵ $1 + C = 1$)

$= A(B + \overline{B})$ (∵ $B + \overline{B} = 1$)

$= A$

**Q5. State the purpose of reducing the switching functions to minimal form.**

**Ans:** Model Paper-III, Q1(g)

The purpose of reducing the switching functions to minimal form includes,

1. Enhanced reliability
2. Reduced complexity of the circuit
3. Less expensive circuitry.

**Q6. Write about sum of products and product of sums of Boolean expressions.**

**Ans:**

**SOP**

In a SOP form, if each product term consists of all the literals (either complemented or uncomplemented), then the SOP is called standard or canonical SOP form. In this form, each individual term is called minterm.

**POS**

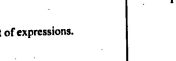
POS stands for "Product of Sum". It is a form used in boolean algebra to represent the logical functions. In this form, a sum term is any group of literals that are ORed (or added) together and the product of SUM is a group of SUM terms that are ANDed (or multiplied) together

**Q7. Draw the symbols of AND, OR and NOT gates.**

**Ans:**

**AND Gate**

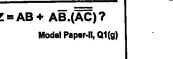
The logic symbol of AND gate is shown in figure (1)




Figure(1)

**OR Gate**

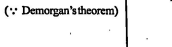
The logic symbol of OR gate is shown in figure (2)




Figure(2)

**NOT Gate**

The logic symbol of NOT gate is shown in figure (3).




Figure(3)

**Q8. What is the importance of universal gates?**

**Ans:**

The logic gates NAND and NOR are known as universal logic gates. In general, any boolean expression can be implemented using AND, OR and NOT gates. While, these basic gates can be implemented using NAND or NOR gate alone. This specifies that NAND or NOT gate alone can be used to implement any boolean expression. Hence, NAND and NOR gates are termed as universal logic gates.

**Q9. List the universal gates and draw their symbols.**

**Ans:**

The two universal logic gates are,

1. NAND gate
2. NOR gate.

1. **NAND Gate**

The logic symbol of NAND gate is shown in figure (1).

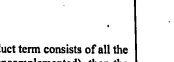



Figure (1)

2. **NOR Gate**

The logic symbol of NOR gate is shown in figure (2).

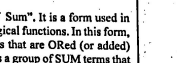



Figure (2)



**Q10. What is a cell of a K-map?**

**Ans:** The cell of a karnaugh map (K-map) is defined as the smallest unit in the map representing a line of a truth table.

**Q11. What do you mean by K-map? Give its advantages and disadvantages.**

**Ans:**

**K-map**

Karnaugh map or K-map is a pictorial representation of a truth table and offers a simple and straight forward method of minimizing boolean expressions. The K-map consists of squares and each square specifies a minterm or maxterm of the expression that is to be simplified. Depending on the number of input variables, the number of squares in the K-map also vary i.e.,

For two-variable K-map, number of squares = $2^2 = 4$

For three-variable K-map, numbers of squares = $2^3 = 8$

For four-variable K-map, numbers of squares = $2^4 = 16$.

**Advantages**

1. K-map is very simple and fast in simplifying lines expressions upto four variables.
2. It do not require boolean laws.
3. It is suitable for minimization of SOP and POS forms of expressions.
4. It is suitable for fast identification of prime implicants and essential prime implicants.
5. It provides visual method for logic simplification.

**Disadvantages**

1. Complexity increases as the number of variables increases.
2. It is not used for computer reduction.

**Q12. What is maxterm?**

**Ans:** Model Paper-III, Q1(h)

The 'Maxterm' is a sum term consisting of all variables in the boolean function either in complemented form (or) uncomplemented form.

The maxterms are generated from an 'OR' term of n-variables, that are primed if binary bit is '1' and unprimed if bit is '0'.

**Q13. What is a prime implicant in K-map?**

**Ans:**

An implicant which is not a subset of another implicant of the function is known as "prime implicant".

**Q14. Obtain the prime implicants for given Boolean expression using K-map.**

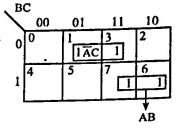
**f(A, B, C) = Σ(1, 3, 6, 7)**

**Ans:**

The given boolean expression is,

$f(A, B, C) = \Sigma(1, 3, 6, 7)$ ... (1)

As the boolean expression is a function of three inputs $A$, $B$, $C$ a 3 variable k-map is used to obtain prime implicants of the given boolean expression.




Figure

∴ The prime implicants are,

$f(A, B, C) = AC + AB$

**Q15. What is gate level minimization?**

**Ans:** Model Paper-II, Q1(h)

The task of minimizing boolean function to determine an optimal gate level implementation of digital circuit is termed as "Gate level minimization".

**Q16. What is combinational circuit? Give examples.**

**Ans:**

The circuit whose output at a given instant of time depends only on the present input at that instant is known as combinational circuit. This circuit comprises of input variables, logic gates and output variables.

The block diagram of an $n \times m$ combinational circuit is as shown in figure.

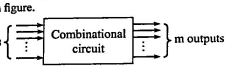



Figure: Combinational Circuit

**Examples**

1. Adders
2. Subtractors
3. Decoders
4. Encoders
5. Comparators
6. Multiplexers.



**Q17. What are the applications of full adder?**

**Ans:**

The major applications of full adders are,

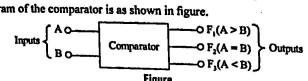
1. Full adders are extensively used in designing Digital Signal Processors (DSPs) and microprocessors.
2. Full adders are the basic building elements in Arithmetic Logic Units (ALUs).
3. It can also be used for designing ripple carry counter to perform $n$-bit addition.

**Q18. Define magnitude comparator.**

**Ans:**

A comparator is a combinational circuit which compares the magnitude of two binary numbers and produces one of the three outputs (i.e., greater than, equal and less than). It is also known as digital comparator or magnitude comparator.

The general block diagram of the comparator is as shown in figure.



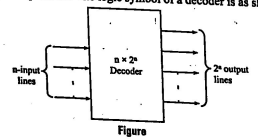

Figure

**Q19. What is a decoder? Give the applications of a decoder.**

**Ans:**

**Decoder**

A decoder is a combinational circuit which has '$n$' number of input lines and $2^n$ number of output lines. It converts an $n$-bit binary input code into a $2^n$ unique output lines. The logic symbol of a decoder is as shown in figure.




Figure

**Applications of Decoder**

1. Decoder is used to convert BCD to 7-segment code.
2. It is used in memories for selection of specific register.
3. It is used to activate single or group of outputs for specific combination of input levels.
4. It is also used for the implementation of combinational circuits.

**Q20. Why do go for priority encoder rather than normal encoder.**

**Ans:** Model Paper-I, Q1(h)

A normal encoder responds only when one of its input is '1' and all others are '0' at any point of time. This is the limitation of a normal encoder. So, when any two input lines become '1' at the same time, the line that has higher priority is considered in a priority encoder. Hence, we go for priority encoder rather than normal encoder.

**Q21. List out the applications of multiplexers.**

**Ans:**

The applications of multiplexers are,

1. Multiplexers are widely used in combinational logic circuit.
2. They are also used in Time Division Multiplexing (TDM) and Frequency Division Multiplexing (FDM).
3. These are used in A/D and D/A converters.
4. These are also employed in data acquisition systems.



| | Asynchronous Sequential Circuits | | Synchronous Sequential Circuits |
|---|---|---|---|
| 1. | In asynchronous sequential circuits, input signals affect memory elements at any instant of time. | 1. | In synchronous sequential circuits input signals can affect memory elements at discrete instances of time. |
| 2. | These circuits are complex to design. | 2. | These circuits are simple to design. |
| 3. | In this circuit, clock is not required. | 3. | Here clock is required as one of the input. |
| 4. | In this circuit, the speed of operation is high. | 4. | In this circuit, the speed of operation is limited by the time delays involved. |
| 5. | Example: Unclocked flipflops | 5. | Example: Clocked flipflops. |

**Q4. Define a latch and a flip-flop.**

**Ans:** Model Paper-II, Q1(i)

**Latch**

A latch is an electronic device, which changes its output immediately based on the applied input. It is used to store either 1 or 0 at any specified time. It consists of two inputs namely 'SET' and RESET and two outputs, which are complement to each other as shown in figure (1).

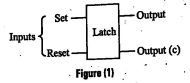



Figure (1)

**Flip-flop**

Flipflop is a basic digital memory circuit, which stores one bit of information. The block schematic representation of flipflop is as shown in figure (2).

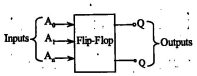



Figure (2)

Where, $Q$ – Normal output

$\overline{Q}$ – Inverted output

$A_0, A_1, A_n$ – Inputs.

**Q5. Write the truth table of D-latch.**

**Ans:**

The truth table of D-latch is shown in table below.

| Input | Output | Operation |
|---|---|---|
| D | $Q_n$ | |
| 0 | $Q_{n-1}$ | No change |
| 1 | $Q_{n-1}$ | |
| 0 | 0 | Data Storage |
| 1 | 1 | |

Table

**Q6. What is edge-triggered flip-flop?**

**Ans:**

The change in output state either at positive edge (raising edge) or negative edge (falling edge) of the clock pulse is known as edge triggering. In this, flip-flop responds only during clock pulse transition at edges. There are two types of edge triggering. They are,

1. Positive edge triggering
2. Negative edge triggering.

**Q7. Define race around condition in flip flop.**

**Ans:**

In JK flip-flop, the condition in which output oscillates more than once between 1 and 0 during a single clock pulse is referred to as "race around condition".

**Q8. What are the applications of flip-flops?**

**Ans:** Model Paper-I, Q1(j)

The applications of flip flops are as follows,

1. To design counters and registers.
2. To reduce key debouncing.
3. To provide delay.
4. To store data i.e., used as memory element.

**Q9. Mention the similarities and differences between latch and flipflop.**

**Ans:**

The Ssimilarities and differences between flipflop and latch are mentioned in table below.

| | Flipflop | | Latch |
|---|---|---|---|
| 1. | Flipflop is a bistable device i.e., it has two stable states that are represented as 0 and 1. | 1. | Latch is also a bistable device whose states are also represented as 0 and 1. |
| 2. | It checks the inputs but changes the output only at times defined by the clock signal or any other control signal. | 2. | It checks the inputs continuously and responds to the changes in inputs immediately. |
| 3. | It is a edge triggered device. | 3. | It is a level triggered device. |
| 4. | They are classified into asynchronous or synchronous flipflops. | 4. | There is no such classification in latches. |
| 5. | Gates like NOR, NOT, AND, NAND are building blocks of flipflops. | 5. | These are also made up of gates. |
| 6. | It forms the building blocks of many sequential circuits like counters. | 6. | These can be used for the designing of sequential circuits but are not generally preferred. |

**Q10. What is the significance of state assignment?**

**Ans:** Model Paper-II, Q1(j)

The performance of a sequential circuit is expressed in terms of four parameters, namely input, present state, the next state and the output. A specific flip-flop inputs are required to generate the next state at a particular present state and input. These flip-flop inputs are obtained from flip-flop input functions. In order to determine the flip-flop input functions, the states in the state diagram must be indicated with binary values rather than alphabets. This process is termed as state assignment. The assignment of binary digits to the states must be in a manner that minimum logic gates are used to implement flip-flop input functions.





**Q11. Define shift register.**

**Ans:**

A register capable of shifting its binary information in one or both directions is called a shift register. Shift register consists of a chain of flip-flops which are cascaded with output of one flip-flop connected to the input of the next flip-flop.

**Q12. Write the differences between synchronous and asynchronous counters.**

**Ans:**

The differences between synchronous and asynchronous counters are mentioned below.

| | Synchronous Counter | | Asynchronous Counter |
|---|---|---|---|
| 1. | In synchronous counter, a single clock pulse is connected to all the flip-flops | 1. | In asynchronous counter, clock pulse connected to first flip-flop and other output of each flip-flop acts as clock input for following flip-flop. |
| 2. | Speed of operation is relatively high. | 2. | Speed of operation is very low. |
| 3. | Propagation delay is less. | 3. | Propagation delay is more. |
| 4. | The overall speed of synchronous counter depends only on the frequency of the clock. | 4. | The overall speed of the asynchronous counter depends upon the frequency of the clock and propagation delay of each flip flop. |
| 5. | Synchronous counters are parallel counters. | 5. | Asynchronous counters are serial or series counters. |
| 6. | These counters are simple to design. | 6. | These counters are difficult to design as the number of flip-flop increases. |

**Q13. What are the advantages and disadvantages of ripple counters?**

**Ans:**

**Advantages**

1. Ripple counter are simple and easy to design.
2. It requires less amount of hardware and thus the cost of circuitry is less expensive.

**Disadvantages**

1. Ripple counters consists of unwanted spikes.
2. These are serial counters and are time consuming.

**Q14. What is the minimum no of flip flop needed to design a counter of modulus 60?**

**Ans:** Model Paper-II, Q1(j)

The number of flip-flops needed for designing a Mod-$N$ counter depends on the number of binary bits required to represent the value of $N$.

The number of flip-flops needed to construct a counter is evaluated using the condition,

$$2^n \geq N$$

Here, $N = 60$

$$2^n \geq 60$$

The minimum value that satisfies the above condition is '6'. Therefore, six flip-flops are required to design a Mod-60 counter.

$\therefore n = 6$