CSCI 6461

Computer Architecture II

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Project 1

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PROF
DR. LEI HE

This project is to help you get familiar with the software SMPCache (http://arco.unex.es/smpcache/). The following tasks provide a powerful tool for understanding the complex design features of a modern computer system.

We will first study the basic algorithms and concepts that are present in every cache memory system, uniprocessor or multiprocessor. We will consequently configure the SMPCache simulator with a single processor, and we will use uniprocessor traces. For this first set of tasks we will consider traces of some SPEC'92 benchmarks (Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp), according to real tests performed on a MIPS R2000 system. The traces used represent a wide variety of "real" application programs. These traces come from the Parallel Architecture Research Laboratory (PARL), New Mexico State University (NMSU), and they are available by anonymous ftp to tracebase.nmsu.edu. The traces had different formats, like Dinero or PDATS, and they have been changed to the SMPCache trace format (see Getting Started with SMPCache 2.0, section 4). These traces, with the correct format for SMPCache, are included in your copy of the simulator. A summary of the traces is given in Table 1.

Name	**Classification**	**Language**	**Comments**
Hydro	Floating point	---	Astrophysics: Hydrodynamic Naiver Stokes equations
Nasa7	Floating point	Fortran	A collection of 7 kernels. For each kernel, the program generates its own input data, performs the kernel and compares the result against an expected result
Cexp	Integer	C	Portion of a Gnu C compiler that exhibits strong random behaviour
Mdljd	Floating point	Fortran	Solves the equations of motion for a model of 500 atoms interacting through the idealized Lennard-Jones potential. It is a numerical program that exhibits mixed looping and random behaviour
Ear	Floating point	---	This trace, the same as the rest, was provided by Nadeem Malik of IBM
Comp	Integer	C	Uses Lempel-Ziv coding for data compression. Compresses an 1 MB file 20 times
Wave	Floating point	Fortran	Solves Maxwell's equations and electromagnetic particle equations of motion.
Swm	Floating point	Fortran	Solves a system of shallow water equations using finite difference approximations on a 256*256 grid
UComp	Integer	C	The uncompress version of *Comp*

Table 1: Uniprocessor traces

Task table:

Tasks	Purpose	Configuration	Experiment	Questions
1. Locality of Different Programs	Show that the programs have different locality, and there are programs with “good” or “bad” locality.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 16. Words by block = 16 (block size = 32 bytes). Blocks in main memory = 8192 (main memory size = 256 KB). Blocks in cache = 128 (cache size = 4 KB). Mapping = Fully-Associative. Replacement policy = LRU.	Obtain the miss rate using the memory traces: Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp (trace files with the same name and extension “.prg”).	Do all the programs have the same locality grade (i.e., local or global)? Which is the program with the best locality? And which does it have the worst? Do you think that the design of memory systems that exploit the locality of certain kind of programs (which will be the most common in a system) can increase the system performance? Why? During the development of the experiments, you can observe graphically how, in general, the miss rate decreases as the execution of the program goes forward. Why? Which is the reason?
2. Influence of the Cache Size	Show the influence of the cache size on the miss rate.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 16. Words by block = 16 (block size = 32 bytes). Blocks in main memory = 8192 (main memory size = 256 KB). Mapping = Fully-Associative. Replacement policy = LRU.	Configure the blocks in cache using the following configurations: 1 (cache size = 0,03 KB), 2, 4, 8, 16, 32, 64, 128, 256, and 512 (cache size = 16 KB). For each of the configurations, obtain the miss rate using the trace files (extension “.prg”): Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.	Does the miss rate increase or decrease as the cache size increases? Why? Does this increment or decrement happen for all the benchmarks or does it depend on the different locality grades? What does it happen with the capacity and conflict (collision) misses when you enlarge the cache? Are there conflict misses in these experiments? Why? In these experiments, it may be observed that for great cache sizes, the miss rate is stabilized. Why? We can also see great differences of miss rate for a concrete increment of cache size. What do these great differences indicate? Do these great differences of miss rate appear at the same point for all the programs? Why? In conclusion, does the increase of cache size improve the system performance?
3. Influence of the Block Size	Study the influence of the block size on the miss rate.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 16. Main memory size = 256 KB (the number of blocks in main memory will vary). Cache size = 4 KB (the number of blocks in cache will vary). Mapping = Fully-Associative.	Configure the words by block using the following configurations: 4 (block size = 8 bytes), 8, 16, 32, 64, 128, 256, 512, and 1024 (block size = 2048 bytes). For each of the configurations, obtain the miss rate using the trace files: Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.	Does the miss rate increase or decrease as the block size increases? Why? Does this increment or decrement happen for all the benchmarks or does it depend on the different locality grades? What does it happen with the compulsory misses when you enlarge the block size? What is the pollution point? Does it appear in these experiments? In conclusion, does the increase of block size improve the system performance?

		Replacement policy = LRU.		
4. Influence of the Block Size for Different Cache Sizes	Show the influence of the block size on the miss rate, but in this case, for several cache sizes.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 32. Main memory size = 1024 KB (the number of blocks in main memory will vary). Mapping = Fully-Associative. Replacement policy = LRU.	Configure the words by block using the following configurations: 8 (block size = 32 bytes), 16, 32, 64, 128, 256, 512, and 1024 (block size = 4096 bytes). For each of the configurations of words by block, configure the number of blocks in cache in order to get the following cache sizes: 4 KB, 8 KB, 16 KB, and 32 KB. For each configuration obtain the miss rate using the memory trace: Ear.	We are first going to ask you the same questions as in the previous project: Does the miss rate increase or decrease as the block size increases? Why? What does it happen with the compulsory misses when you enlarge the block size? Does the pollution point appear in these experiments? Does the influence of the pollution point increase or decrease as the cache size increases? Why?
5. Influence of the Mapping for Different Cache Sizes	Analyse the influence of the mapping on the miss rate for several cache sizes.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 32. Words by block = 64 (block size = 256 bytes). Blocks in main memory = 4096 (main memory size = 1024 KB). Replacement policy = LRU.	Configure the mapping using the following configurations: Direct, two-way set associative, four-way set associative, eight-way set associative, and fully-associative (remember: Number_of_ways = Number_of_blocks_in_cache / Number_of_cache_sets). For each of the configurations of mapping, configure the number of blocks in cache in order to get the following cache sizes: 4 KB (16 blocks in cache), 8 KB, 16 KB, and 32 KB (128 blocks in cache). For each configuration obtain the miss rate using the memory trace: Ear.	Does the miss rate increase or decrease as the associativity increases? Why? What does it happen with the conflict misses when you enlarge the associativity grade? Does the influence of the associativity grade increase or decrease as the cache size increases? Why? In conclusion, does the increase of associativity improve the system performance? If the answer is yes, in general, which is the step with more benefits: from direct to 2-way, from 2-way to 4-way, from 4-way to 8-way, or from 8-way to fully-associative?
6. Influence of the Replacement Policy	Show the influence of the replacement policy on the miss rate.	Processors in SMP = 1. Cache coherence protocol = MESI. Scheme for bus arbitration = Random. Word wide (bits) = 16. Words by block = 16 (block size = 32 bytes). Blocks in main memory = 8192 (main memory size = 256 KB). Blocks in cache = 128 (cache size = 4 KB). Mapping = 8-way set-associative (cache sets = 16).	Configure the replacement policy using the following configurations: Random, LRU, LFU, and FIFO. For each of the configurations, obtain the miss rate using the trace files (extension ".prg"): Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.	In general, which is the replacement policy with the best miss rate? And which does it have the worst? Do the benefits of LFU and FIFO policies happen for all the benchmarks or do they depend on the different locality grades? For a direct-mapped cache, would you expect the results for the different replacement policies to be different? Why or why not? In conclusion, does the use of a concrete replacement policy improve the system performance? If the answer is yes, in general, which is the step with more benefits: from Random to LRU, from Random to LFU, or from Random to FIFO? Why (consider the cost/performance aspect)?

Task 1

Locality of Different Programs

Purpose

Show that the programs have different locality, and there are programs with “good” or “bad” locality.

Configuration

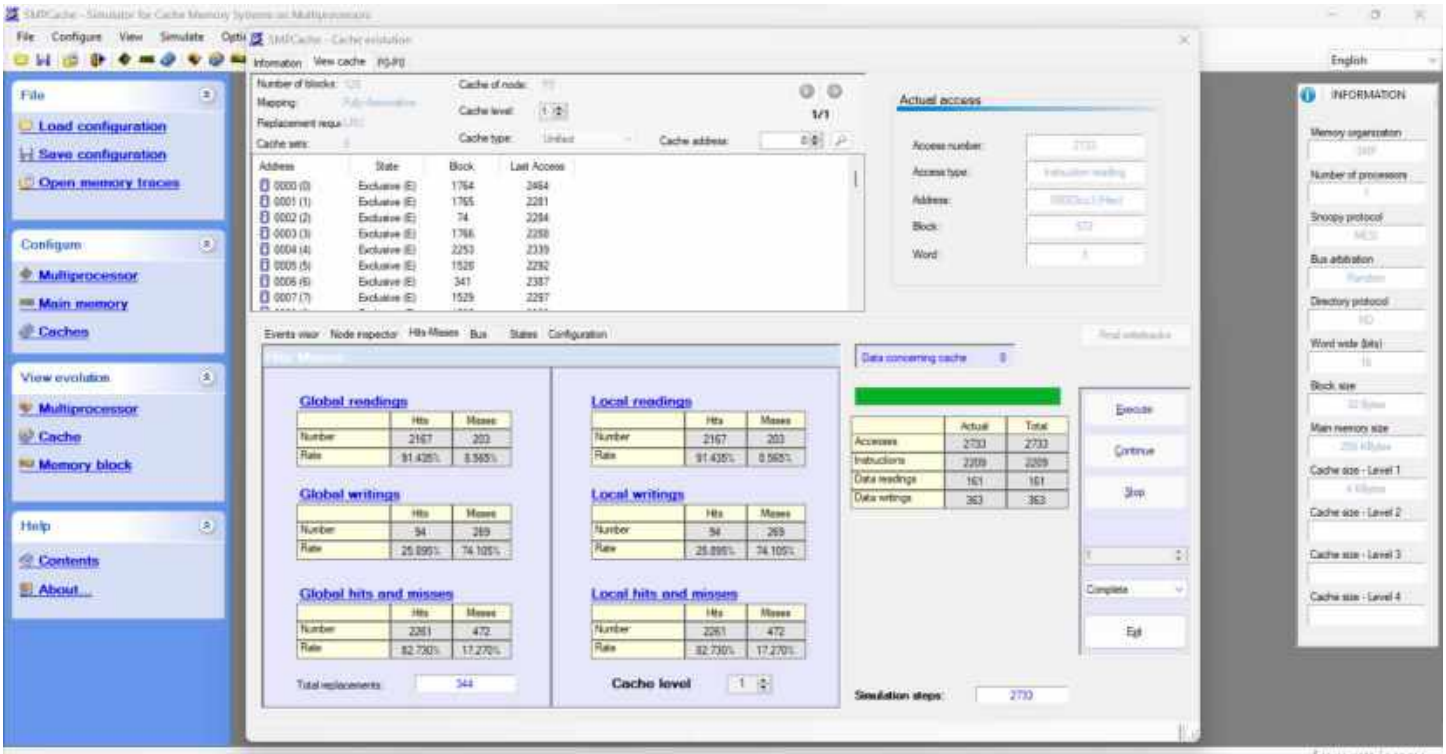
Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 16.
Words by block = 16 (block size = 32 bytes).
Blocks in main memory = 8192 (main memory size = 256 KB).
Blocks in cache = 128 (cache size = 4 KB).
Mapping =
Fully-Associative.
Replacement policy = LRU

Experiment

Do all the programs have the same locality grade (i.e., local or global)? Which is the program with the best locality? And which does it have the worst? Do you think that the design of memory systems that exploit the locality of certain kind of programs (which will be the most common in a system) can increase the system performance? Why?

During the development of the experiments, you can observe graphically how, in general, the miss rate decreases as the execution of the program goes forward. Why? Which is the reason?

Ucomp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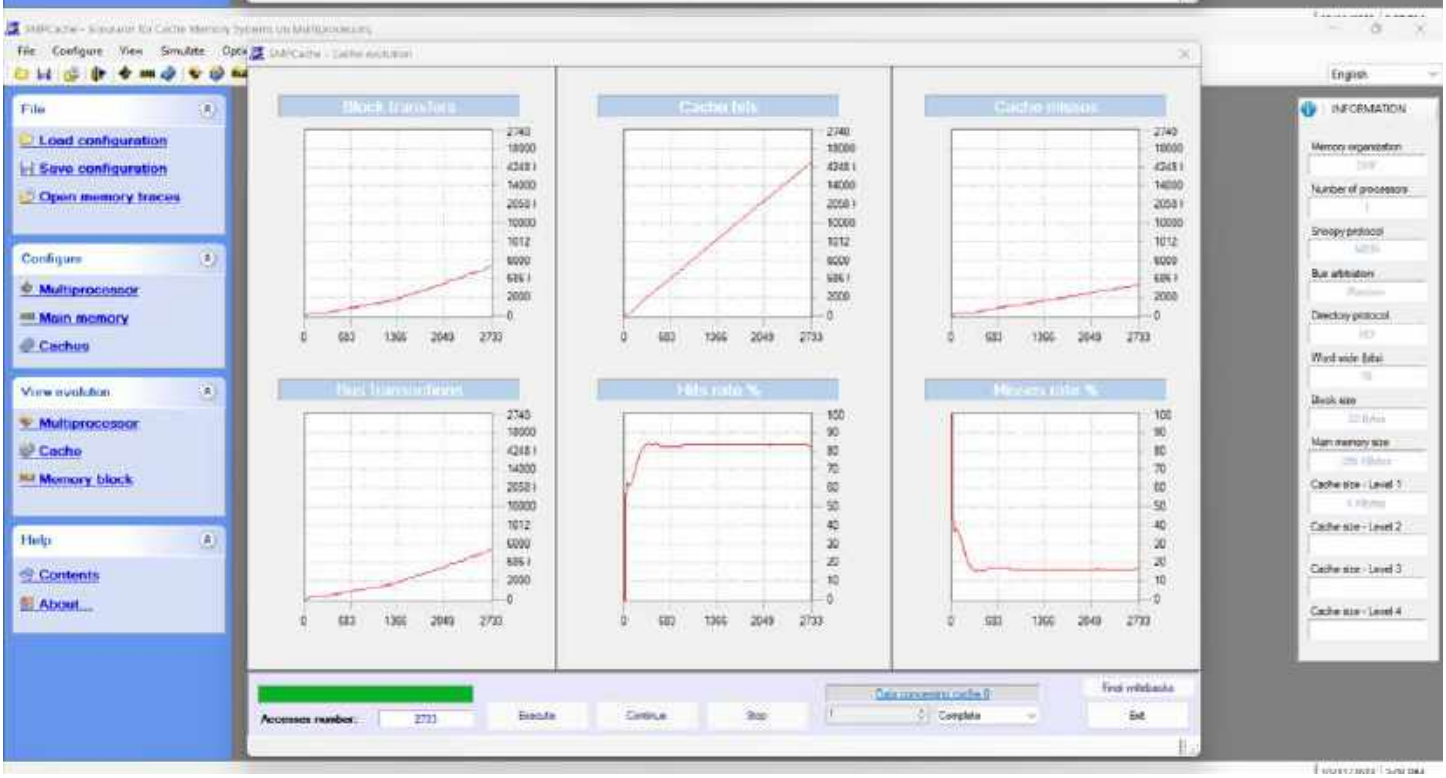
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INFORMATION

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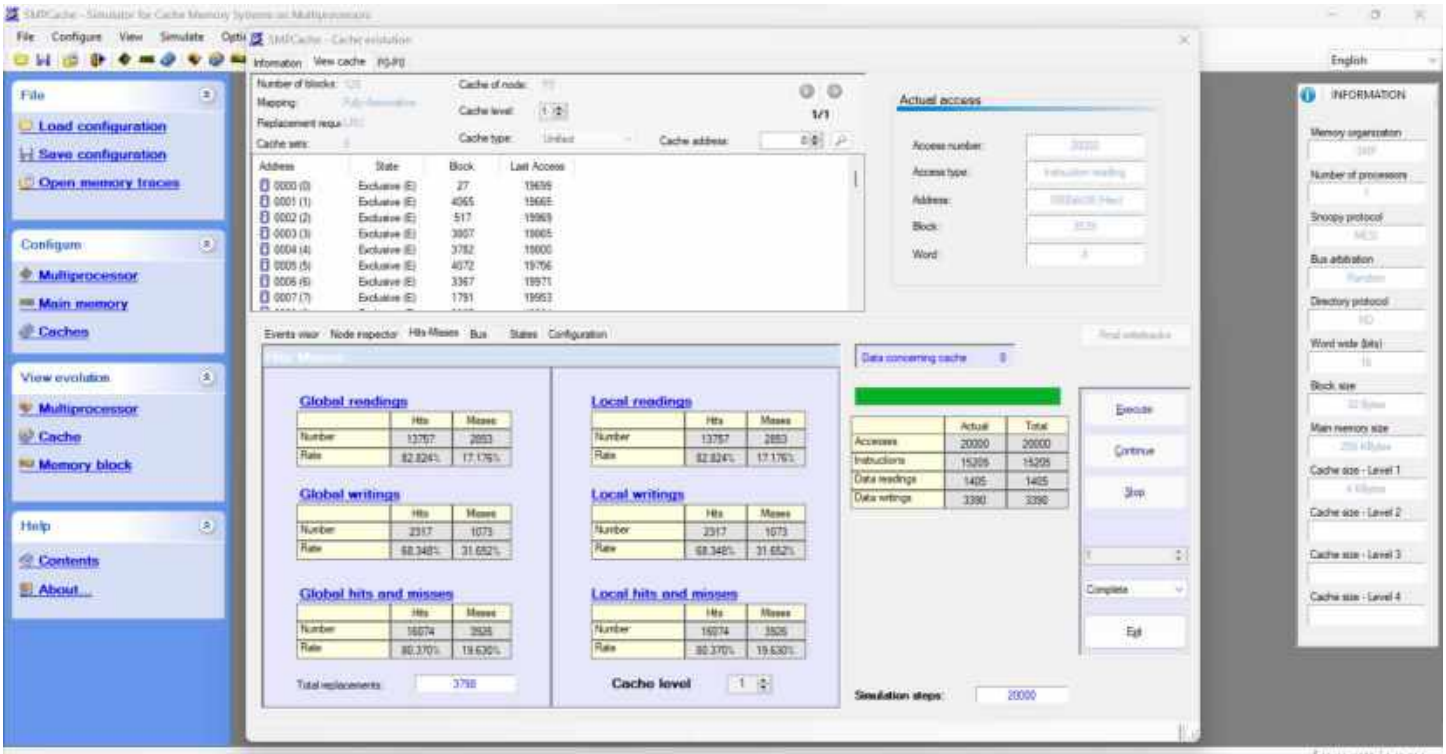
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Local writings
Global hits and misses
Local hits and misses
Cache level
Actual access
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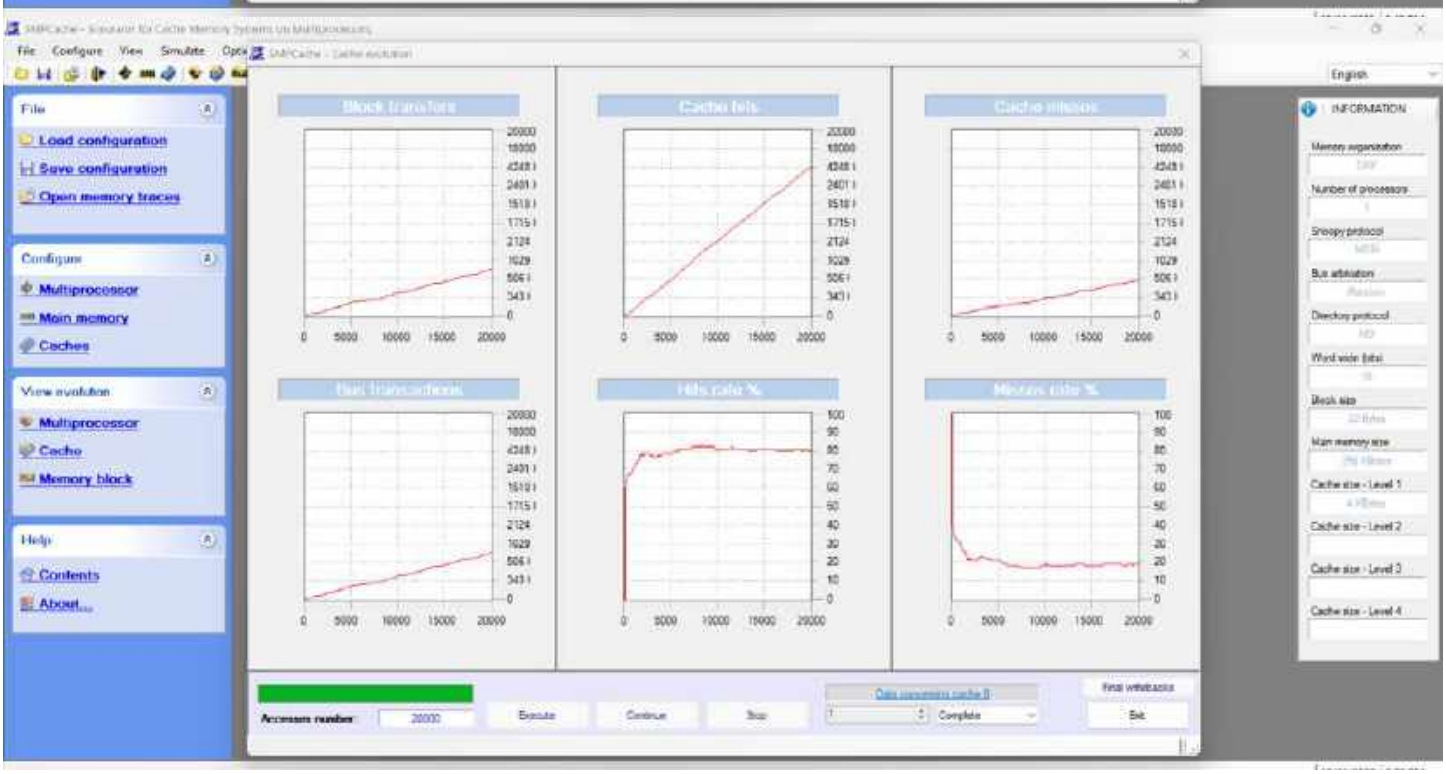
INFORMATION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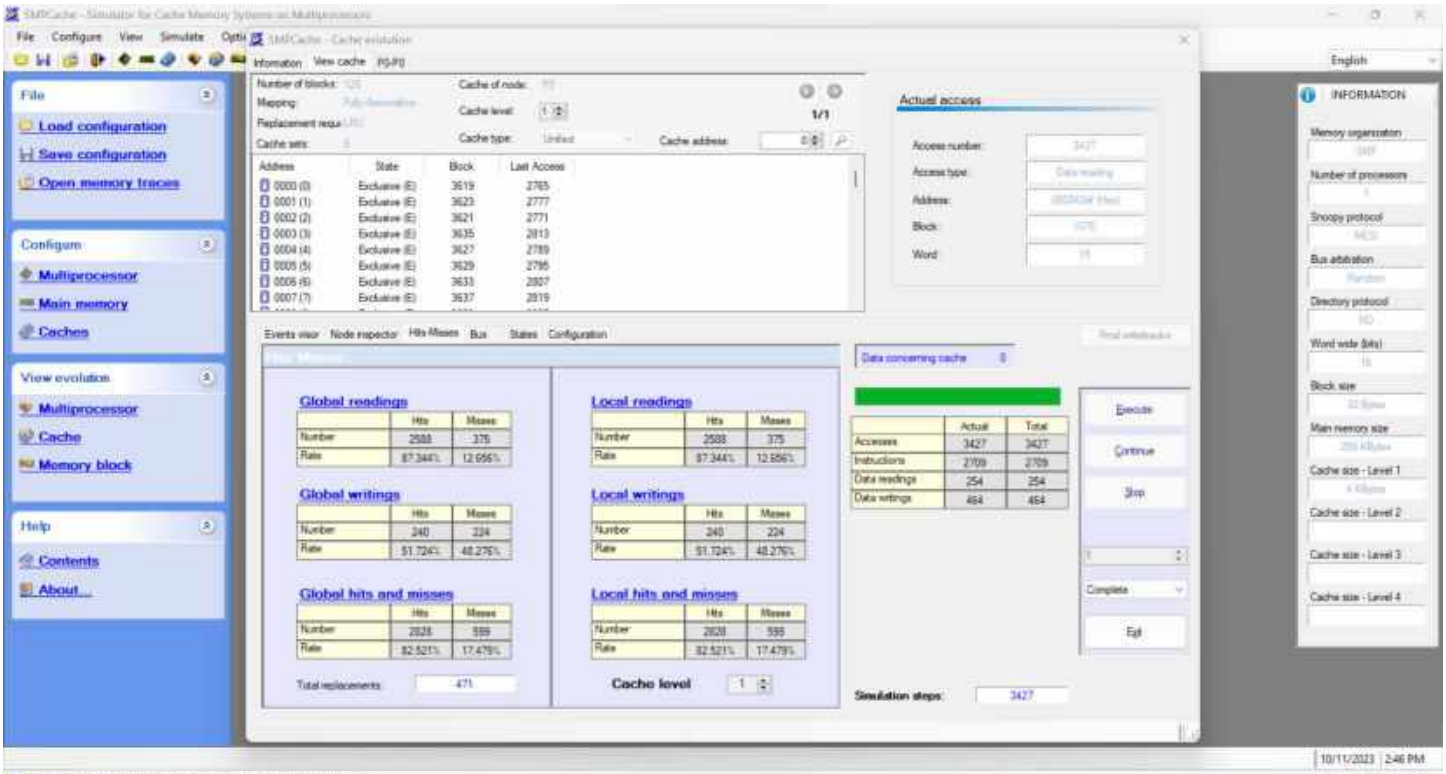
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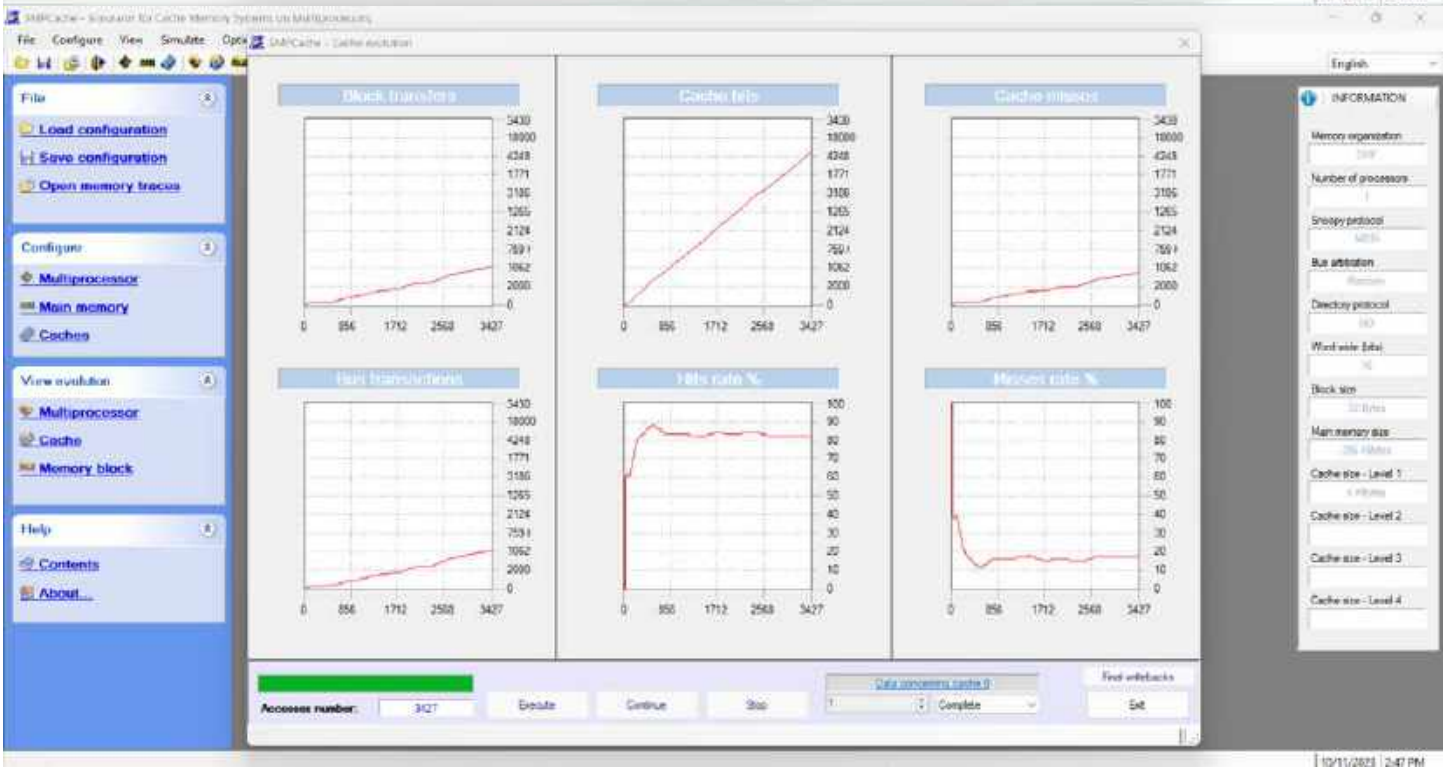
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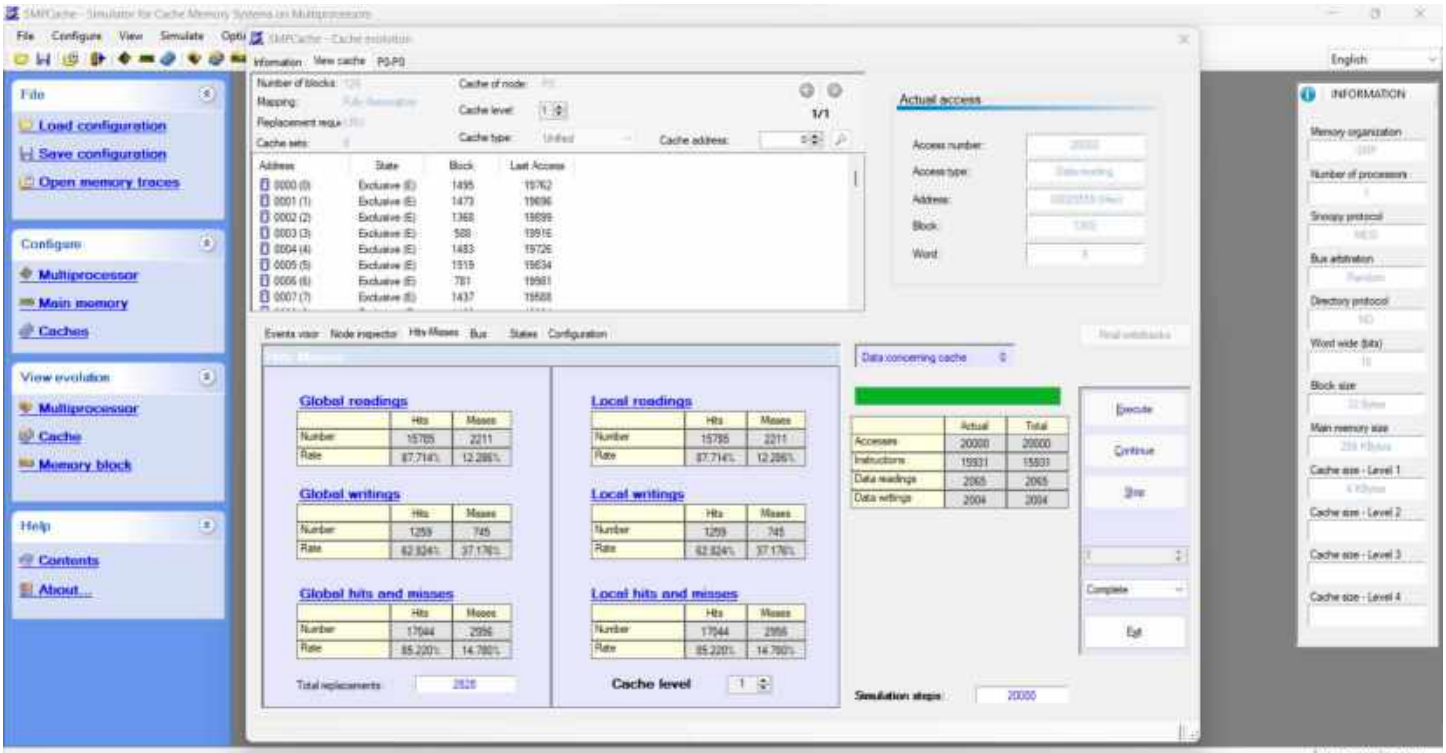
Mdljd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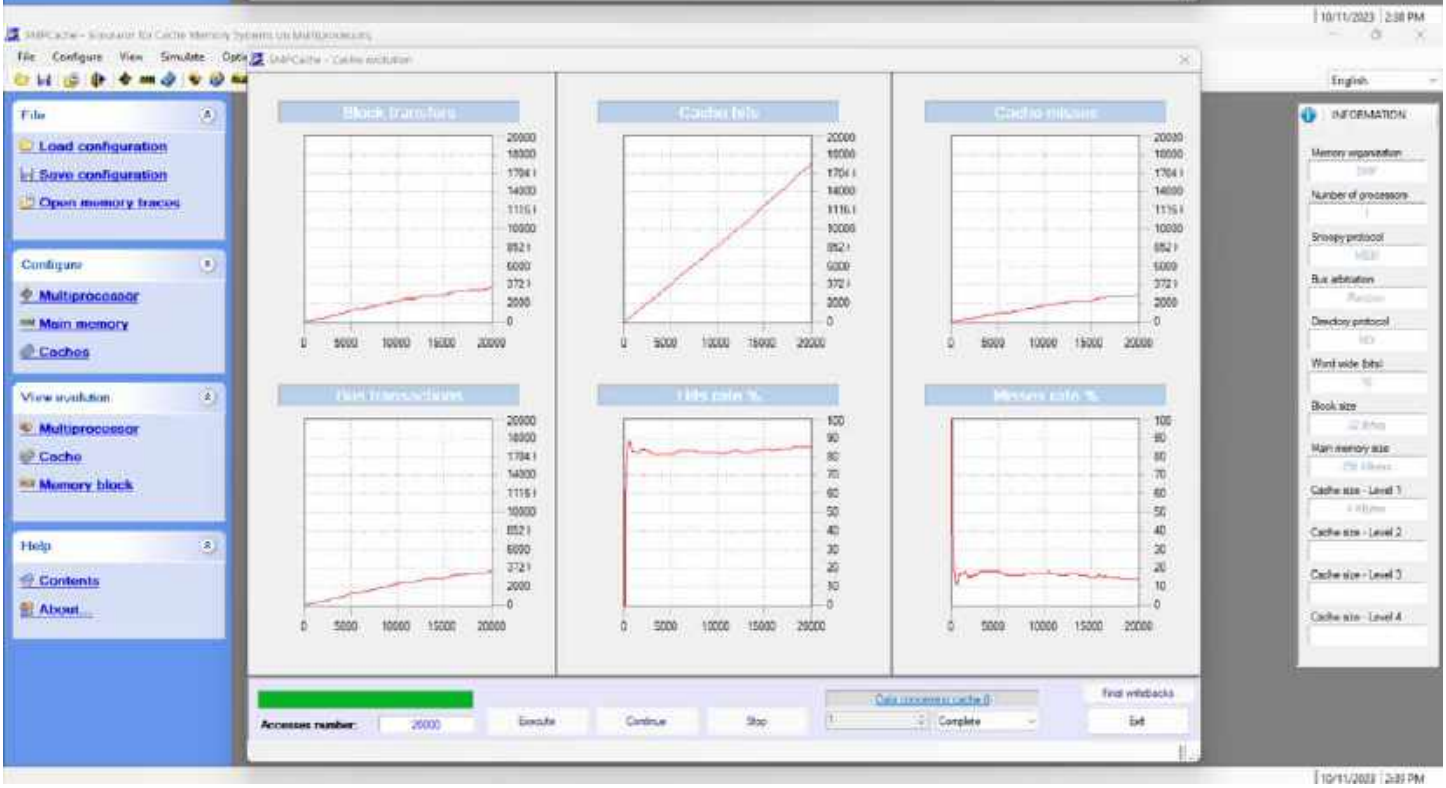
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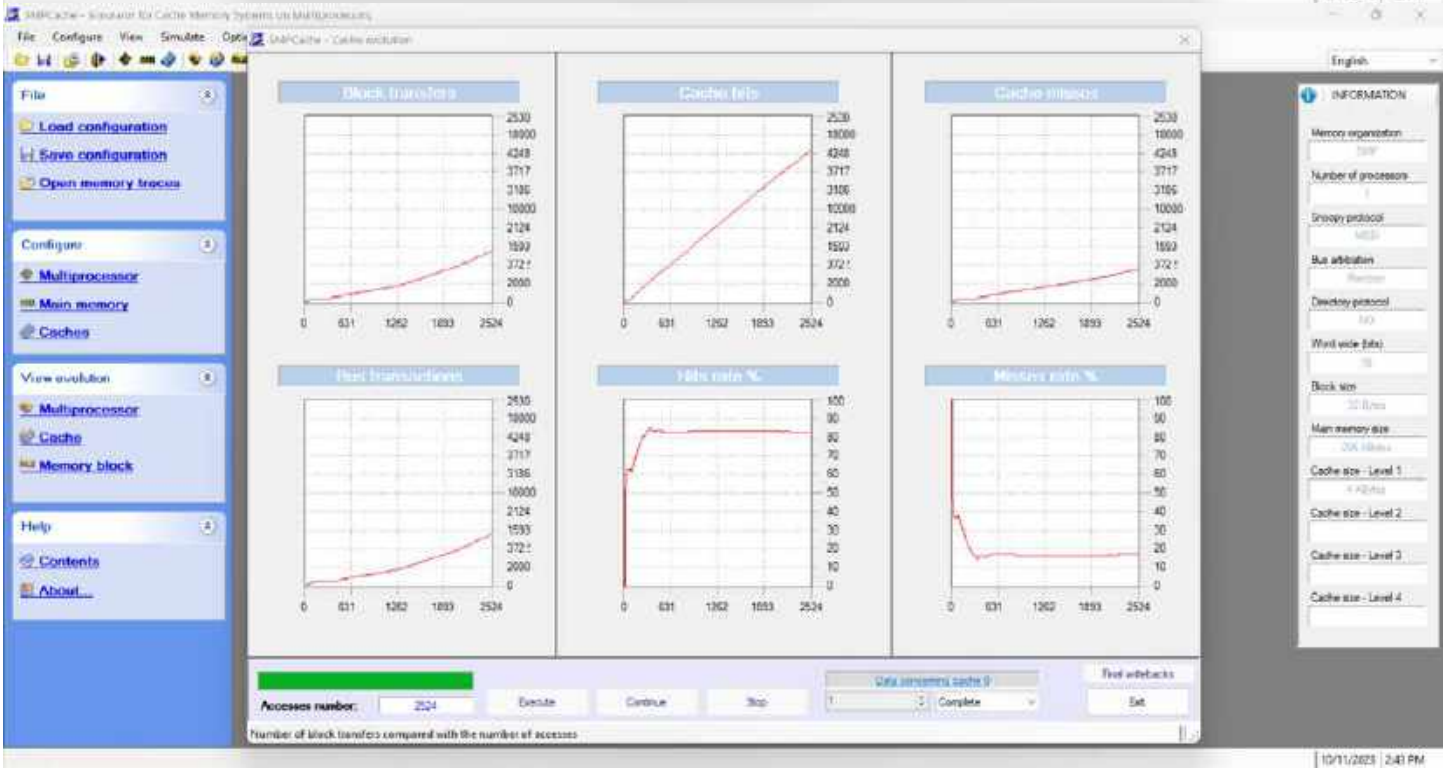
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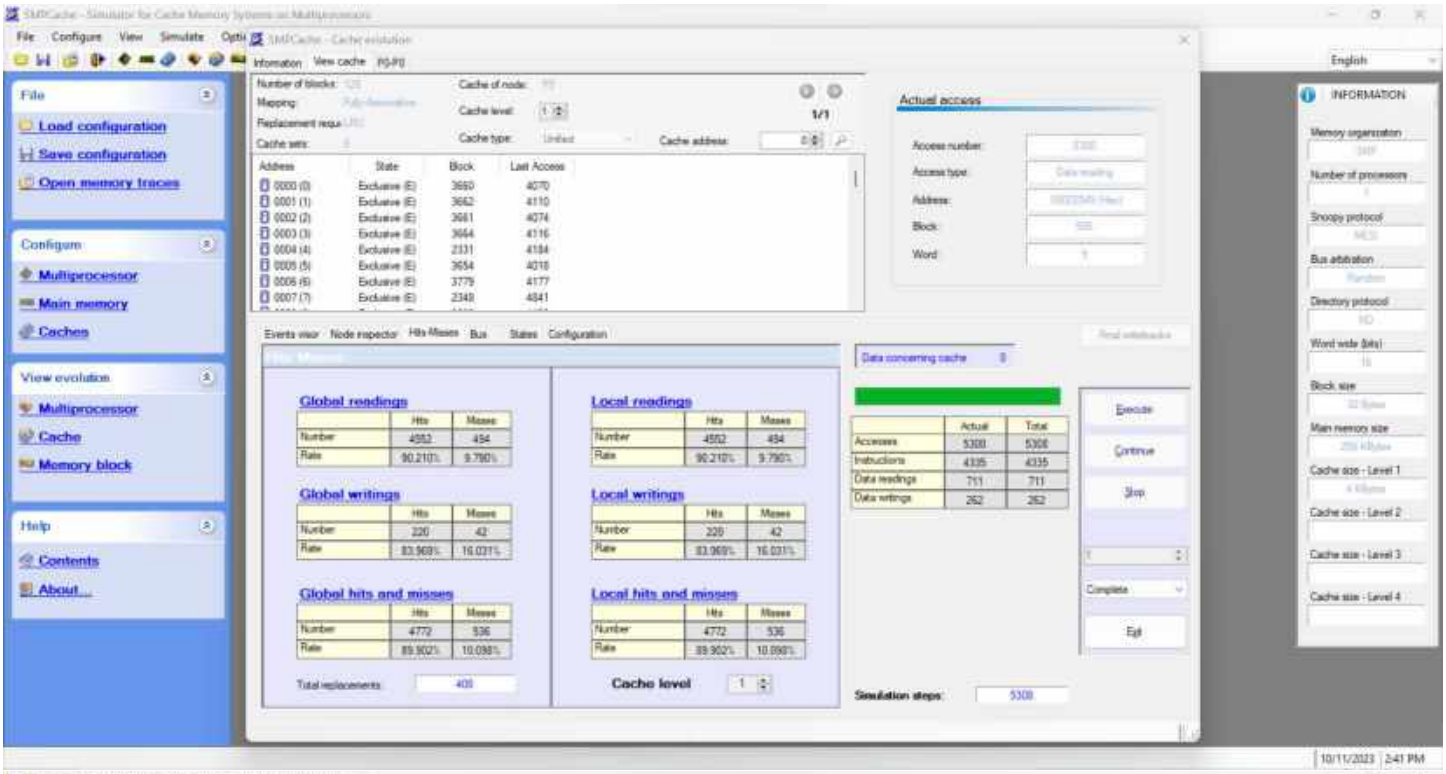
Ear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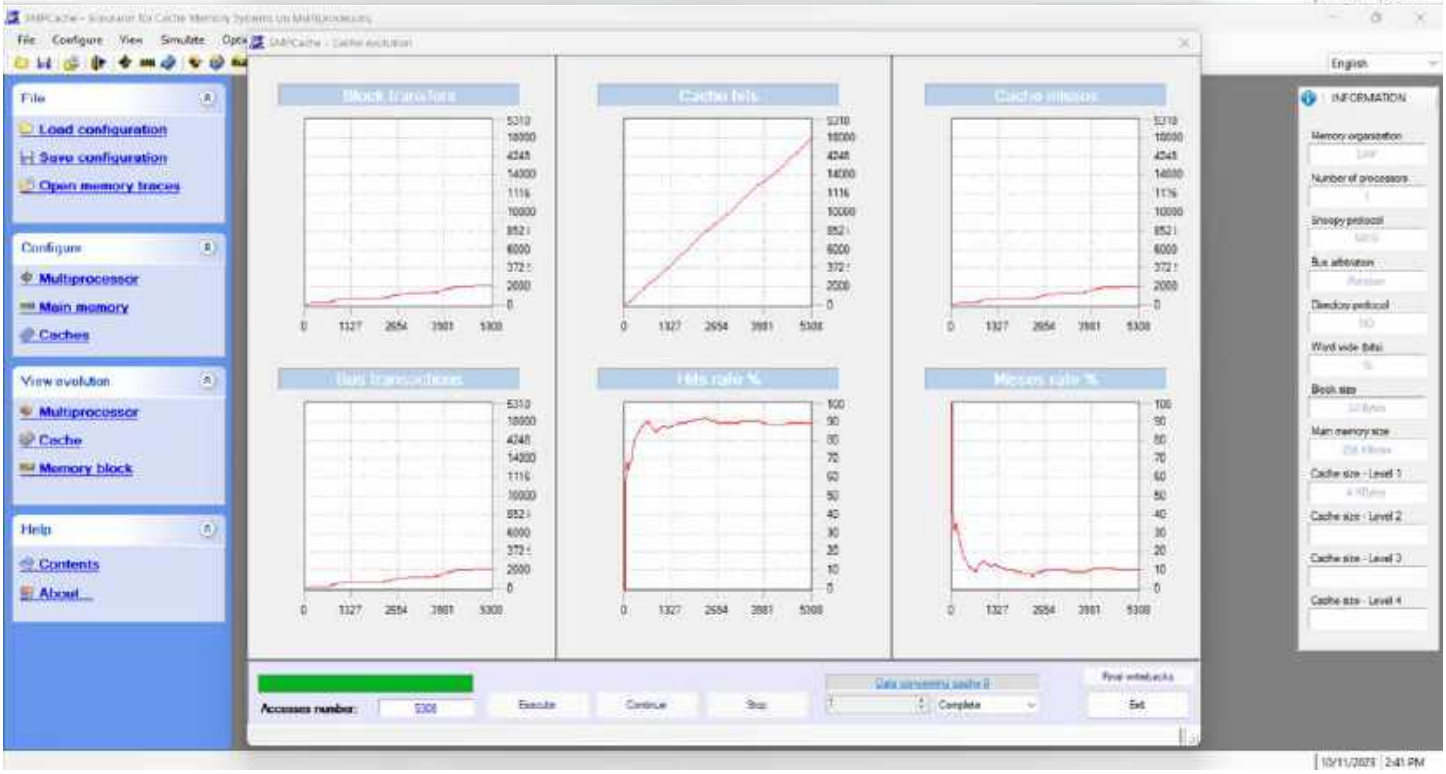
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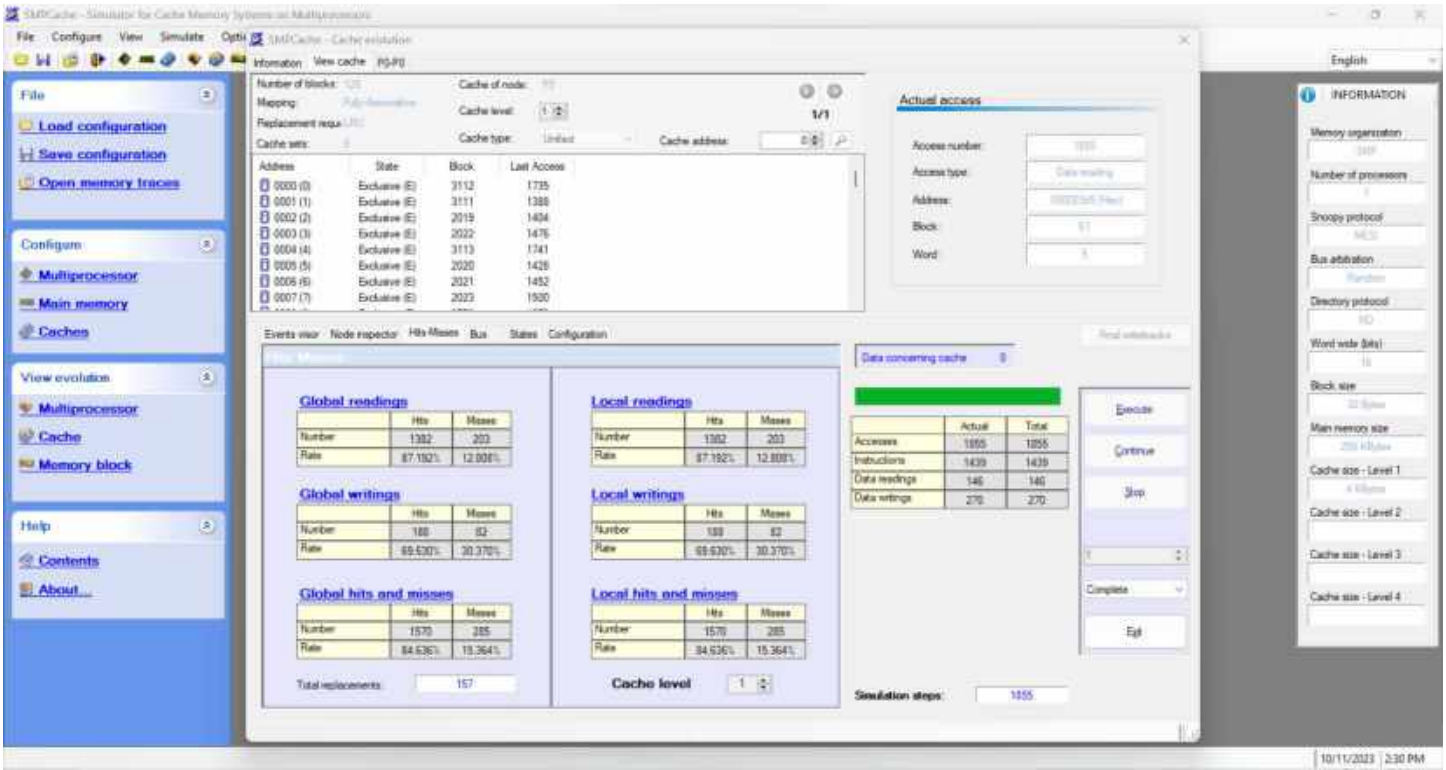
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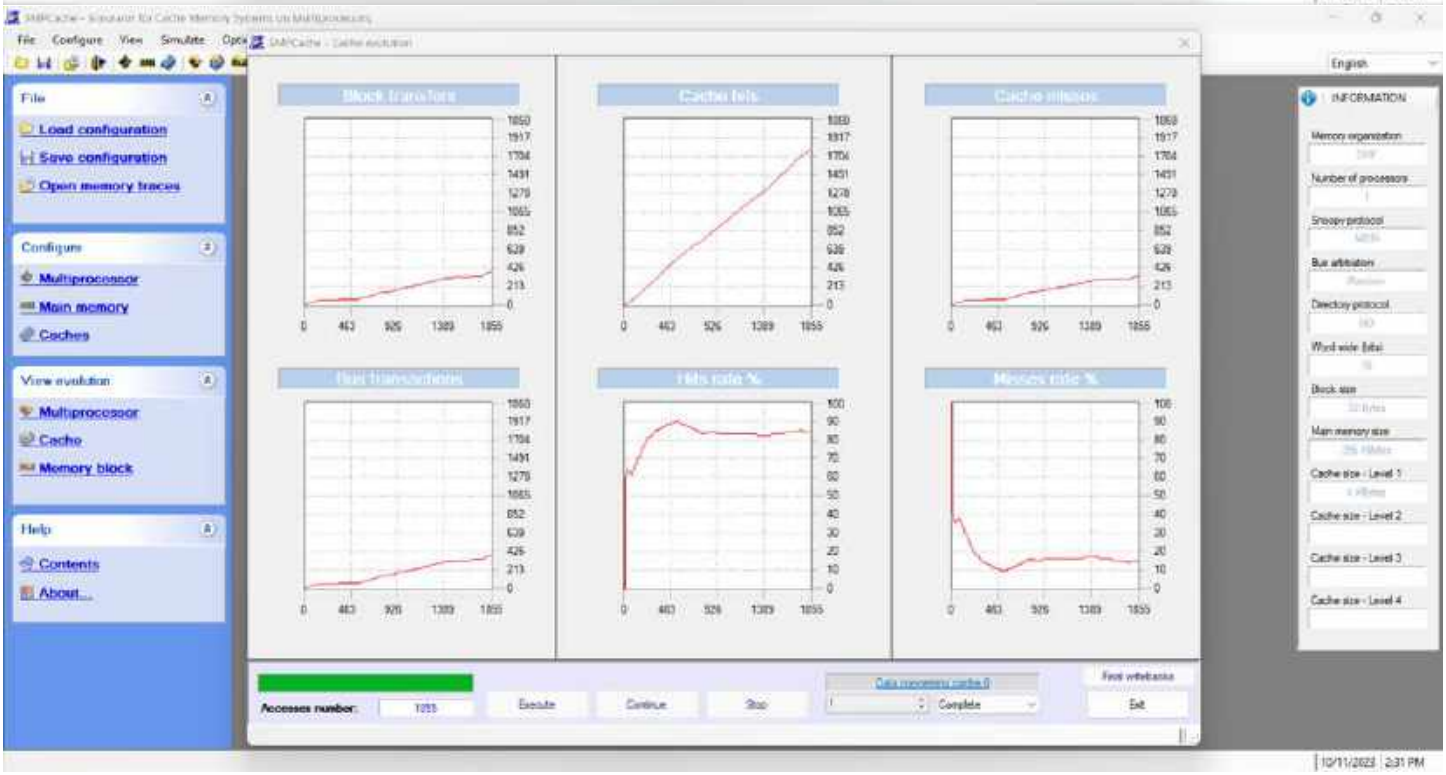
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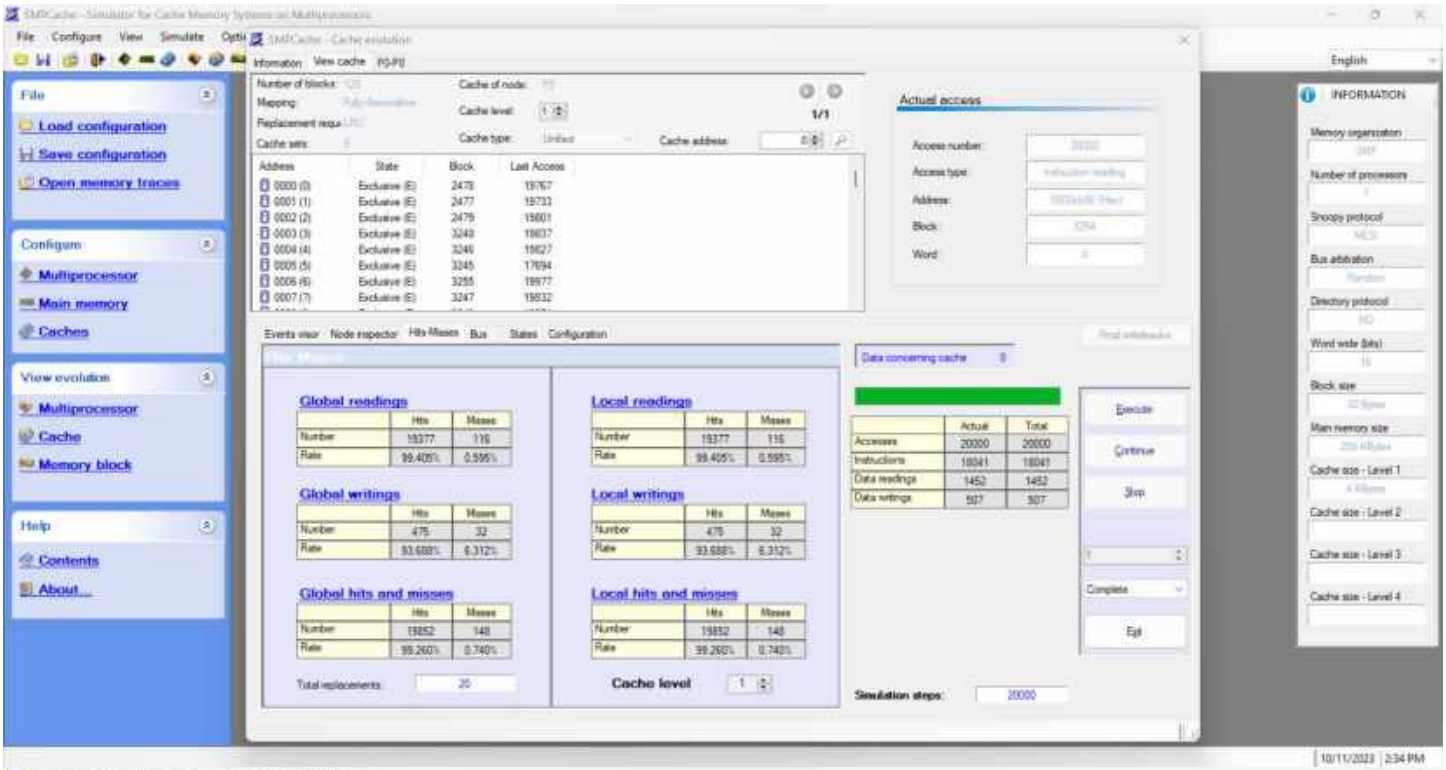
Cexp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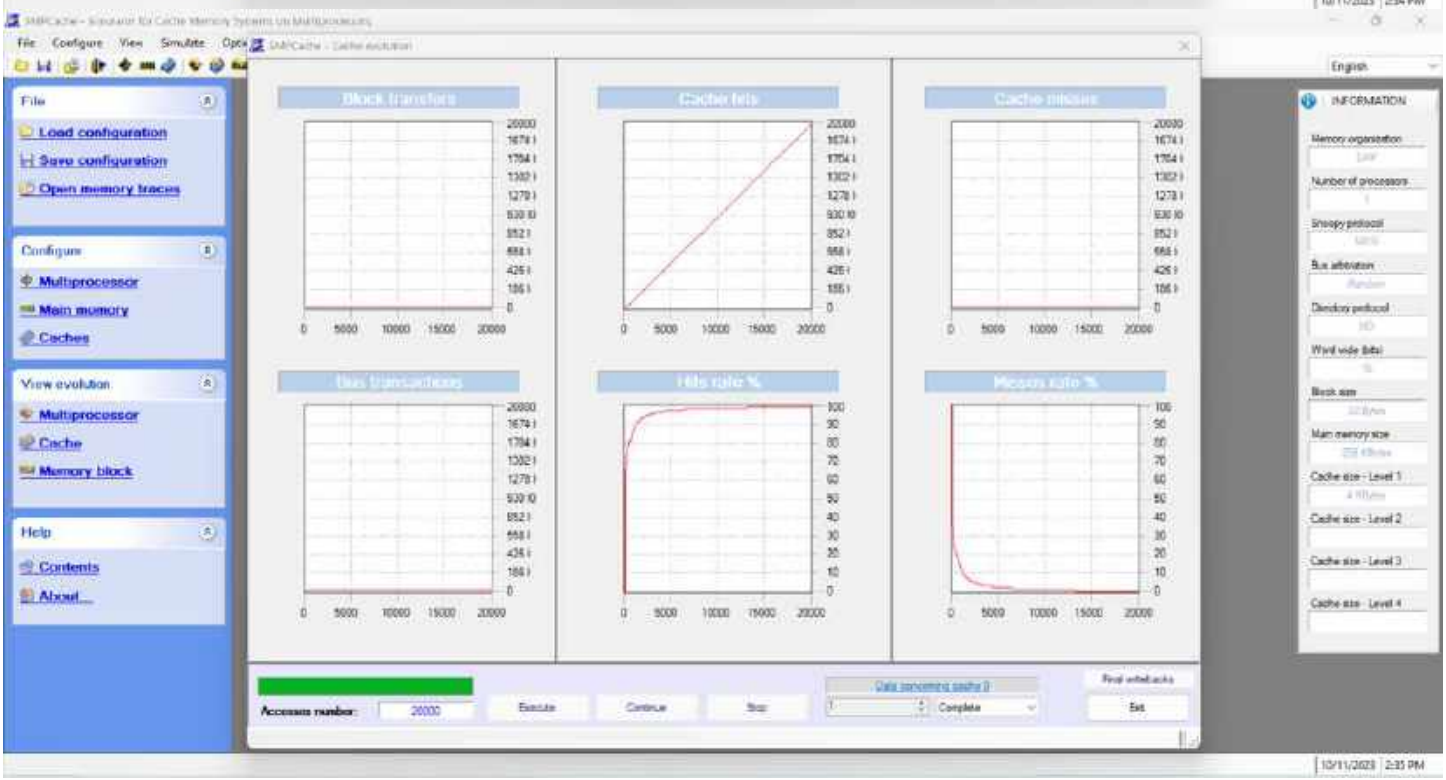
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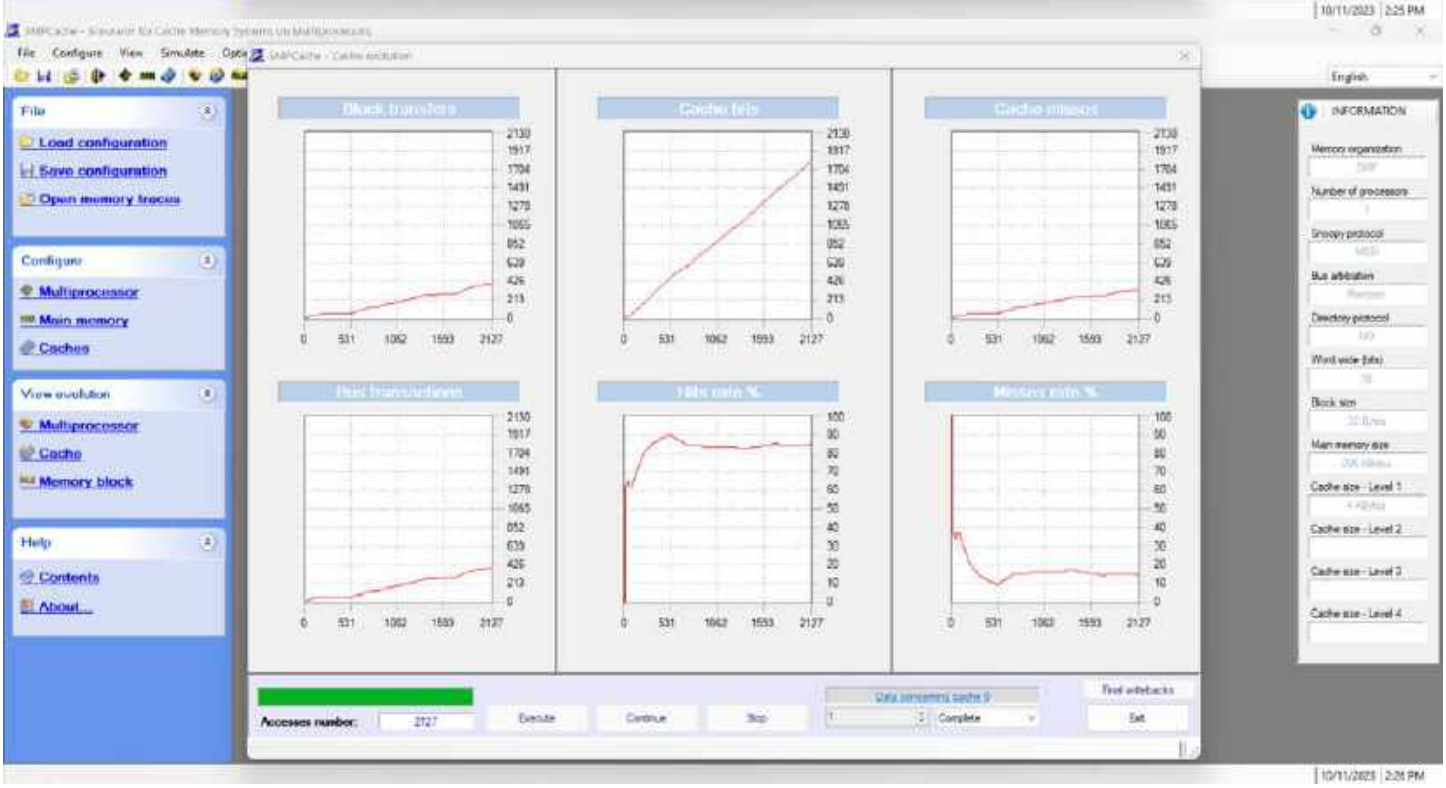
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Q. Do all the programs have the same locality grade (i.e., local or global)? Which is the program with the best locality? And which does it have the worst?

A. The experimental results clearly exhibit distinct locality grades for various programs, even when they possess the same instruction count. This discrepancy is reflected in different hit/miss ratios, block transfers, and total replacements.

CEXP stands out for having the best locality, boasting a remarkably lowest Miss Rate or a highest Hit Rate. Conversely, SWM demonstrates the weakest locality, resulting in the highest Miss Rate or the lowest Hit Rate.

Q. Do you think that the design of memory systems that exploit the locality of certain kind of programs (which will be the most common in a system) can increase the system performance? Why?

A. Indeed, optimizing memory system designs to exploit the specific locality patterns of programs can greatly enhance system performance. Leveraging temporal locality ensures frequently accessed data remains close to the processor, while capitalizing on spatial locality ensures efficient placement of crucial data needed in subsequent processing stages. Memory systems achieve this by incorporating larger block sizes and caches.

Q. During the development of the experiments, you can observe graphically how, in general, the miss rate decreases as the execution of the program goes forward. Why? Which is the reason?

A. The miss rate diminishes as the cache starts accommodating the processor's most frequently accessed requests. Moreover, it decreases as both bus transactions and block transfers increase, effectively optimizing the pertinent data requested by the processor.

Task 2

Influence of the Cache Size

Purpose

Show the influence of the cache size on the miss rate.

Configuration

Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 16.
Words by block = 16 (block size = 32 bytes).
Blocks in main memory = 8192 (main memory size = 256 KB).
Mapping =
Fully-Associative.
Replacement policy = LRU.

Experiment

Configure the blocks in cache using the following configurations: 1 (cache size = 0,03 KB), 2, 4, 8, 16, 32, 64, 128, 256, and 512 (cache size = 16 KB). For each of the configurations, obtain the miss rate using the trace files (extension ".prg"): Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.

Questions

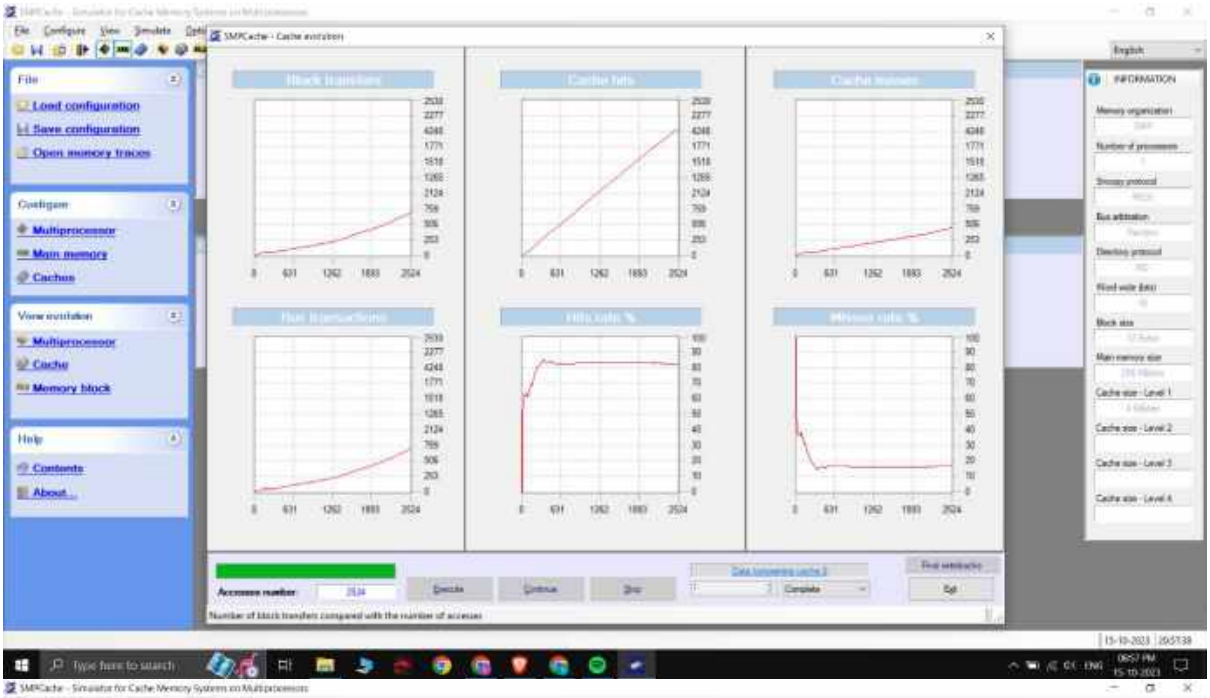
Does the miss rate increase or decrease as the cache size increases? Why? Does this increment or decrement happen for all the benchmarks or does it depend on the different locality grades? What does it happen with the capacity and conflict (collision) misses when you enlarge the cache? Are there conflict misses in these experiments? Why?
In these experiments, it may be observed that for great cache sizes, the miss rate is stabilized. Why? We can also see great differences of miss rate for a concrete increment of cache size. What do these great differences indicate? Do these great differences of miss rate appear at the same point for all the programs? Why?
In conclusion, does the increase of cache size improve the system performance?

Based on the results of our SMP cache simulator, we can confirm that the miss rate decreases with the increase in cache size. This happens because when we increase our cache size, we are able to store more data locally, and by virtue of that, increase the hit rate.

We were able to observe this decline in all of our benchmarks. The miss rate depends on the locality grade taking advantage of spatial locality.

If the cache is enlarged, it can contain all the blocks accessed by the program. This results in conflict which will make one memory location matched with the same cache location. There are no conflict misses in our experiments. This is because the cache size is increasing.

Comp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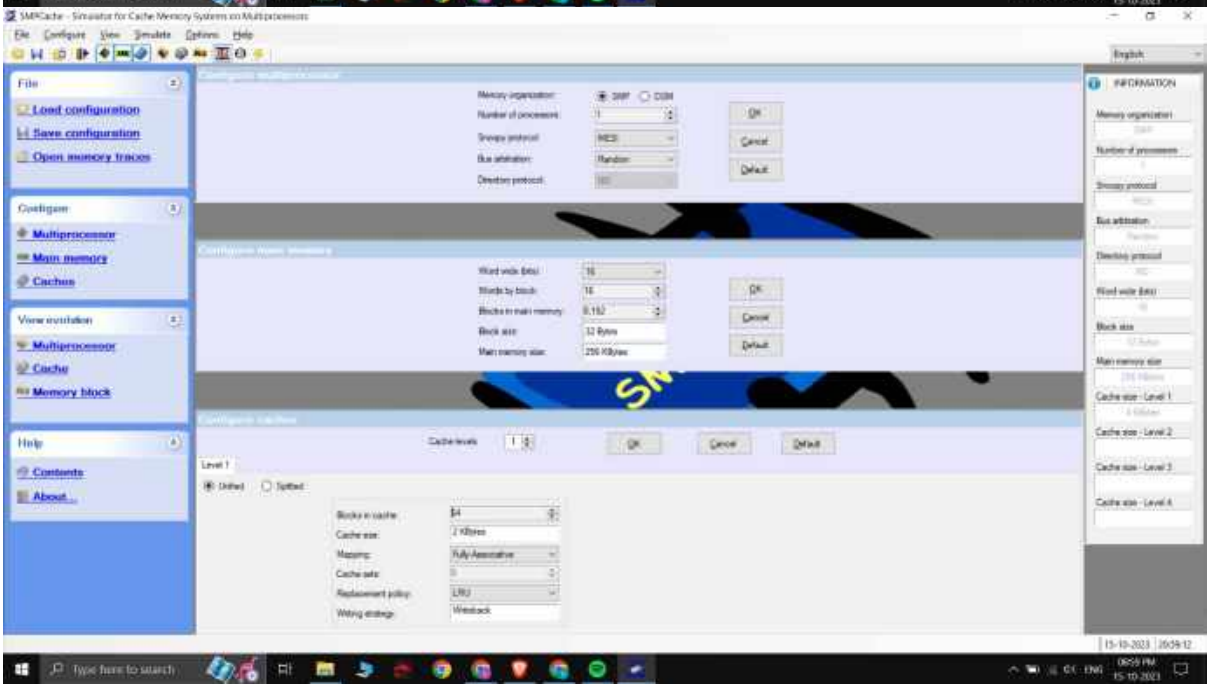
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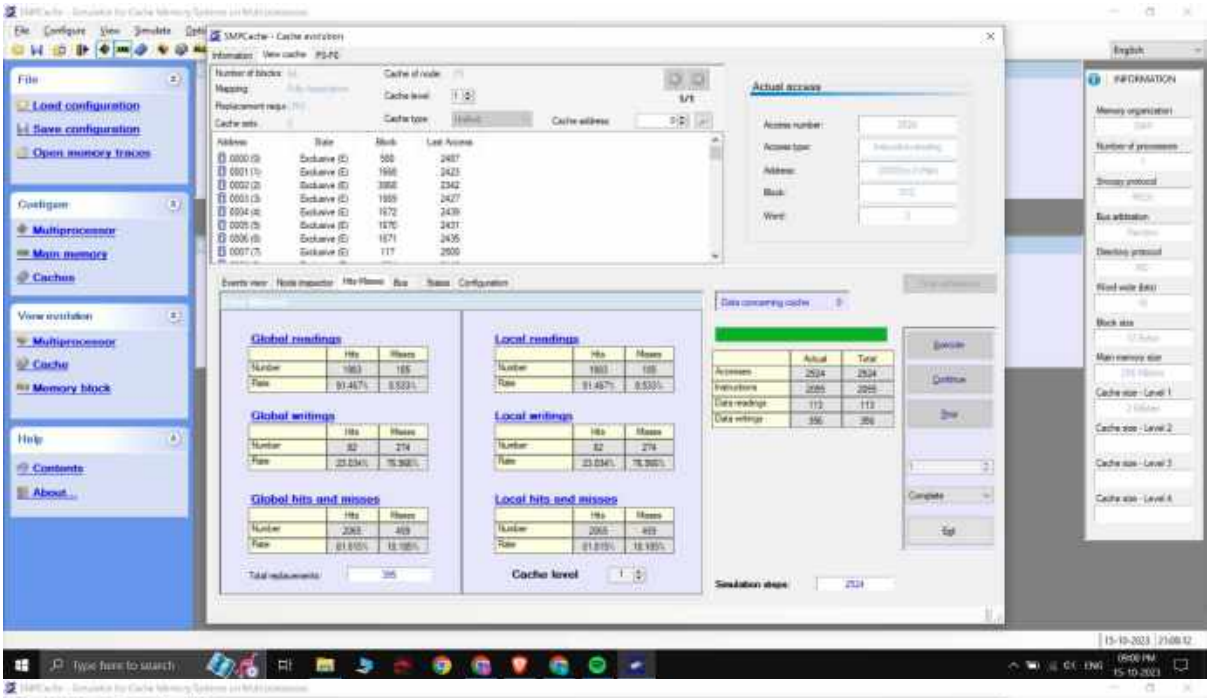
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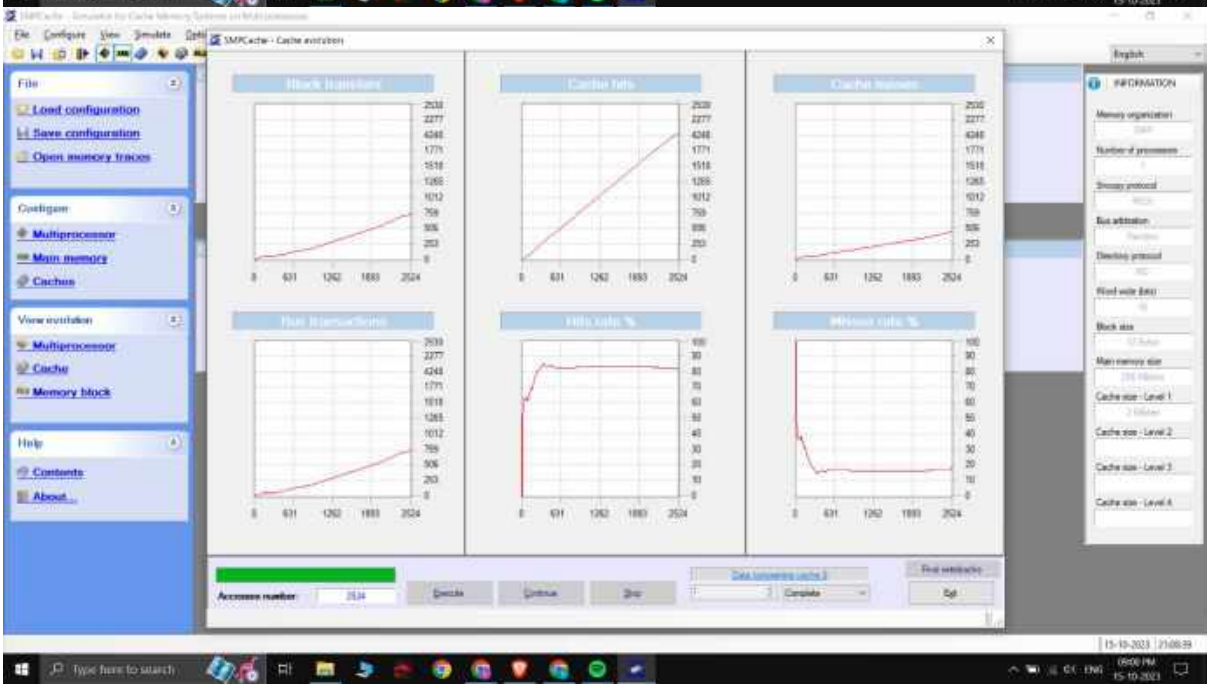
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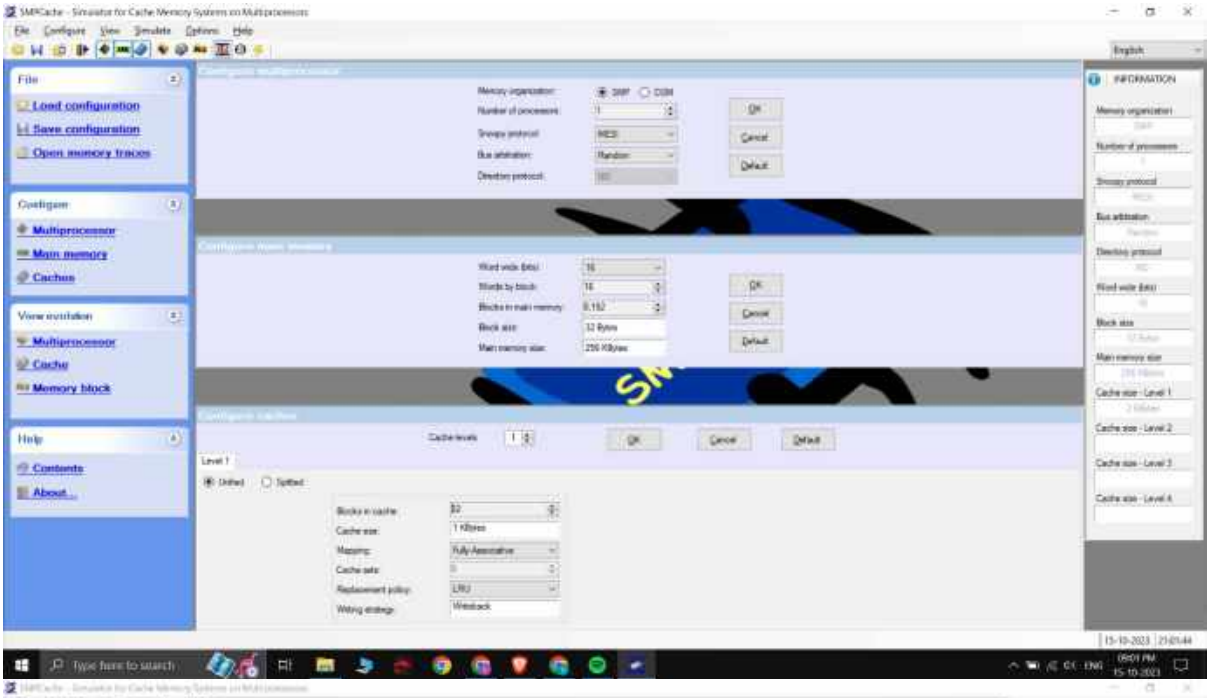
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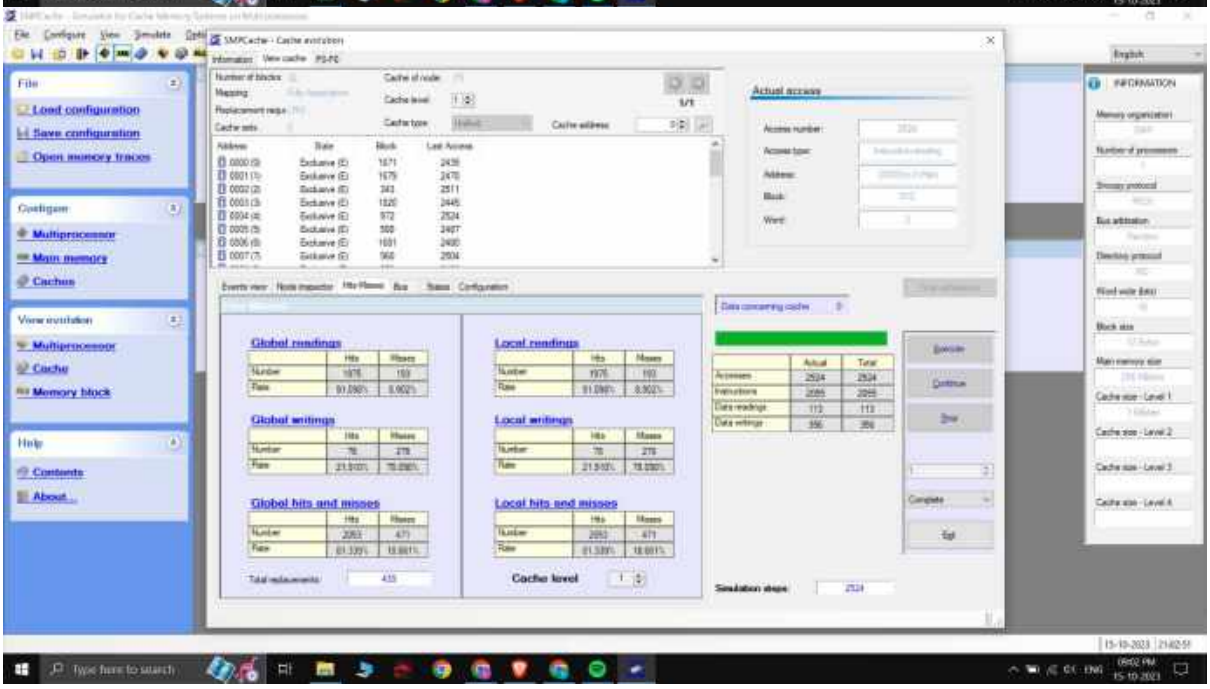
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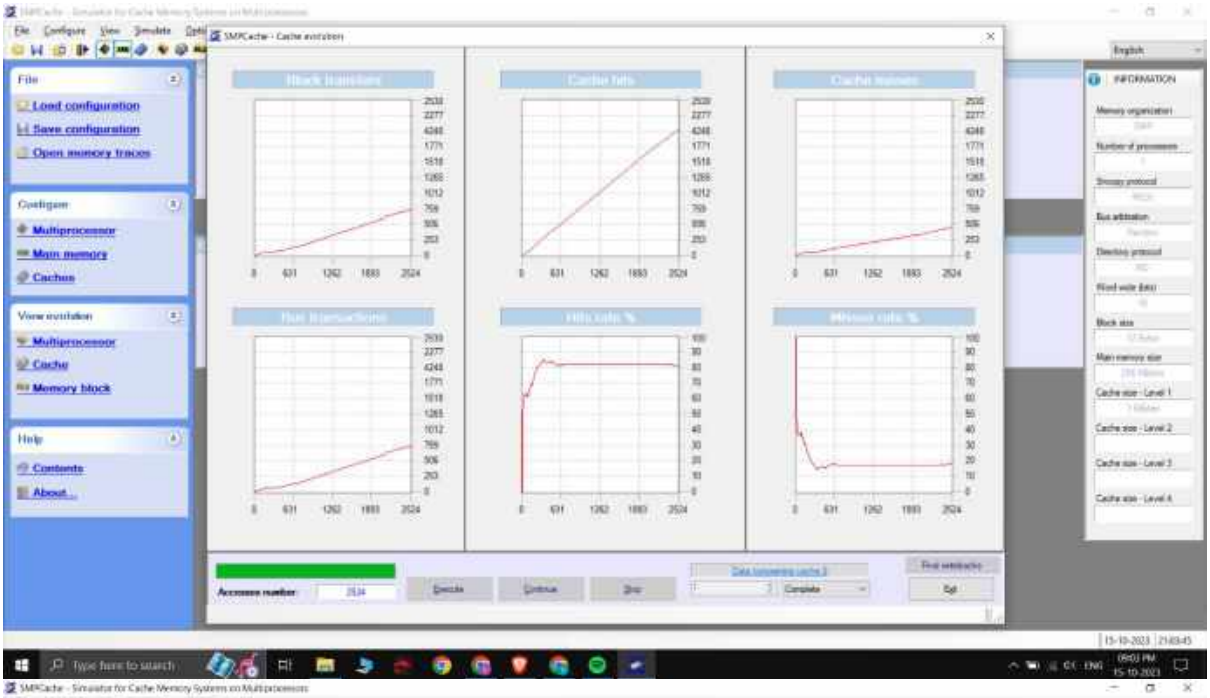
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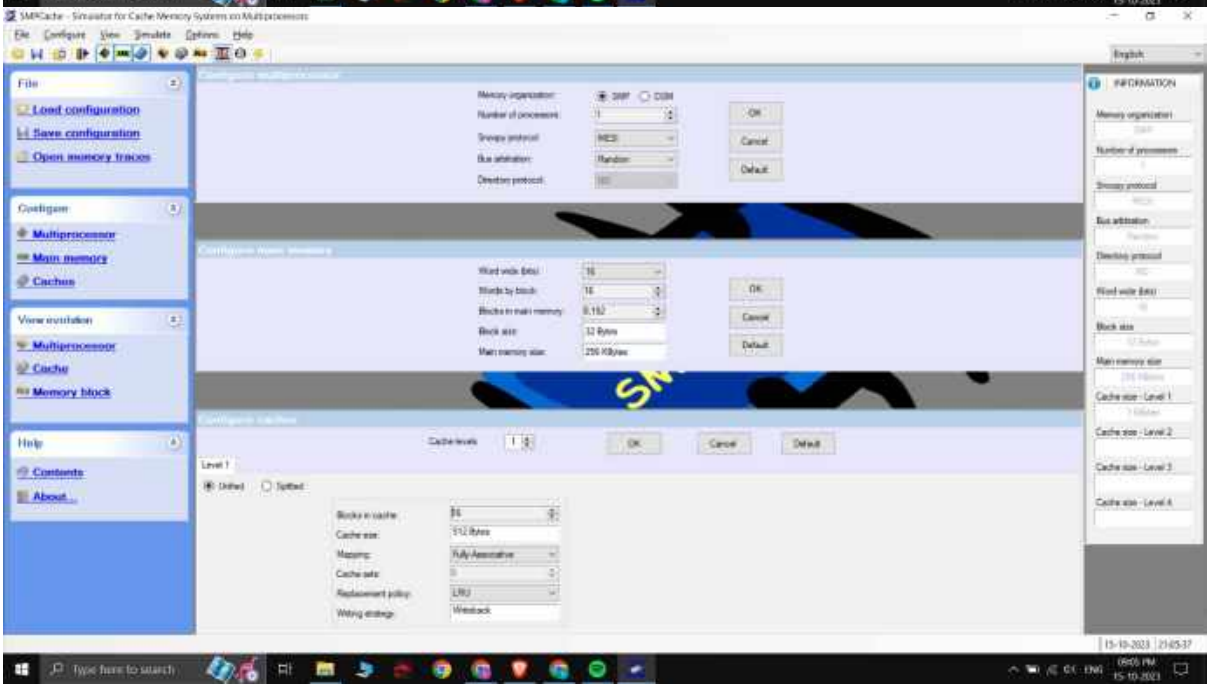
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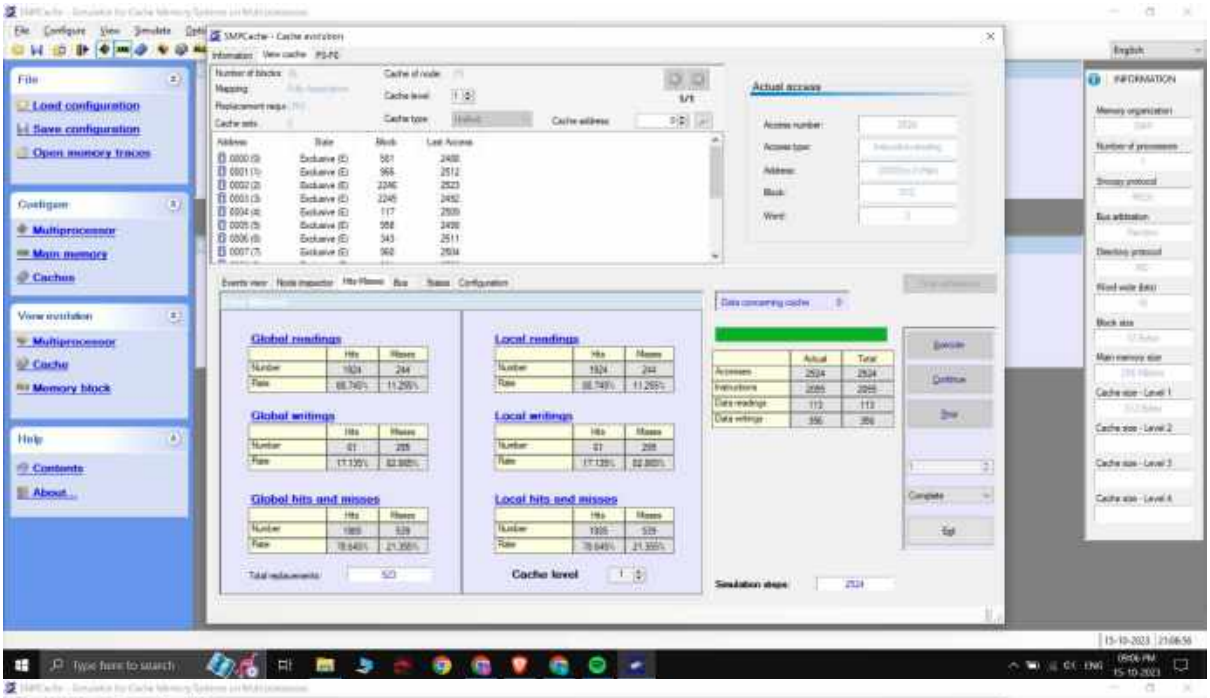
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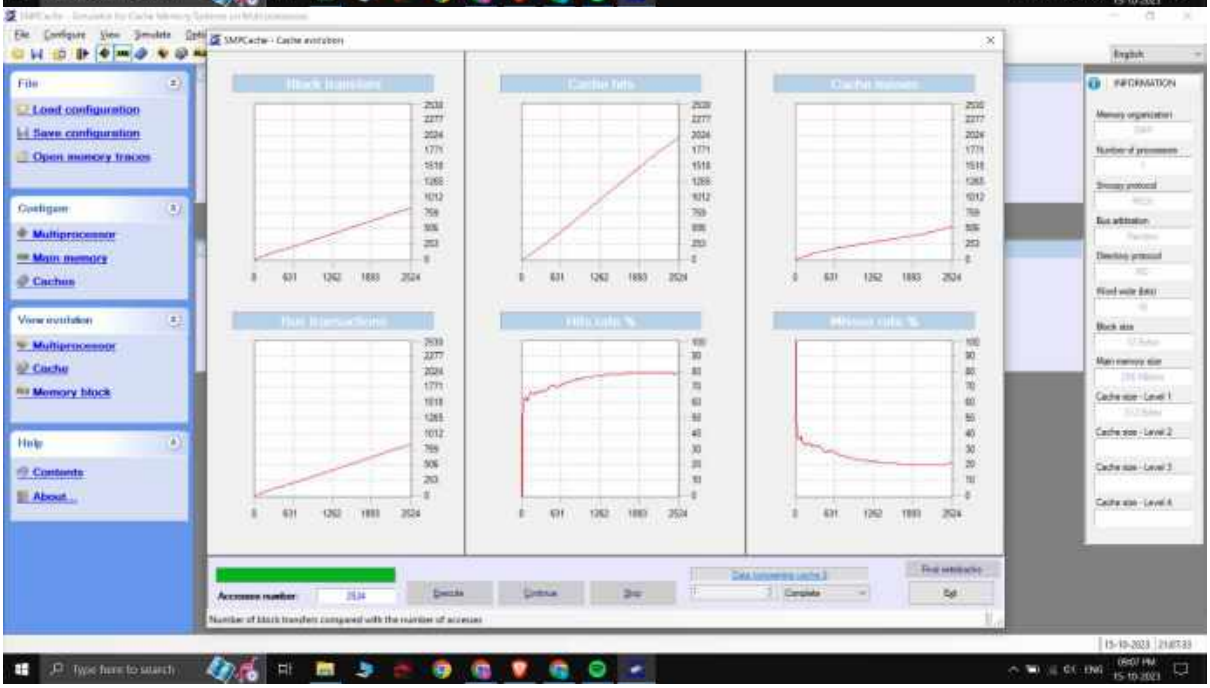
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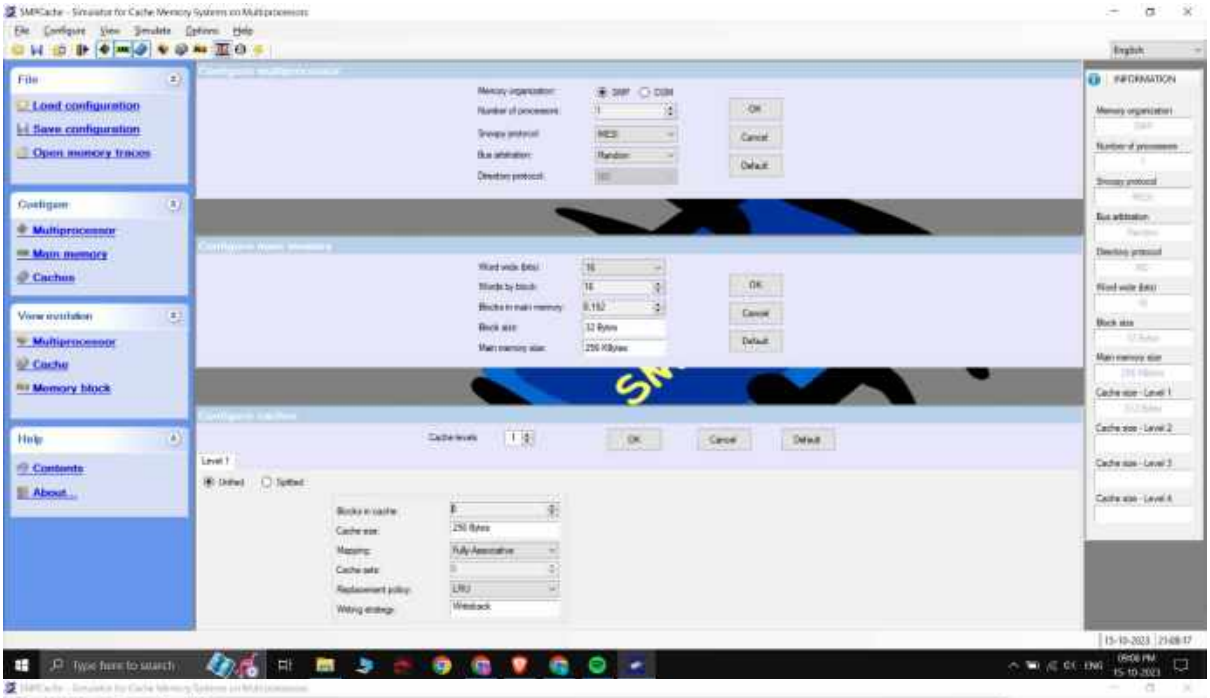
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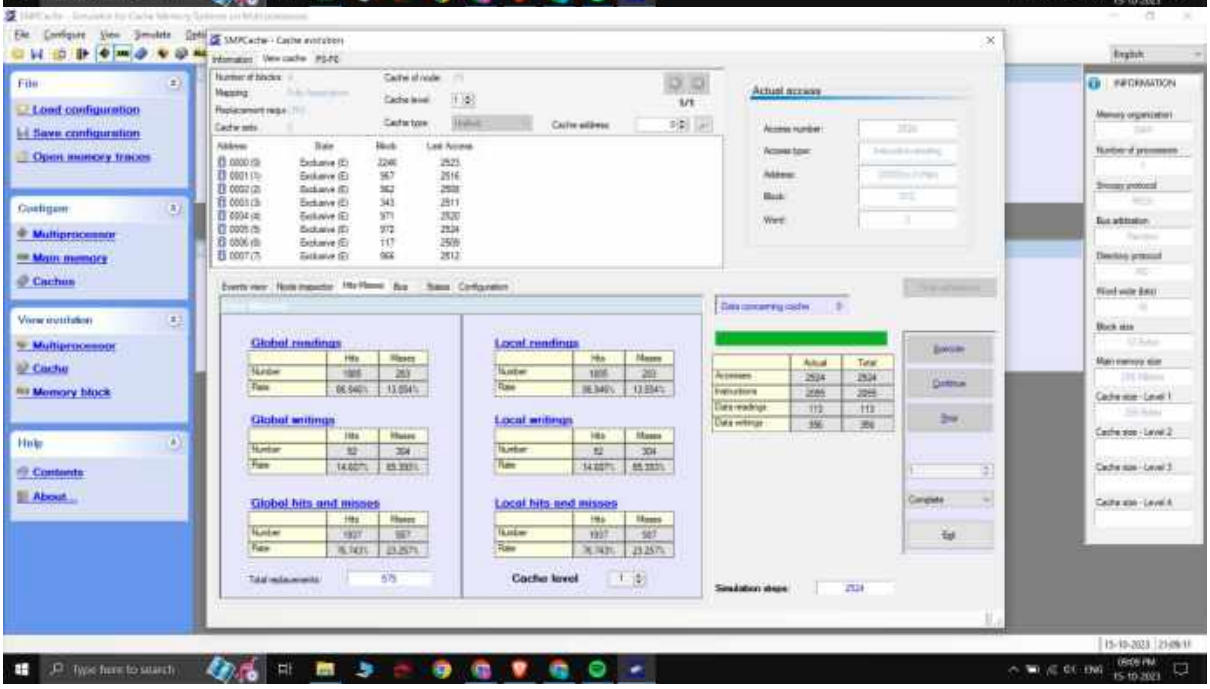
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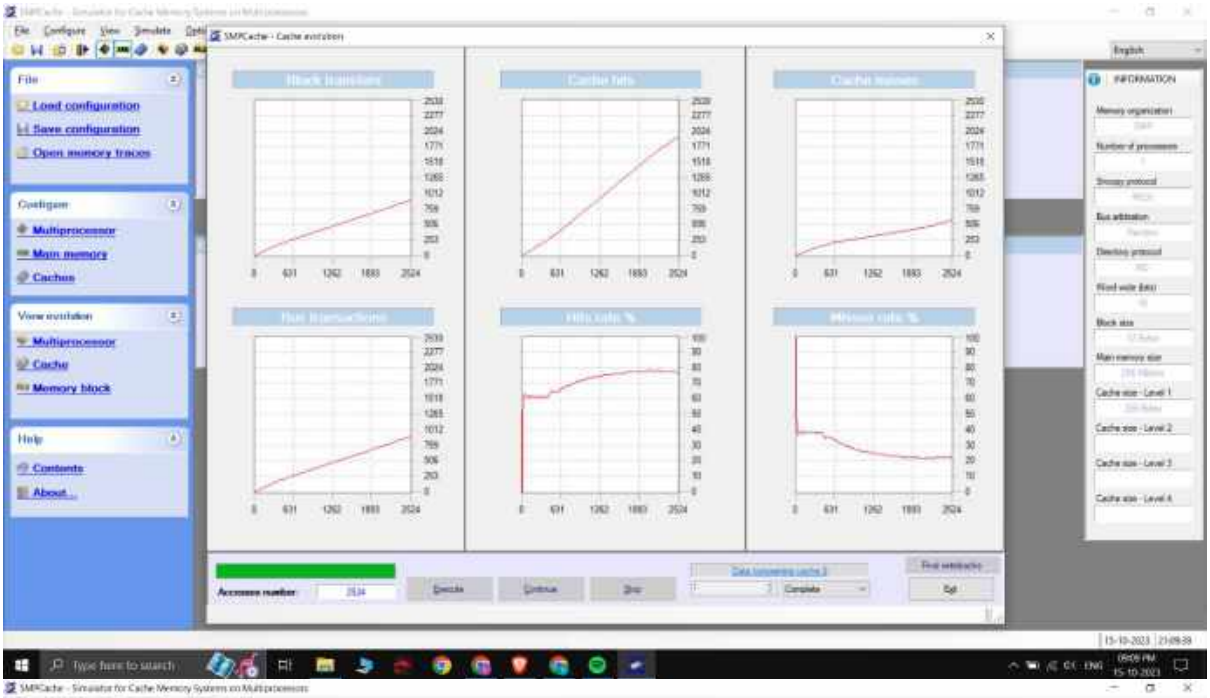
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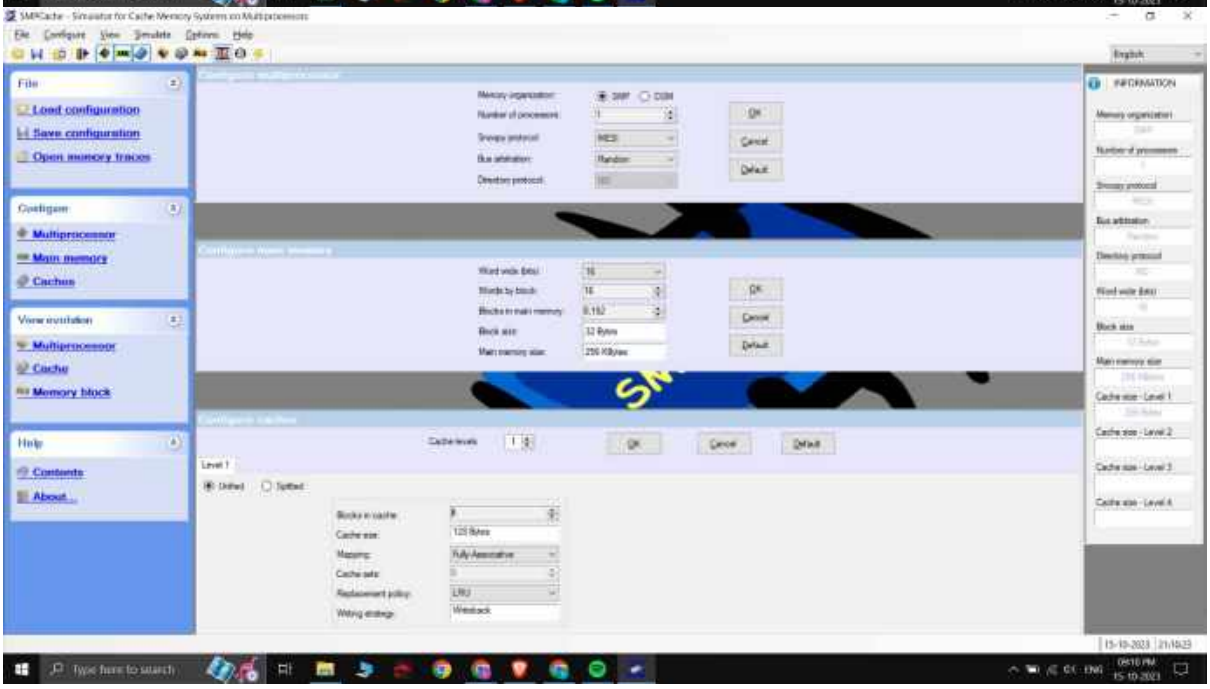
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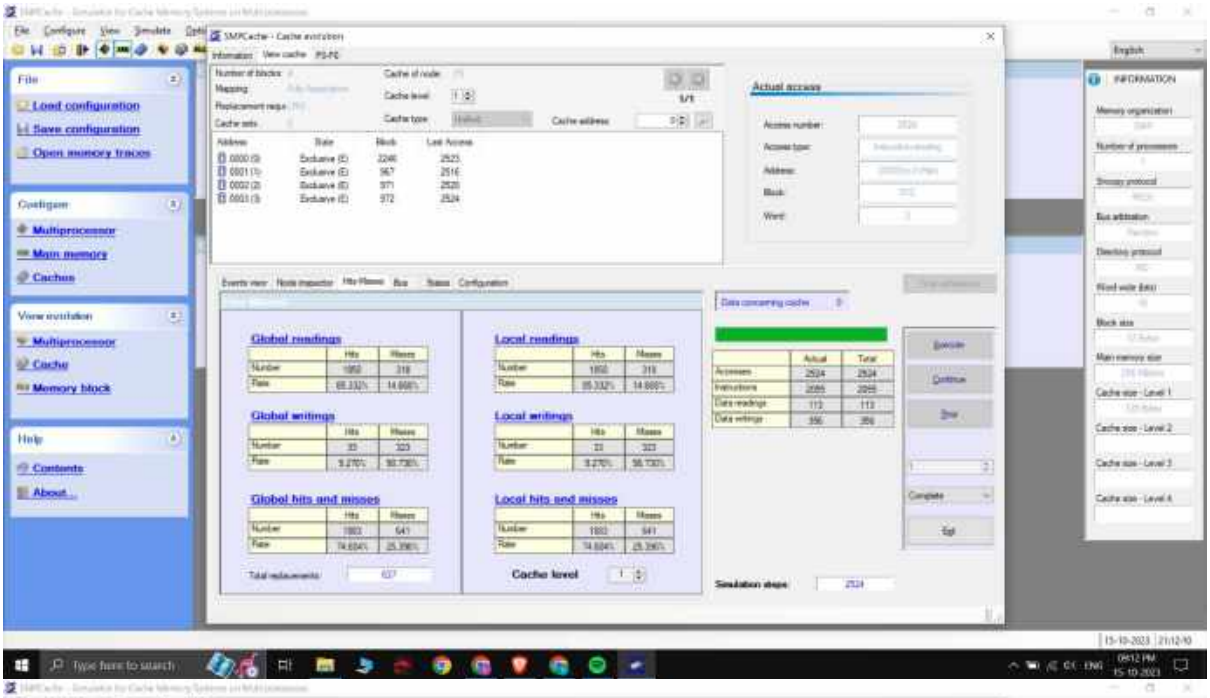
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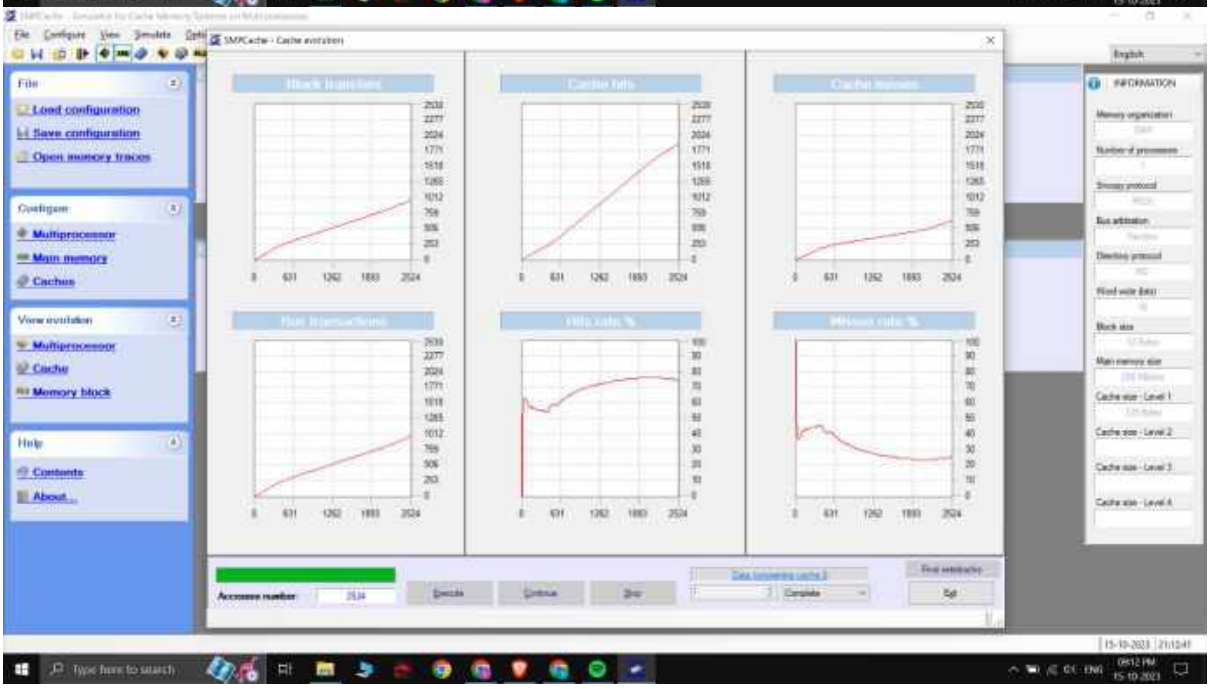
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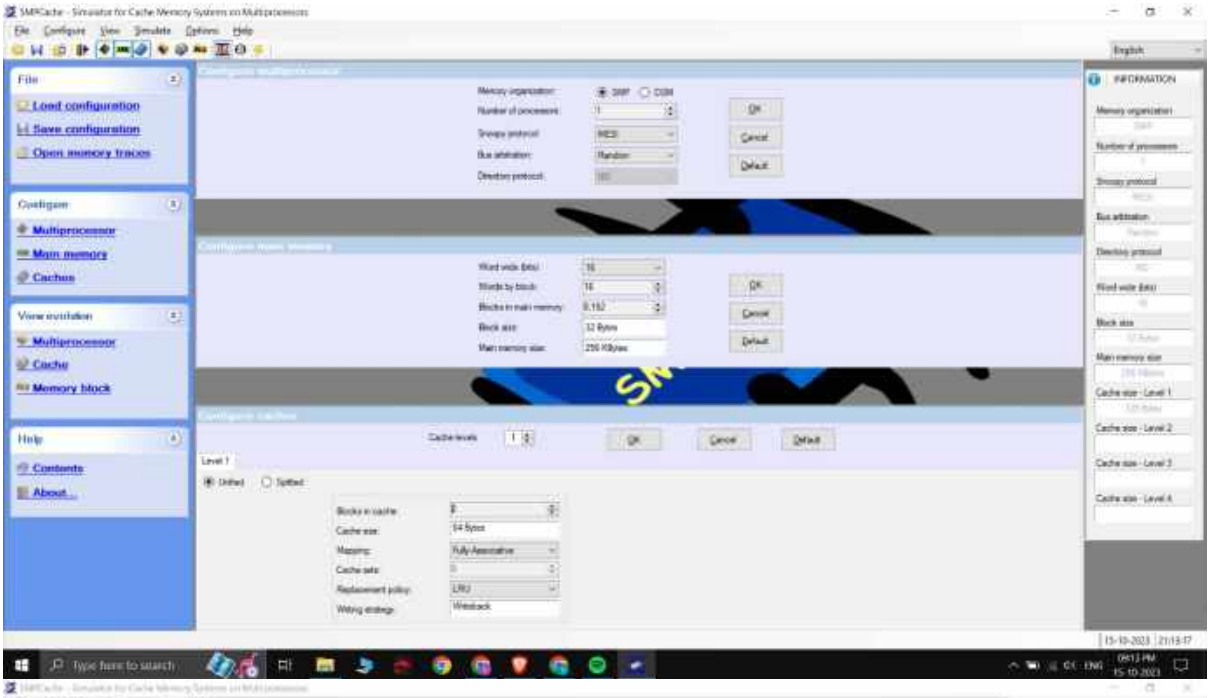
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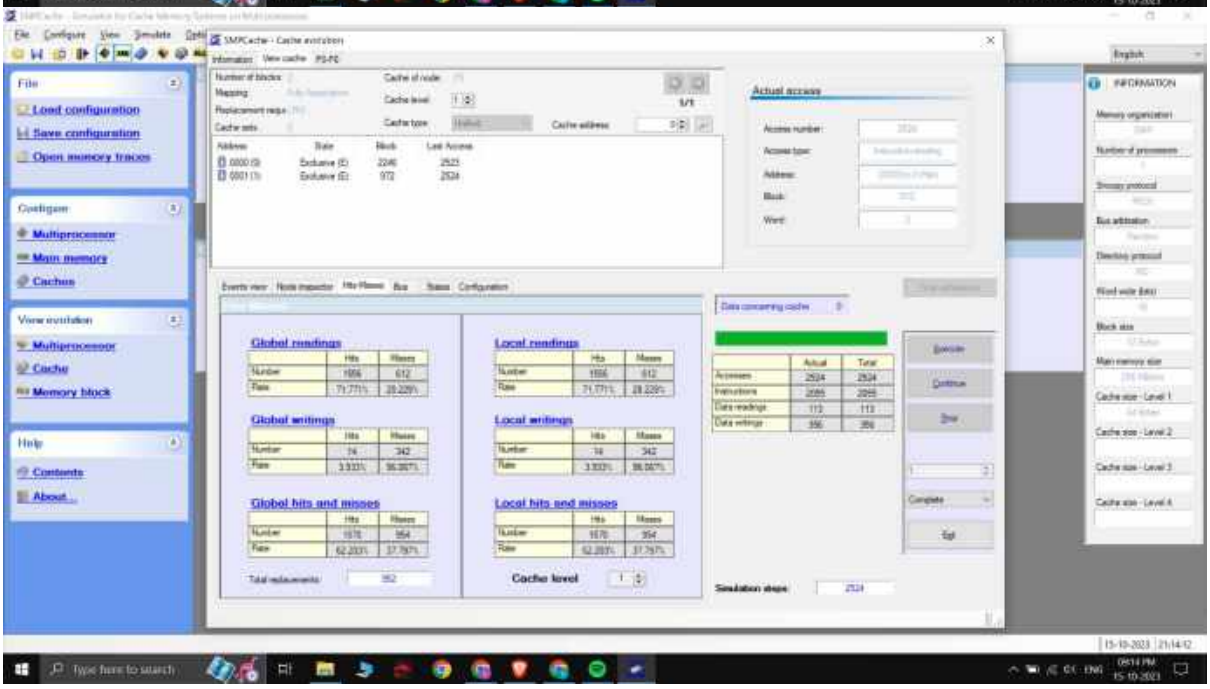
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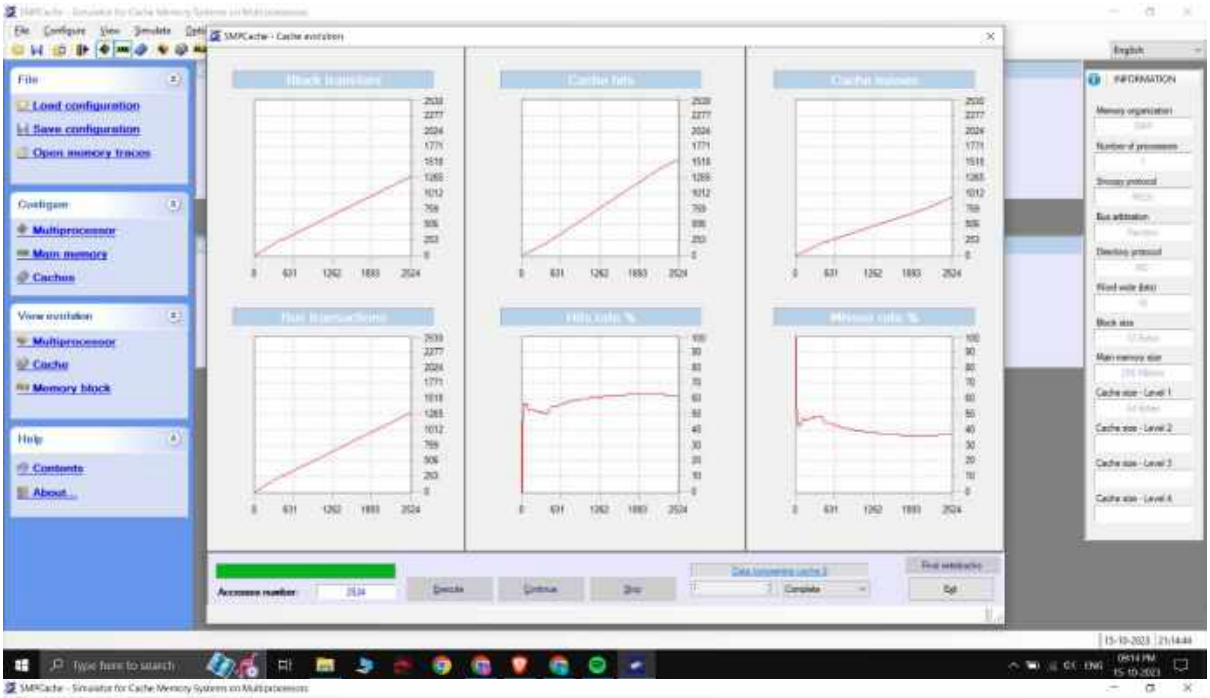
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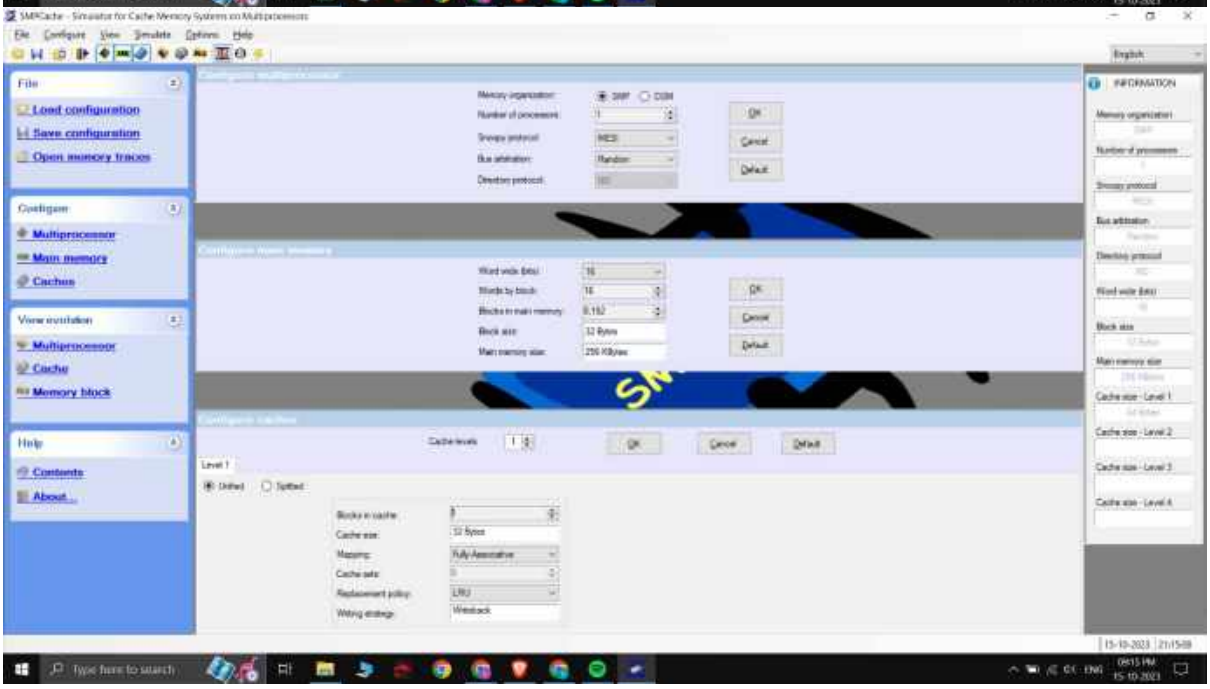
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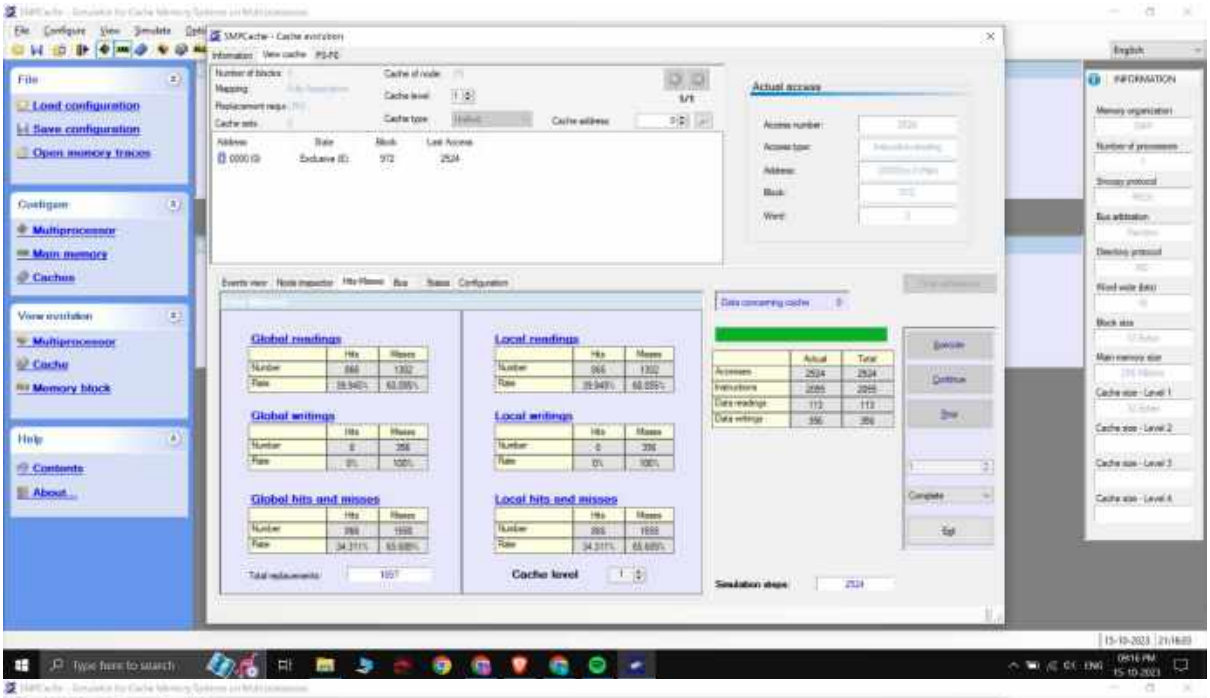
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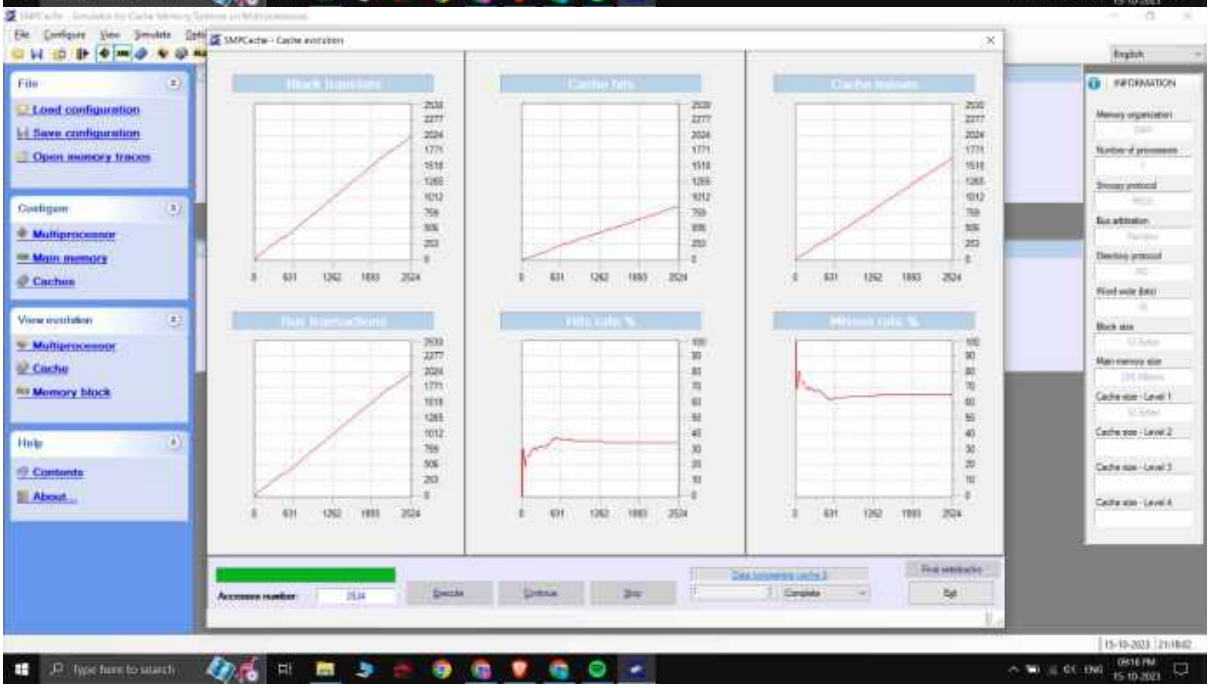
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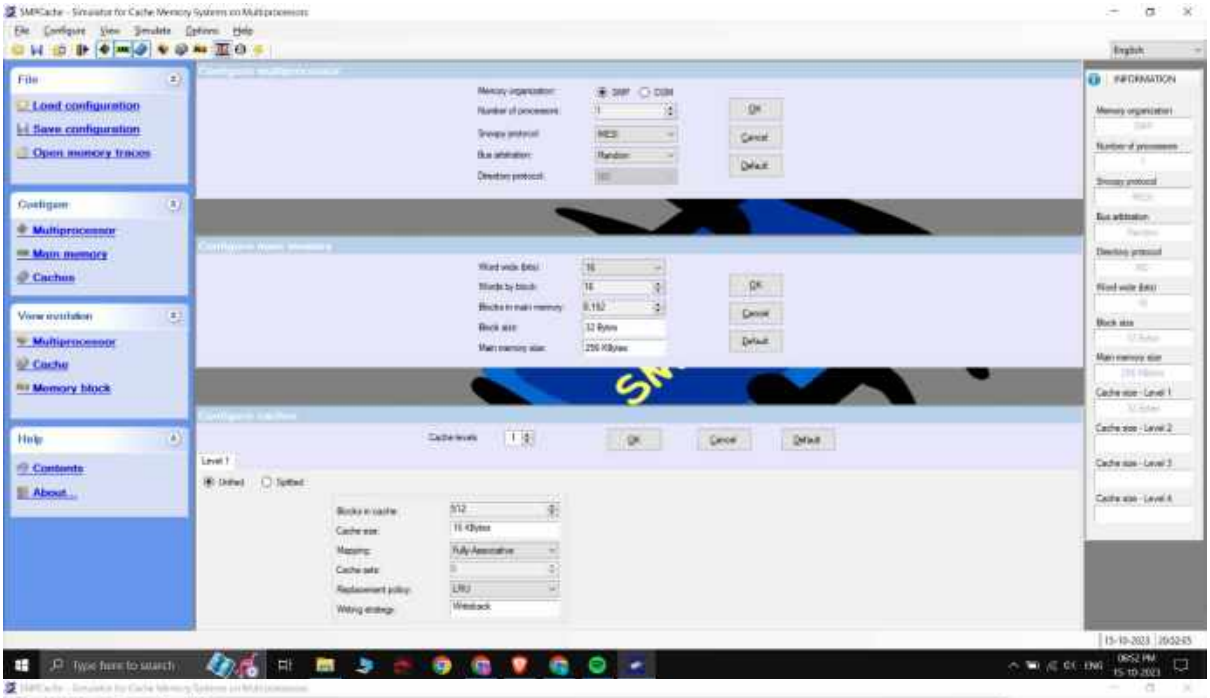
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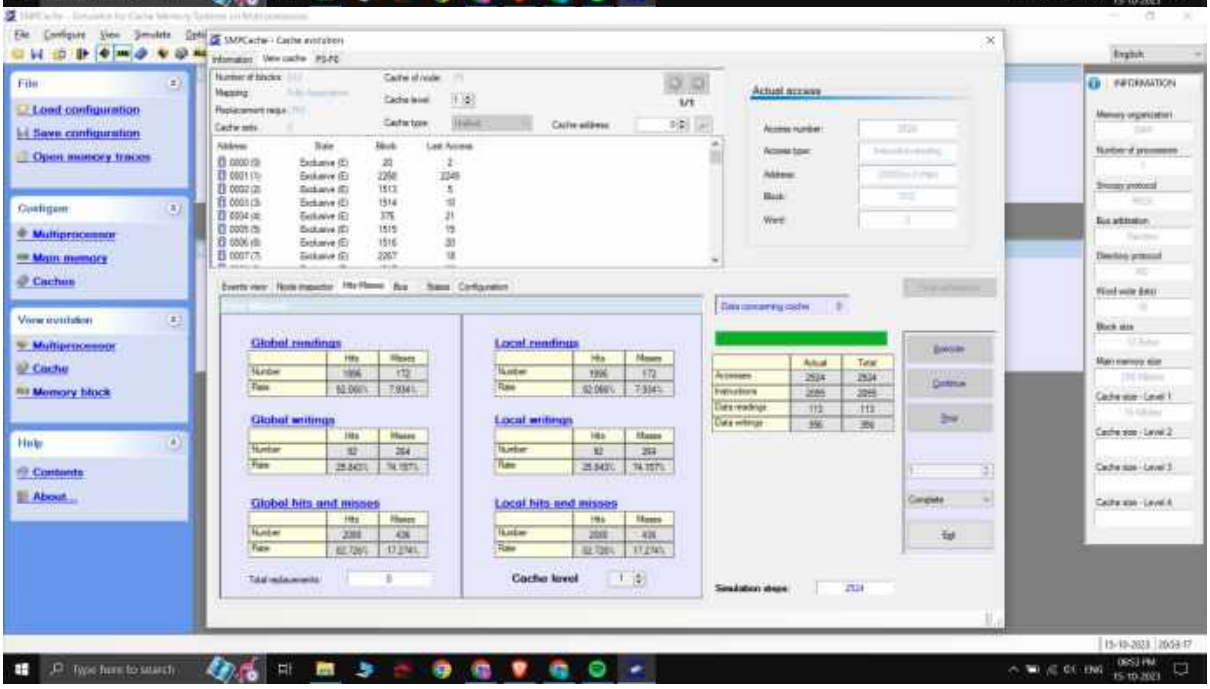
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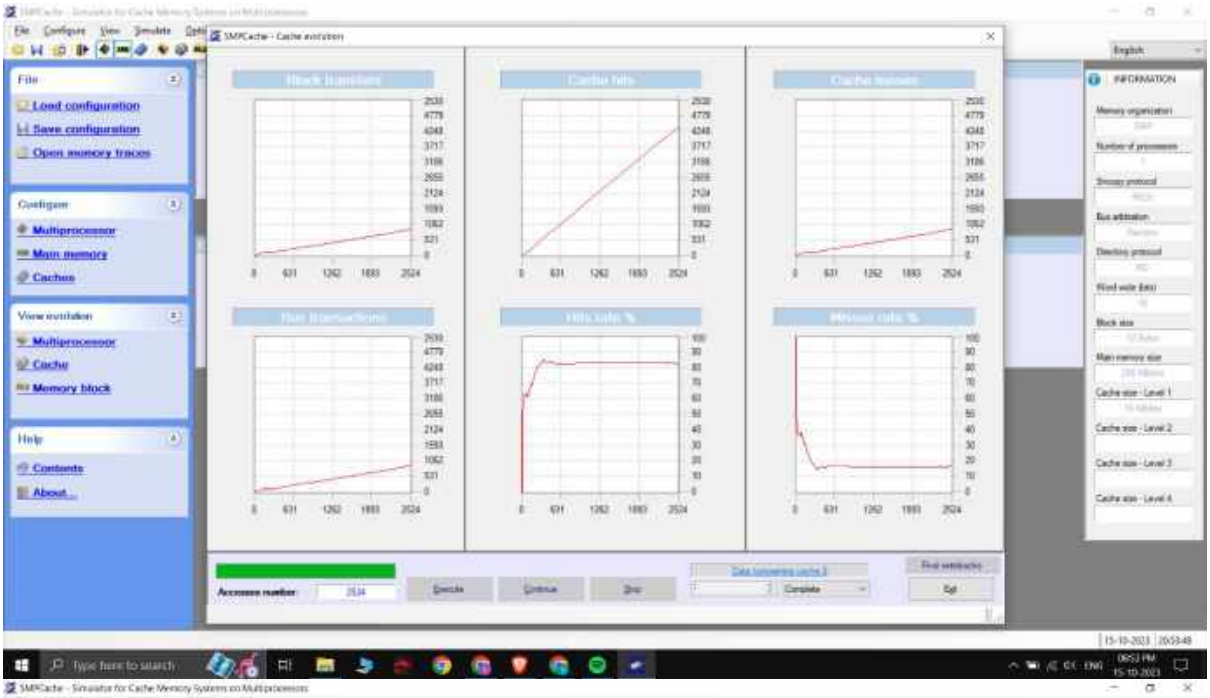
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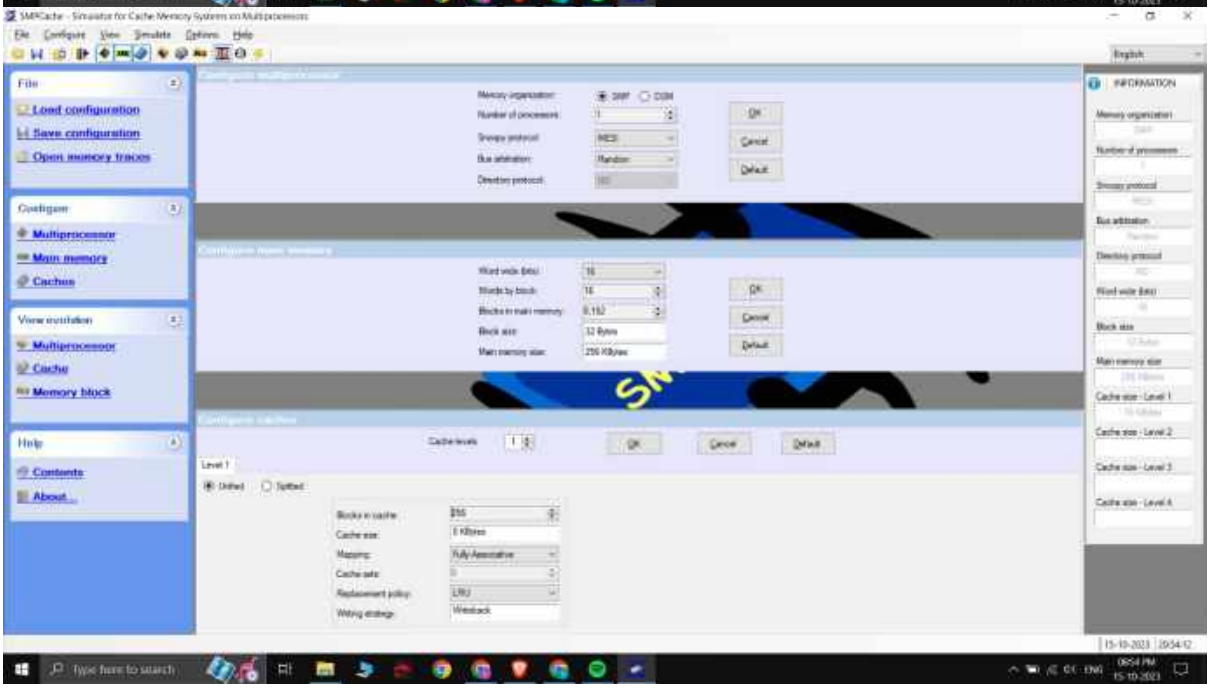
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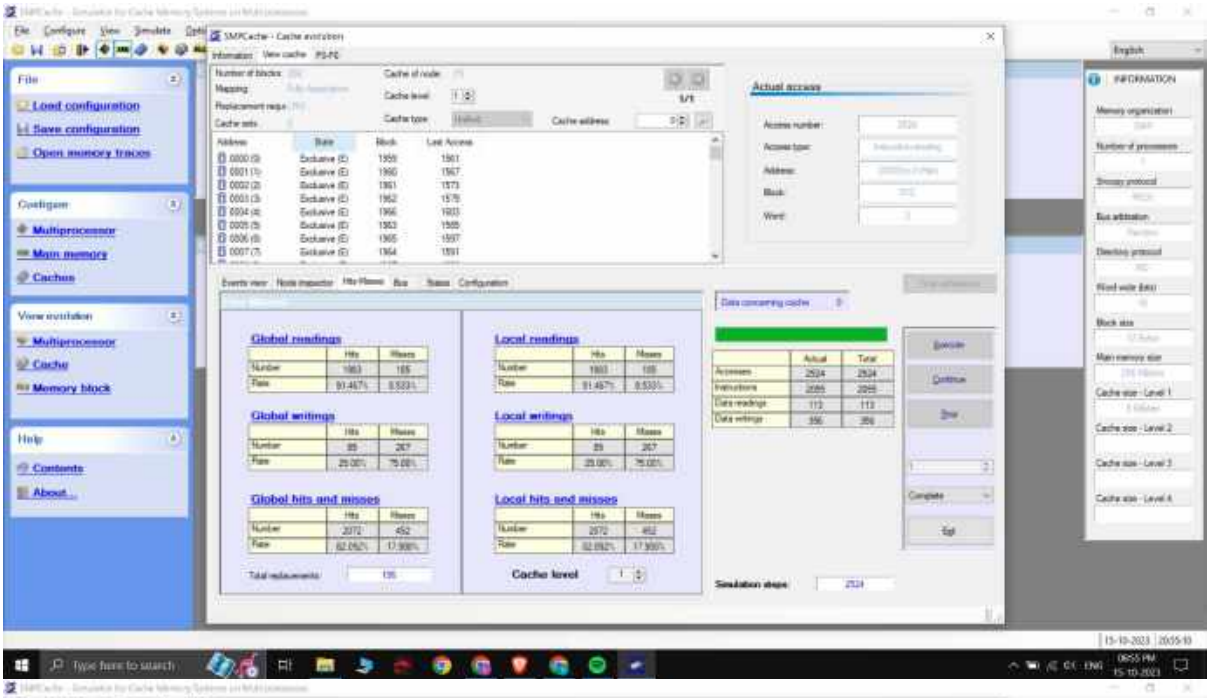
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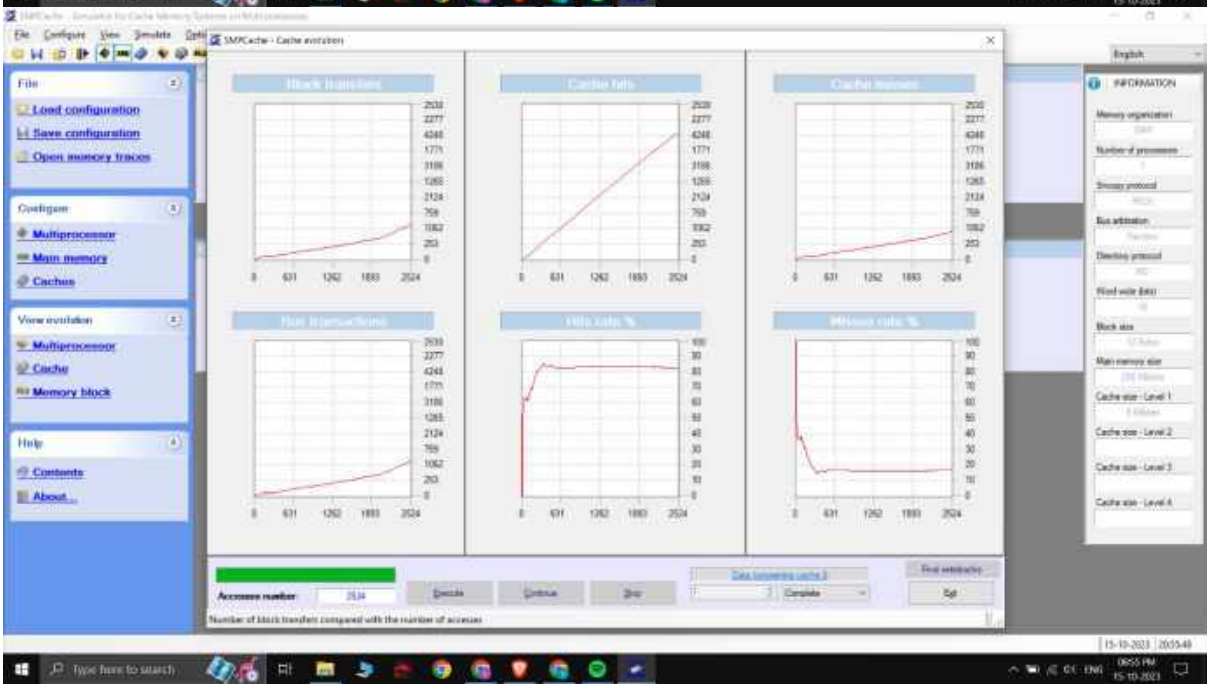
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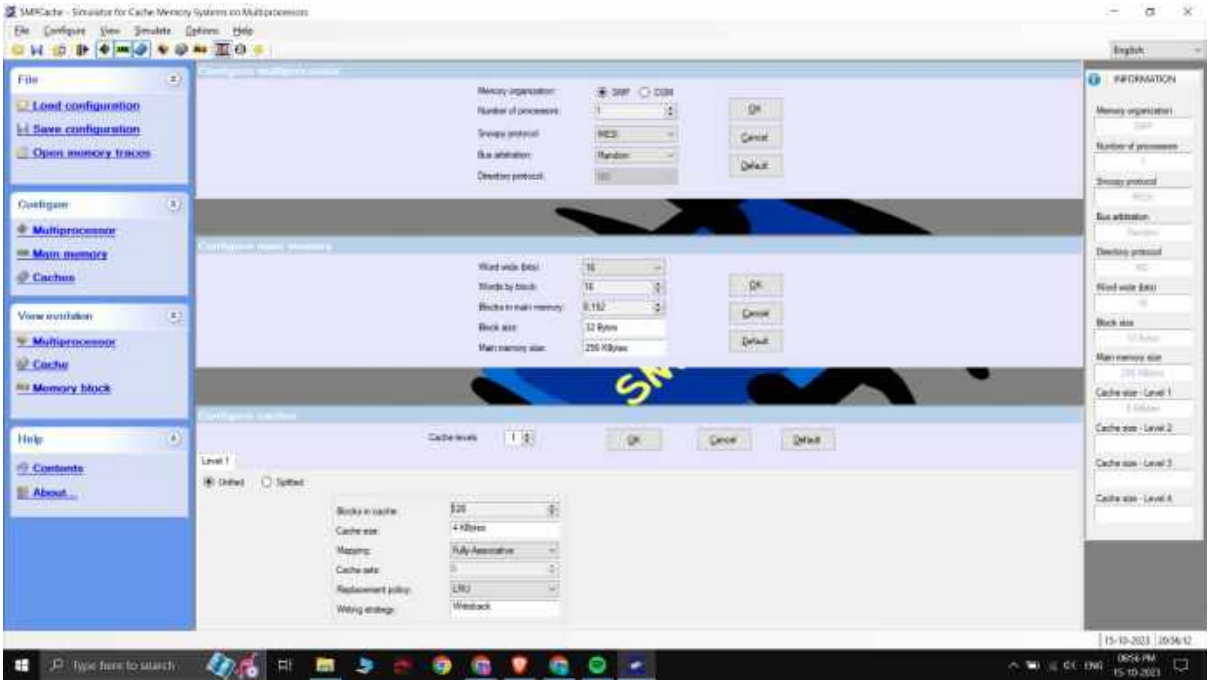
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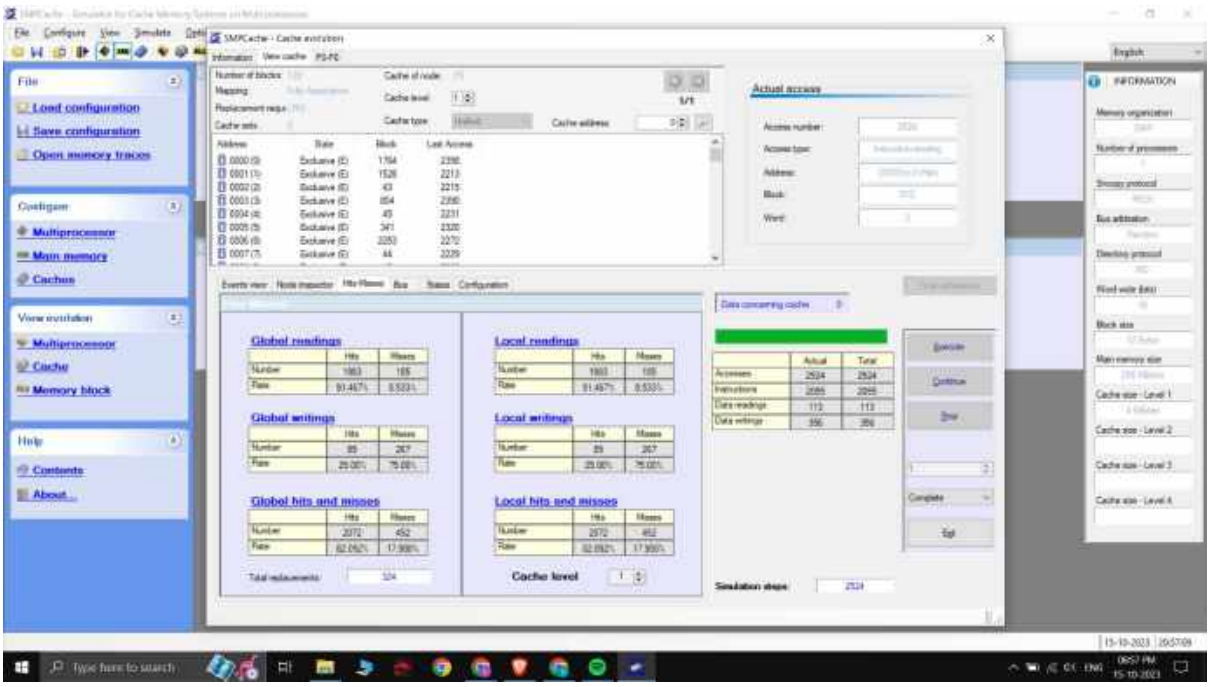
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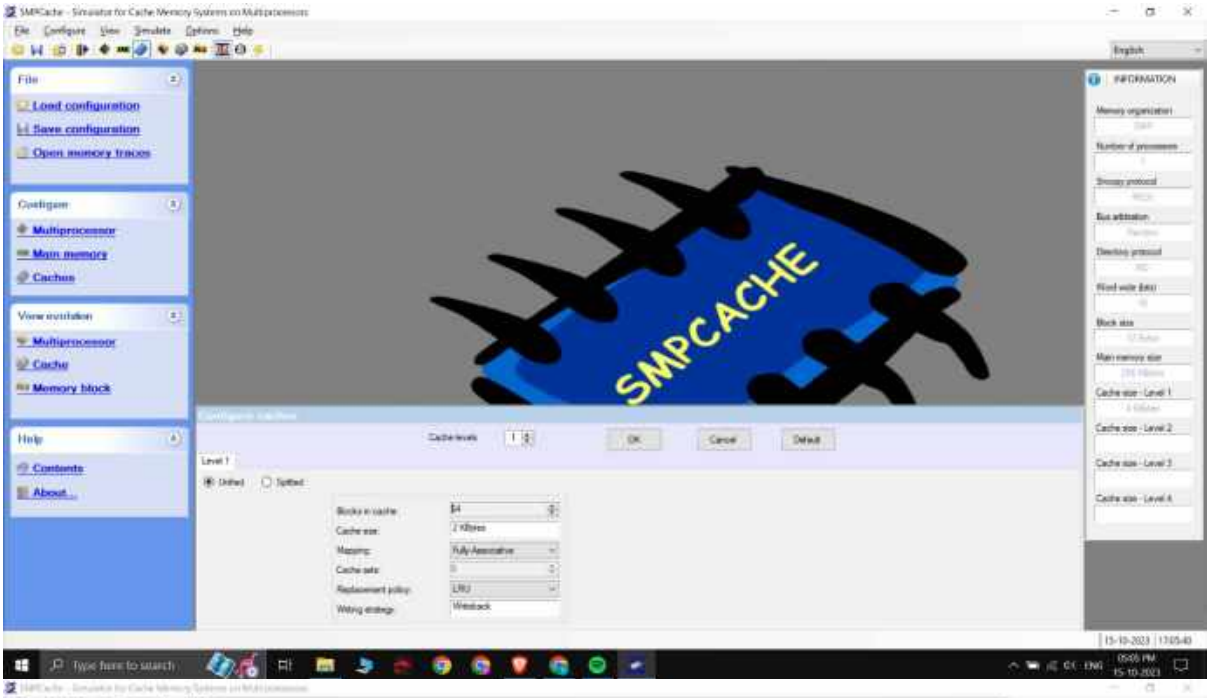
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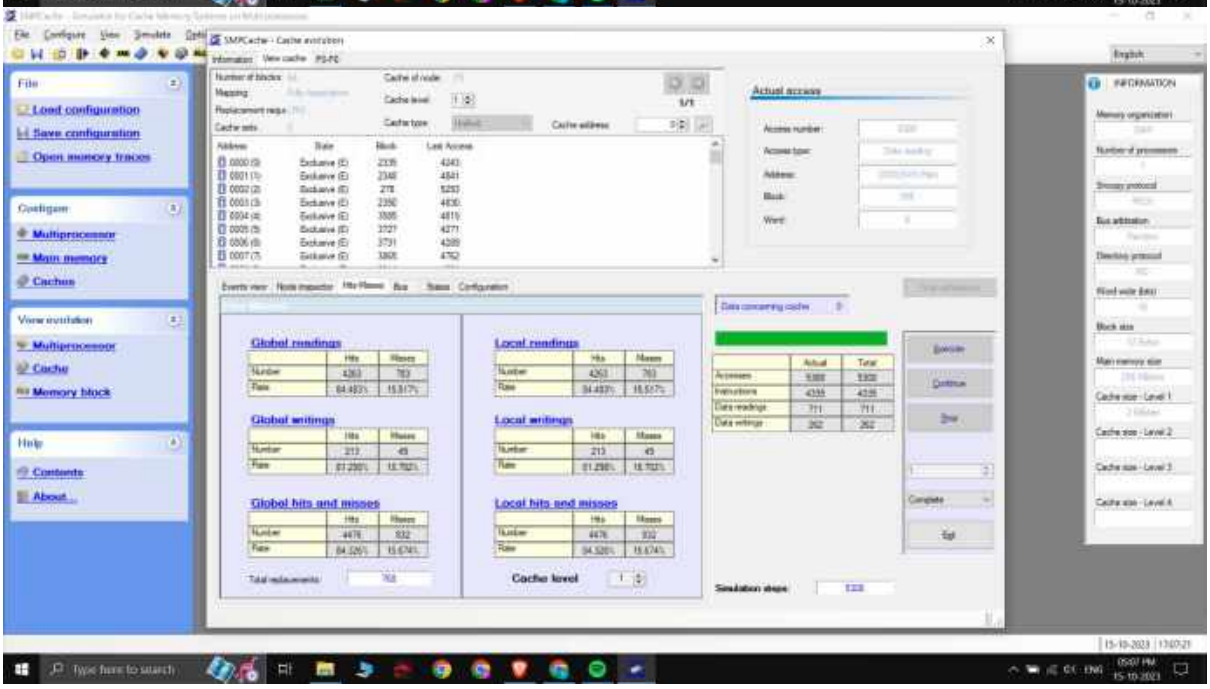
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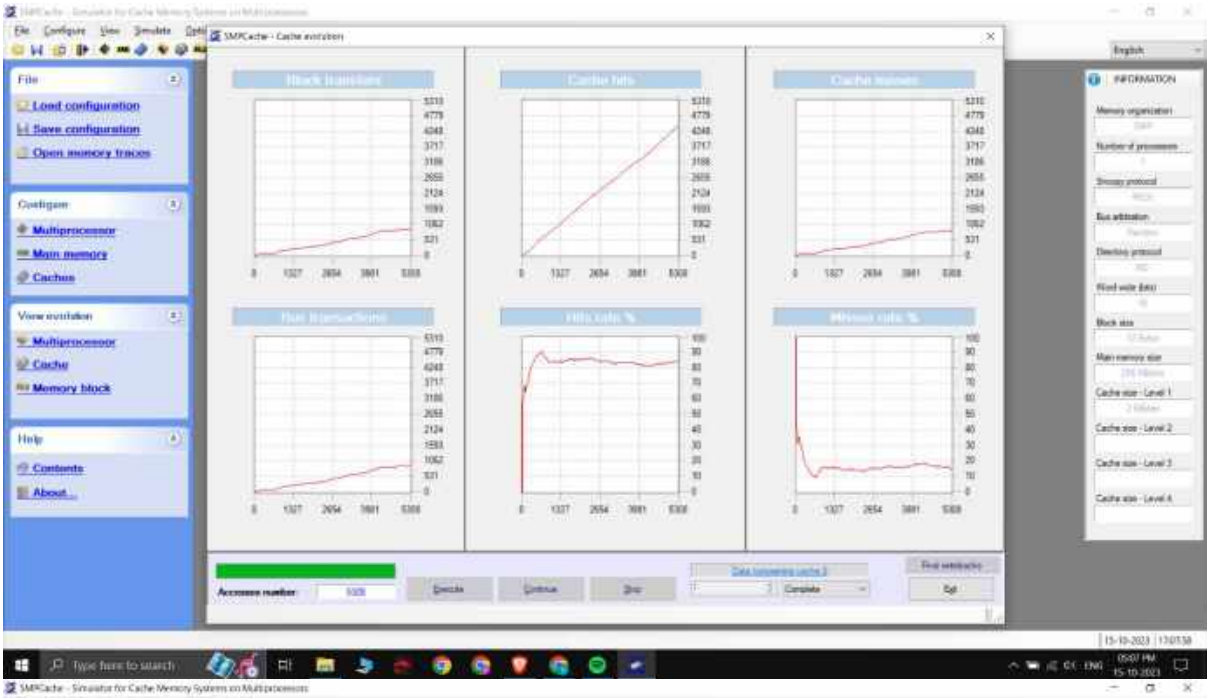
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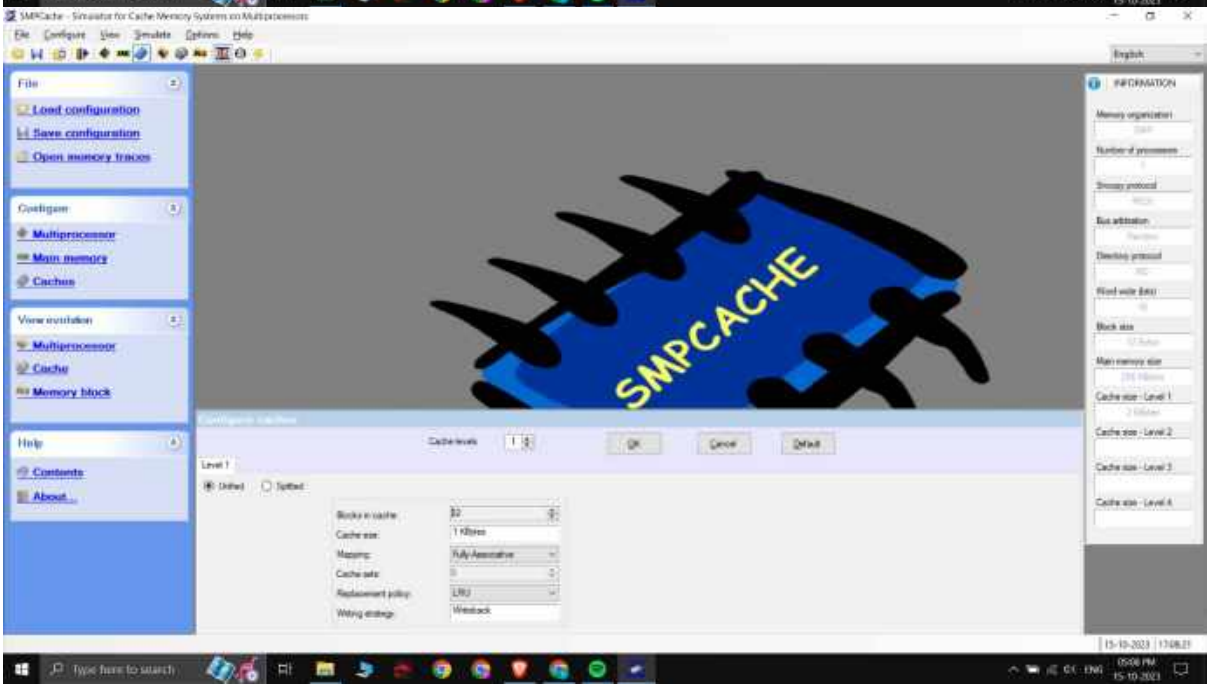
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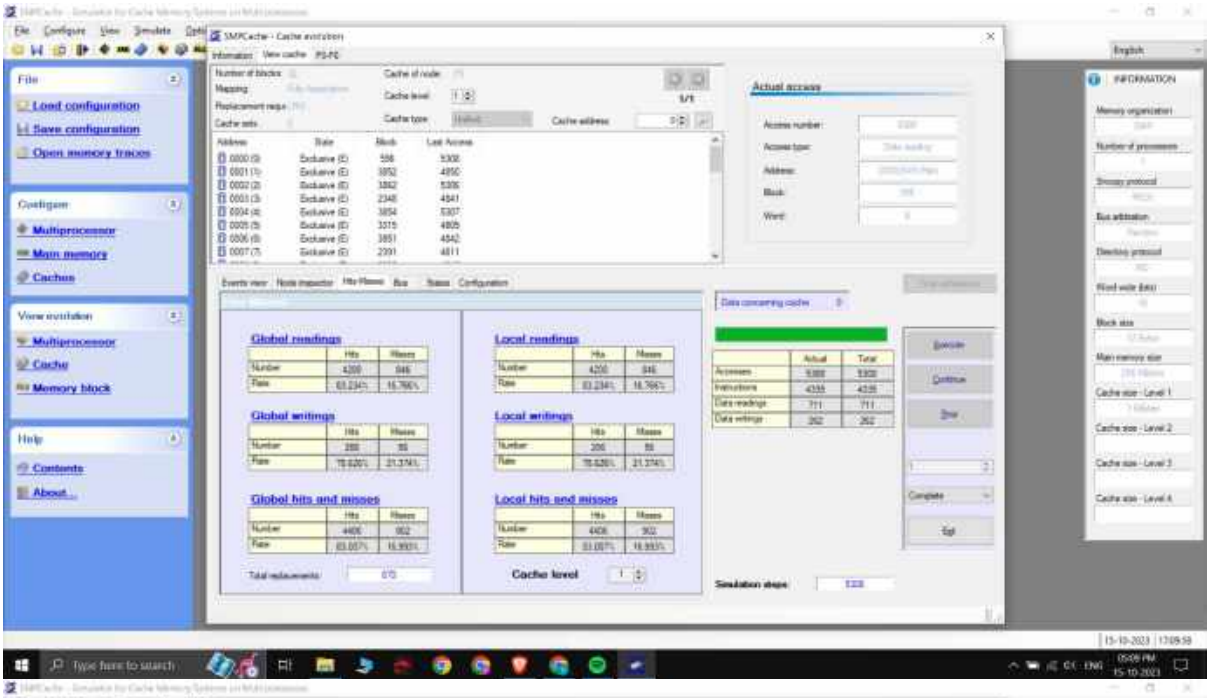
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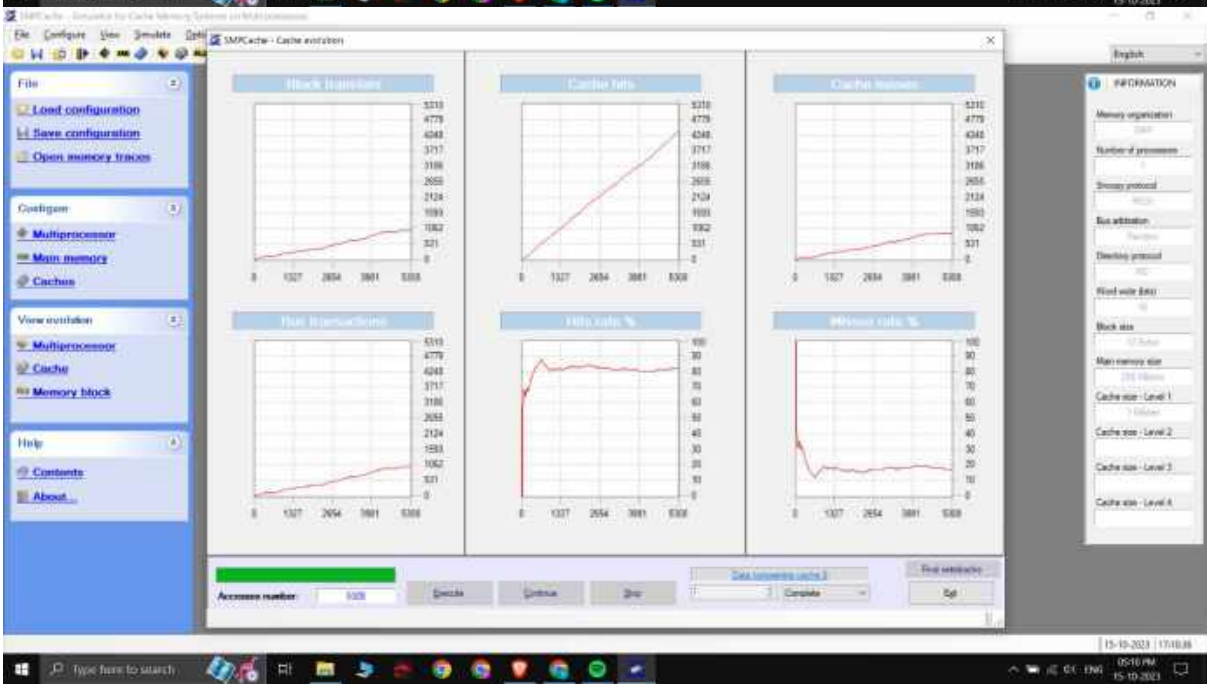
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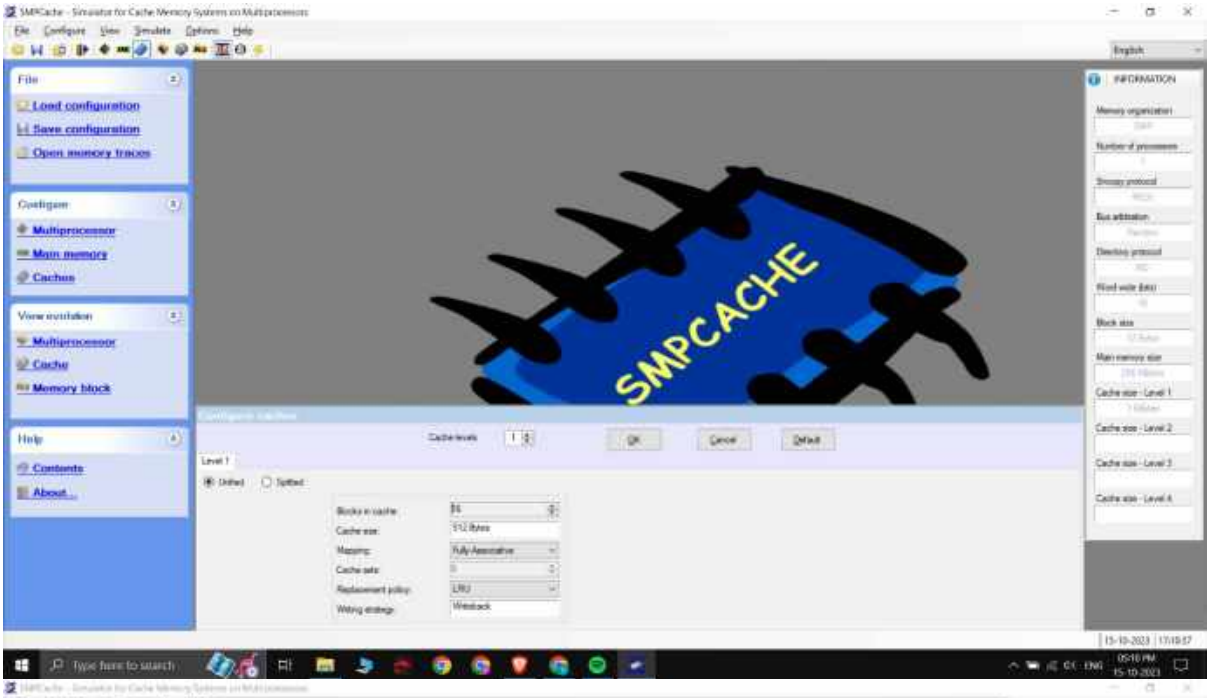
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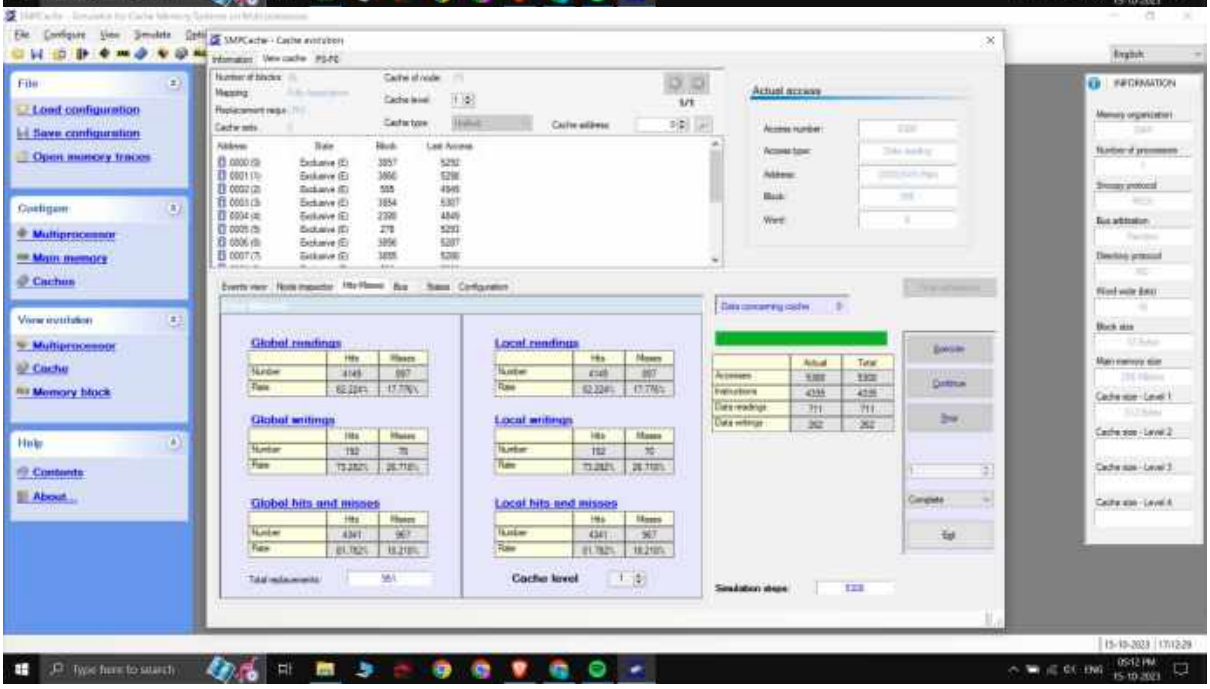
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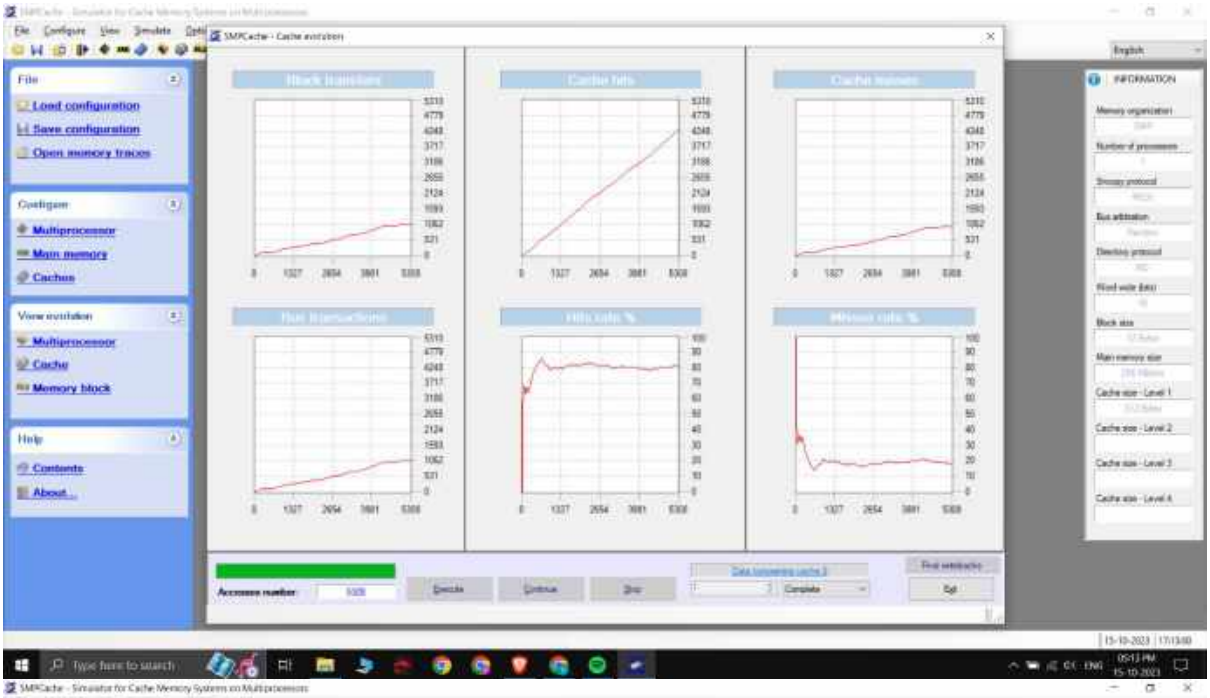
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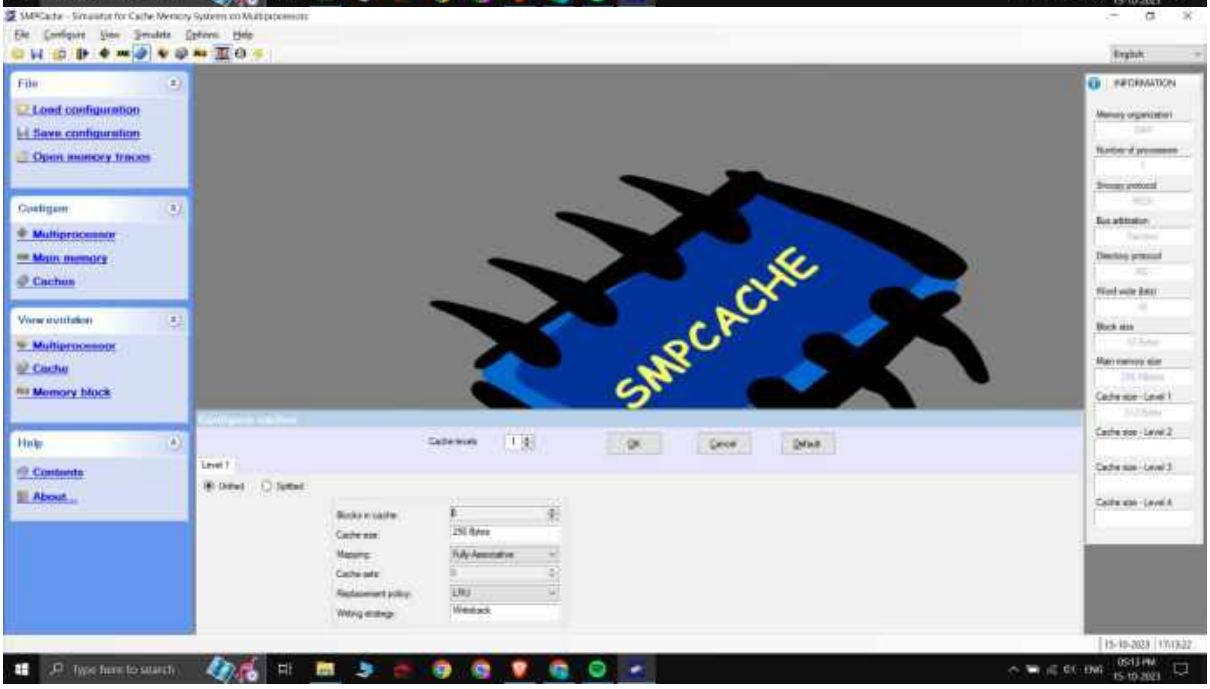
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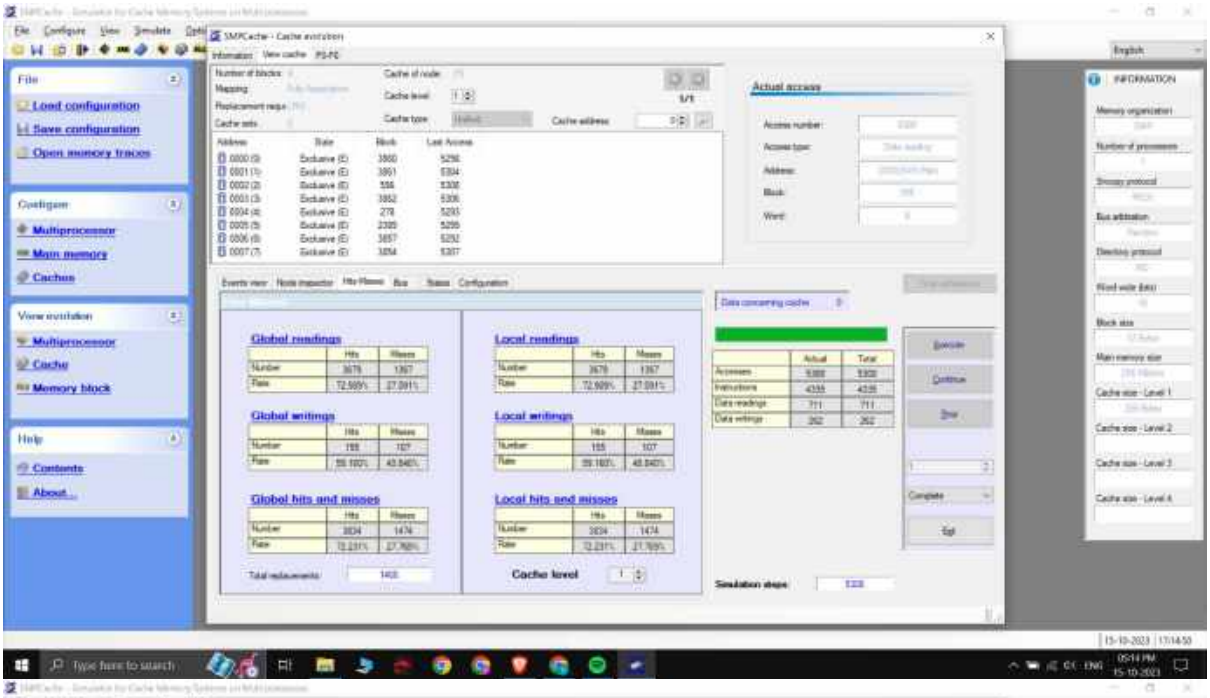
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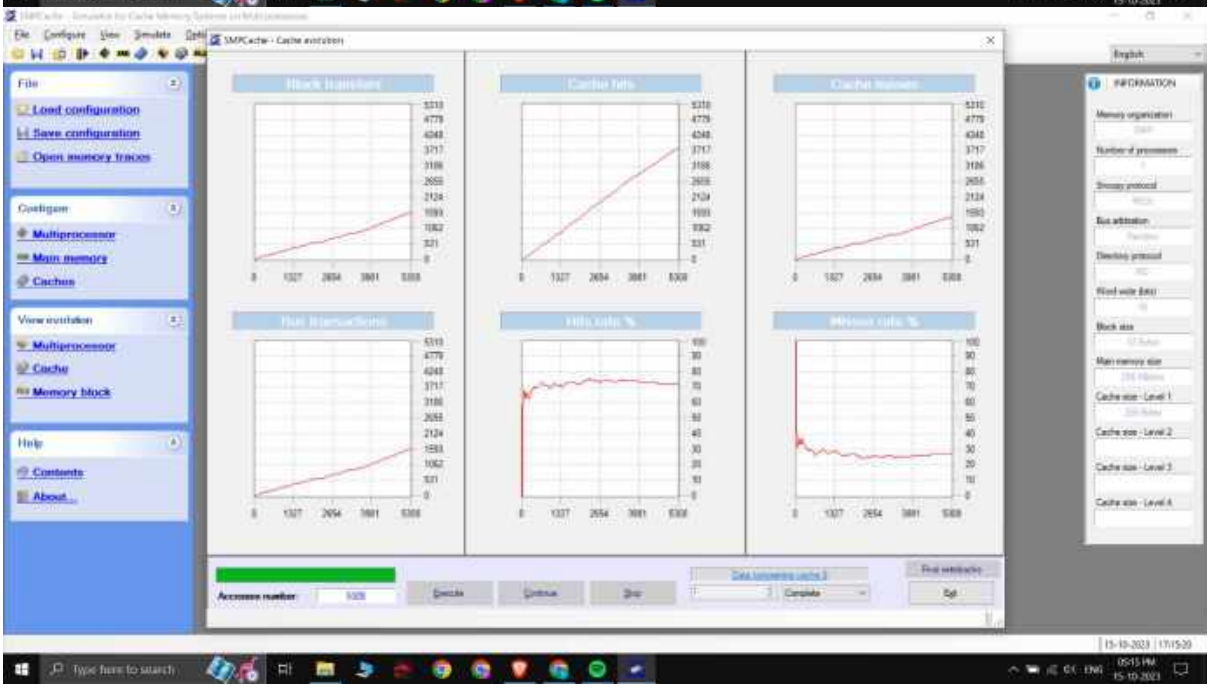
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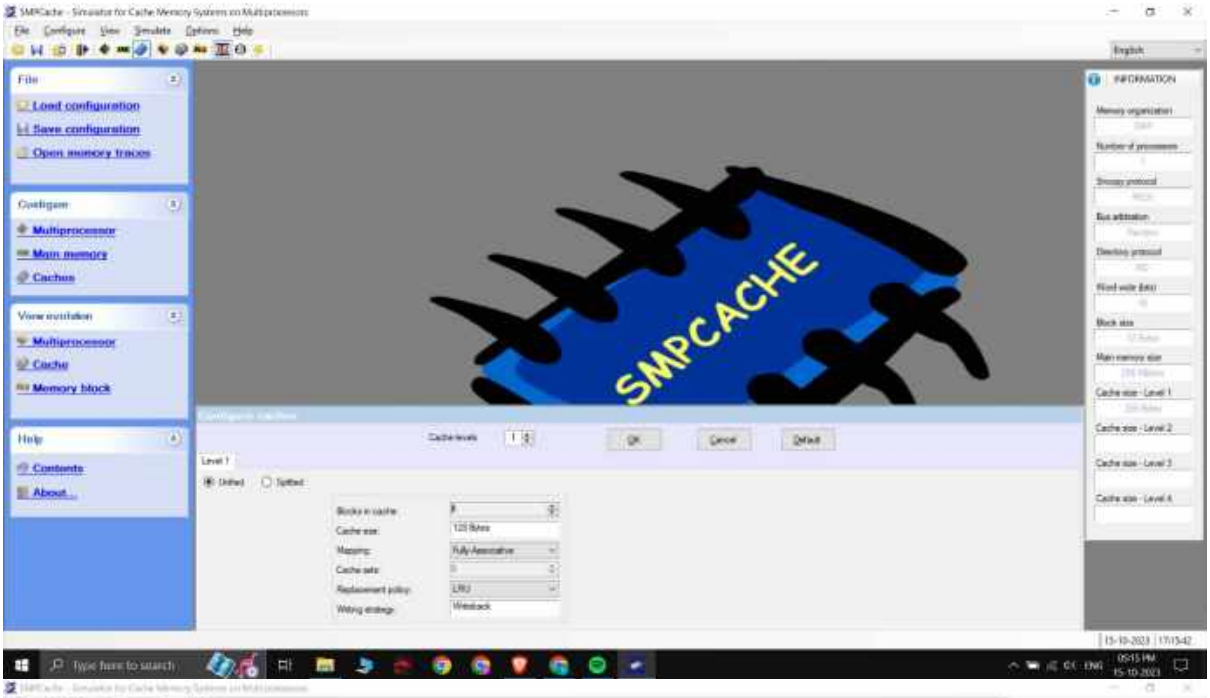
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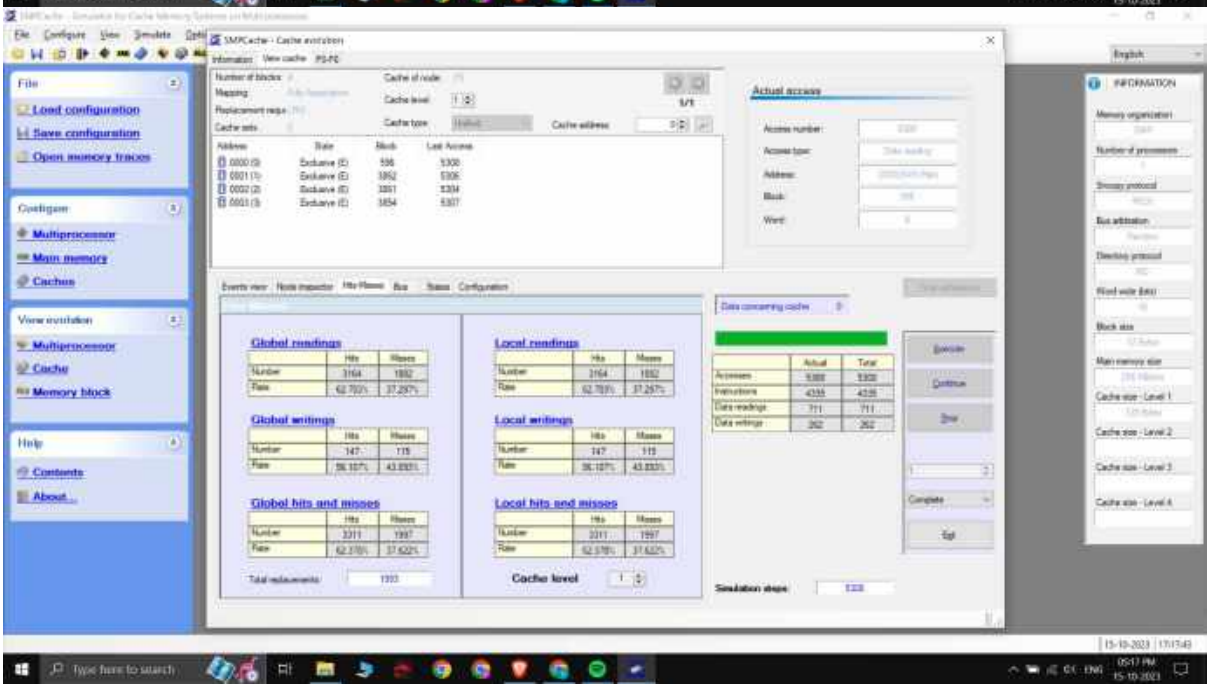
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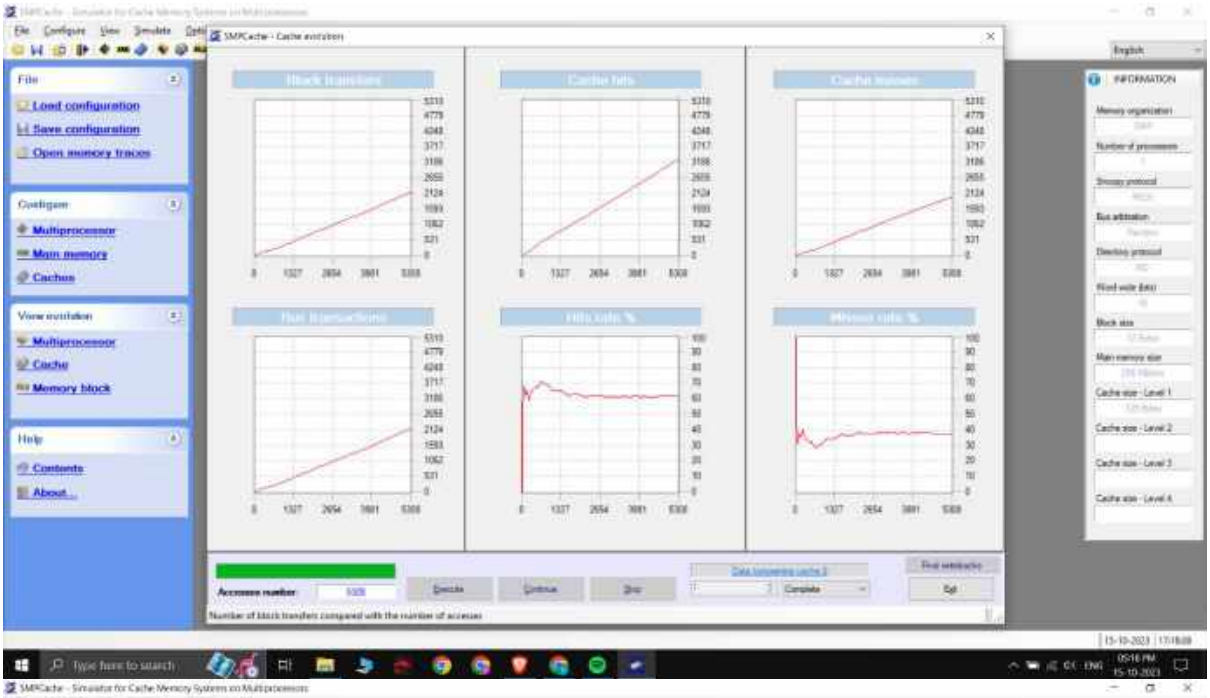
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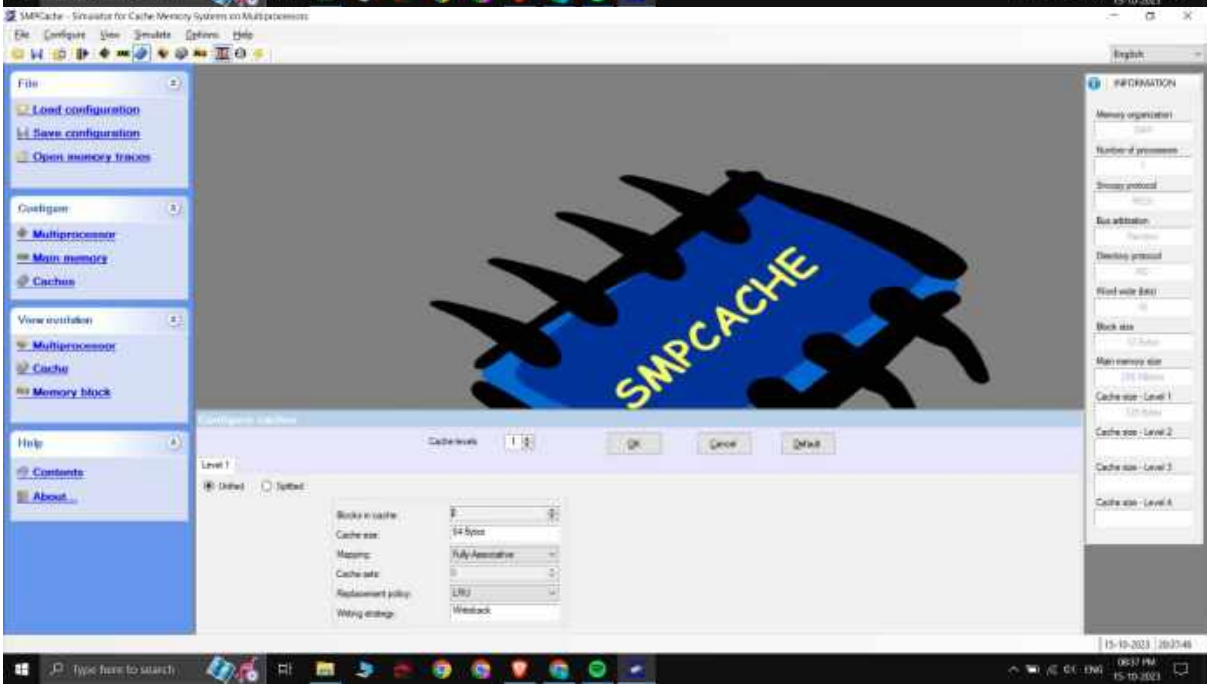
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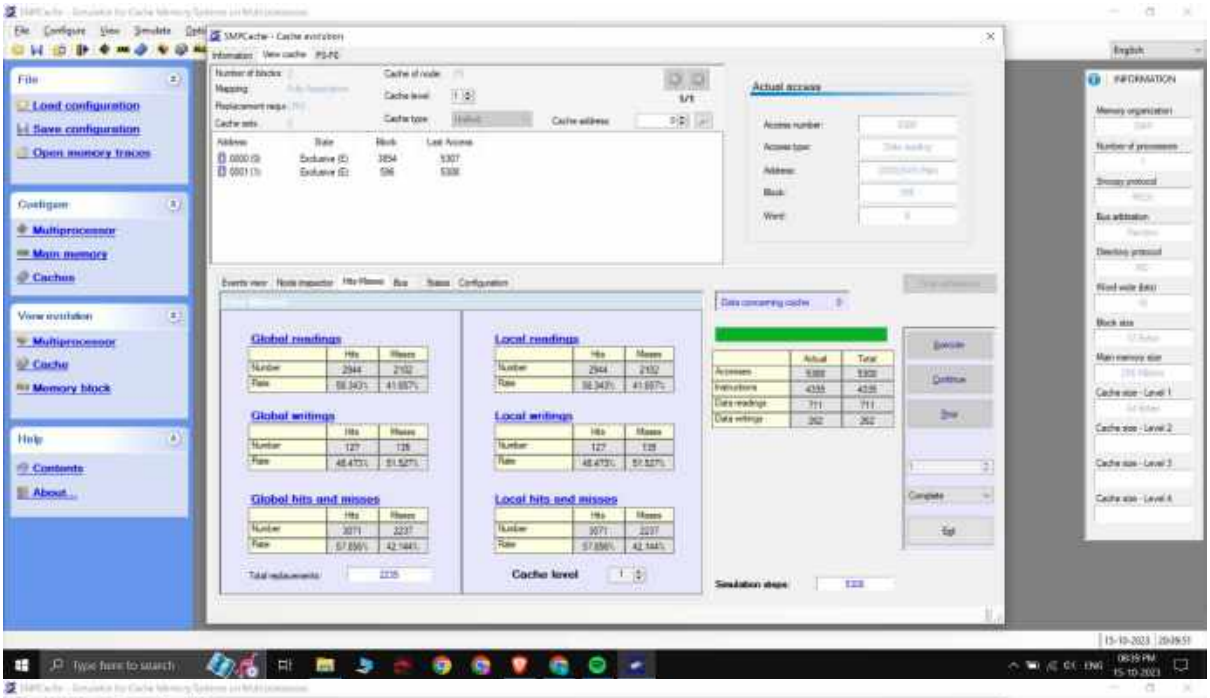
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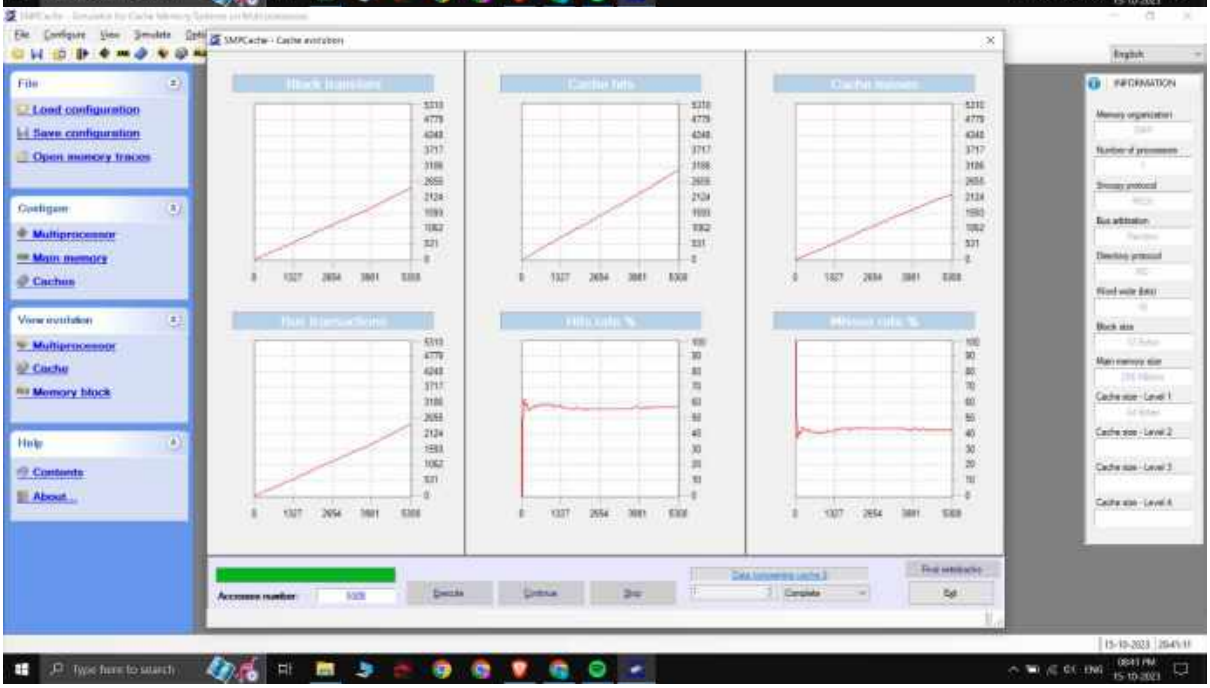
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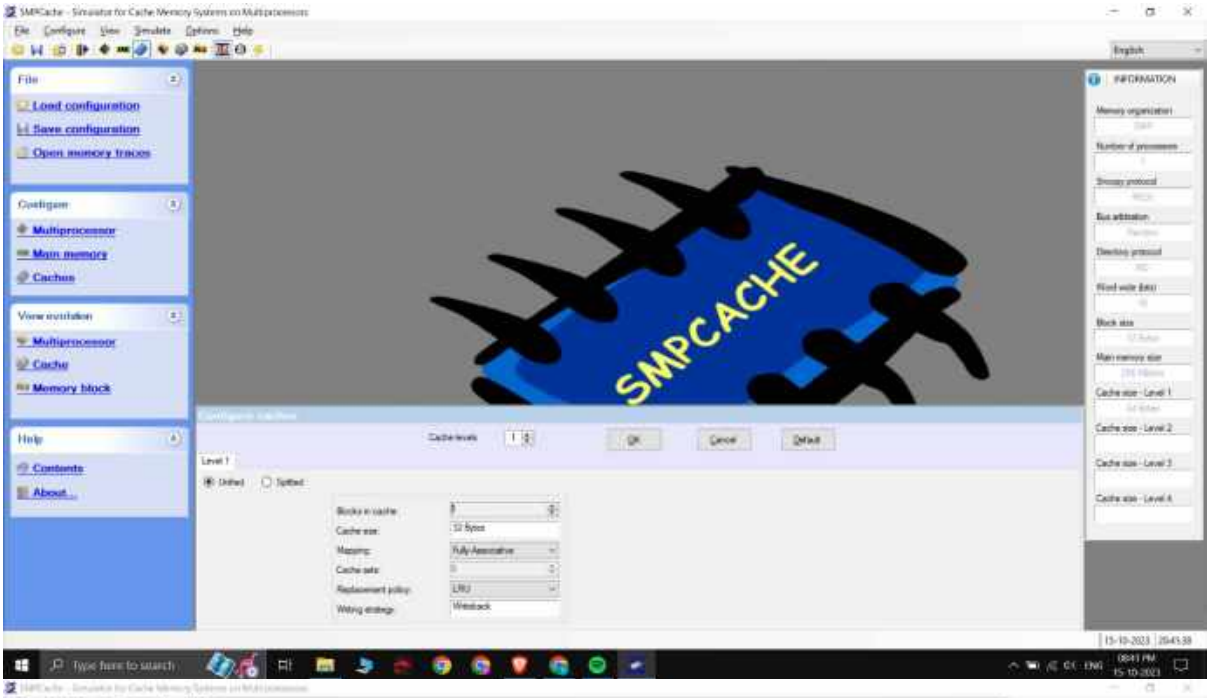
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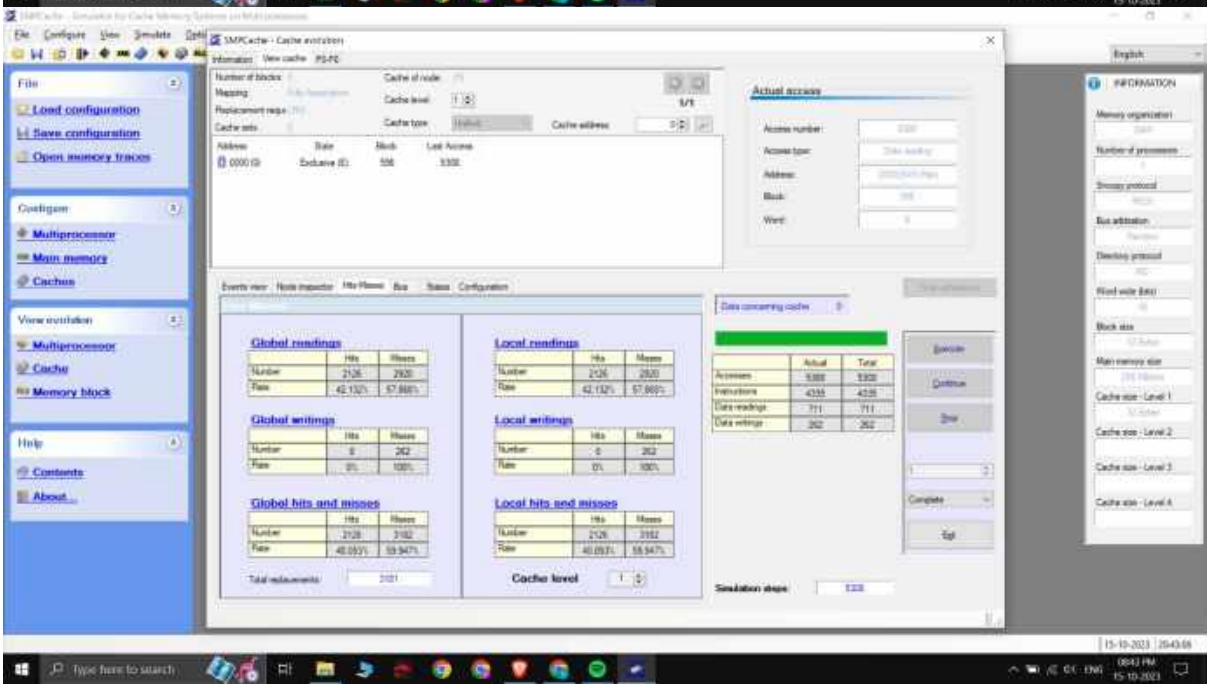
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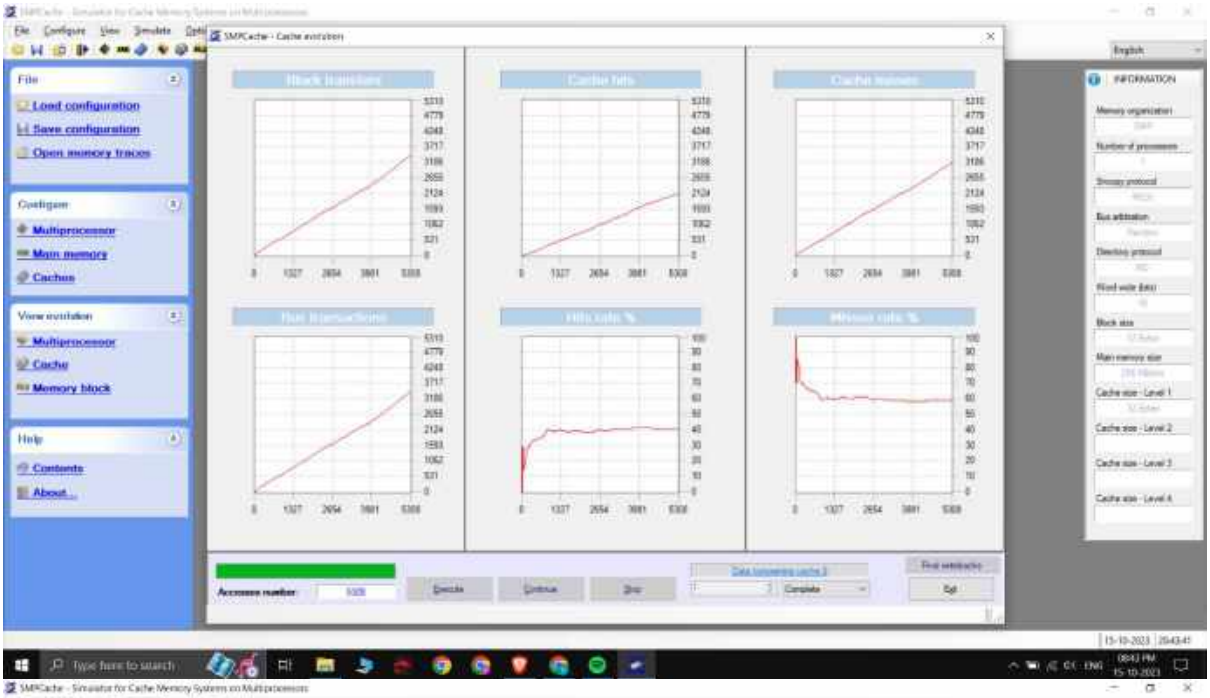
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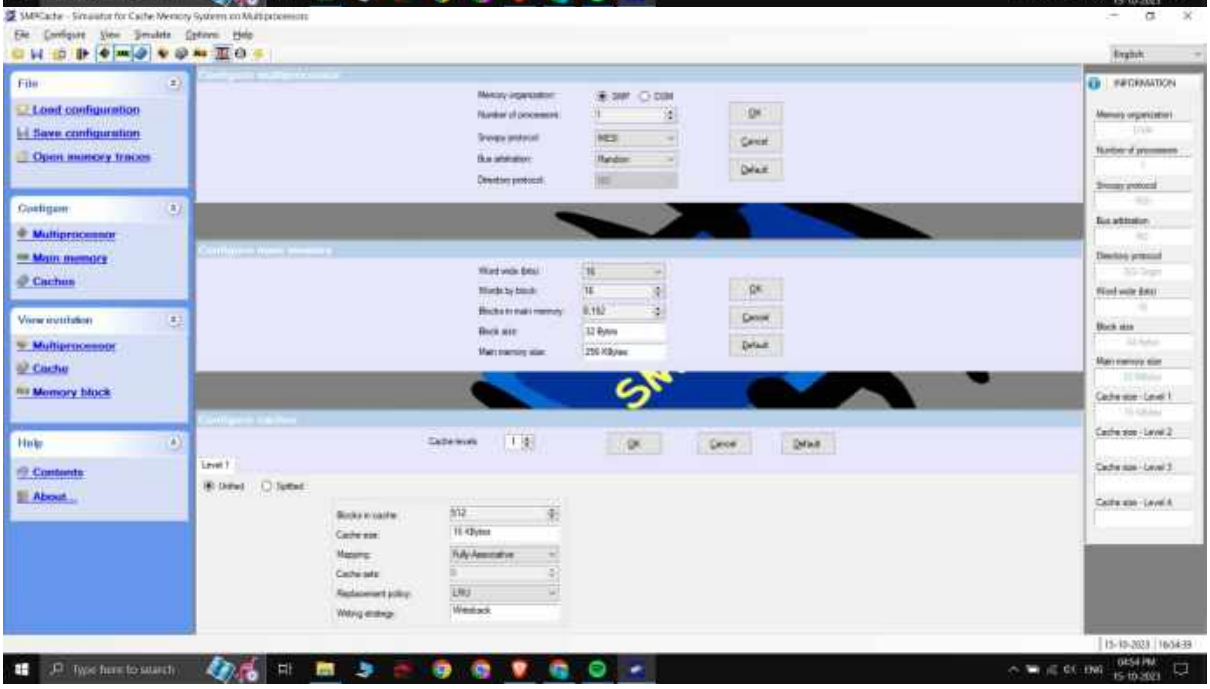
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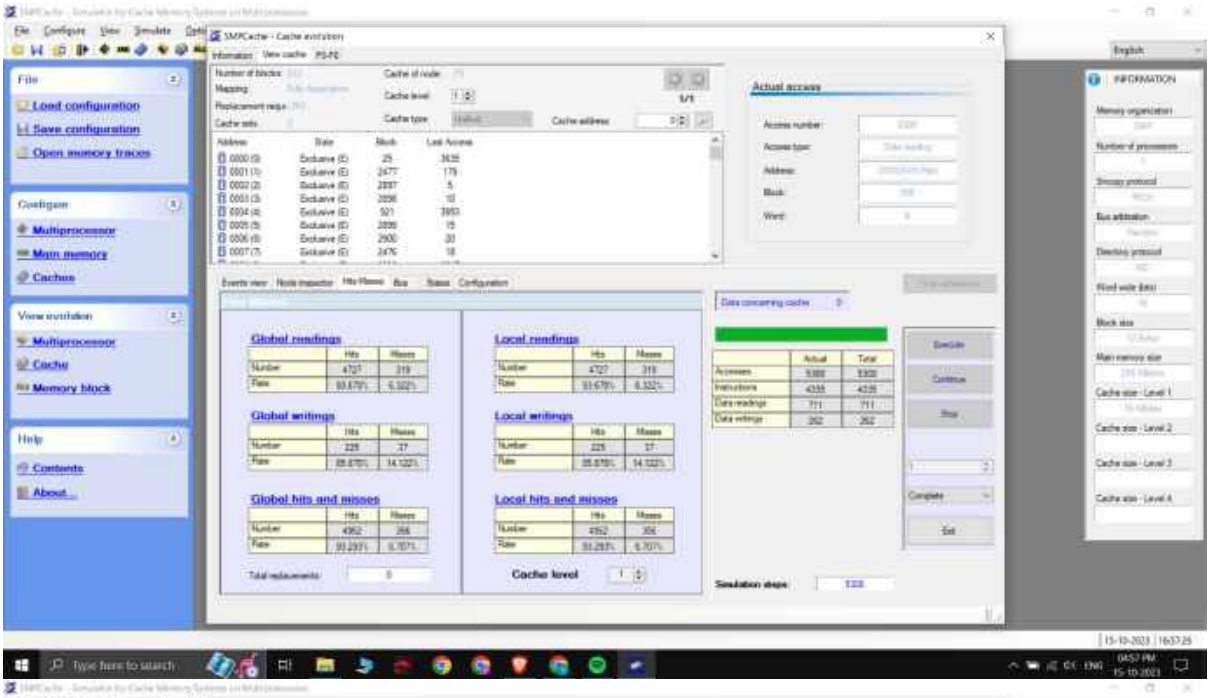
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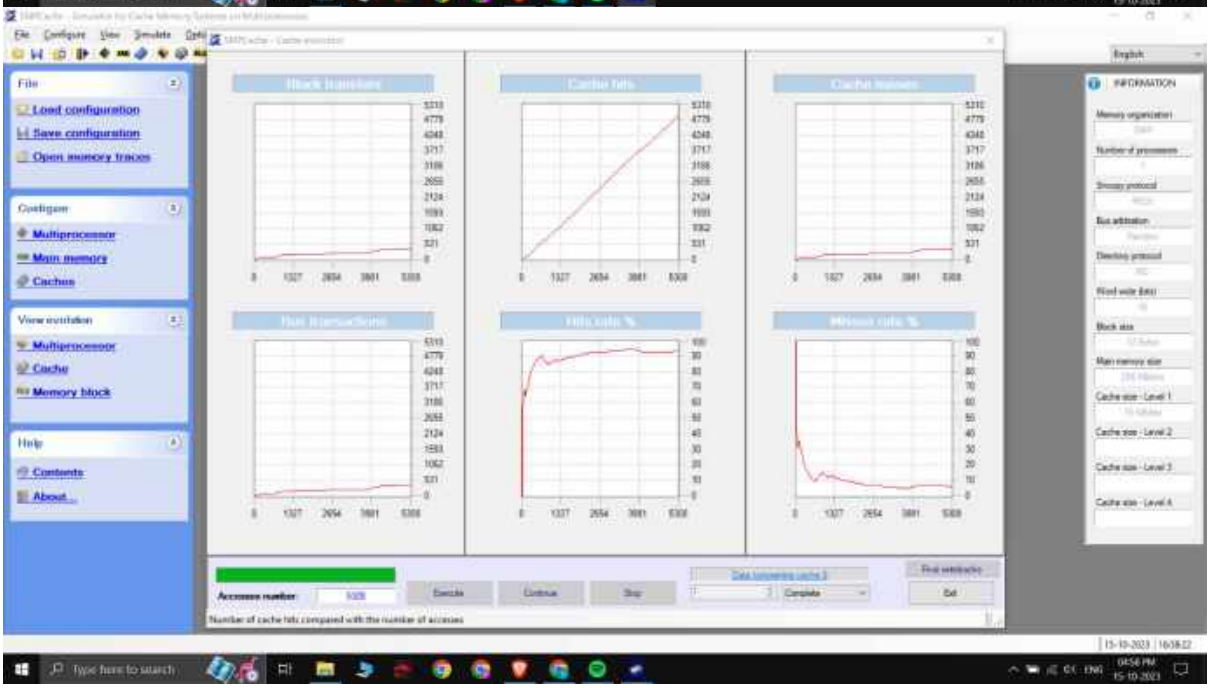
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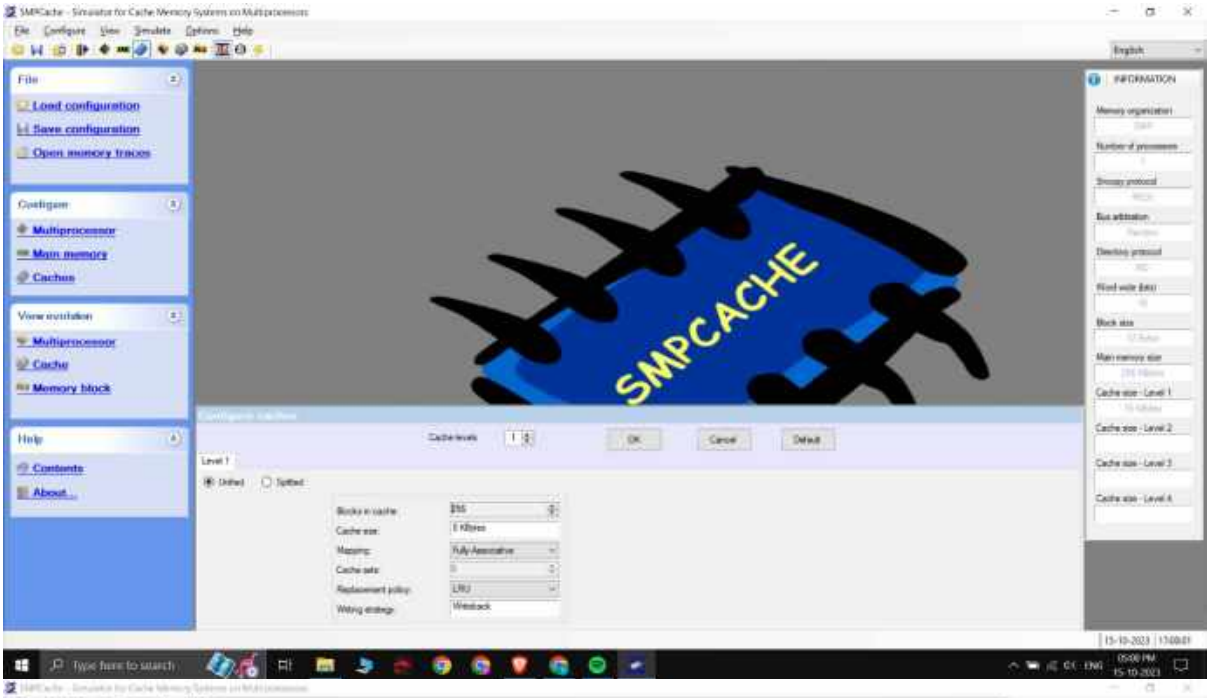
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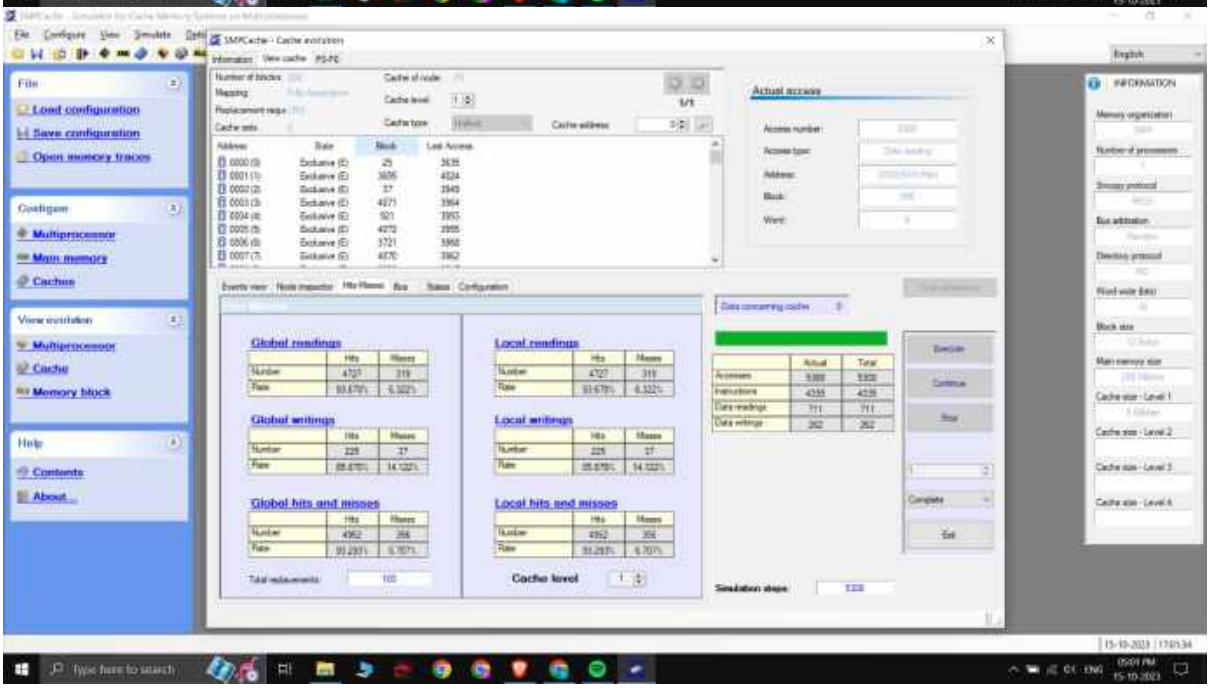
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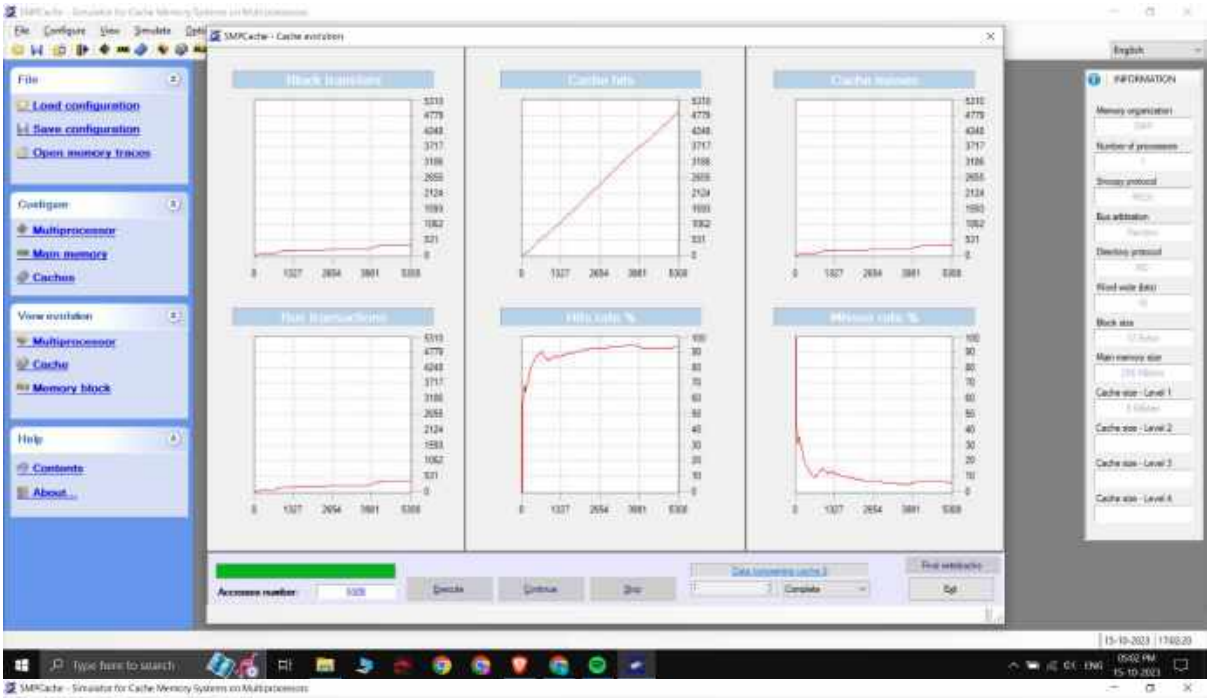
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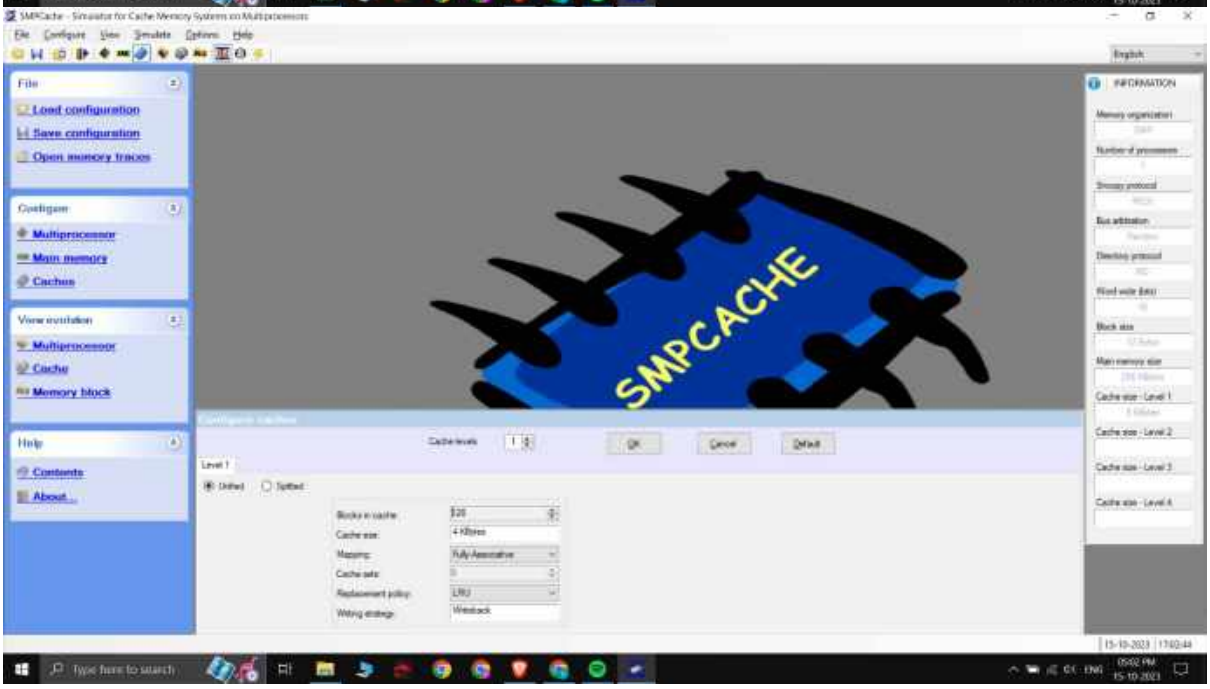
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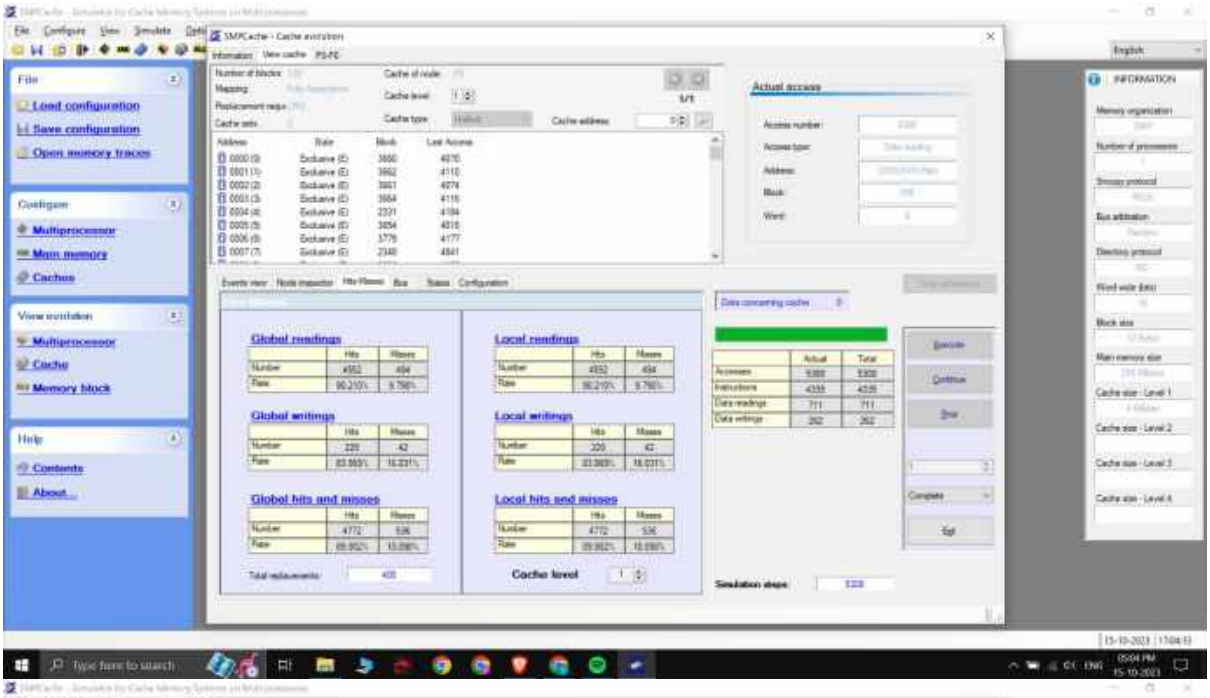
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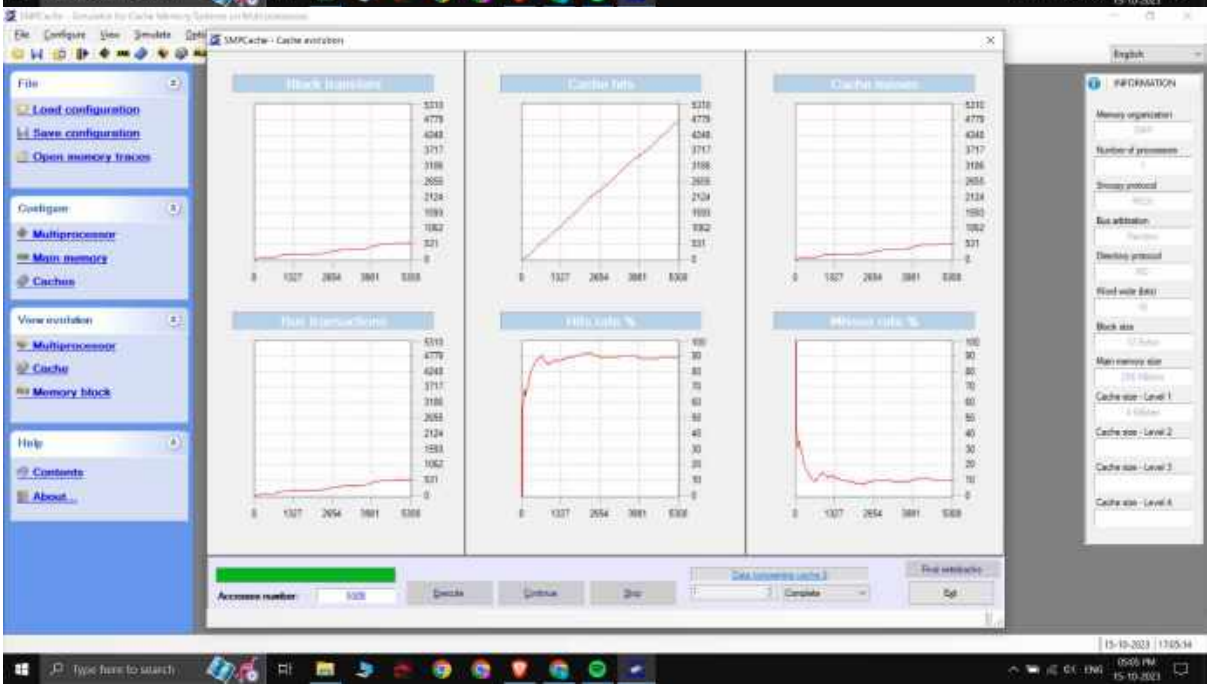
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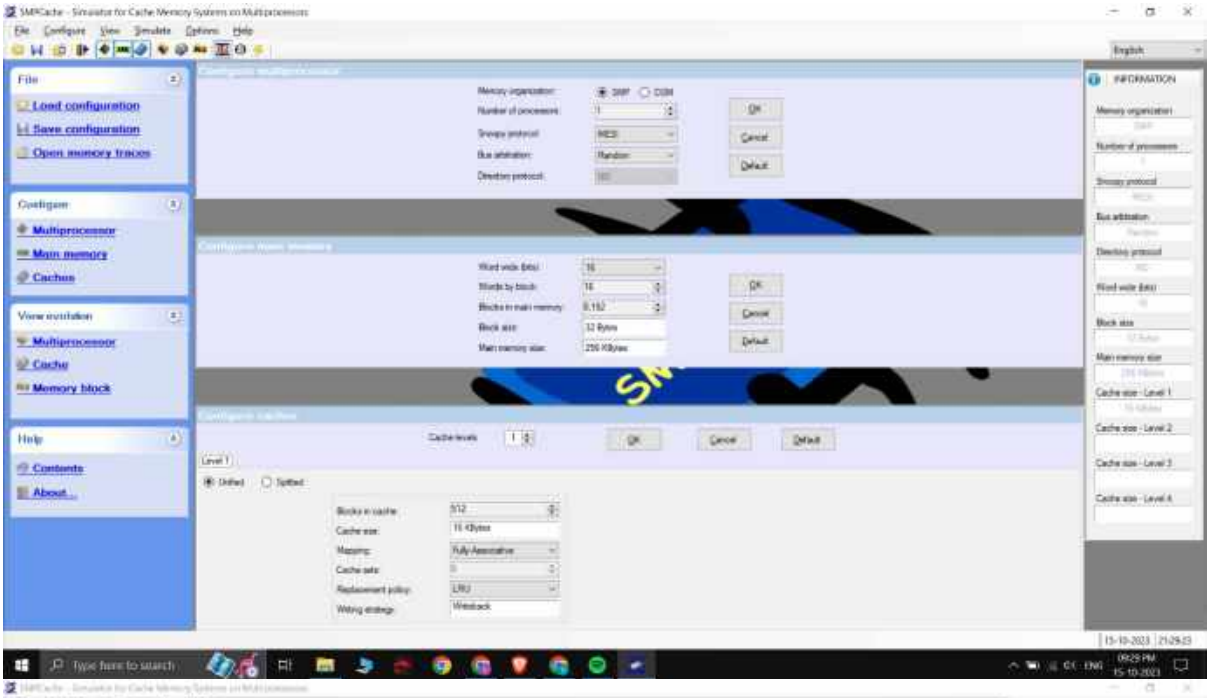
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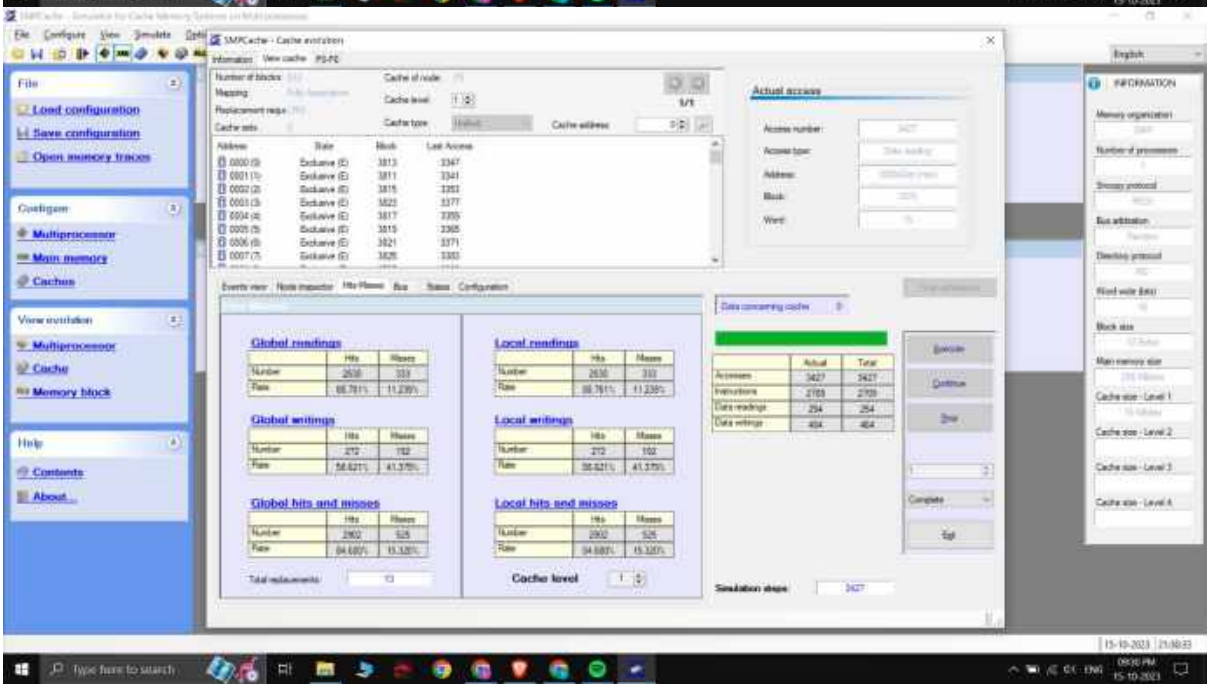
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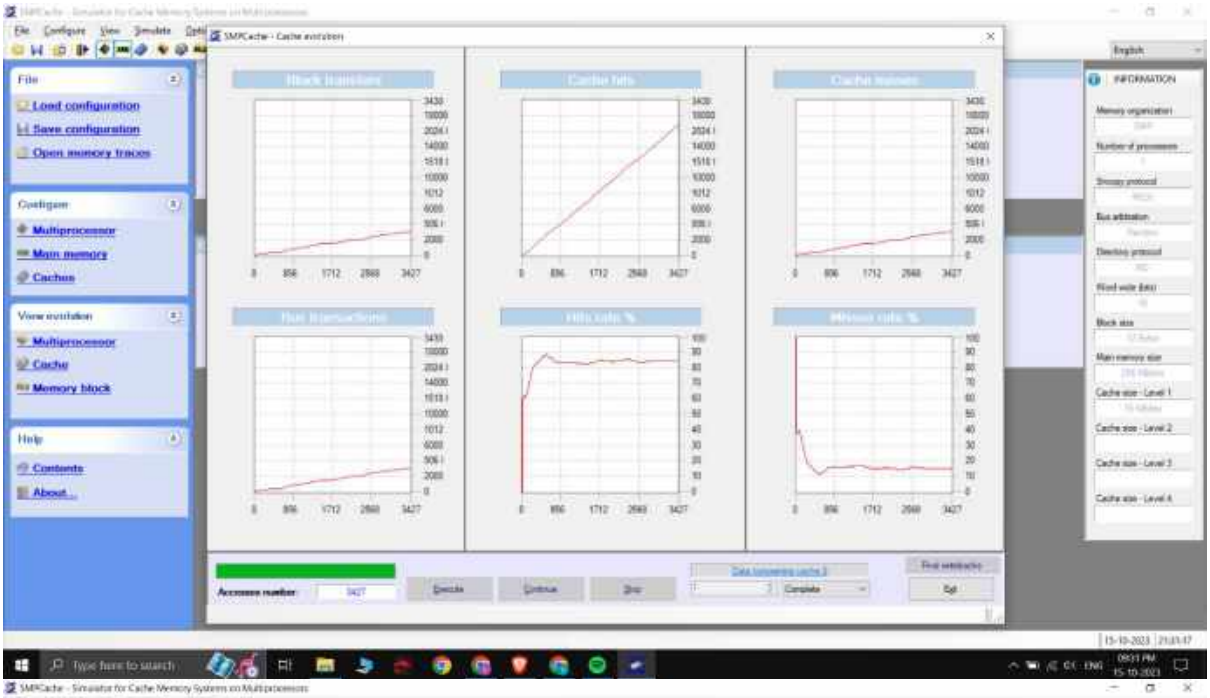
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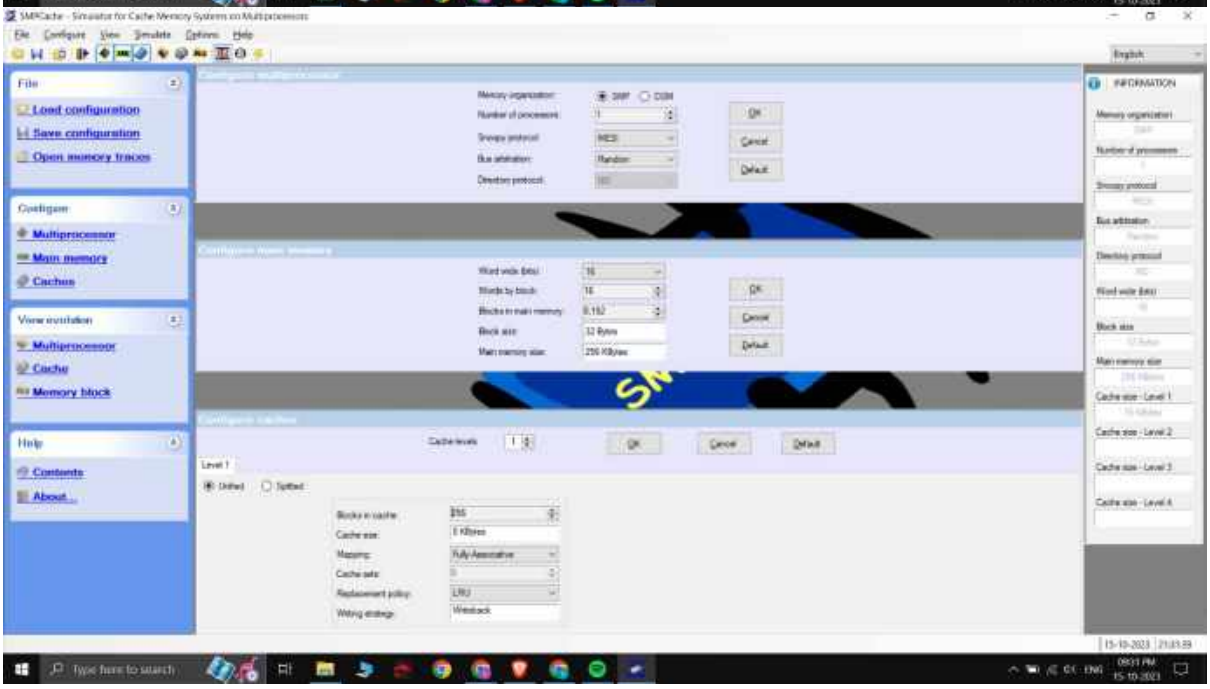
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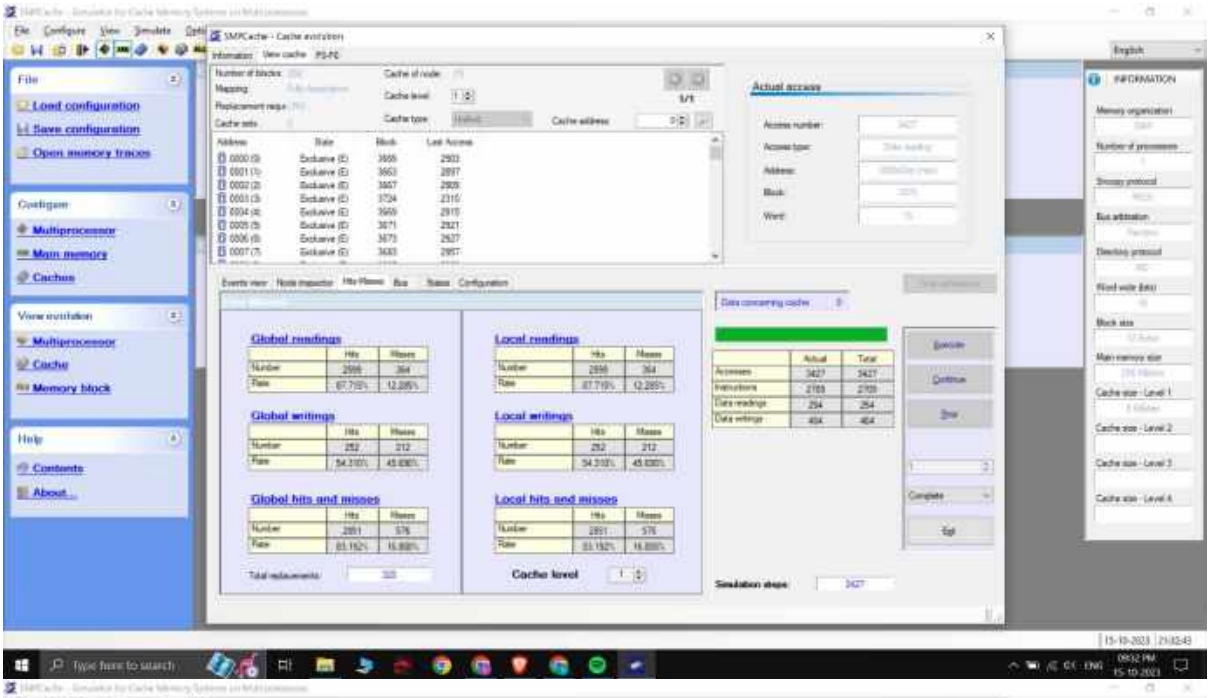
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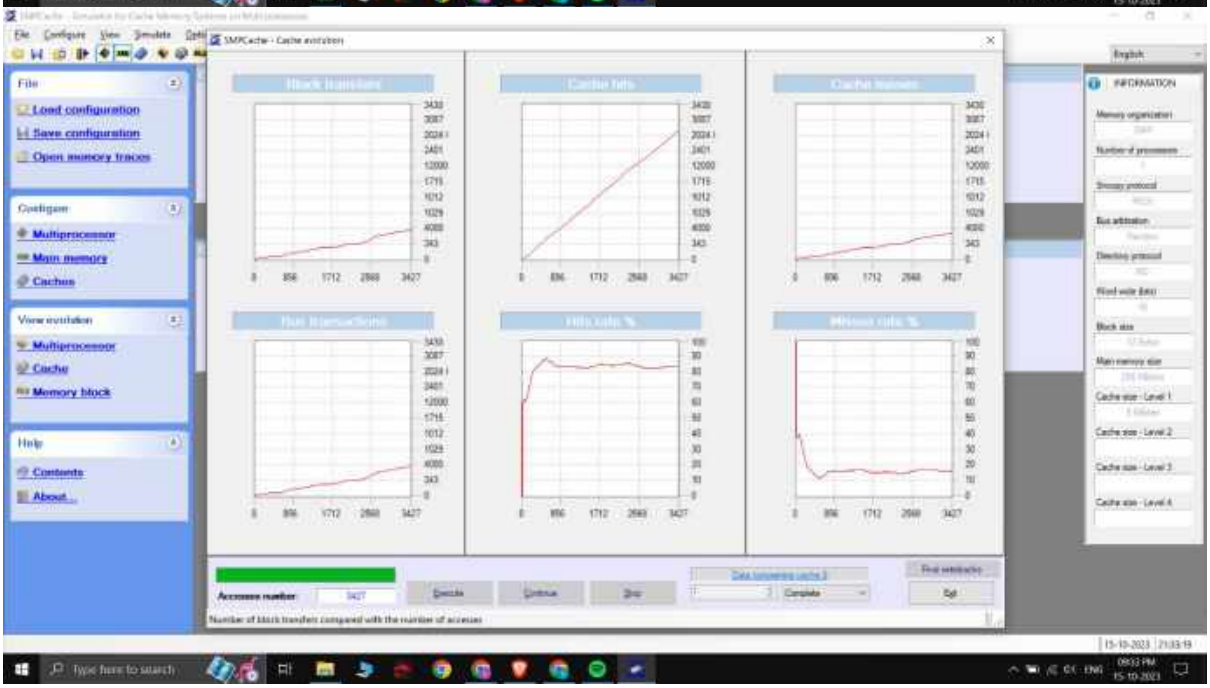
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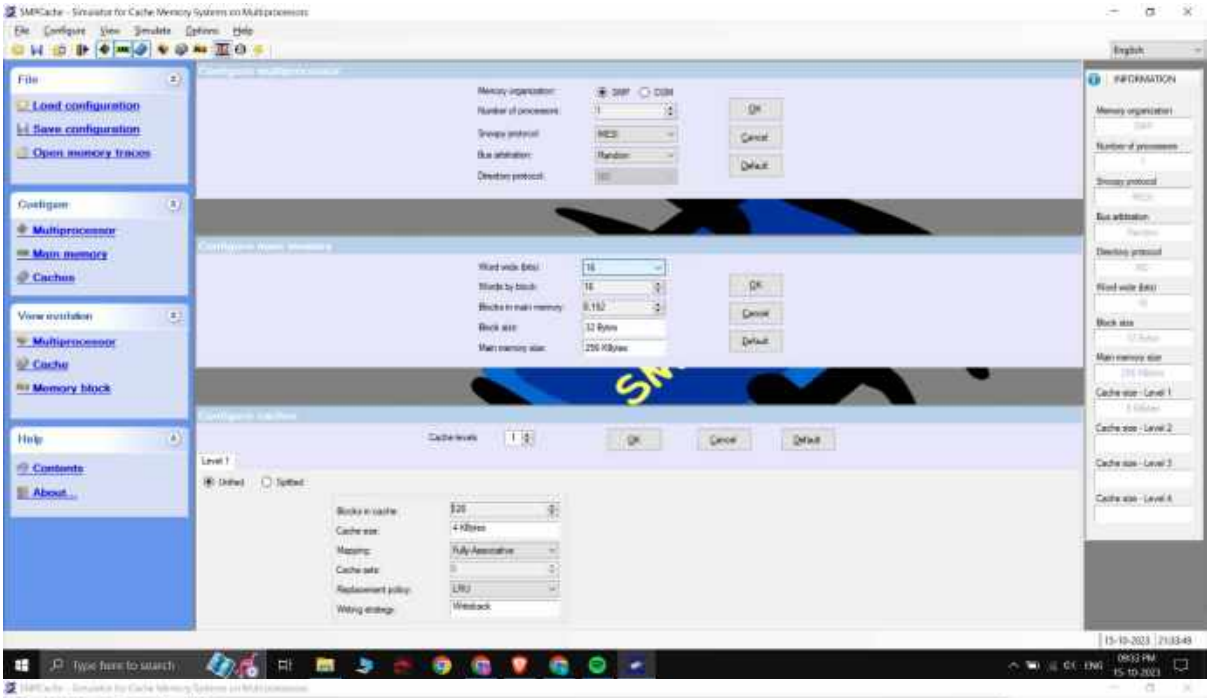
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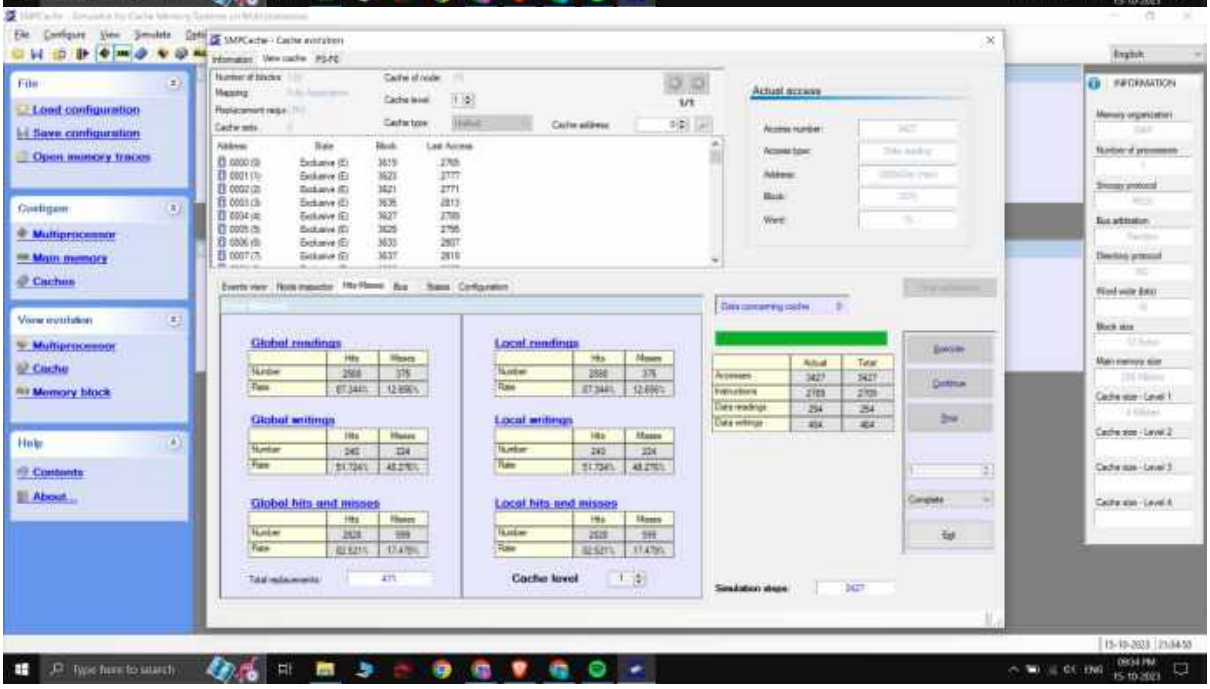
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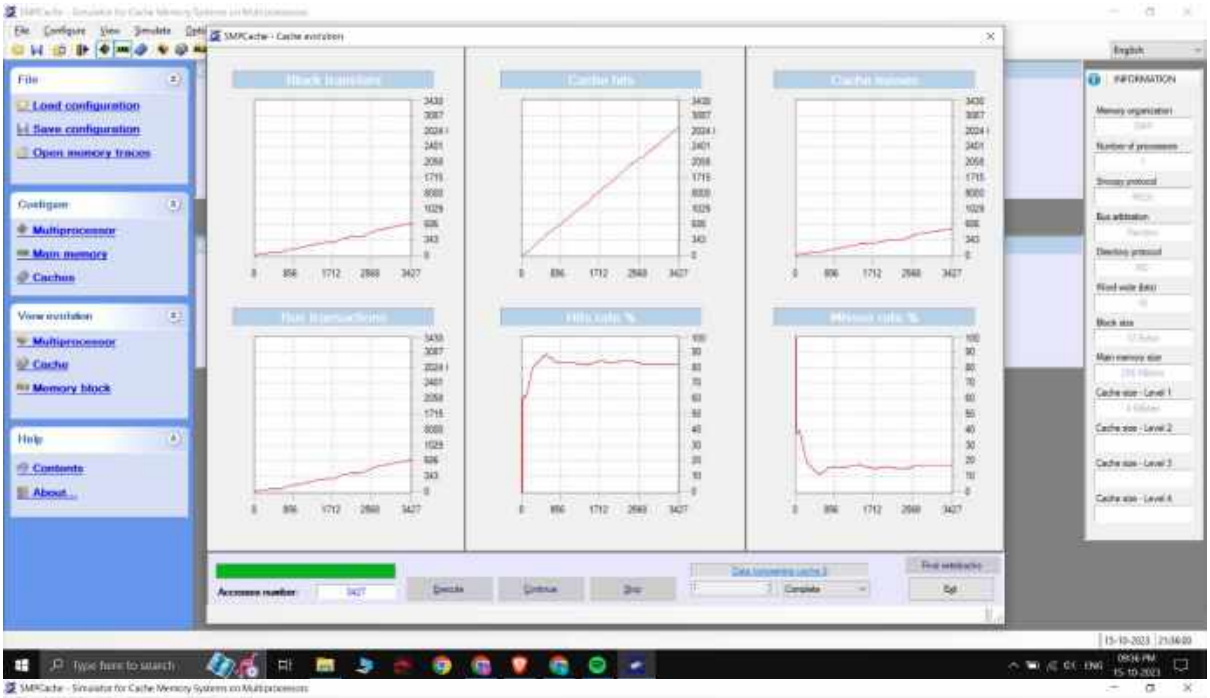
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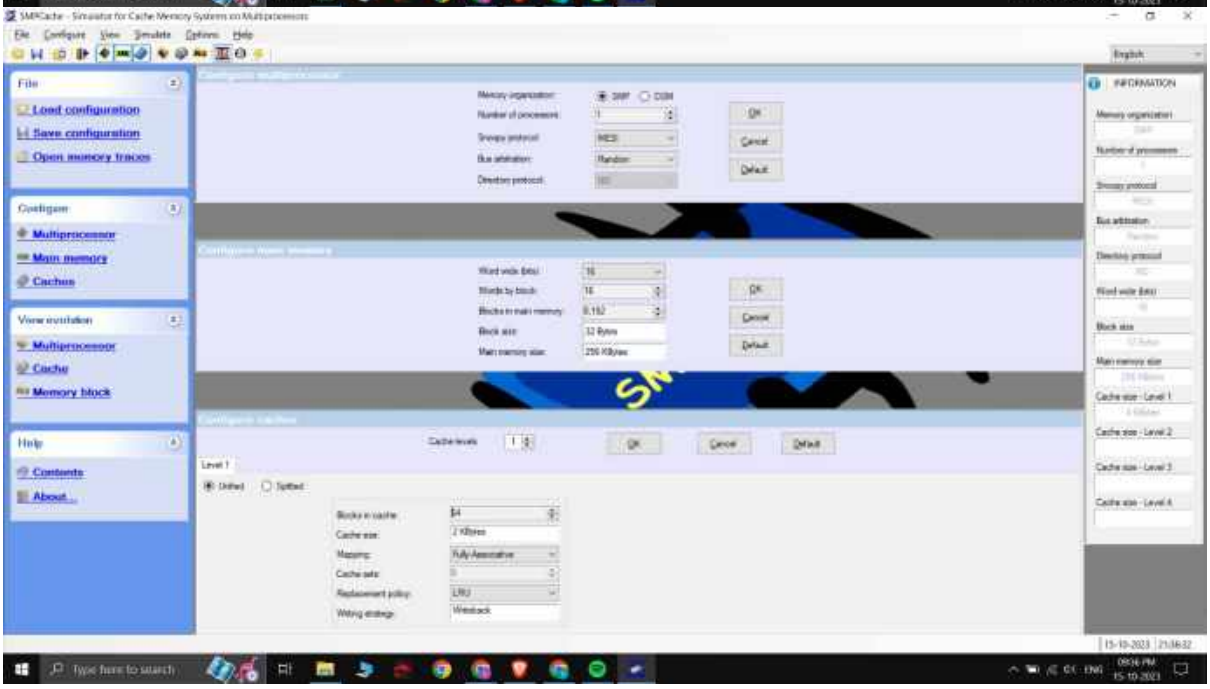
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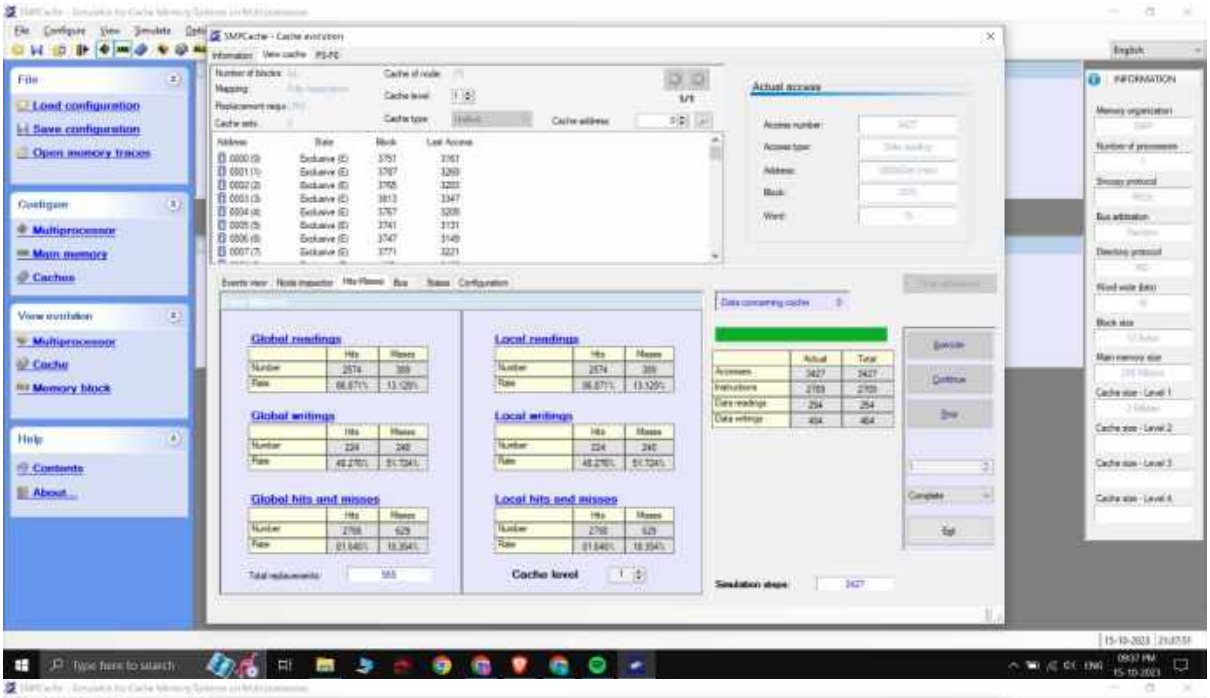
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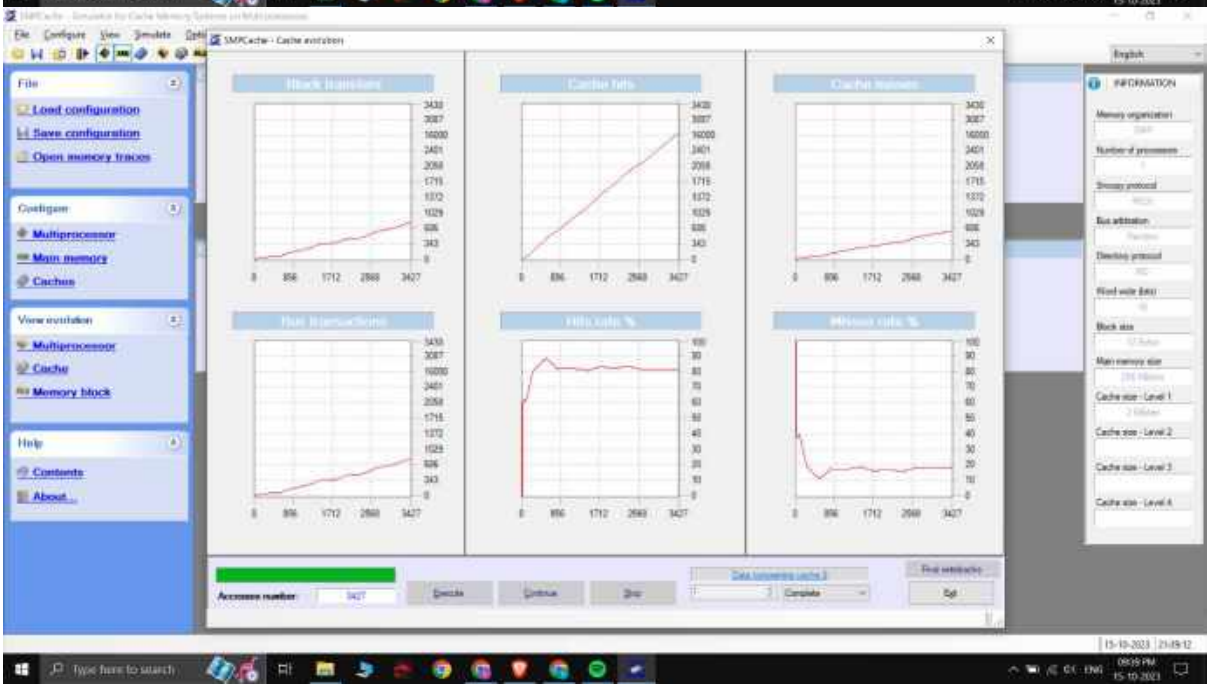
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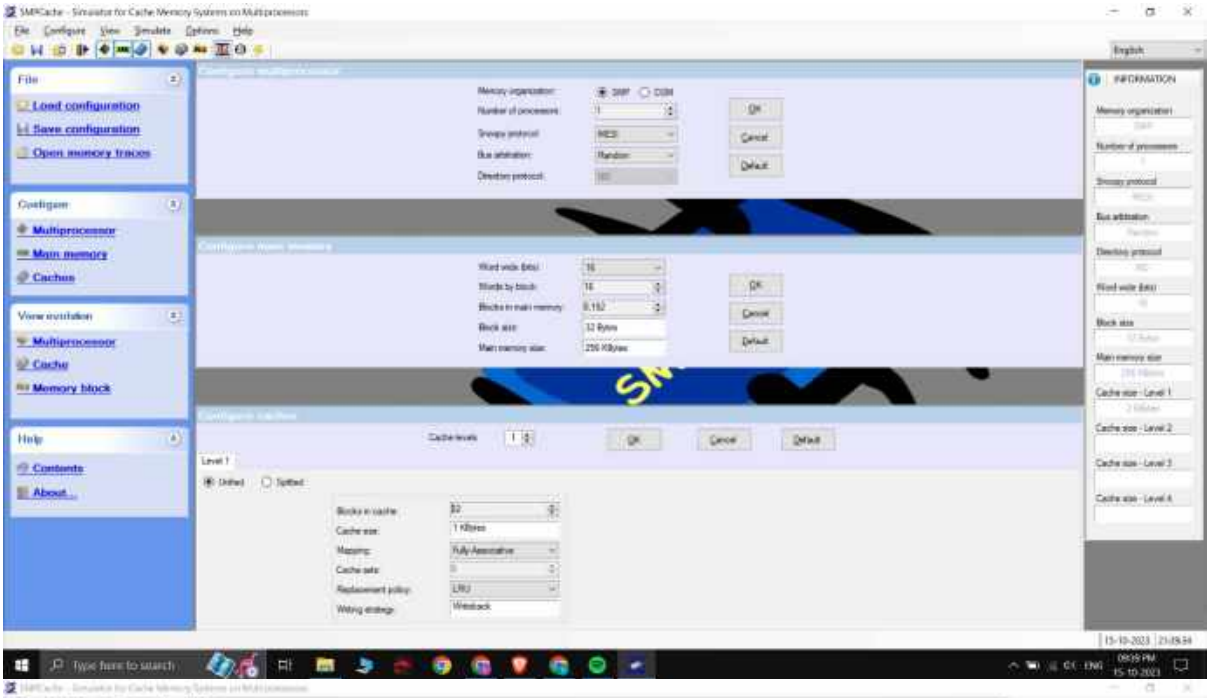
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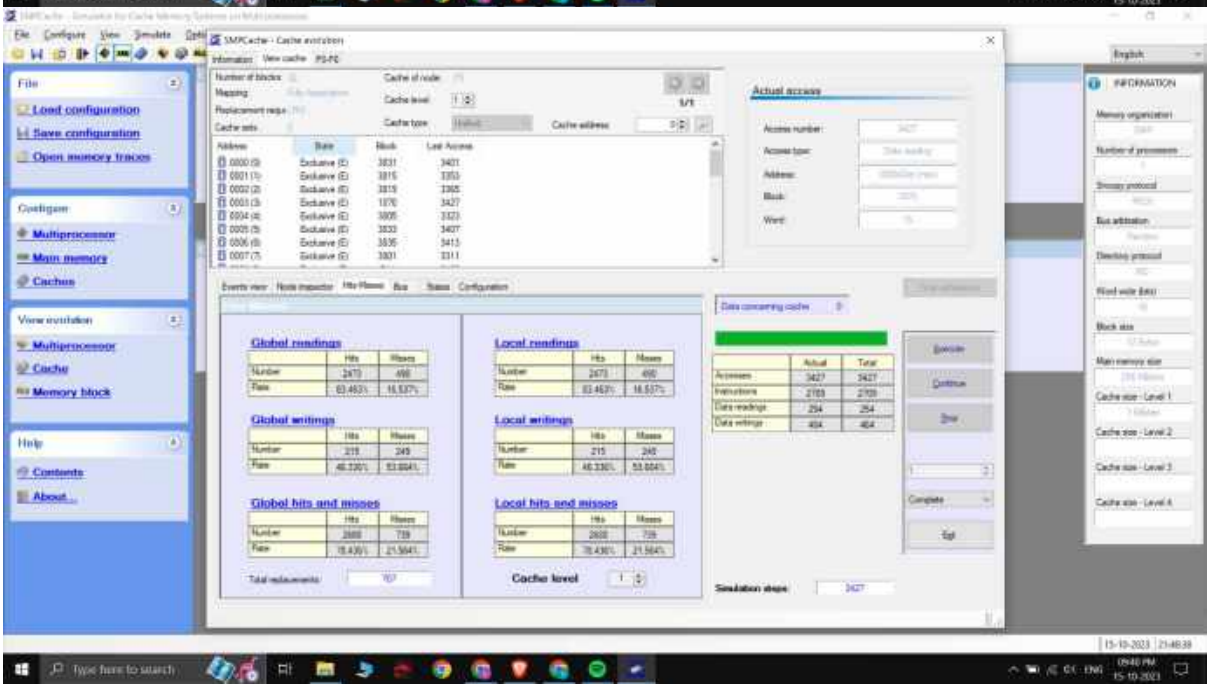
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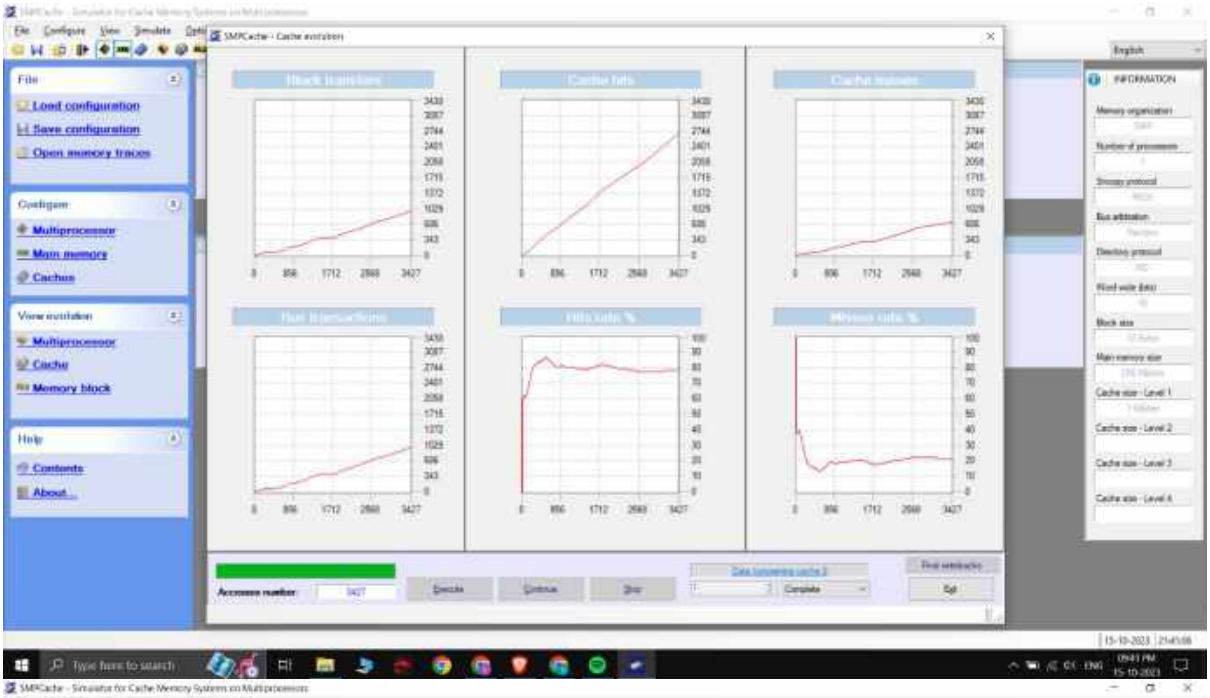
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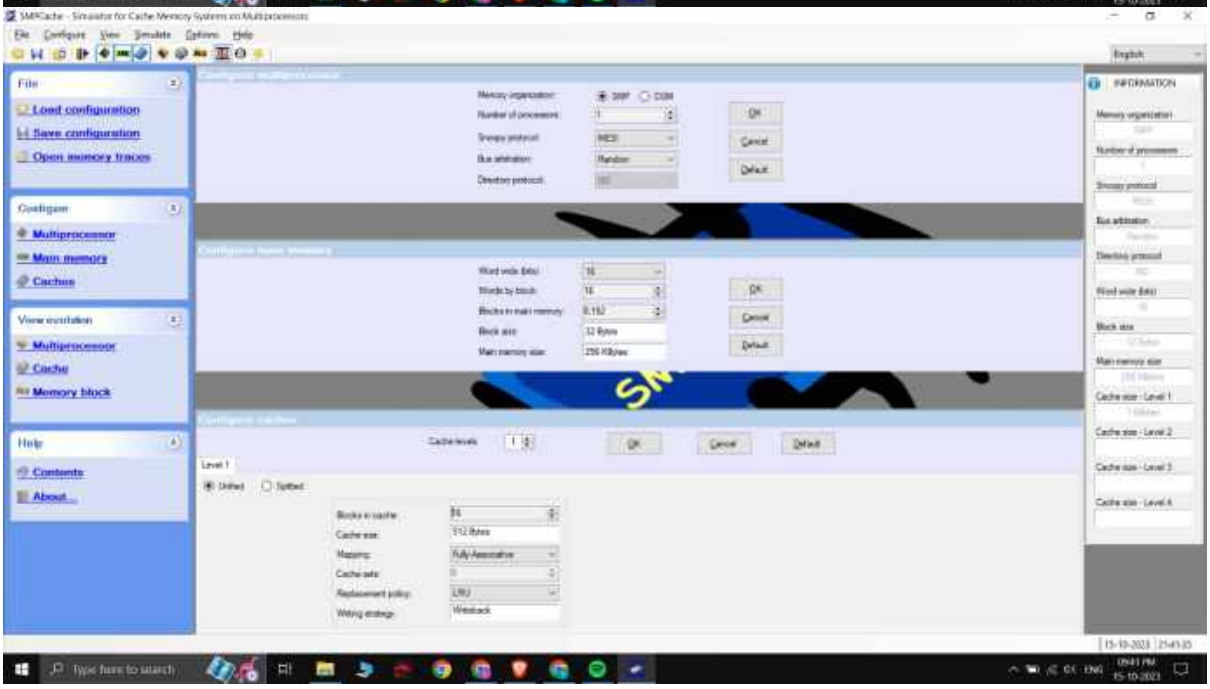
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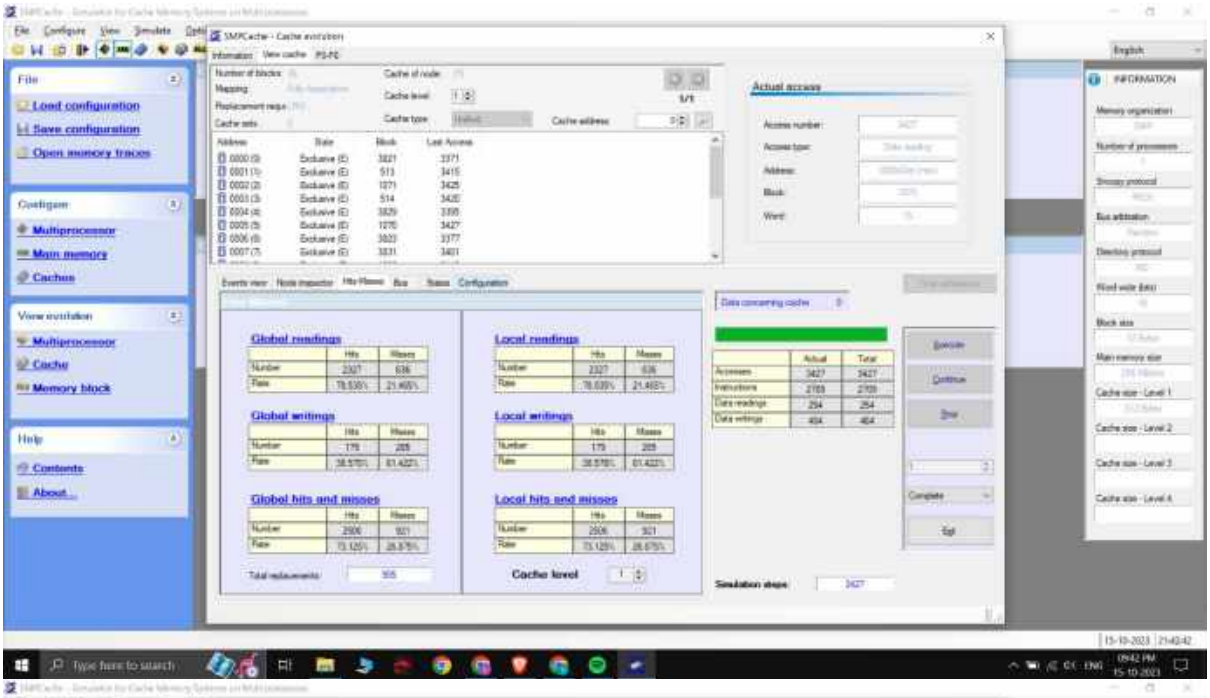
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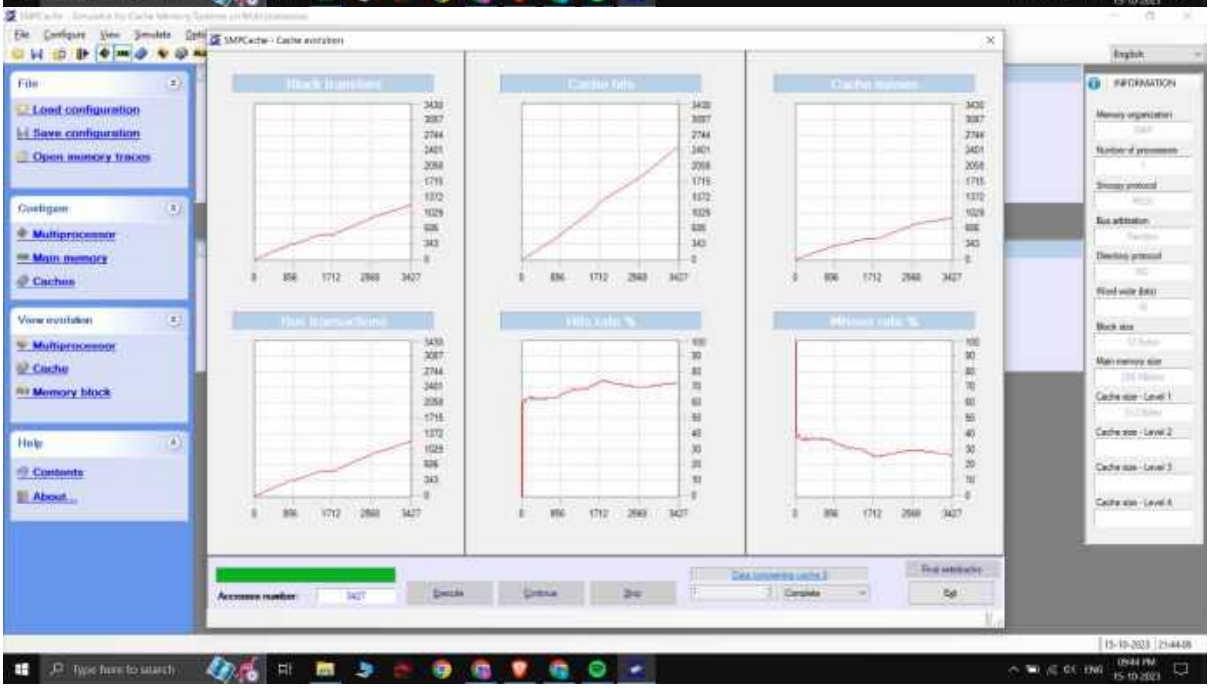
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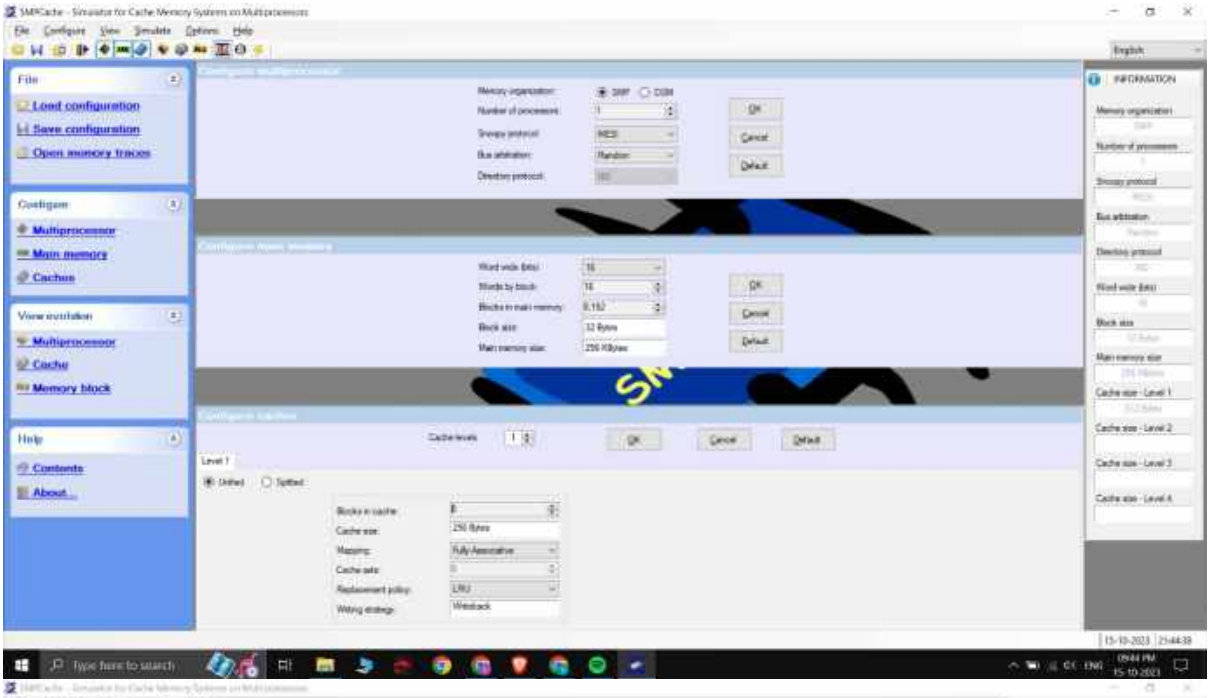
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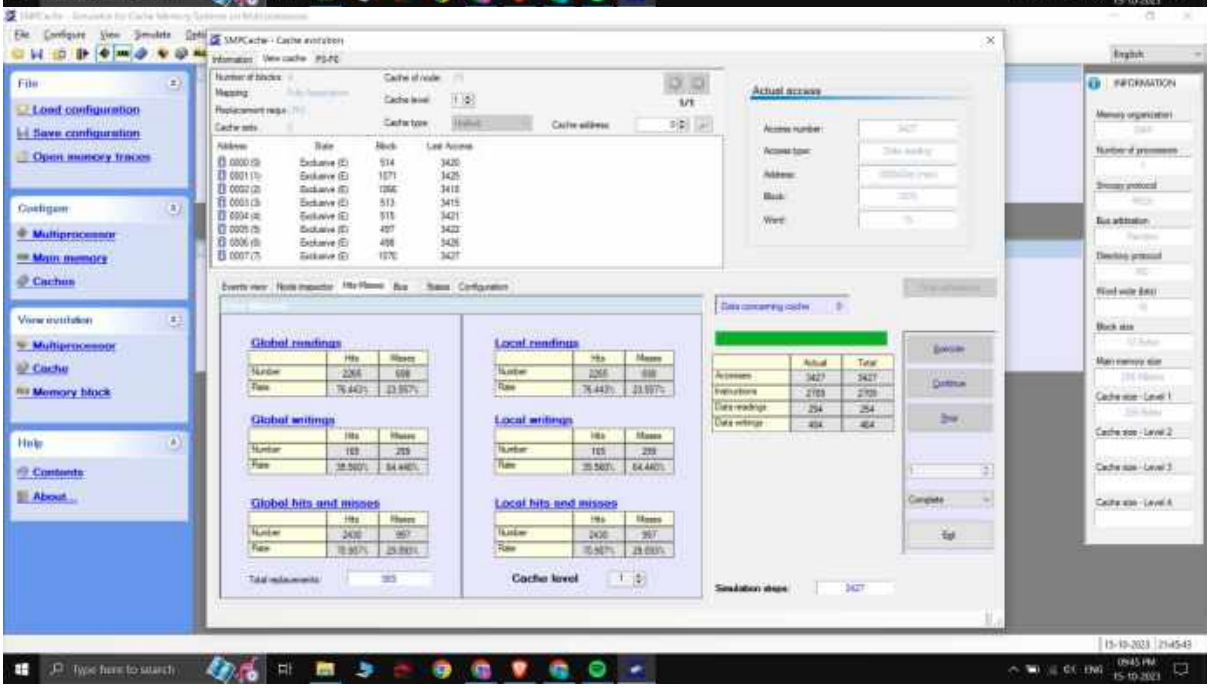
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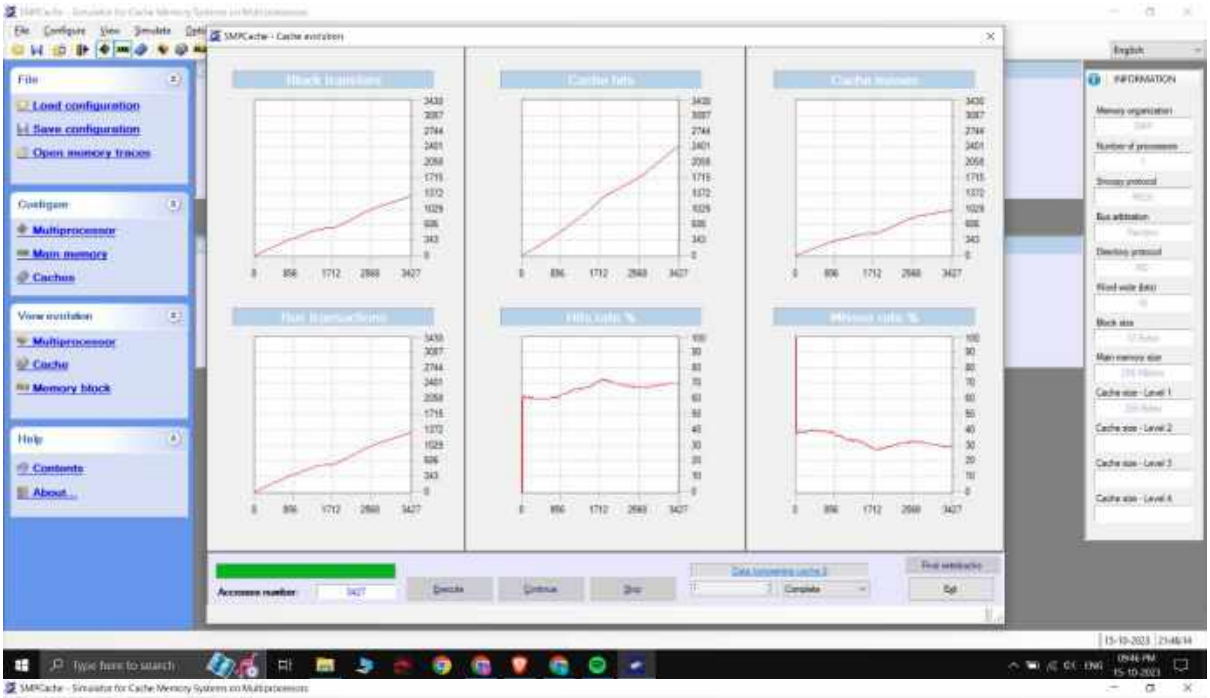
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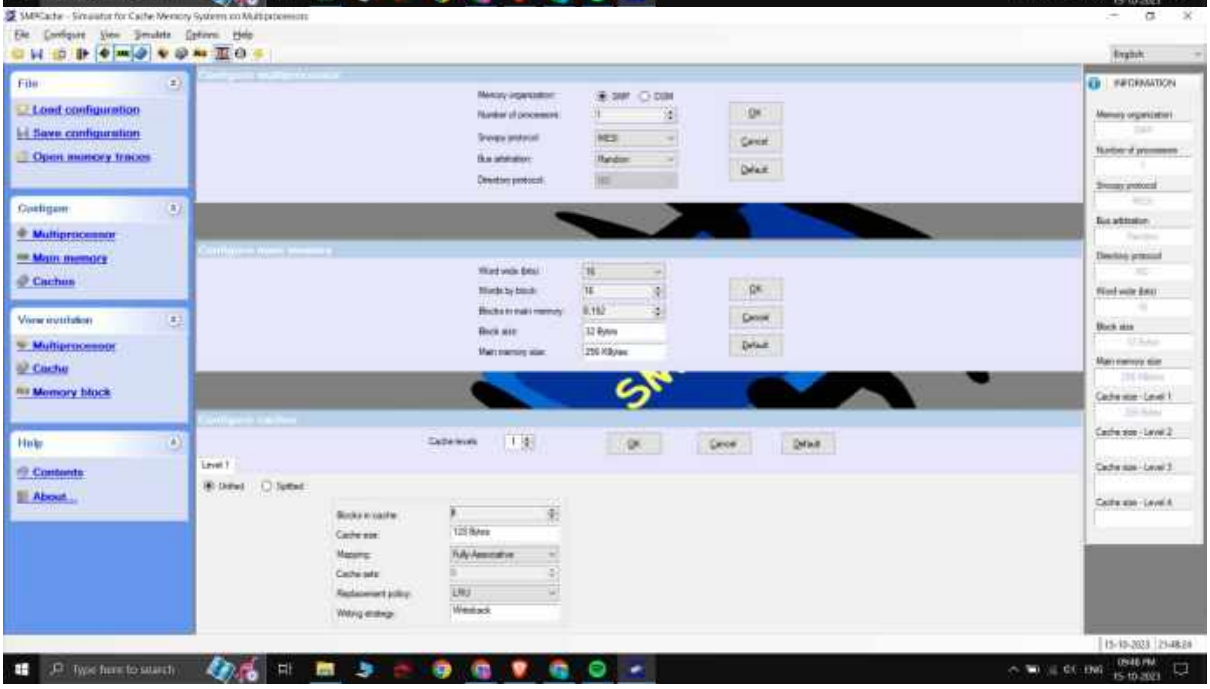
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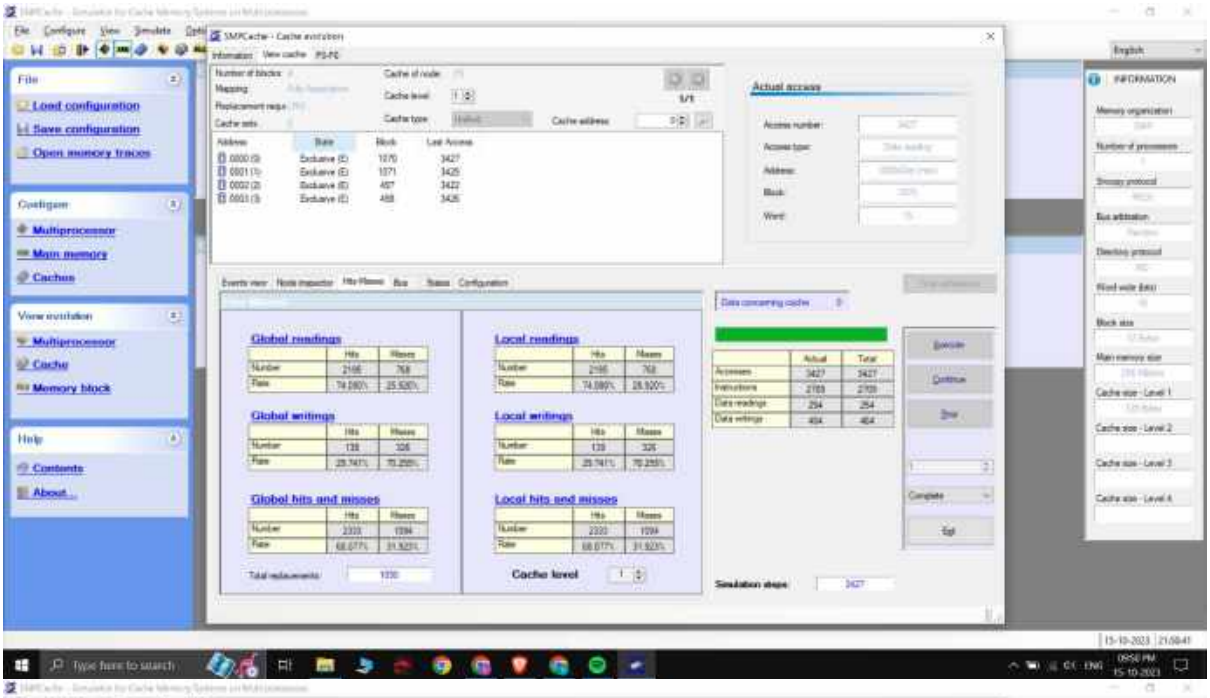
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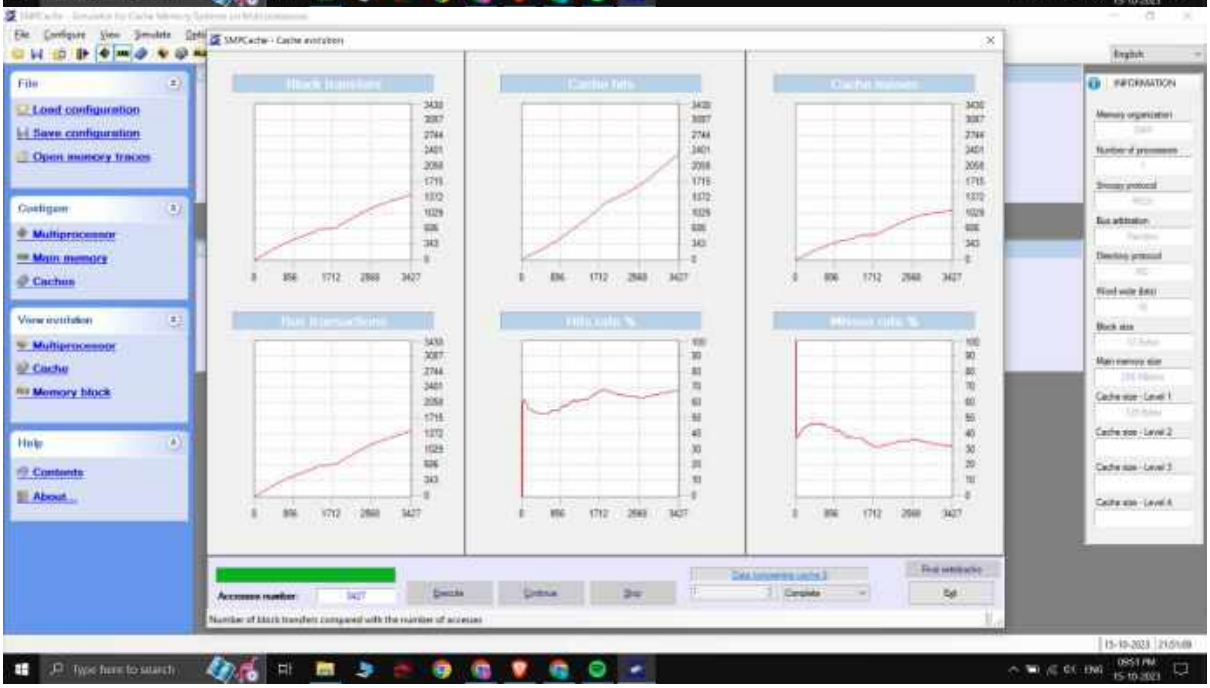
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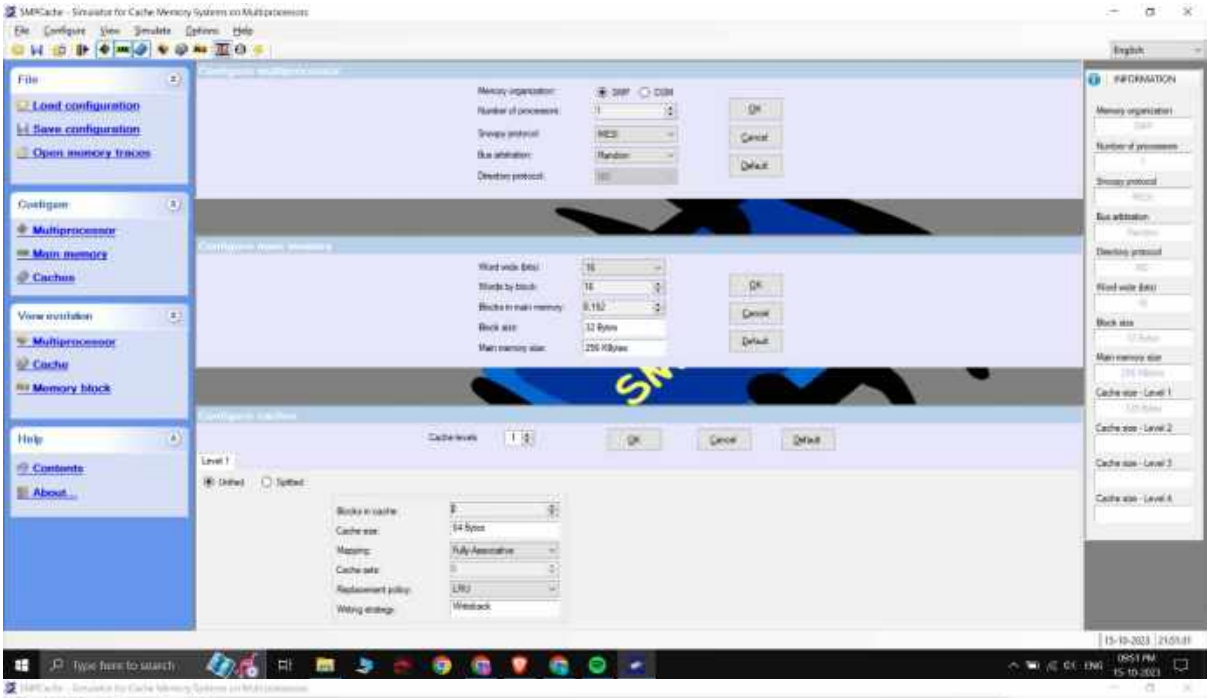
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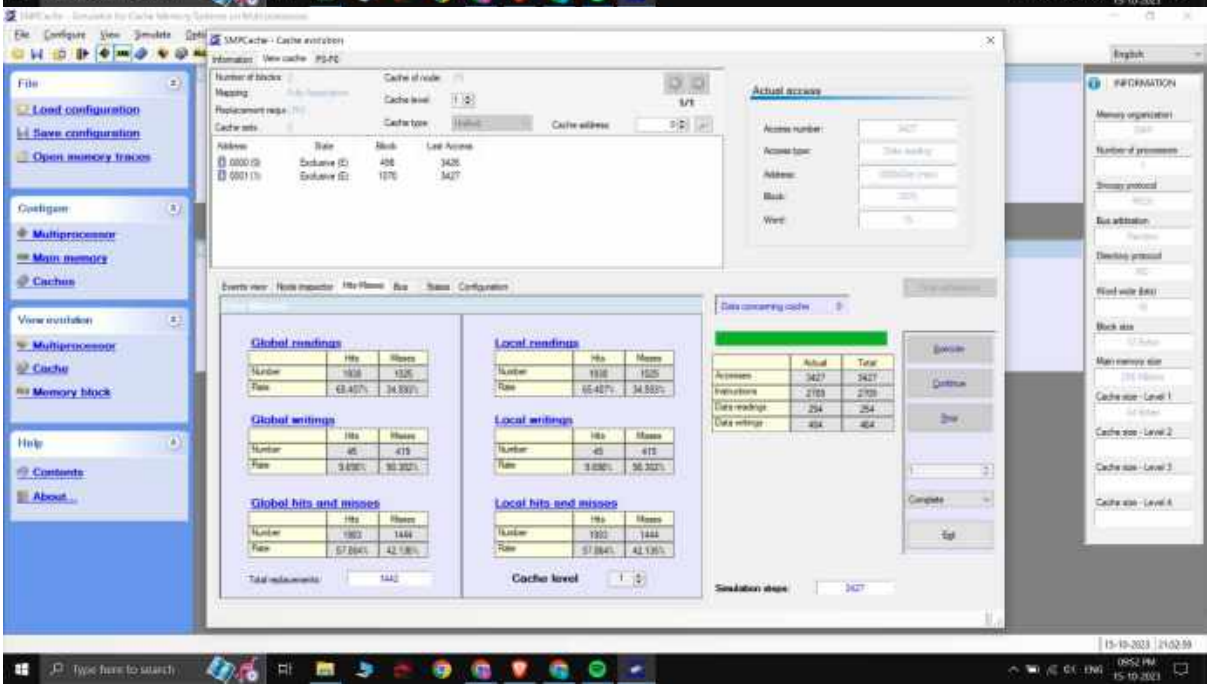
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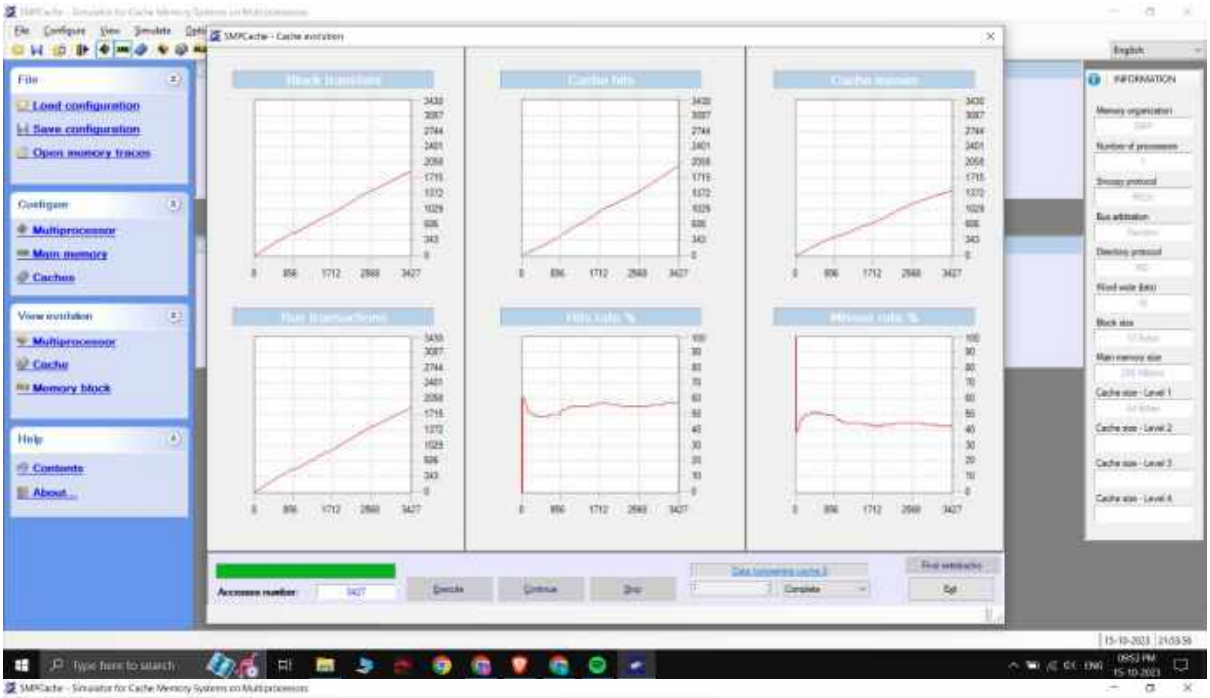
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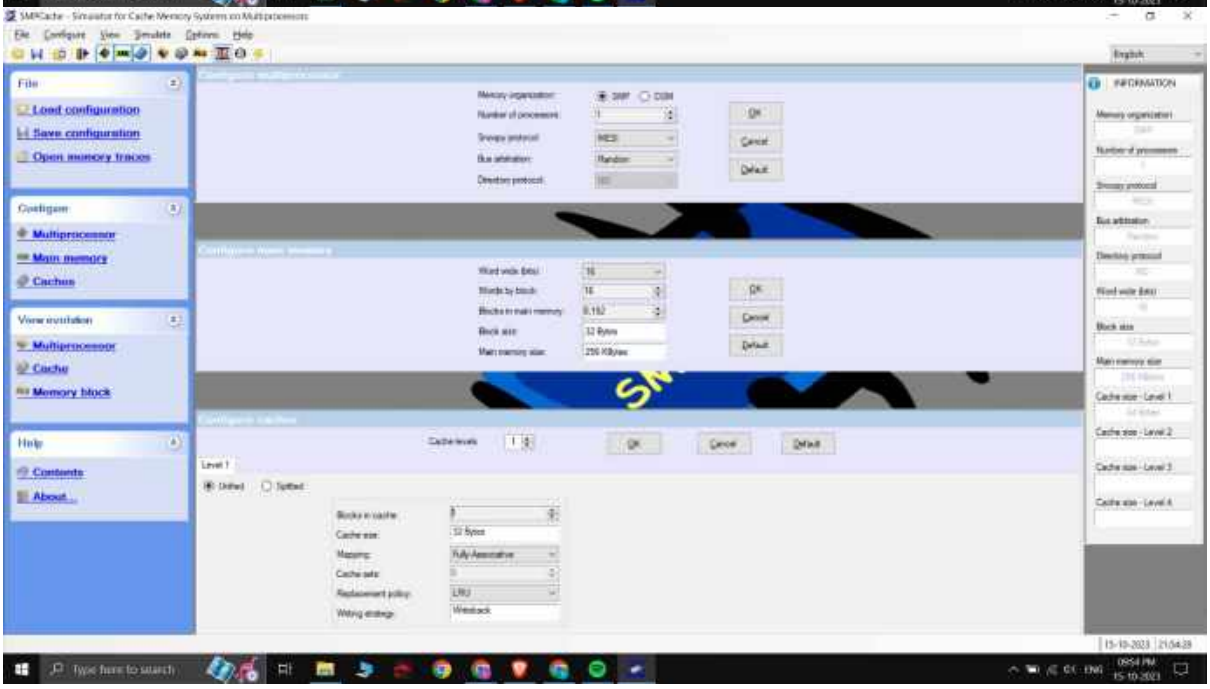
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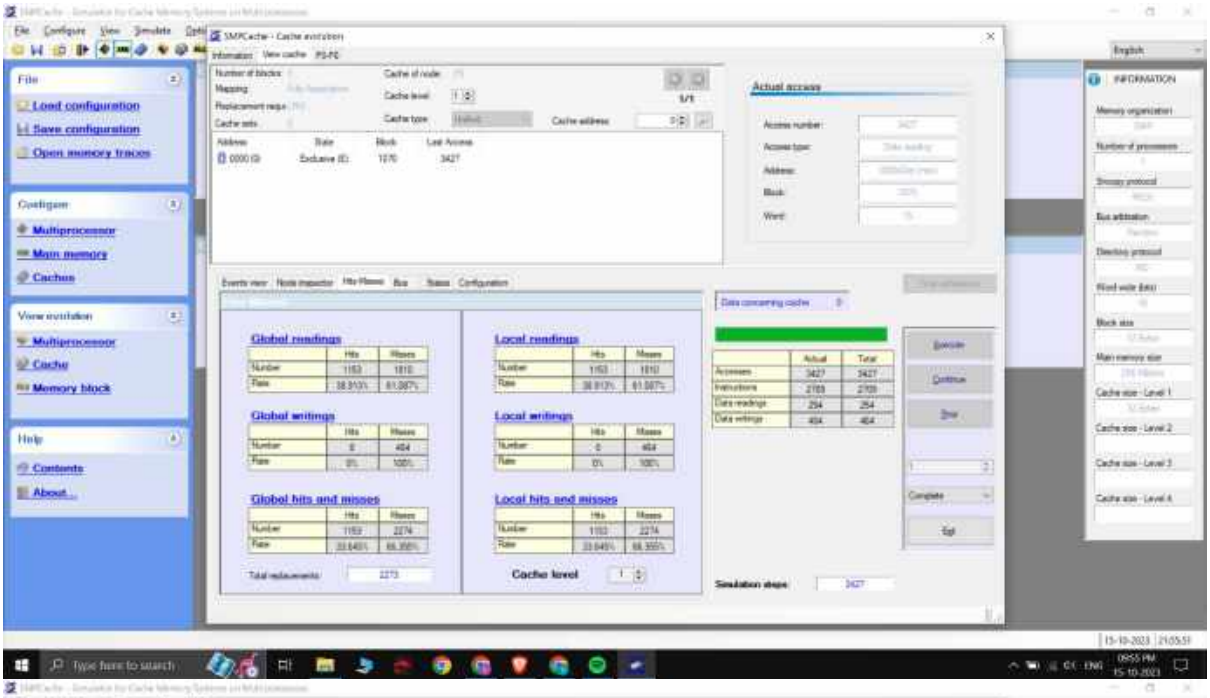
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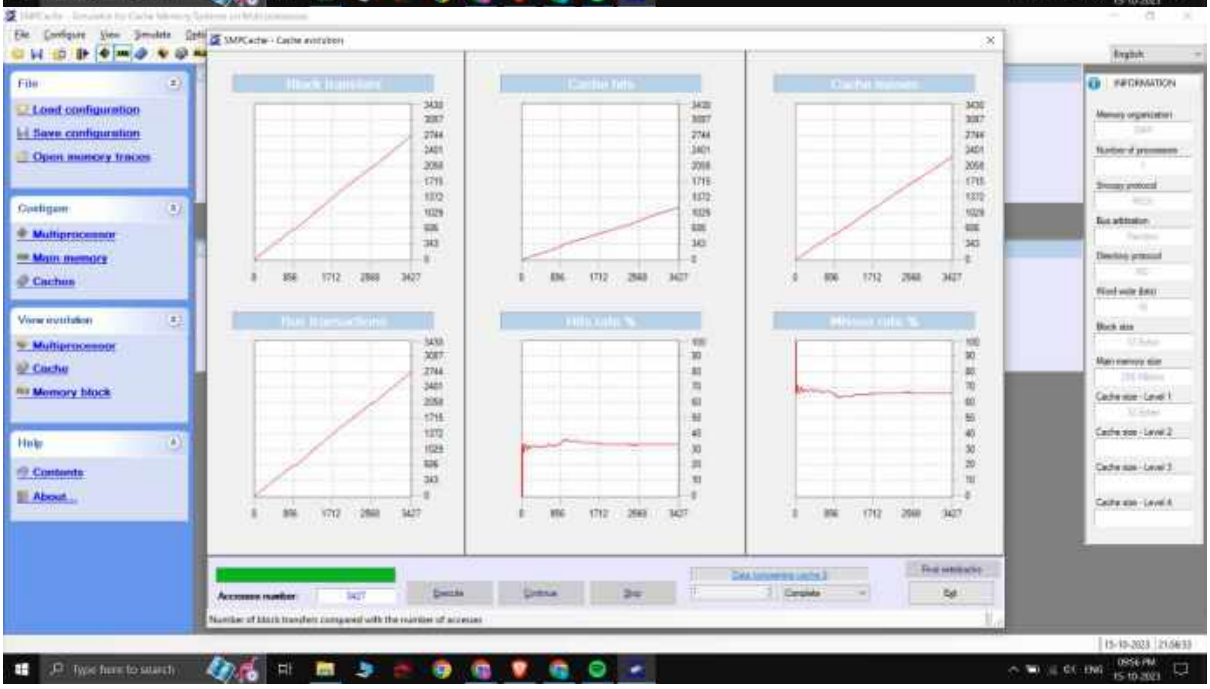
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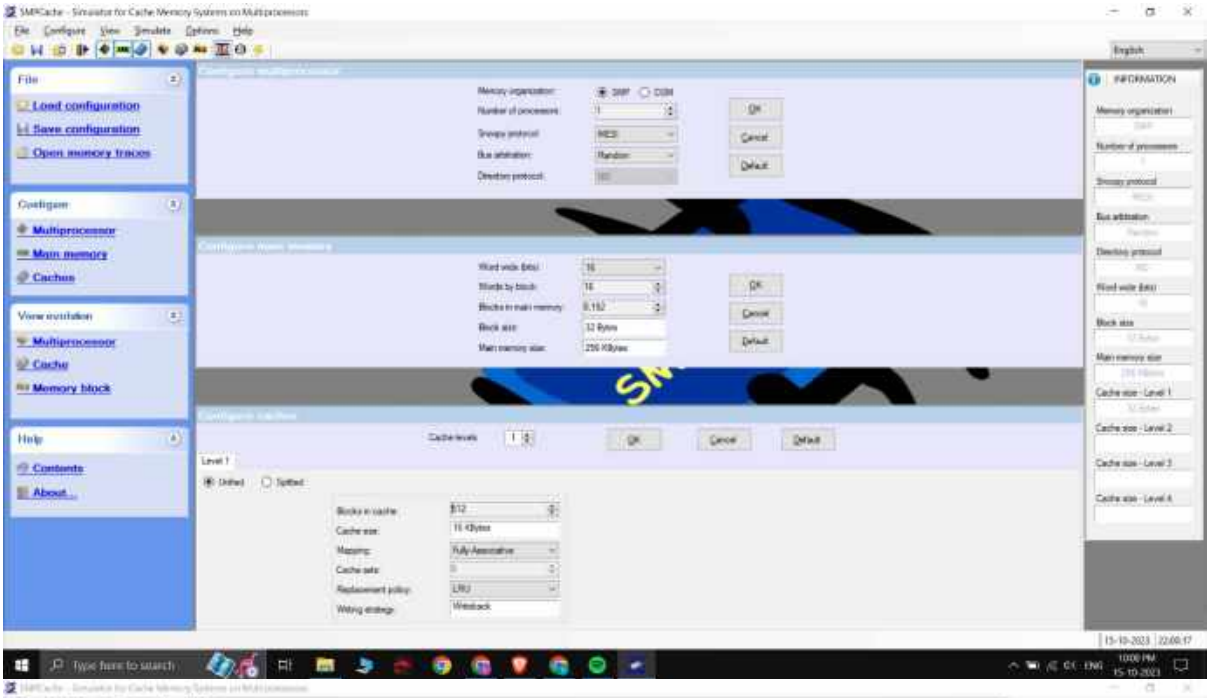
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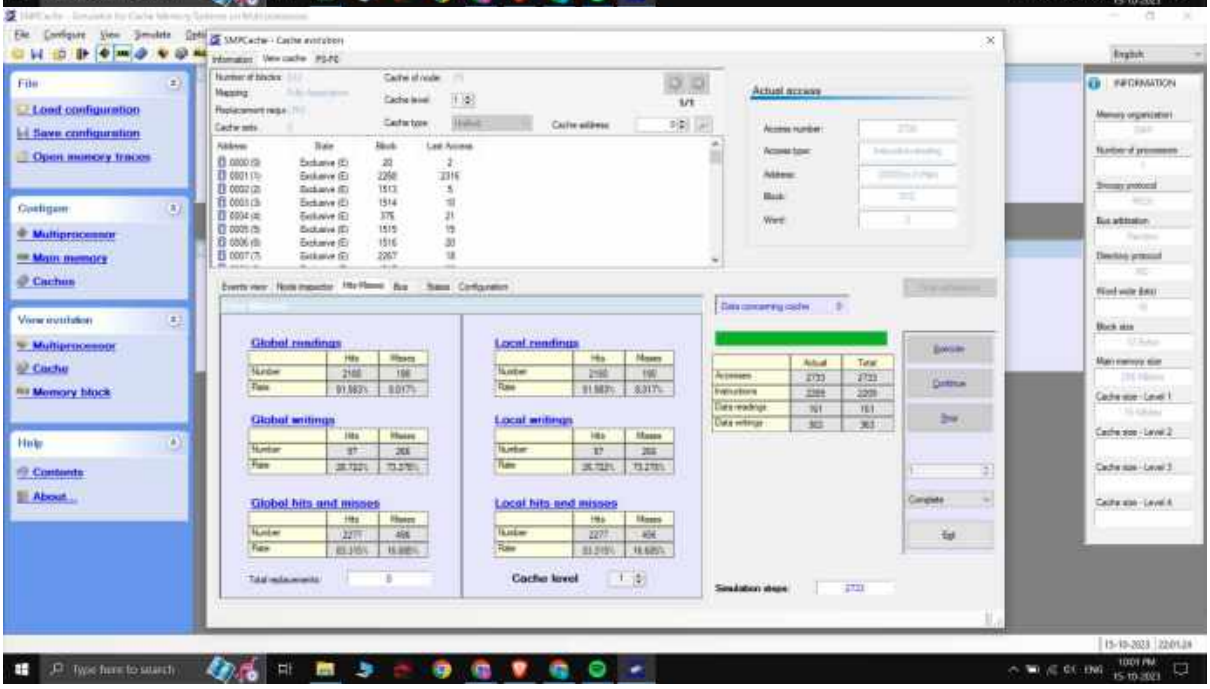
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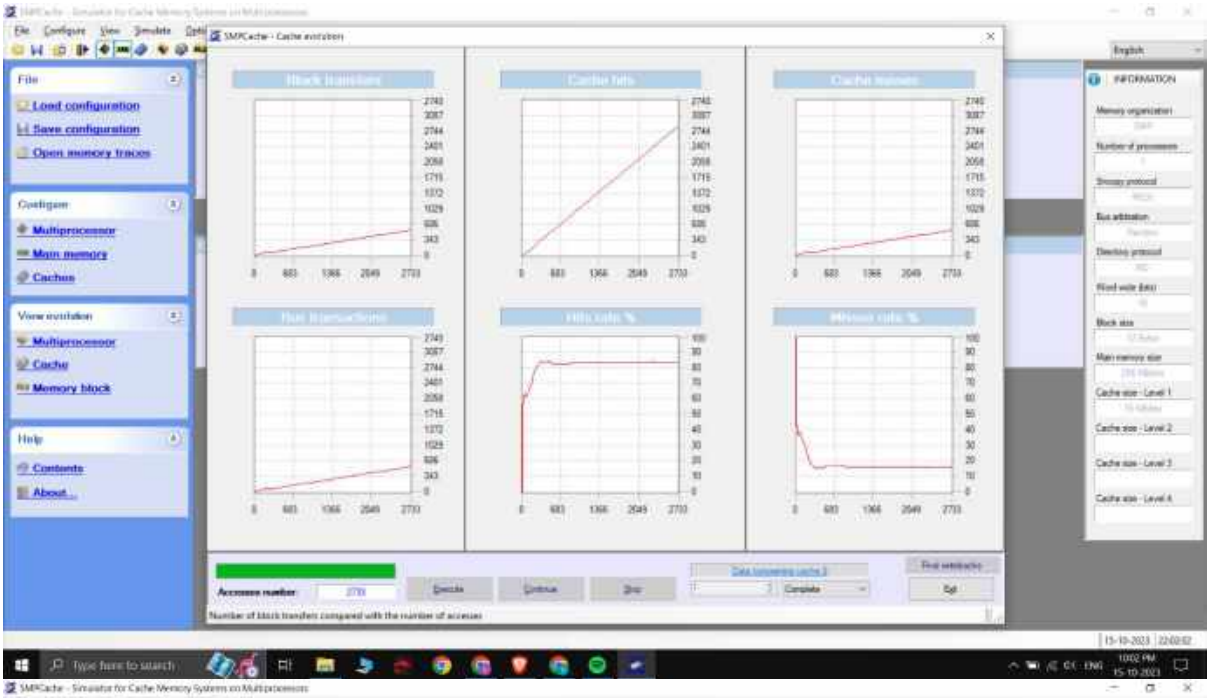
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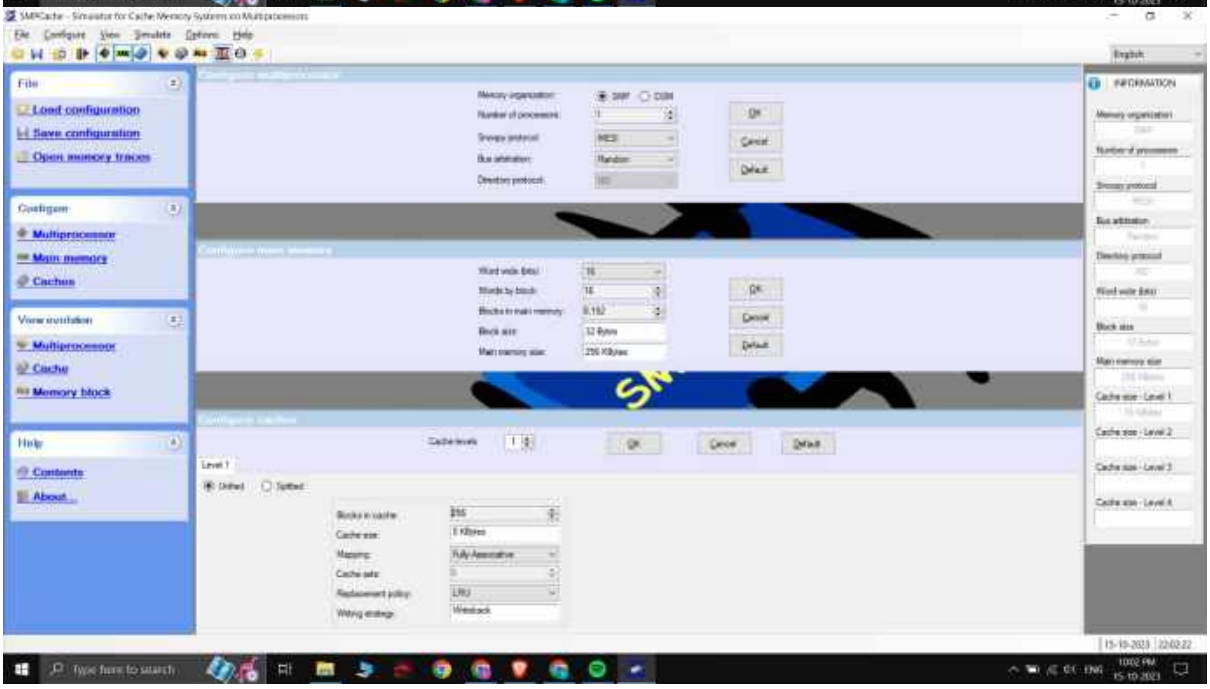
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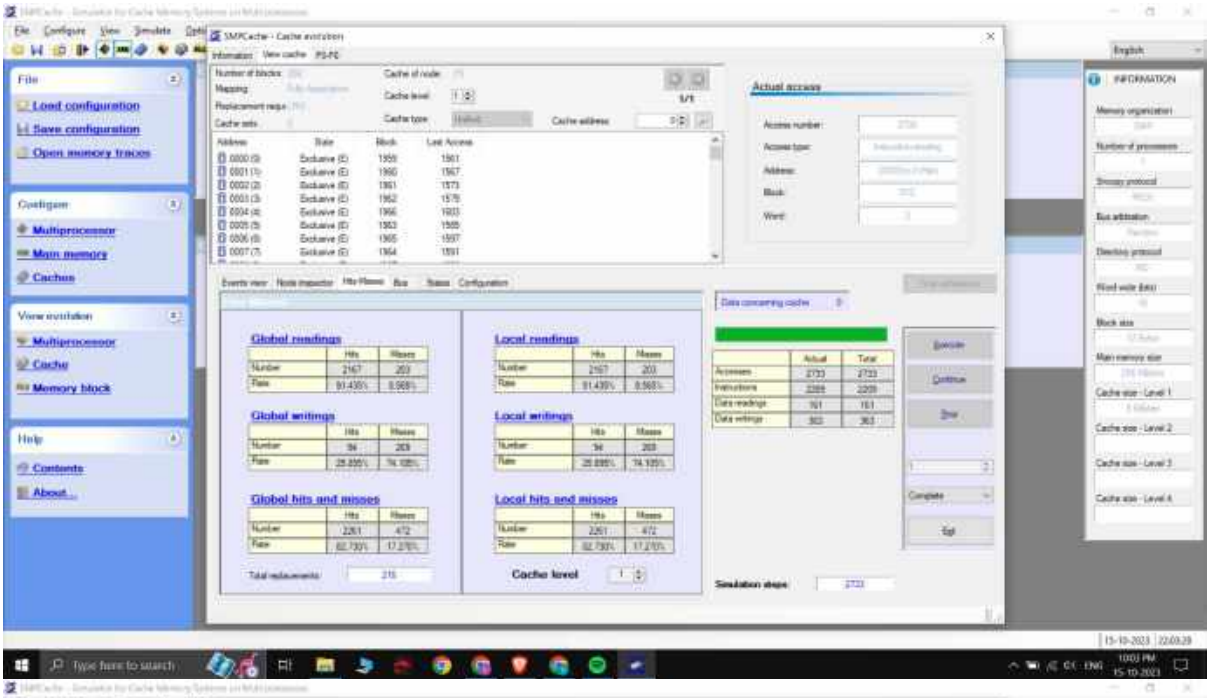
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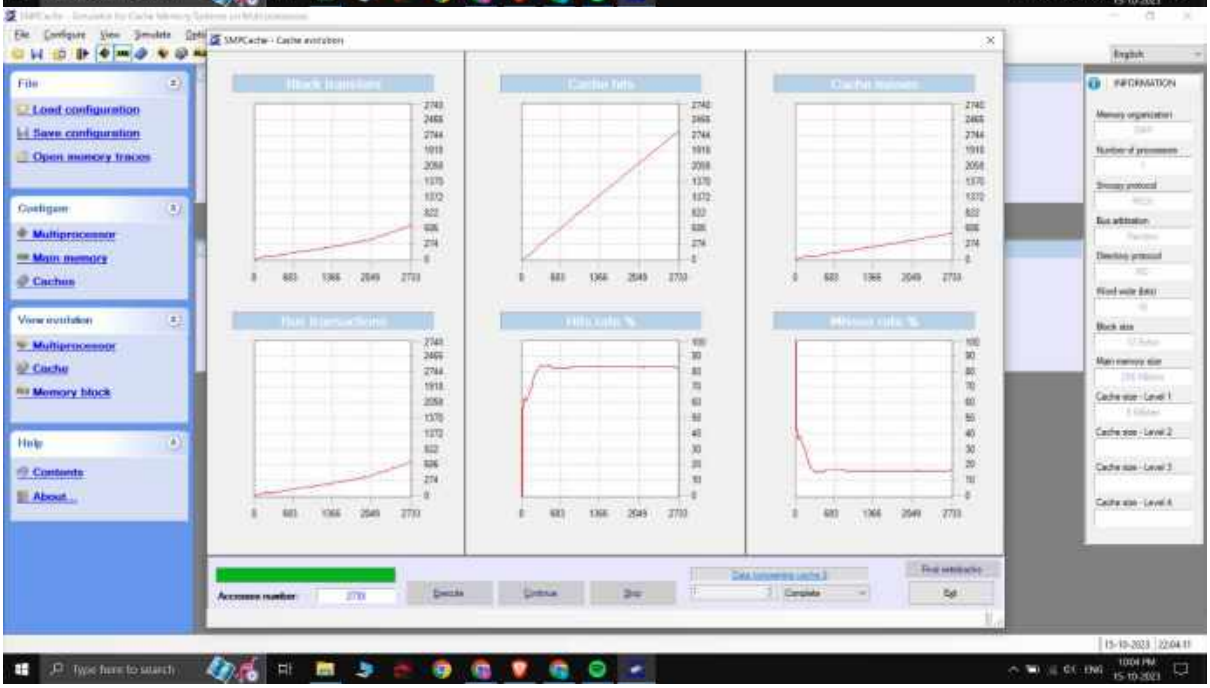
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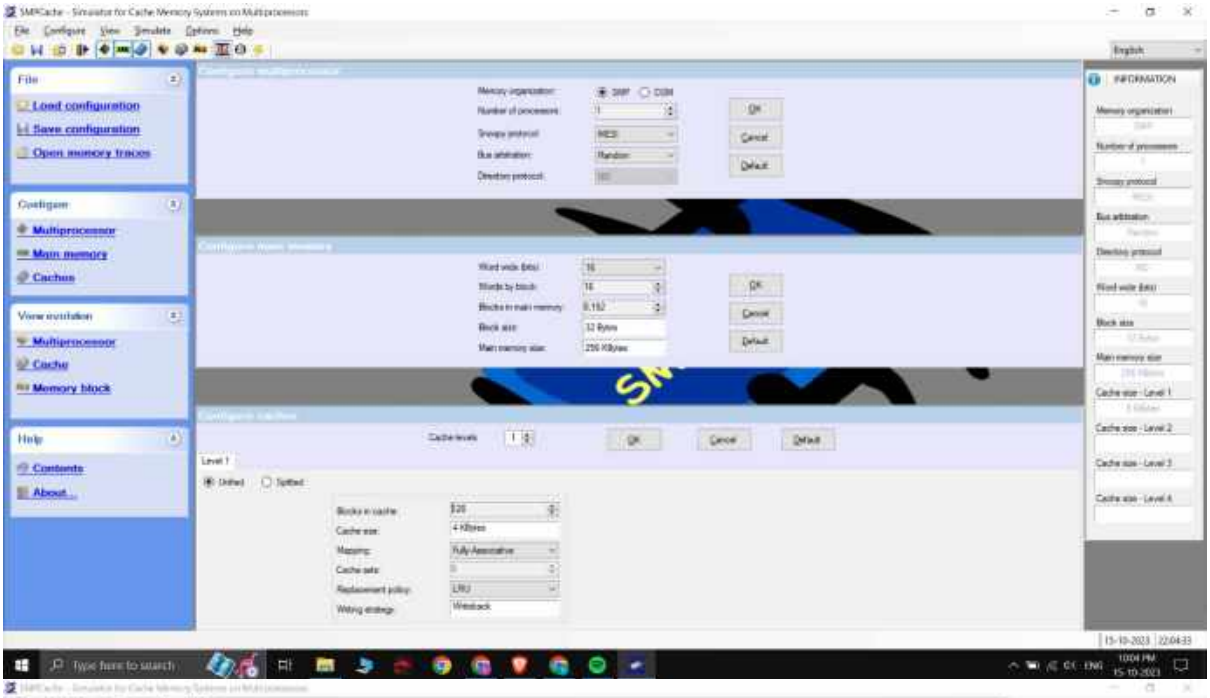
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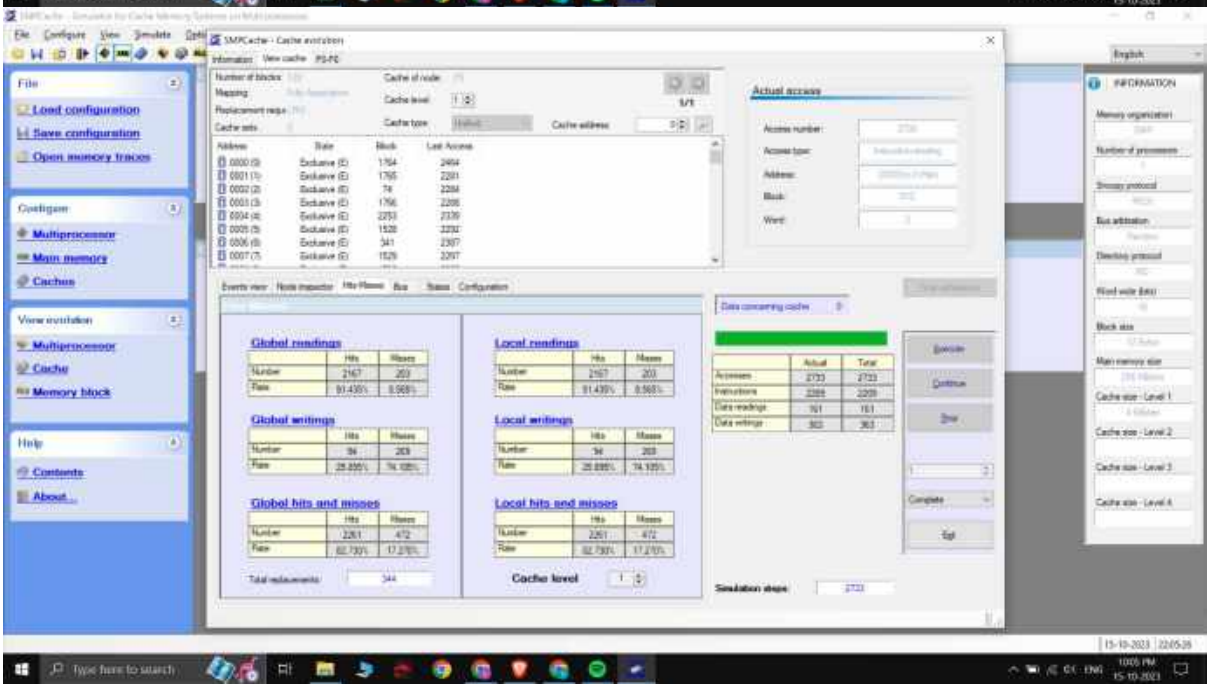
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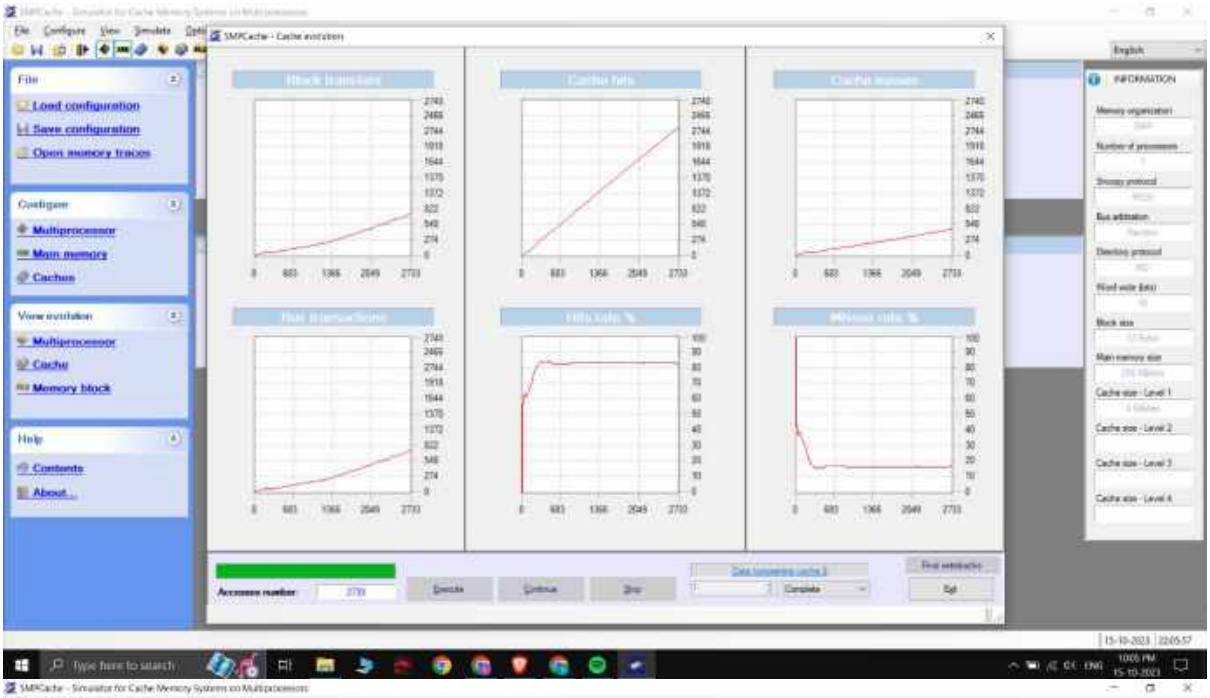
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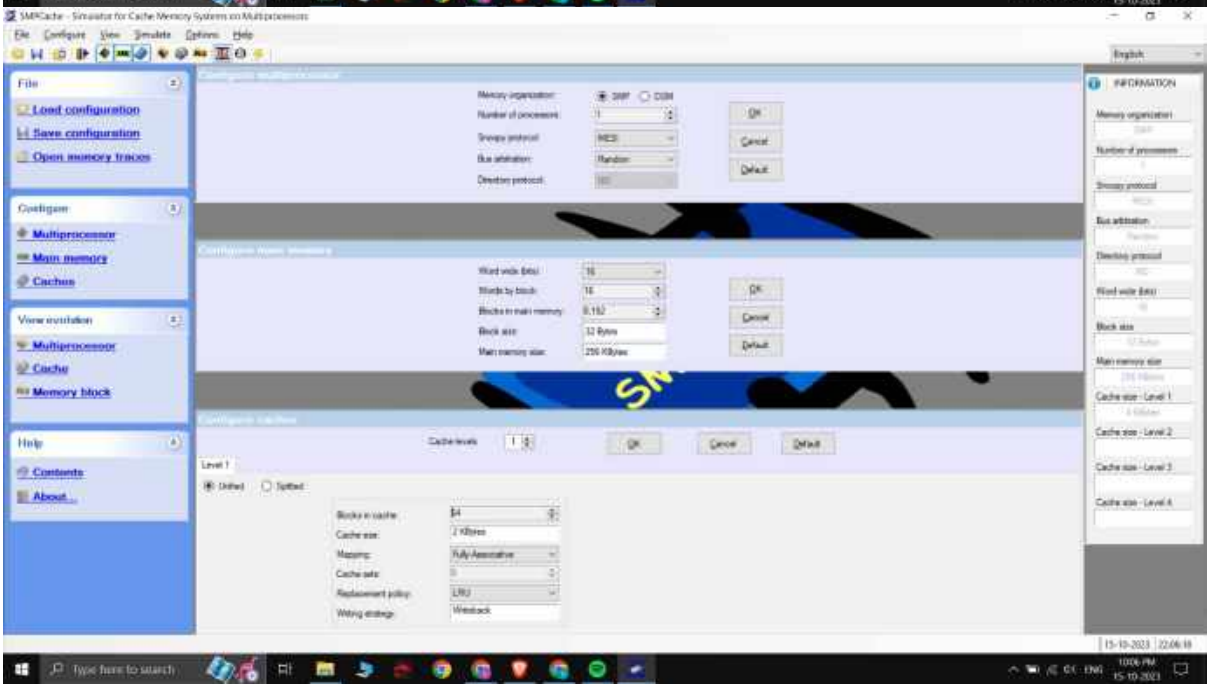
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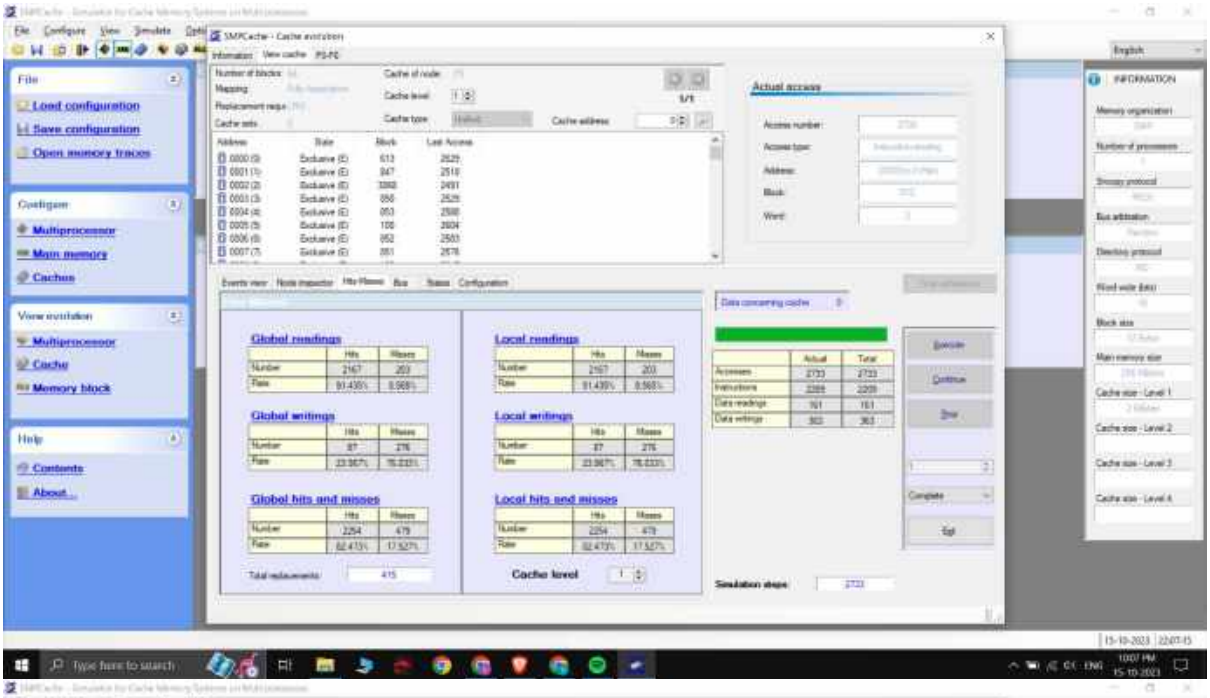
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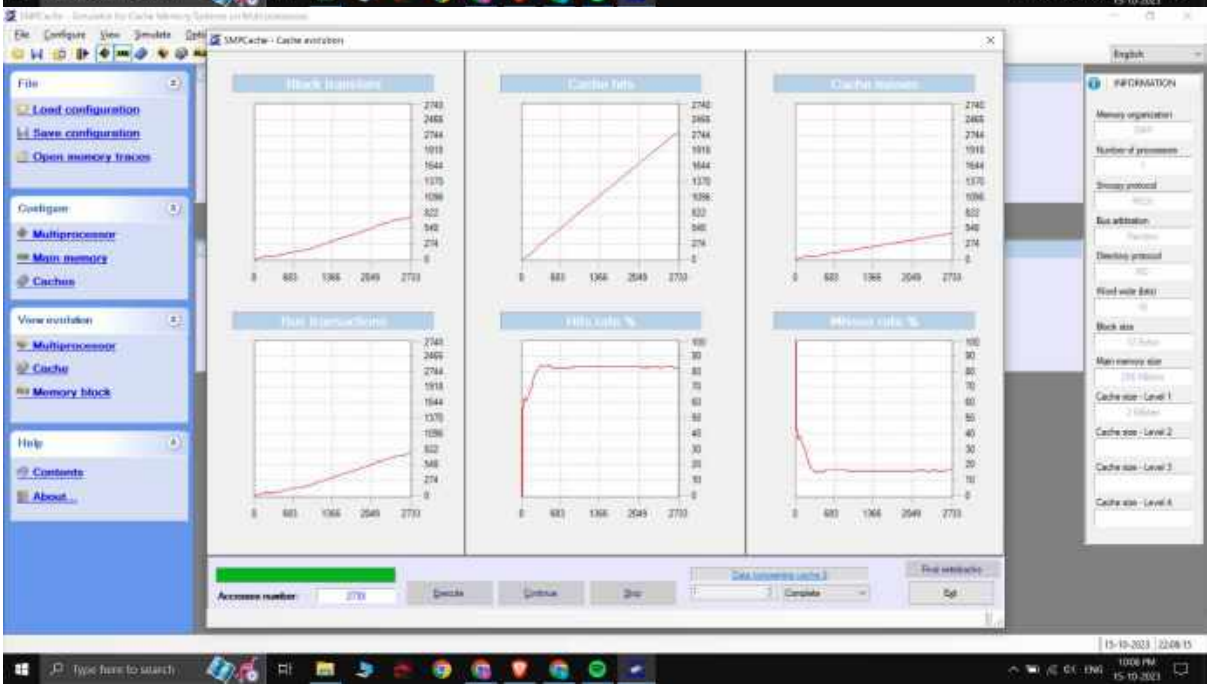
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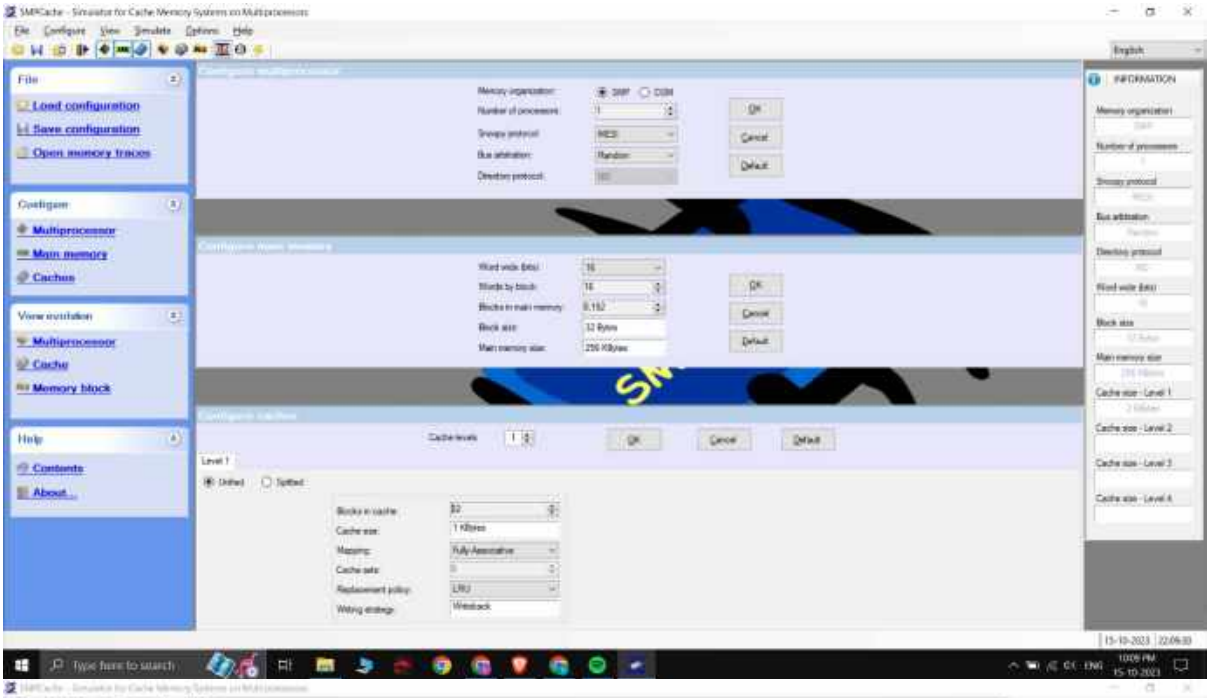
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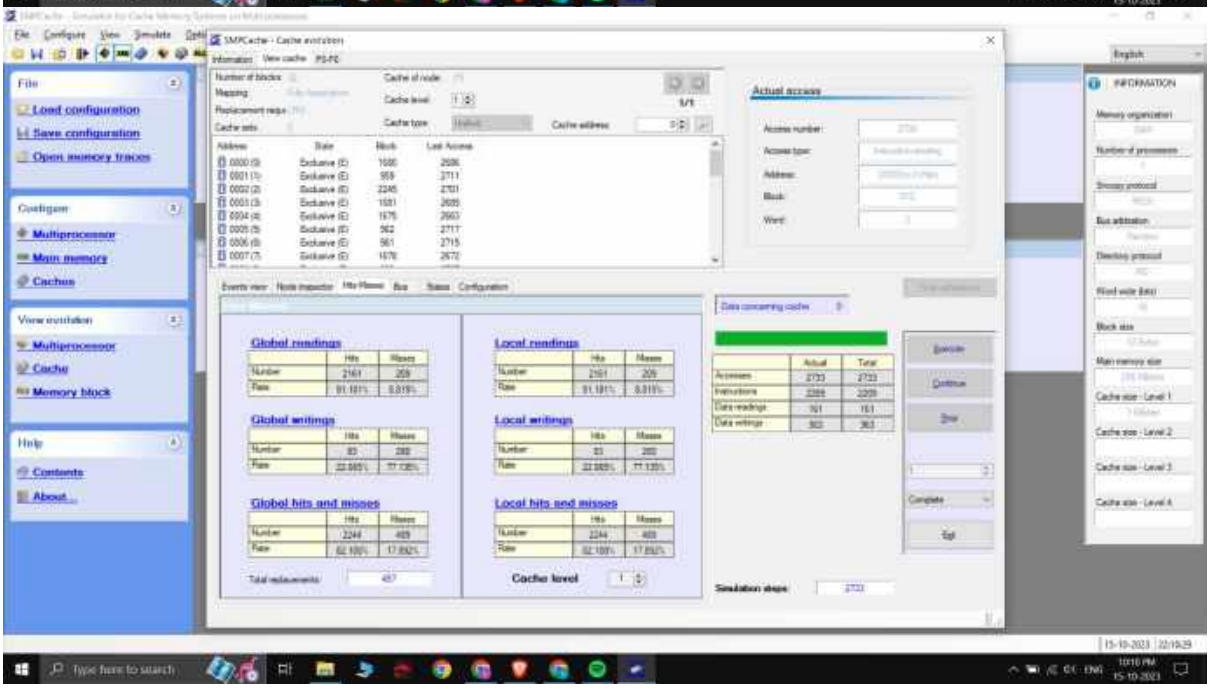
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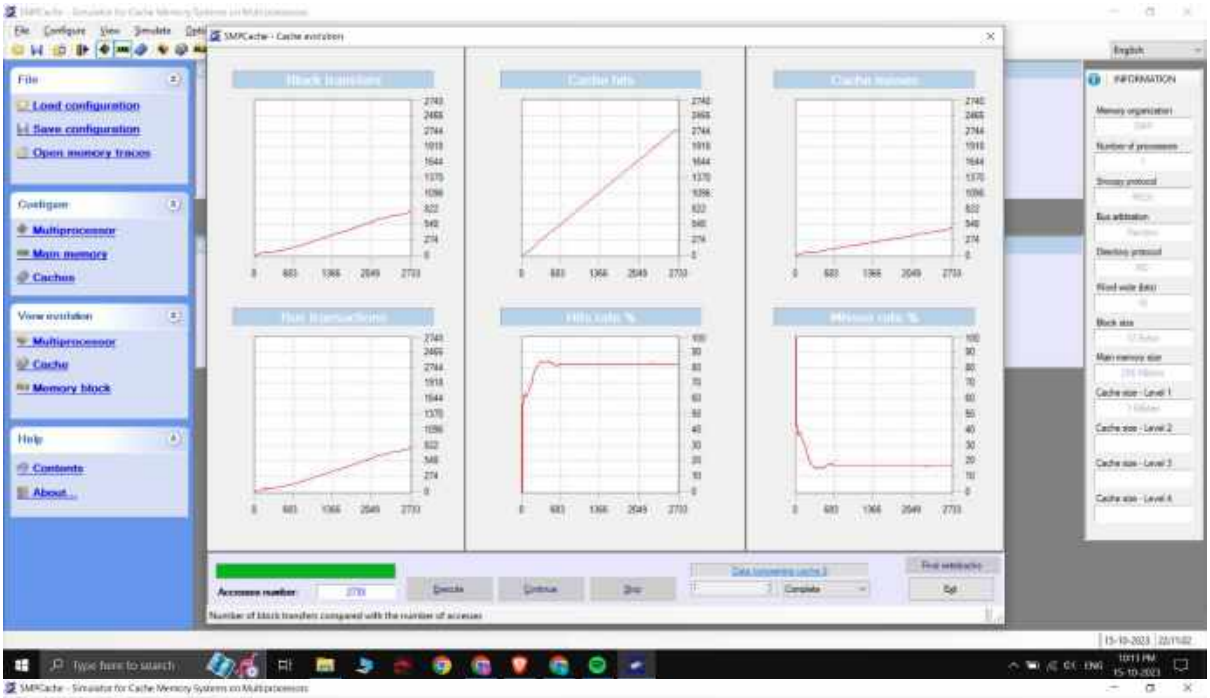
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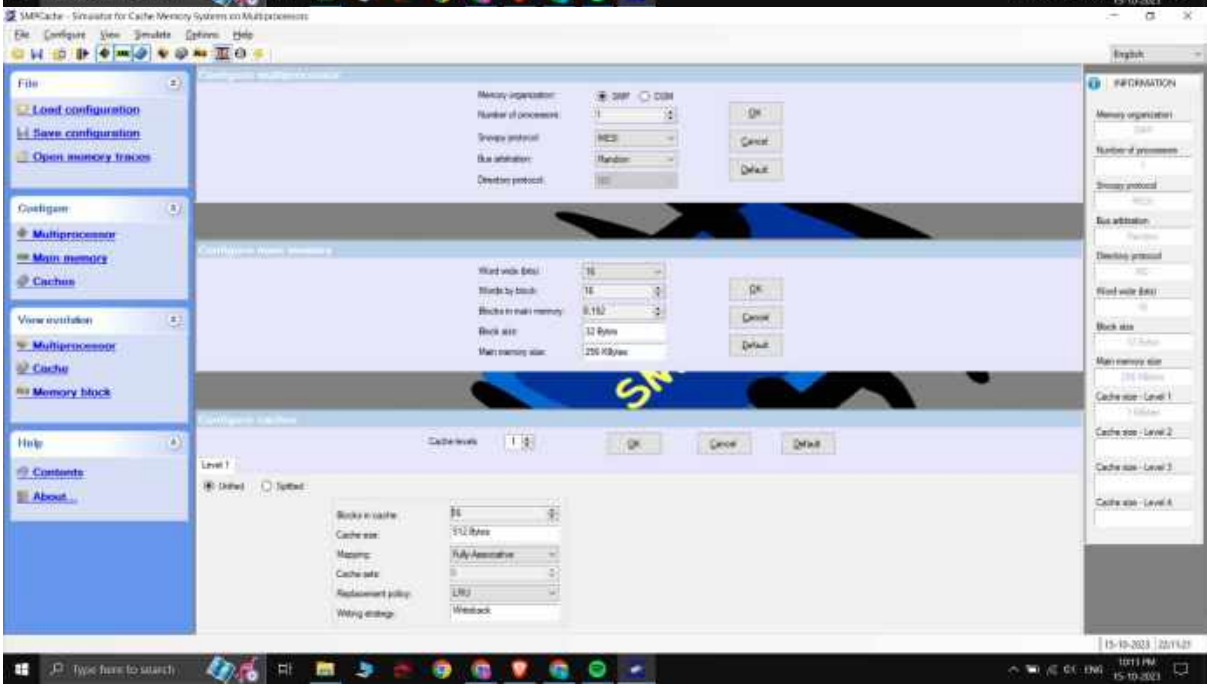
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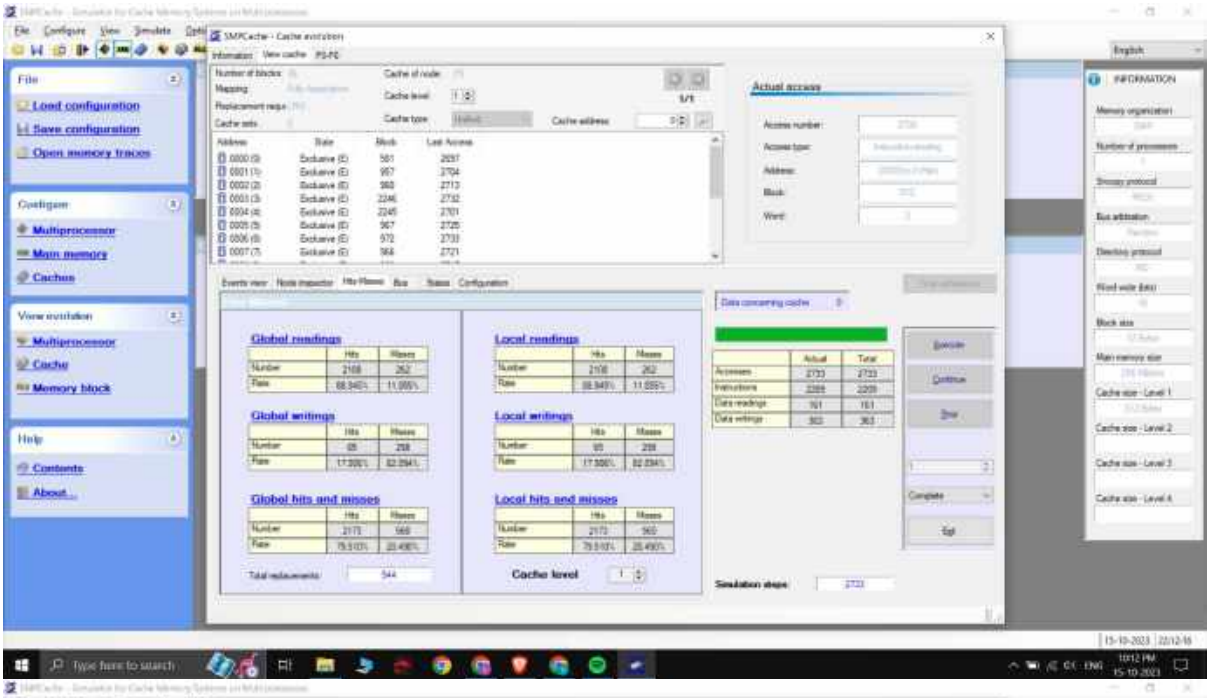
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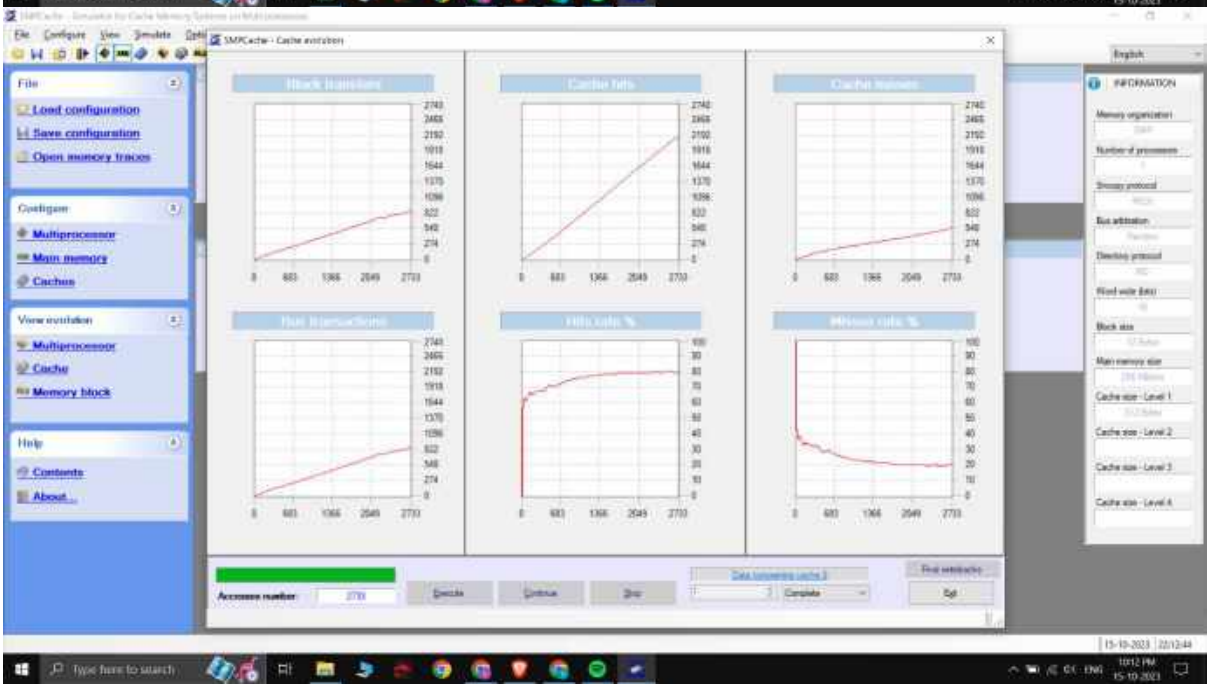
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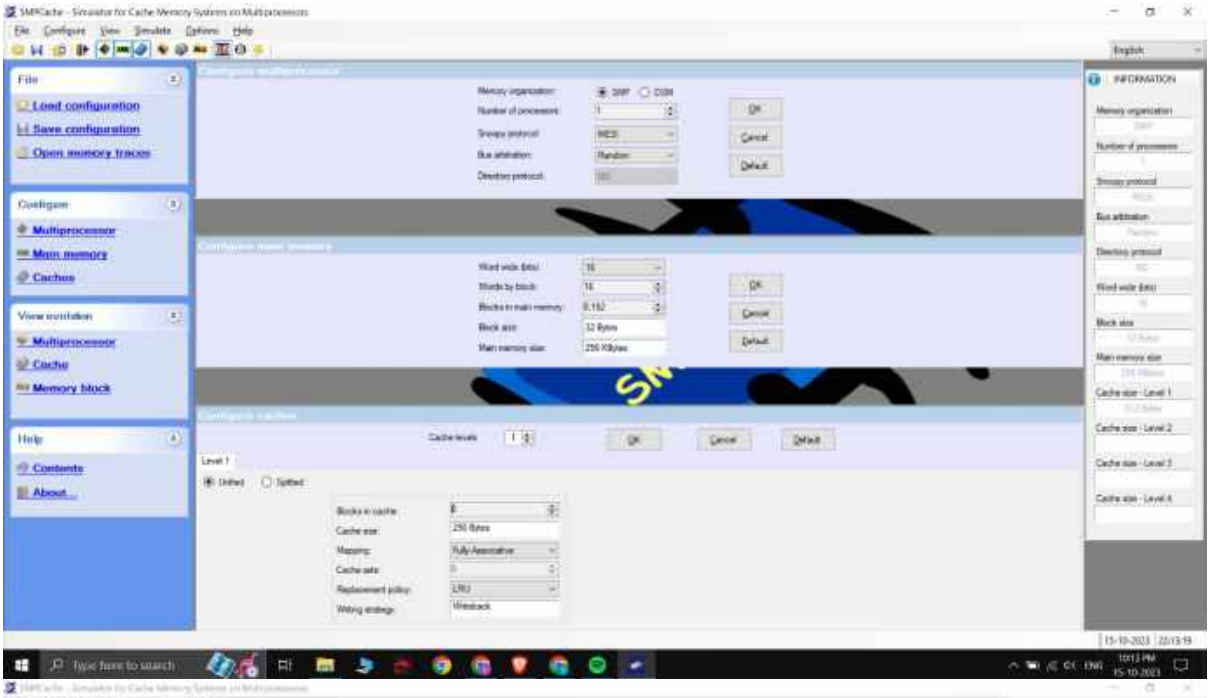
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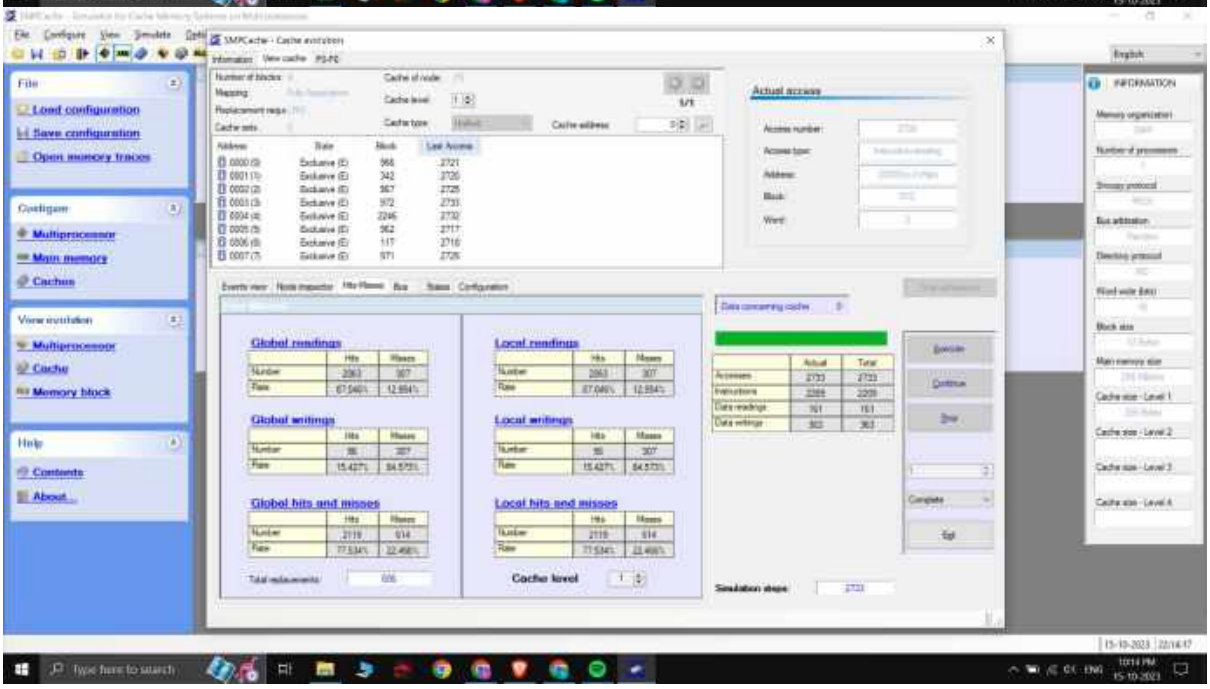
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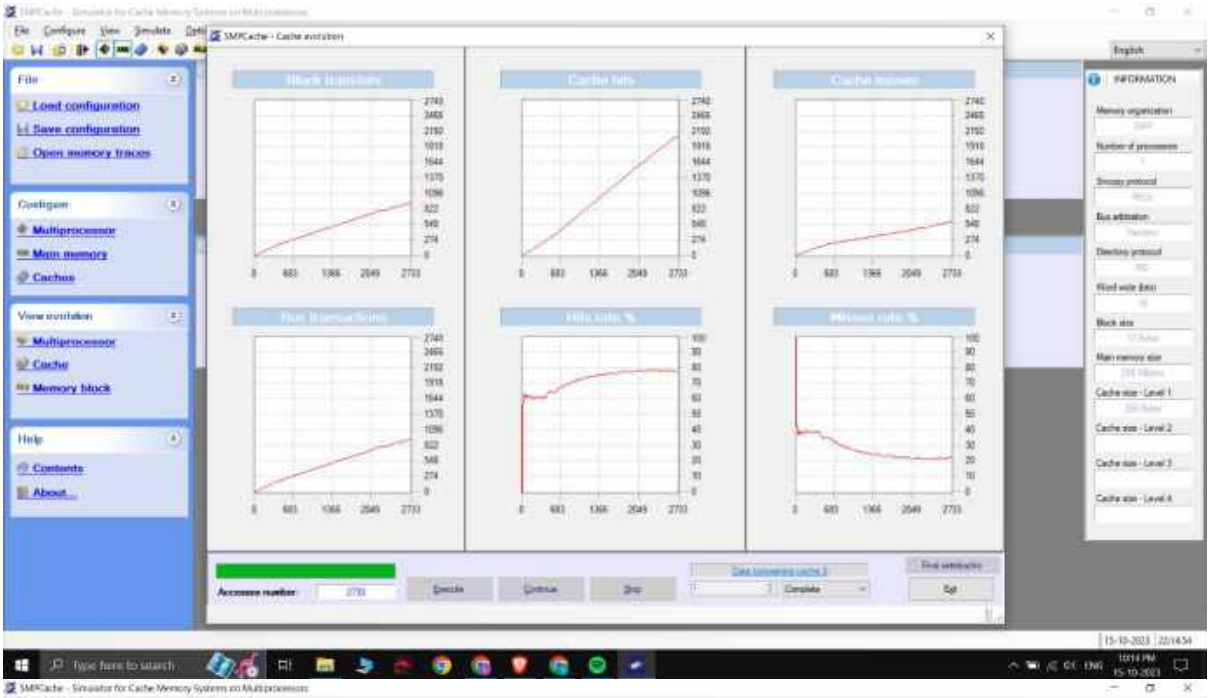
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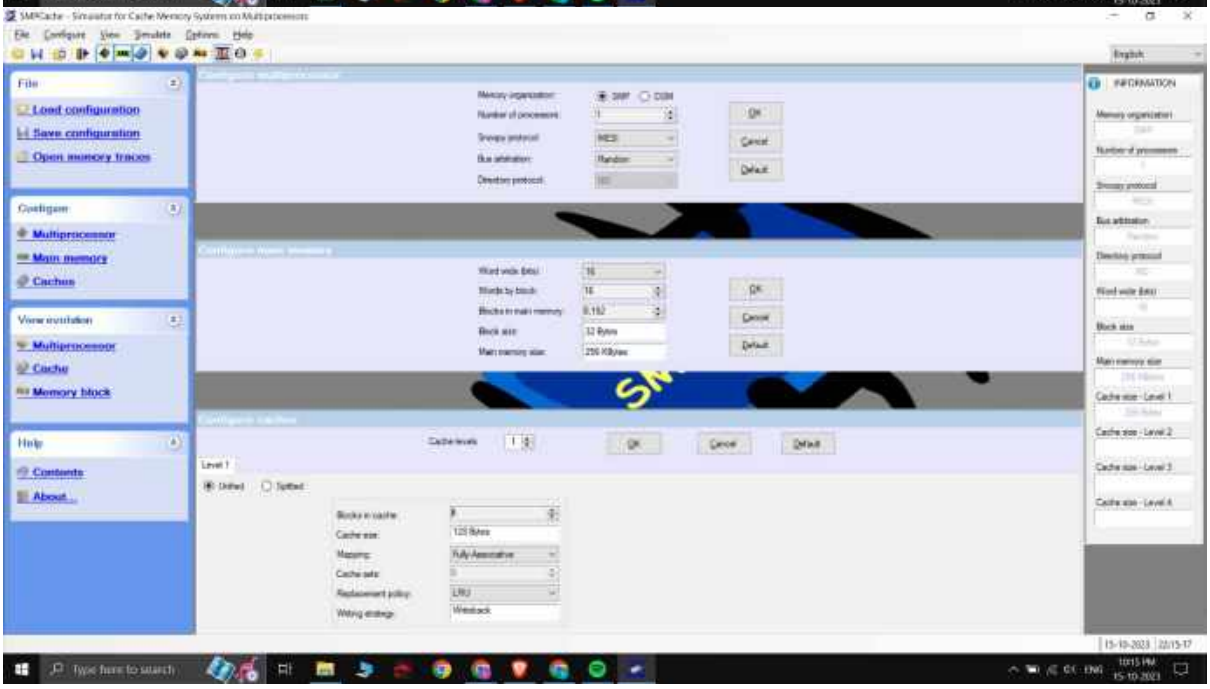
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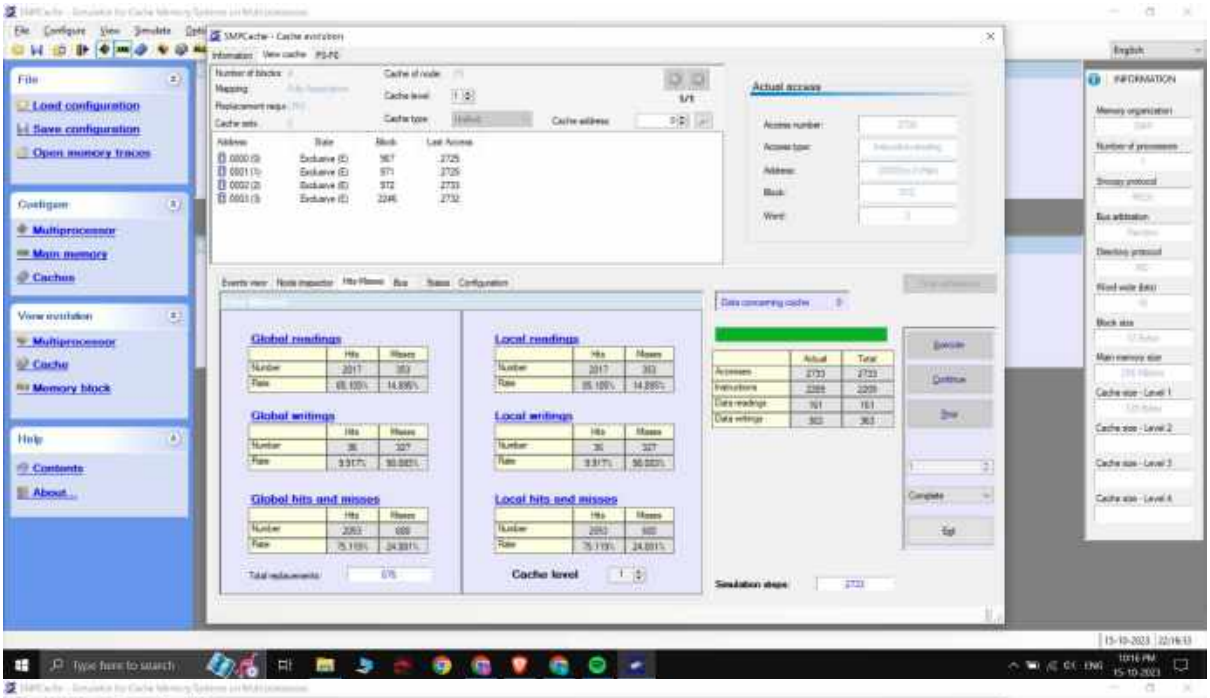
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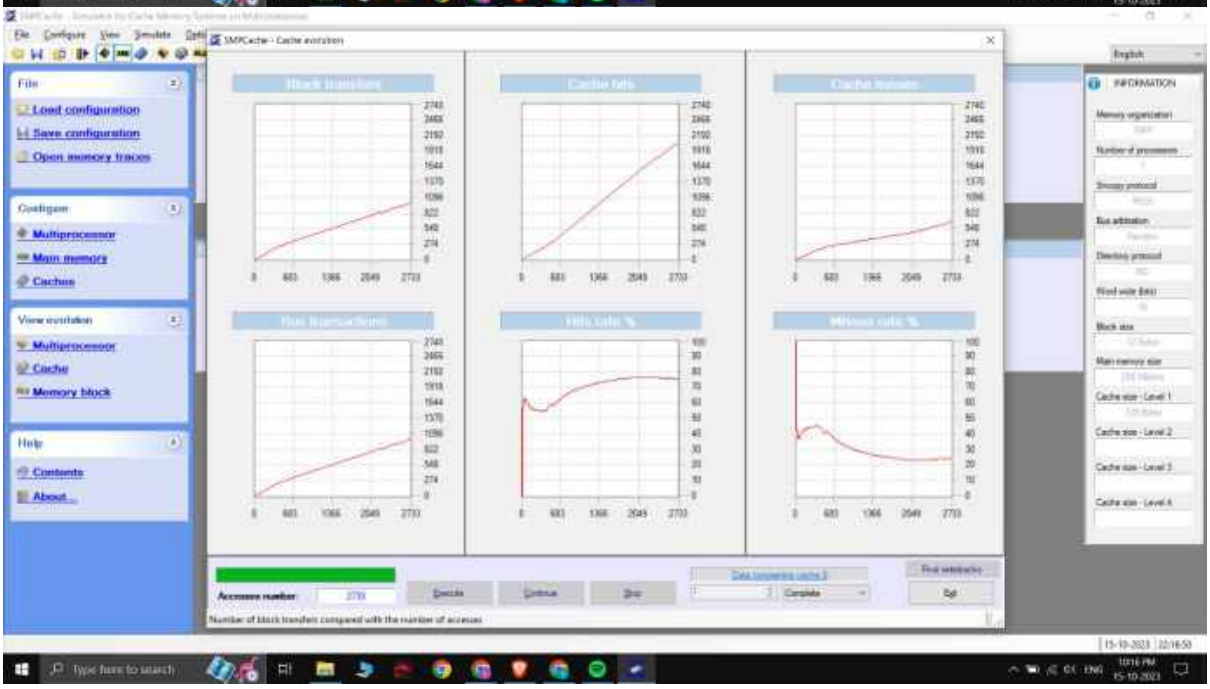
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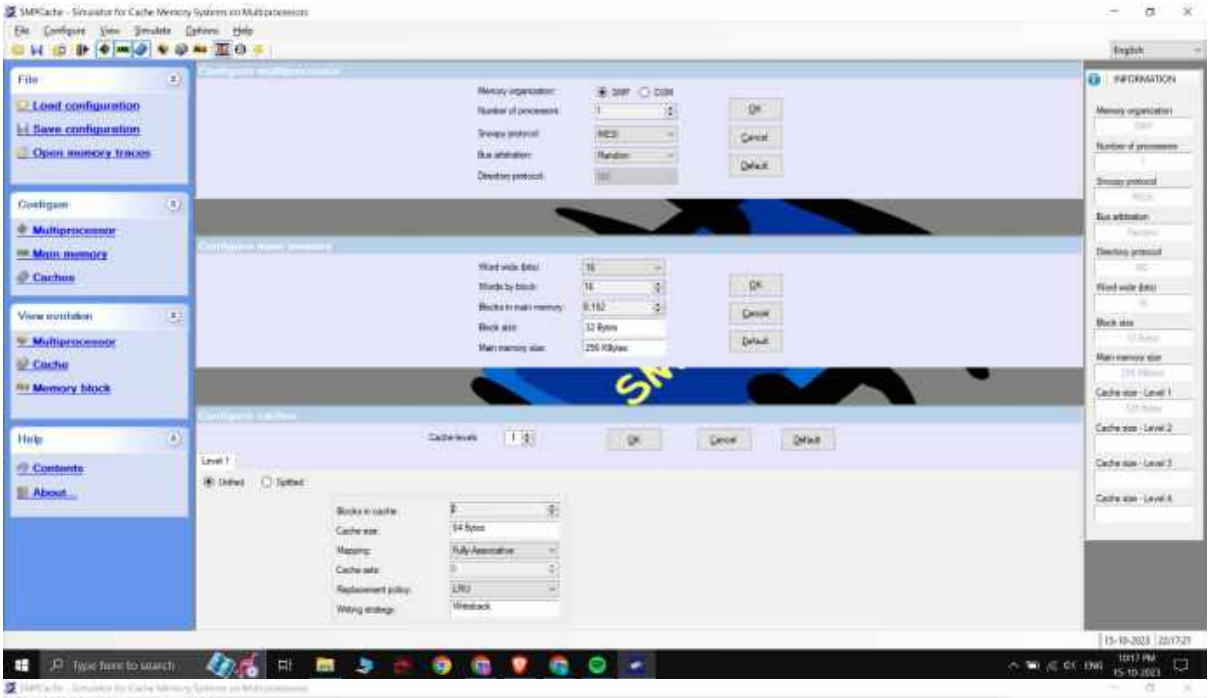
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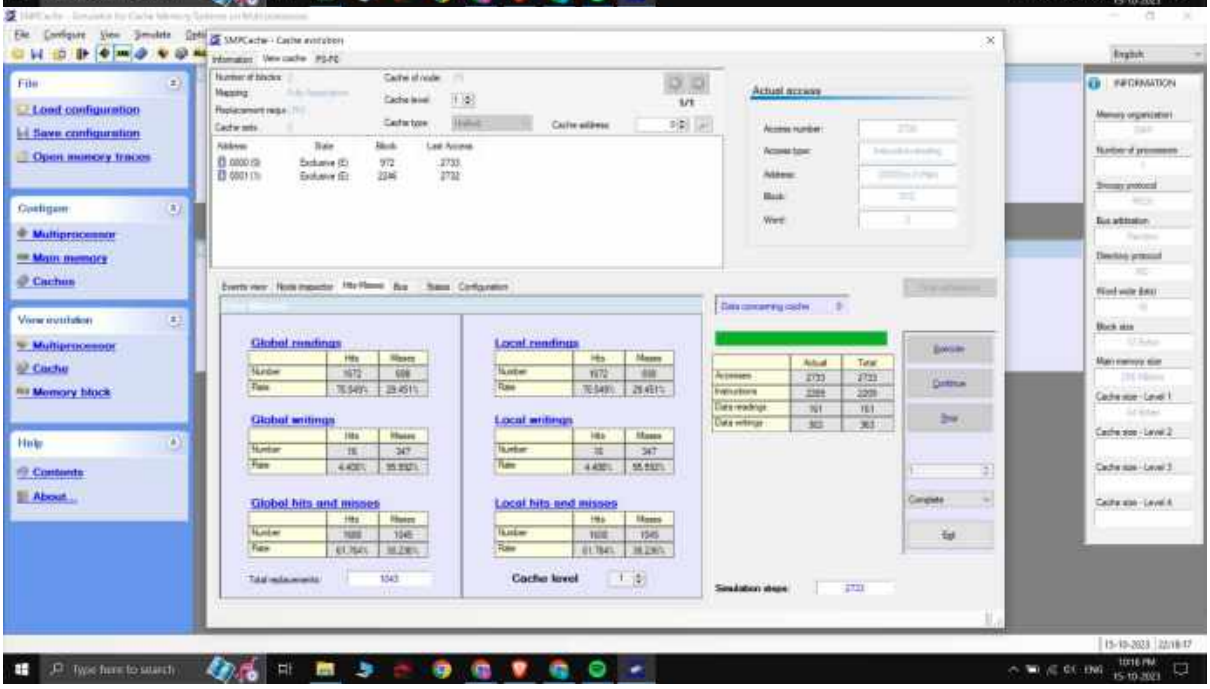
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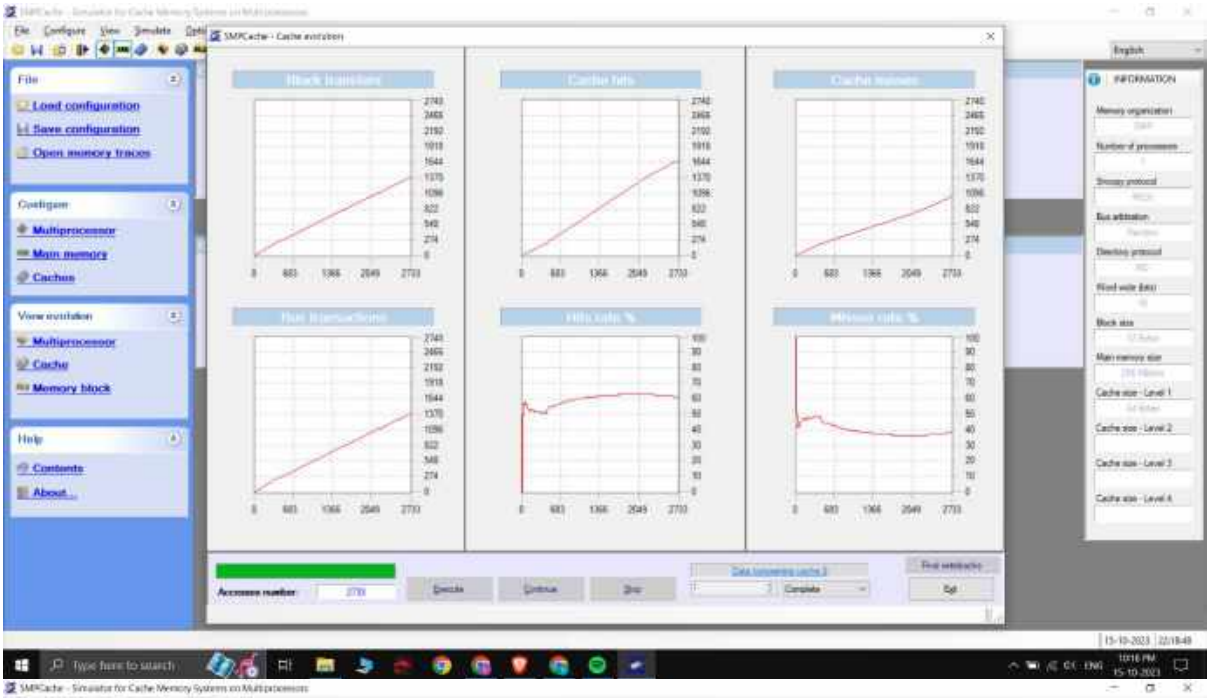
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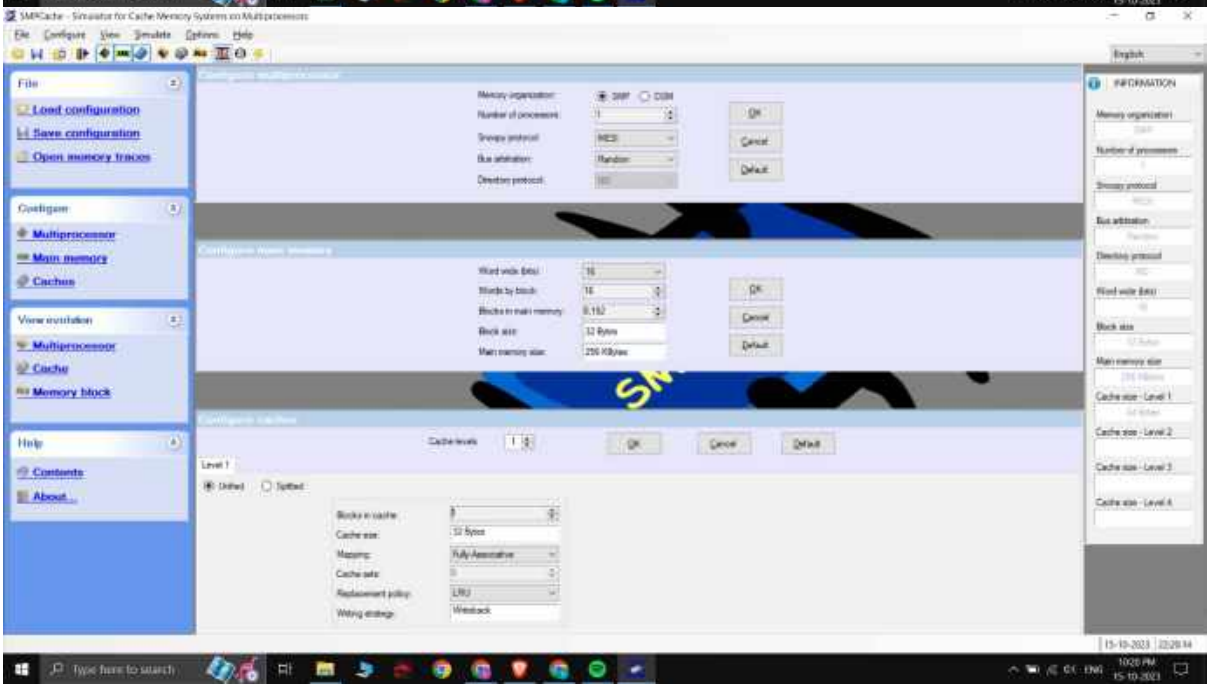
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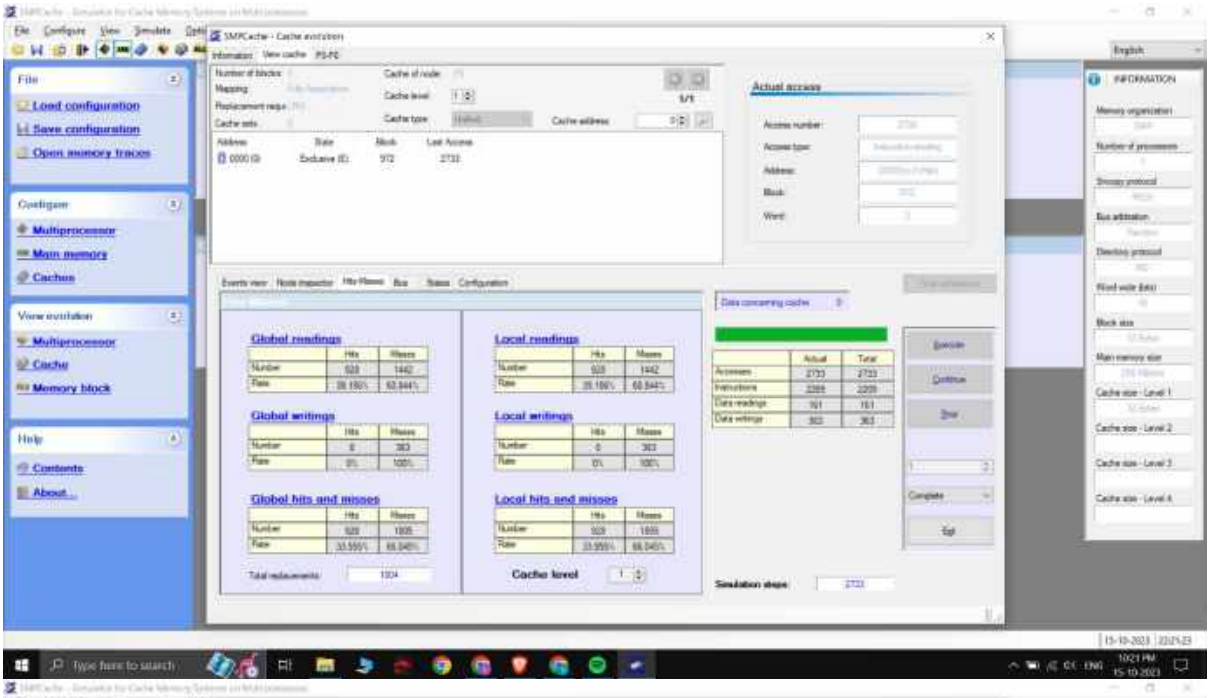
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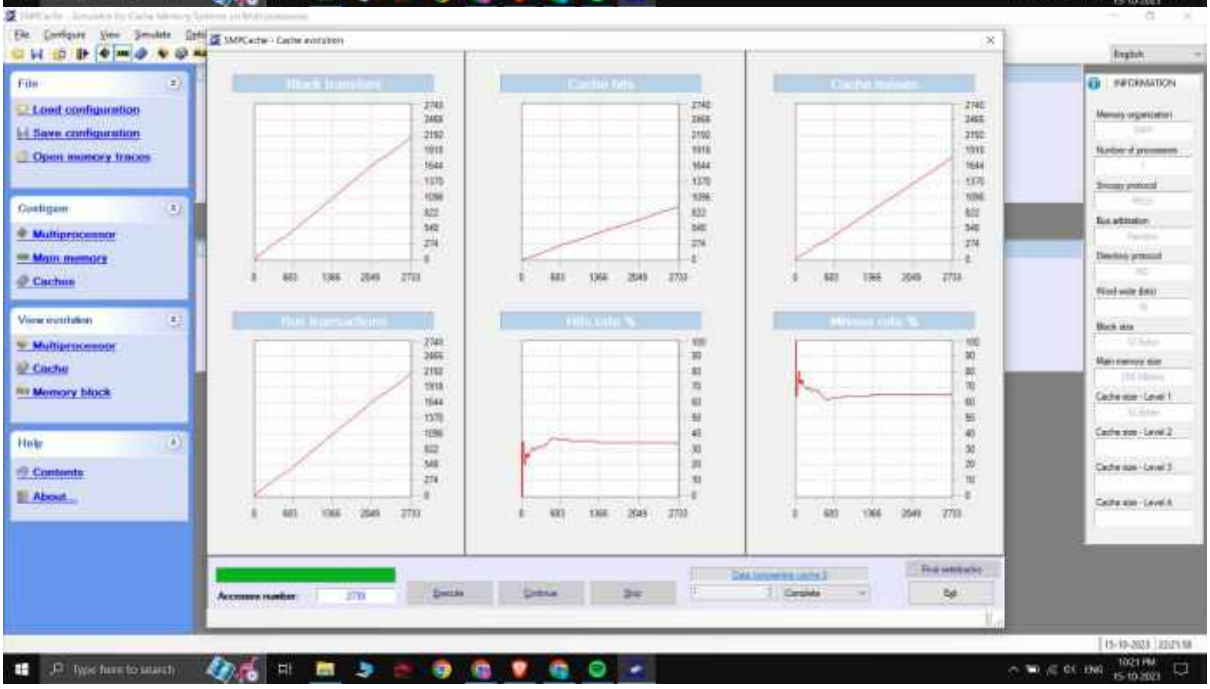
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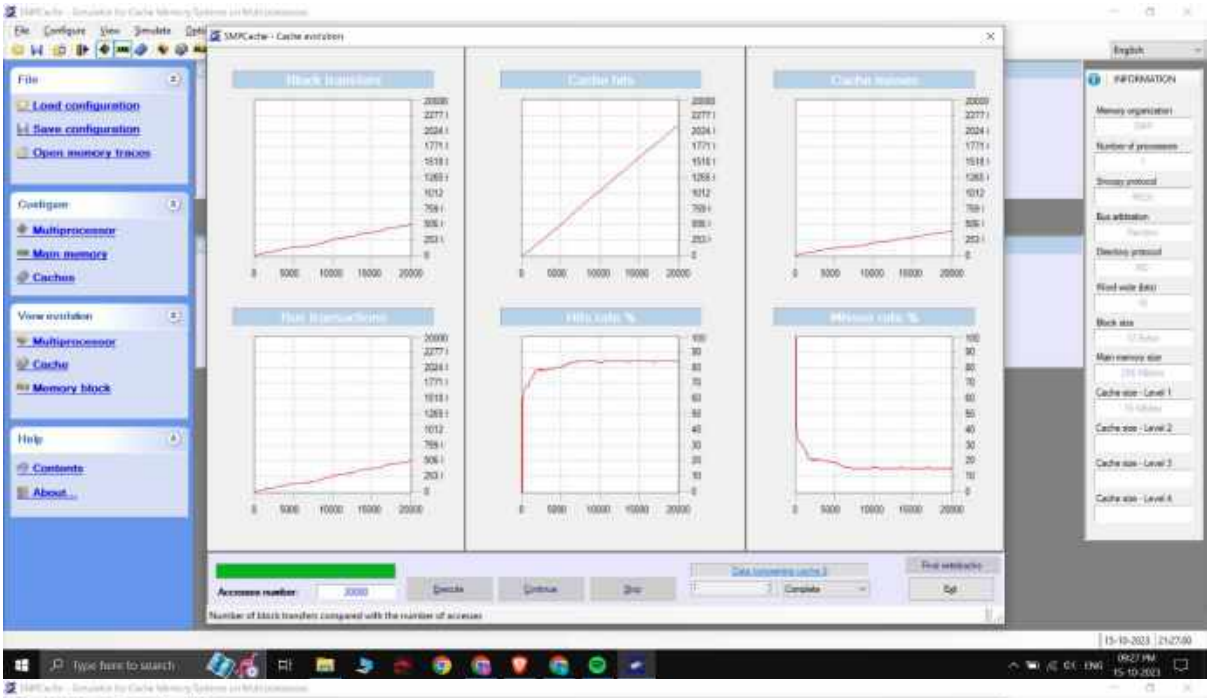
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Misses rate %
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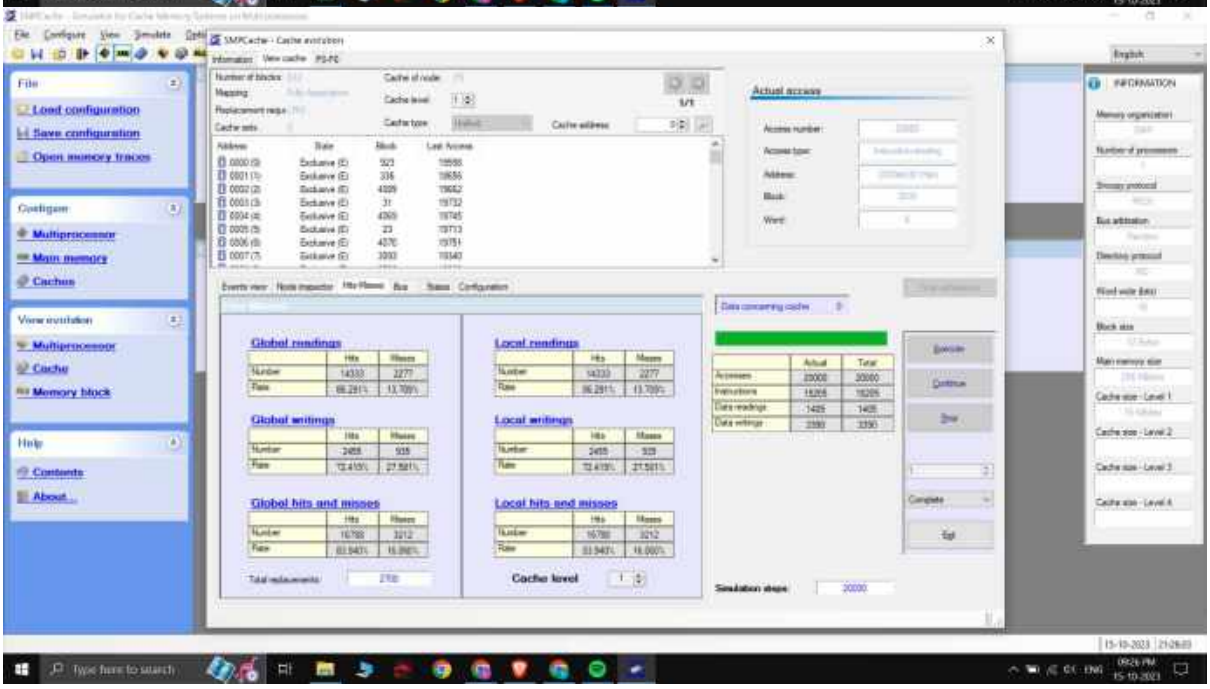
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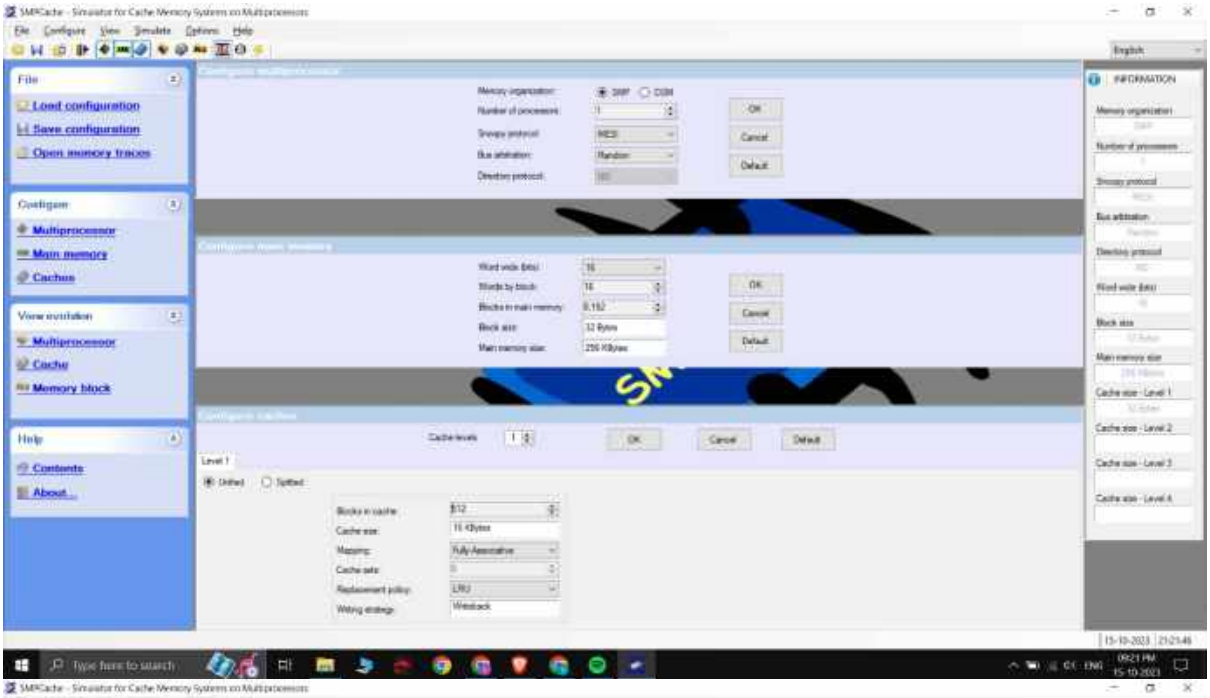
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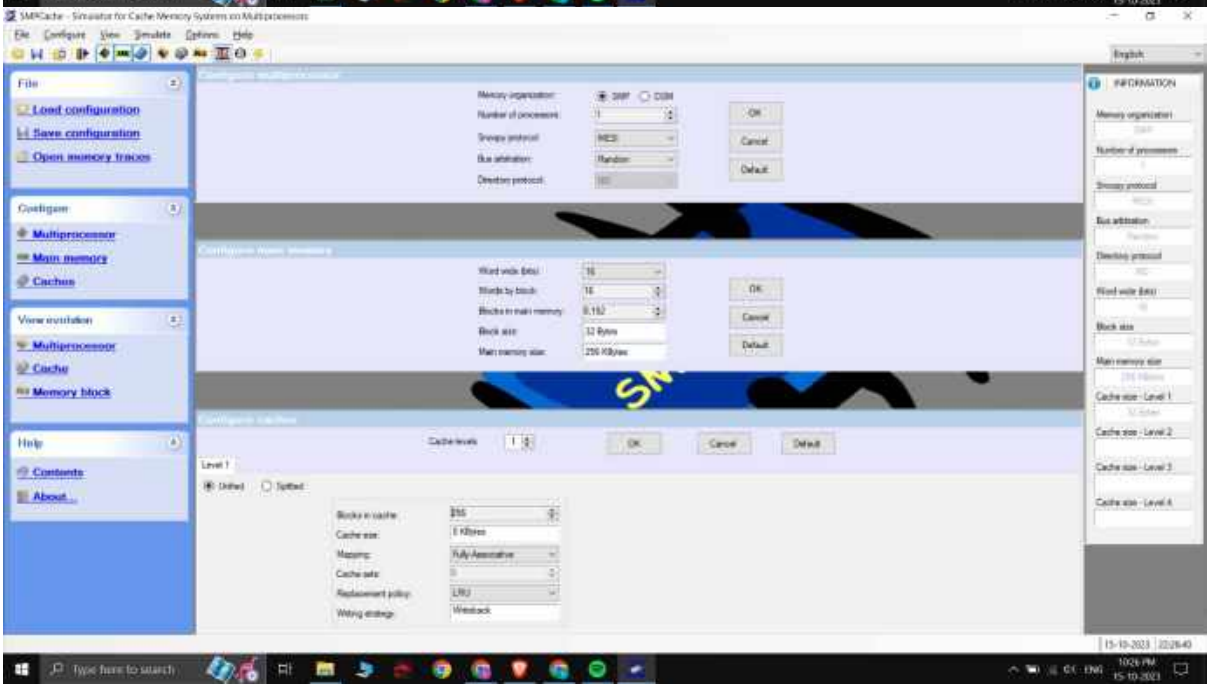
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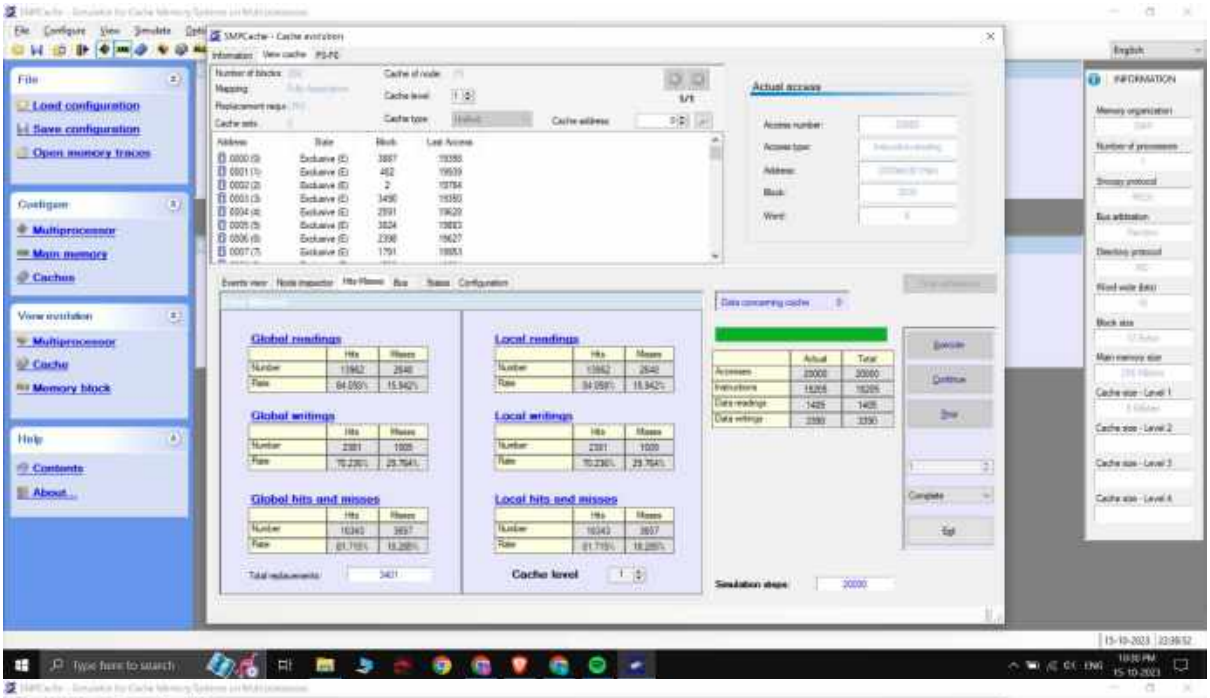
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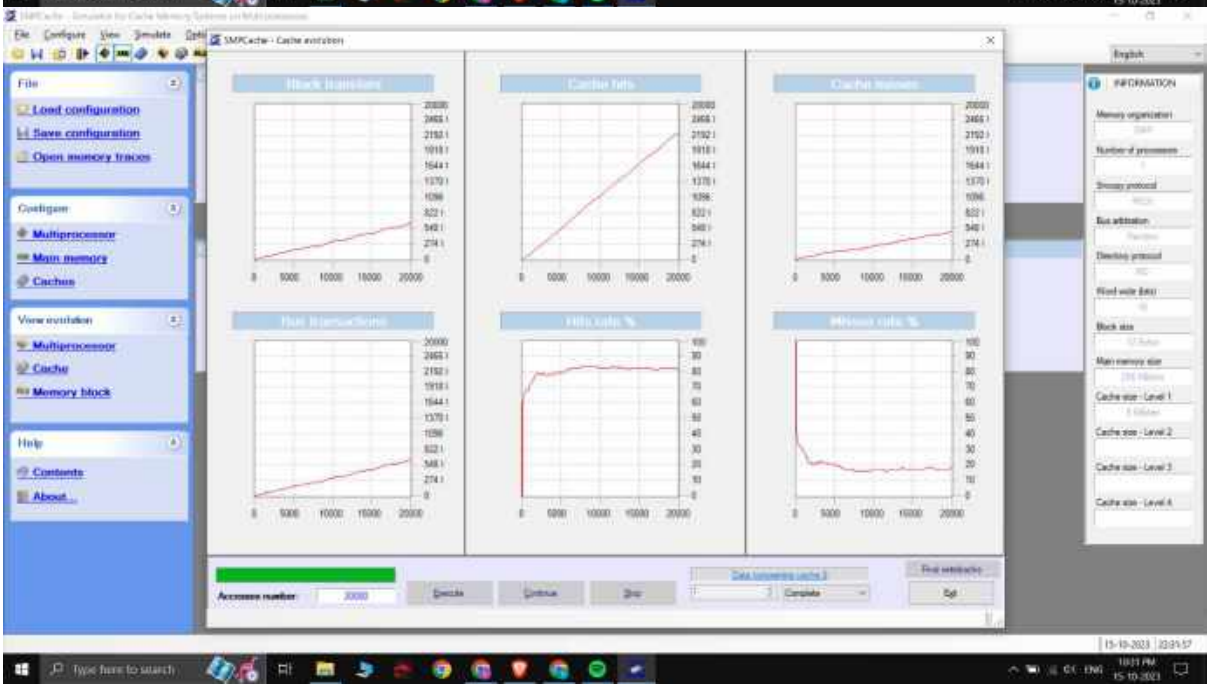
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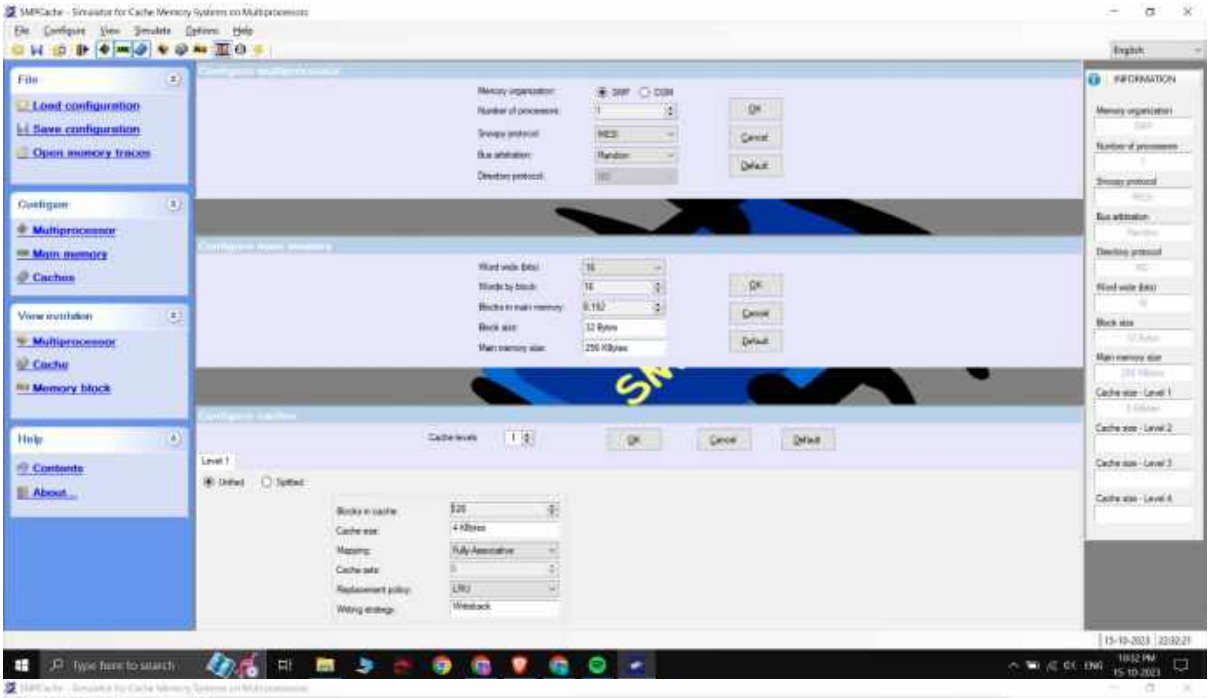
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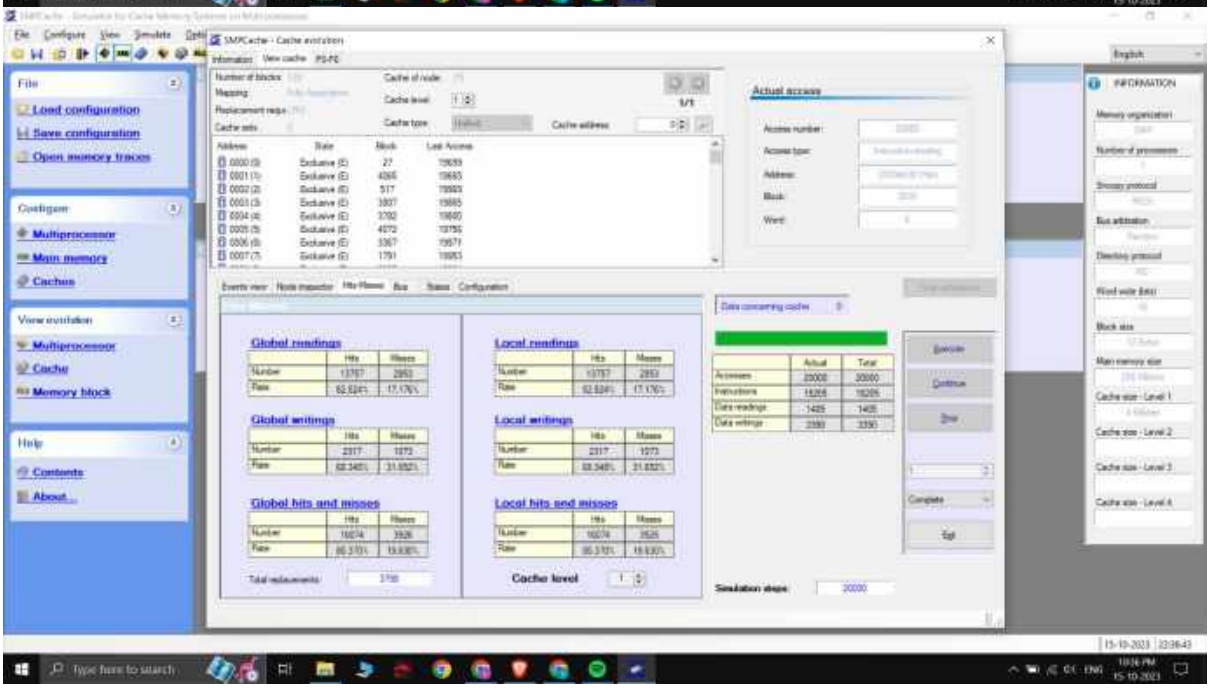
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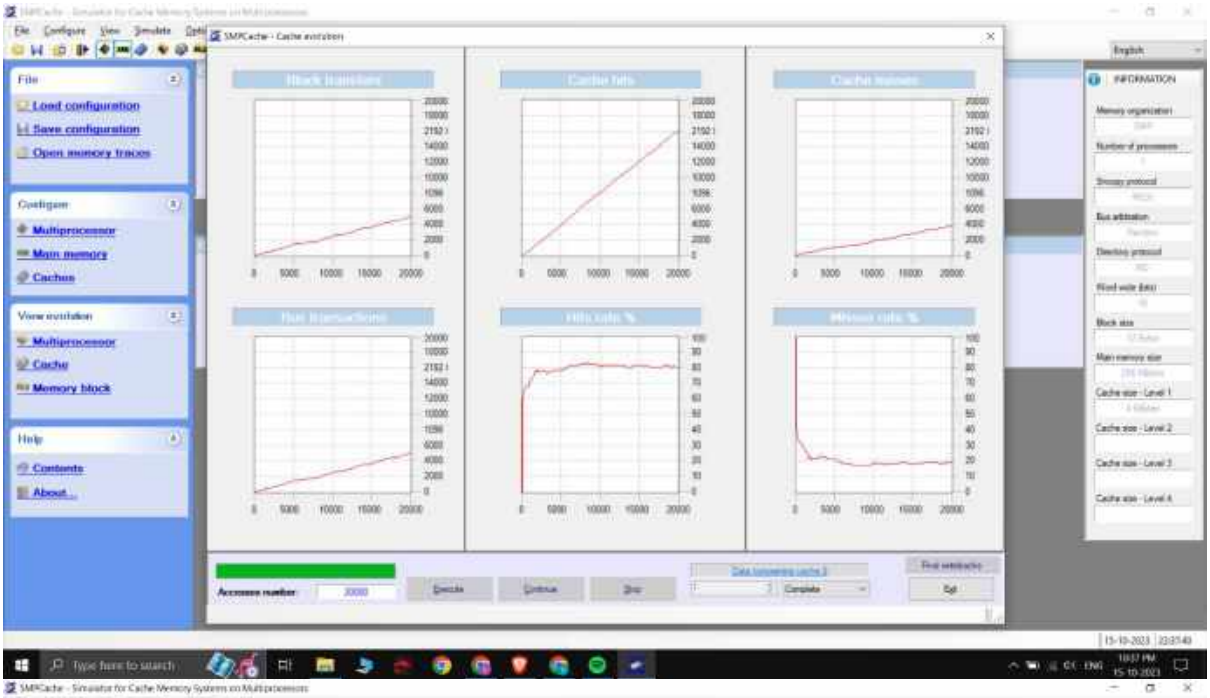
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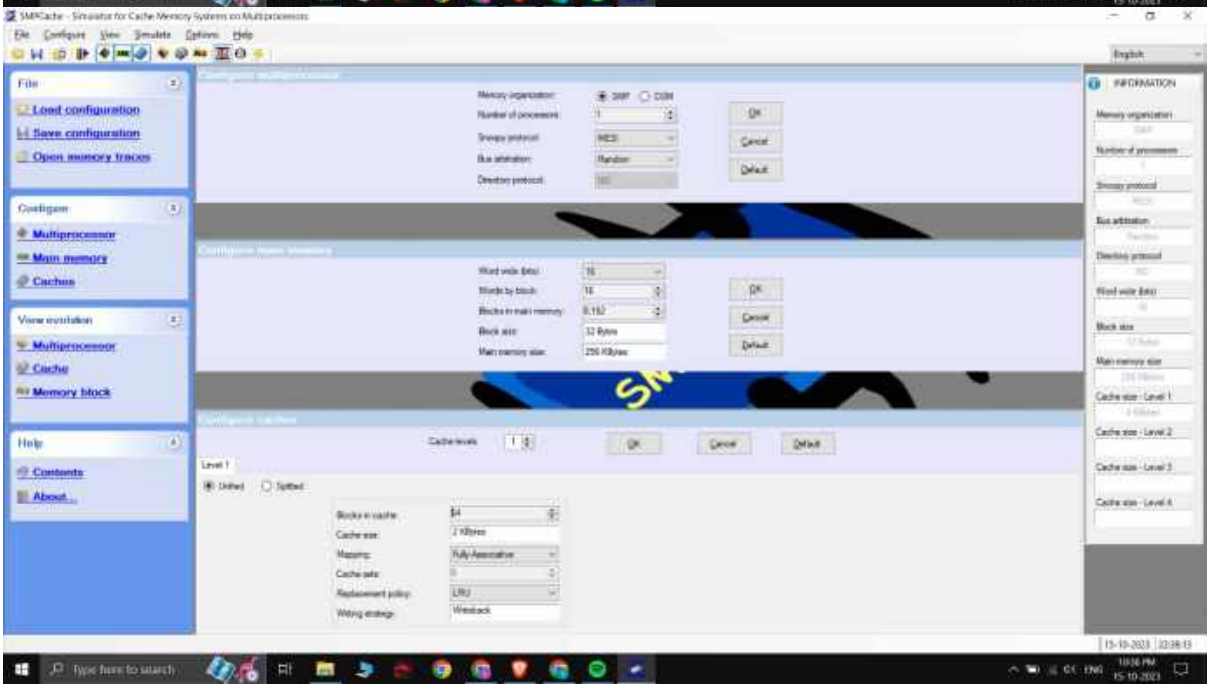
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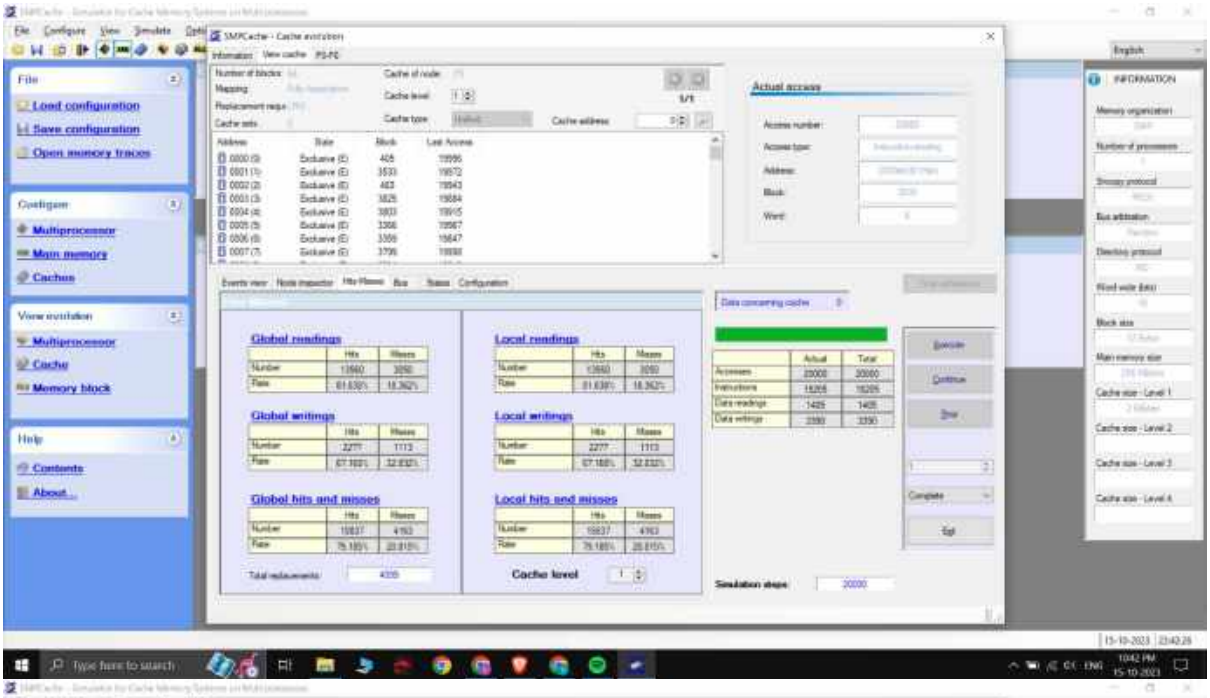
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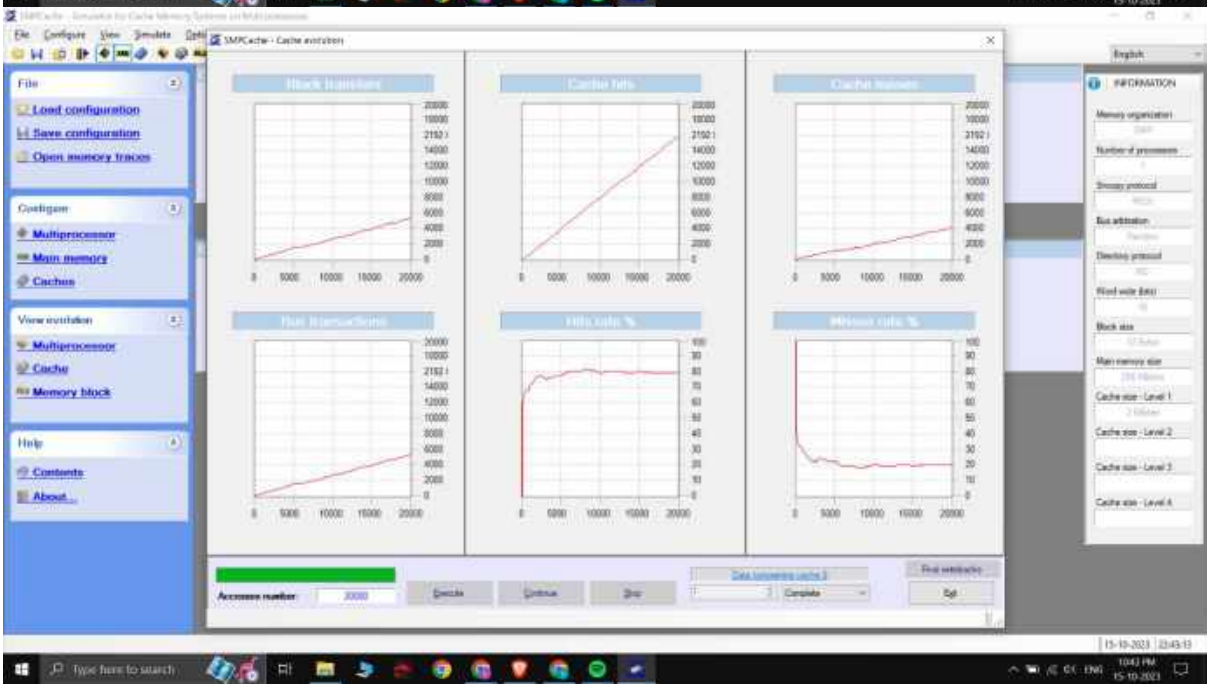
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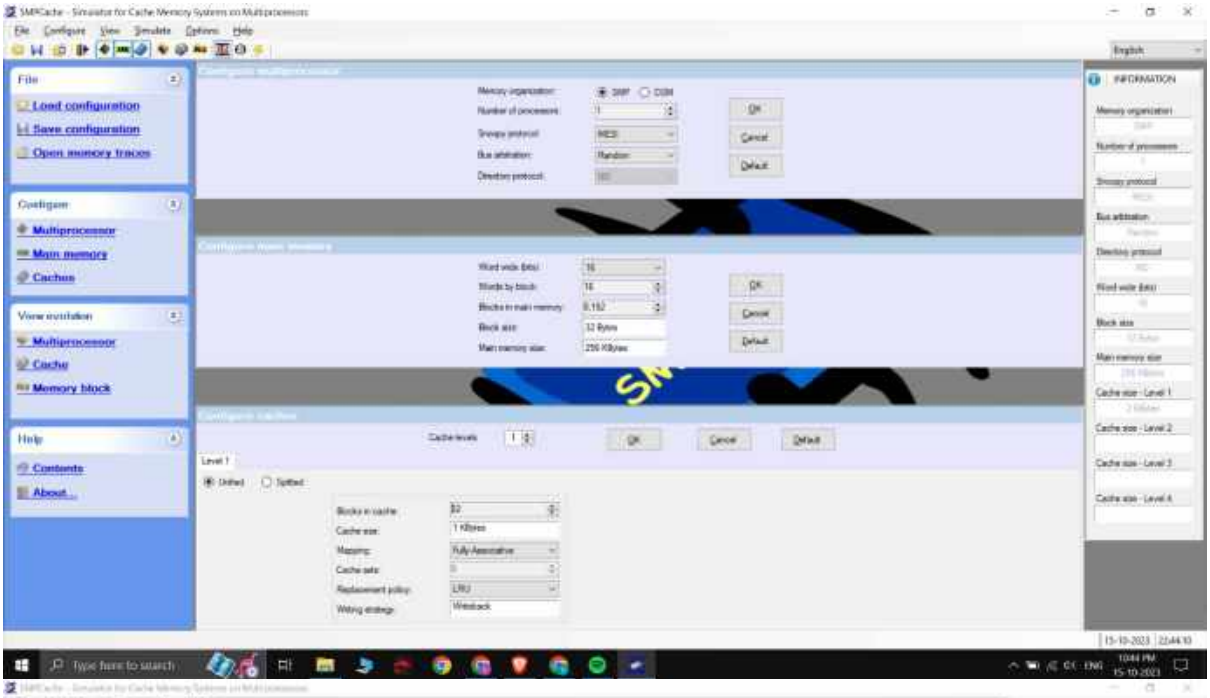
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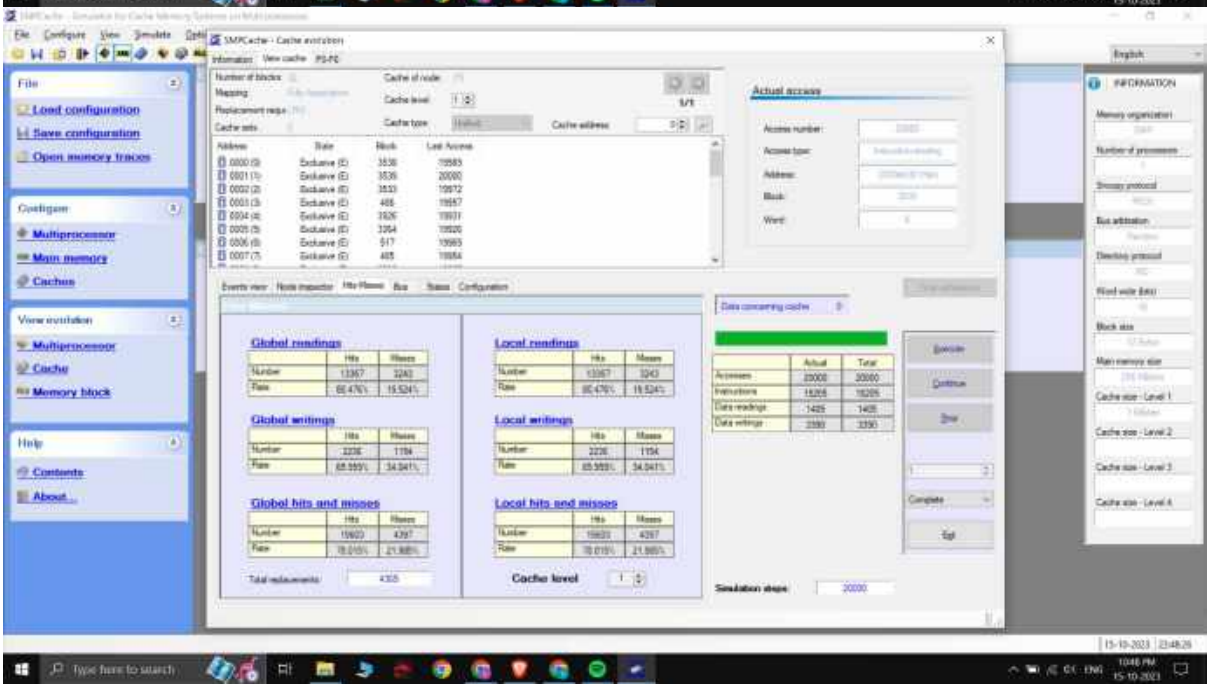
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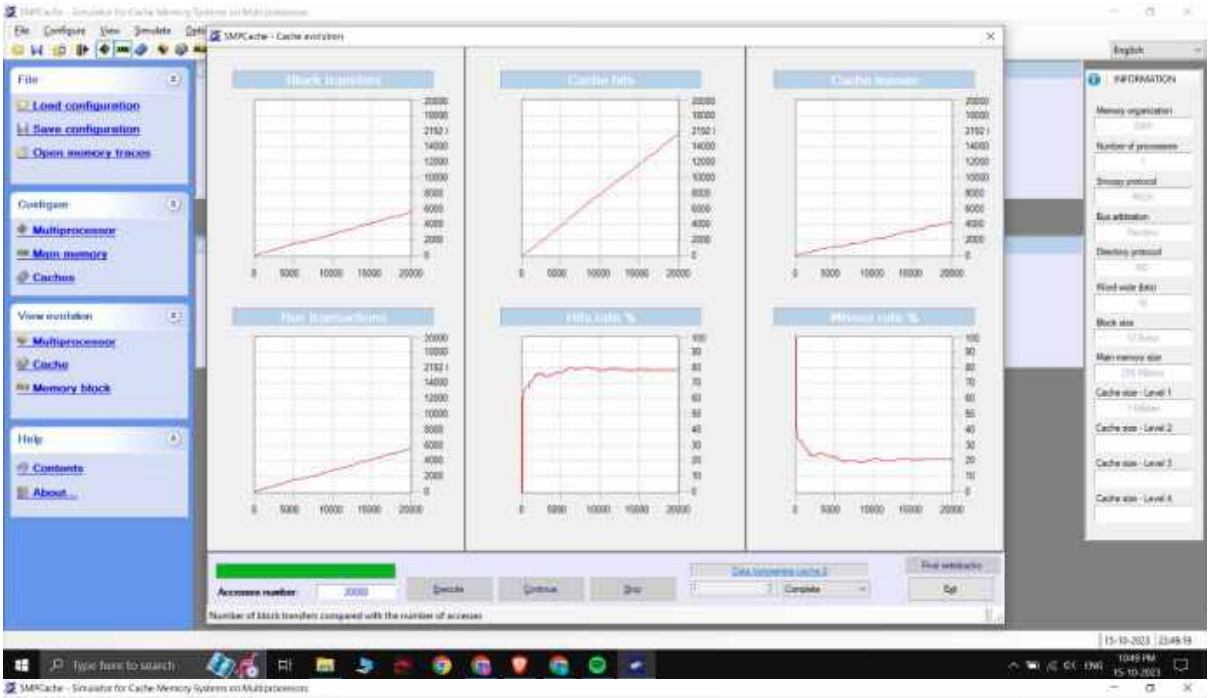
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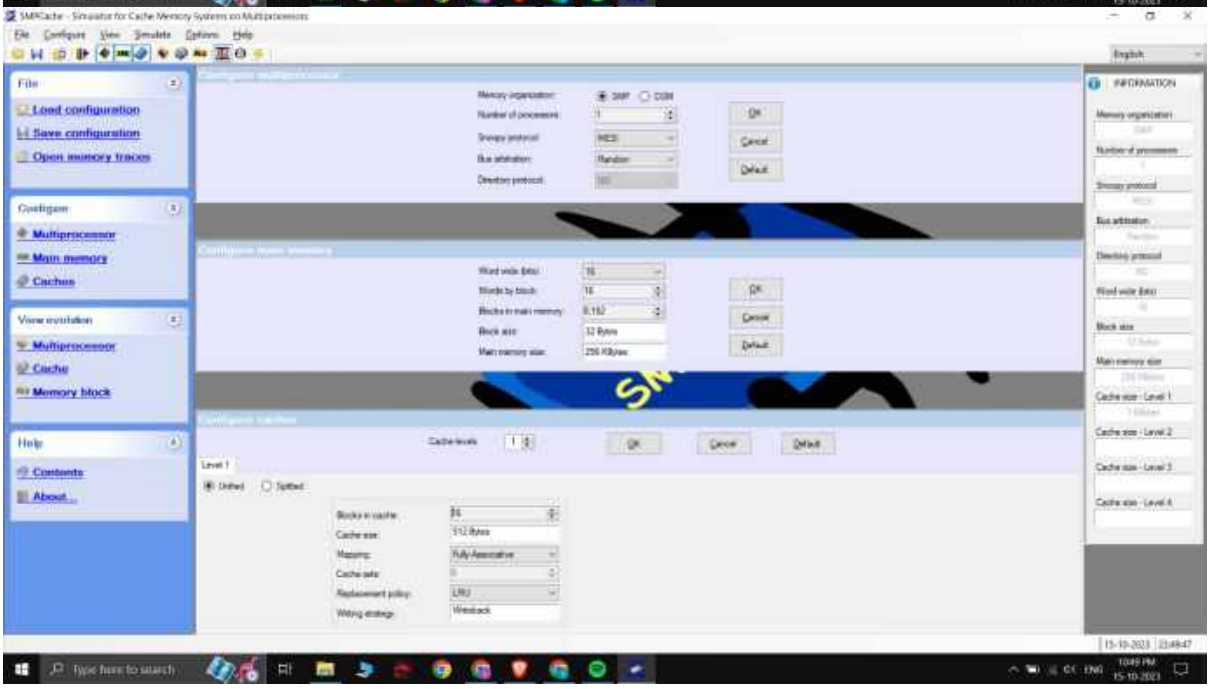
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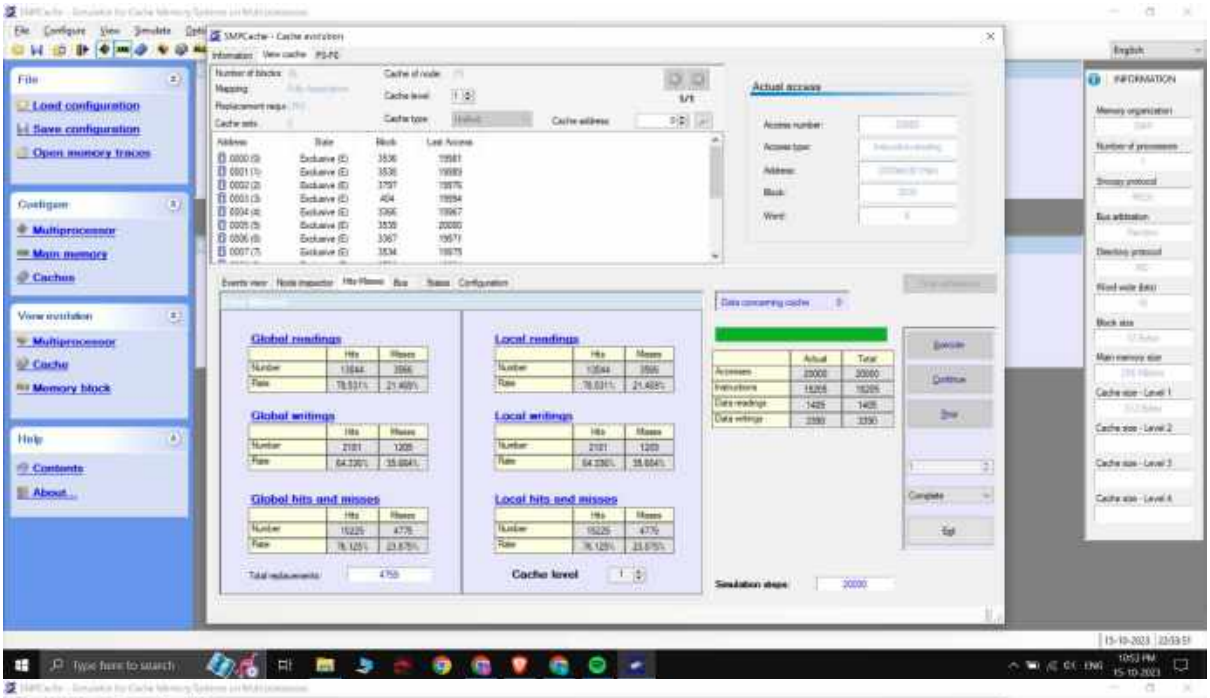
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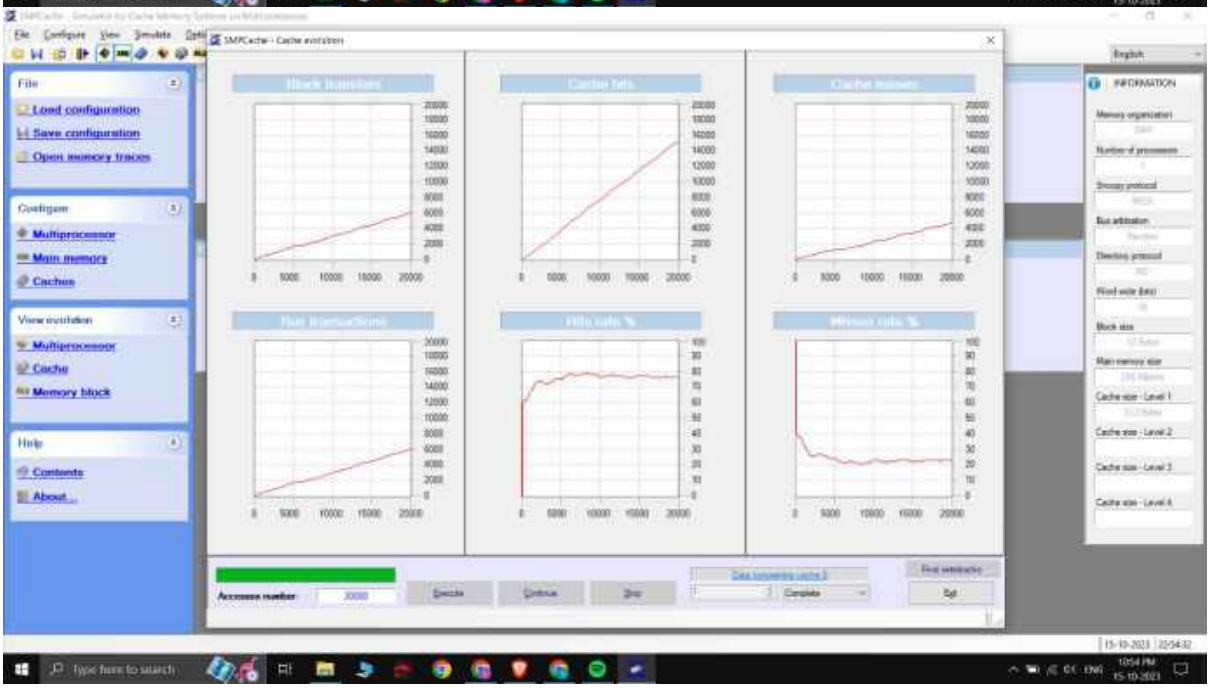
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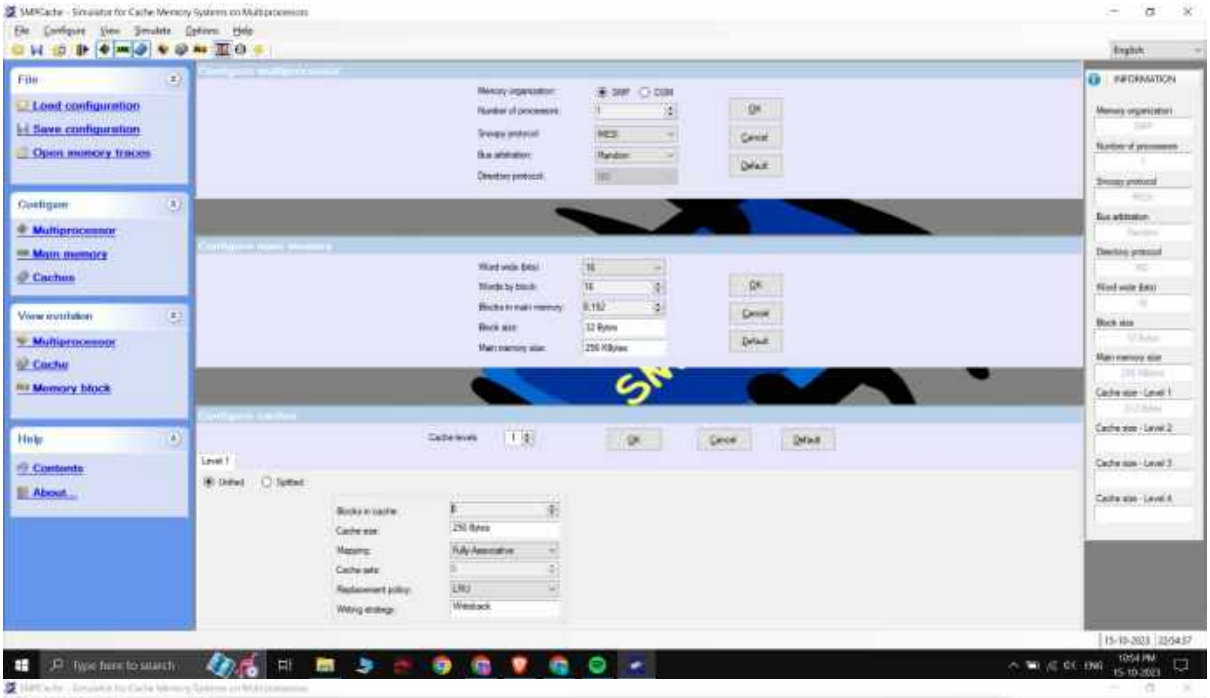
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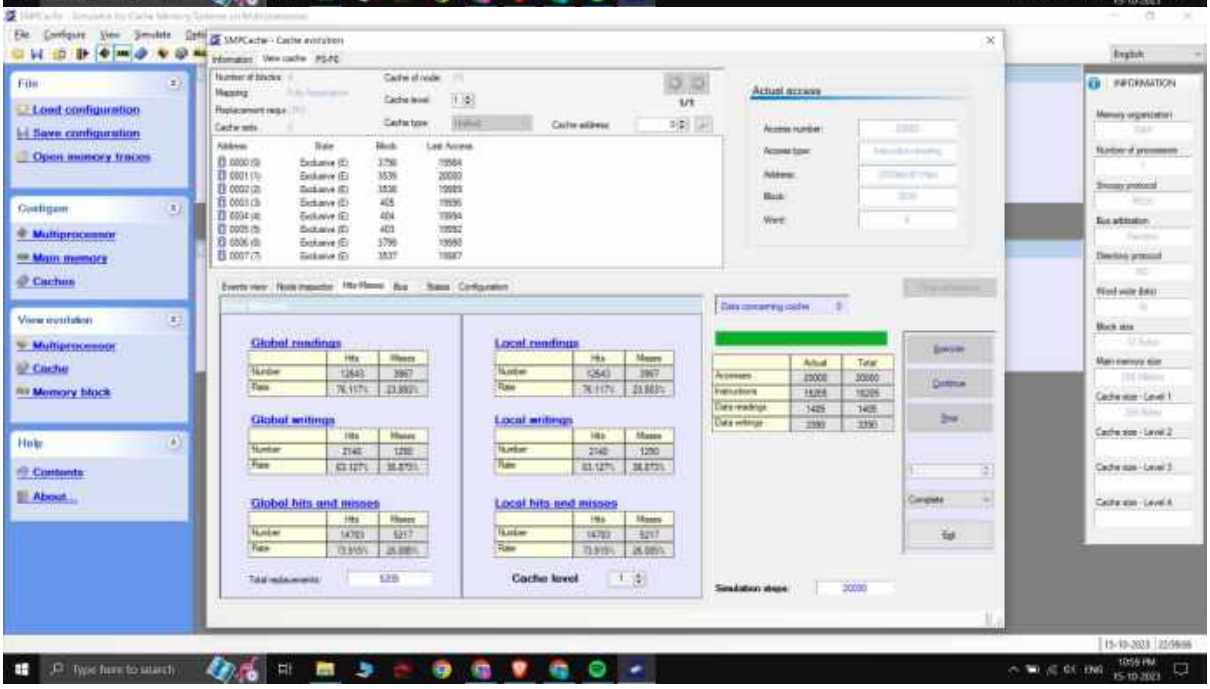
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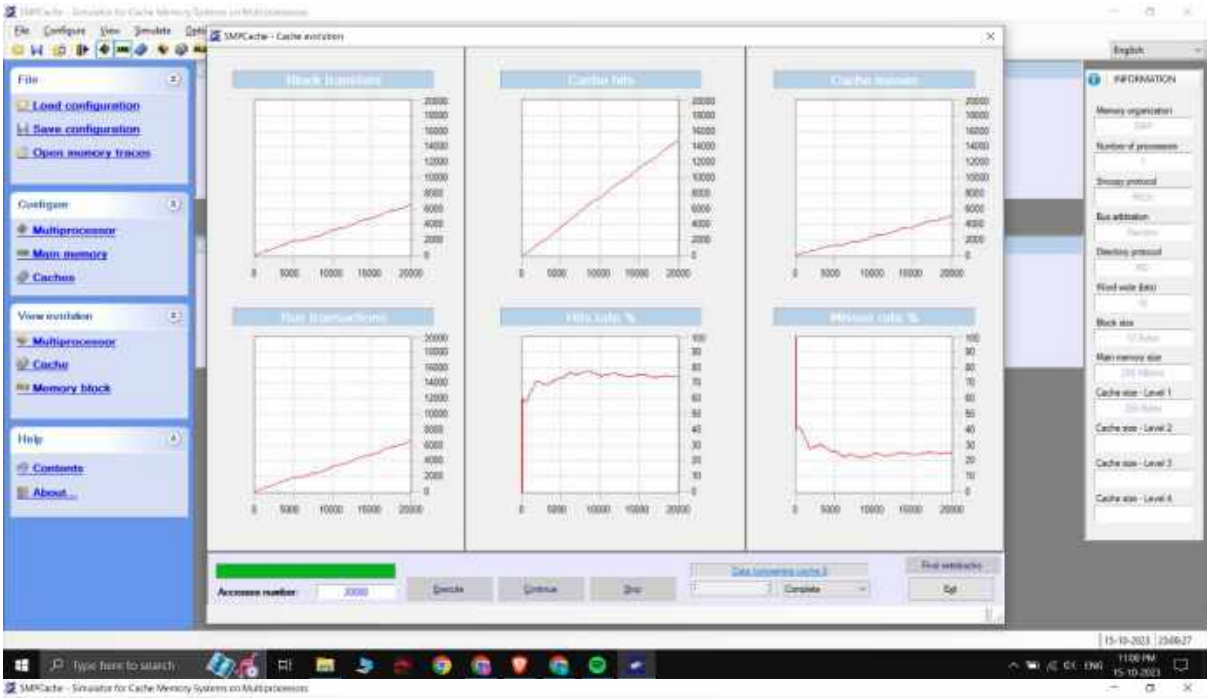
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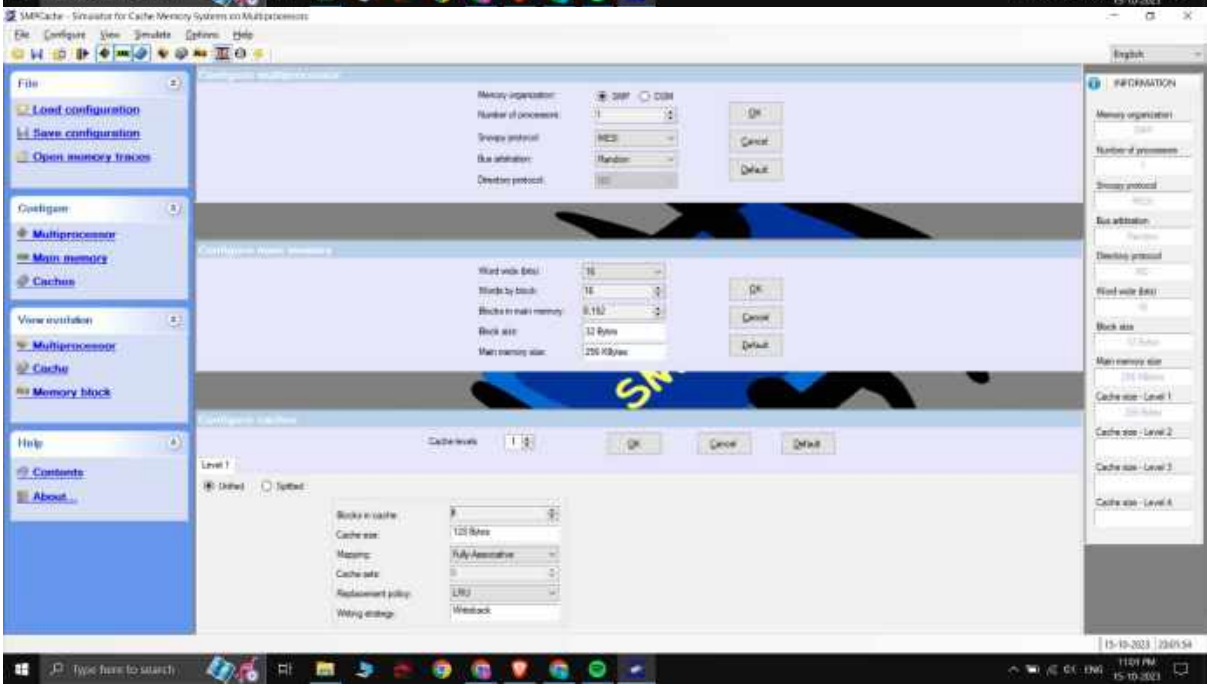
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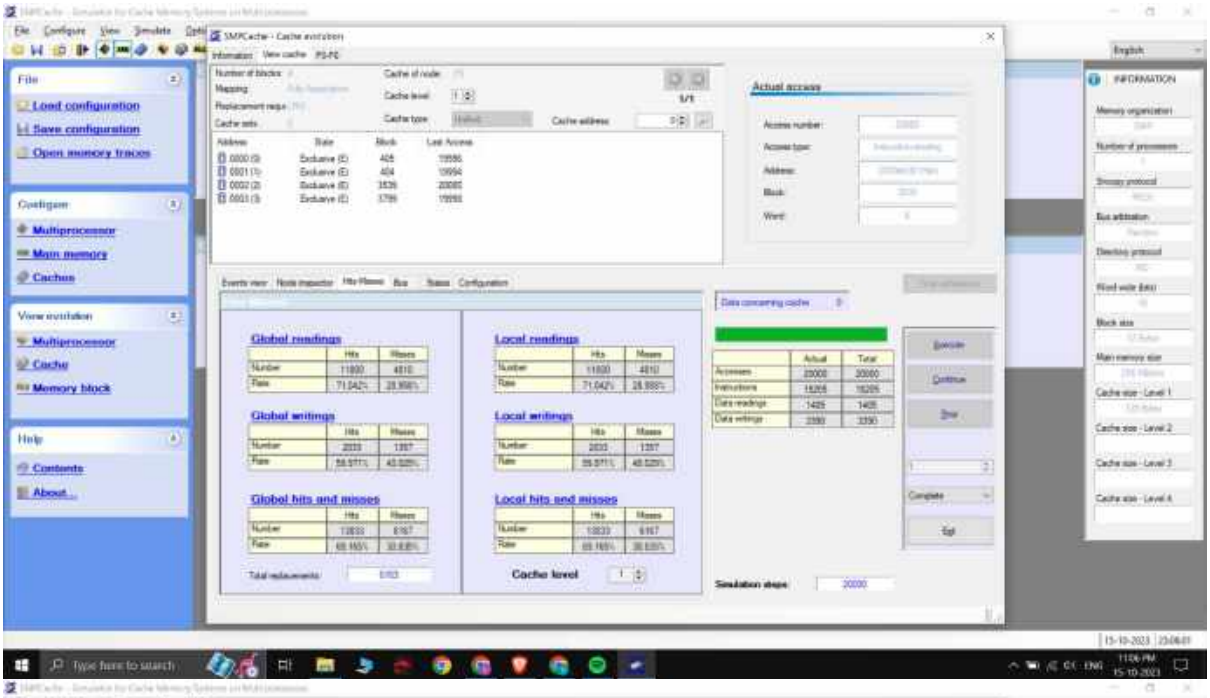
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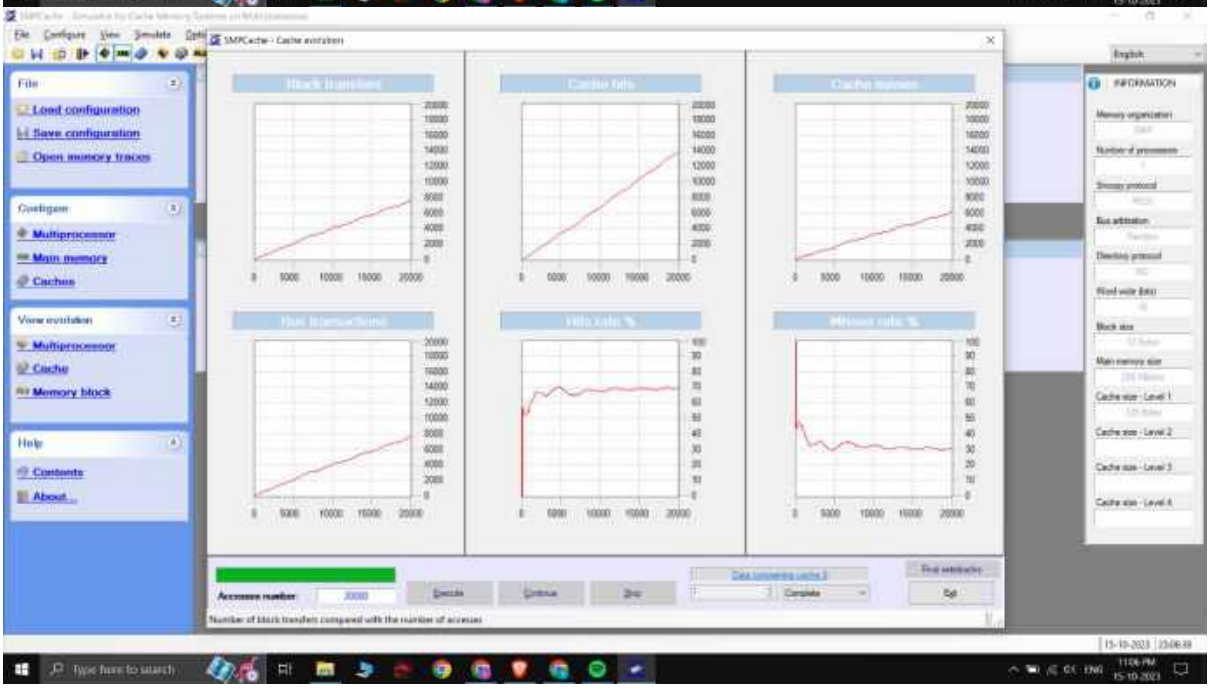
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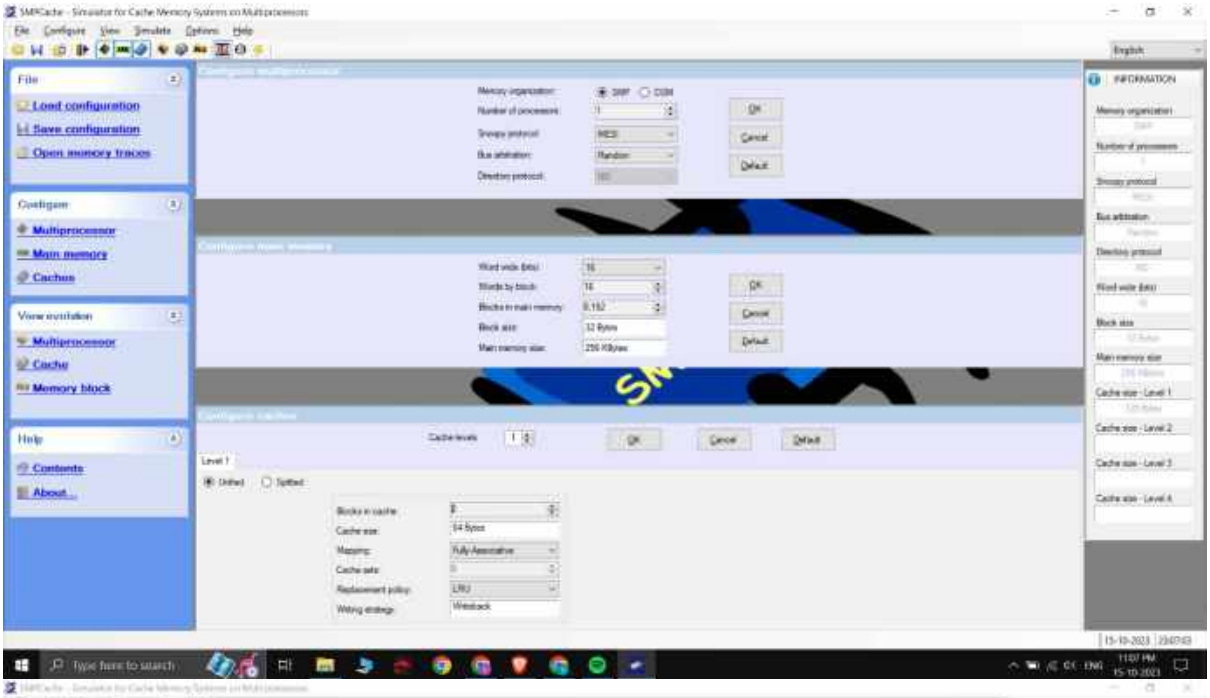
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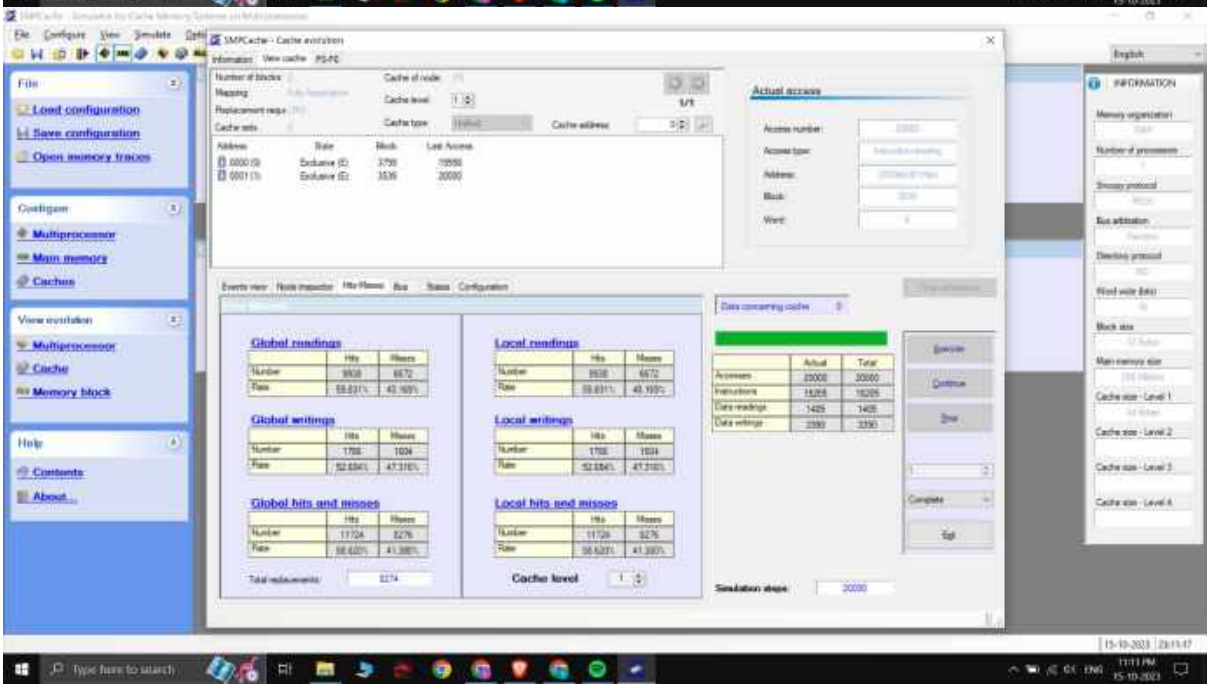
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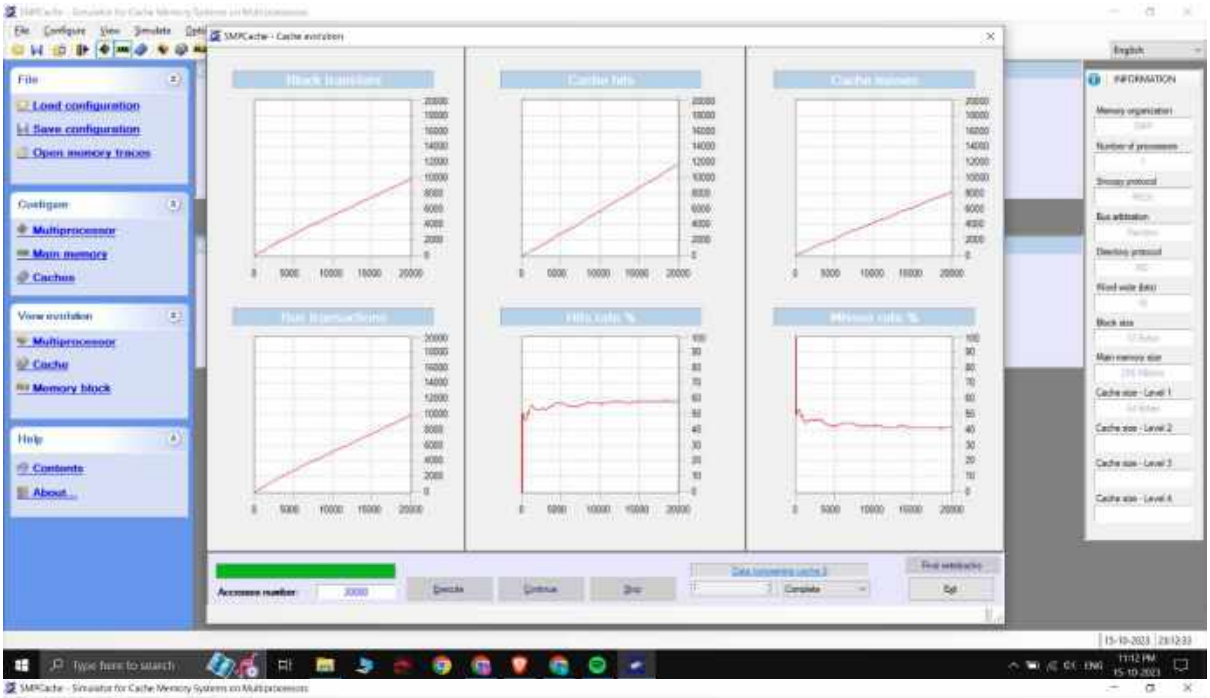
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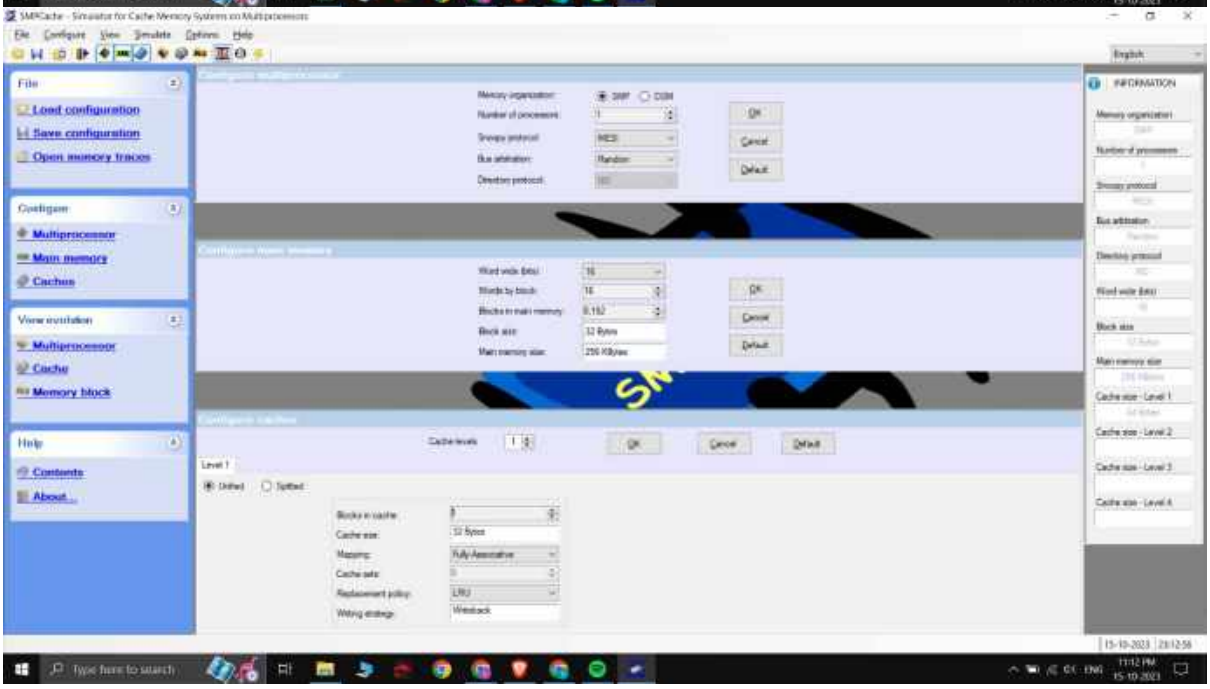
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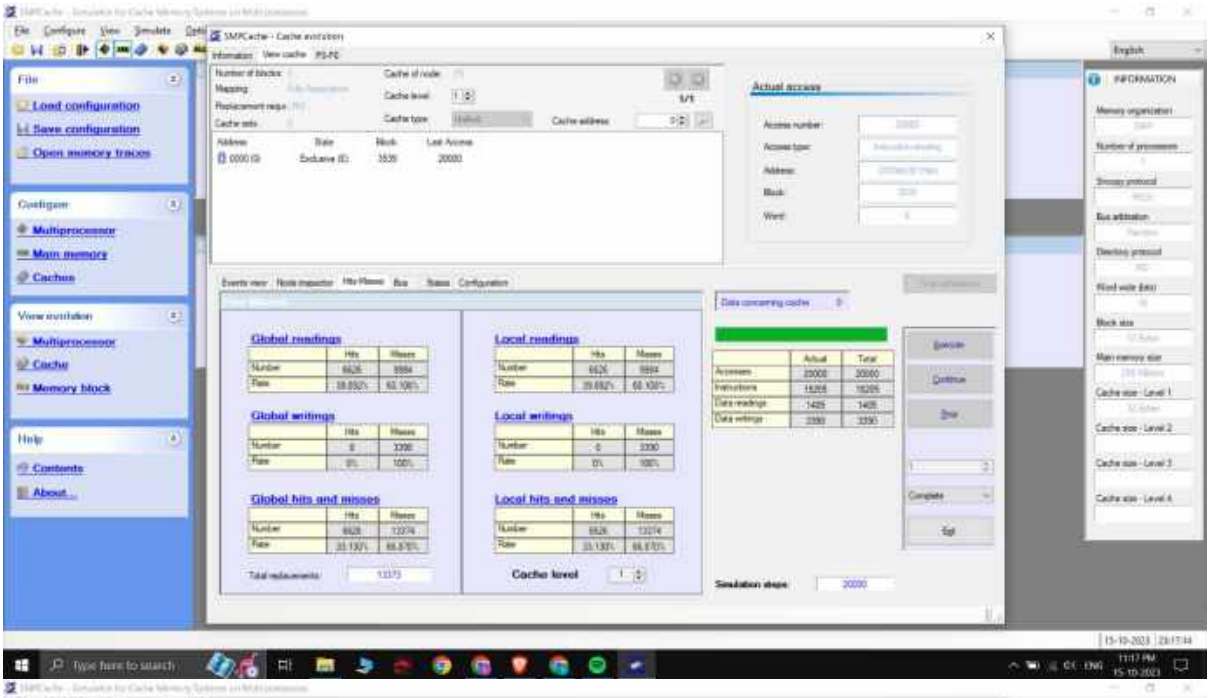
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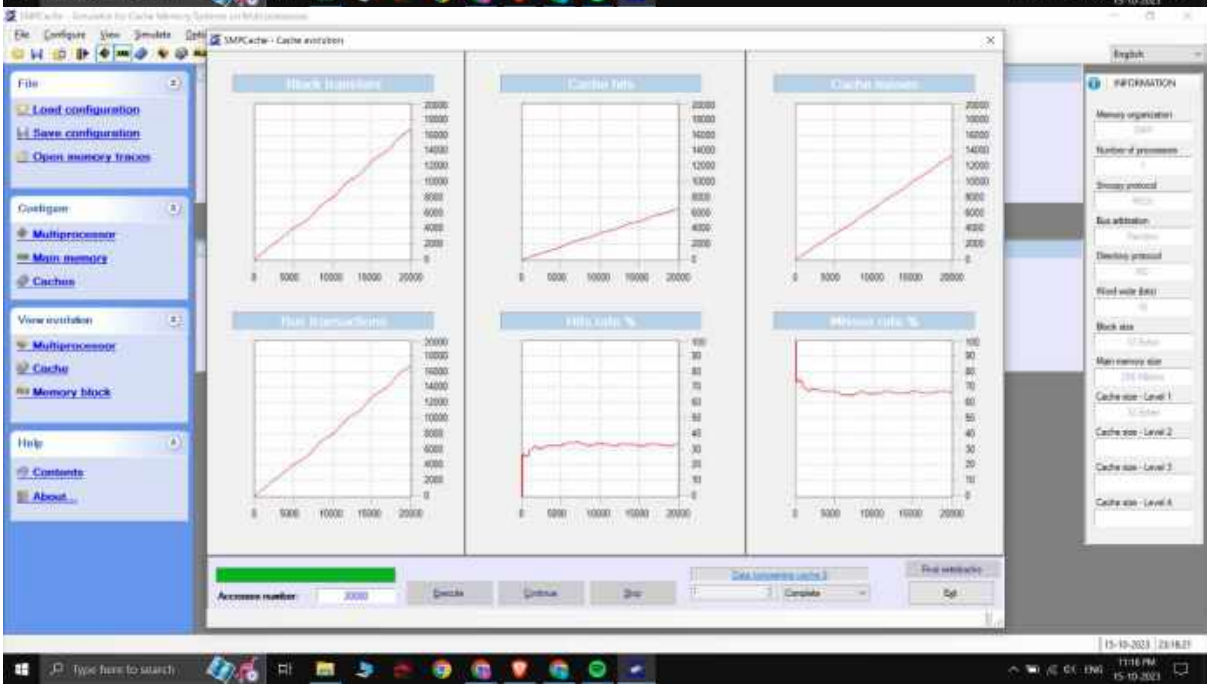
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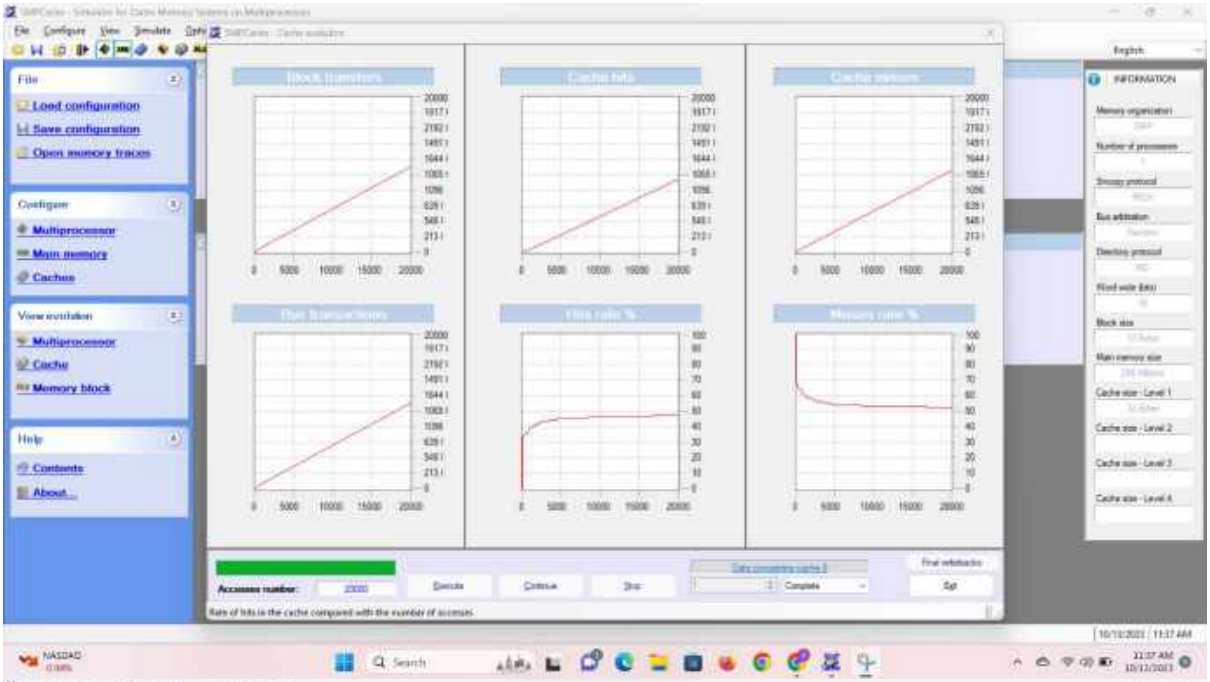
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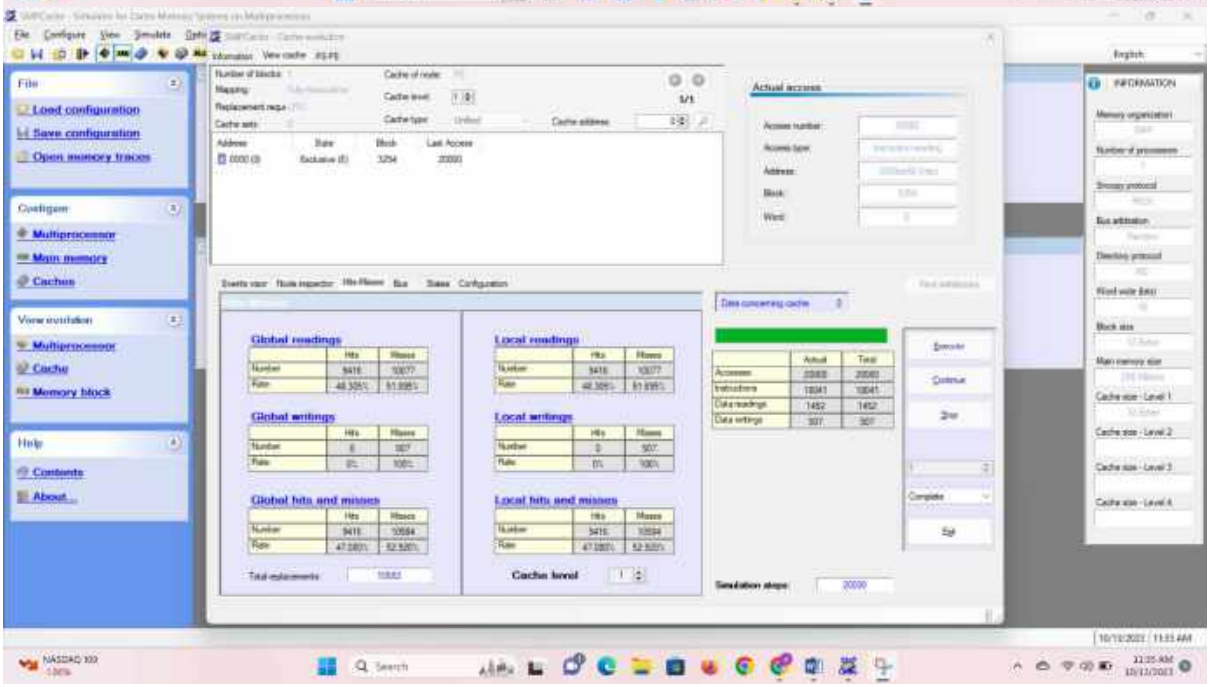
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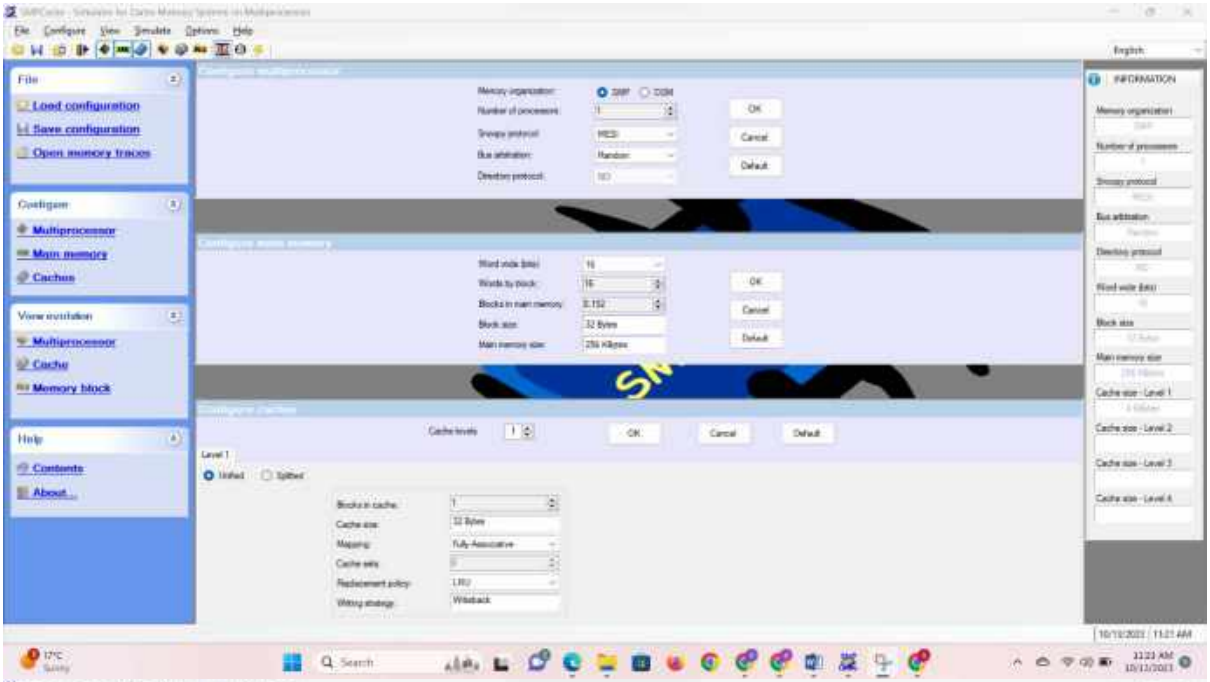
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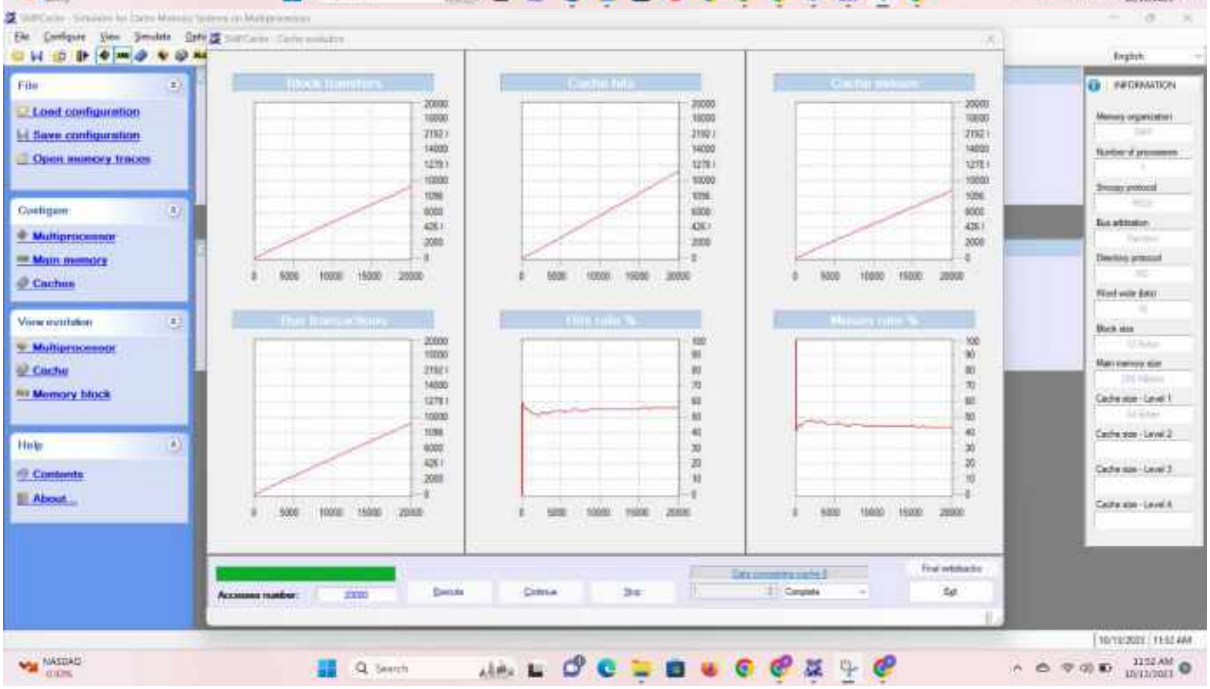
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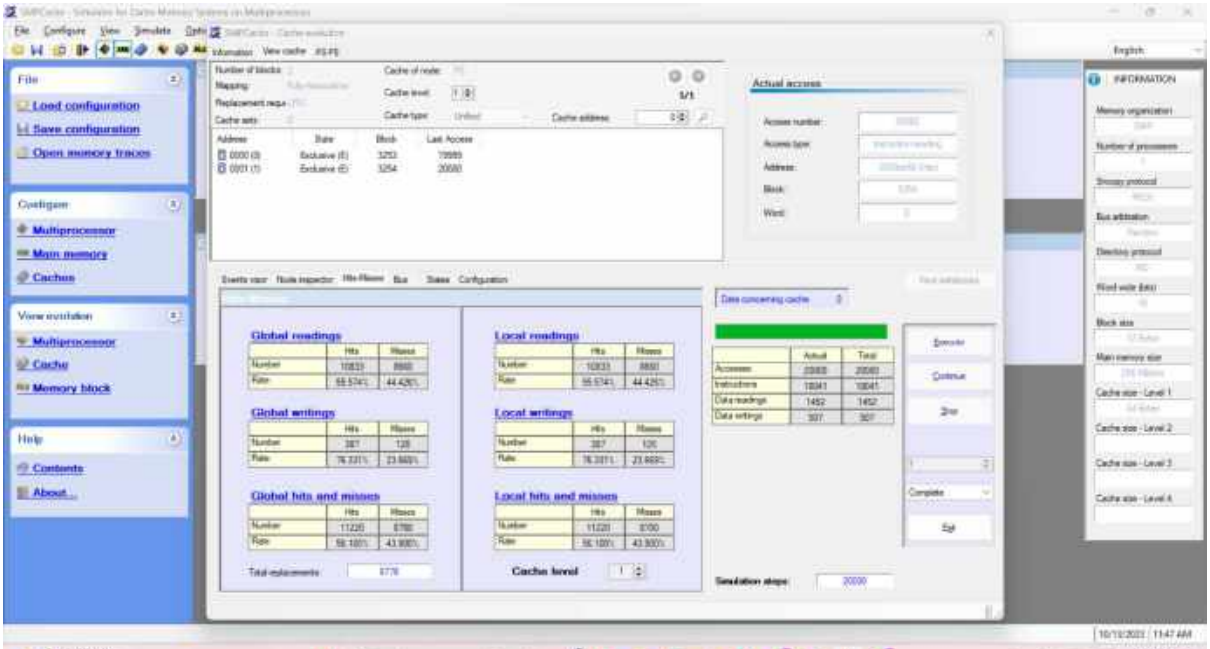
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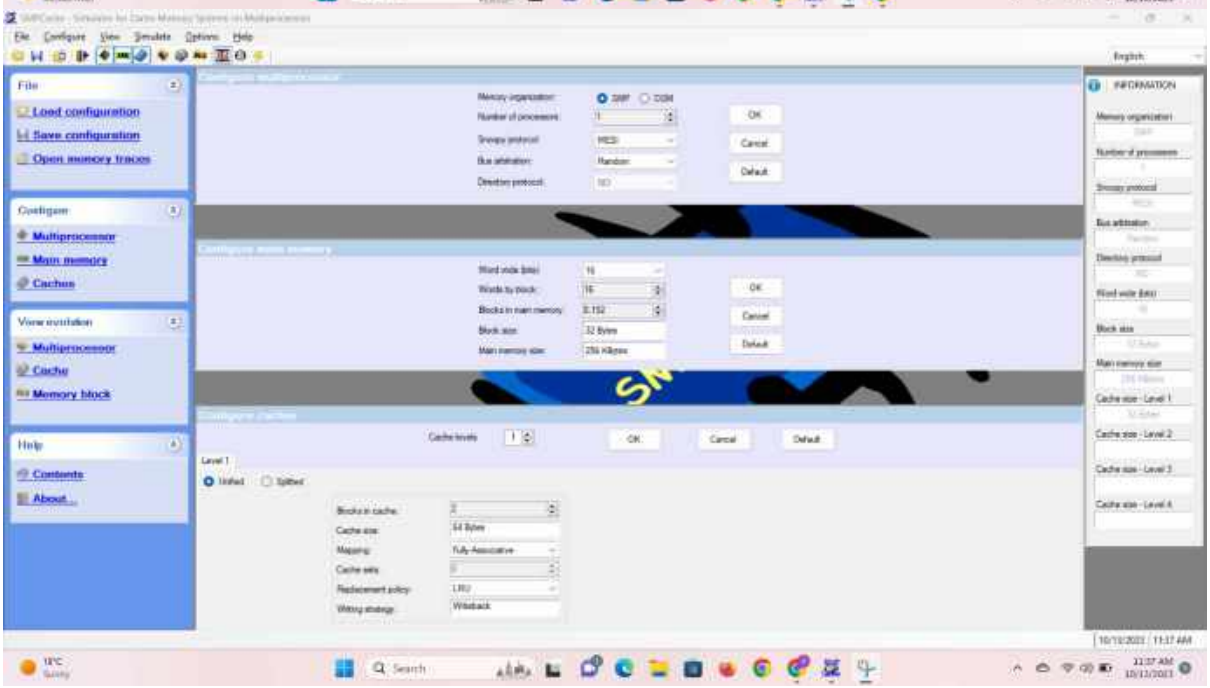
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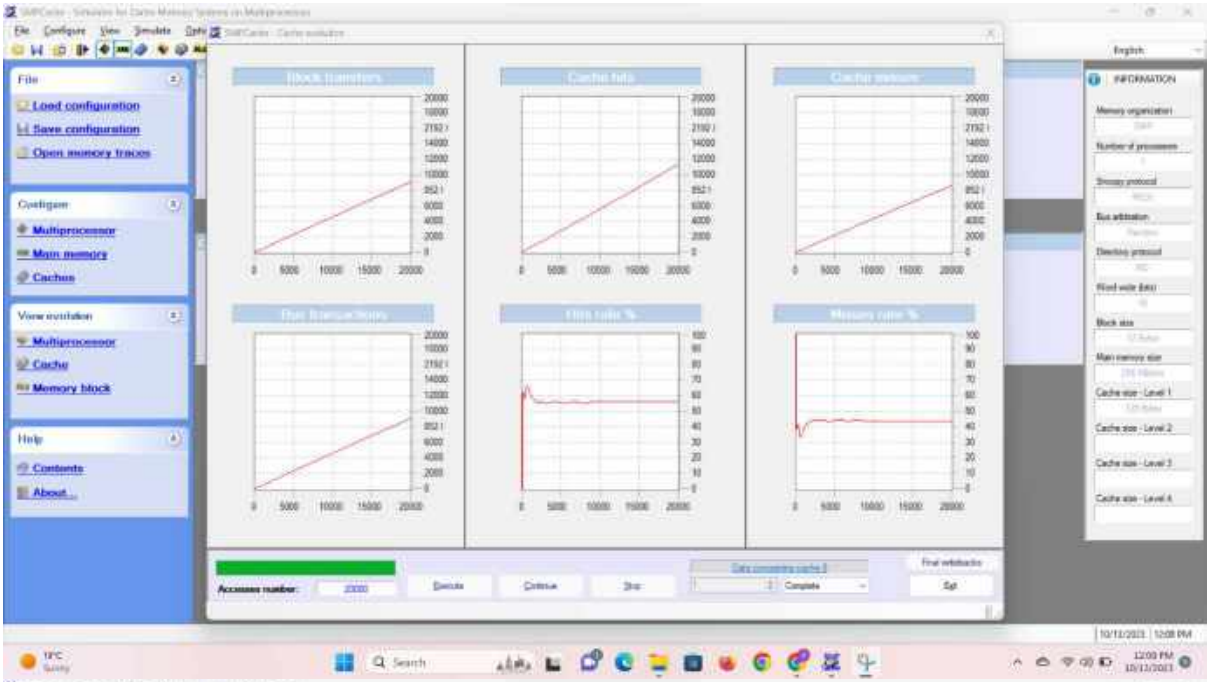
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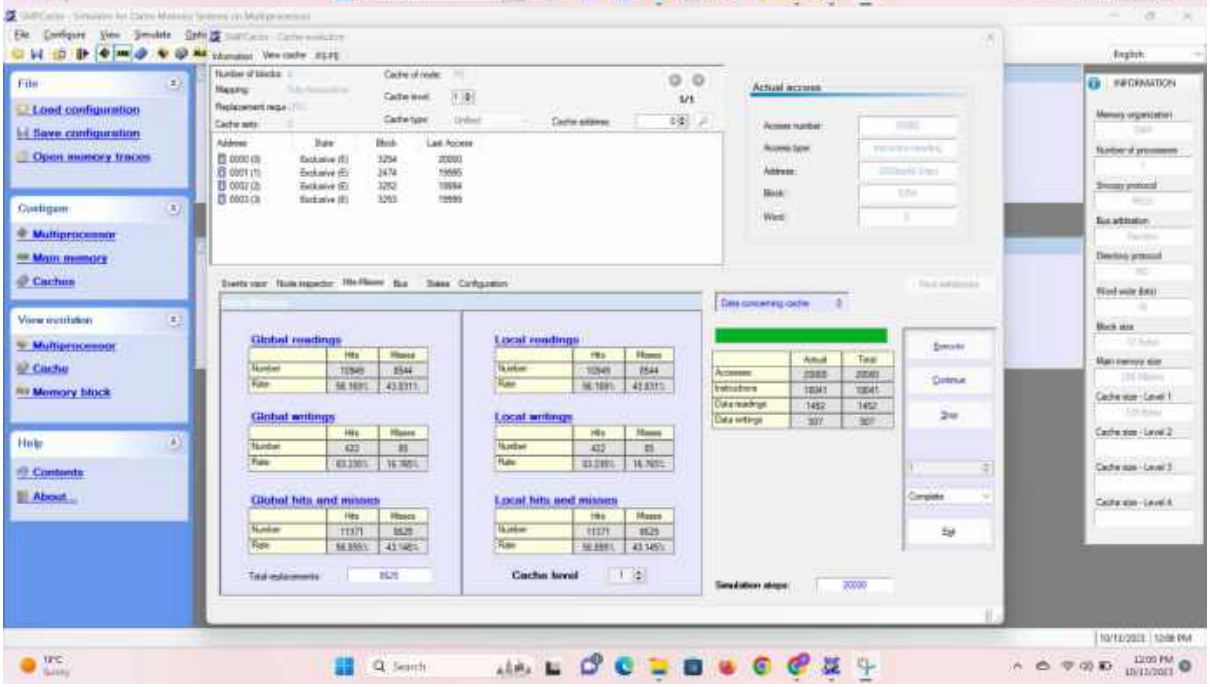
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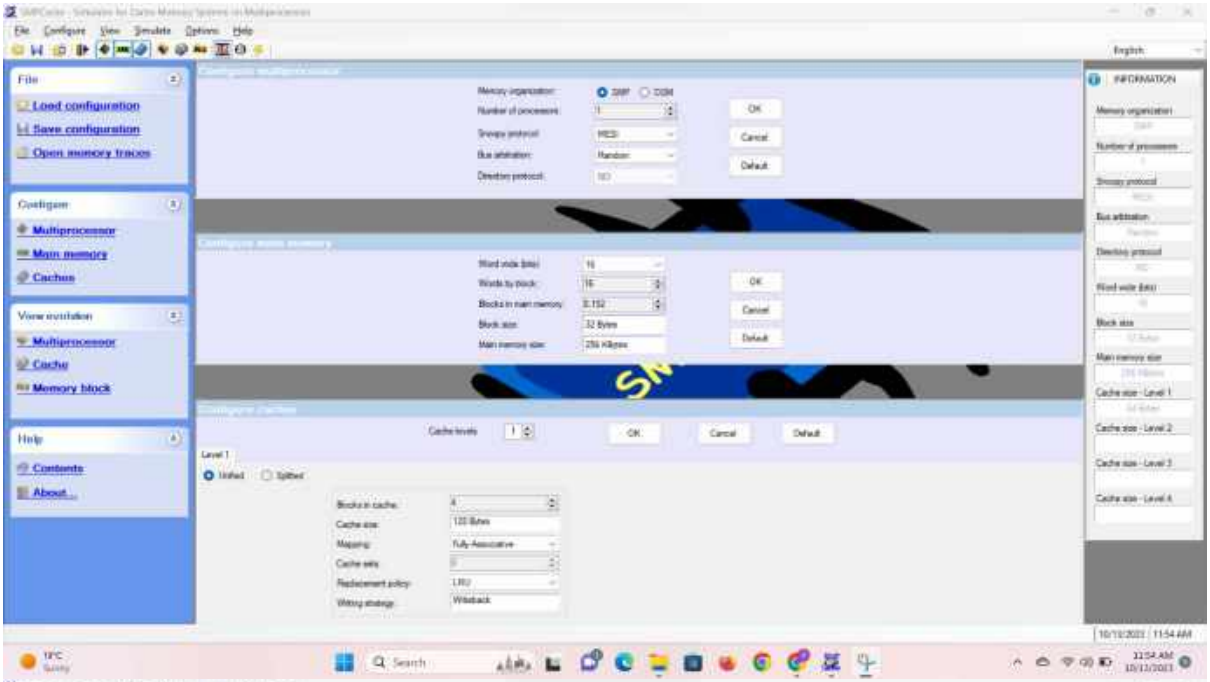
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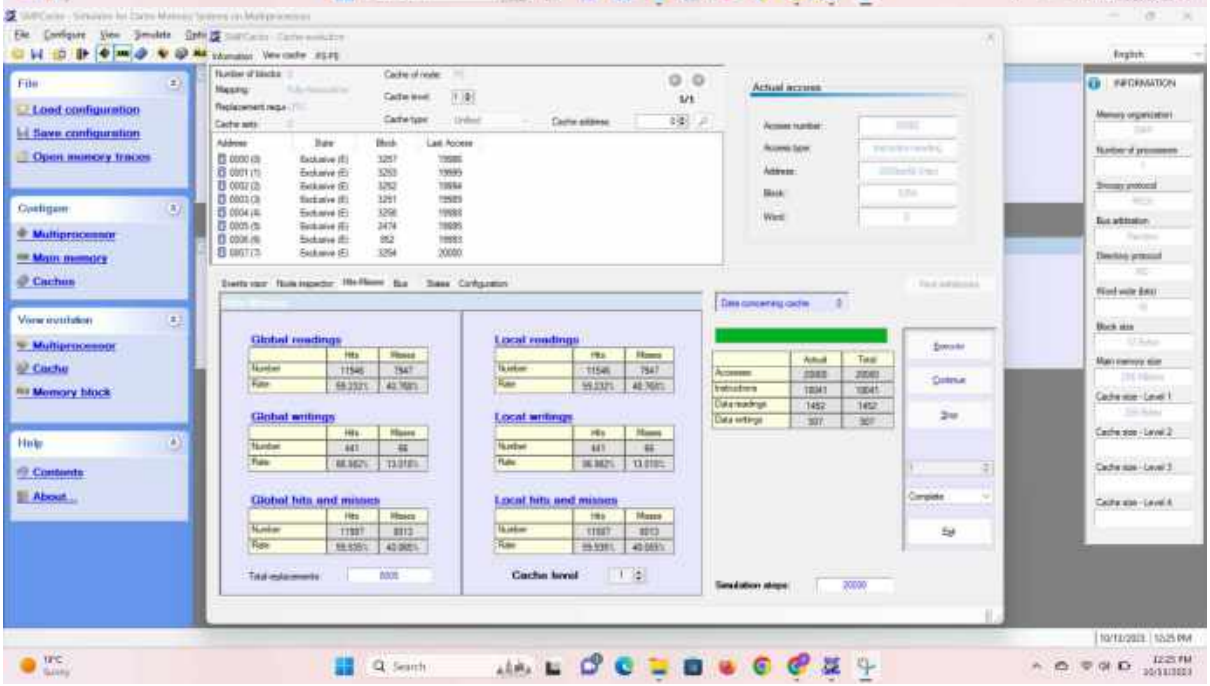
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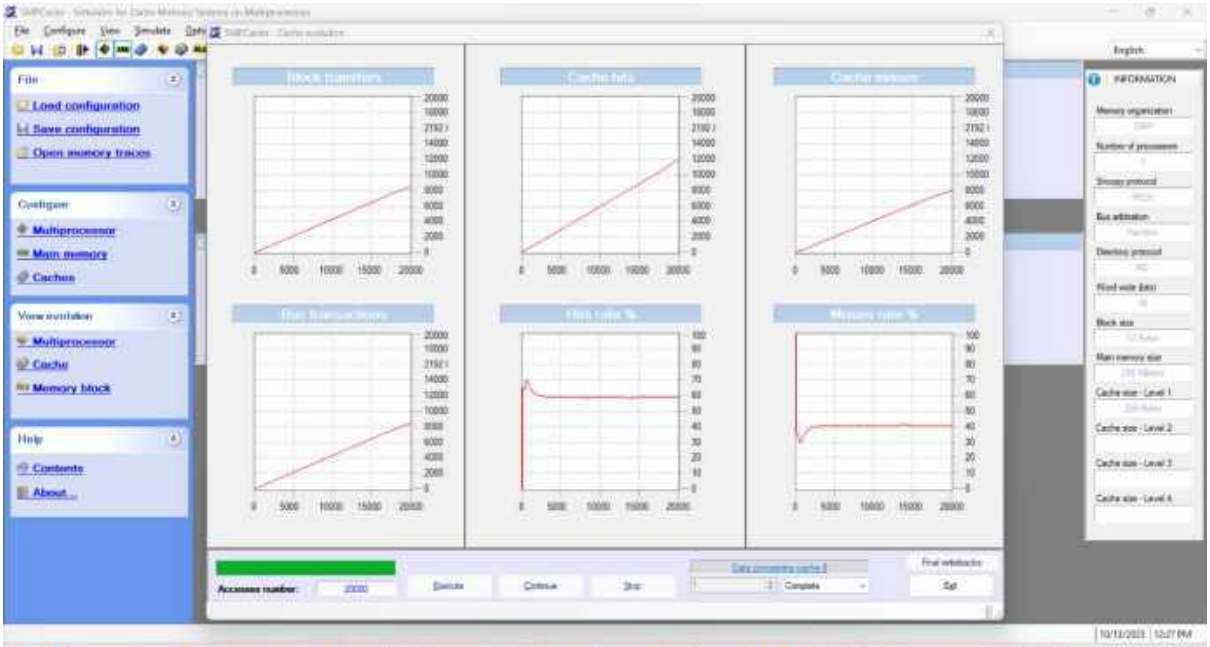
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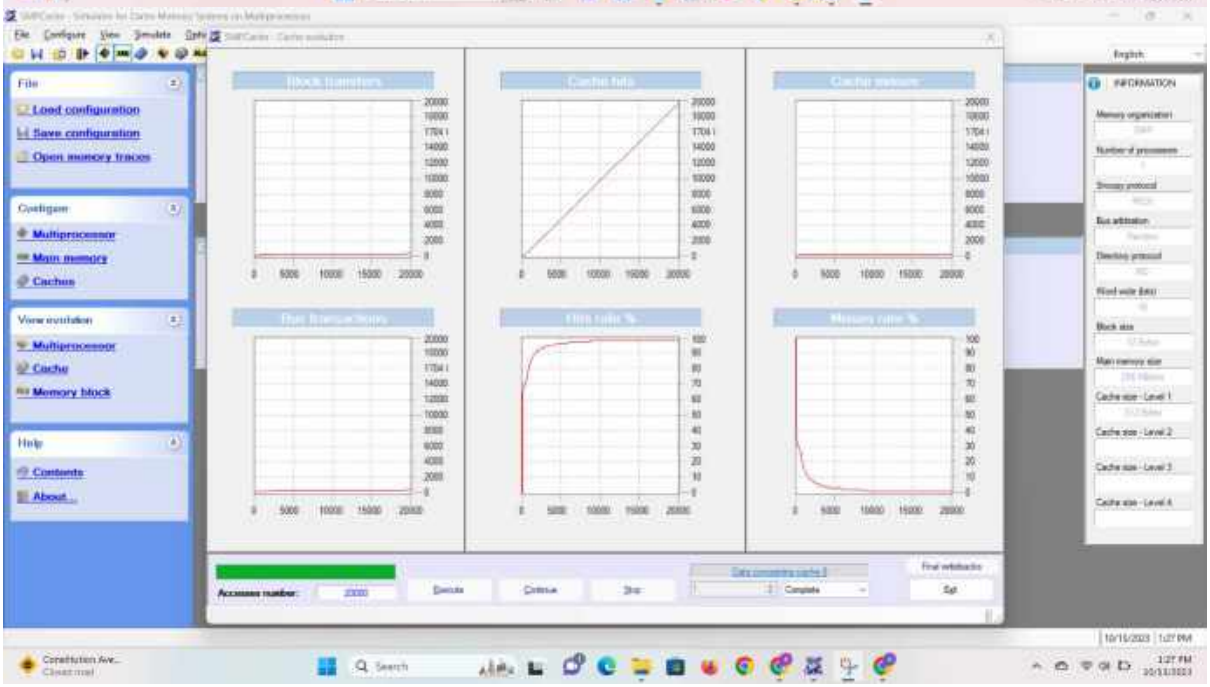
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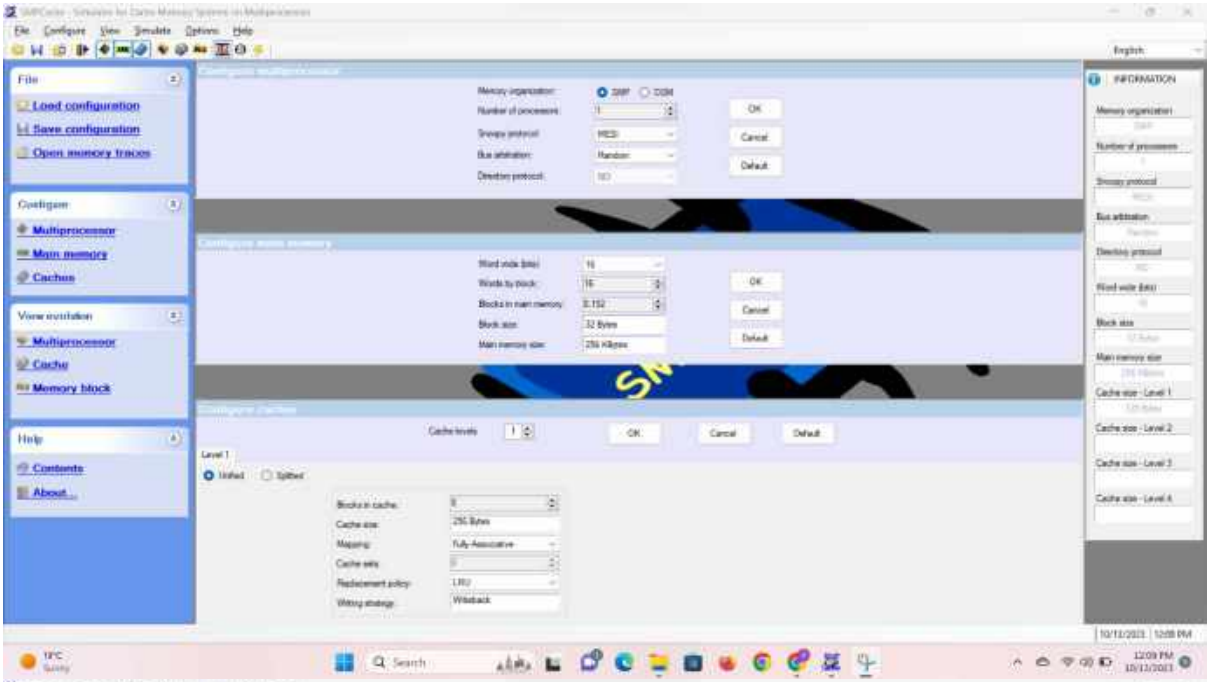
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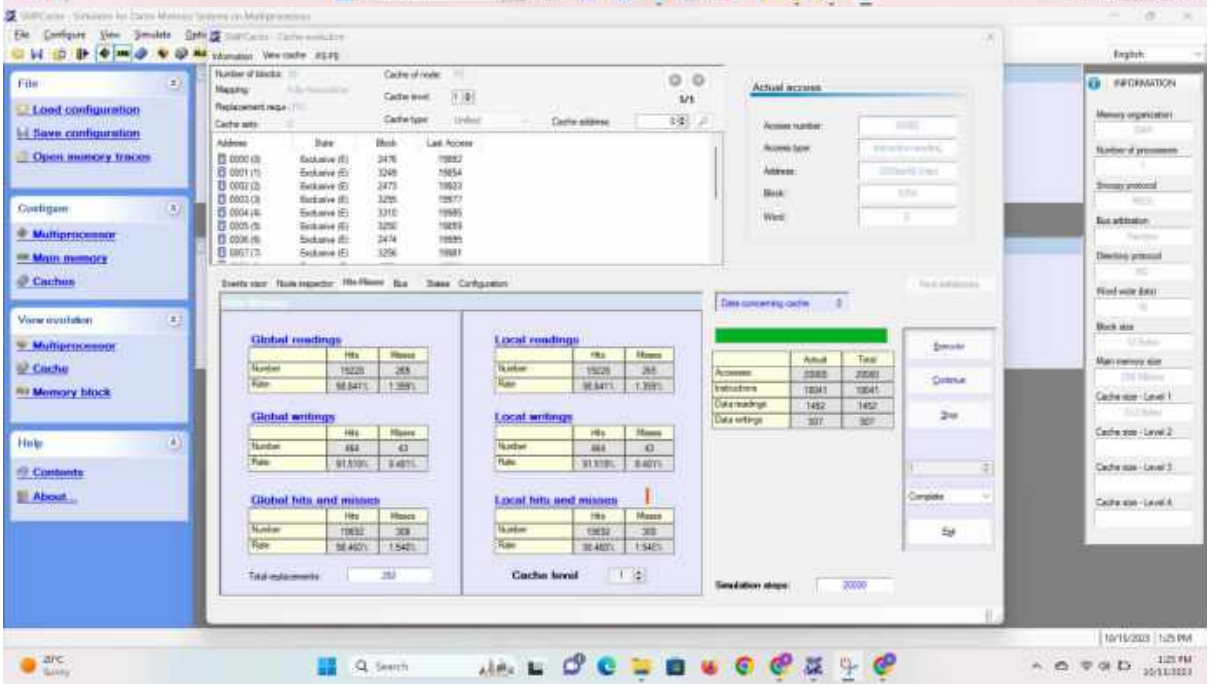
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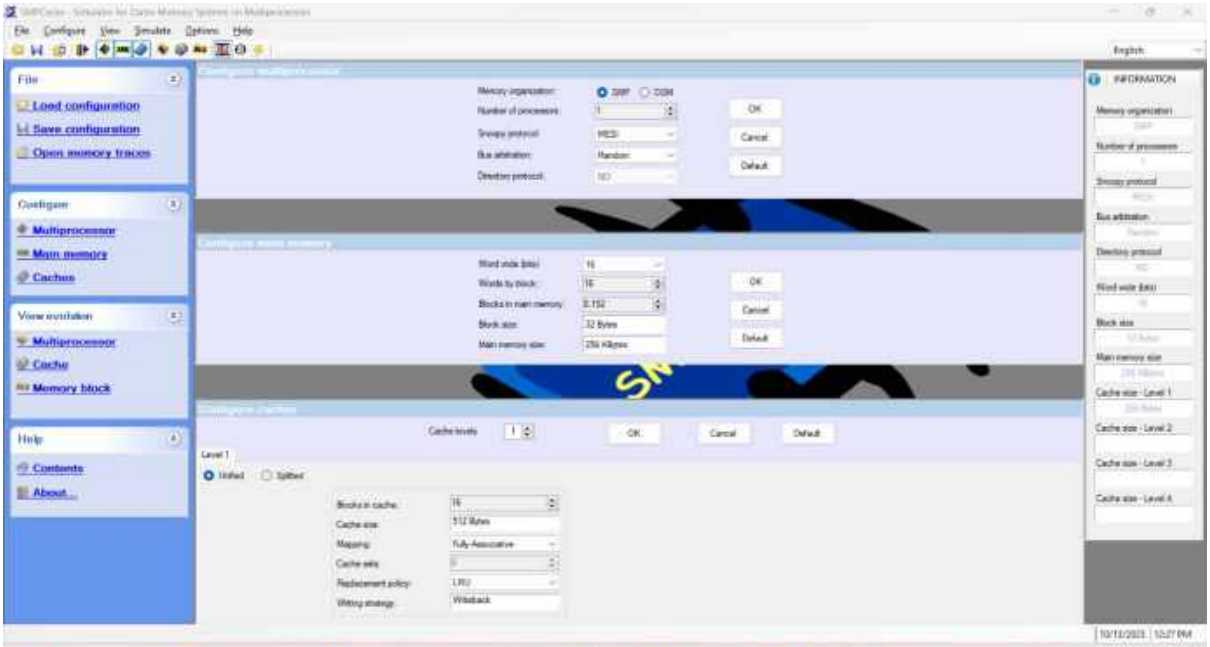
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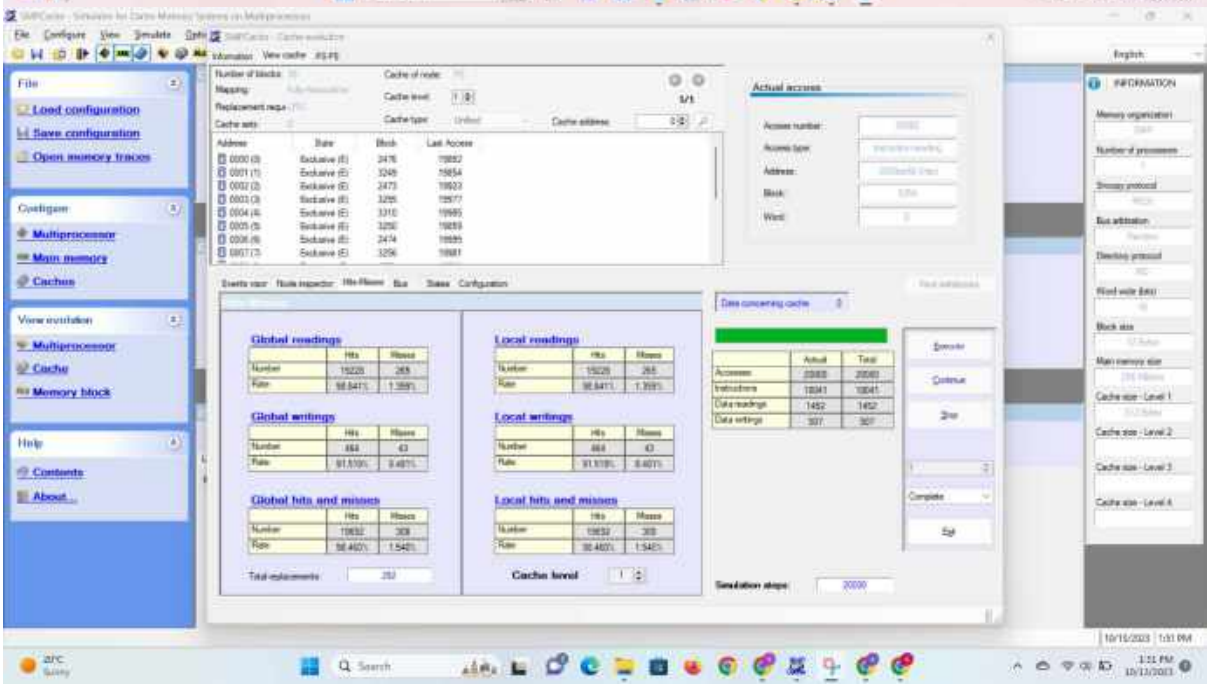
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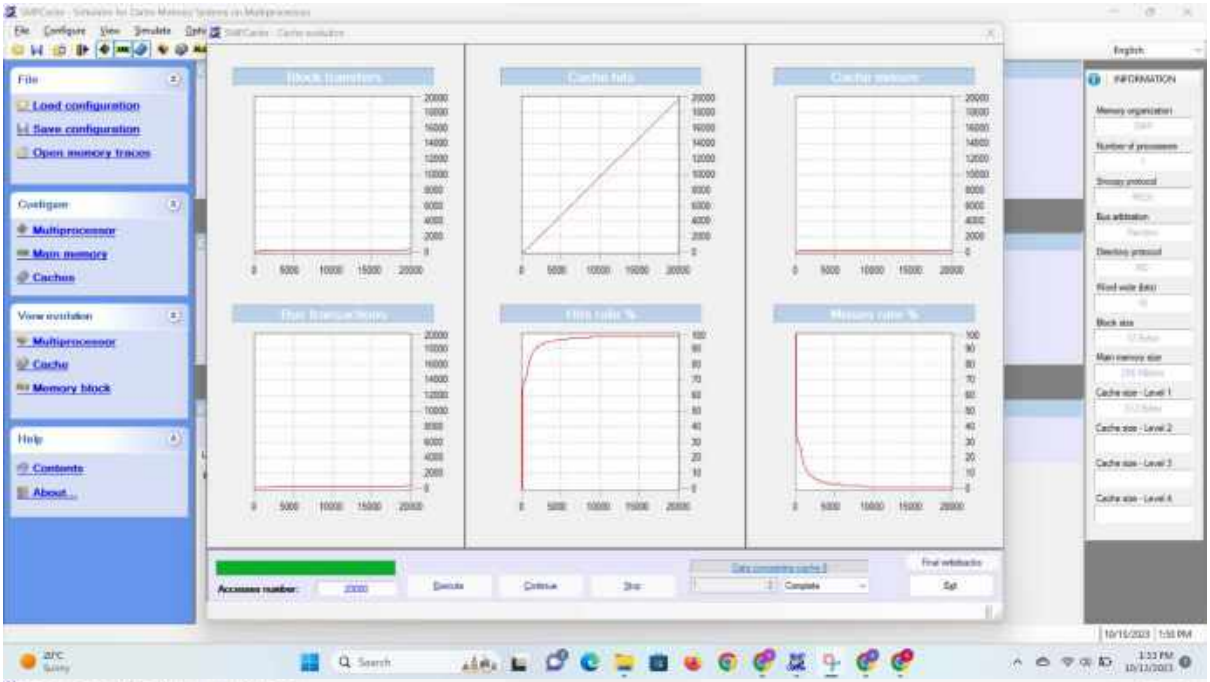
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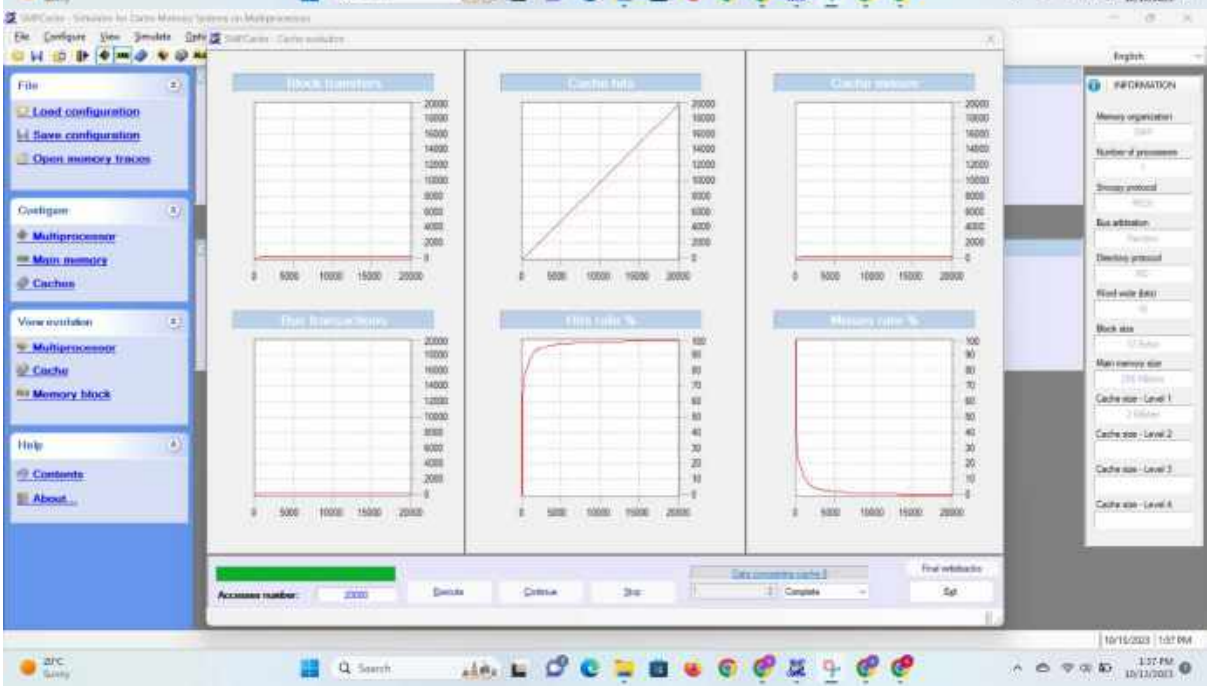
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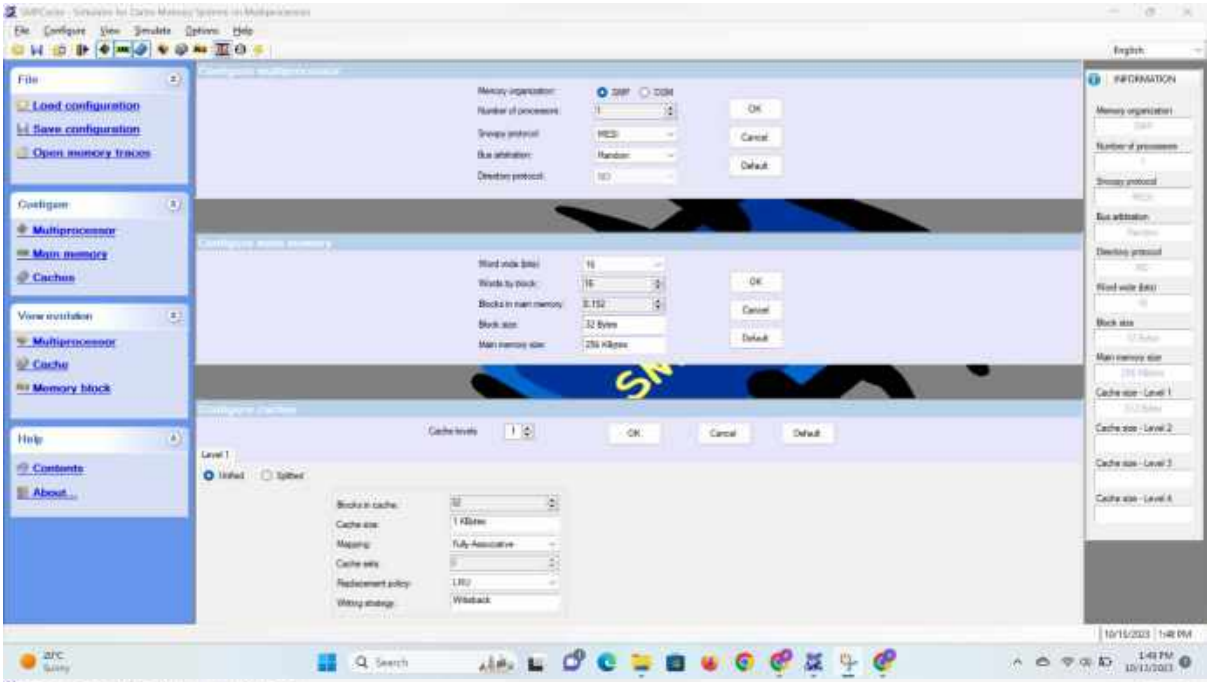
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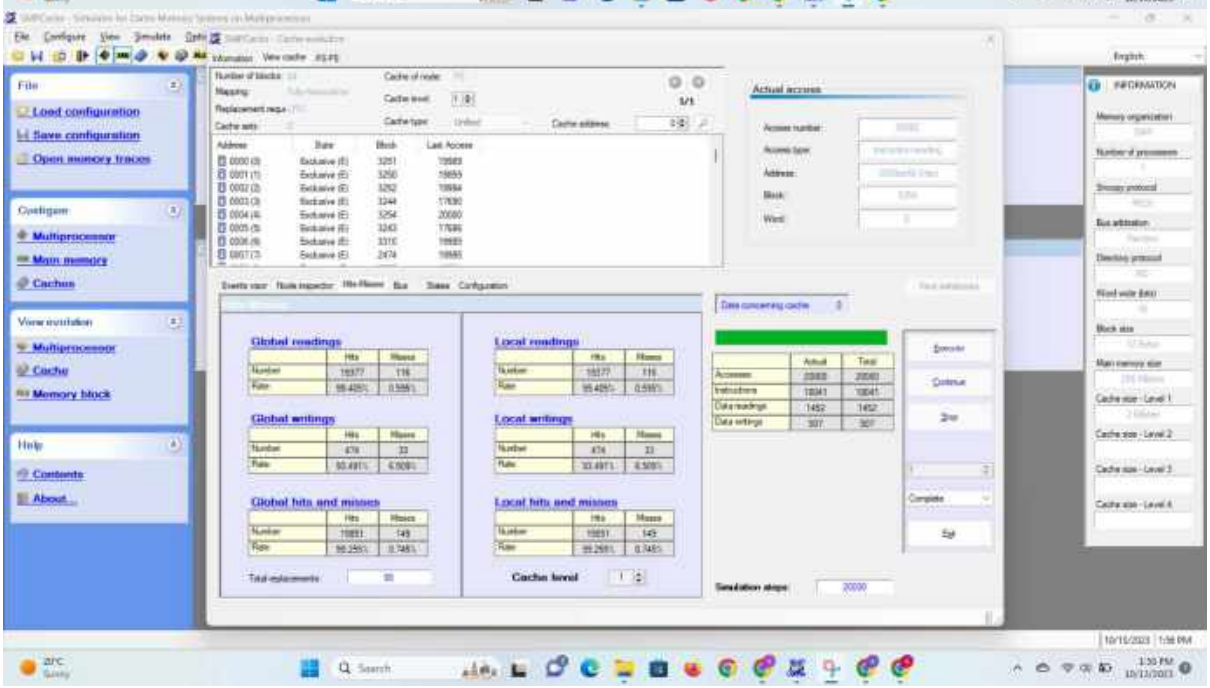
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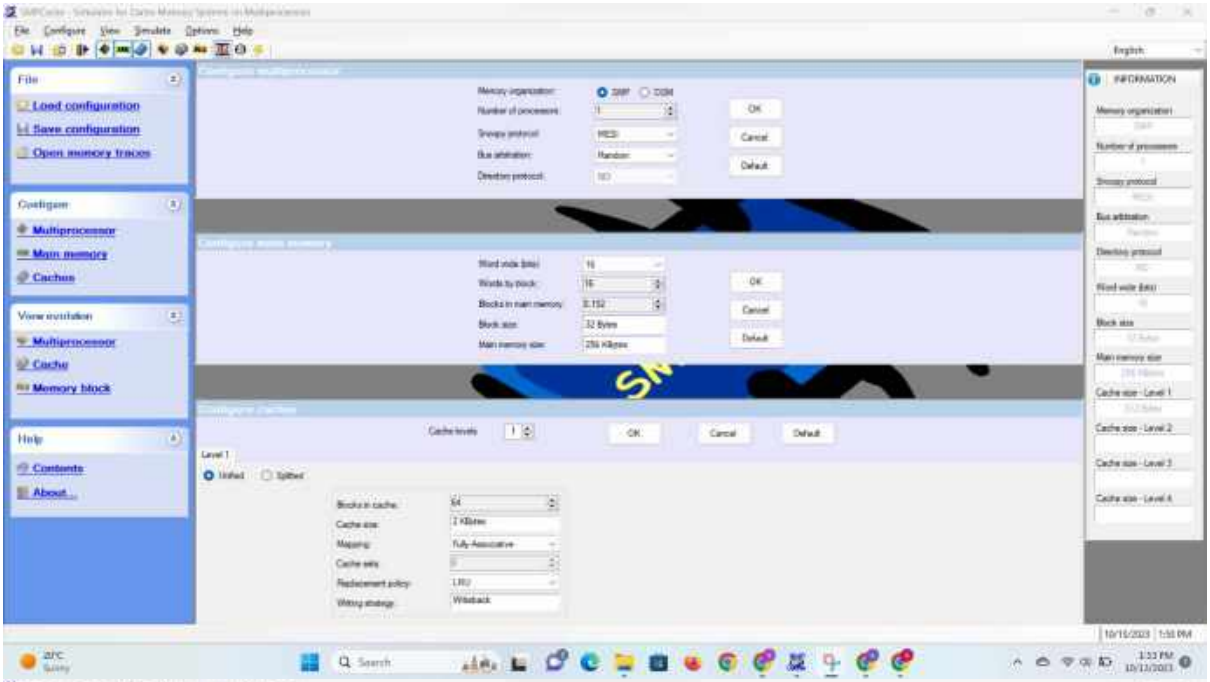
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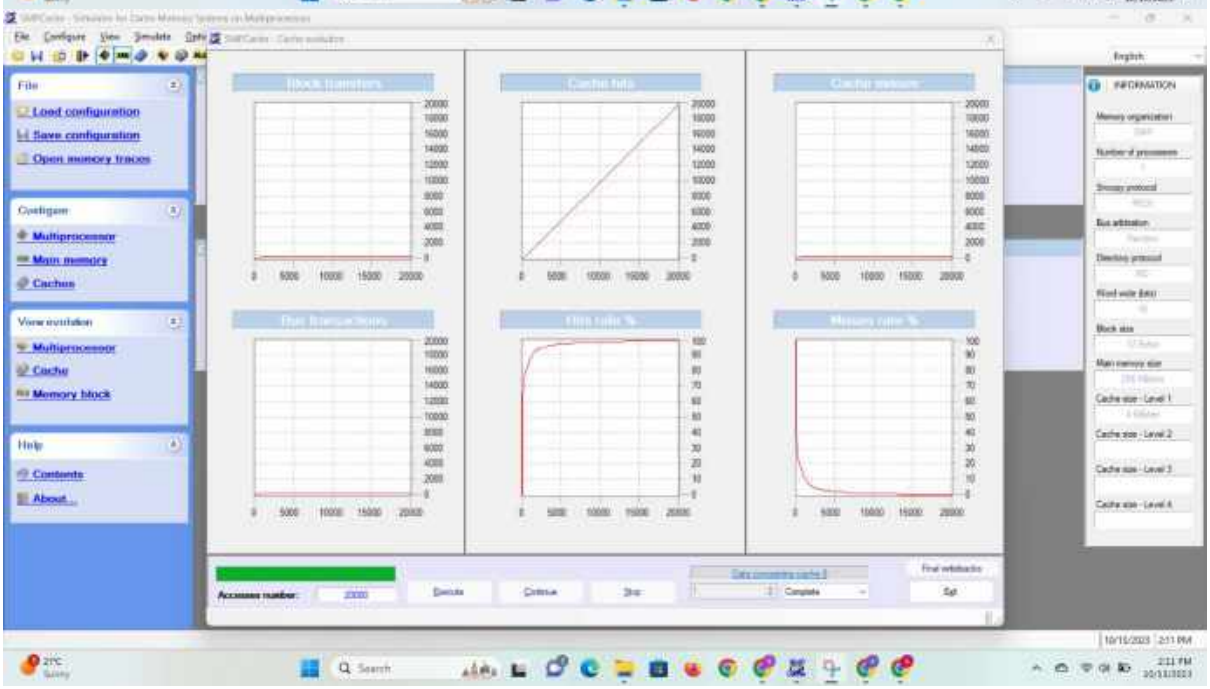
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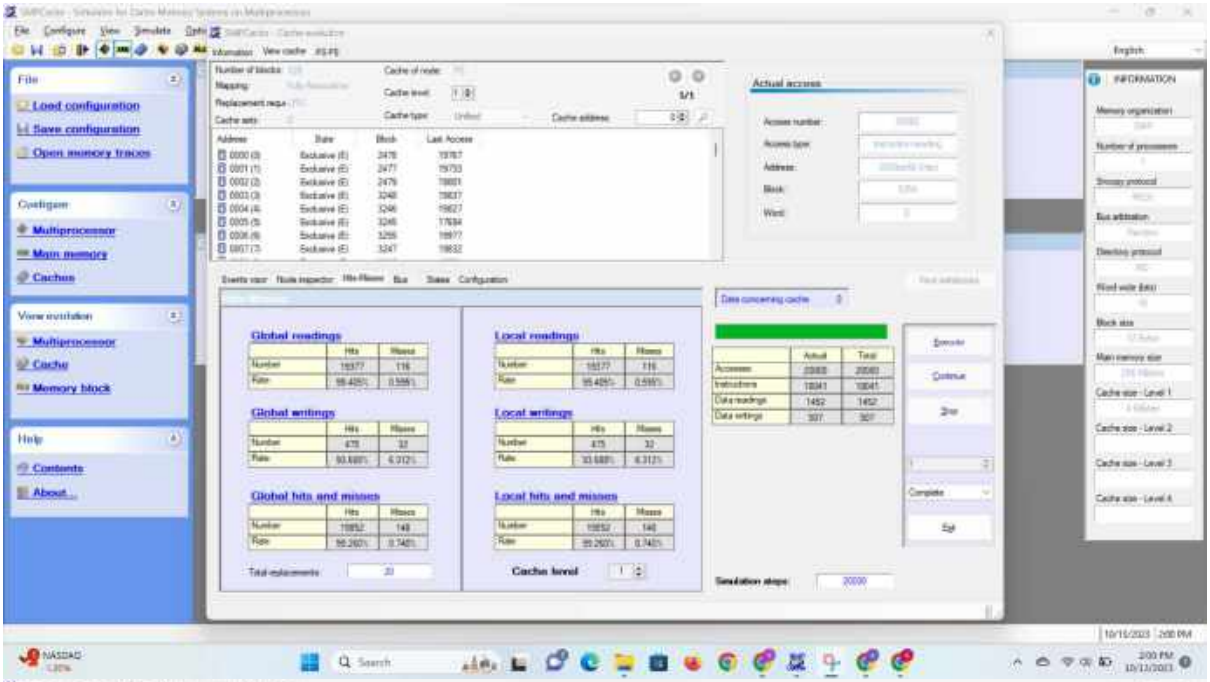
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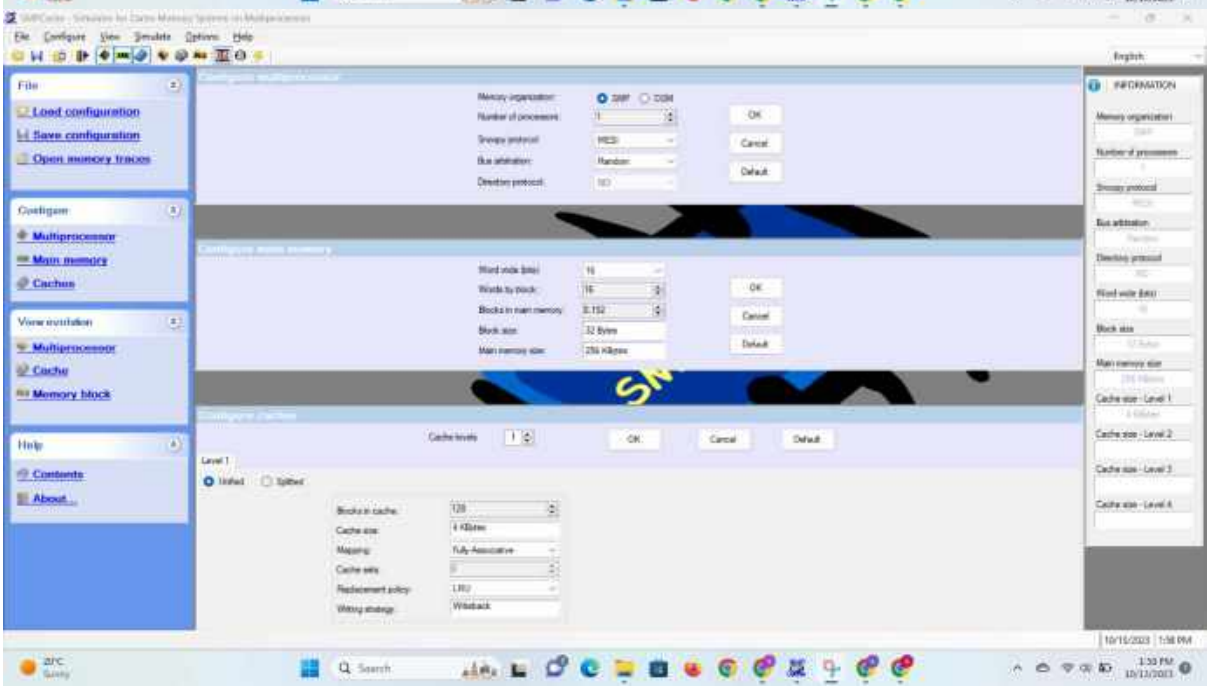
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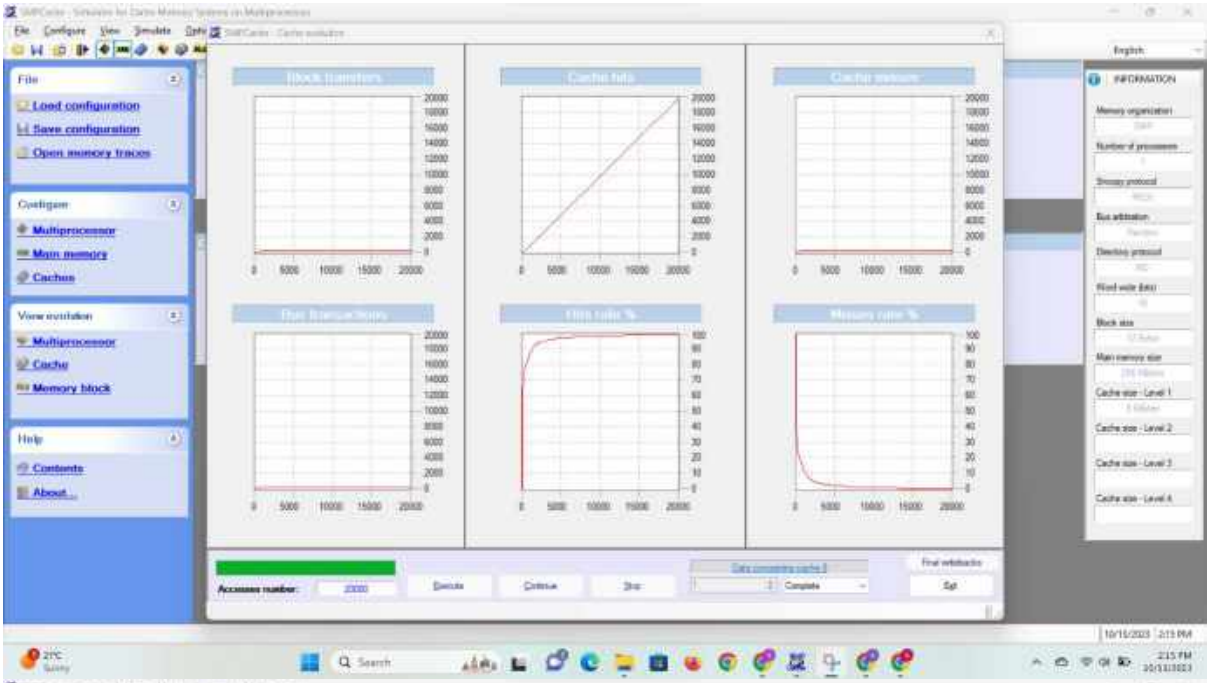
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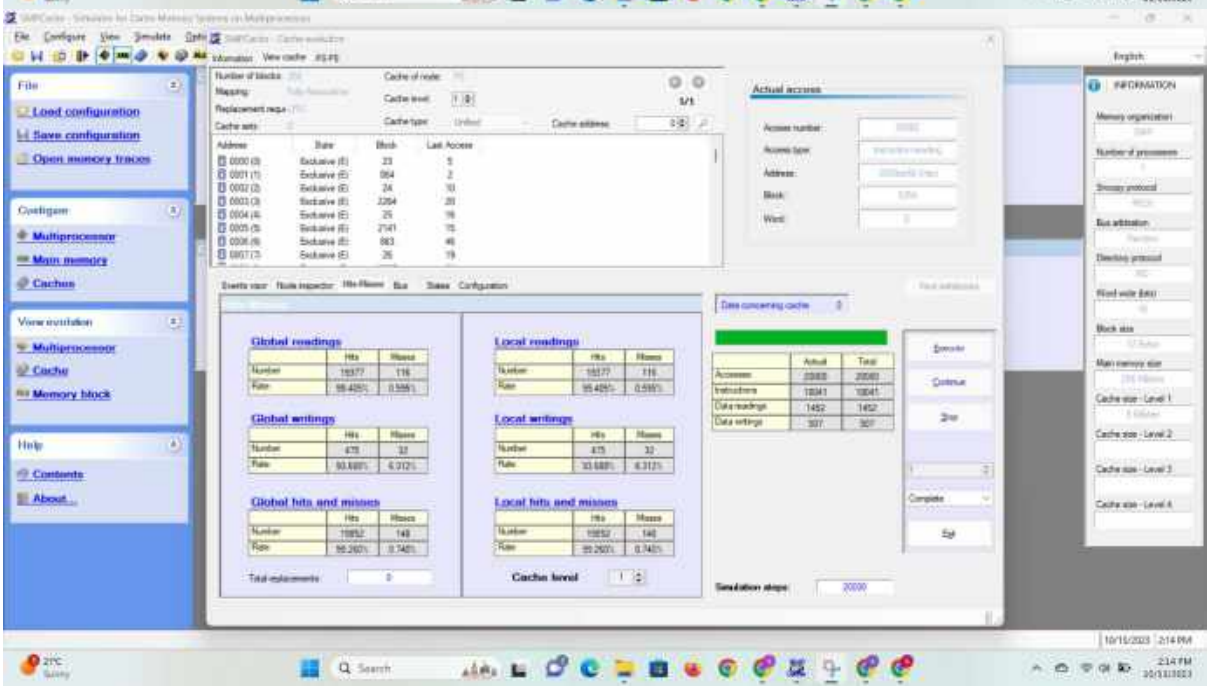
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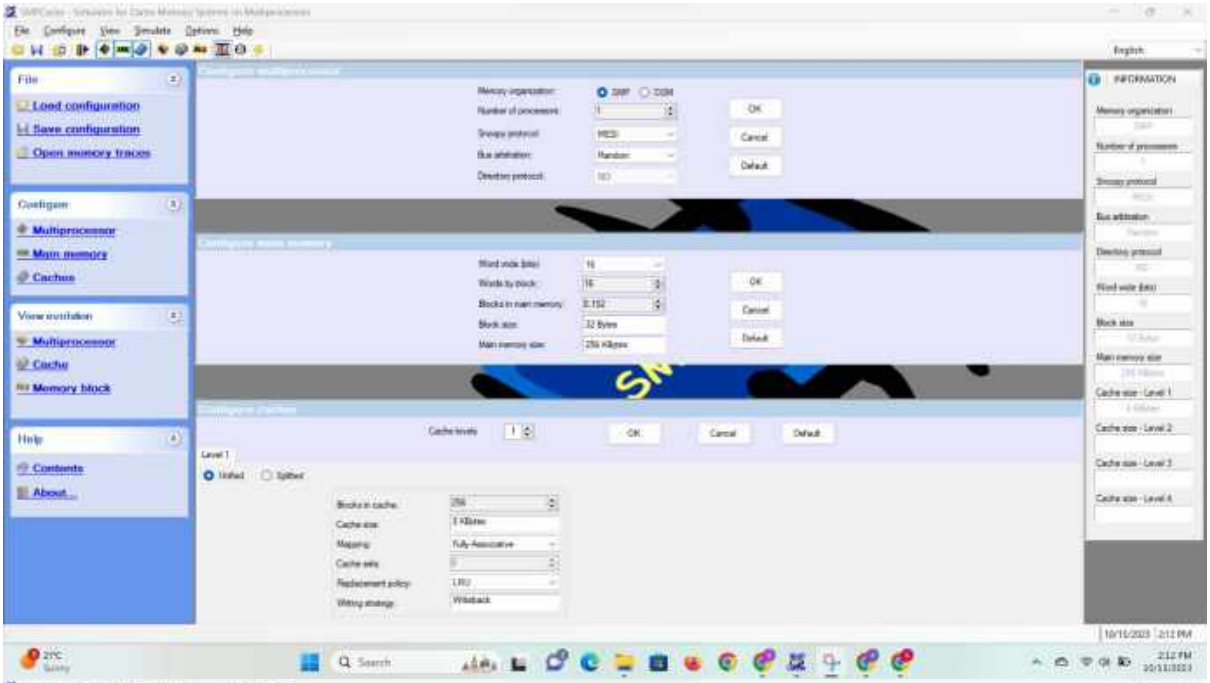
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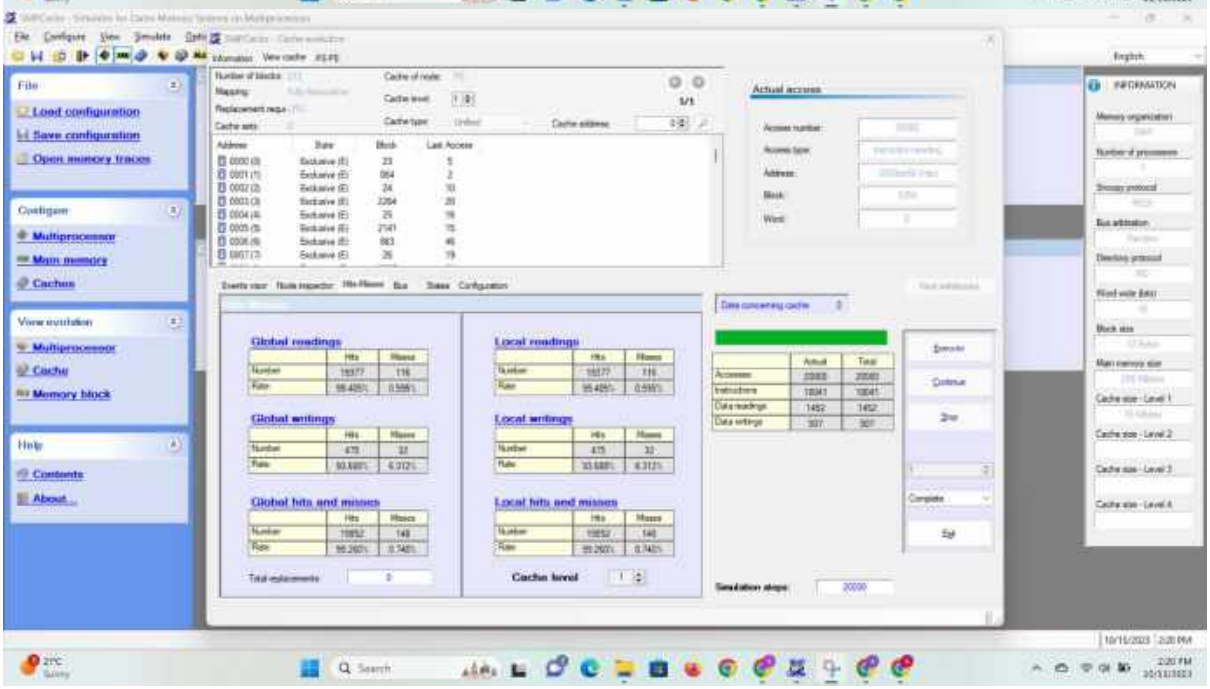
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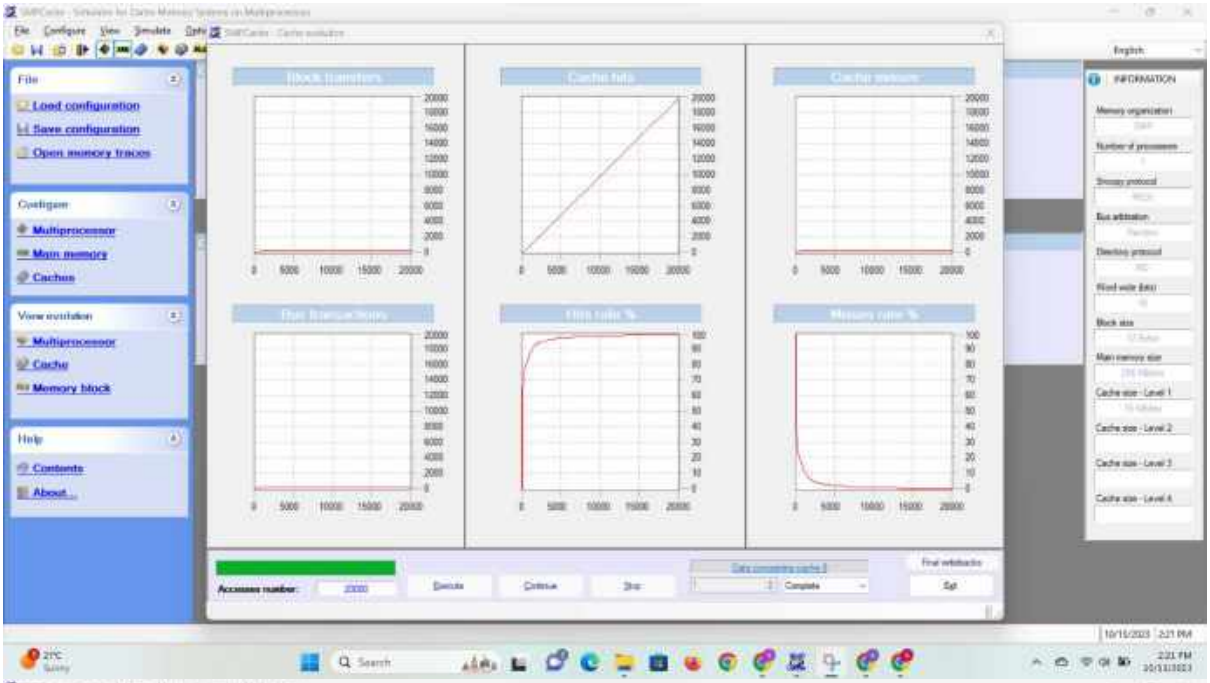
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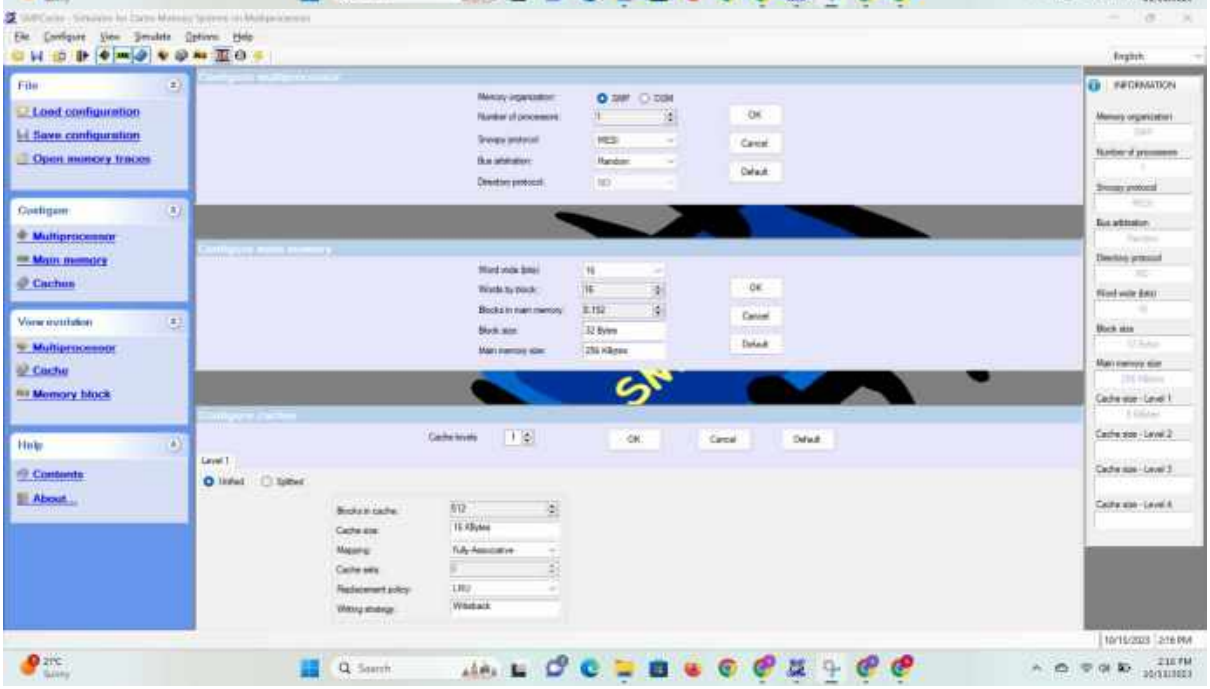
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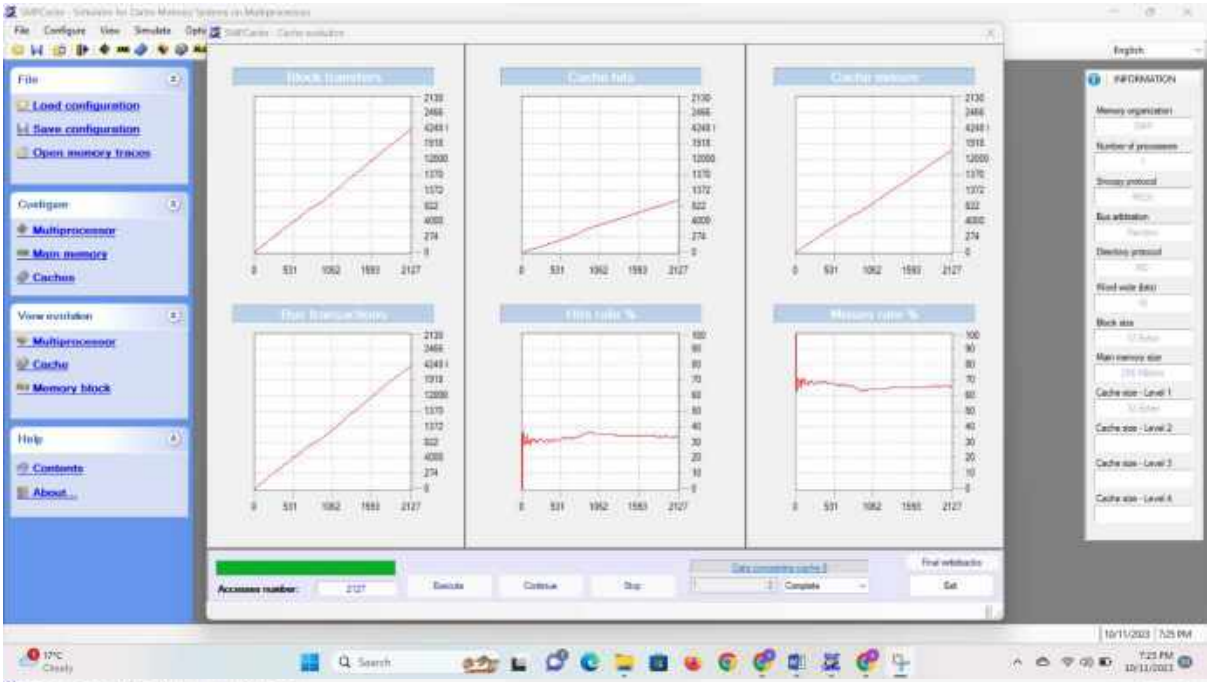
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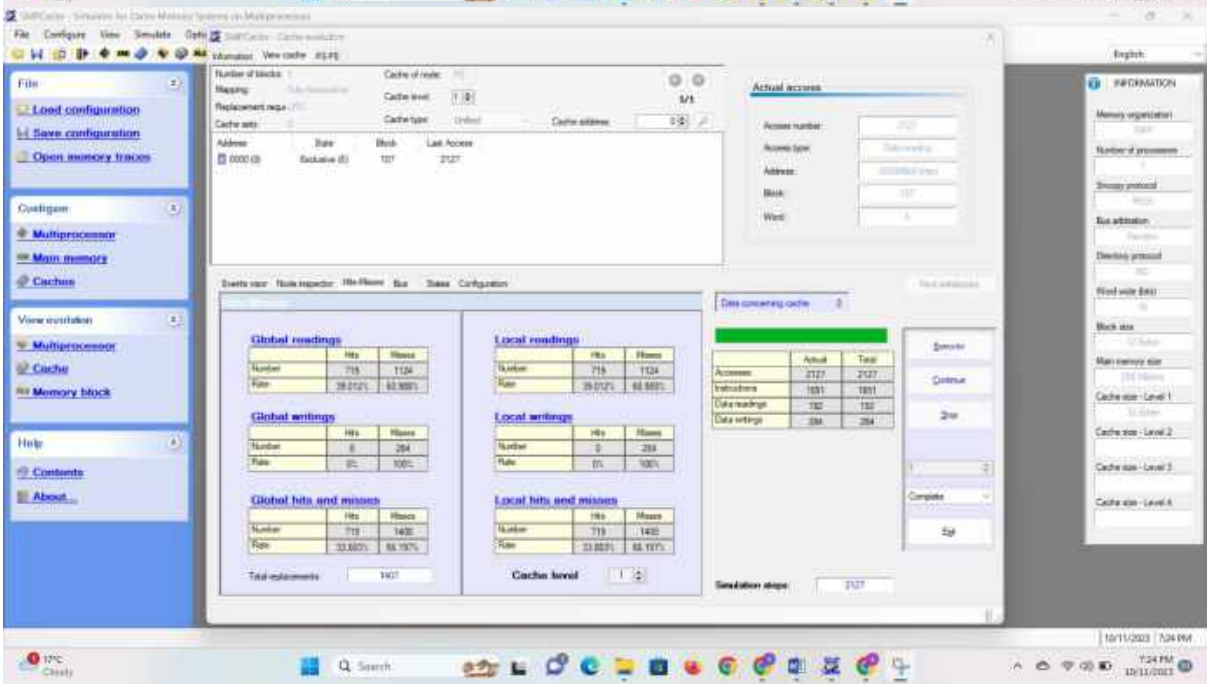
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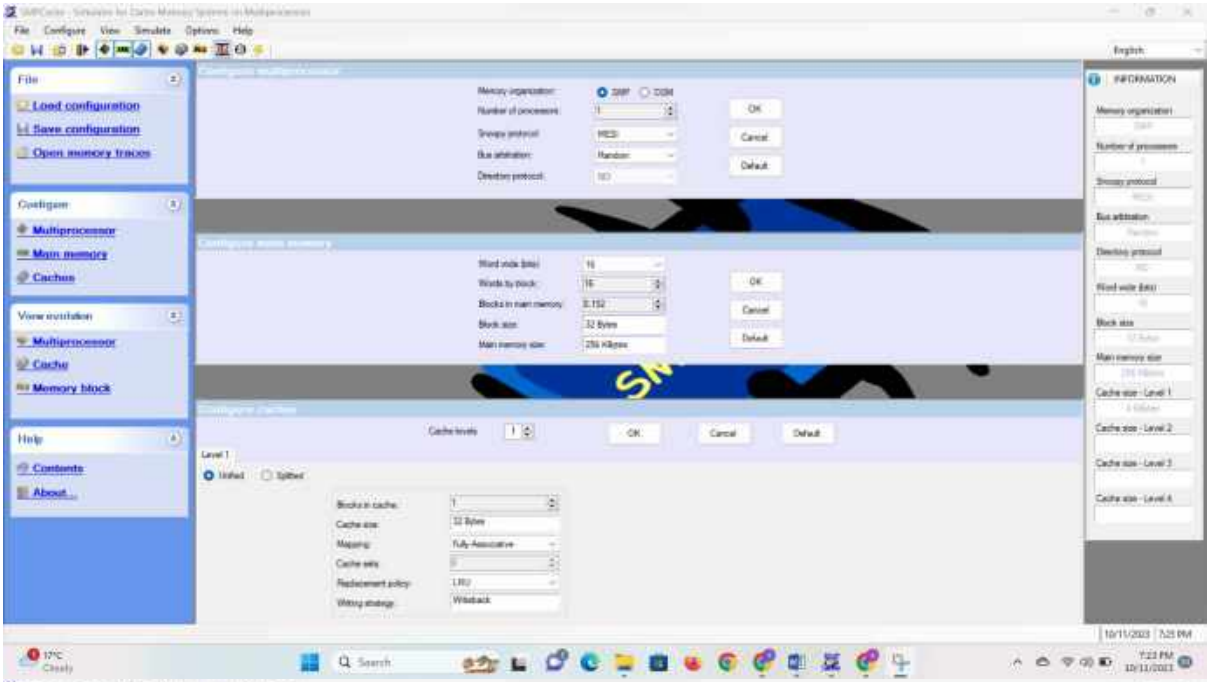
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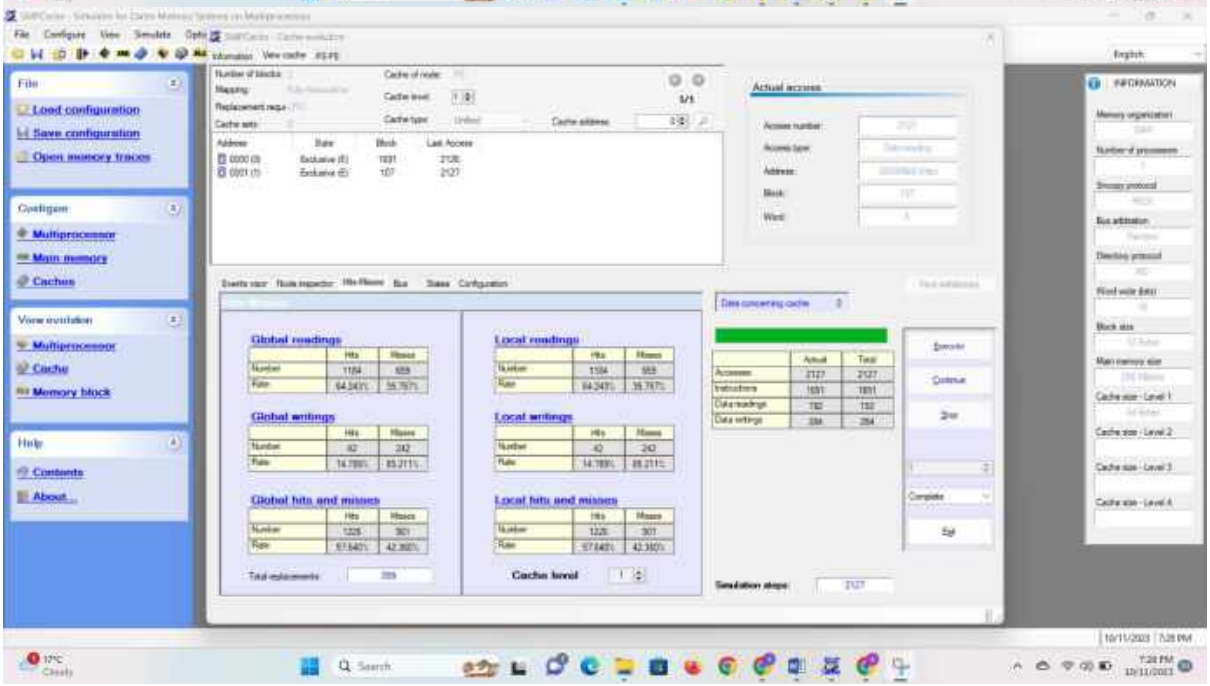
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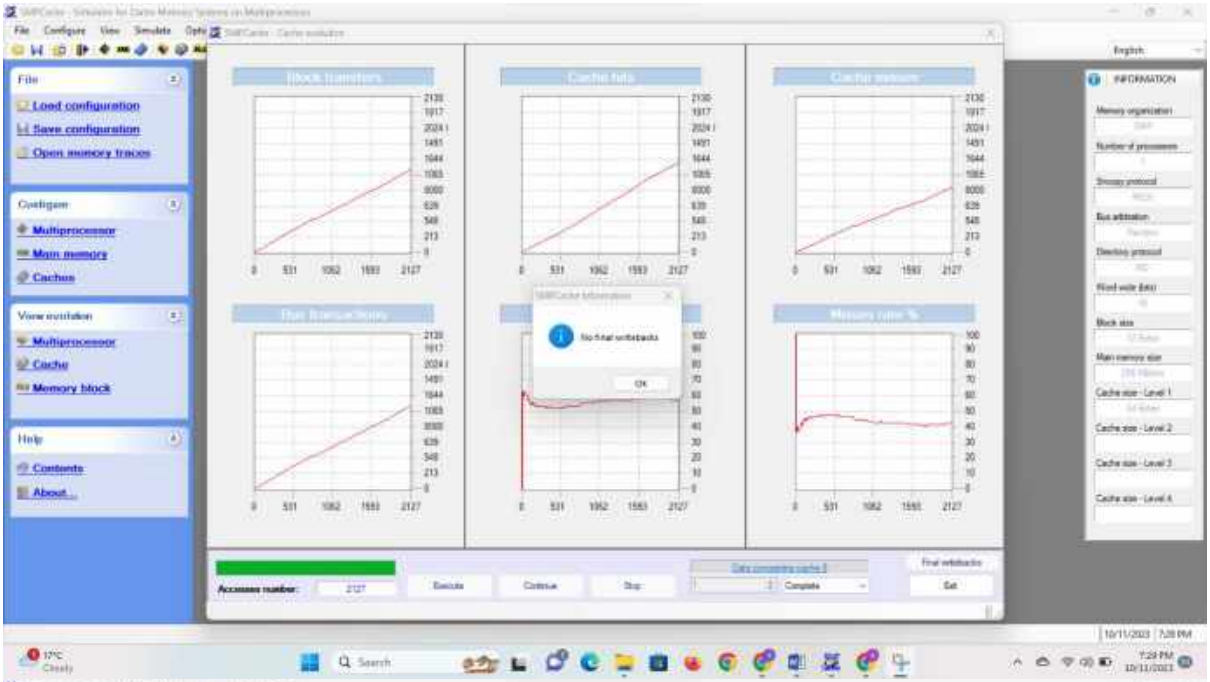
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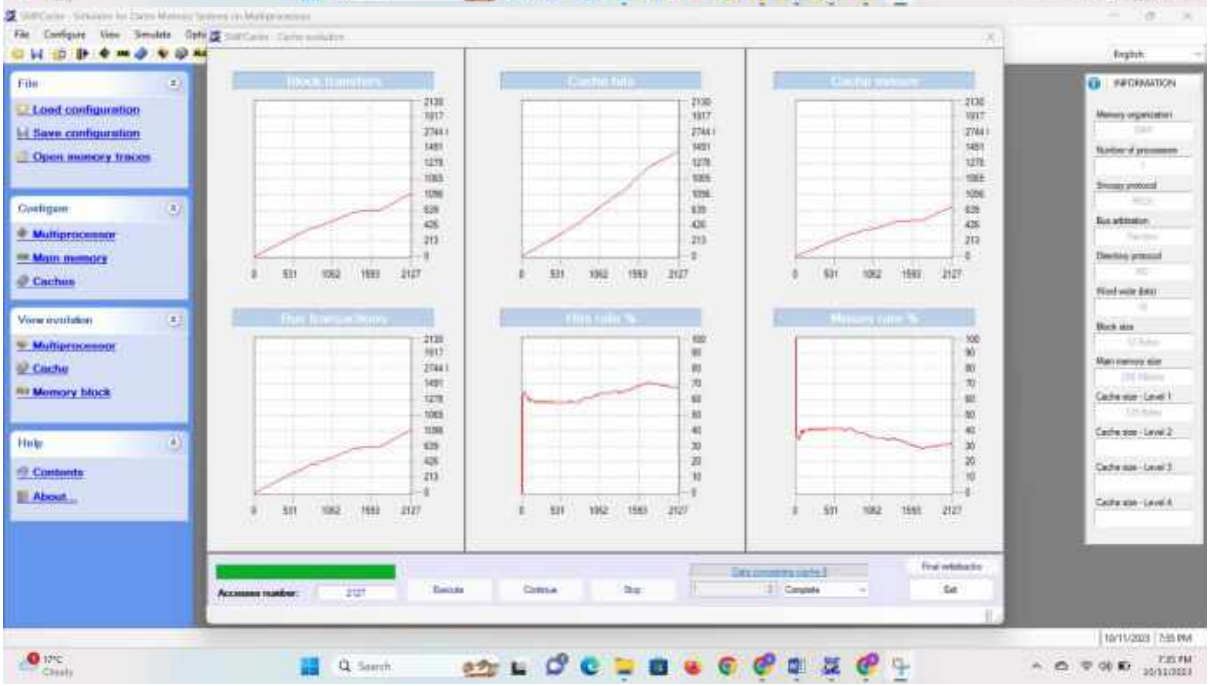
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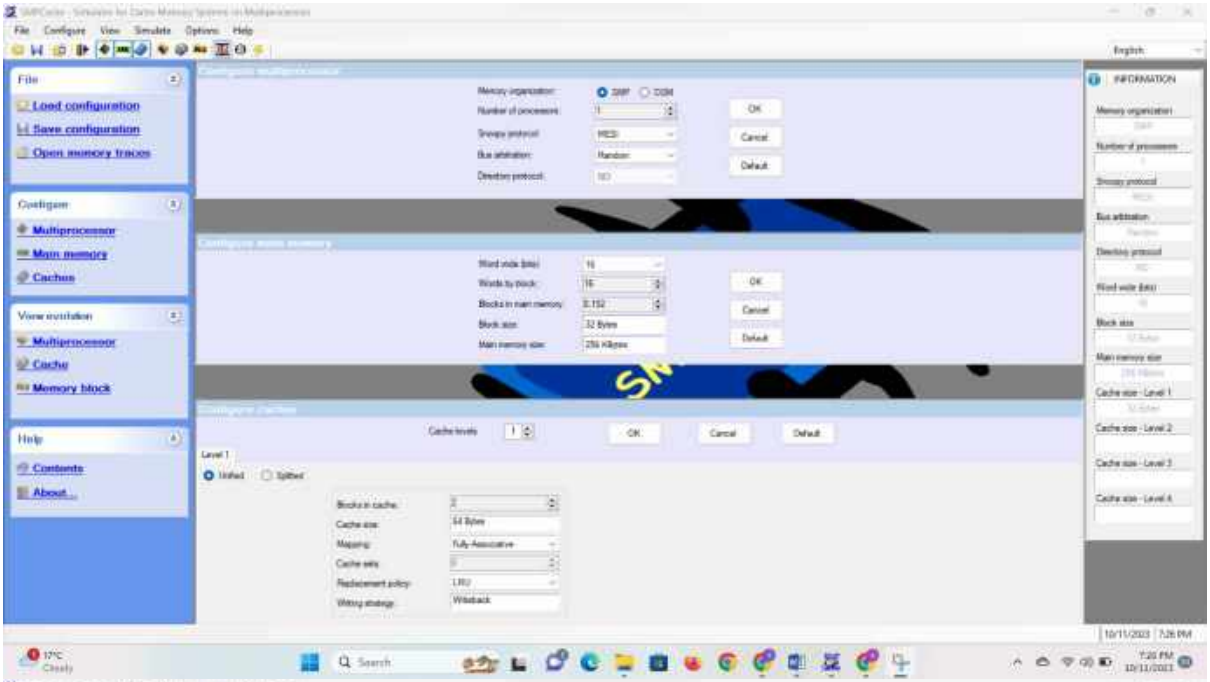
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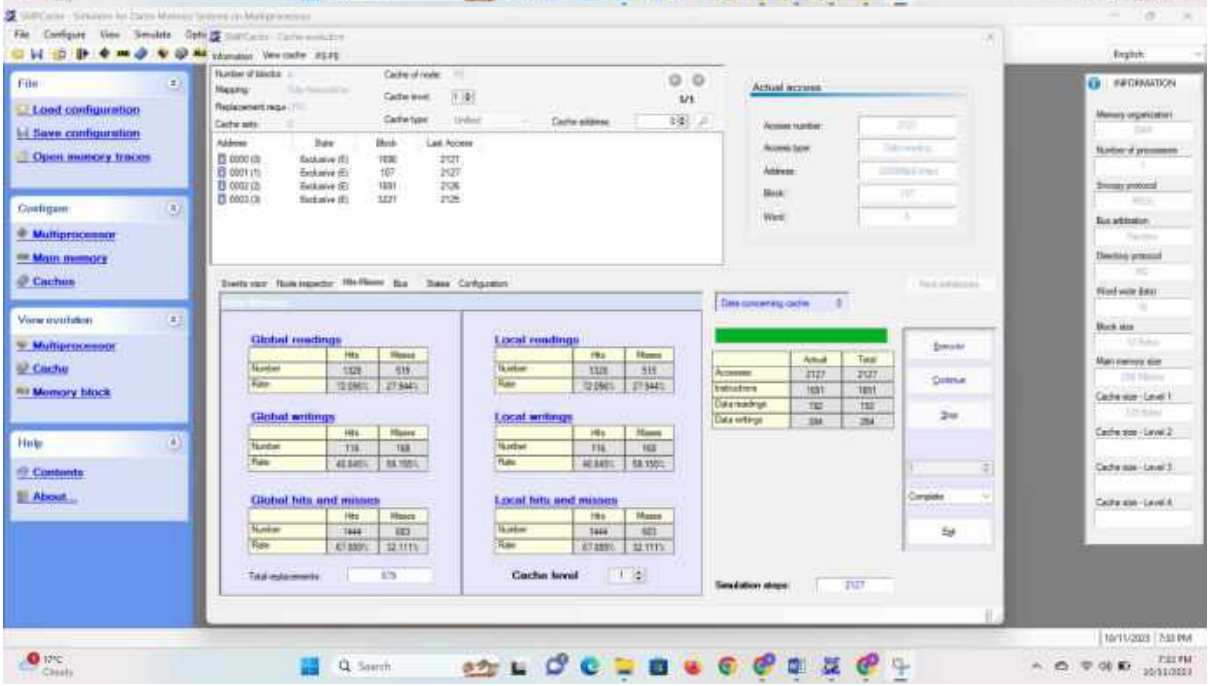
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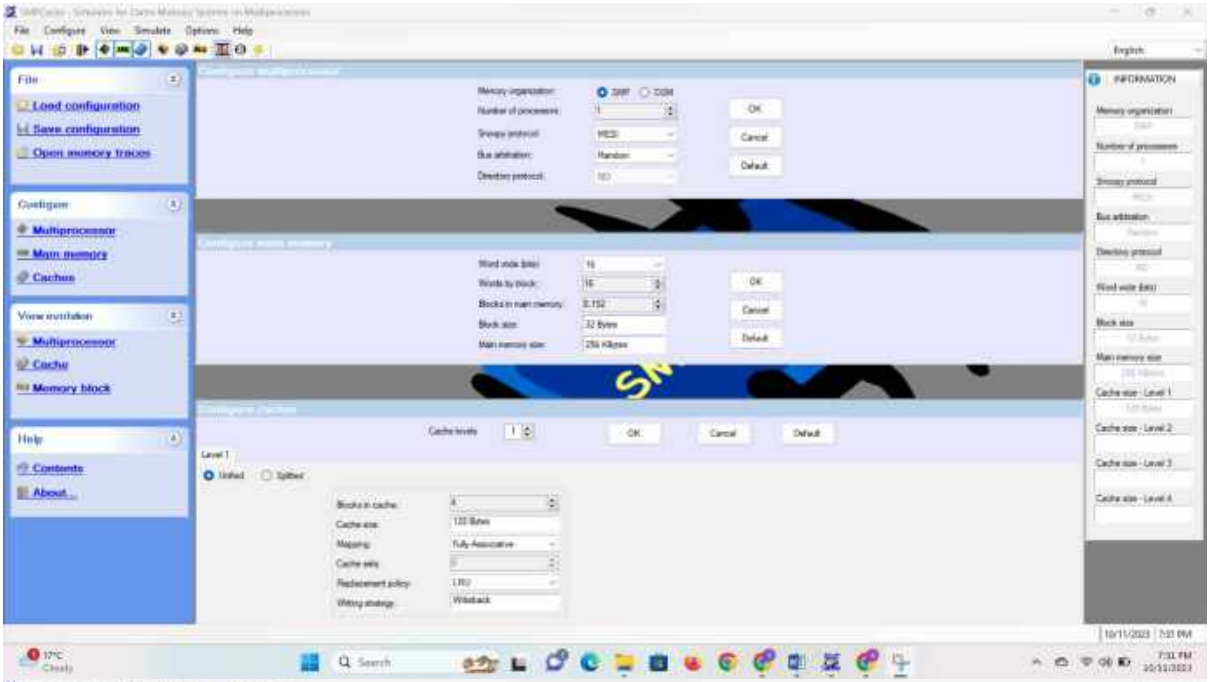
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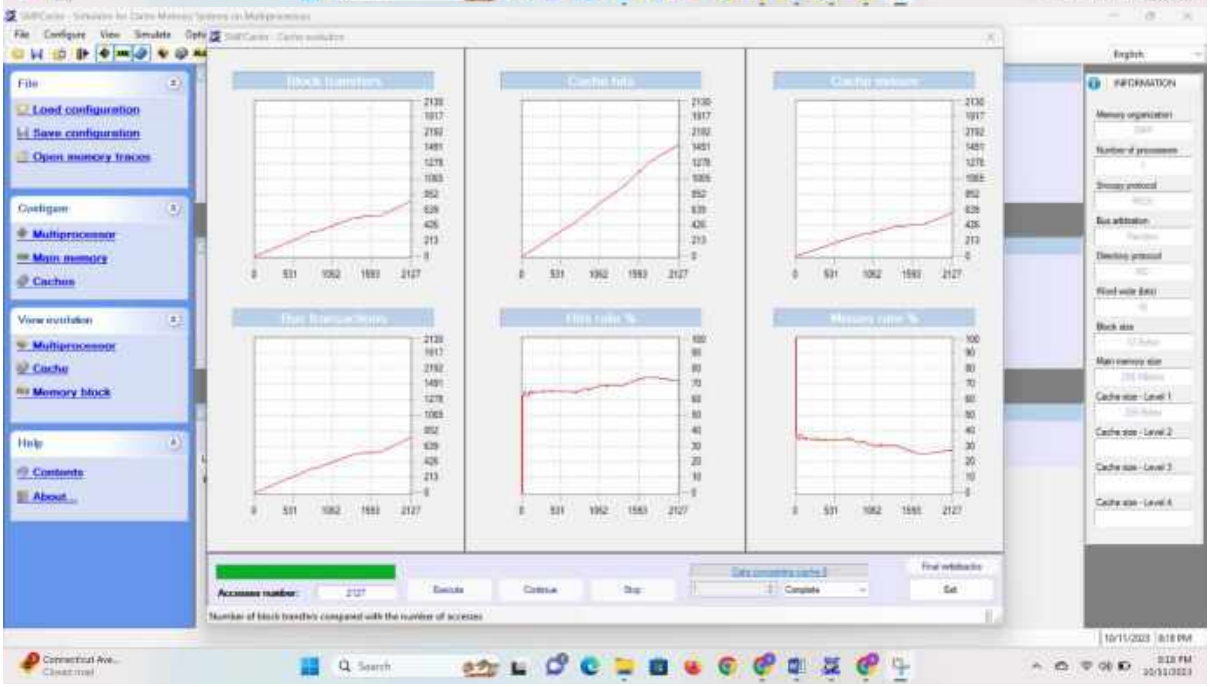
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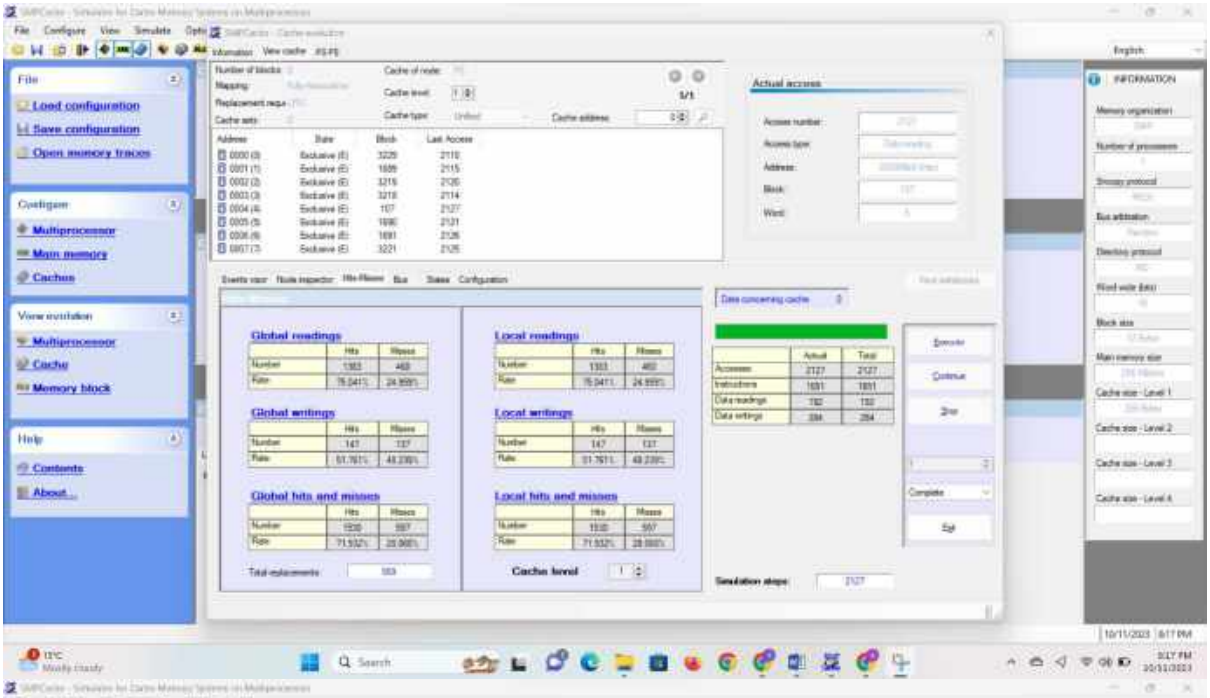
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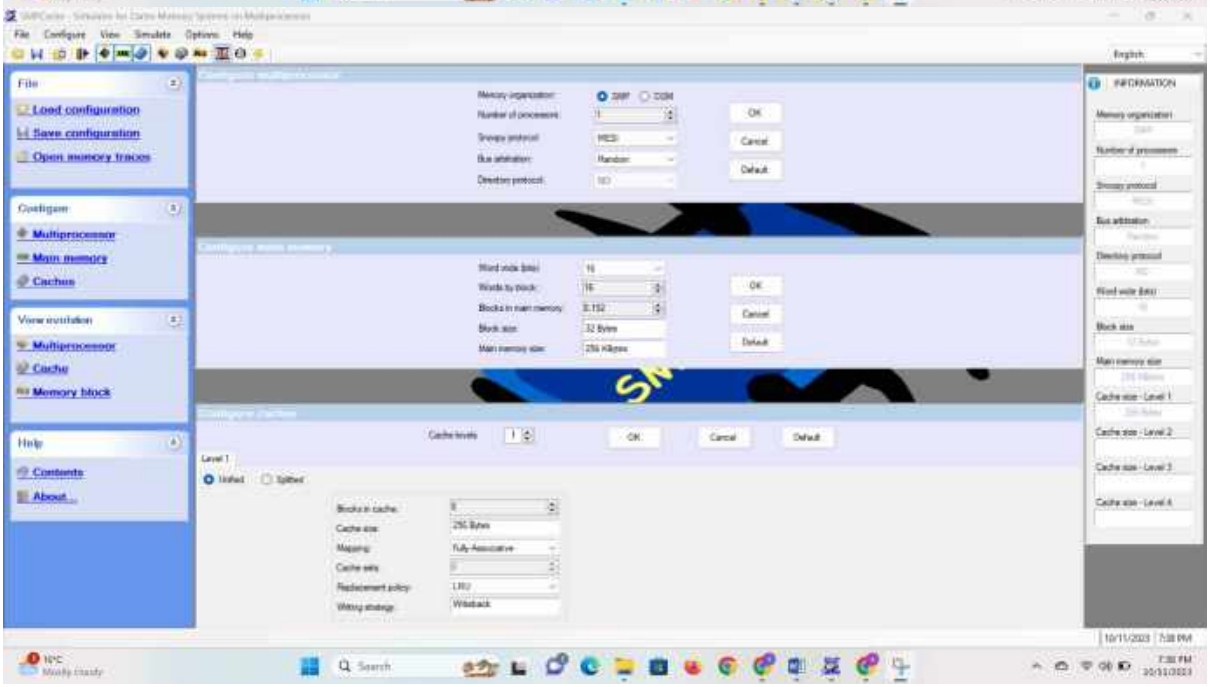
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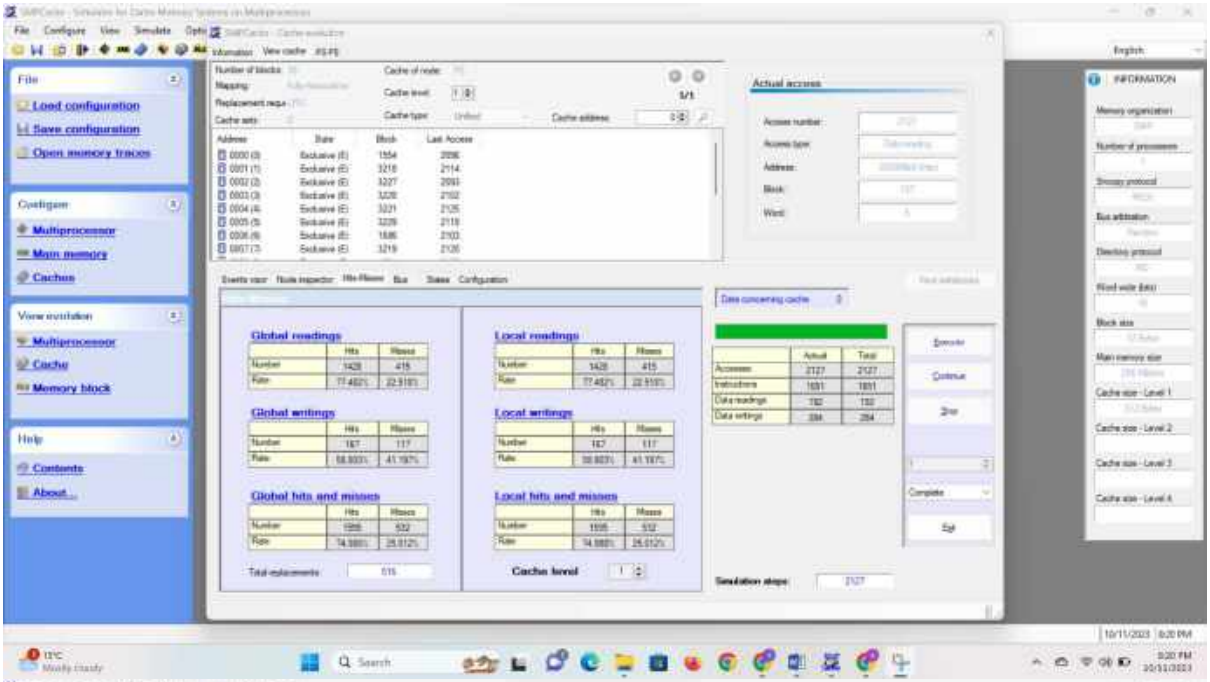
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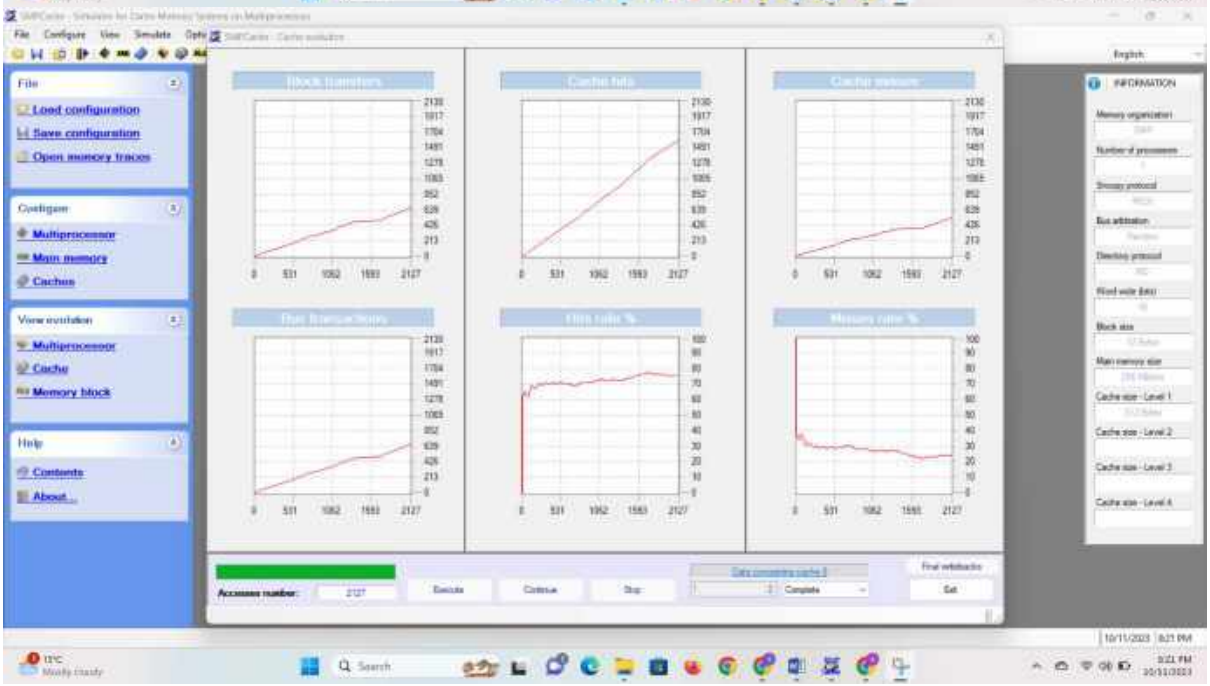
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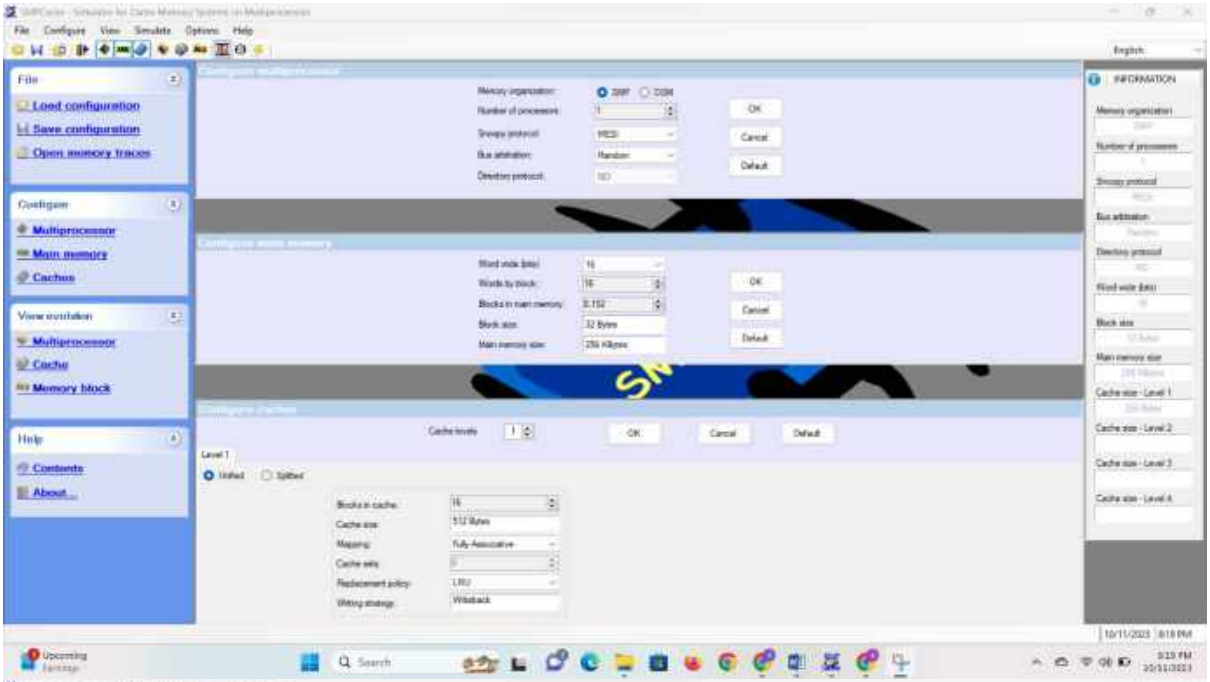
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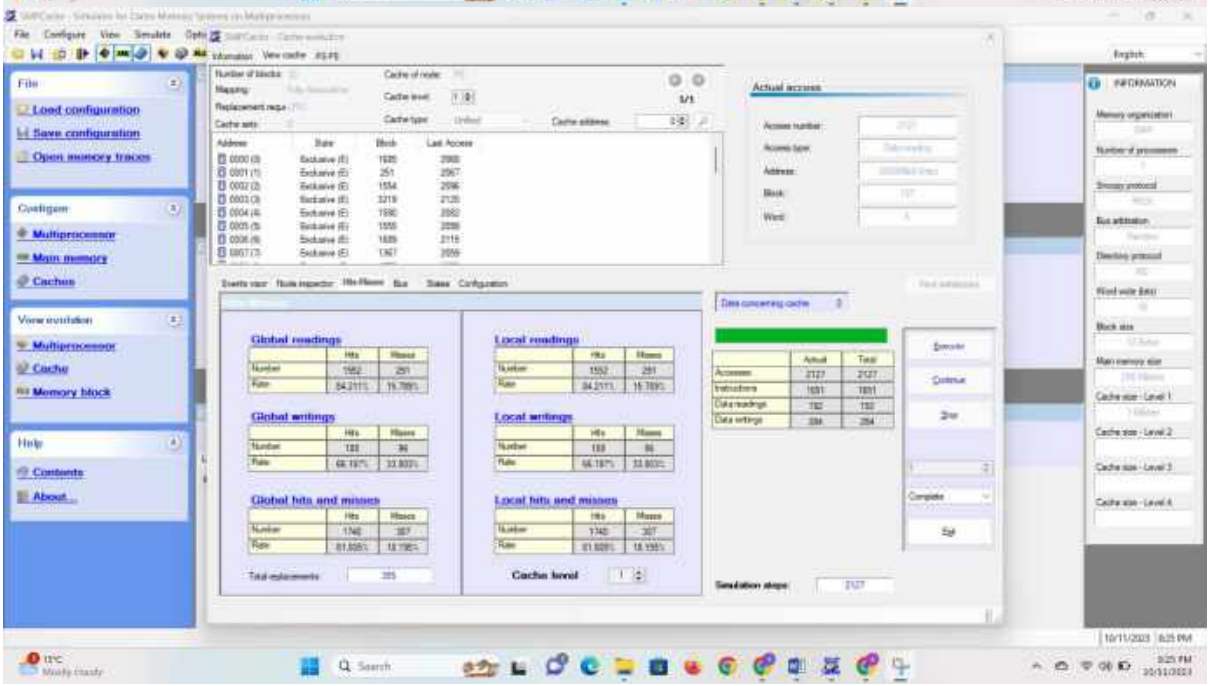
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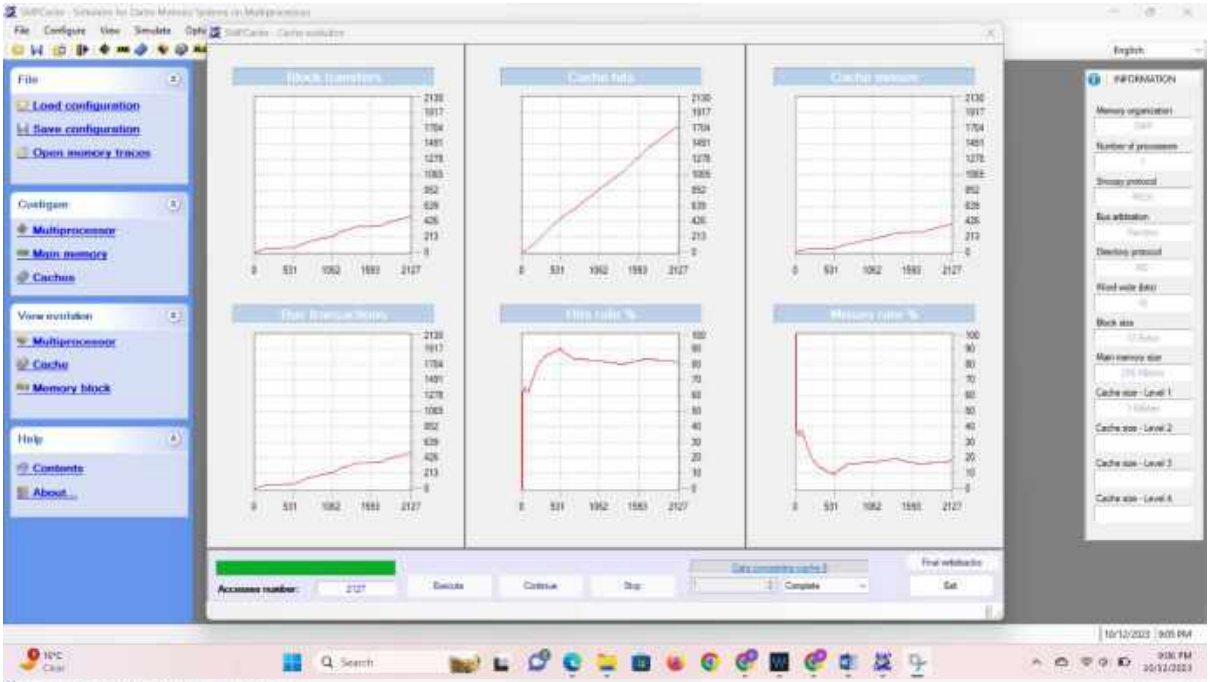
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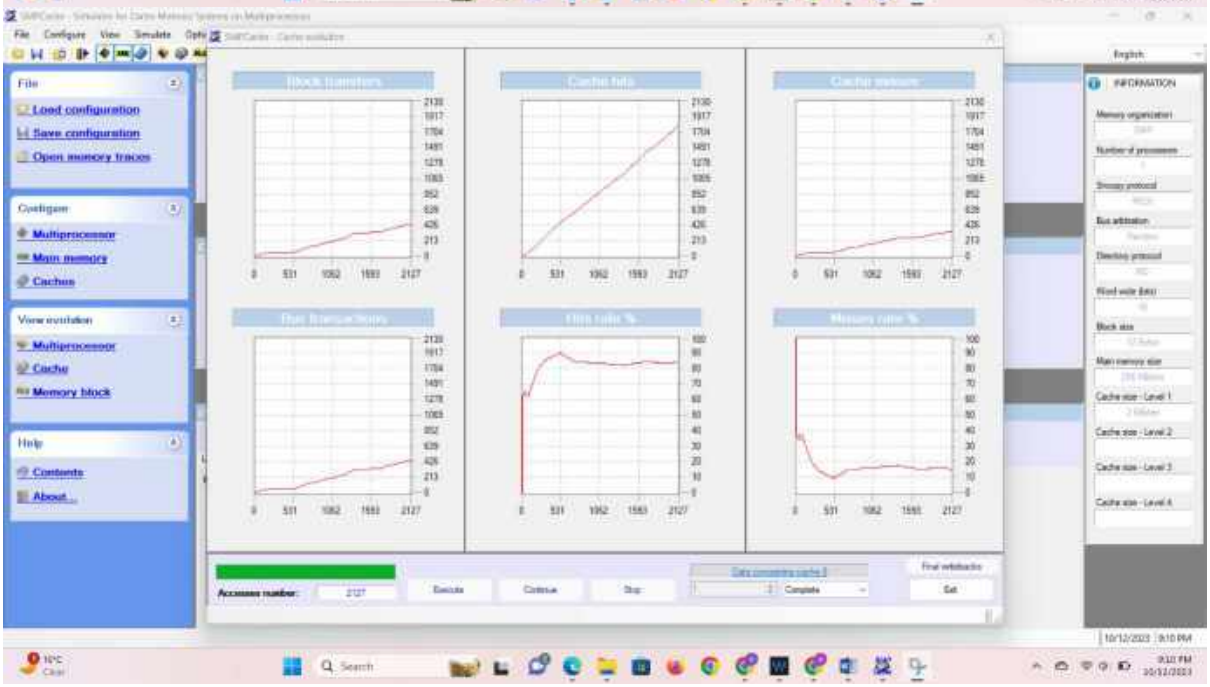
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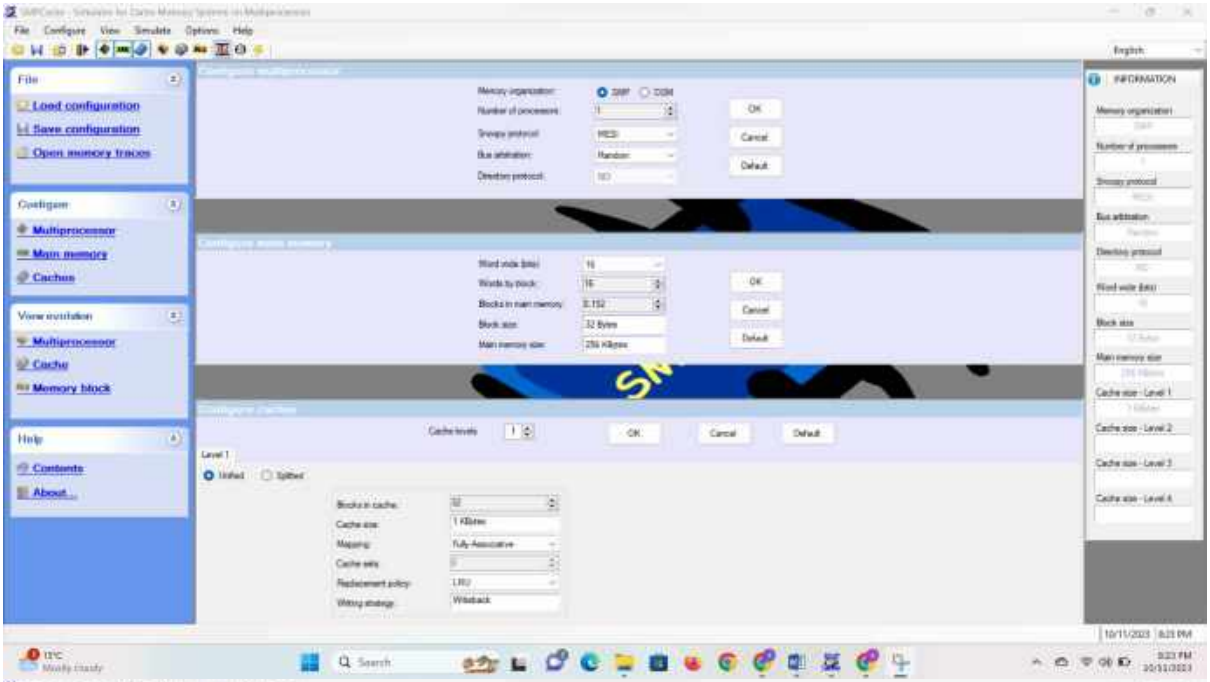
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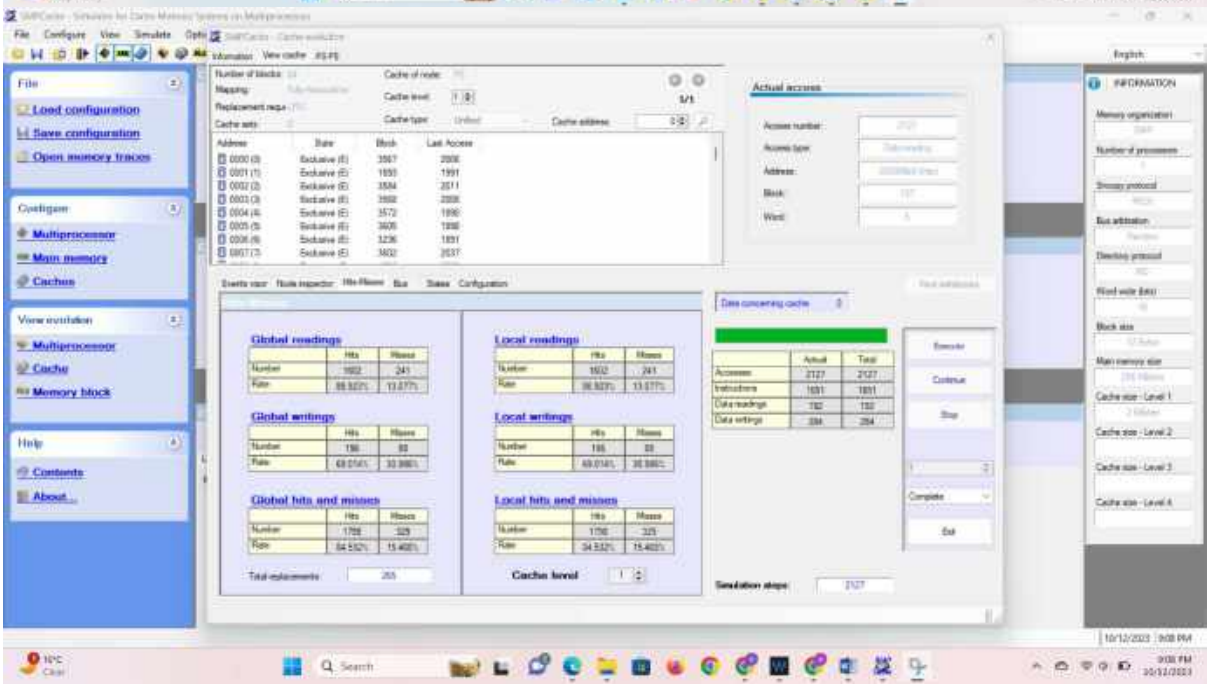
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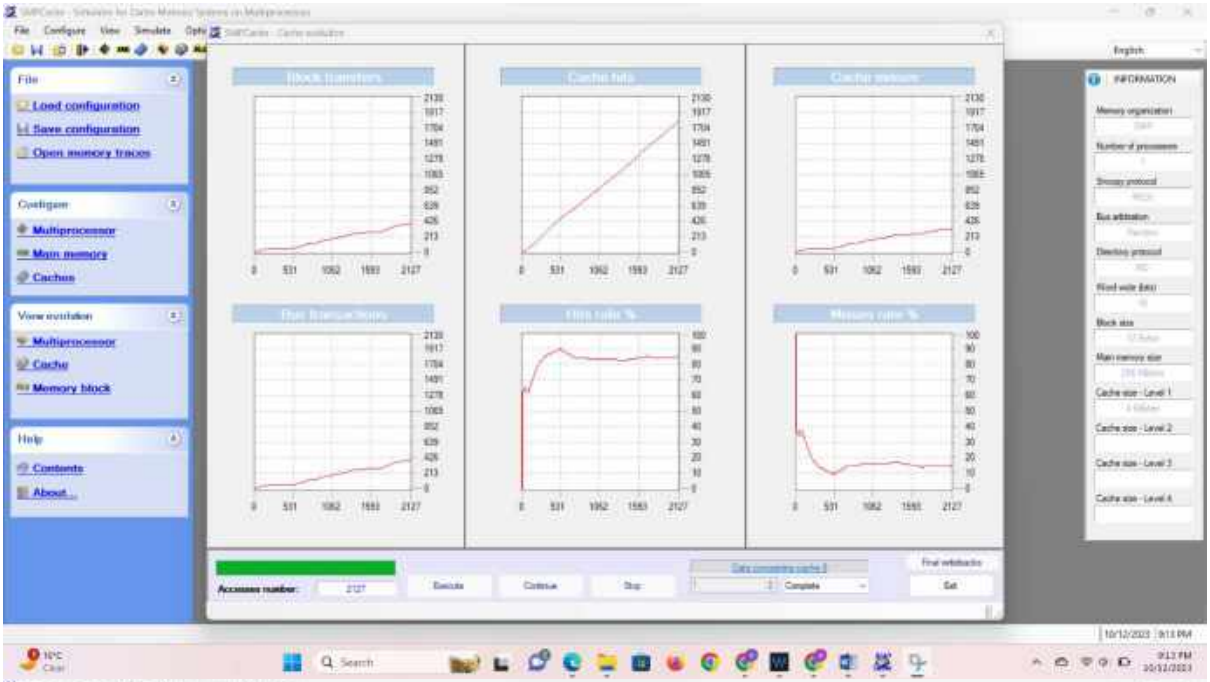
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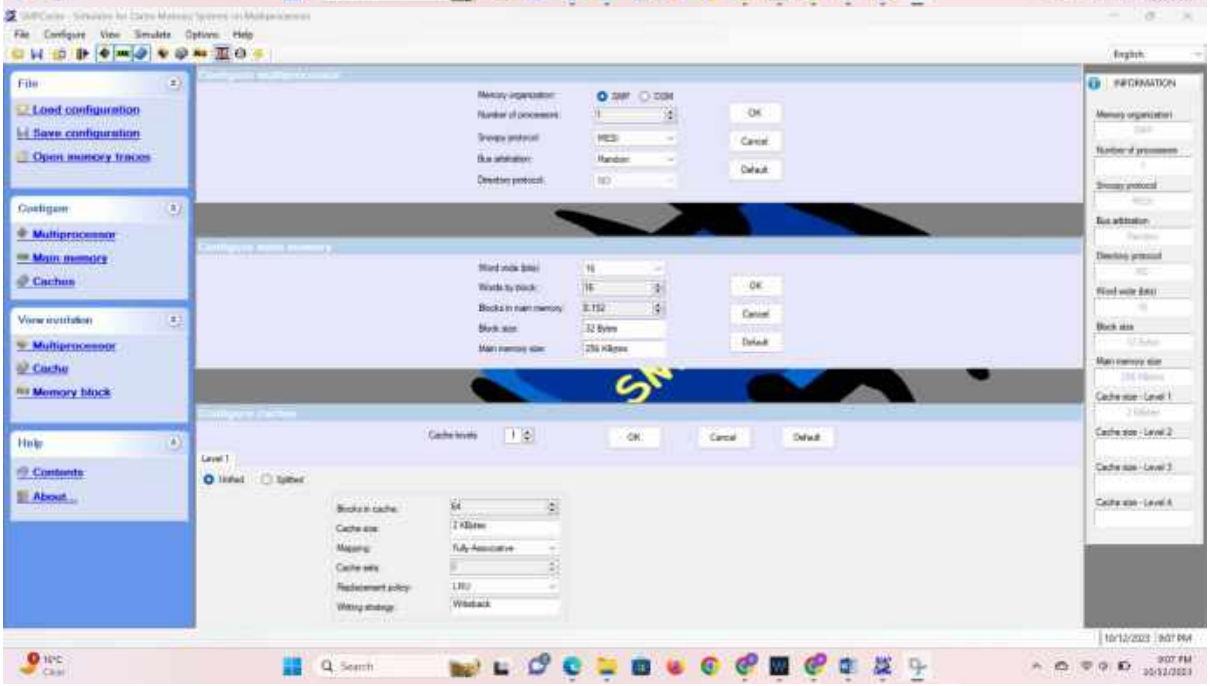
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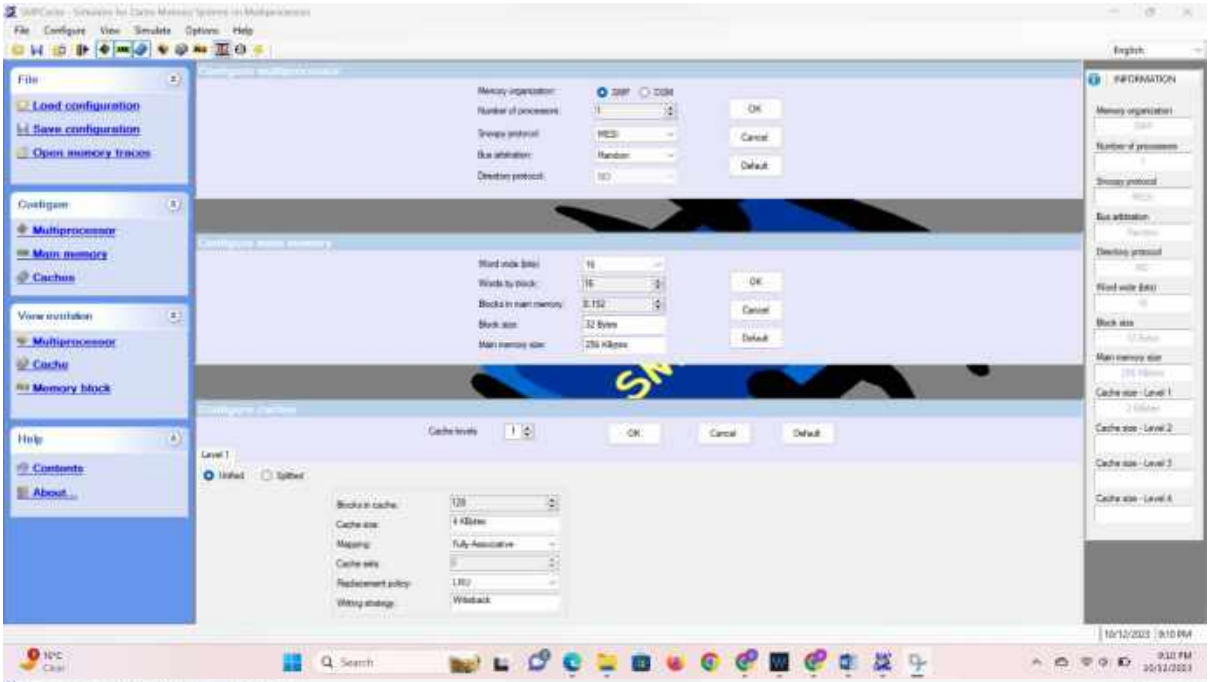
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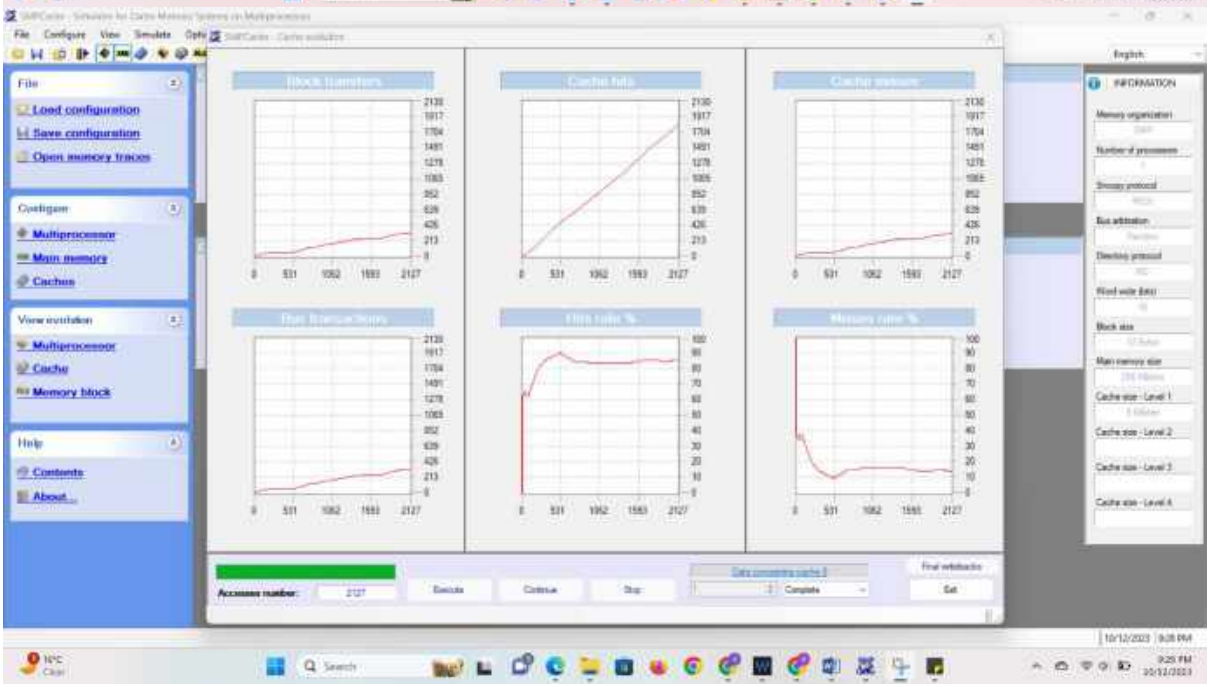
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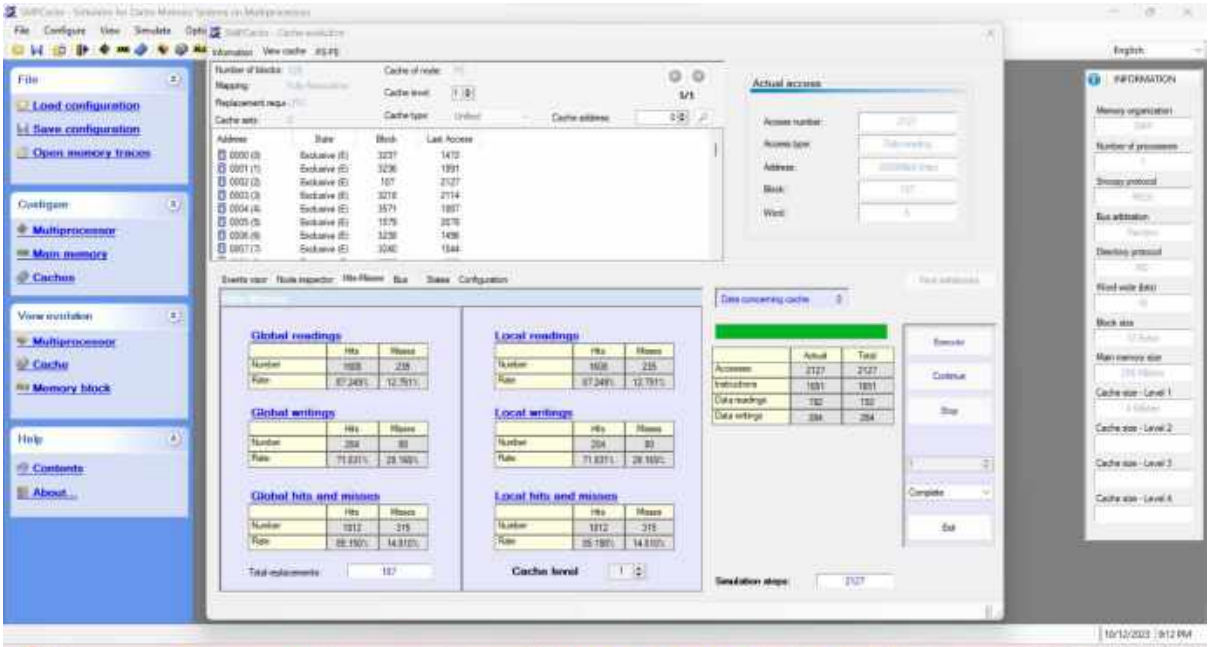
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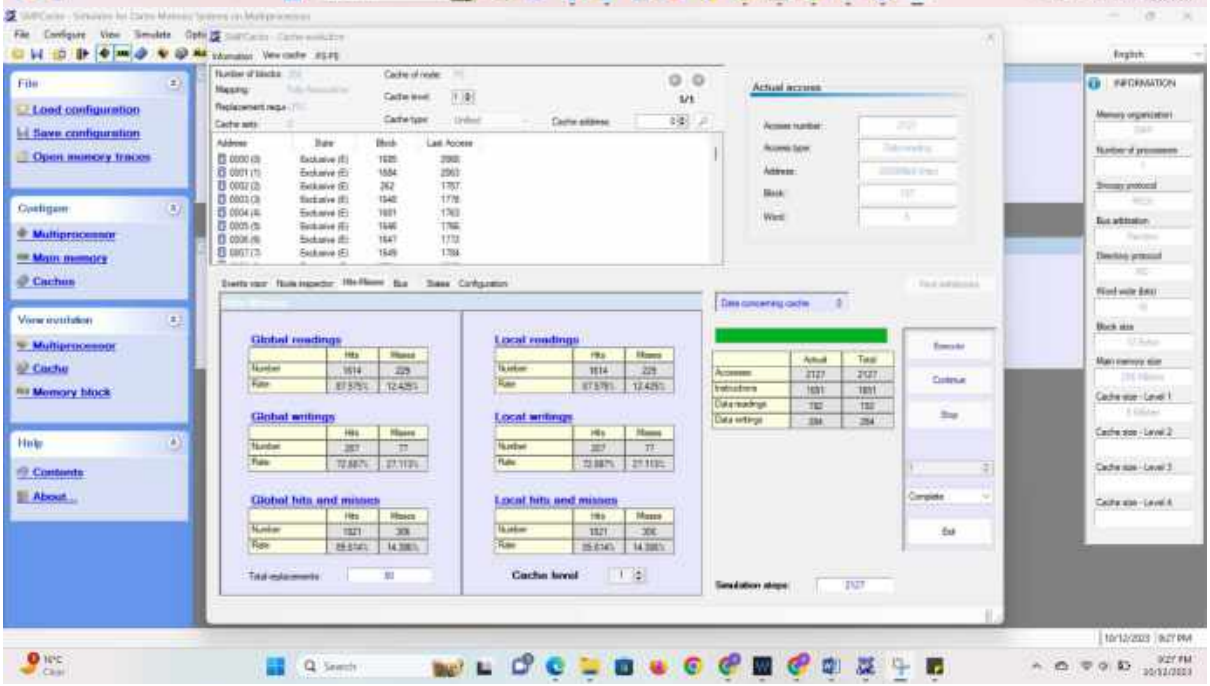
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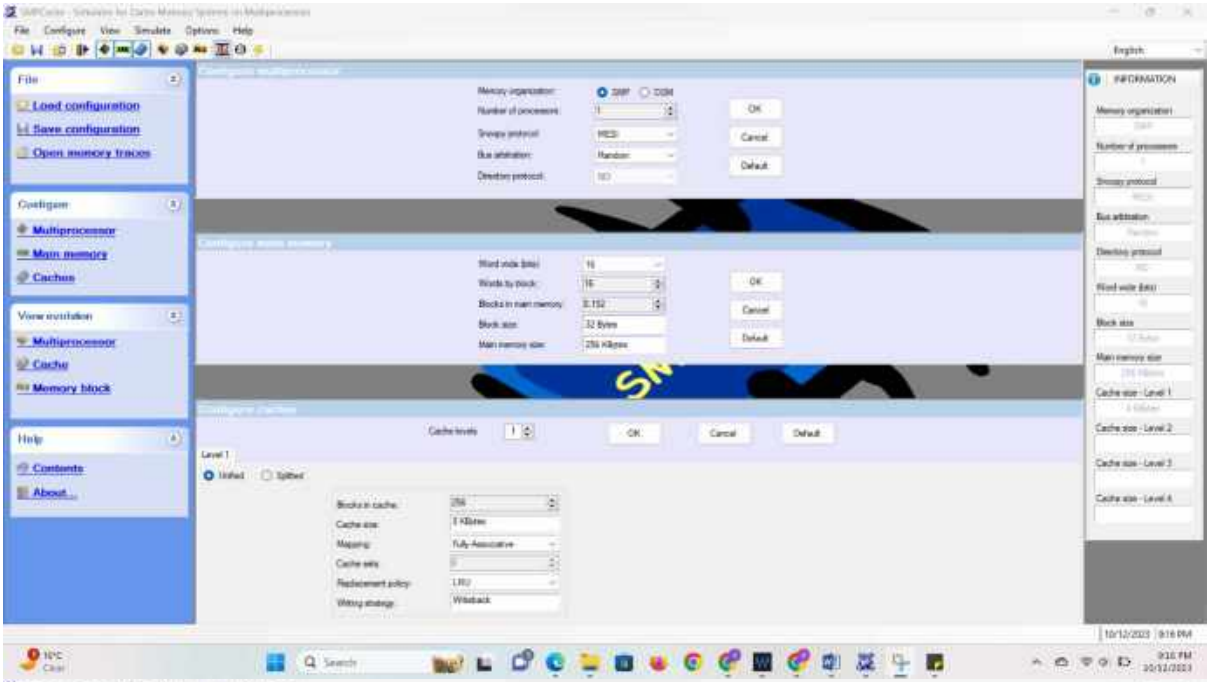
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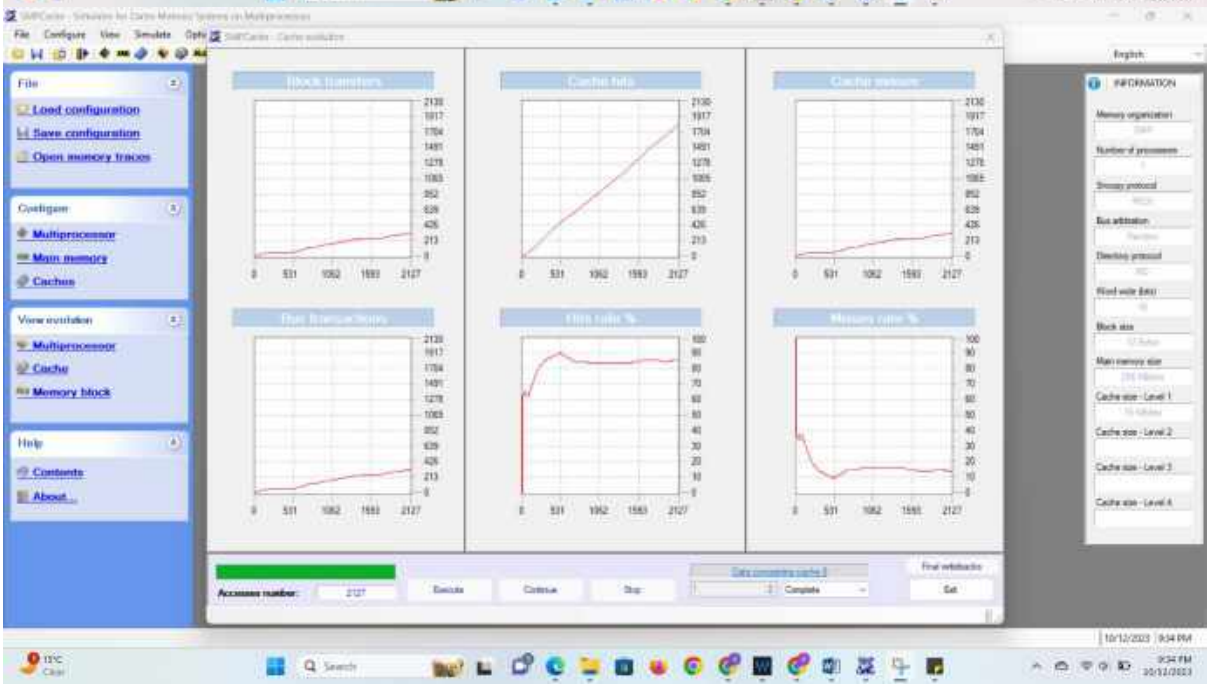
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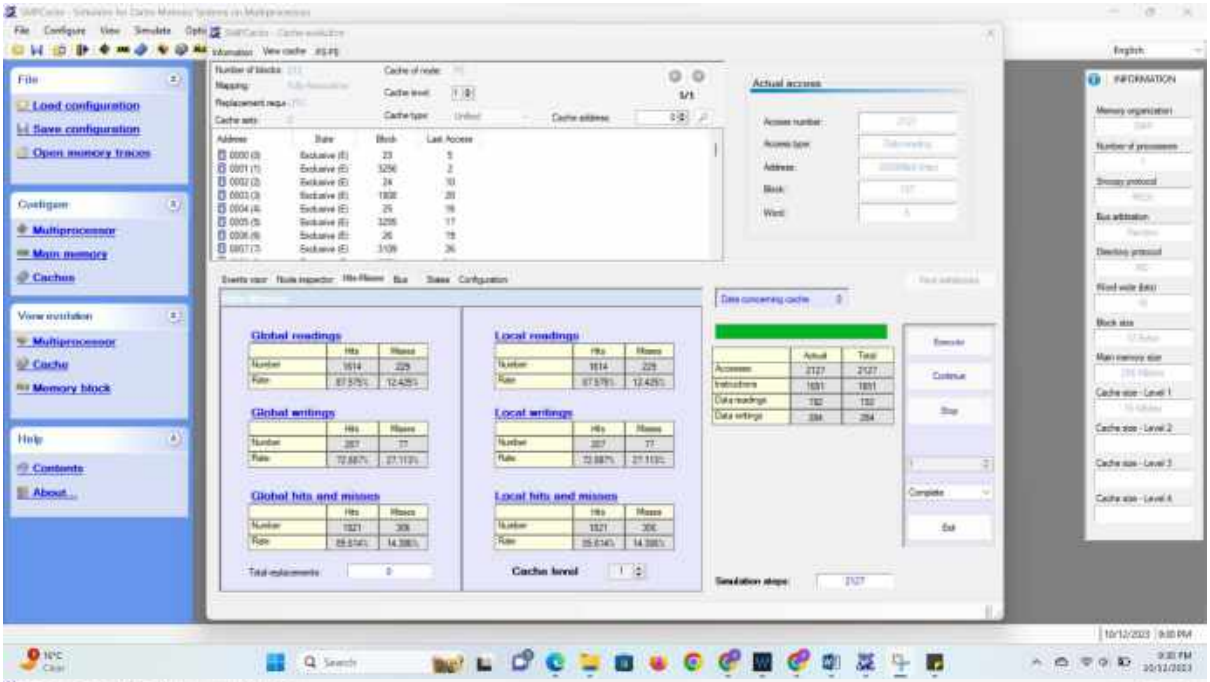
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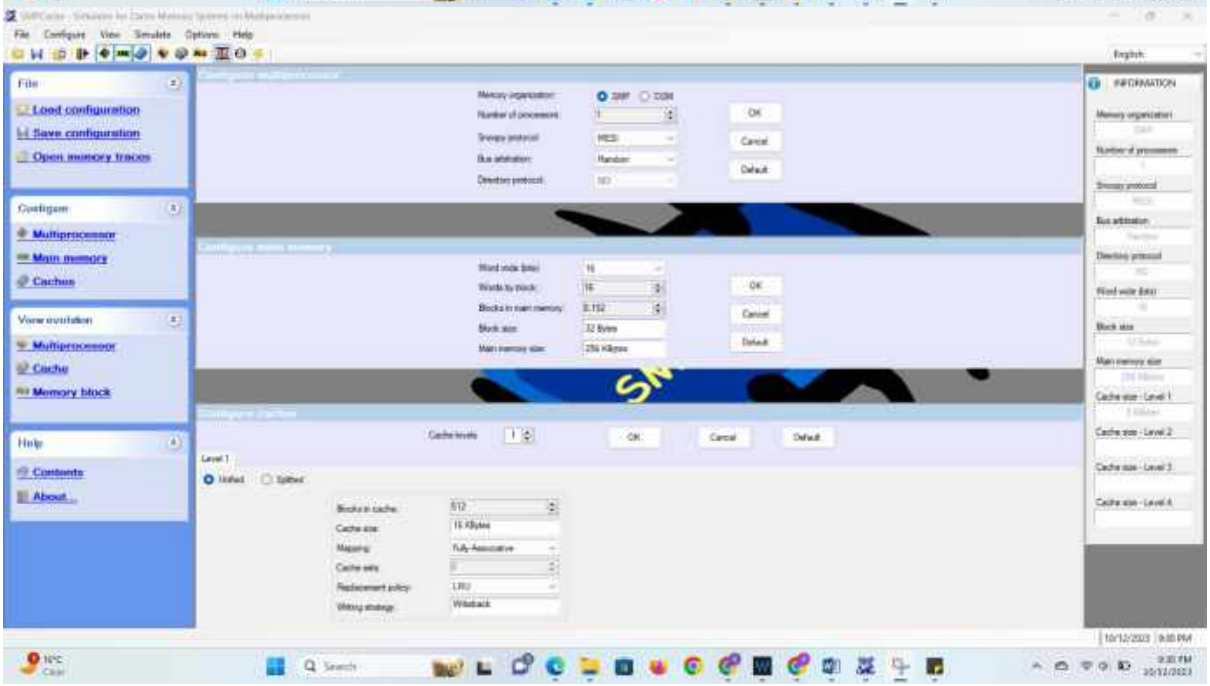
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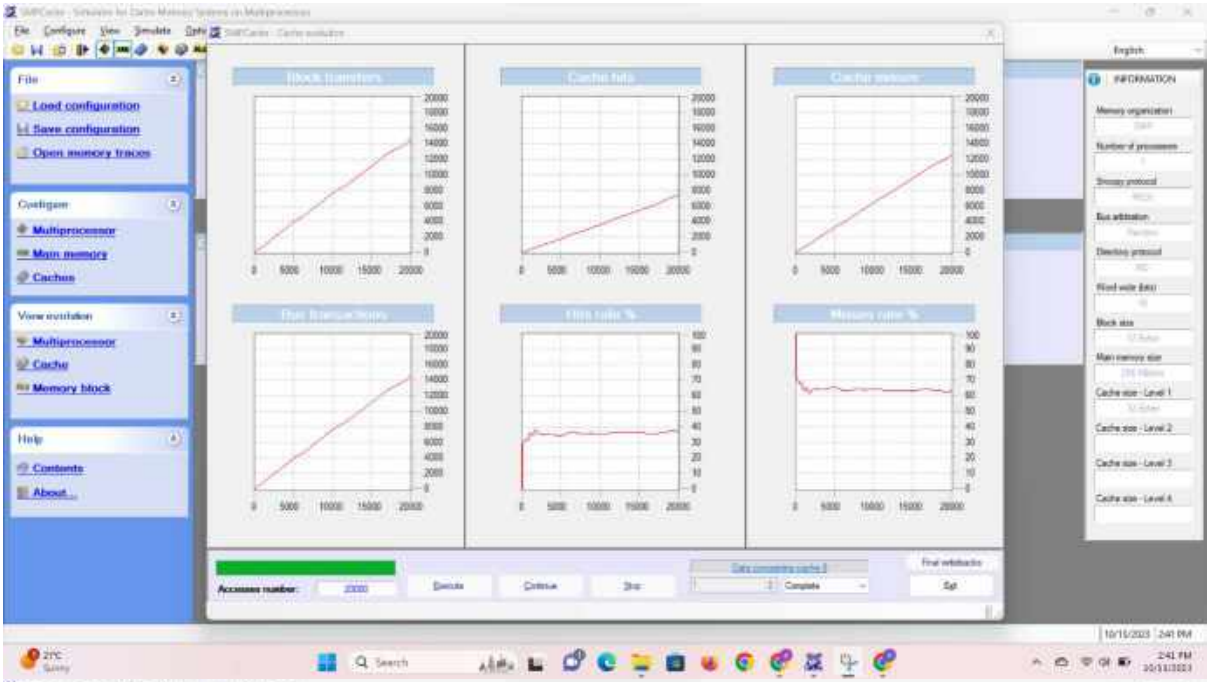
Mdljd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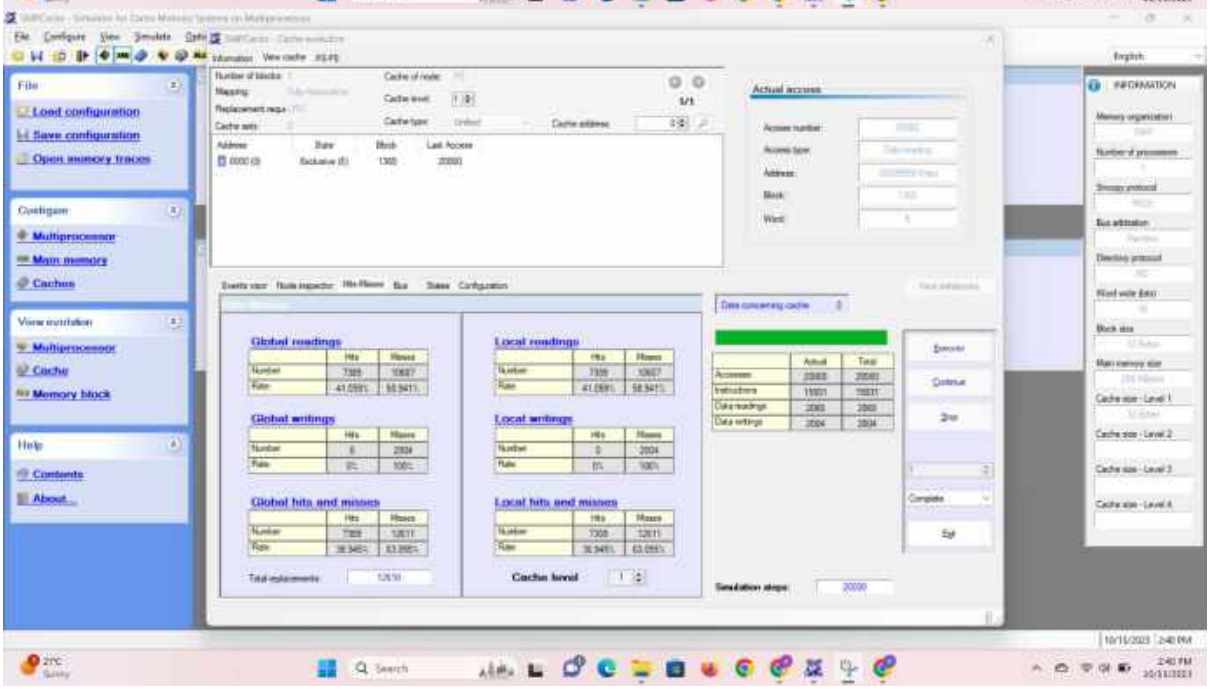
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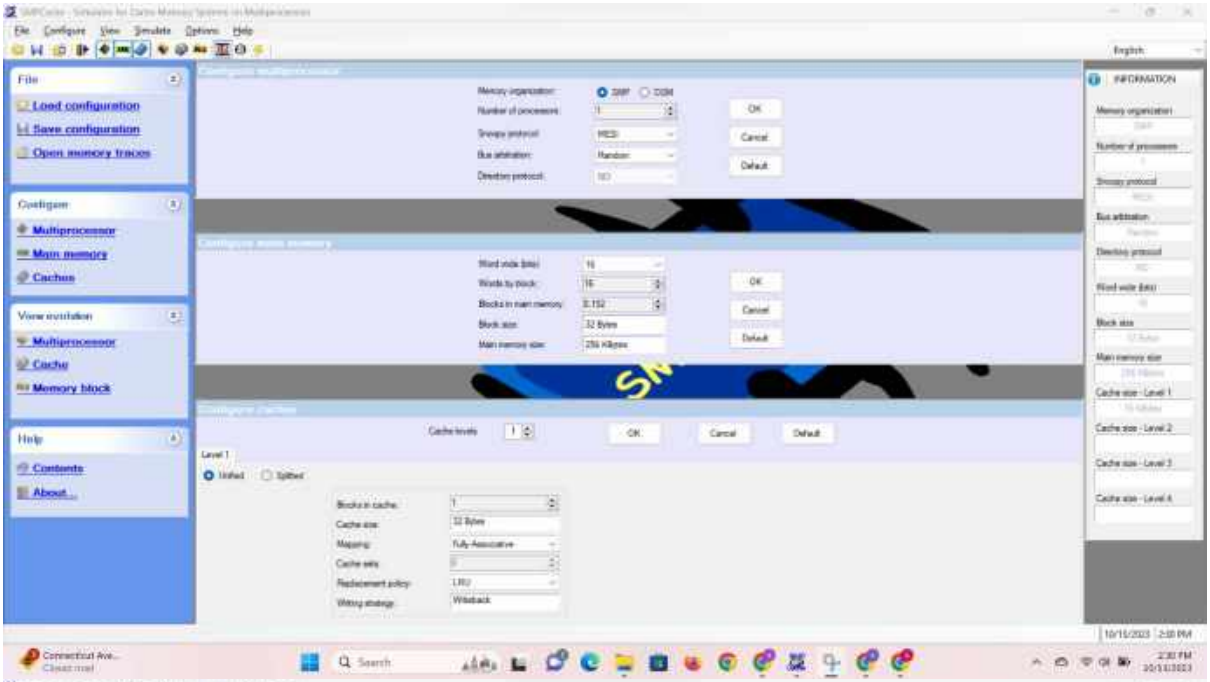
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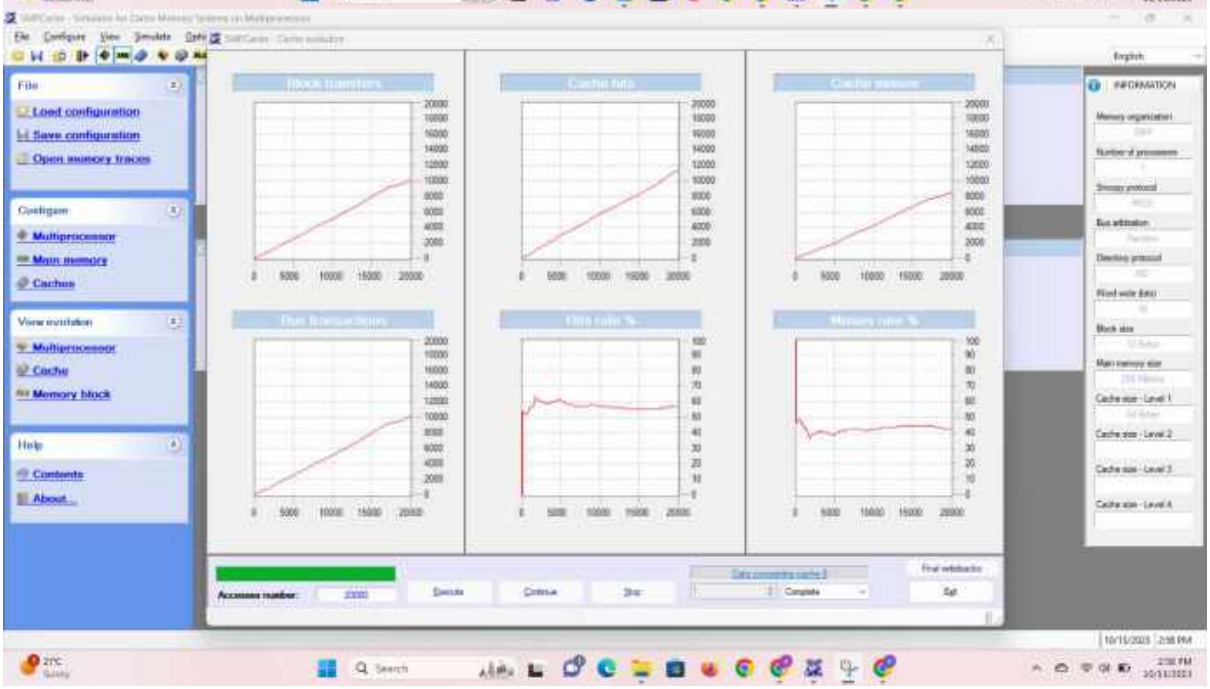
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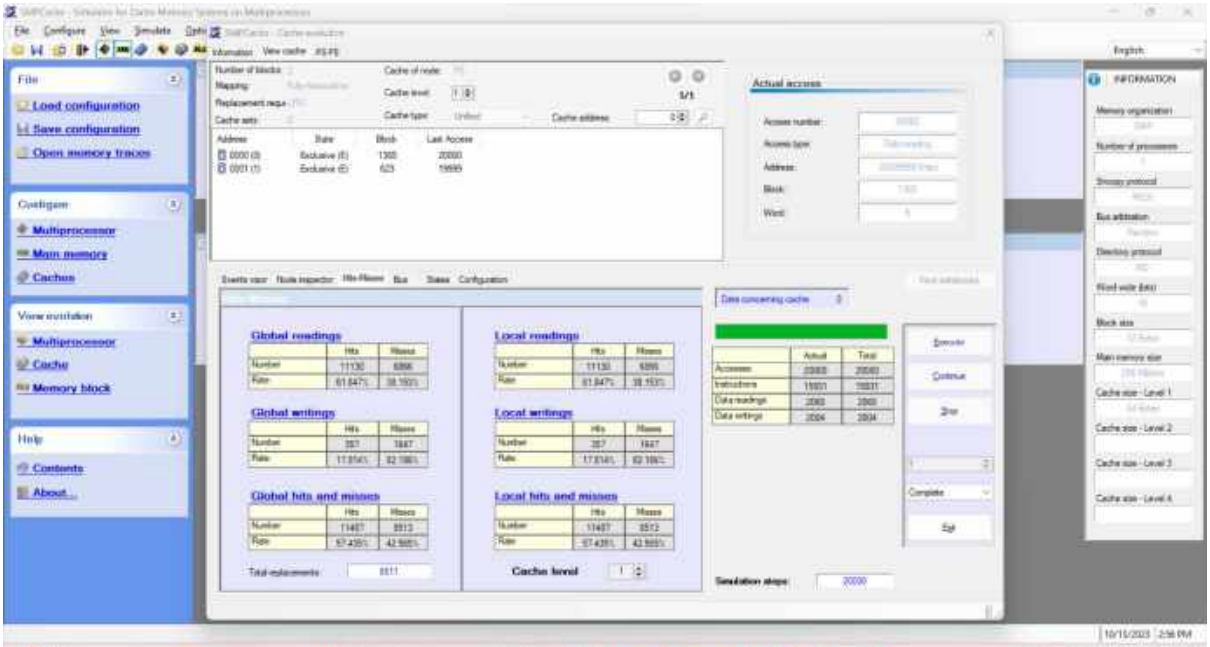
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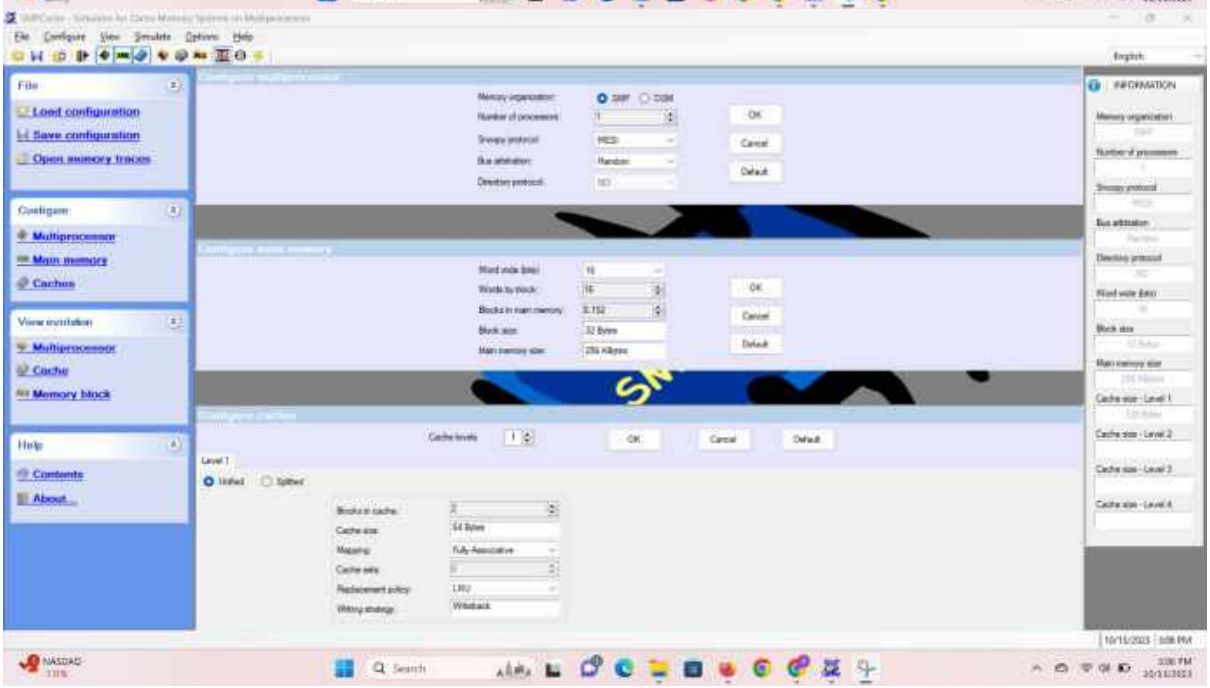
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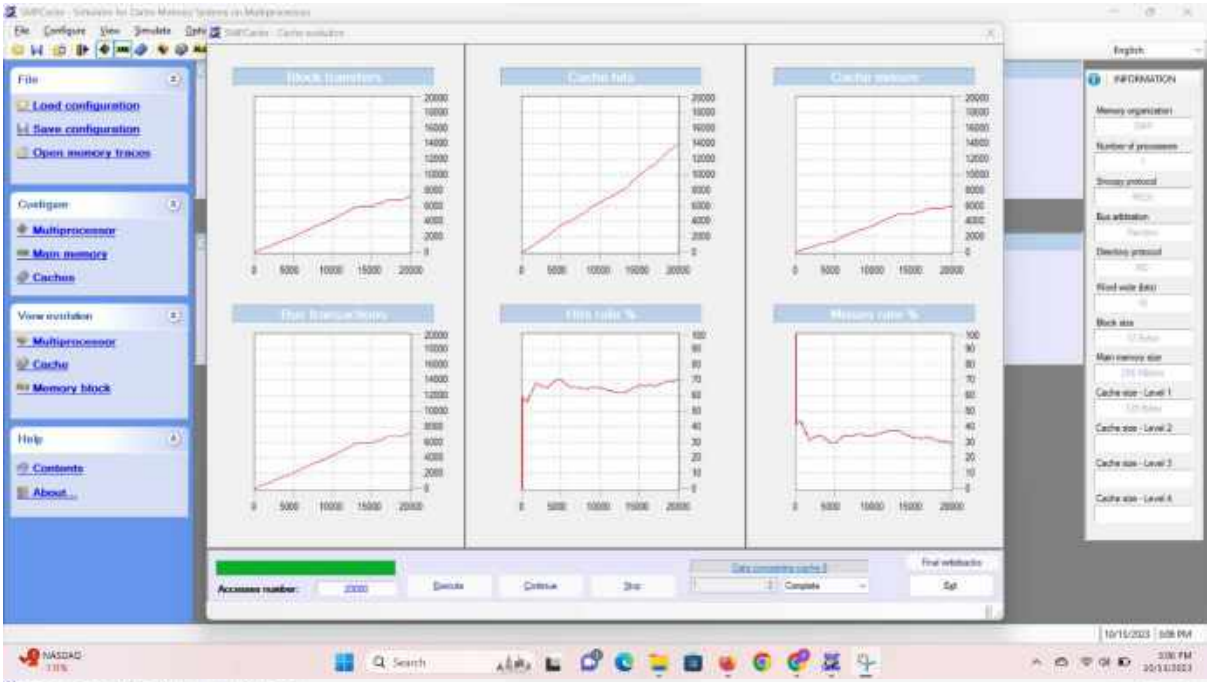
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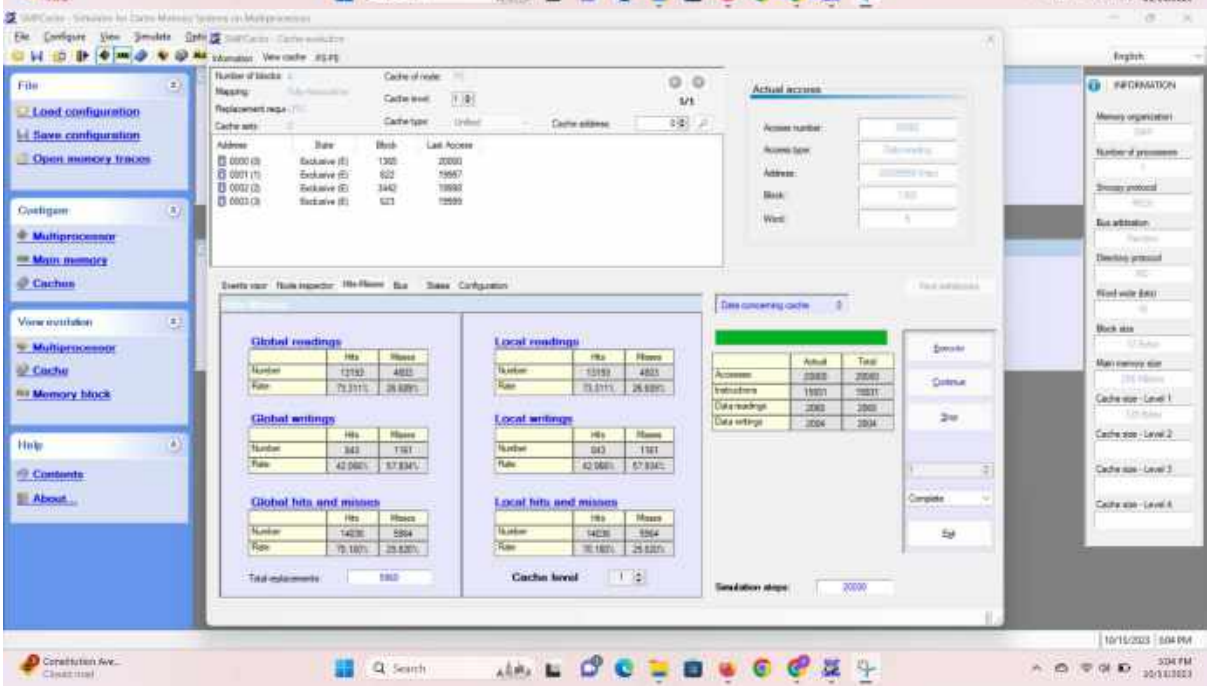
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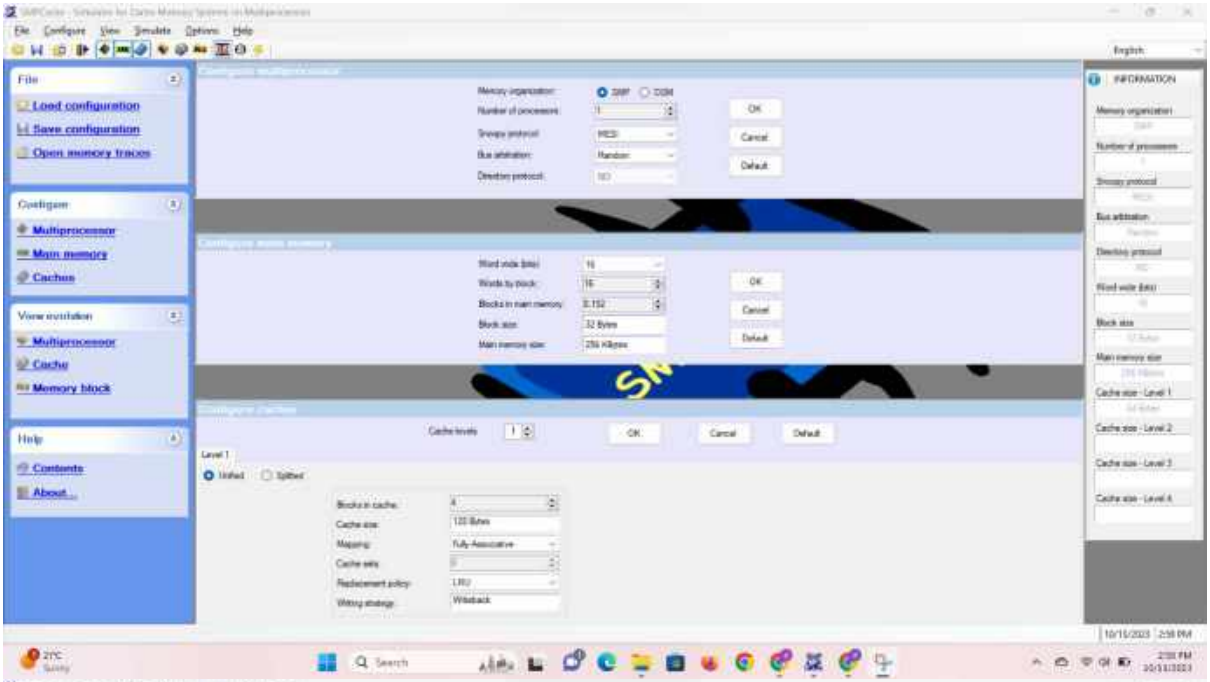
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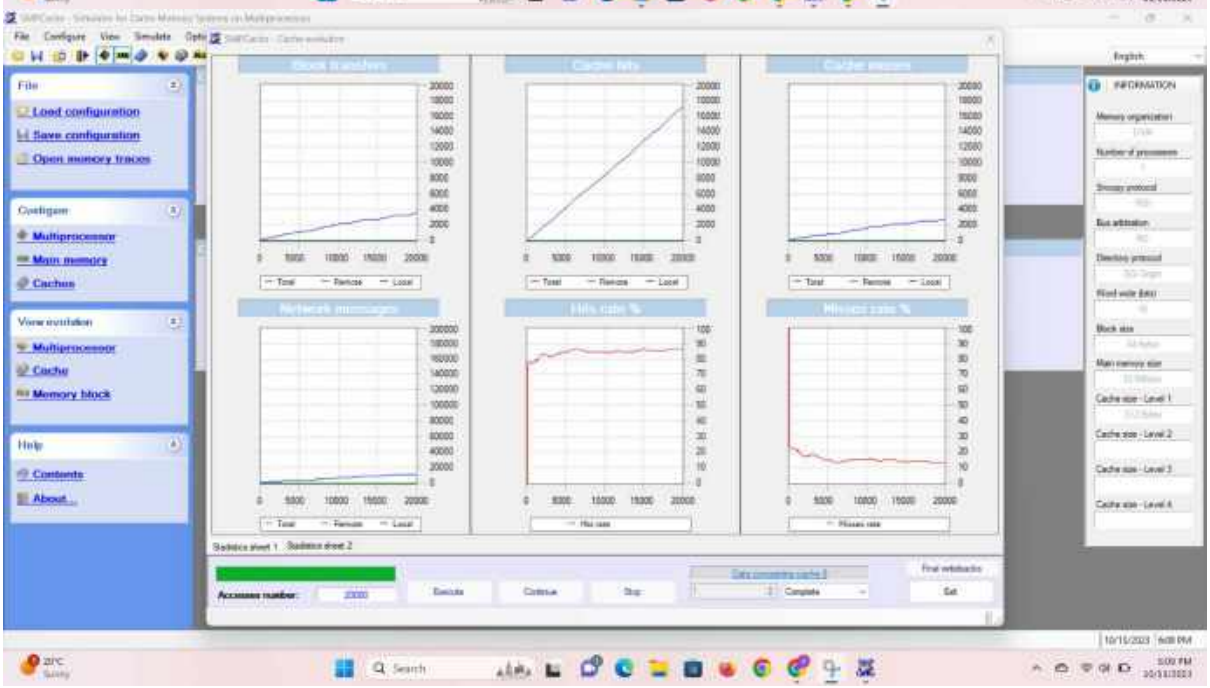
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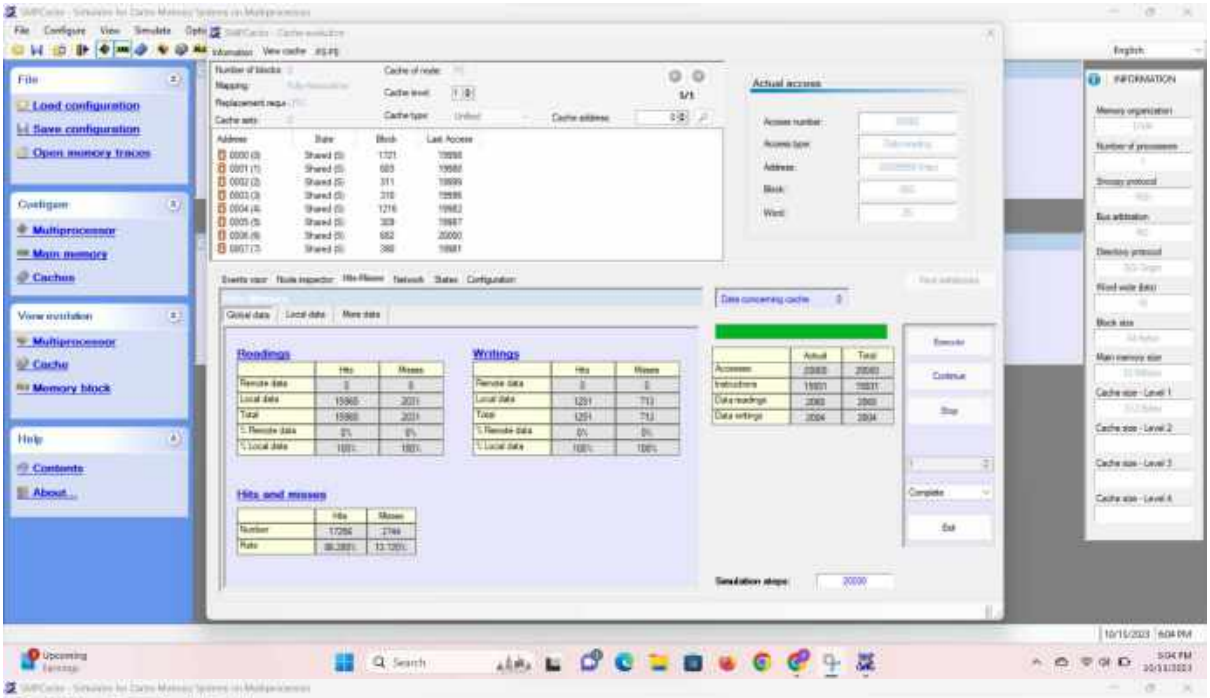
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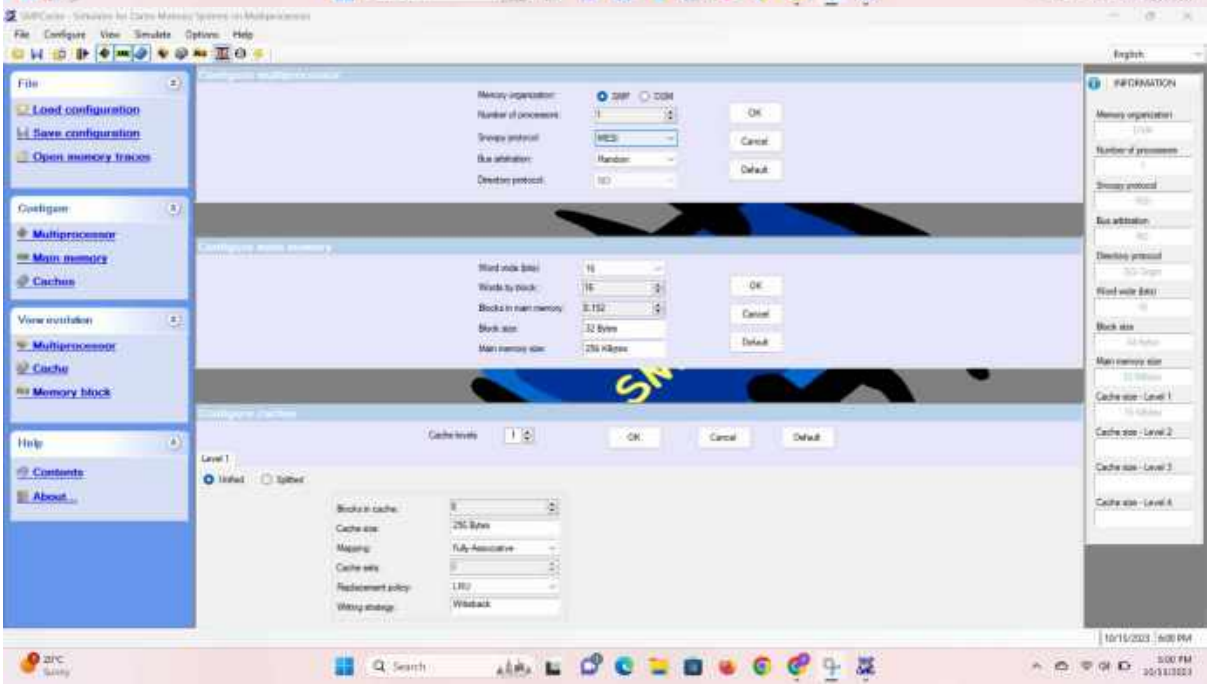
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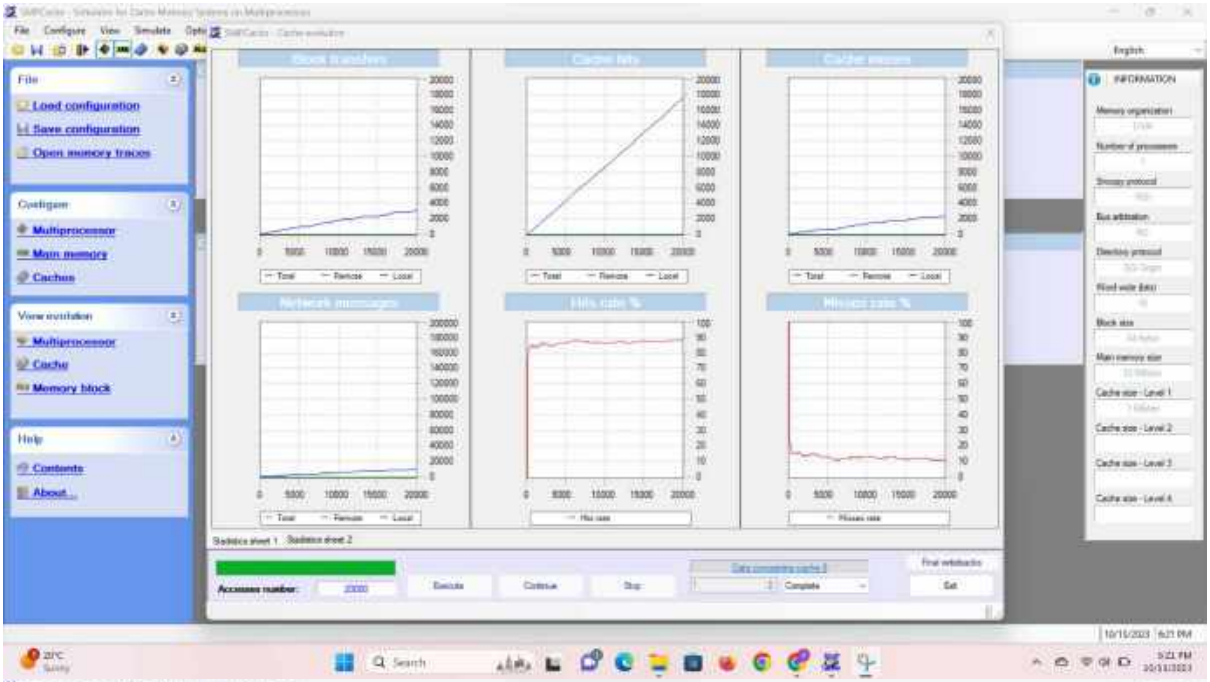
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Hits rate %
Misses rate %
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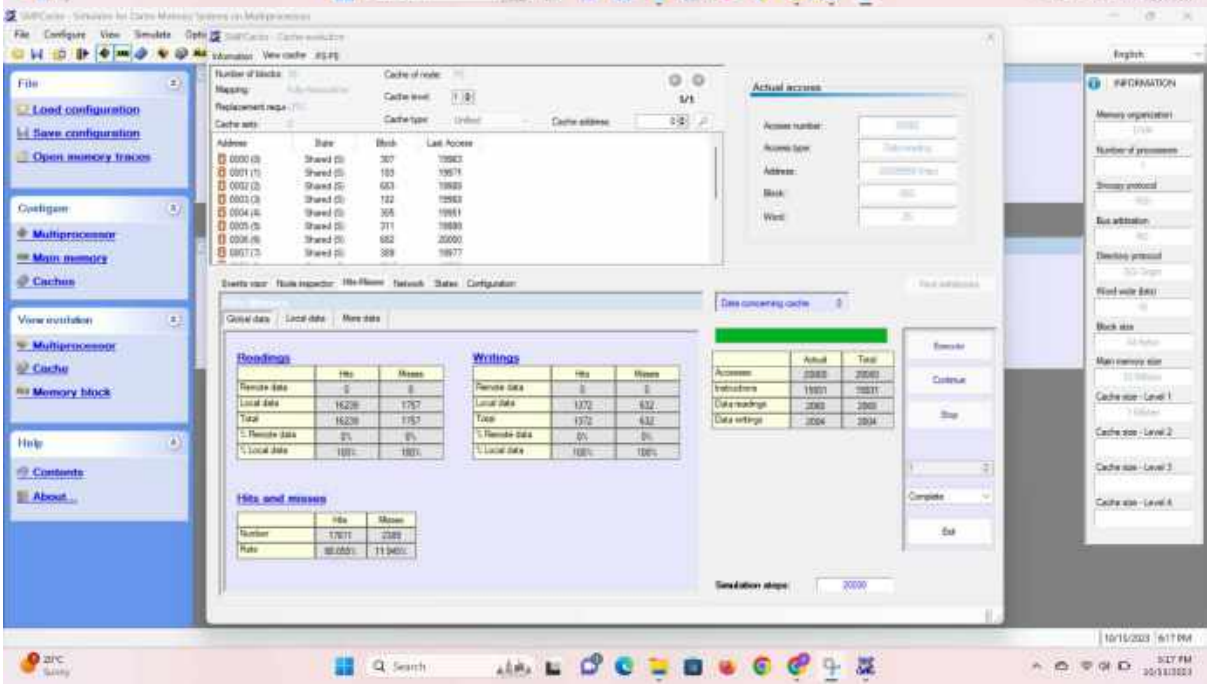
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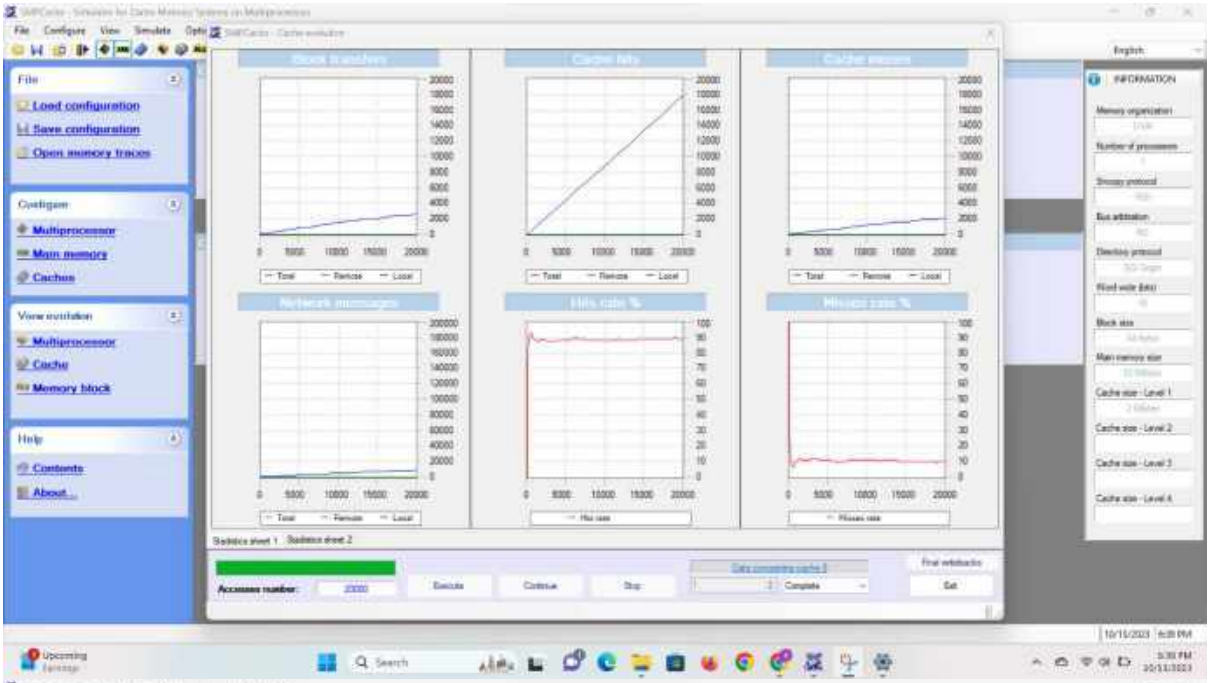
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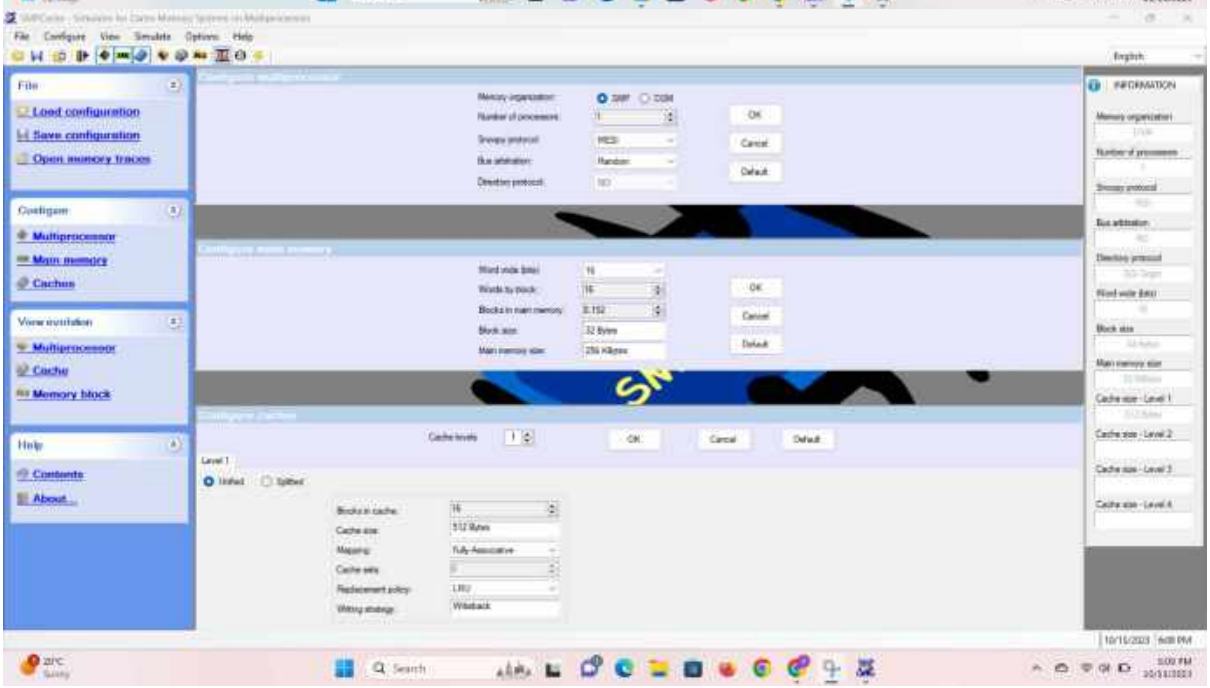
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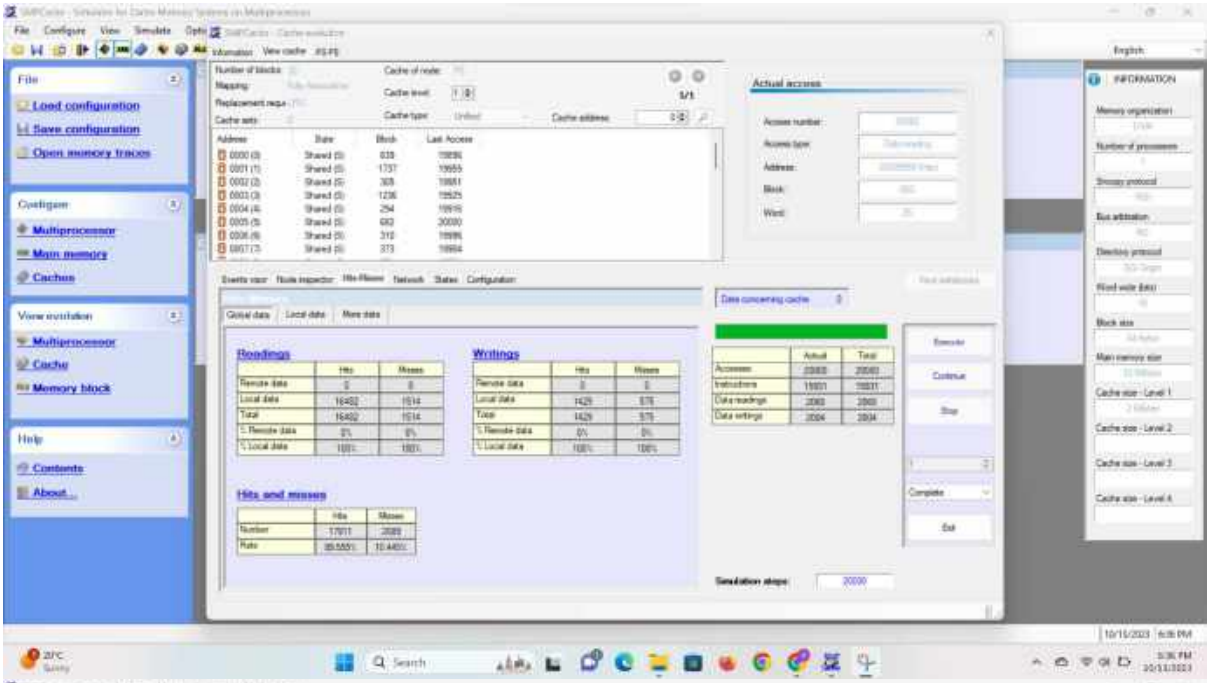
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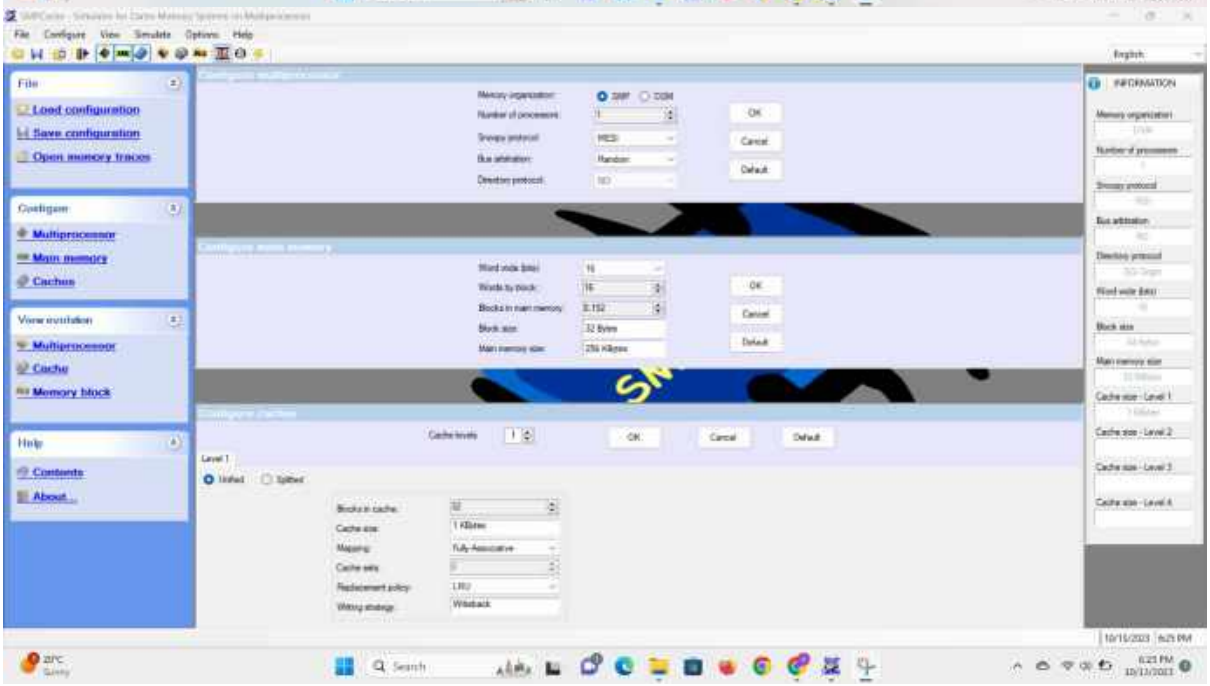
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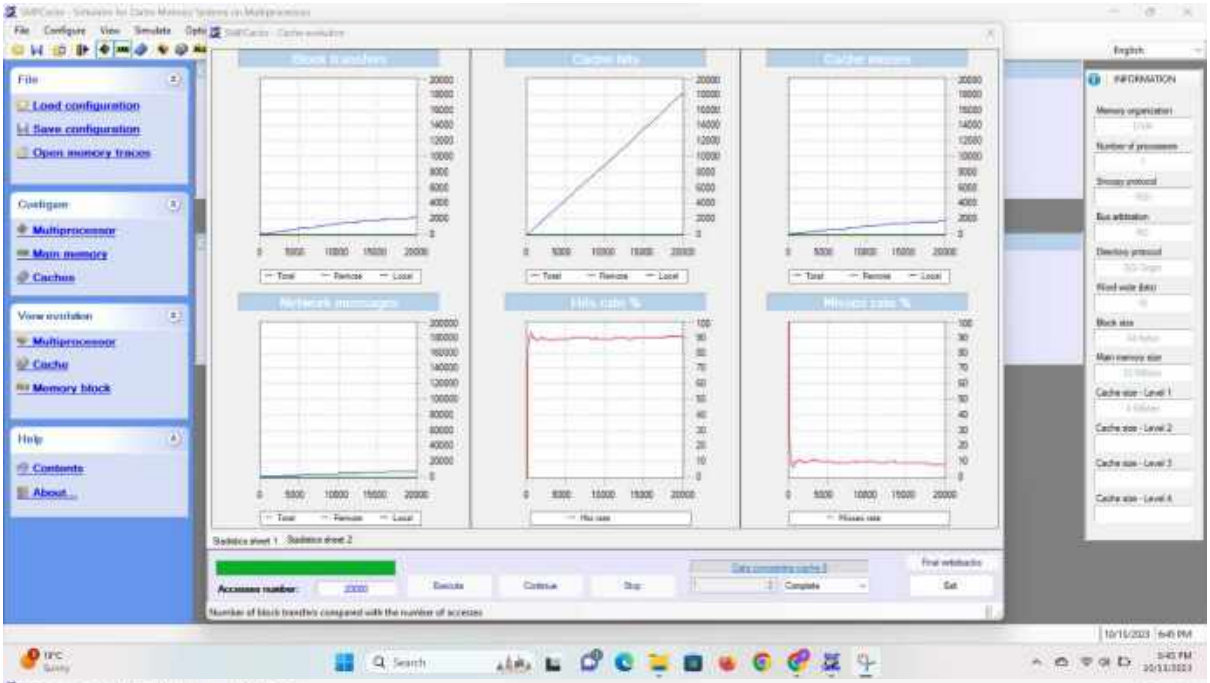
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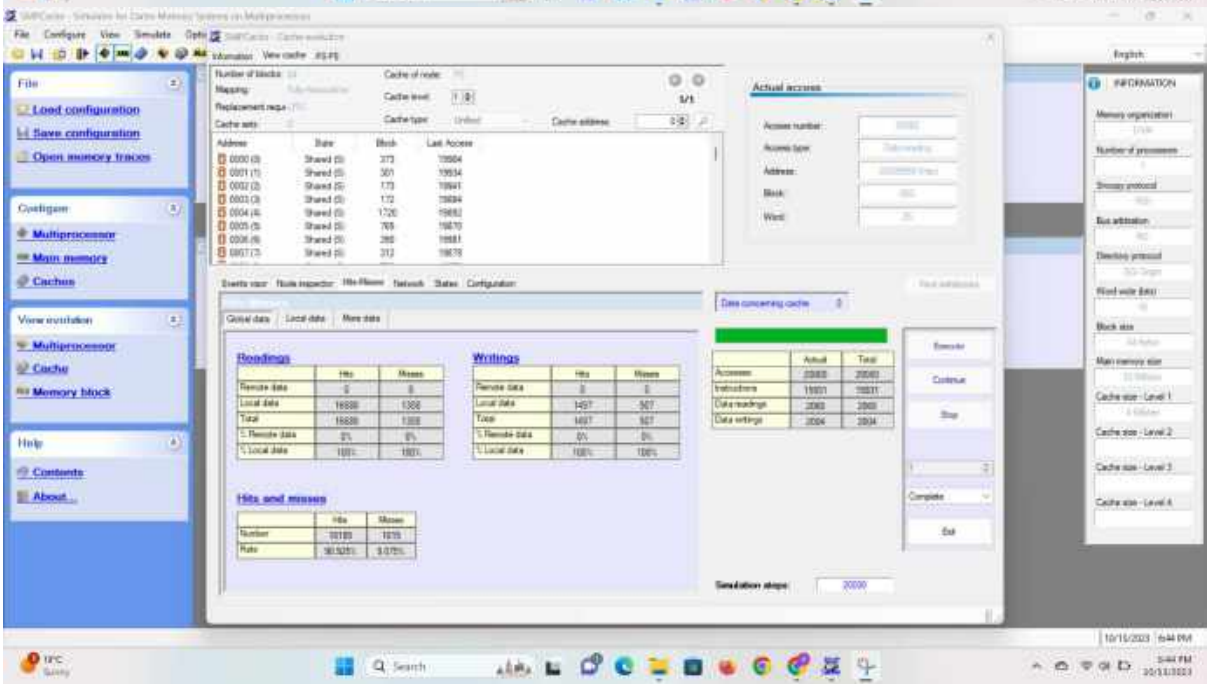
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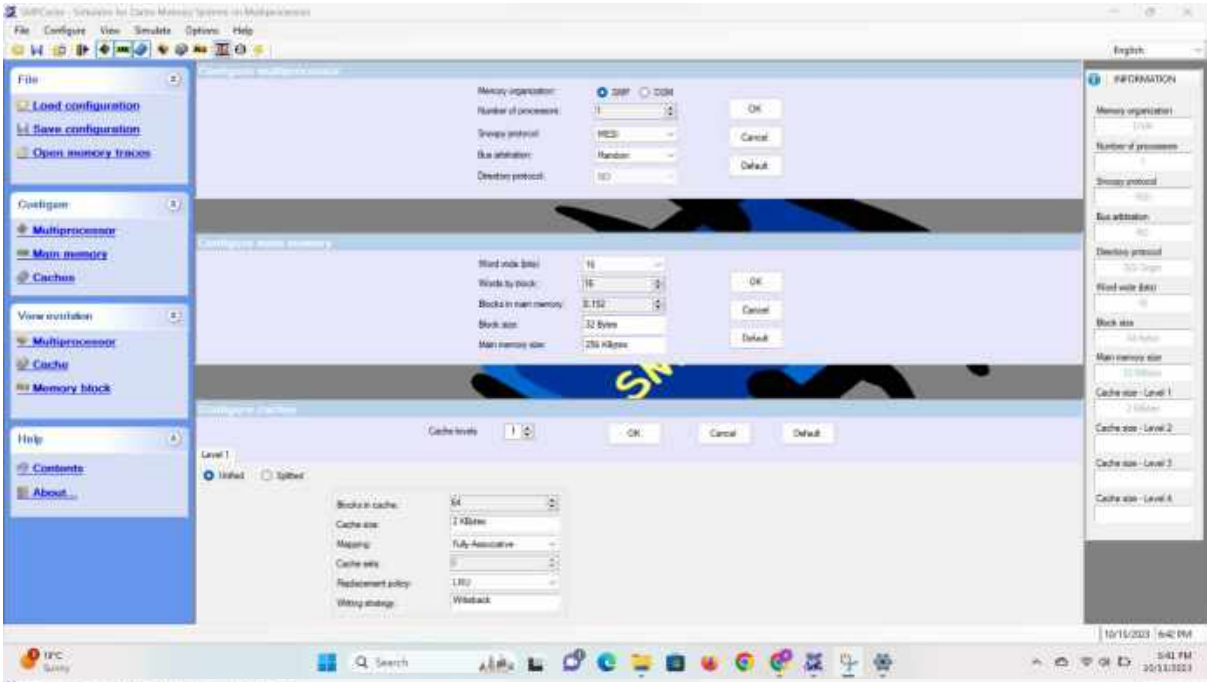
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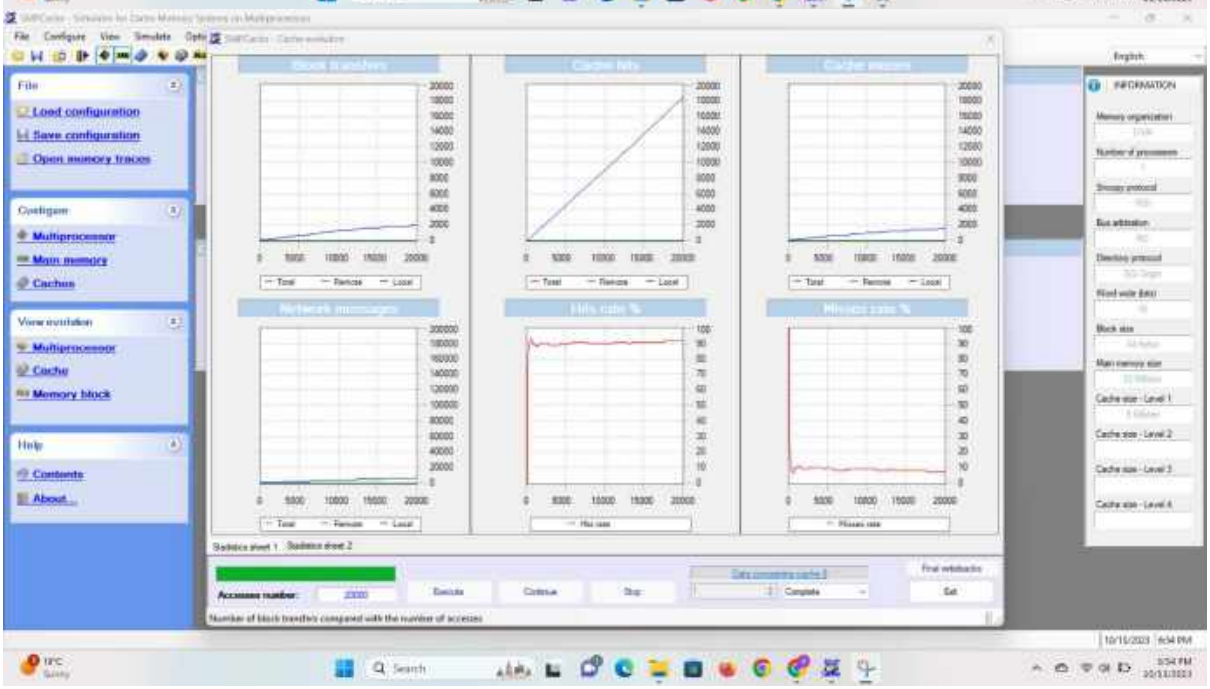
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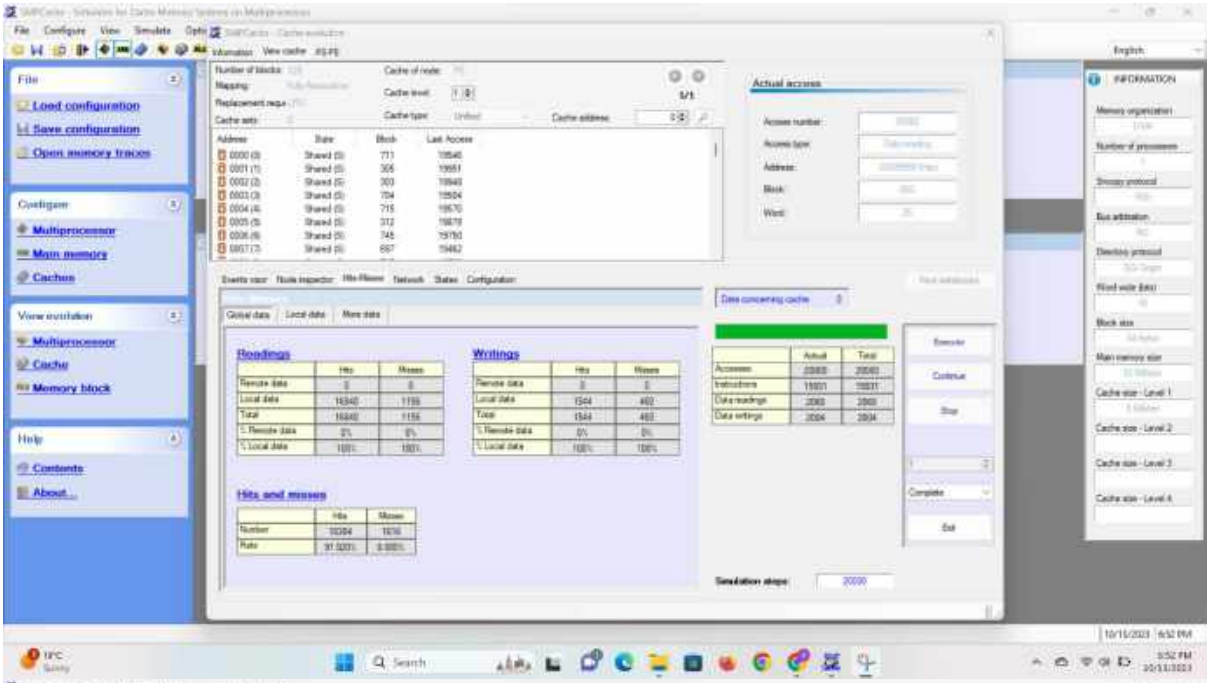
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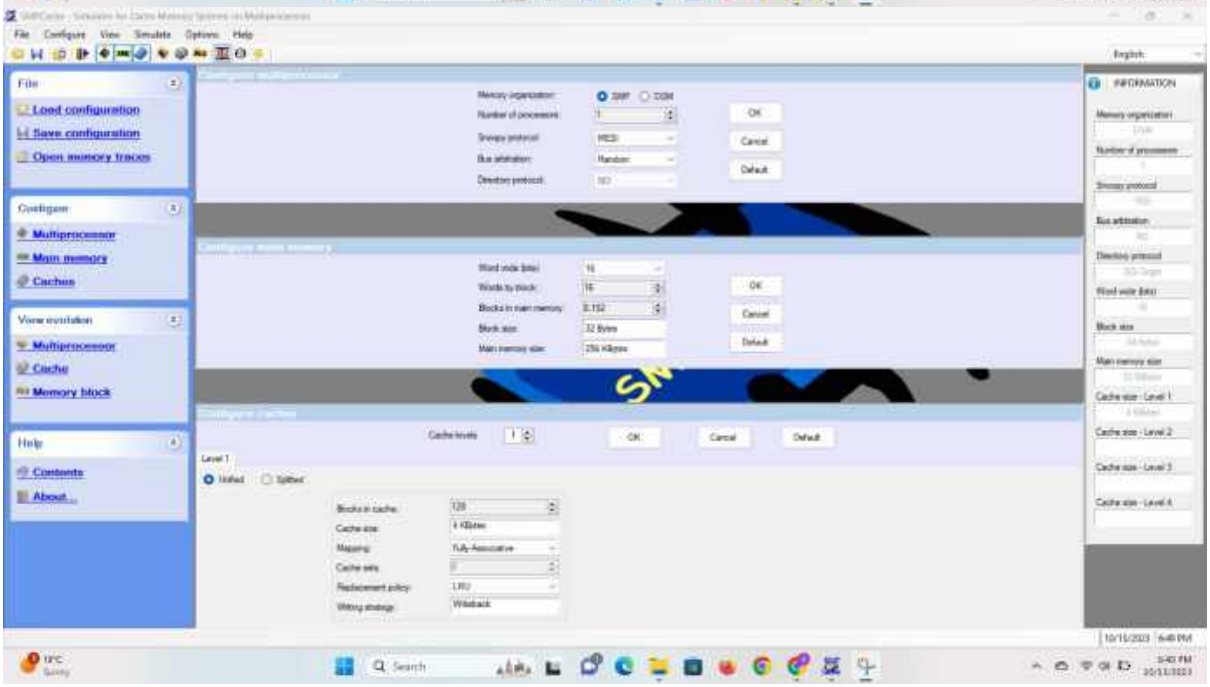
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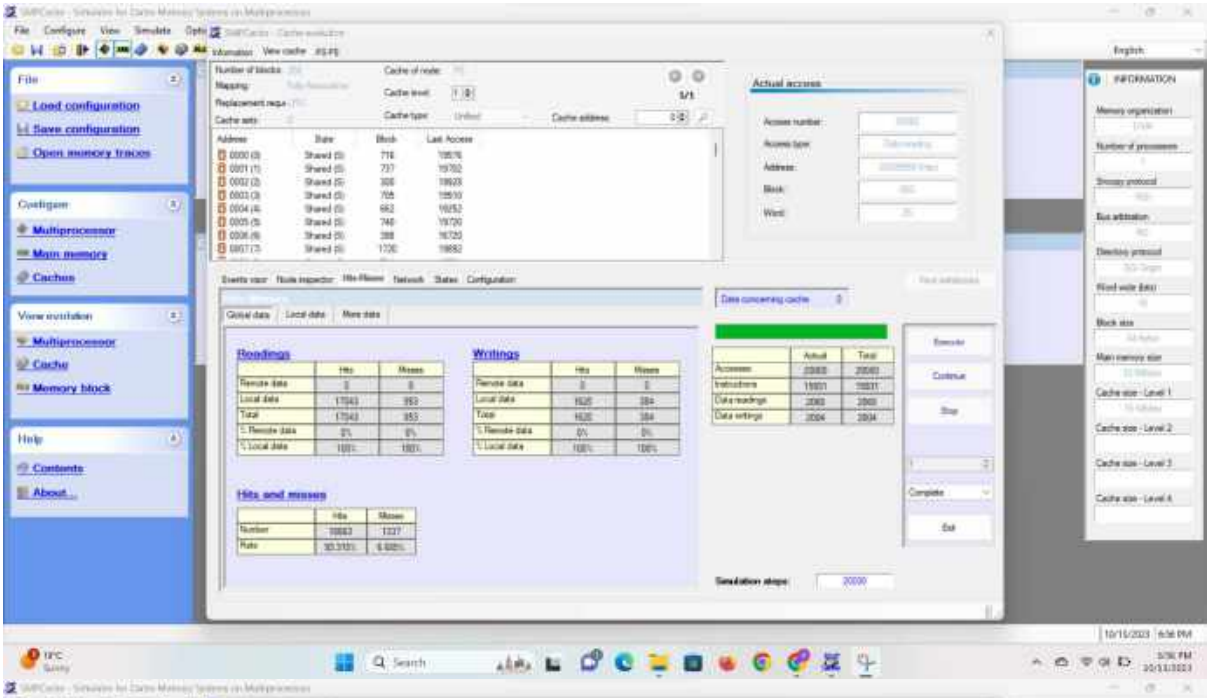
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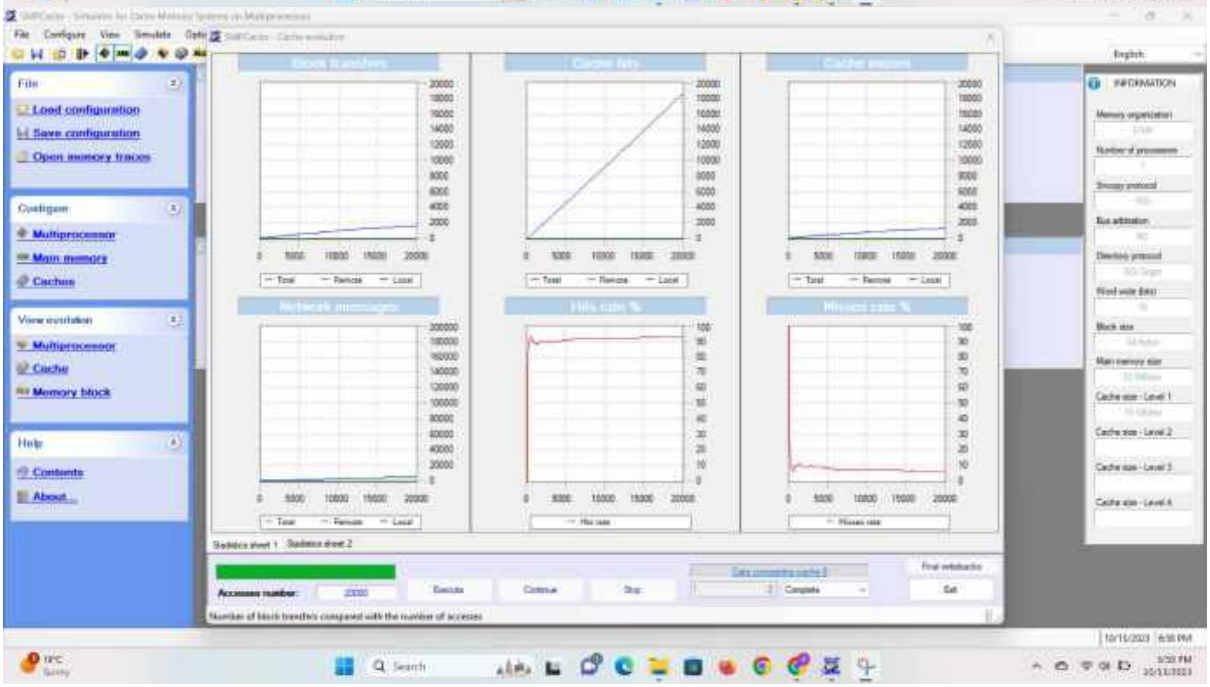
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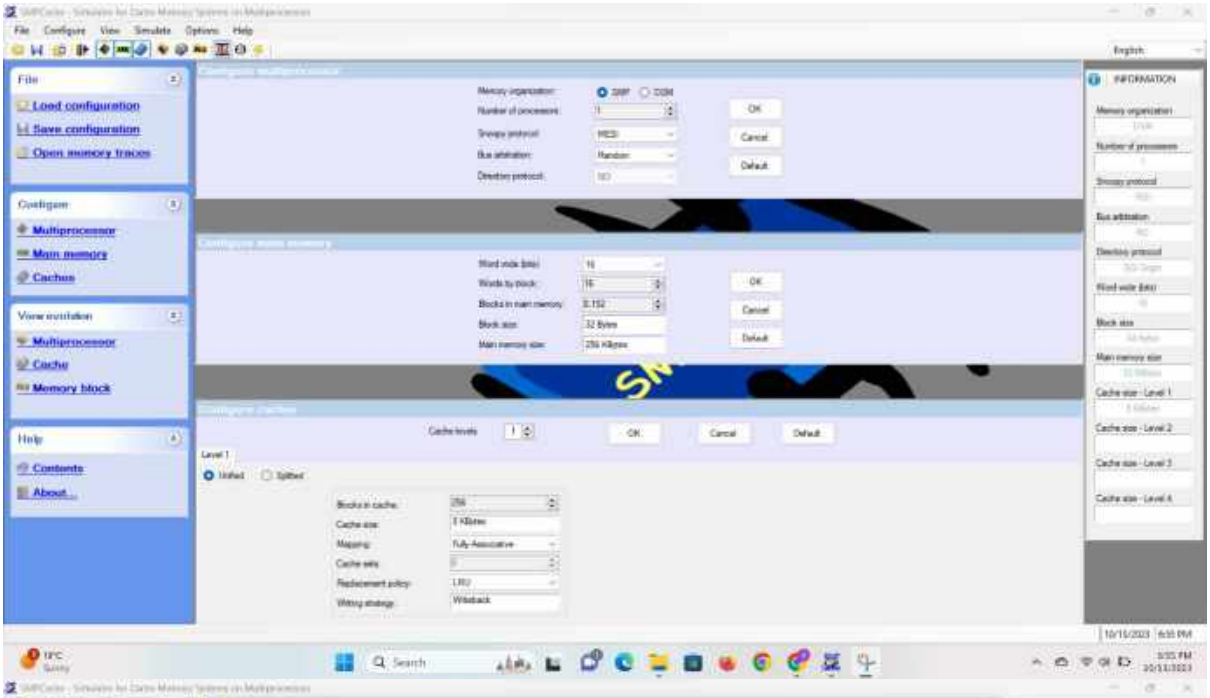
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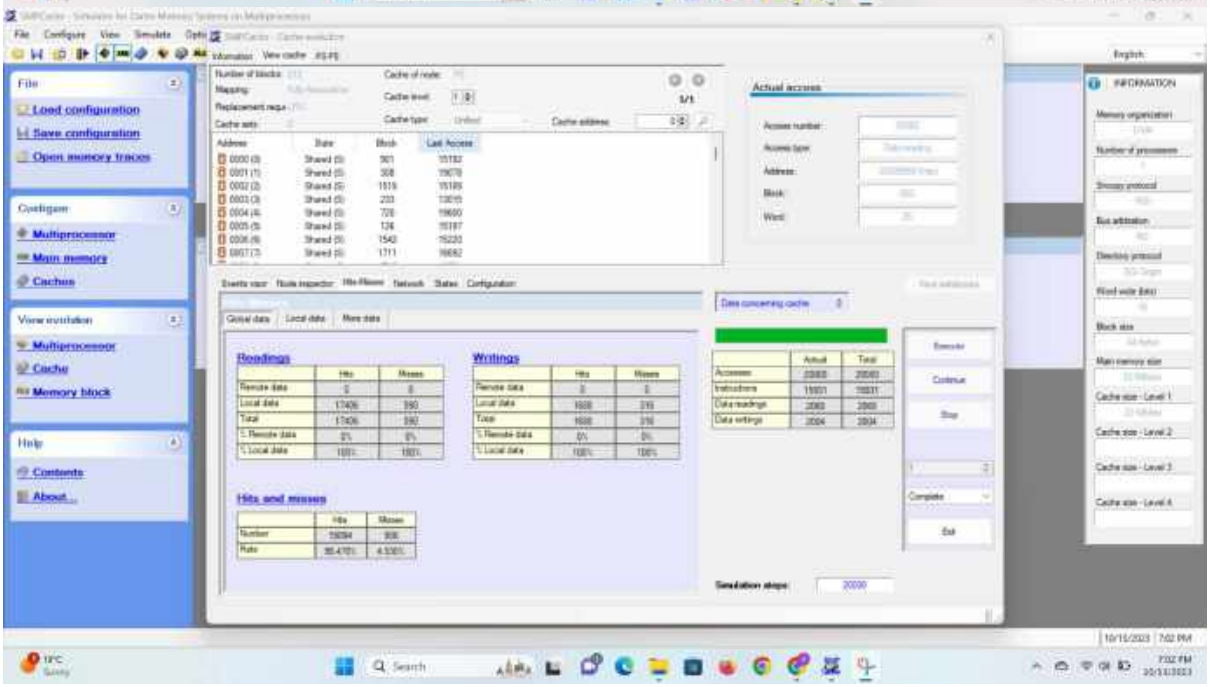
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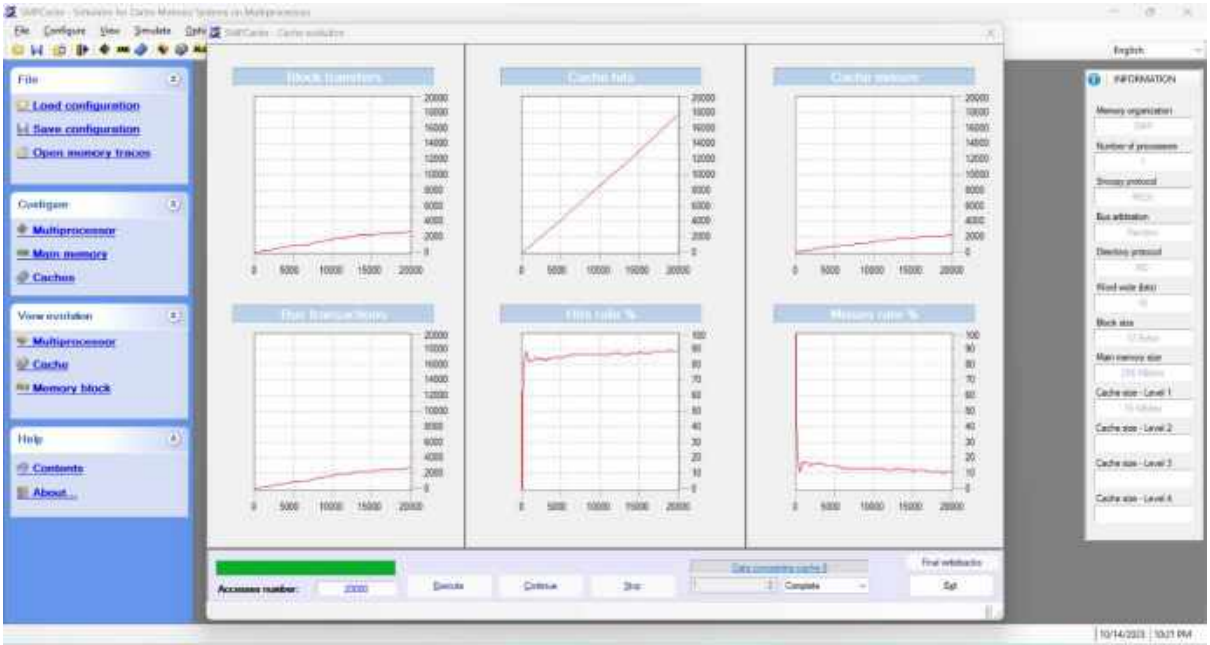
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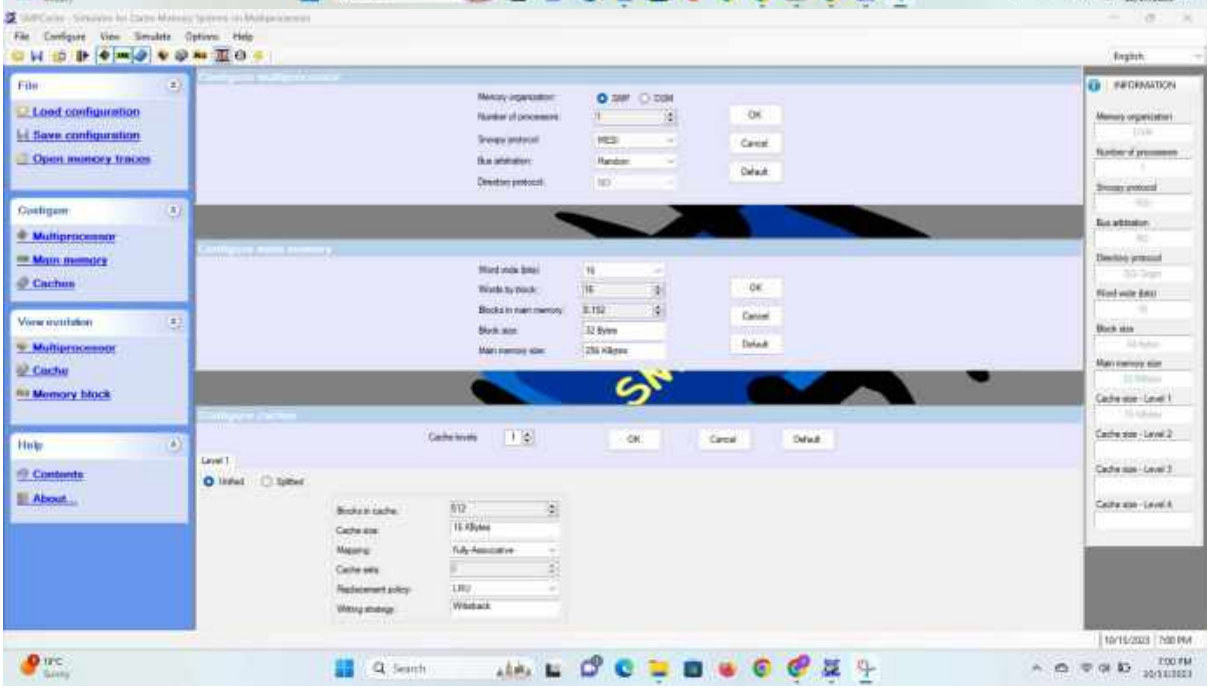
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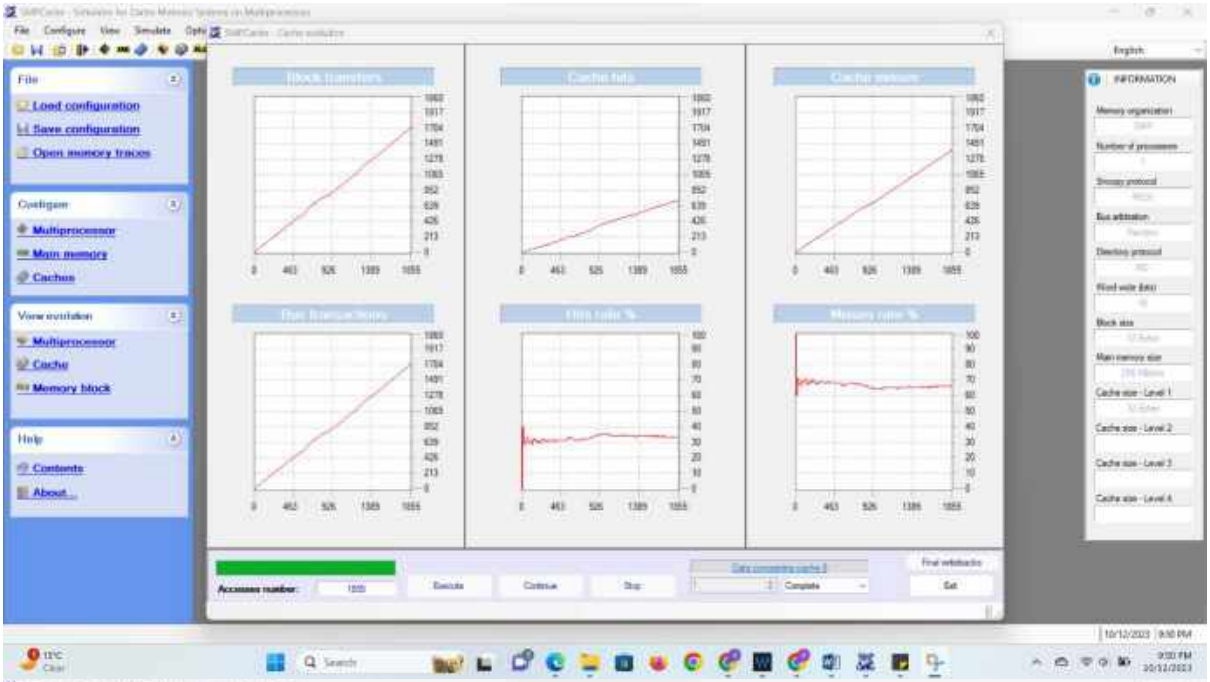
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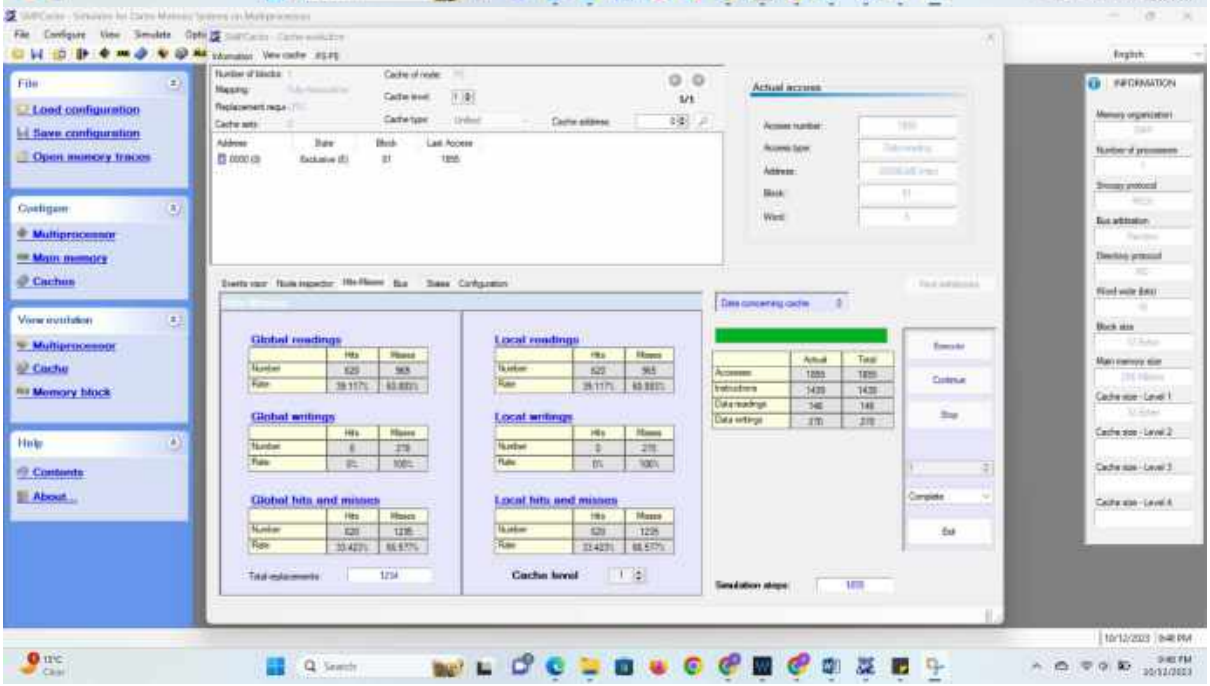
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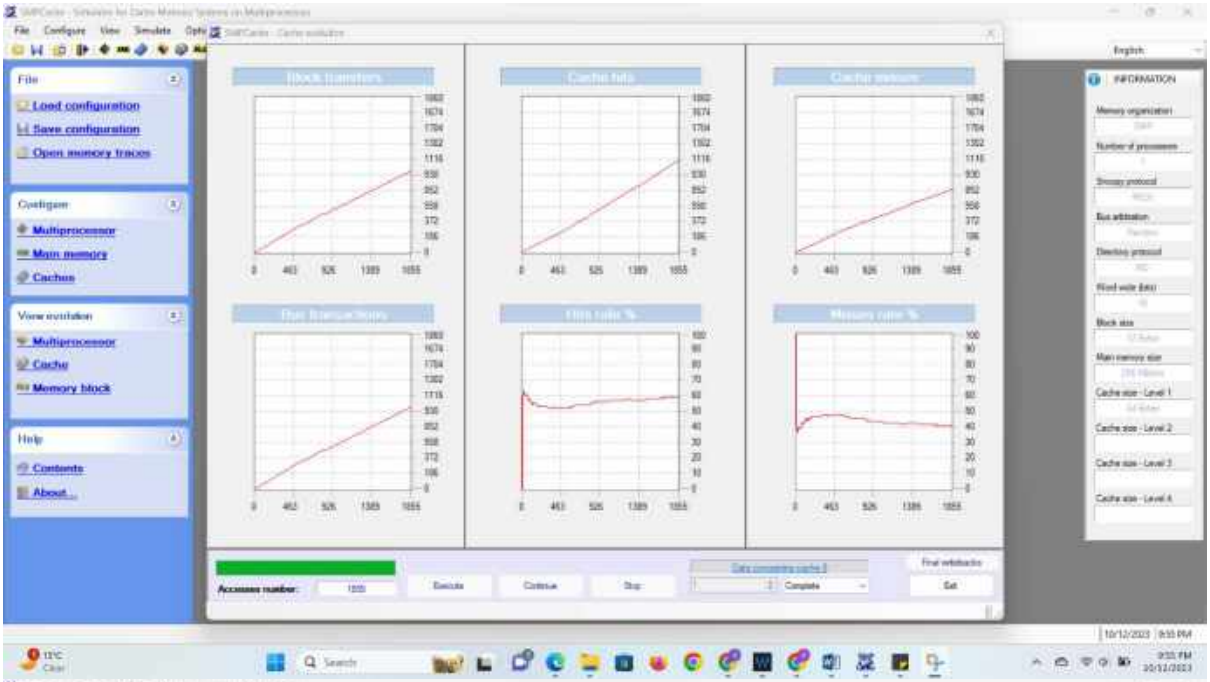
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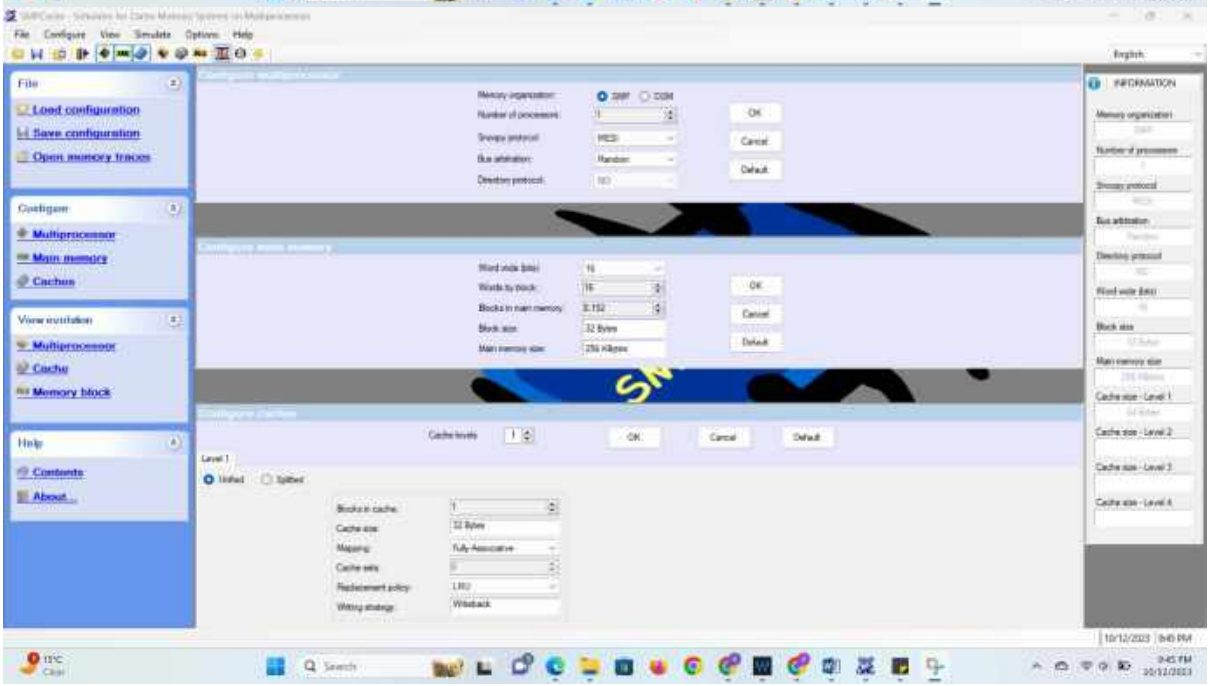
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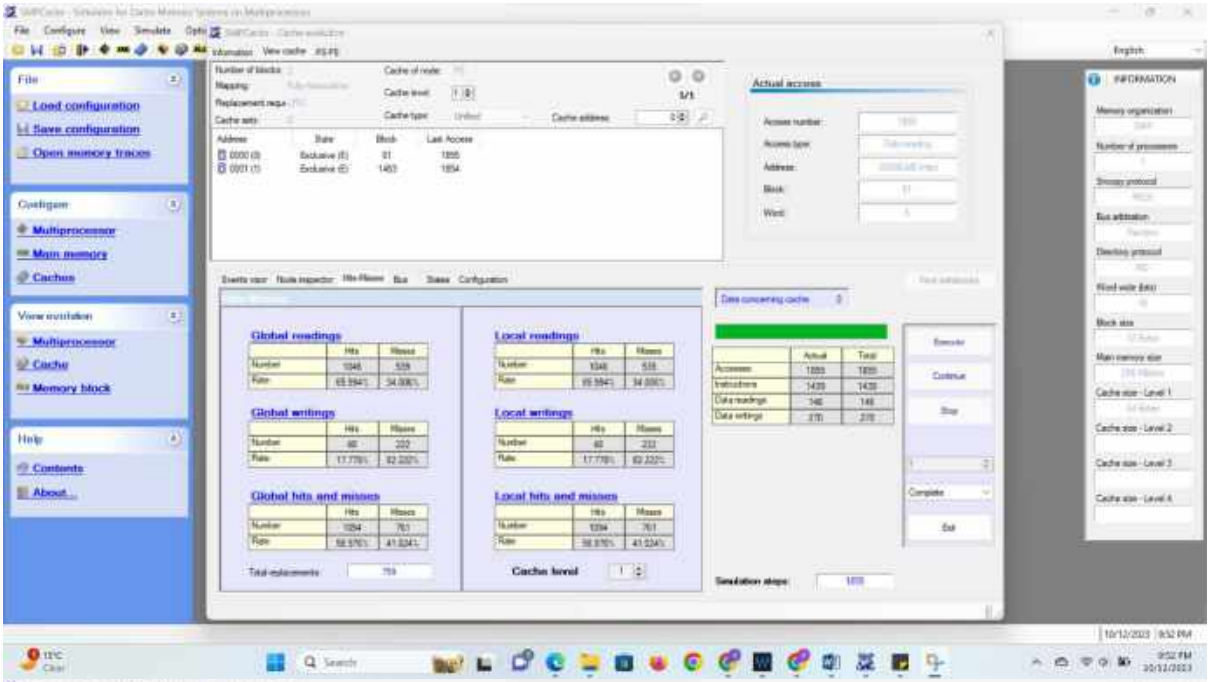
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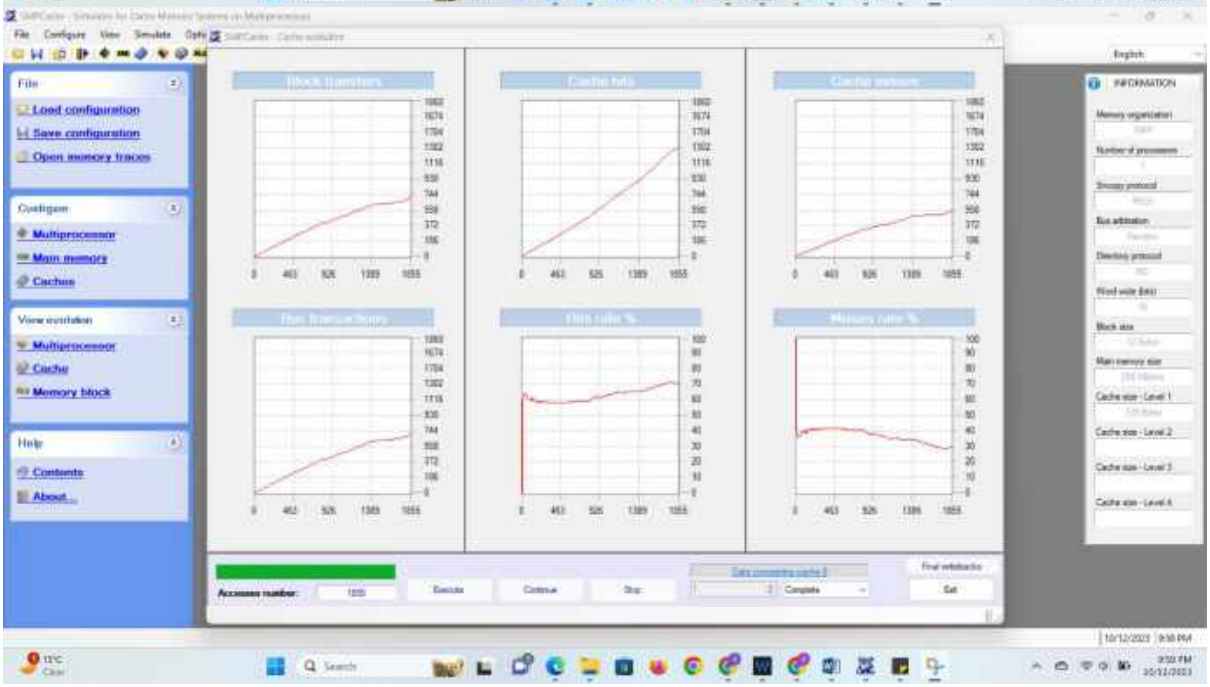
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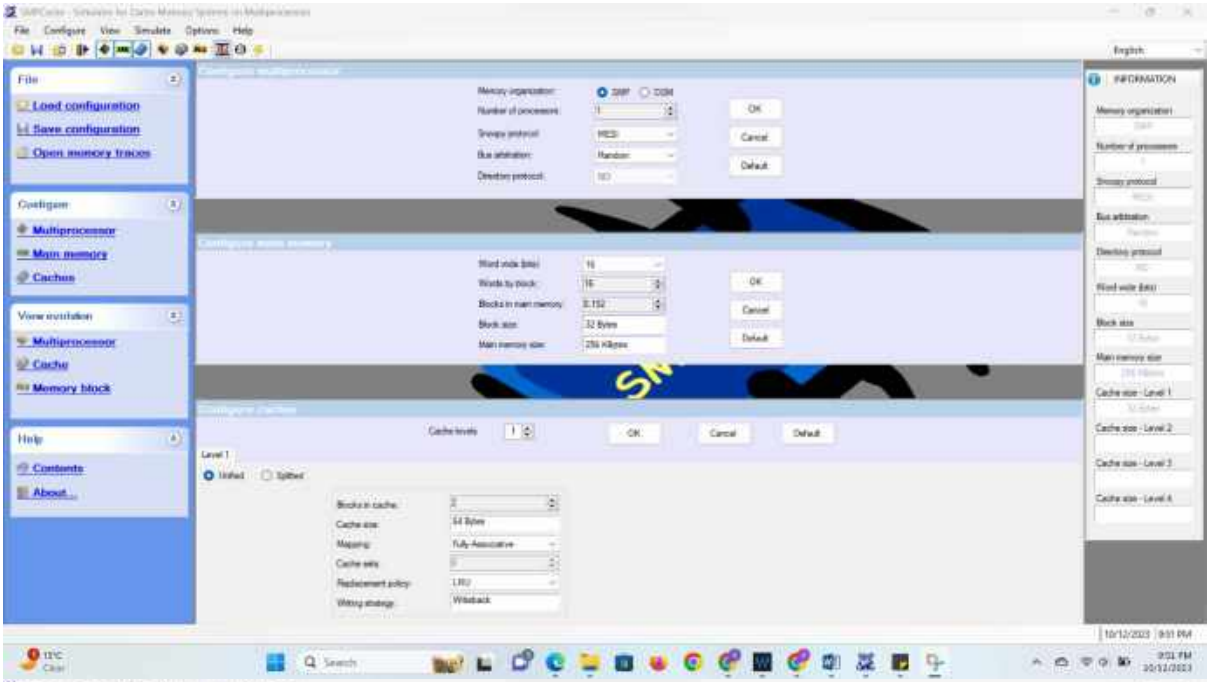
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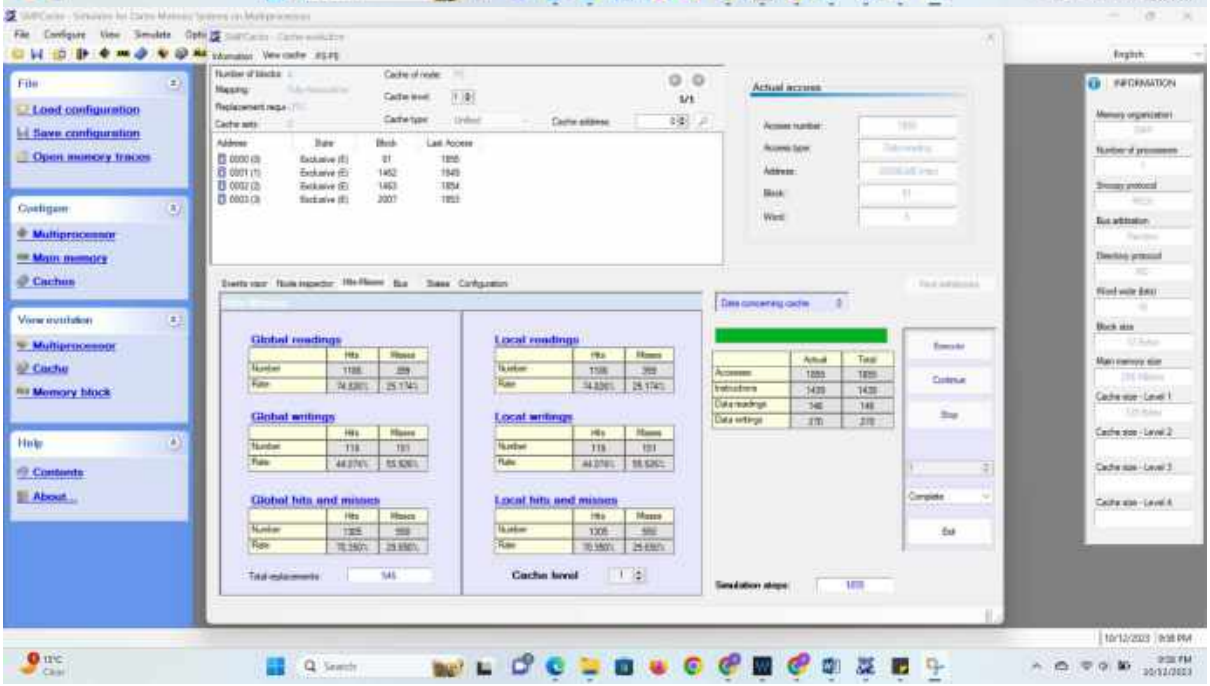
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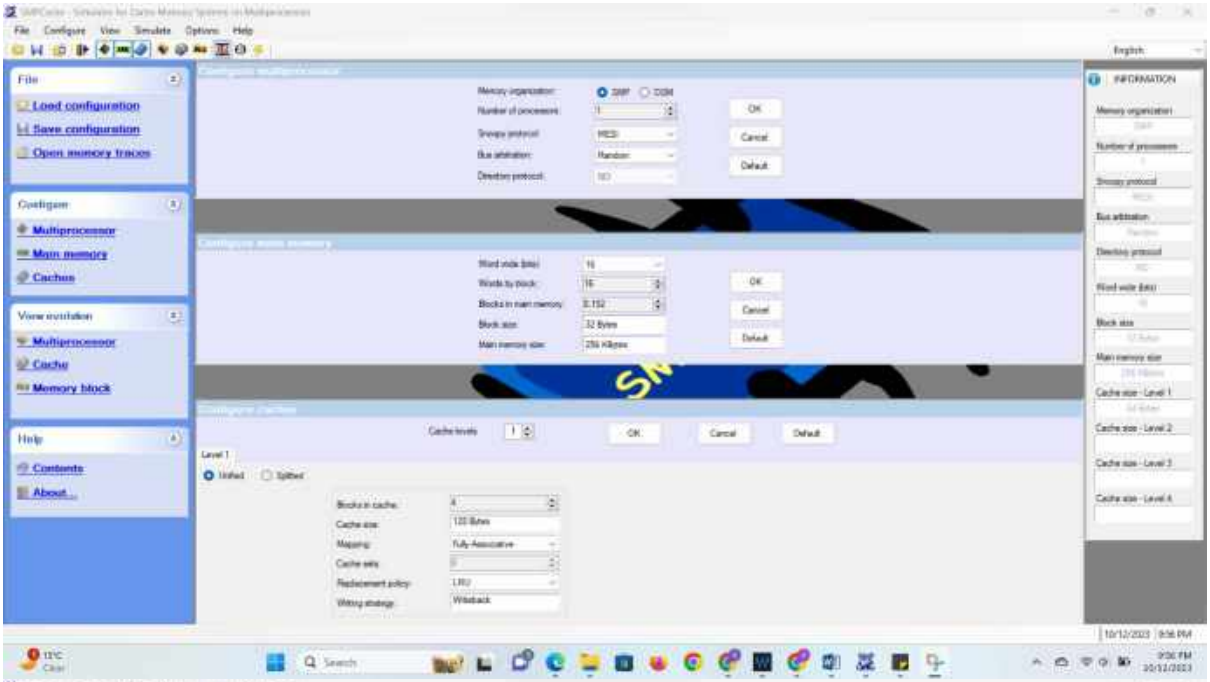
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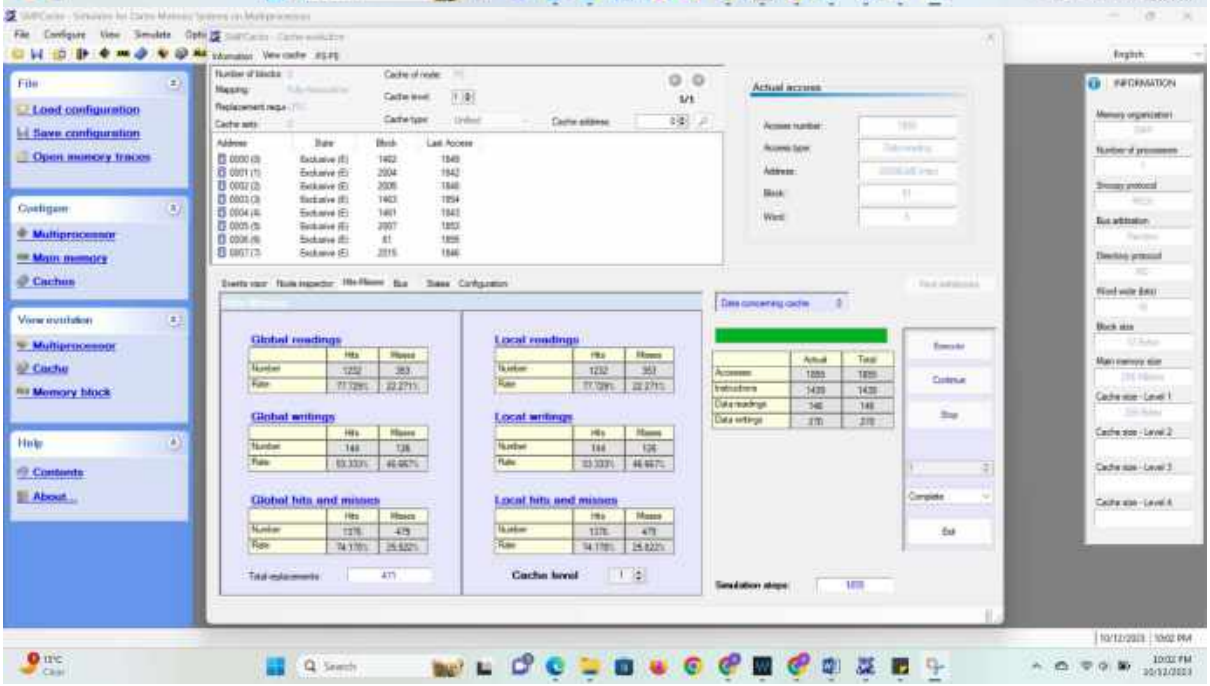
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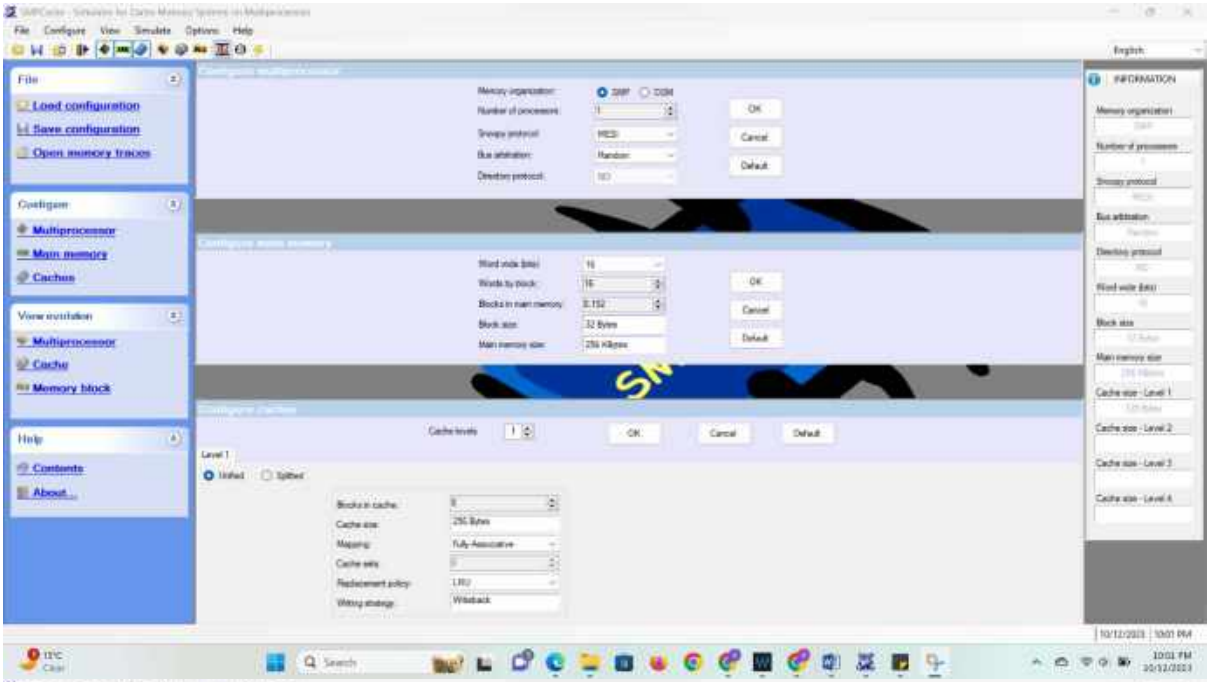
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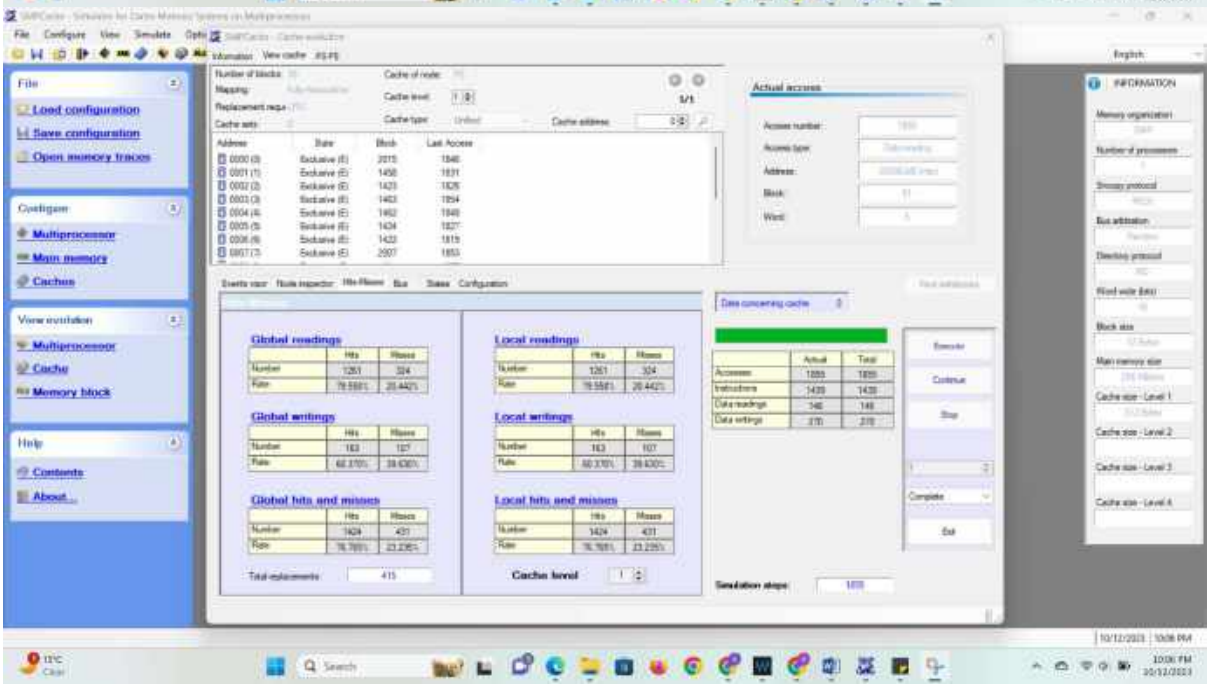
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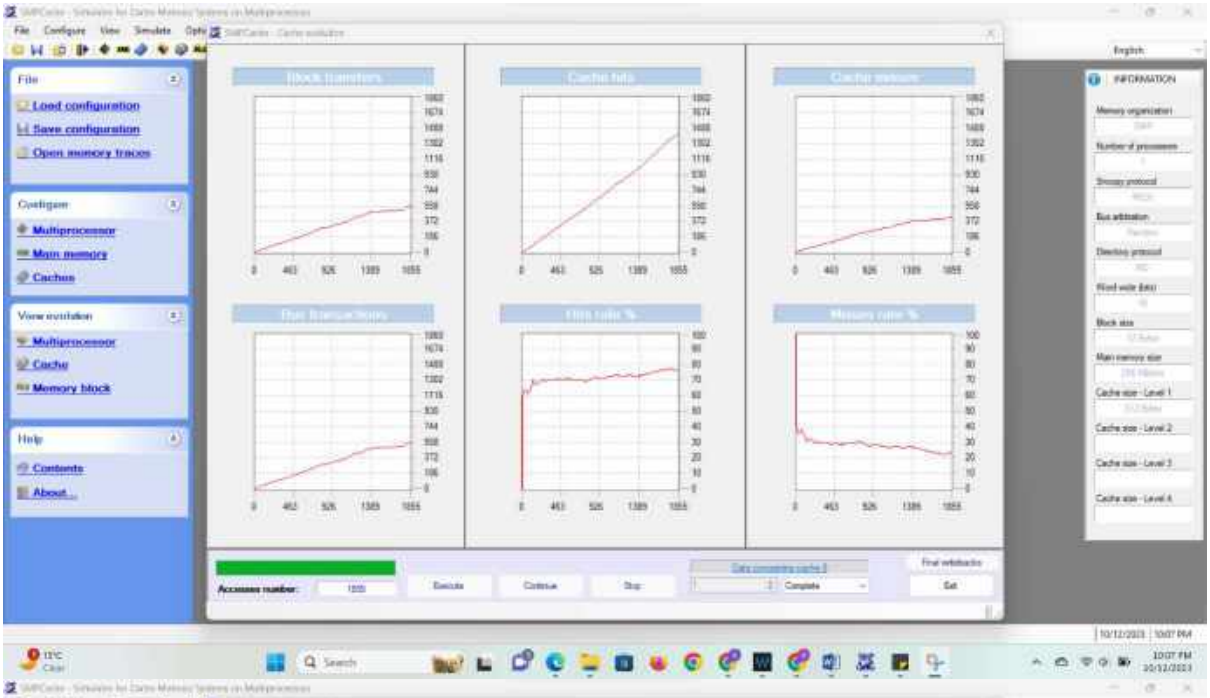
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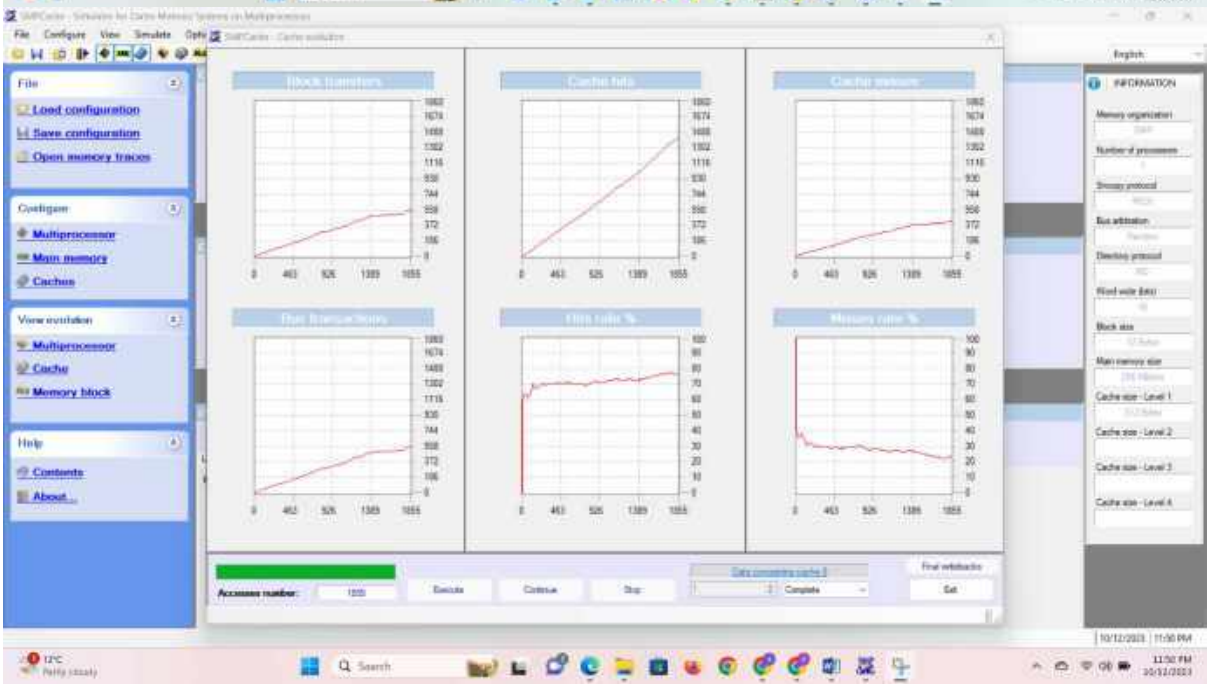
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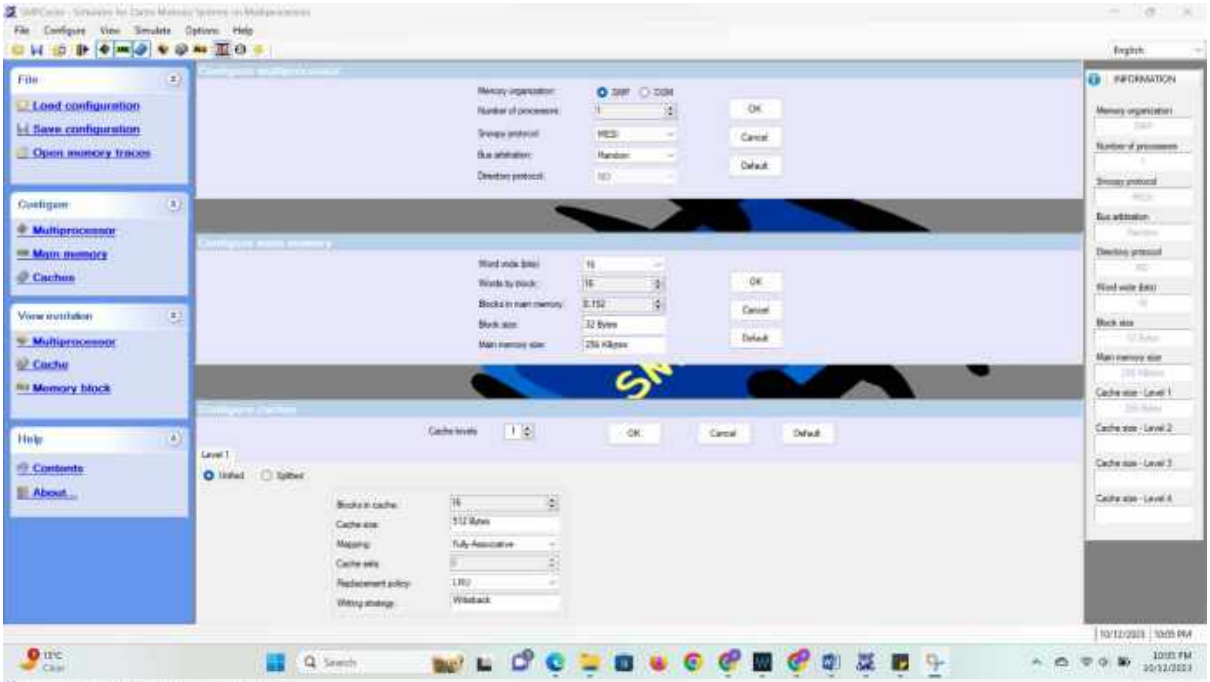
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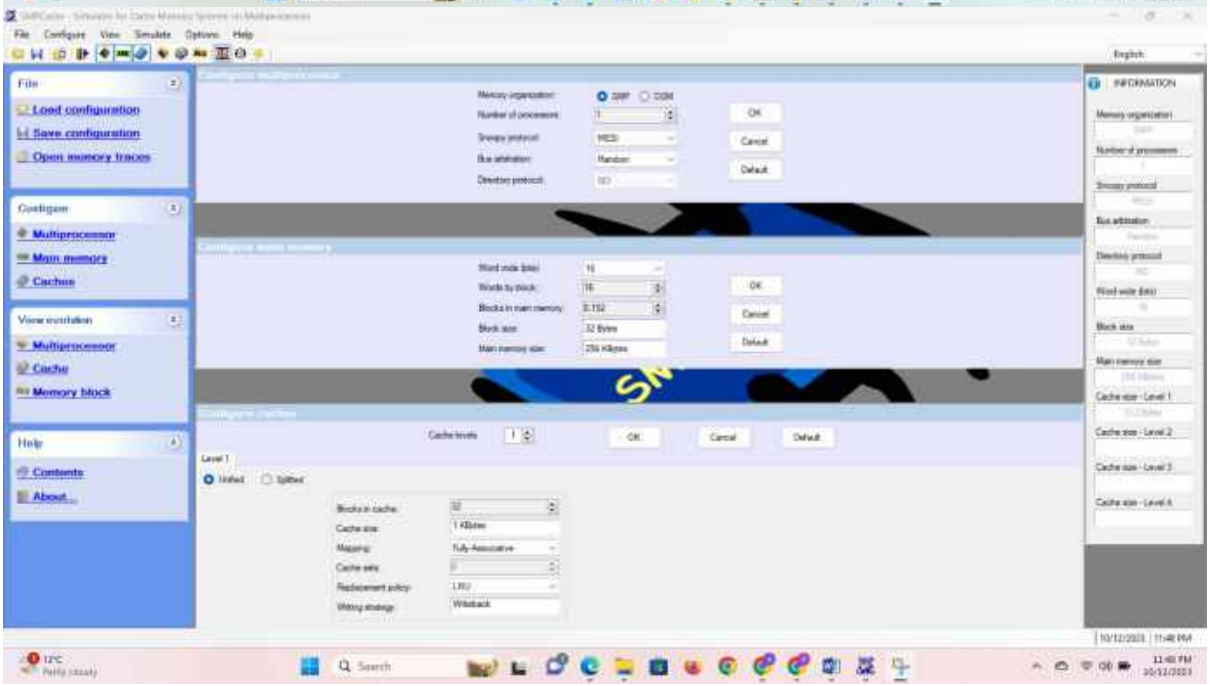
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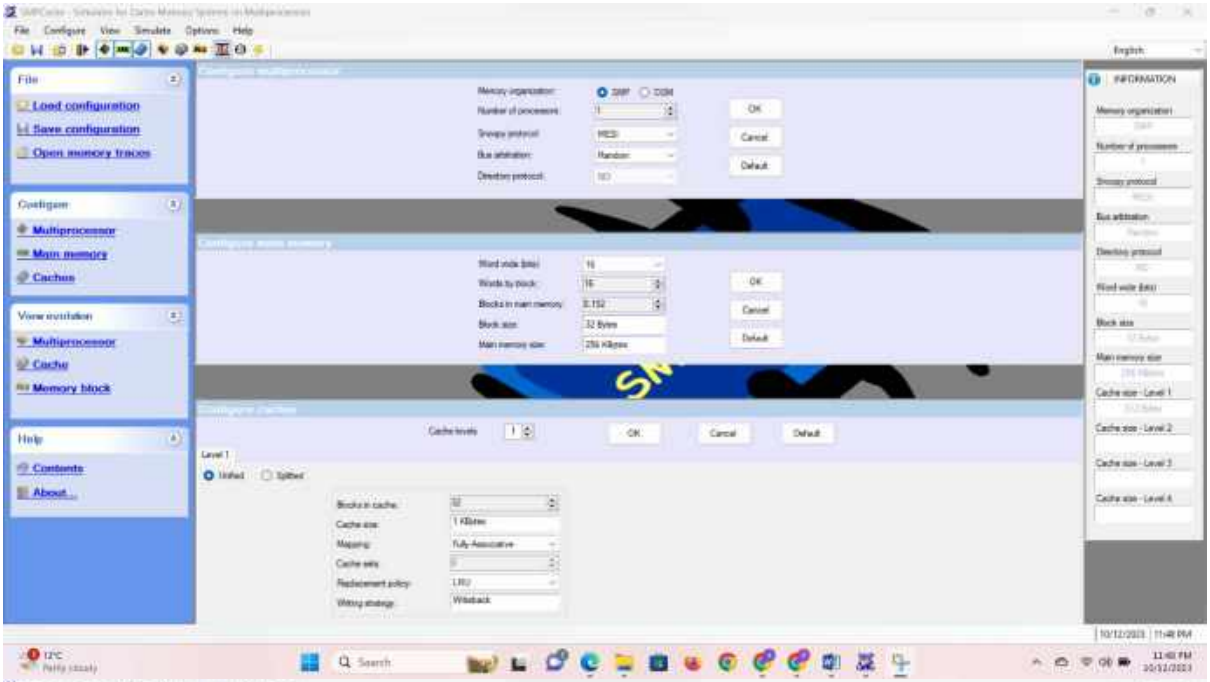
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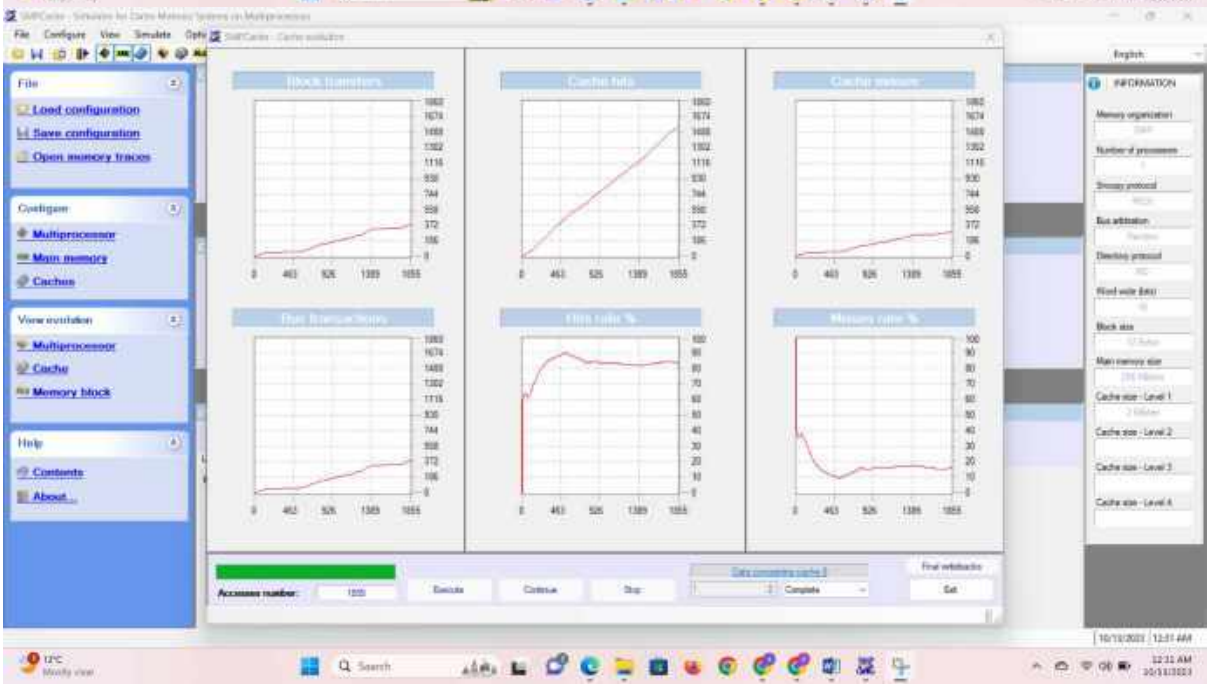
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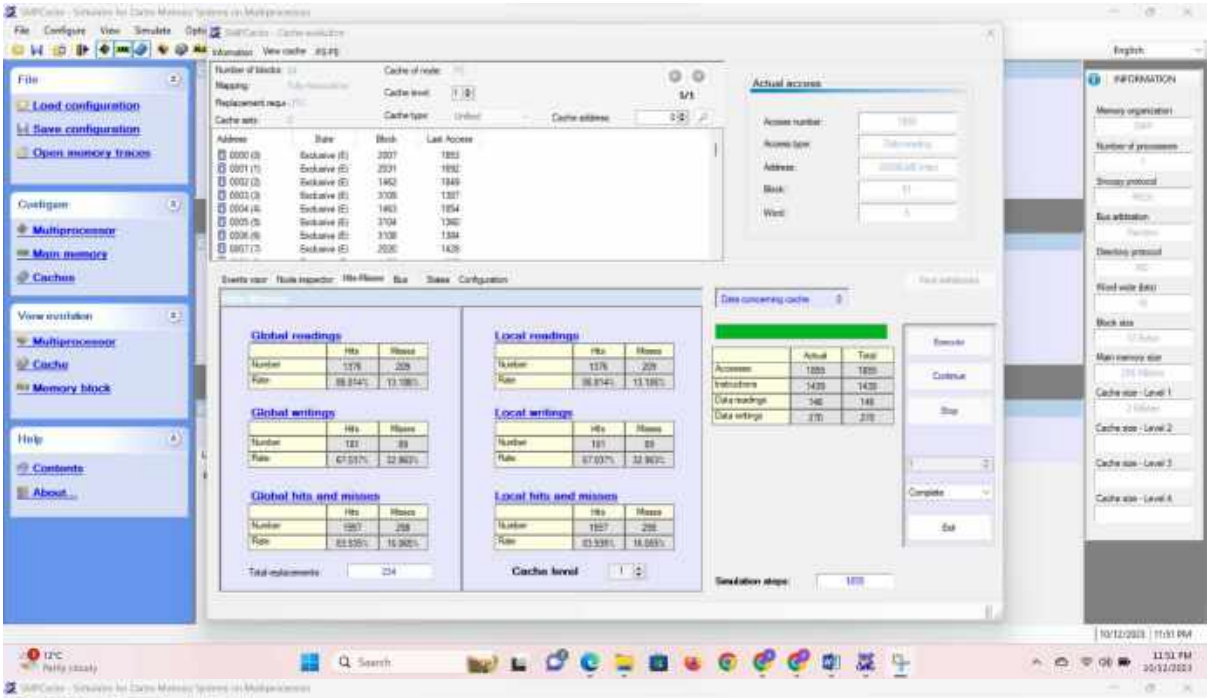
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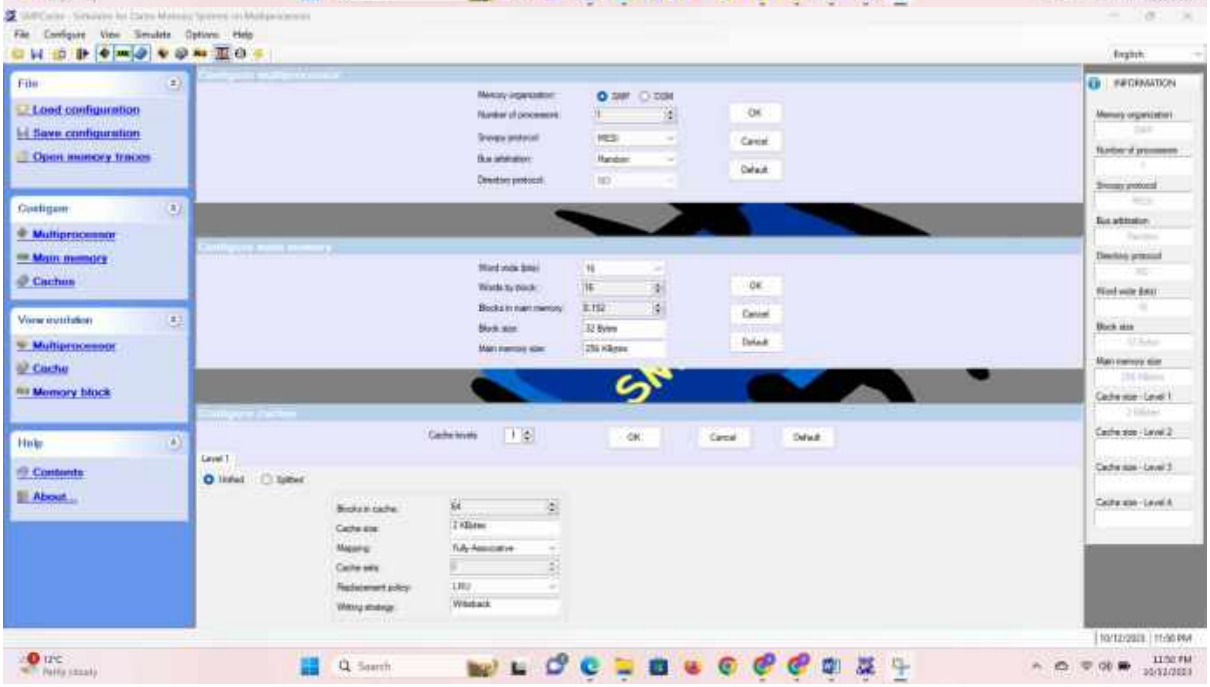
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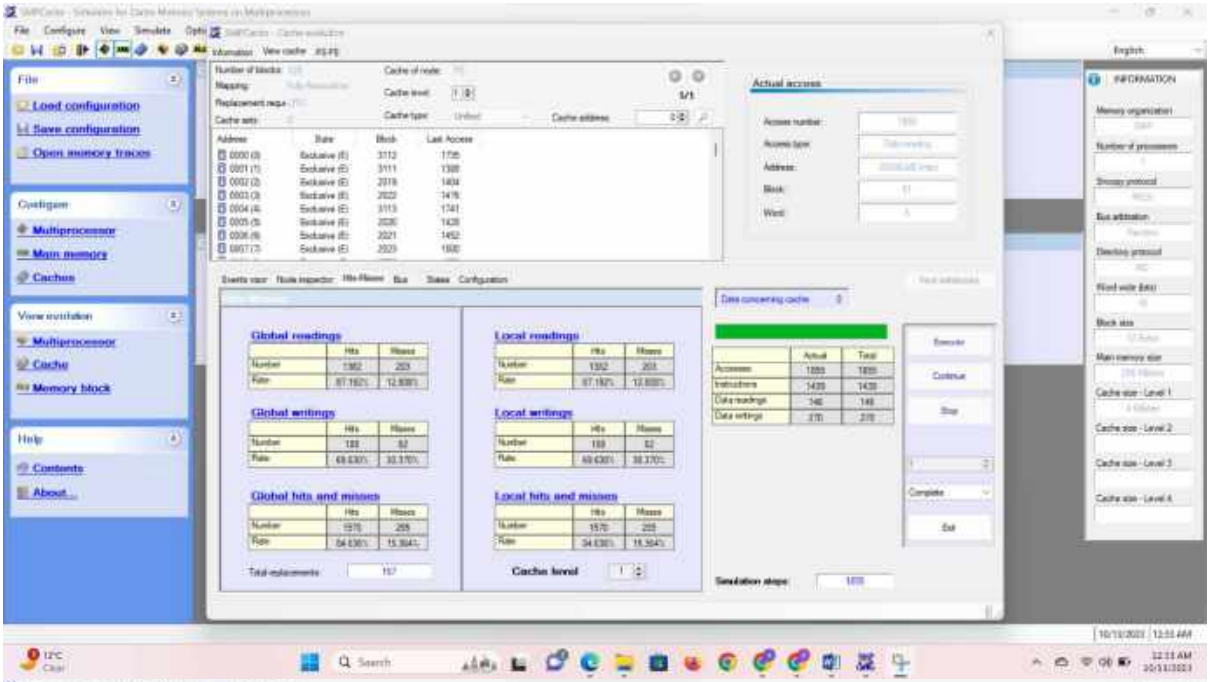
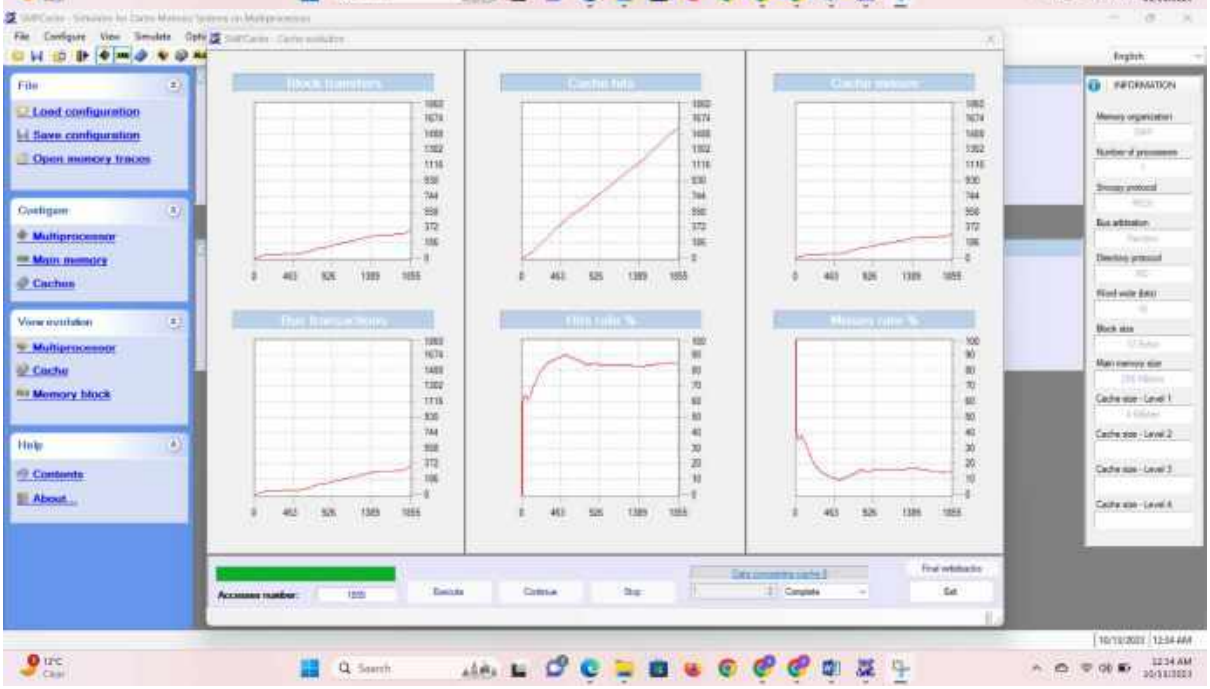
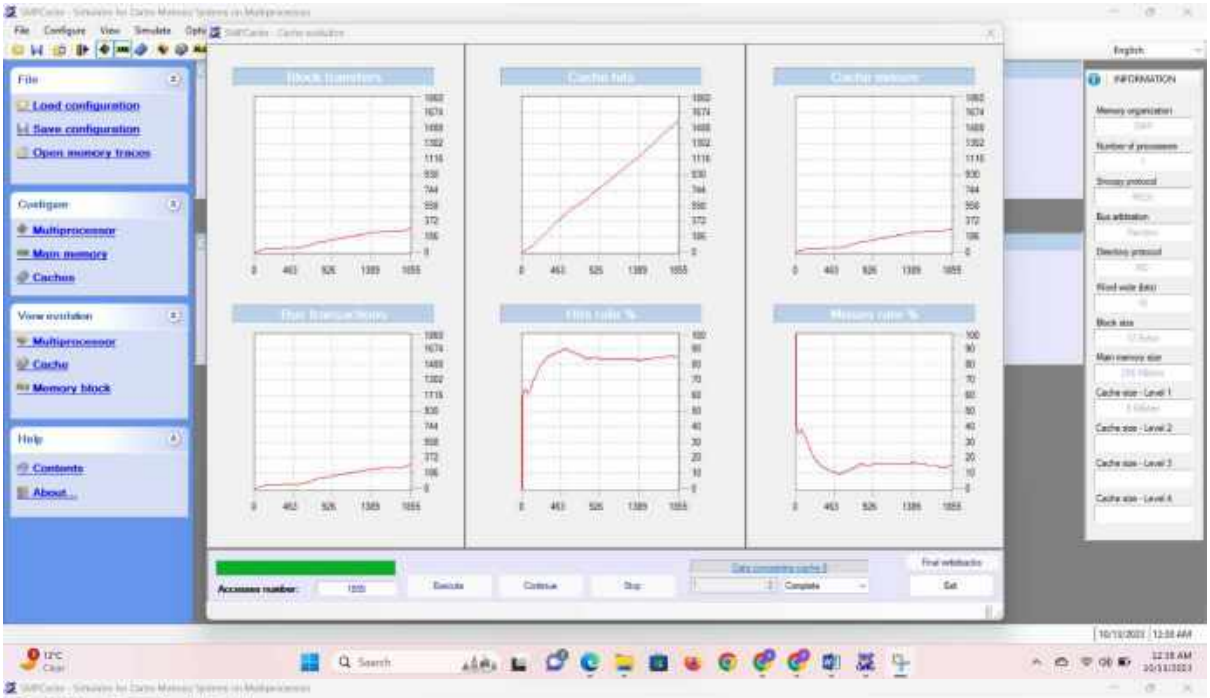
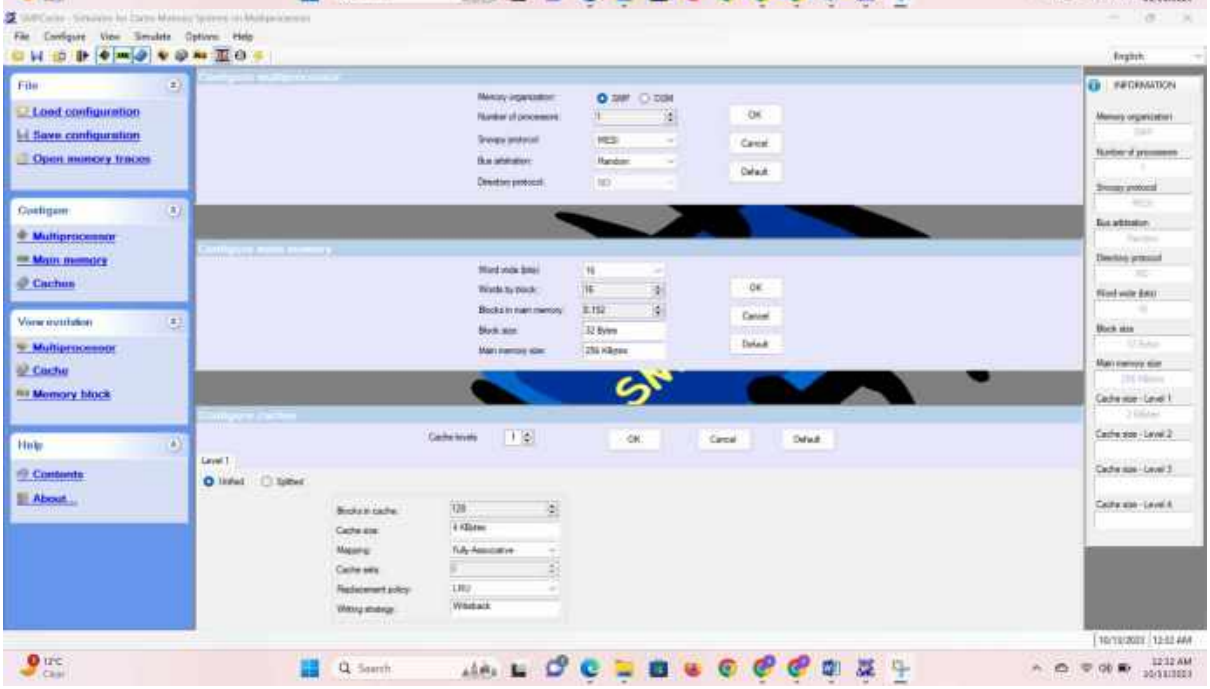
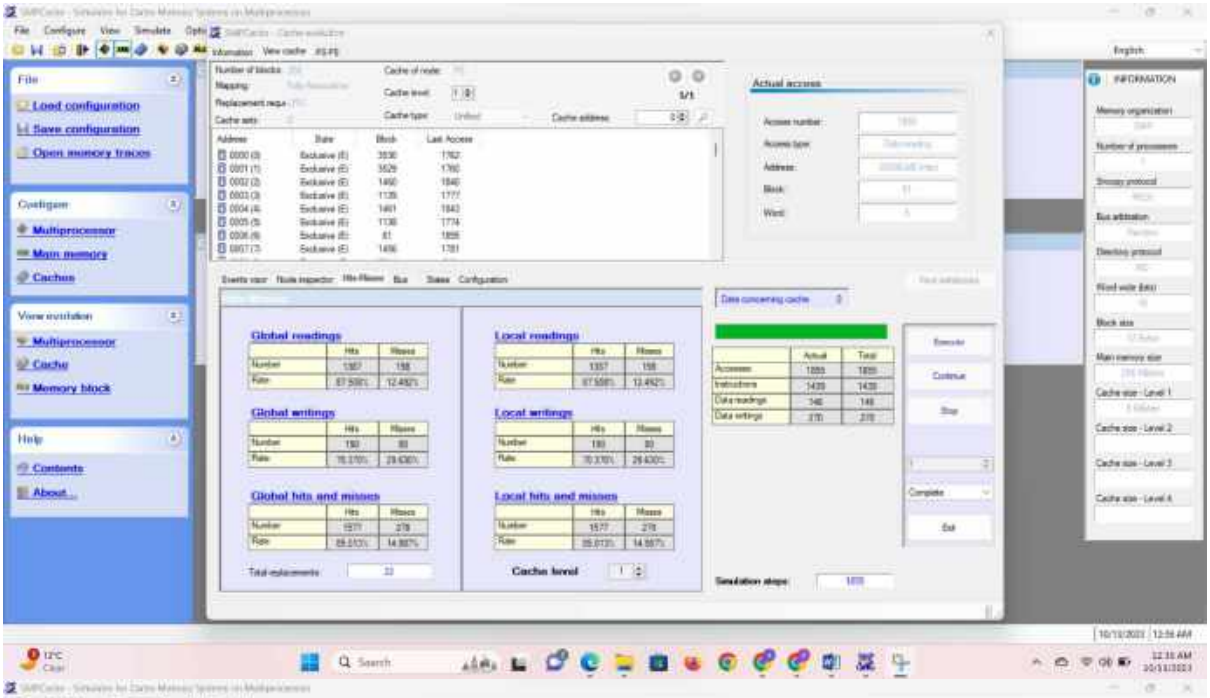
Default
INFORMATION

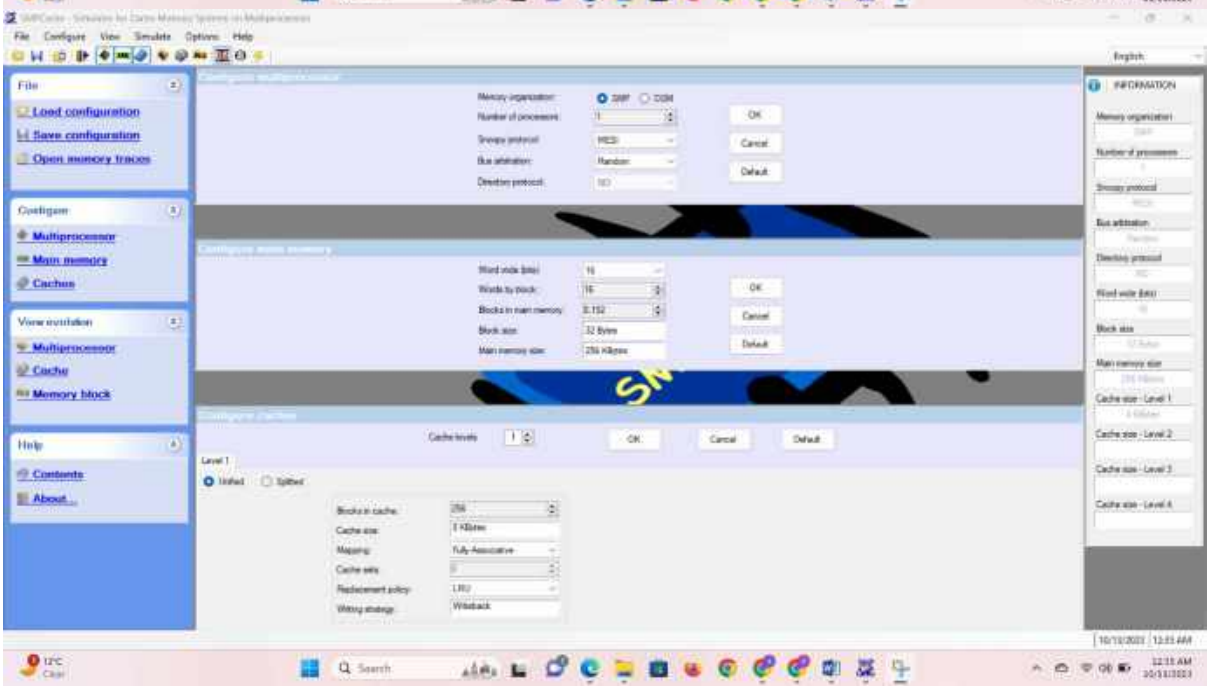

File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
INFORMATION

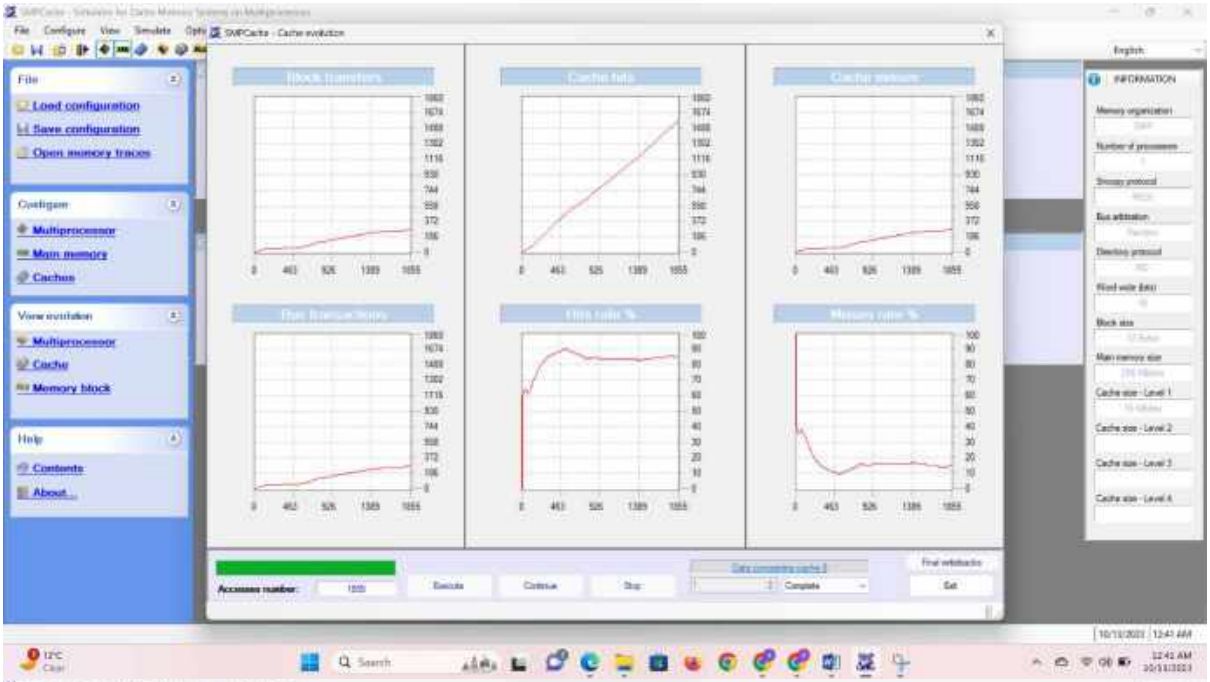

File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION

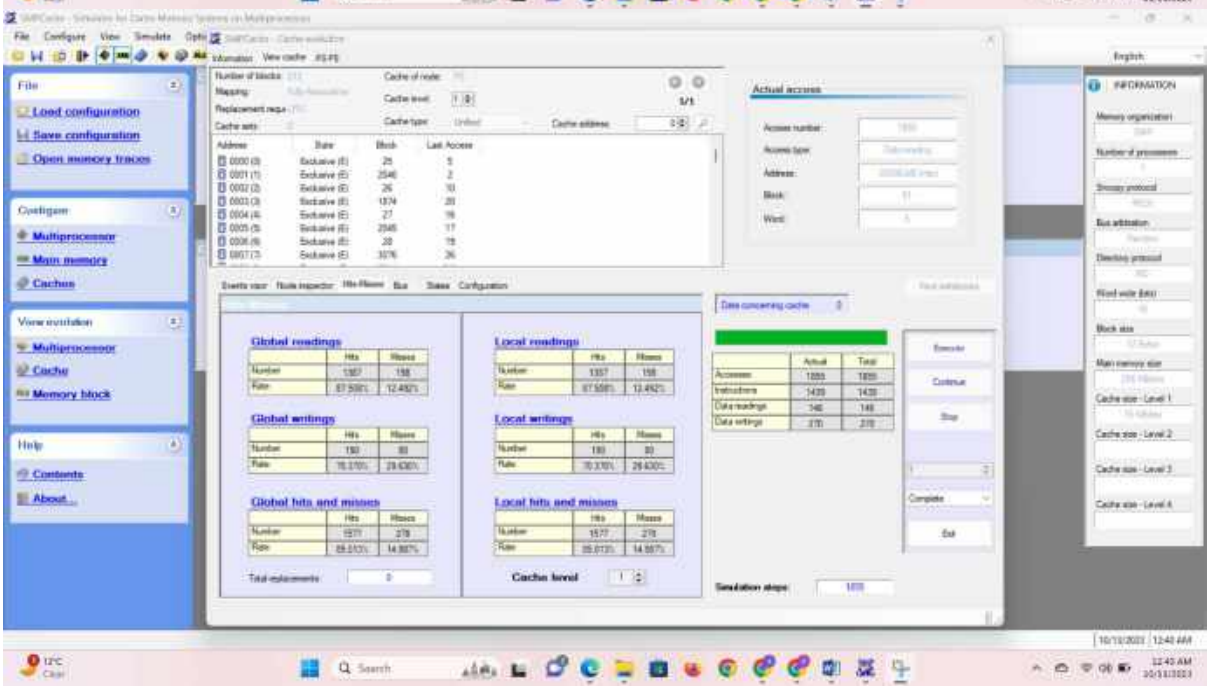

File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION

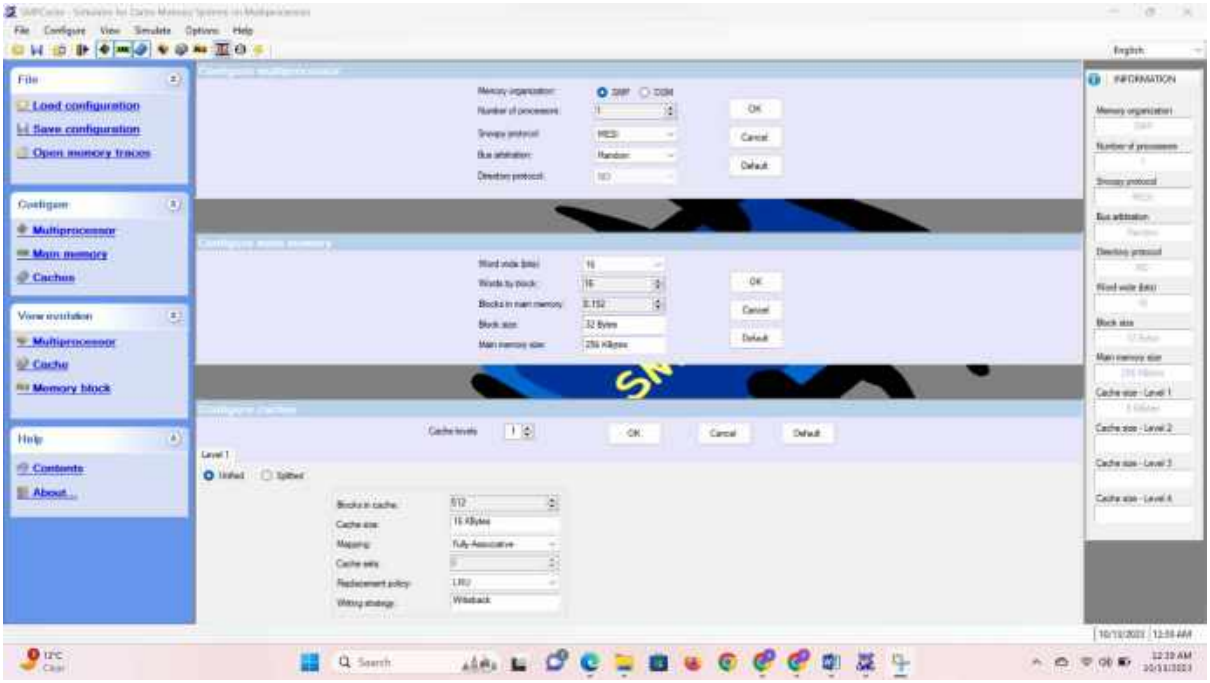

File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
Default
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level



Task 3

Influence of the Block Size

Purpose

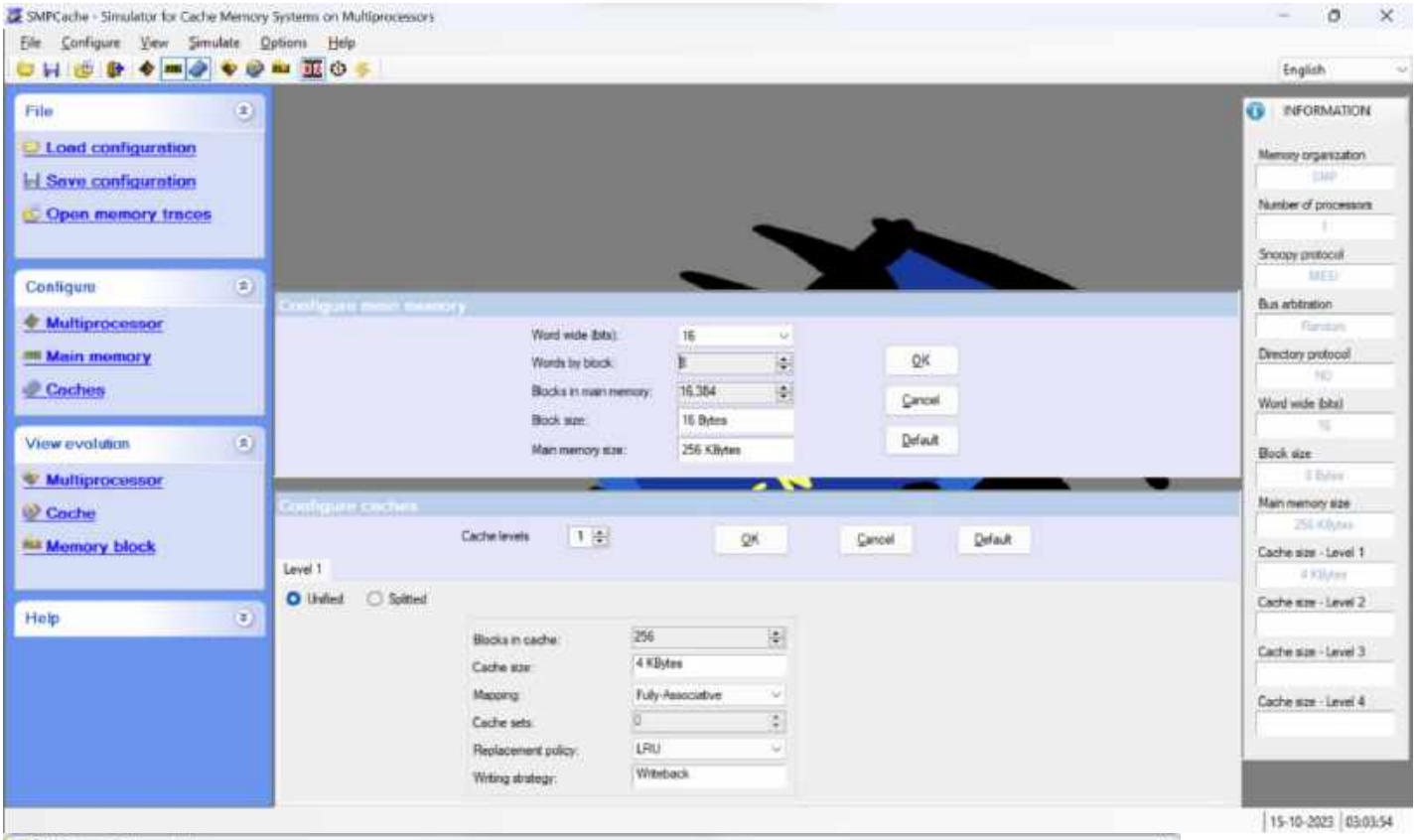
Study the influence of the block size on the miss rate.

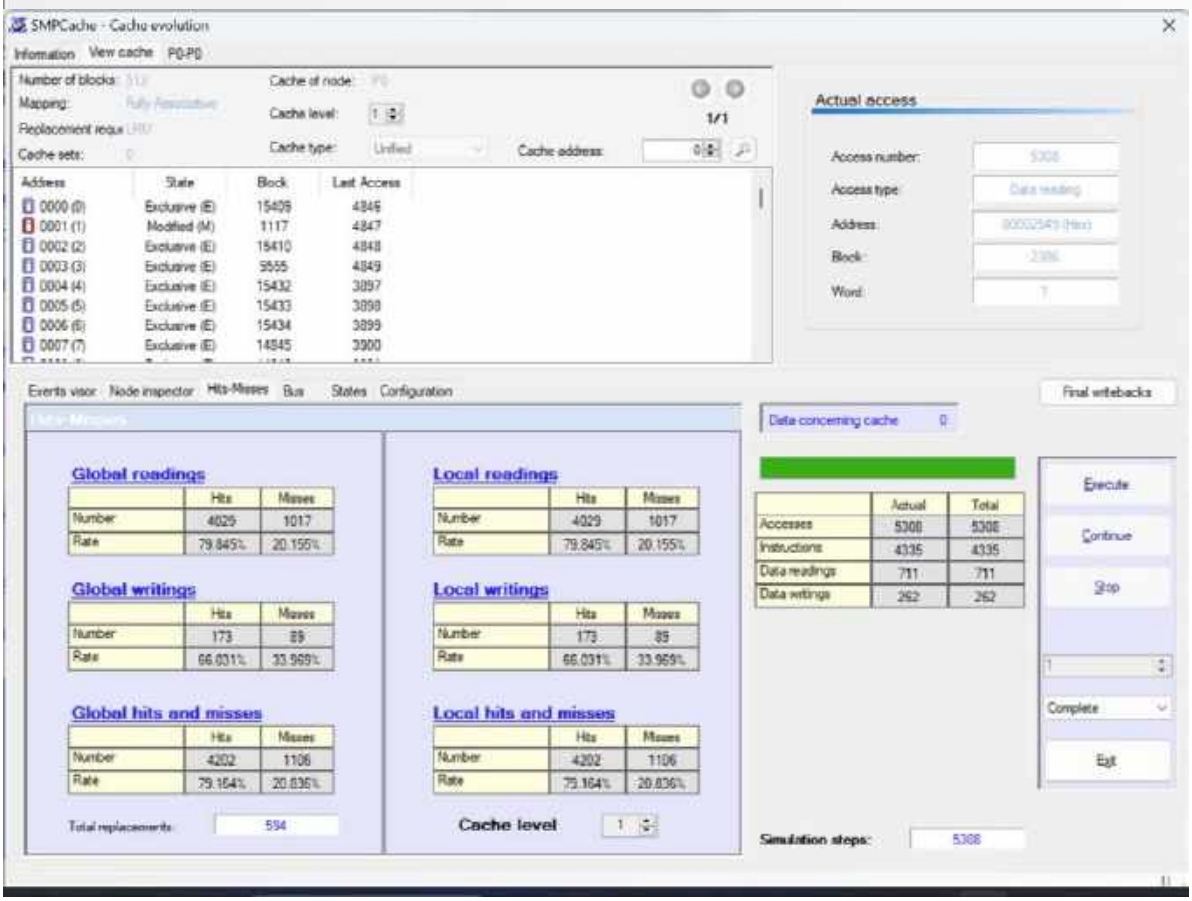
Configuration

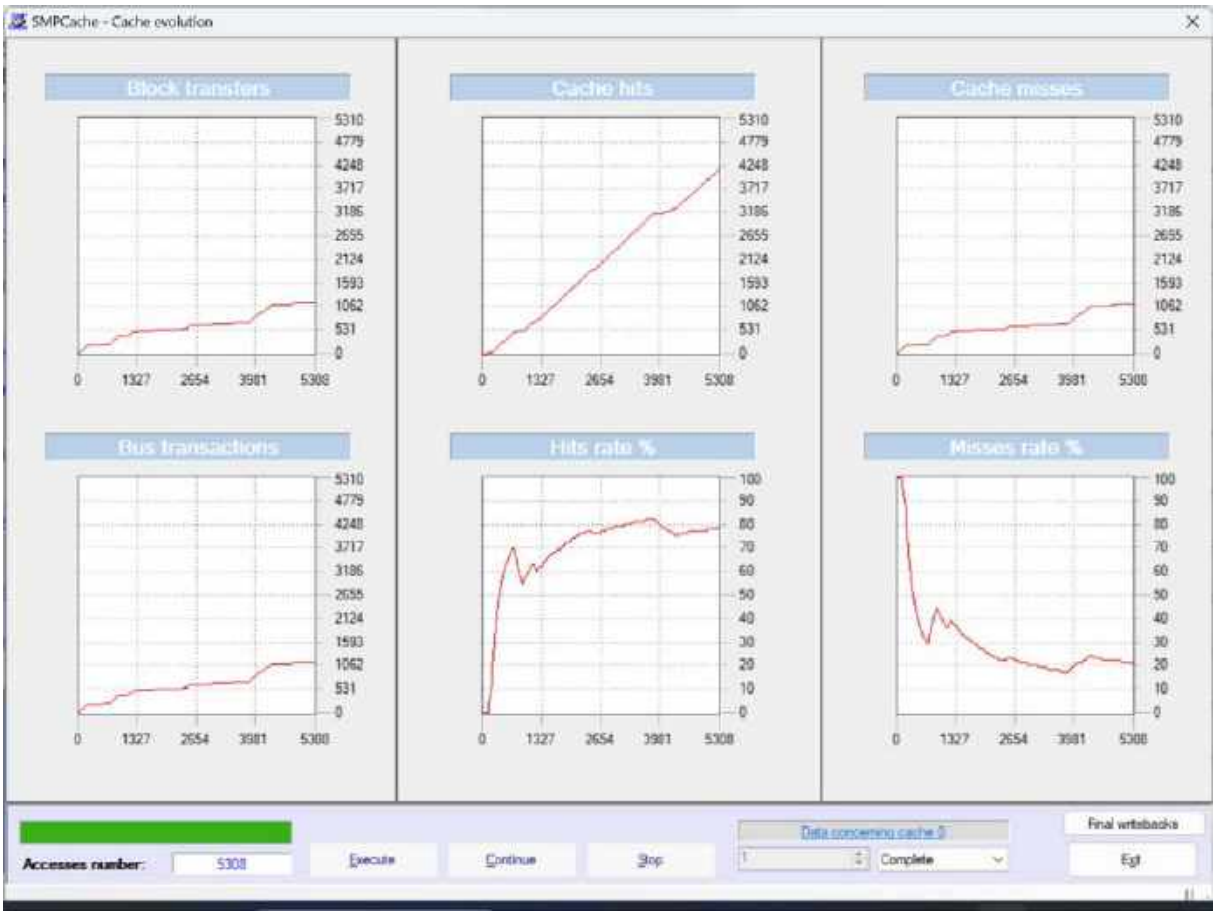
Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 16.
Main memory size = 256 KB (the number of blocks in main memory will vary).
Cache size = 4 KB (the number of blocks in cache will vary).
Mapping =
Fully-Associative.
Replacement policy = LRU.

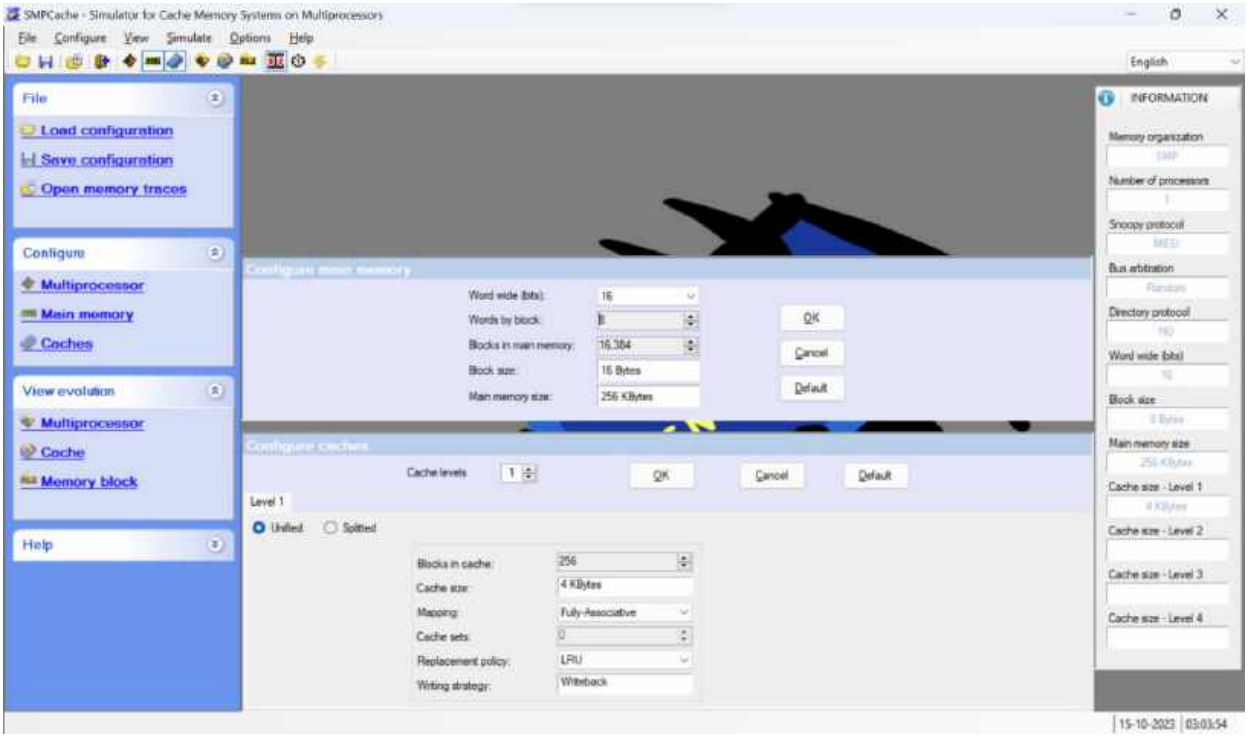
Experiment

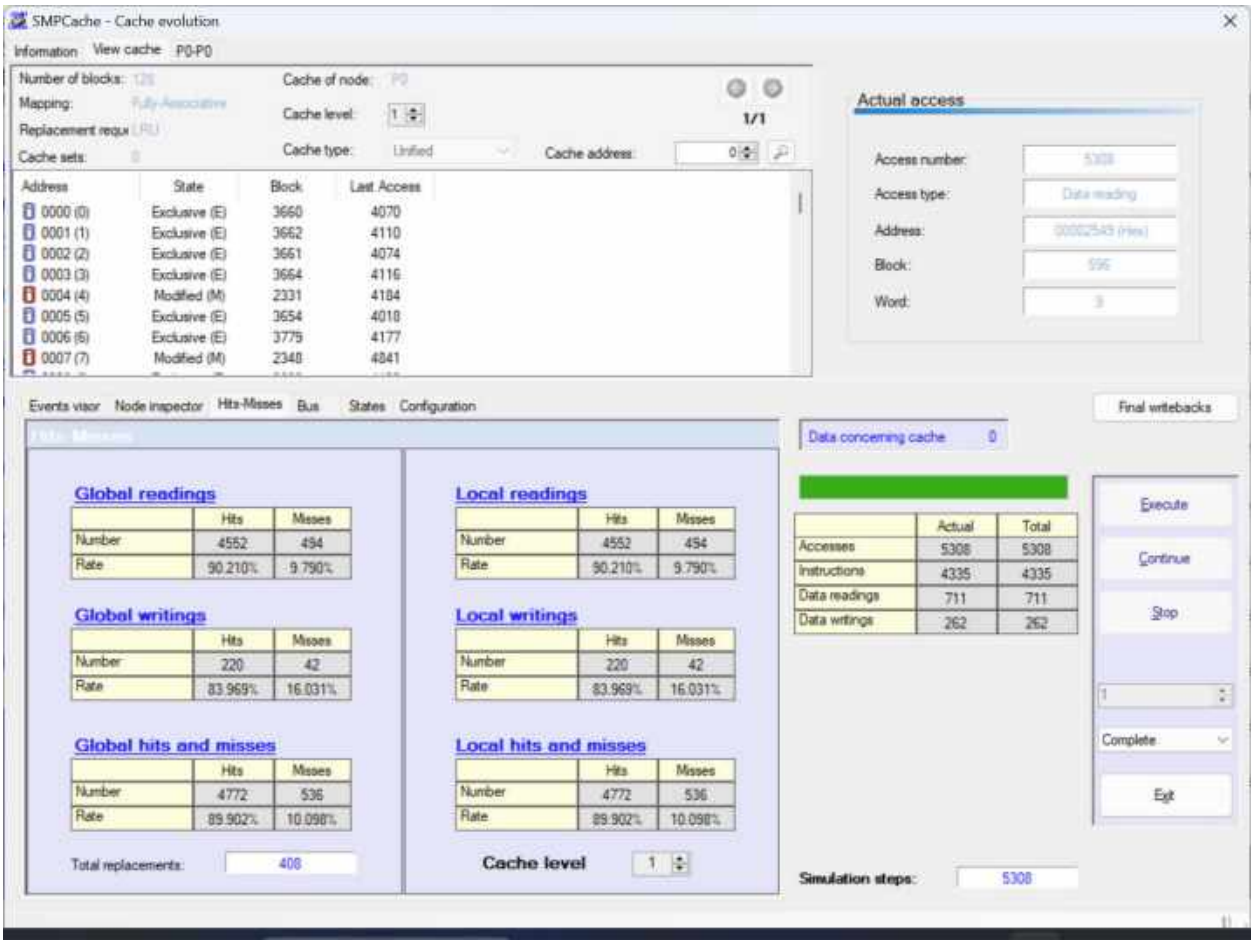
Configure the words by block using the following configurations: 4 (block size = 8 bytes), 8, 16, 32, 64, 128, 256, 512, and 1024 (block size = 2048 bytes). For each of the configurations, obtain the miss rate using the trace files: Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.

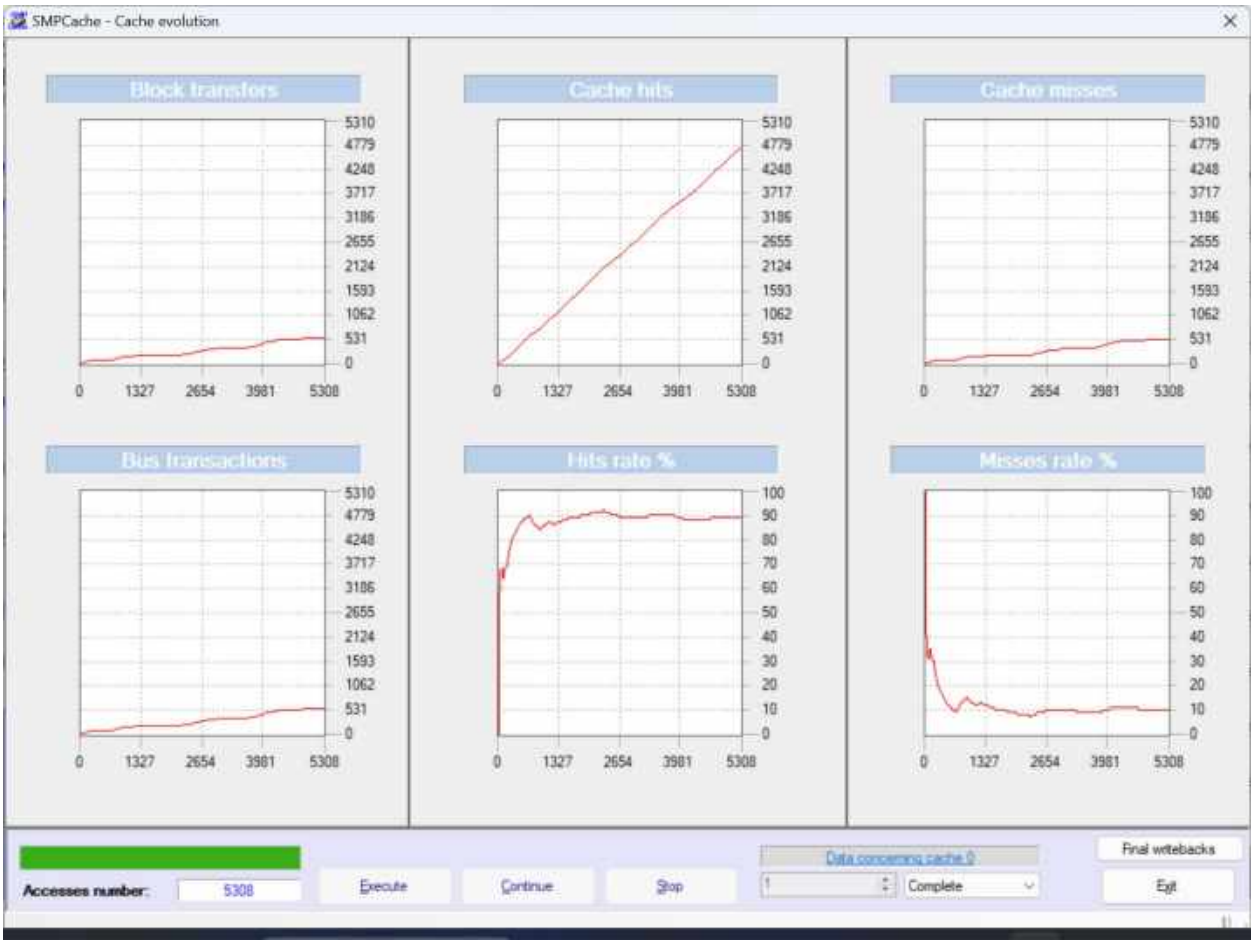

SMPCache - Simulator for Cache Memory Systems on Multiprocessors
File Configure View Simulate Options Help
English
File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
INFORMATION
Memory organization
Number of processors
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
Configure main memory
Word wide (bits): 16
Words by block: 8
Blocks in main memory: 16,384
Block size: 16 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
Level 1
Unified
Splitted
Blocks in cache: 256
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
15-10-2023 03:03:54

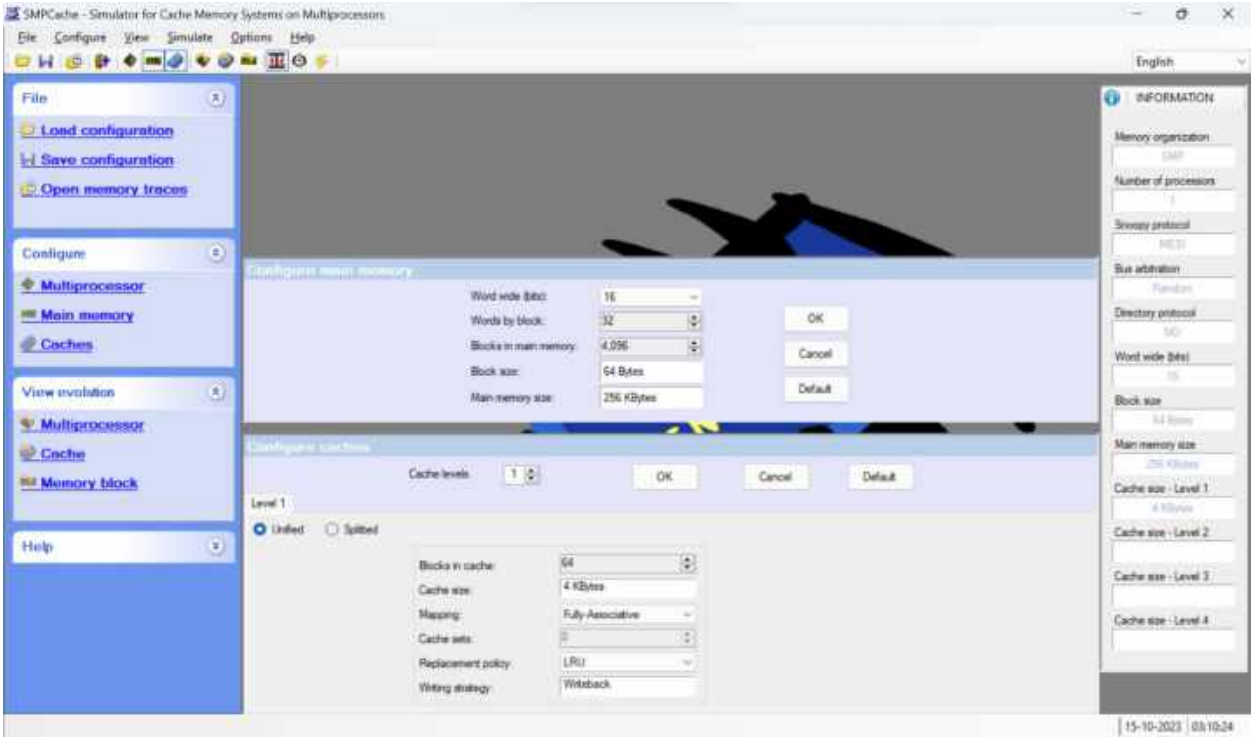

SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks
Mapping
Replacement requ
Cache sets
Cache of node
Cache level 1
Cache type Unified
Cache address 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 15409 4846
0001 (1) Modified (M) 1117 4847
0002 (2) Exclusive (E) 15410 4848
0003 (3) Exclusive (E) 5555 4849
0004 (4) Exclusive (E) 15432 3897
0005 (5) Exclusive (E) 15433 3898
0006 (6) Exclusive (E) 15434 3899
0007 (7) Exclusive (E) 14845 3900
Actual access
Access number: 5308
Access type: Data reading
Address: 00002549 (Hex)
Block: 2396
Word: 7
Events visor Node inspector Hits-Misses Bus States Configuration
Hits-Misses
Global readings
Hits Misses
Number 4029 1017
Rate 79.845% 20.155%
Global writings
Hits Misses
Number 173 89
Rate 66.031% 33.969%
Global hits and misses
Hits Misses
Number 4202 1106
Rate 79.164% 20.836%
Total replacements 594
Local readings
Hits Misses
Number 4029 1017
Rate 79.845% 20.155%
Local writings
Hits Misses
Number 173 89
Rate 66.031% 33.969%
Local hits and misses
Hits Misses
Number 4202 1106
Rate 79.164% 20.836%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Final writebacks
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308

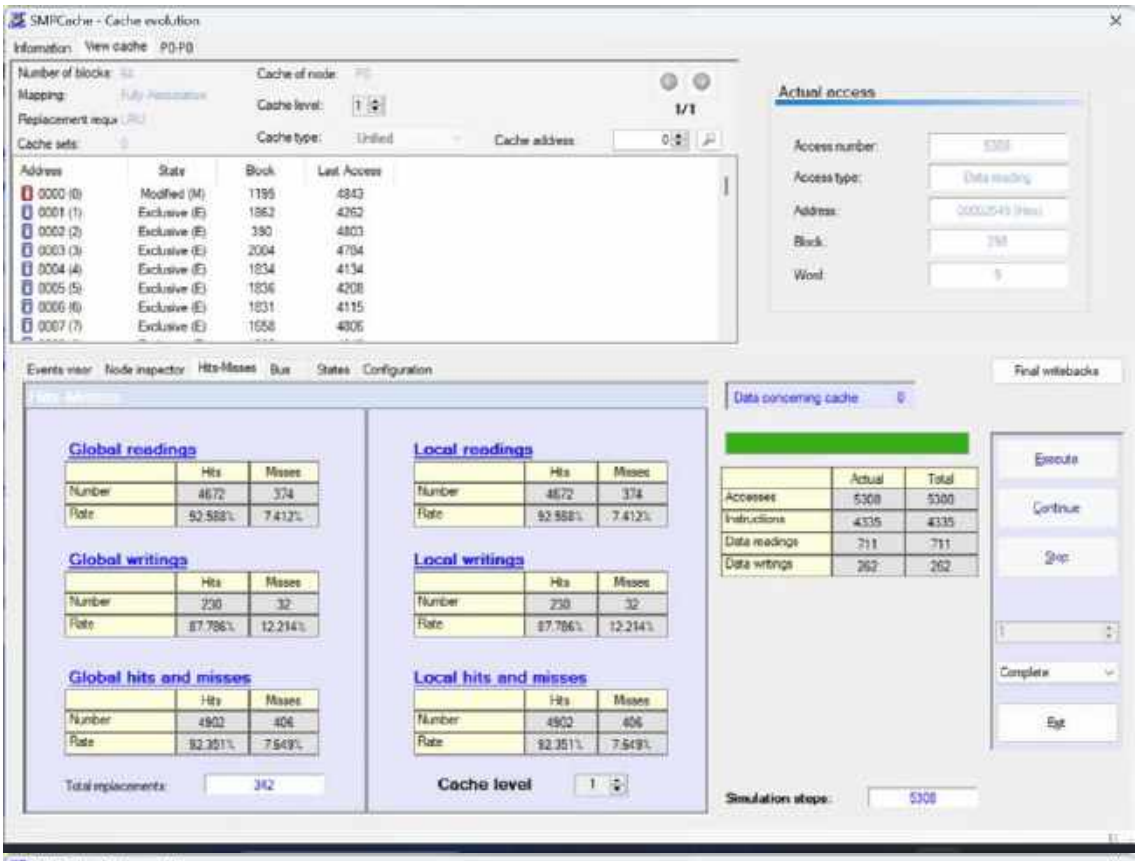

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

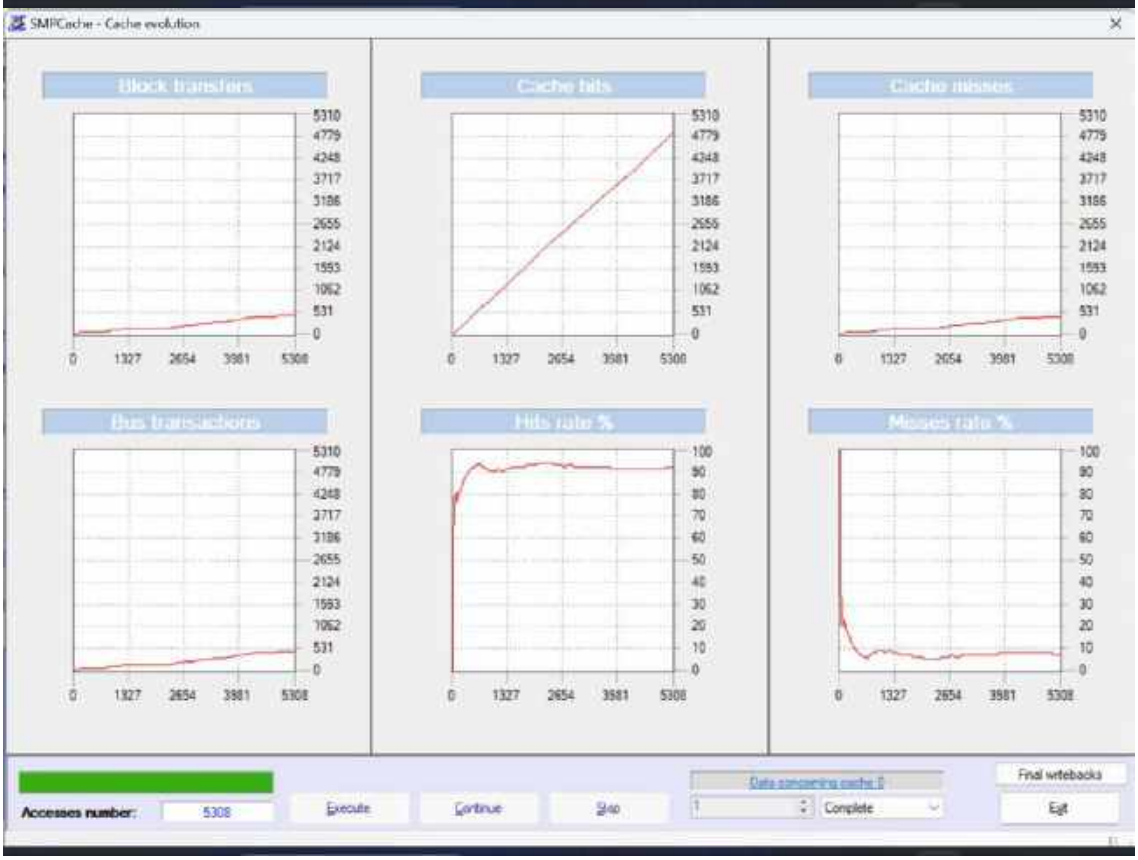

SMPCache - Simulator for Cache Memory Systems on Multiprocessors
File
Configure
View
Simulate
Options
Help
English
Load configuration
Save configuration
Open memory traces
Multiprocessor
Main memory
Caches
Multiprocessor
Cache
Memory block
INFORMATION
Memory organization
Number of processors
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
Configure main memory
Word wide (bits):
Words by block:
Blocks in main memory:
Block size:
Main memory size:
OK
Cancel
Default
Configure caches
Cache levels
Level 1
Unified
Splitted
Blocks in cache:
Cache size:
Mapping:
Cache sets:
Replacement policy:
Writing strategy:
Fully-Associative
LRU
Writeback
15-10-2023
03:03:54

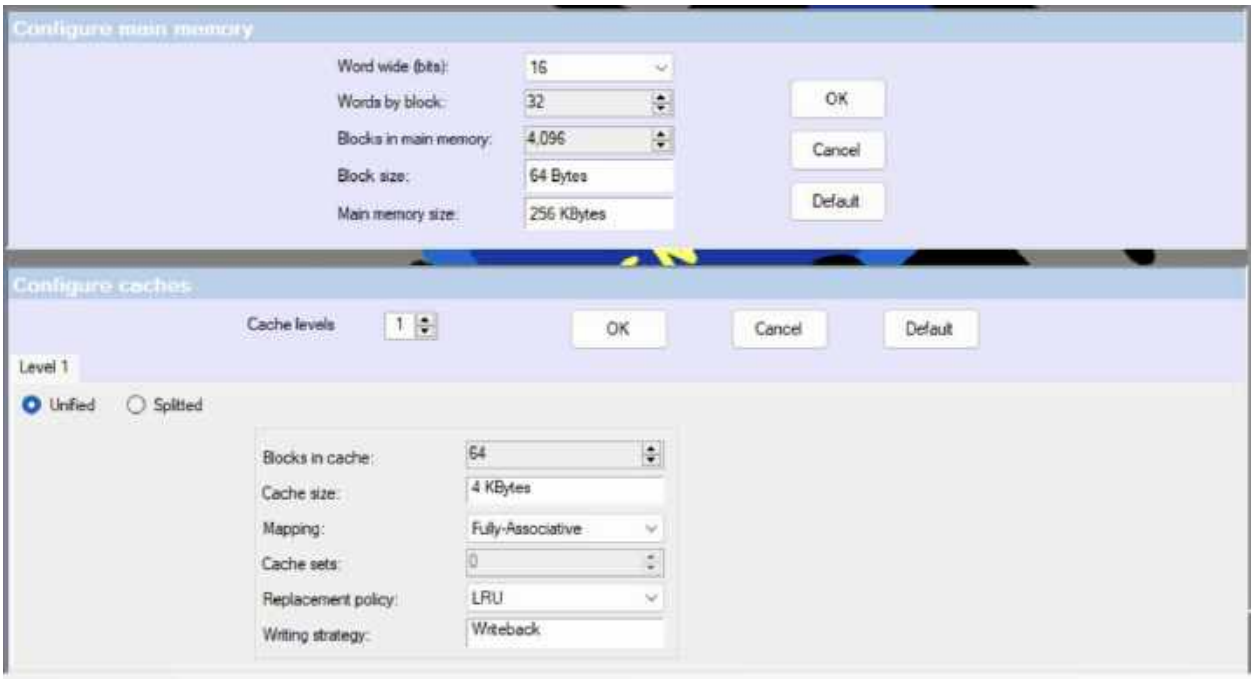

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 3660 4070
0001 (1) Exclusive (E) 3662 4110
0002 (2) Exclusive (E) 3661 4074
0003 (3) Exclusive (E) 3664 4116
0004 (4) Modified (M) 2331 4184
0005 (5) Exclusive (E) 3654 4018
0006 (6) Exclusive (E) 3775 4177
0007 (7) Modified (M) 2348 4841
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viaor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number 4552 494
Rate 90.210% 9.790%
Global writings
Number 220 42
Rate 83.969% 16.031%
Global hits and misses
Number 4772 536
Rate 89.902% 10.098%
Total replacements:
408
Local readings
Number 4552 494
Rate 90.210% 9.790%
Local writings
Number 220 42
Rate 83.969% 16.031%
Local hits and misses
Number 4772 536
Rate 89.902% 10.098%
Cache level
1
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps:
5308

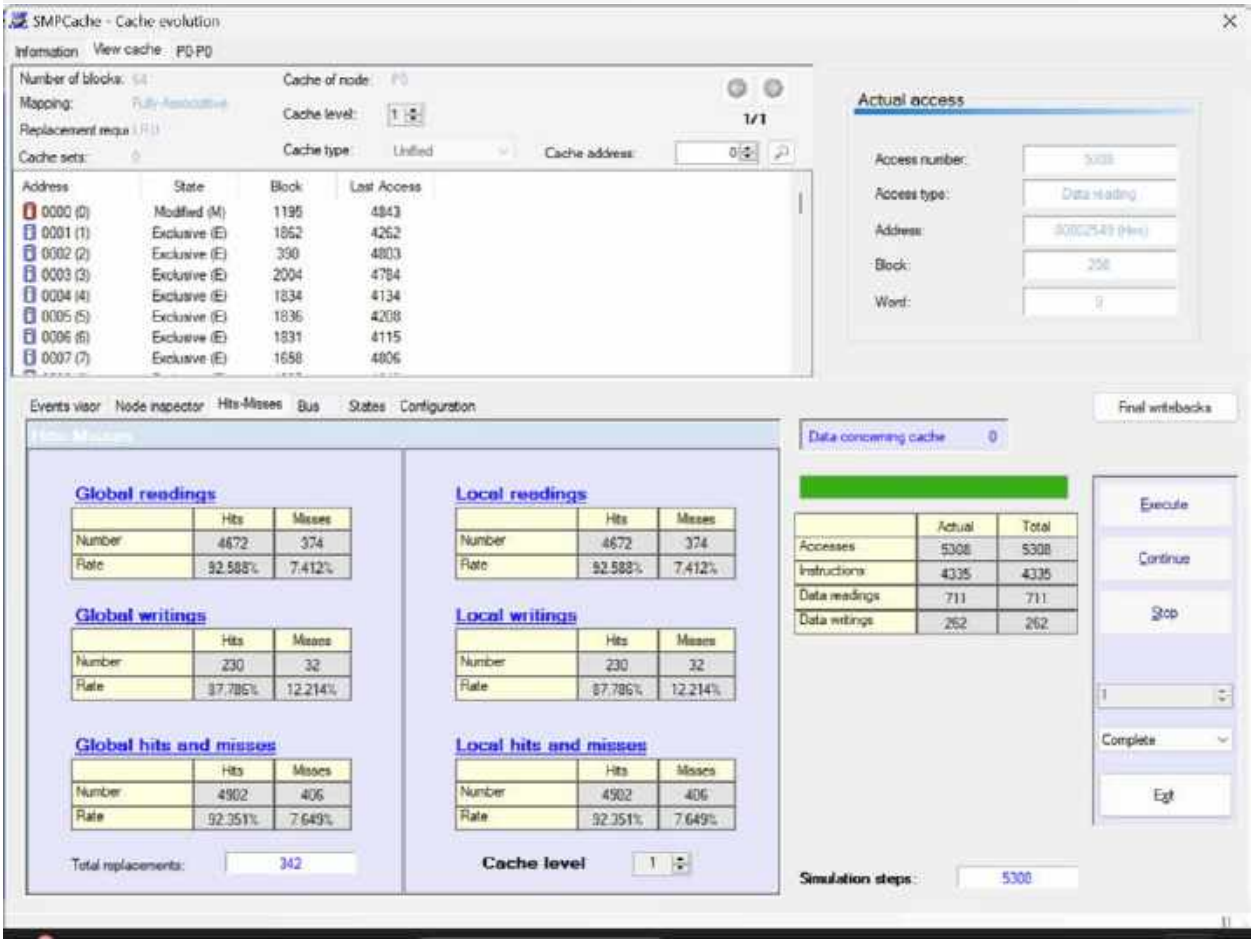

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

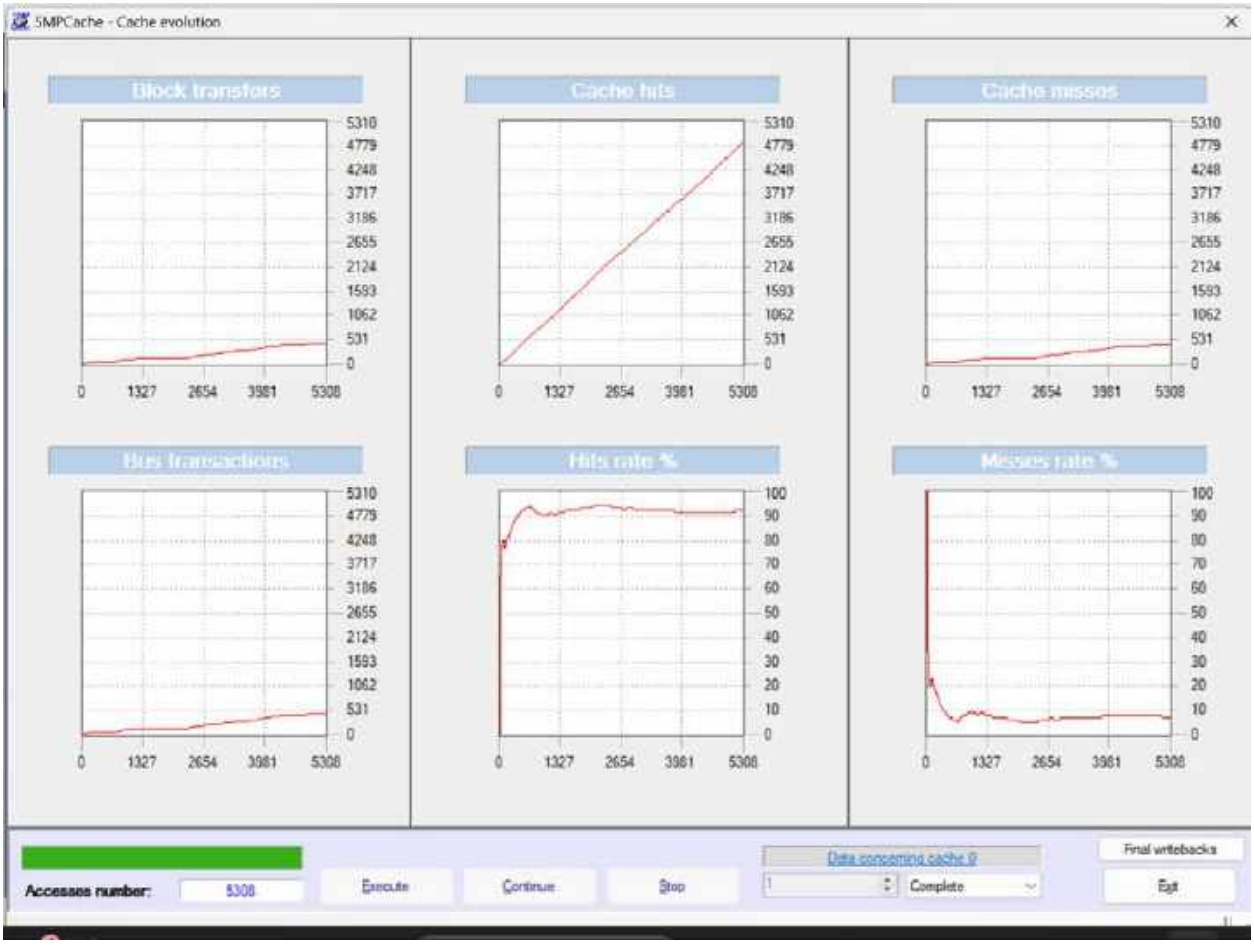

SMPCache - Simulator for Cache Memory Systems on Multiprocessors
File
Configure
View
Simulate
Options
Help
English
File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Configure main memory
Word wide (bits):
Words by block:
Blocks in main memory:
Block size:
Main memory size:
OK
Cancel
Default
Configure caches
Cache levels:
Level 1
Unified
Splitted
Blocks in cache:
Cache size:
Mapping:
Fully-Associative
Cache sets:
Replacement policy:
LRU
Writing strategy:
Writeback
INFORMATION
Memory organization
Number of processors
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
15-10-2023 03:10:24

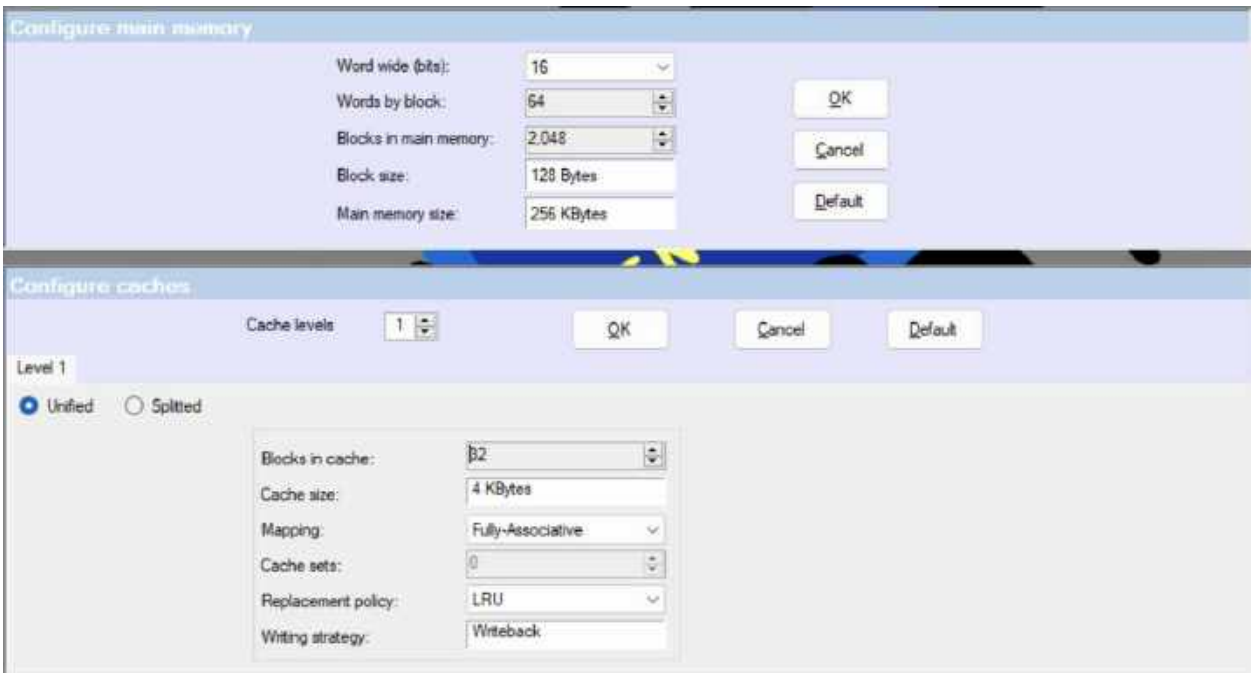

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 1195 4843
0001 (1) Exclusive (E) 1862 4262
0002 (2) Exclusive (E) 390 4803
0003 (3) Exclusive (E) 2004 4784
0004 (4) Exclusive (E) 1834 4134
0005 (5) Exclusive (E) 1836 4208
0006 (6) Exclusive (E) 1831 4115
0007 (7) Exclusive (E) 1658 4806
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events view
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
Global readings
Hits
Misses
Number 4672 374
Rate 92.588% 7.412%
Global writings
Number 230 32
Rate 87.786% 12.214%
Global hits and misses
Number 4902 406
Rate 92.351% 7.649%
Total replacements: 342
Local readings
Number 4672 374
Rate 92.588% 7.412%
Local writings
Number 230 32
Rate 87.786% 12.214%
Local hits and misses
Number 4902 406
Rate 92.351% 7.649%
Cache level
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps:
5308

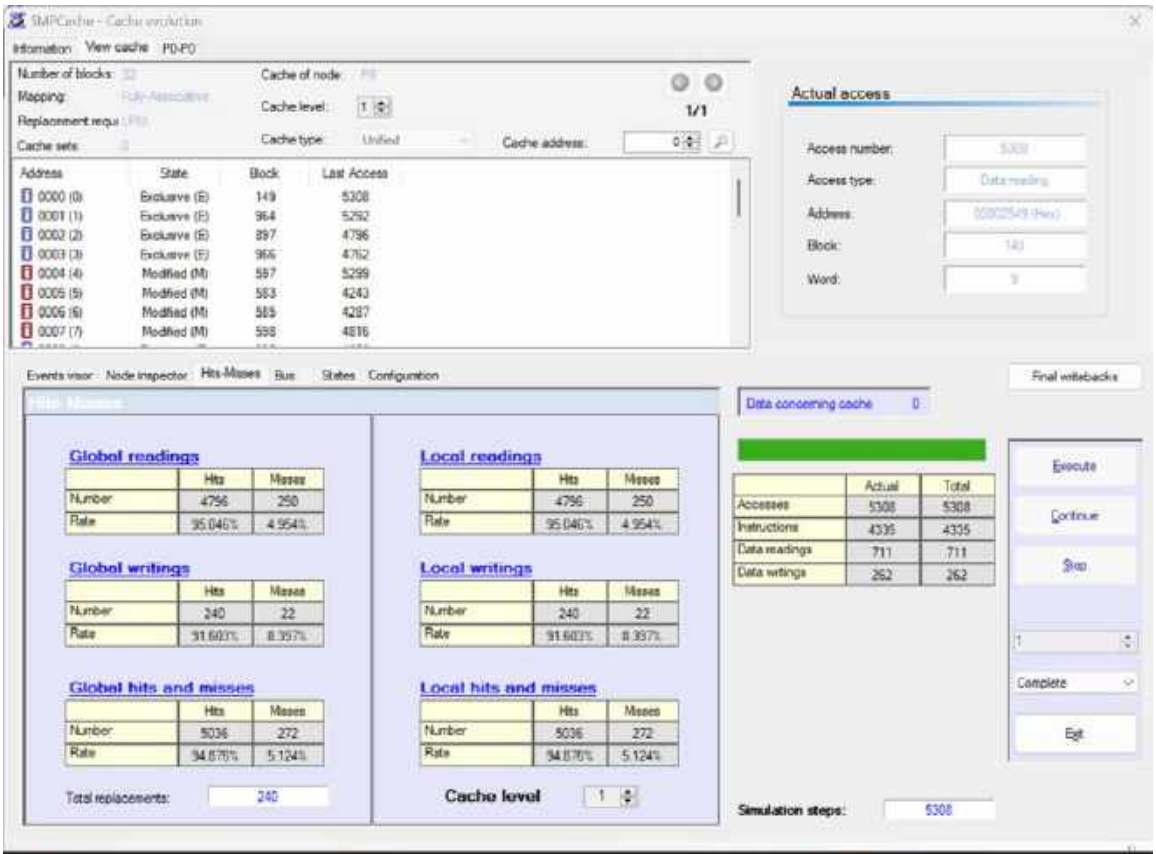

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache
Complete
Final writebacks
Exit

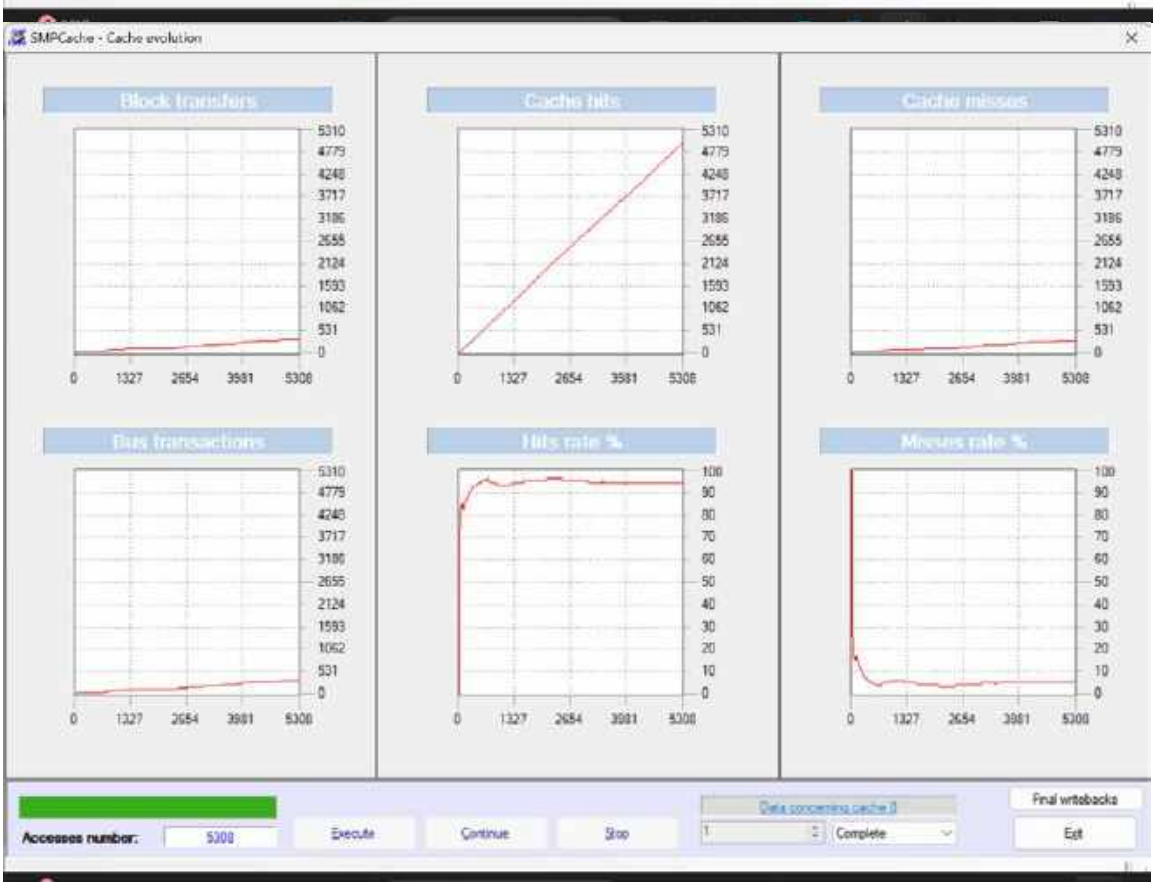

Configure main memory
Word wide (bits): 16
Words by block: 32
Blocks in main memory: 4,096
Block size: 64 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 64
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

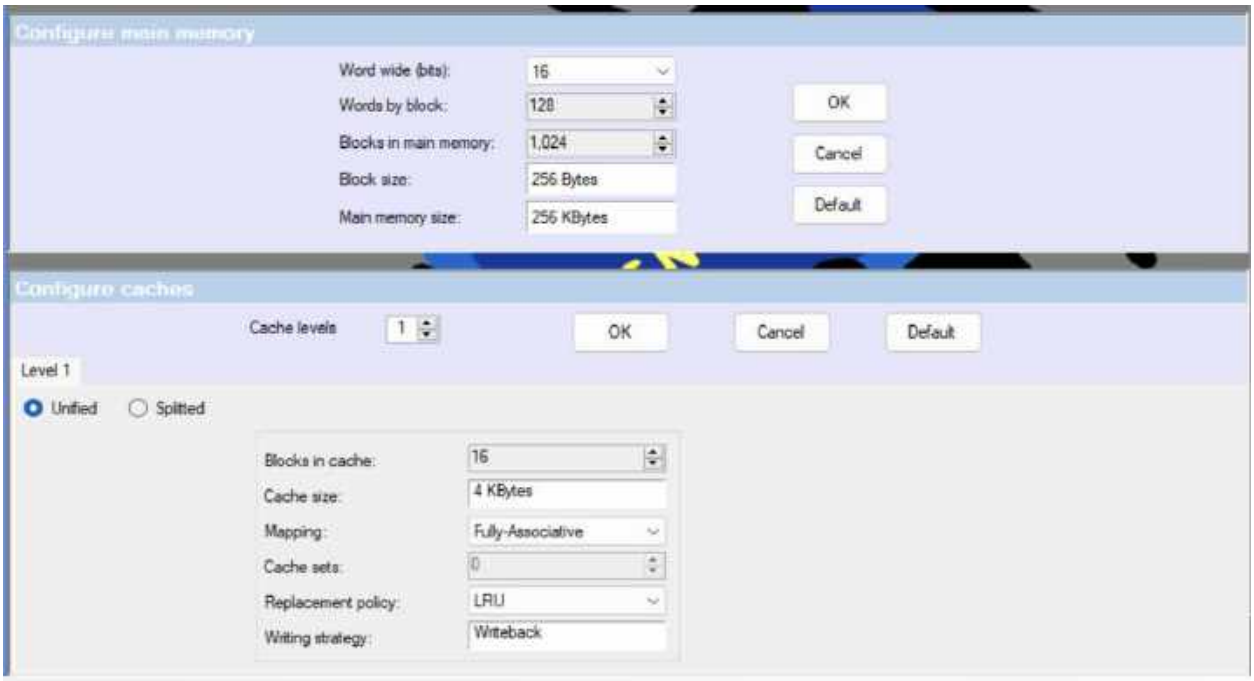

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 1195 4843
0001 (1) Exclusive (E) 1862 4262
0002 (2) Exclusive (E) 390 4803
0003 (3) Exclusive (E) 2004 4784
0004 (4) Exclusive (E) 1834 4134
0005 (5) Exclusive (E) 1836 4208
0006 (6) Exclusive (E) 1831 4115
0007 (7) Exclusive (E) 1658 4806
Actual access
Access number:
Access type: Data reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4672 374
Rate 92.588% 7.412%
Global writings
Hits Misses
Number 230 32
Rate 87.786% 12.214%
Global hits and misses
Hits Misses
Number 4902 406
Rate 92.351% 7.649%
Total replacements: 342
Local readings
Hits Misses
Number 4672 374
Rate 92.588% 7.412%
Local writings
Hits Misses
Number 230 32
Rate 87.786% 12.214%
Local hits and misses
Hits Misses
Number 4902 406
Rate 92.351% 7.649%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308

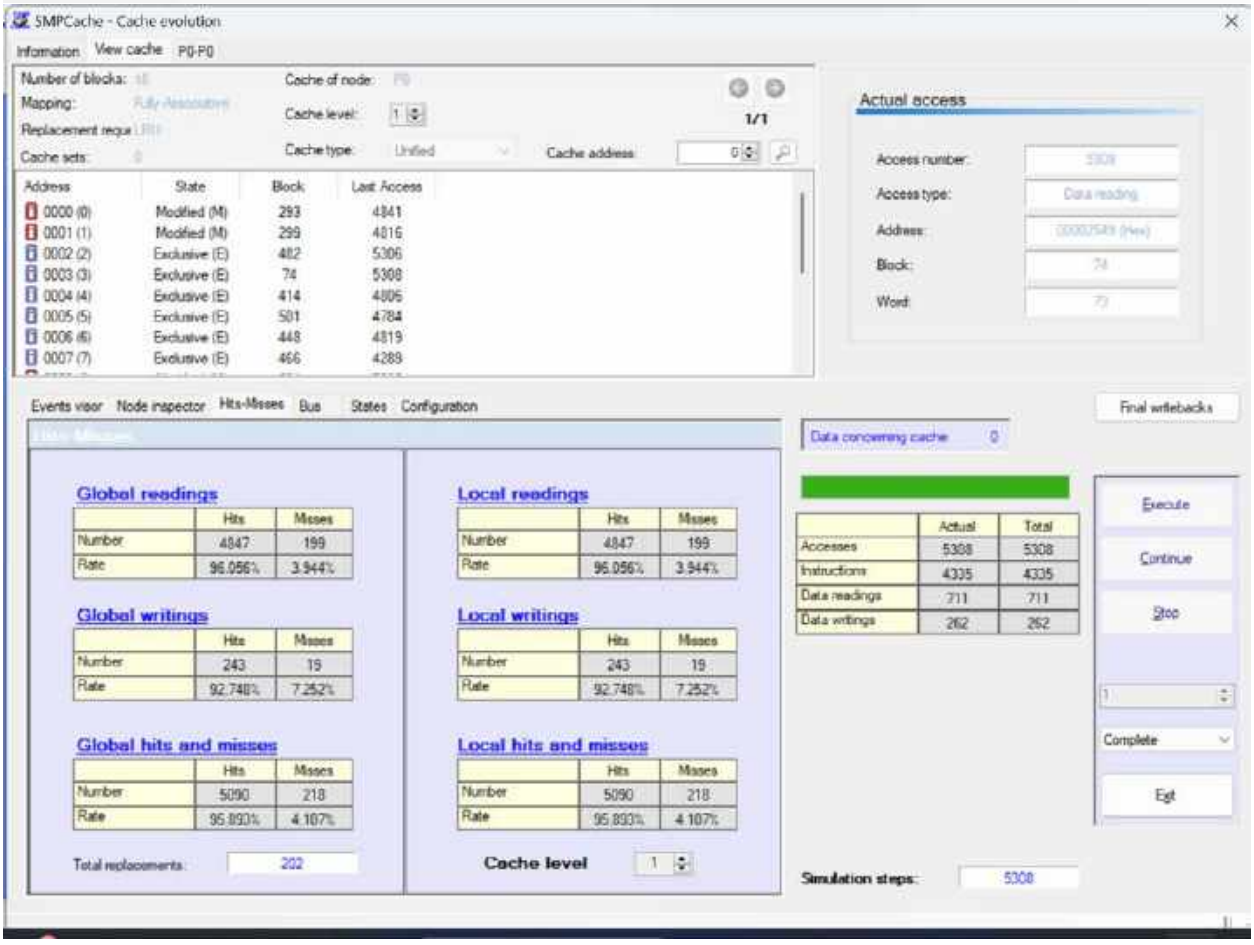

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

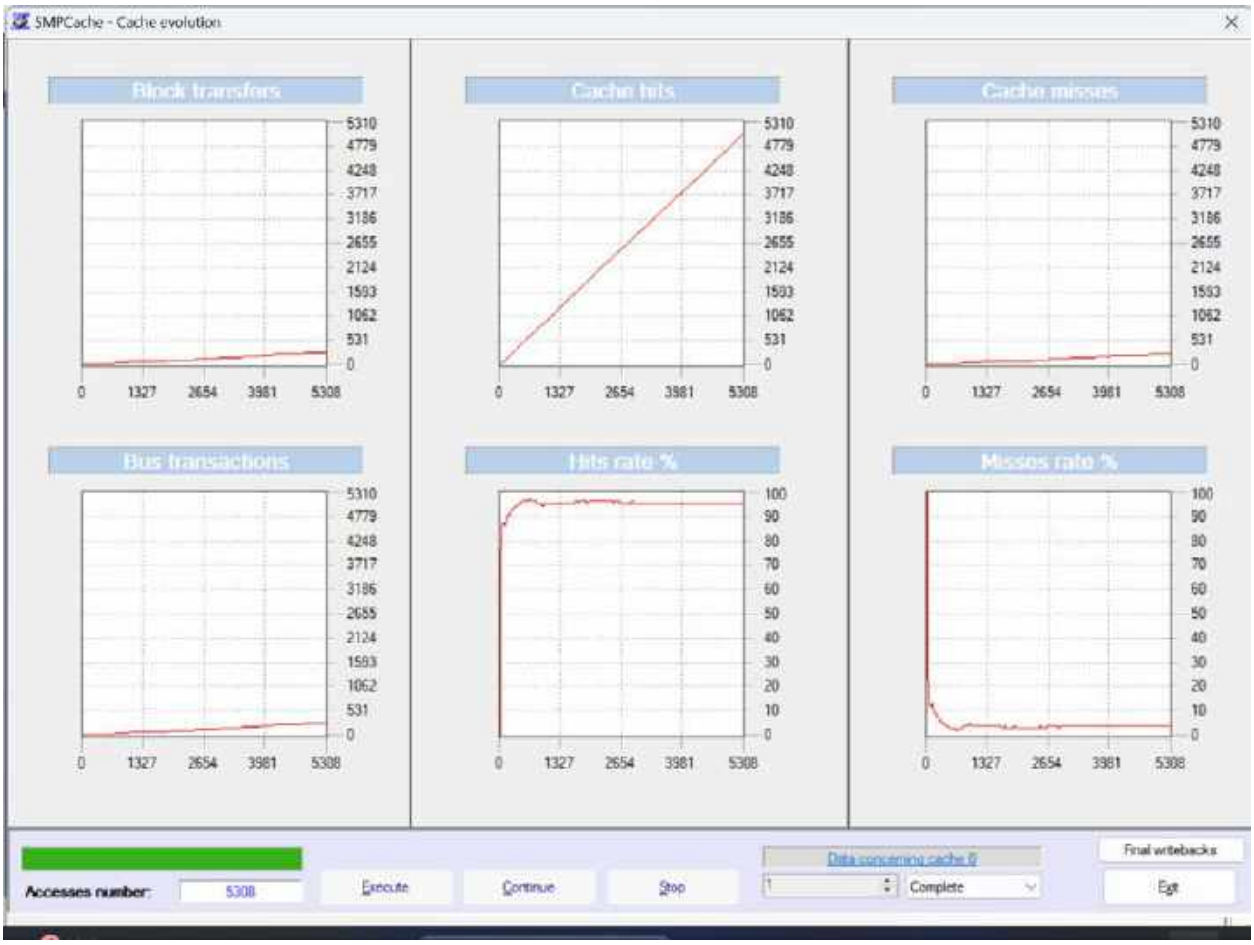

Configure main memory
Word wide (bits): 16
Words by block: 64
Blocks in main memory: 2.048
Block size: 128 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 32
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

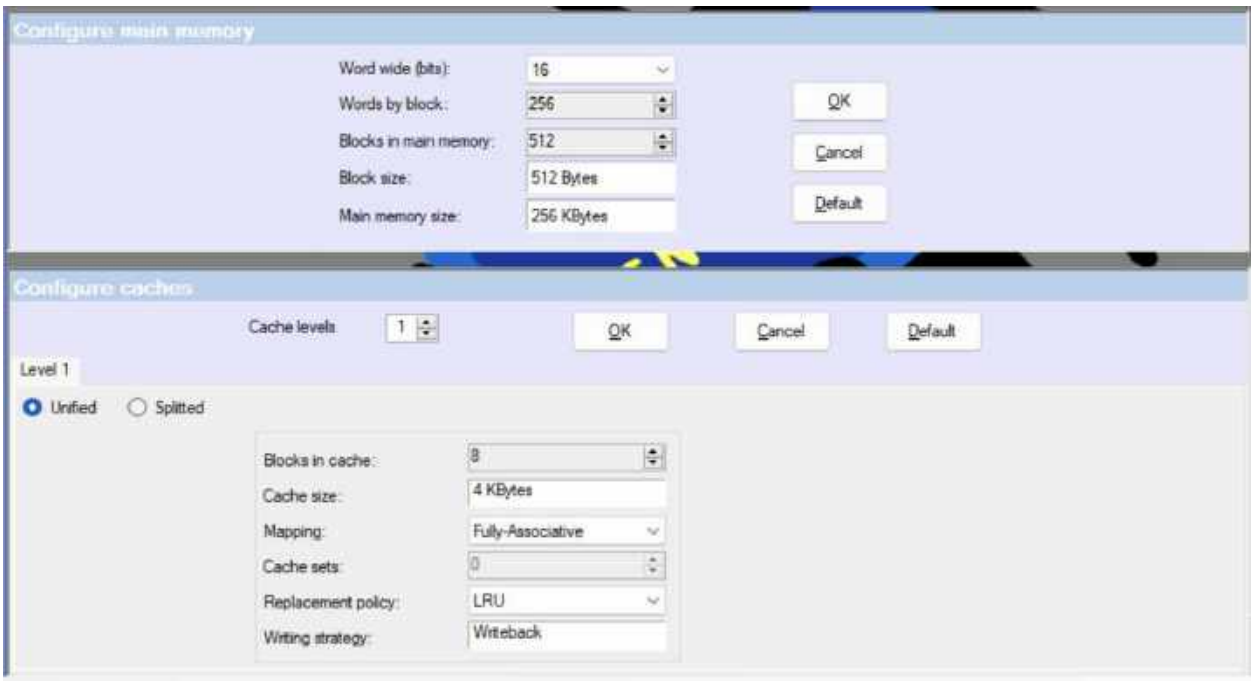

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 149 5308
0001 (1) Exclusive (E) 964 5292
0002 (2) Exclusive (E) 897 4796
0003 (3) Exclusive (E) 966 4762
0004 (4) Modified (M) 597 5299
0005 (5) Modified (M) 583 4243
0006 (6) Modified (M) 585 4287
0007 (7) Modified (M) 598 4816
Actual access
Access number:
Access type:
Data reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number 4796 250
Rate 95.046% 4.954%
Global writings
Number 240 22
Rate 91.603% 8.397%
Global hits and misses
Number 5036 272
Rate 94.878% 5.124%
Total replacements: 240
Local readings
Number 4796 250
Rate 95.046% 4.954%
Local writings
Number 240 22
Rate 91.603% 8.397%
Local hits and misses
Number 5036 272
Rate 94.878% 5.124%
Cache level
1
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps:
5308

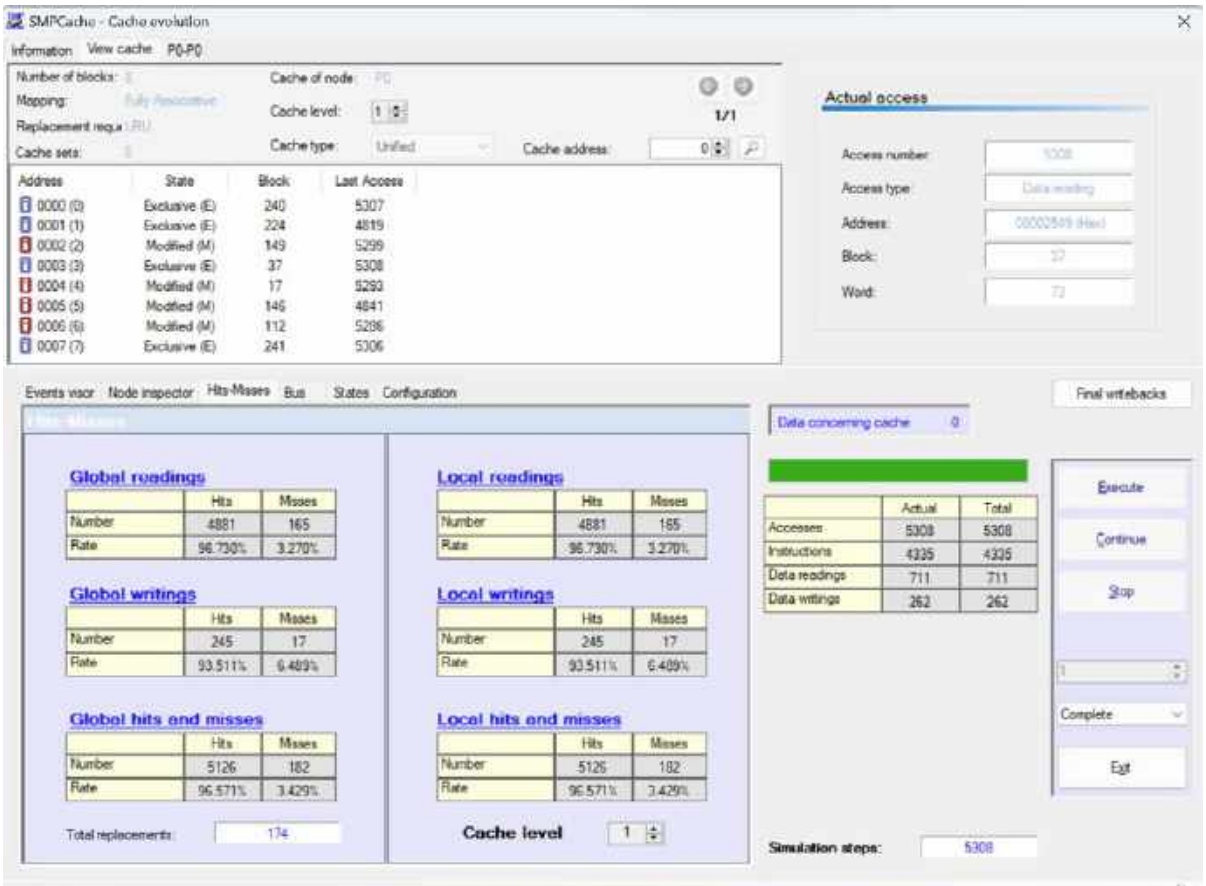

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

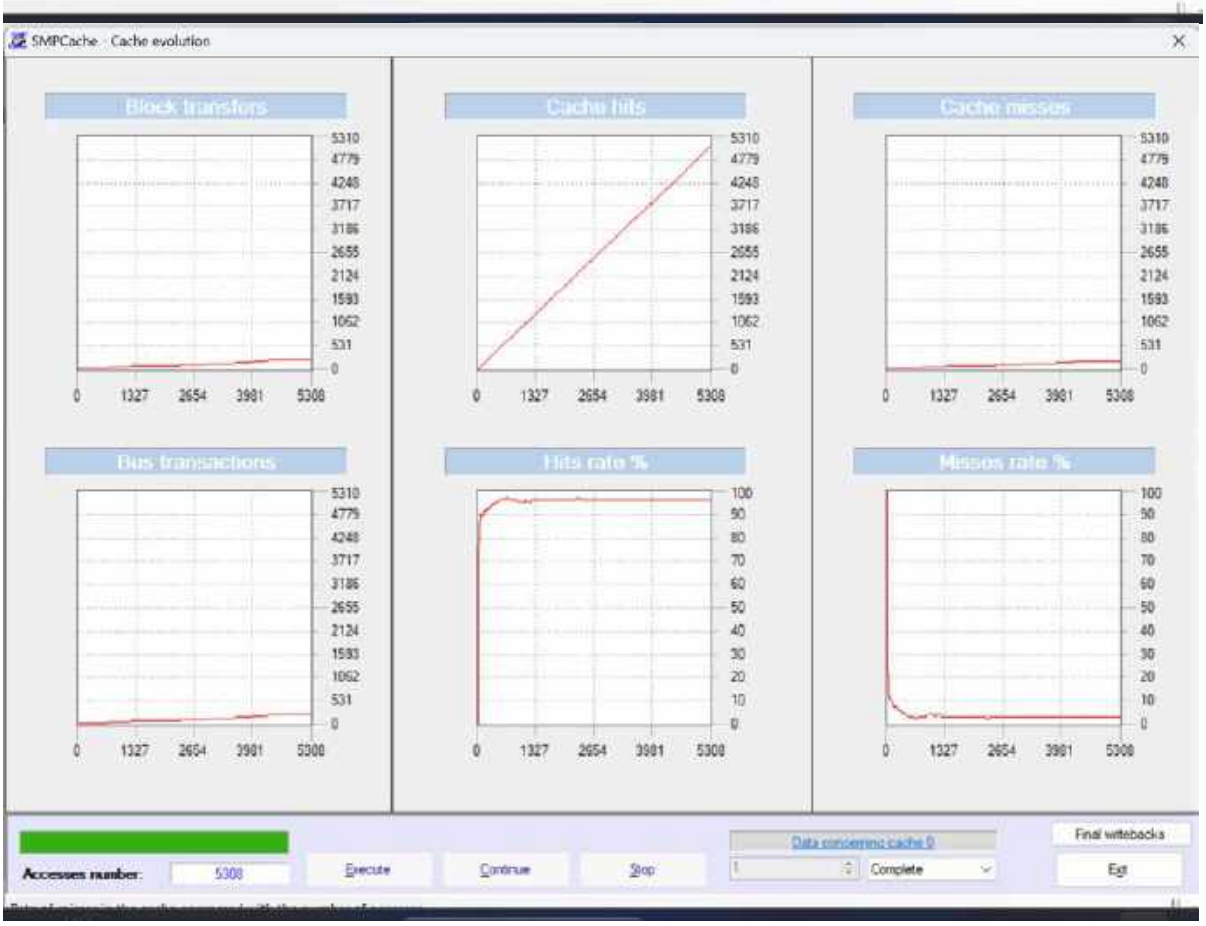

Configure main memory
Word wide (bits): 16
Words by block: 128
Blocks in main memory: 1,024
Block size: 256 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 16
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

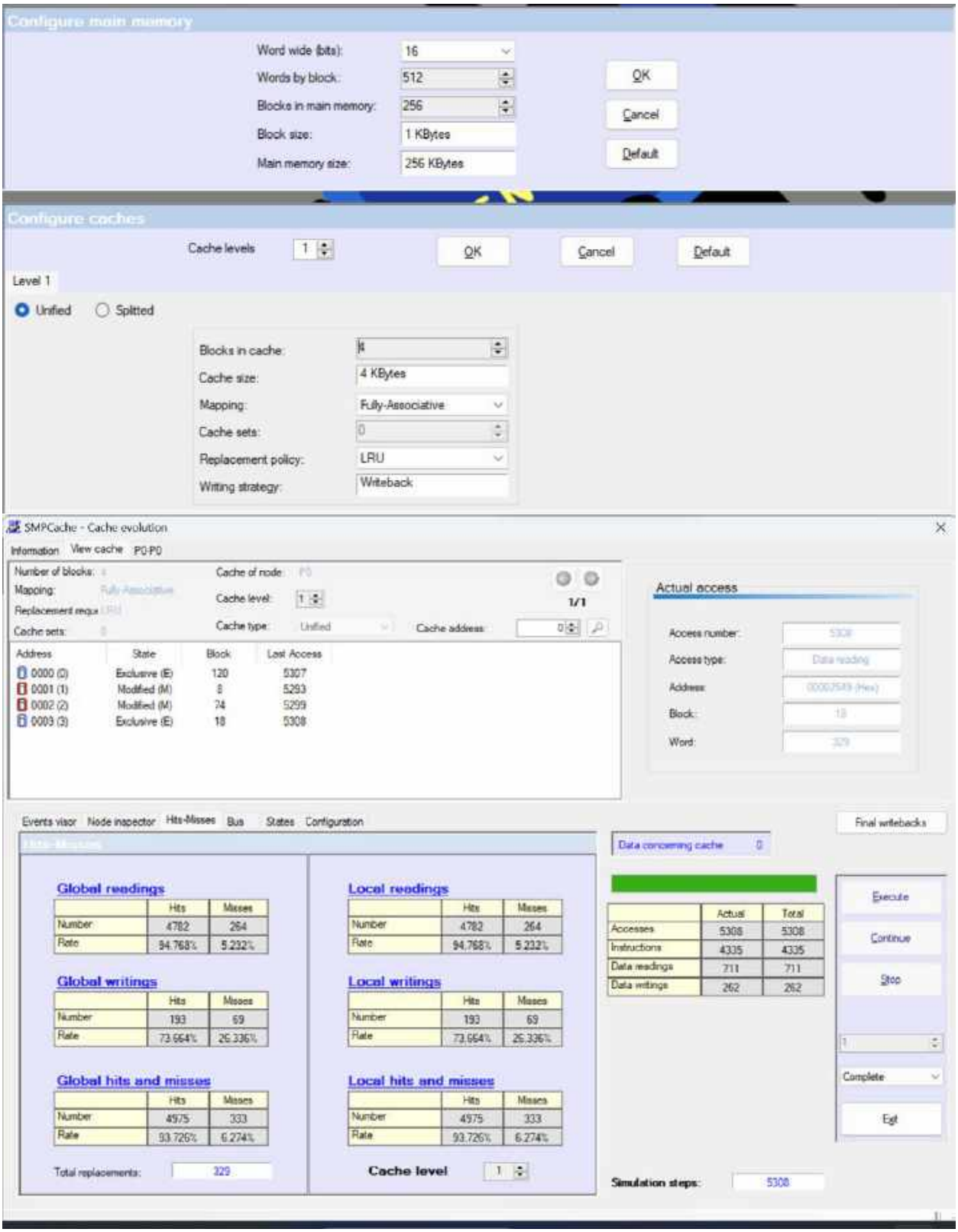

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement regul
Cache sets:
Cache of node:
Cache level:
Cache type: Unified
Cache address:
1/1
Address State Block Last Access
0000 (0) Modified (M) 293 4841
0001 (1) Modified (M) 299 4816
0002 (2) Exclusive (E) 482 5306
0003 (3) Exclusive (E) 74 5308
0004 (4) Exclusive (E) 414 4806
0005 (5) Exclusive (E) 501 4784
0006 (6) Exclusive (E) 448 4819
0007 (7) Exclusive (E) 466 4289
Actual access
Access number:
Access type: Data reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4847 199
Rate 96.056% 3.944%
Global writings
Hits Misses
Number 243 19
Rate 92.748% 7.252%
Global hits and misses
Hits Misses
Number 5090 218
Rate 95.893% 4.107%
Total replacements: 202
Local readings
Hits Misses
Number 4847 199
Rate 96.056% 3.944%
Local writings
Hits Misses
Number 243 19
Rate 92.748% 7.252%
Local hits and misses
Hits Misses
Number 5090 218
Rate 95.893% 4.107%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308

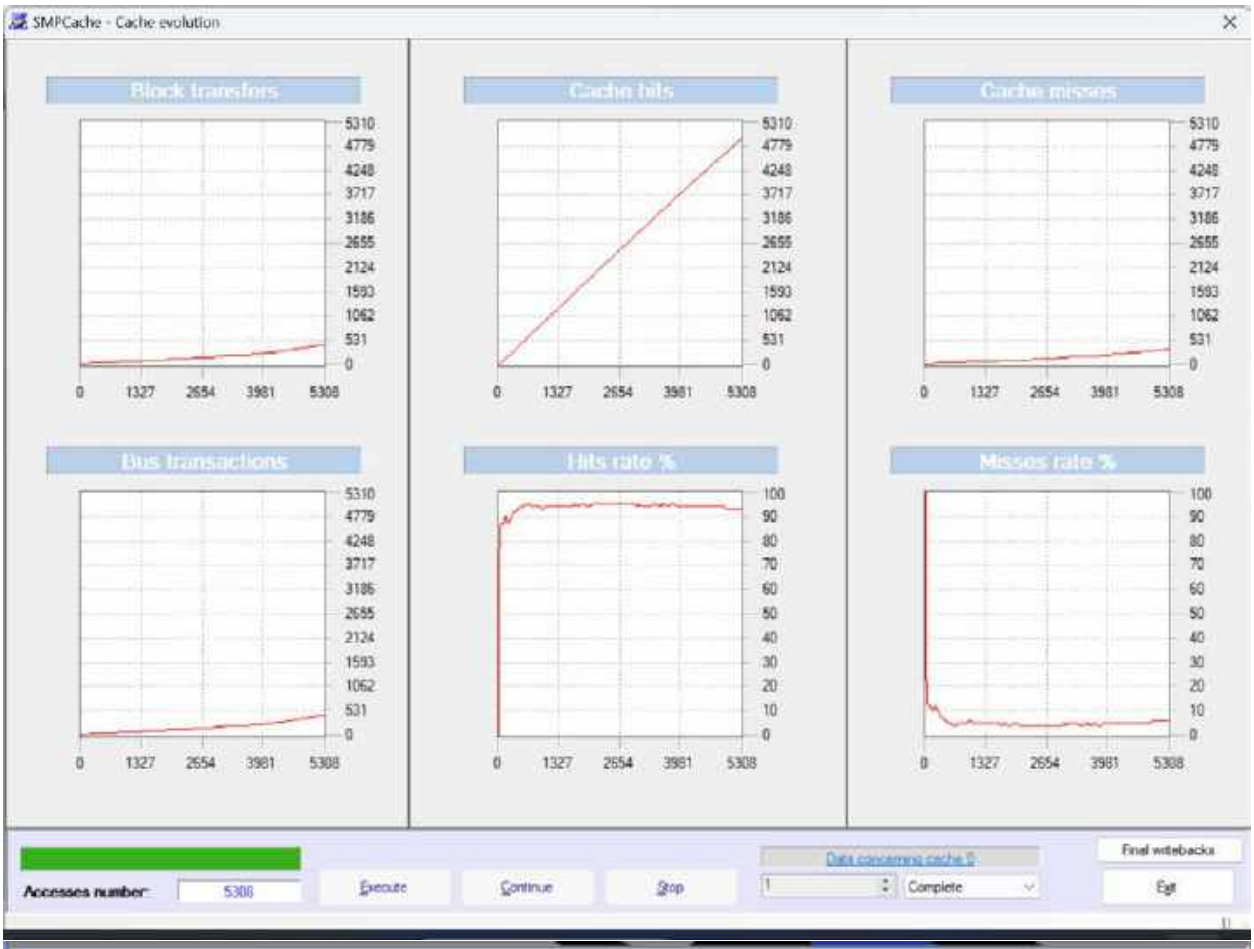

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
1
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits):
16
Words by block:
256
Blocks in main memory:
512
Block size:
512 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

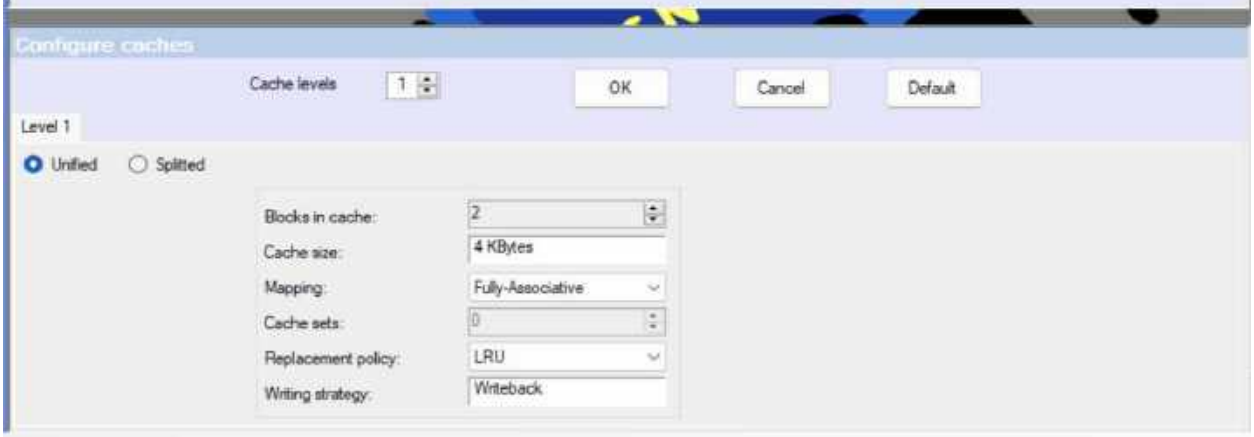

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.:
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 240 5307
0001 (1) Exclusive (E) 224 4819
0002 (2) Modified (M) 149 5299
0003 (3) Exclusive (E) 37 5308
0004 (4) Modified (M) 17 5293
0005 (5) Modified (M) 146 4841
0006 (6) Modified (M) 112 5286
0007 (7) Exclusive (E) 241 5306
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4881 165
Rate 96.730% 3.270%
Global writings
Number 245 17
Rate 93.511% 6.489%
Global hits and misses
Number 5126 182
Rate 96.571% 3.429%
Total replacements: 174
Local readings
Number 4881 165
Rate 96.730% 3.270%
Local writings
Number 245 17
Rate 93.511% 6.489%
Local hits and misses
Number 5126 182
Rate 96.571% 3.429%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308

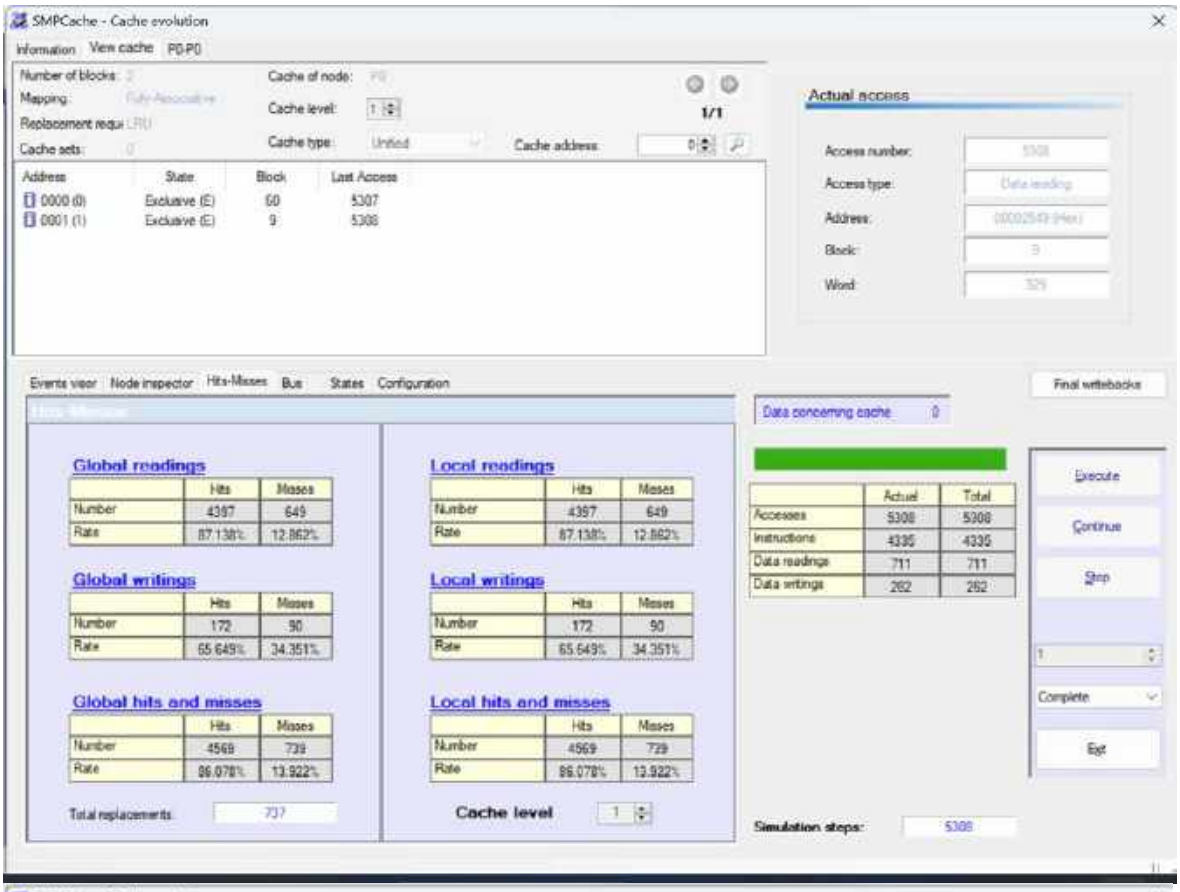

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number: 5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

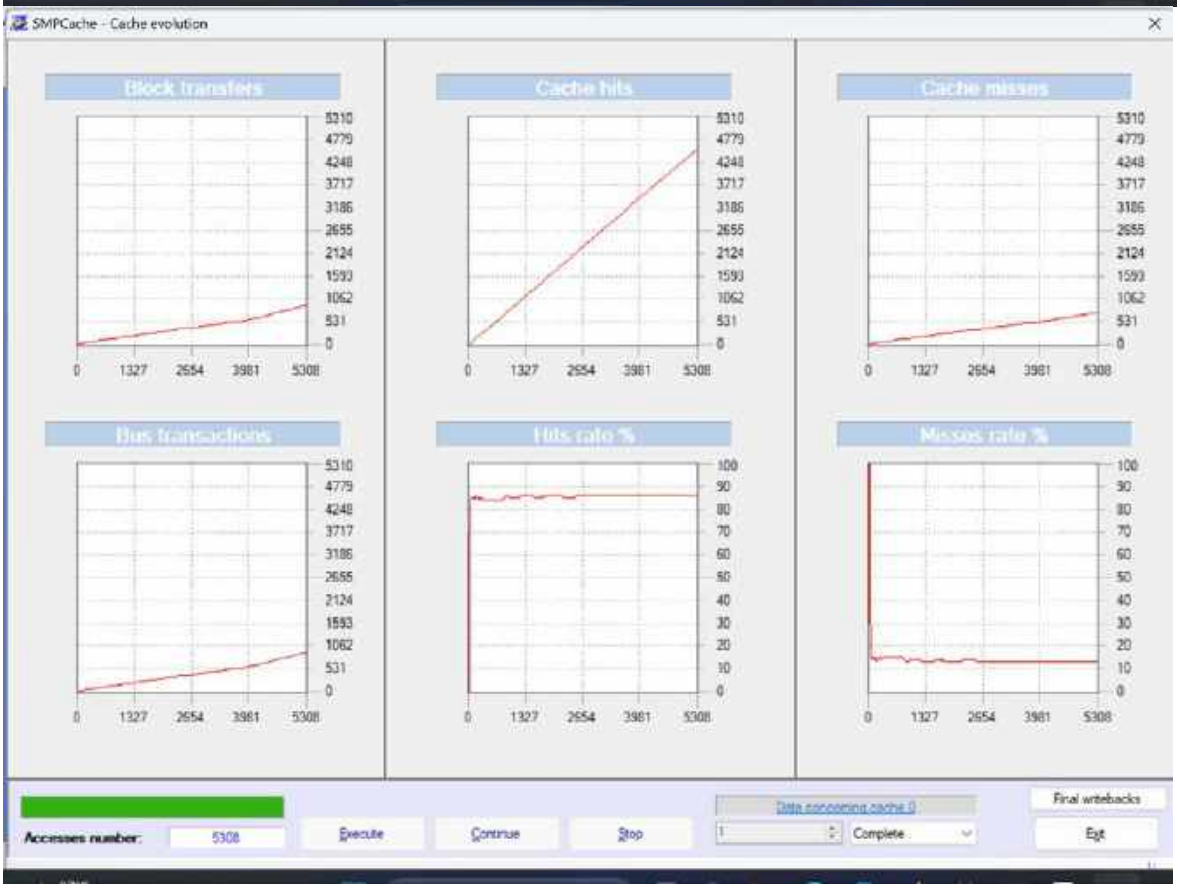

Configure main memory
Word wide (bits): 16
Words by block: 512
Blocks in main memory: 256
Block size: 1 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 4
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 120 5307
0001 (1) Modified (M) 8 5293
0002 (2) Modified (M) 74 5299
0003 (3) Exclusive (E) 18 5308
Actual access
Access number: 5308
Access type: Data reading
Address: 00002549 (Hex)
Block: 18
Word: 329
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4782 264
Rate 94.768% 5.232%
Global writings
Hits Misses
Number 193 69
Rate 73.664% 26.336%
Global hits and misses
Hits Misses
Number 4975 333
Rate 93.726% 6.274%
Total replacements: 329
Local readings
Hits Misses
Number 4782 264
Rate 94.768% 5.232%
Local writings
Hits Misses
Number 193 69
Rate 73.664% 26.336%
Local hits and misses
Hits Misses
Number 4975 333
Rate 93.726% 6.274%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Complete
Final writebacks
Exit

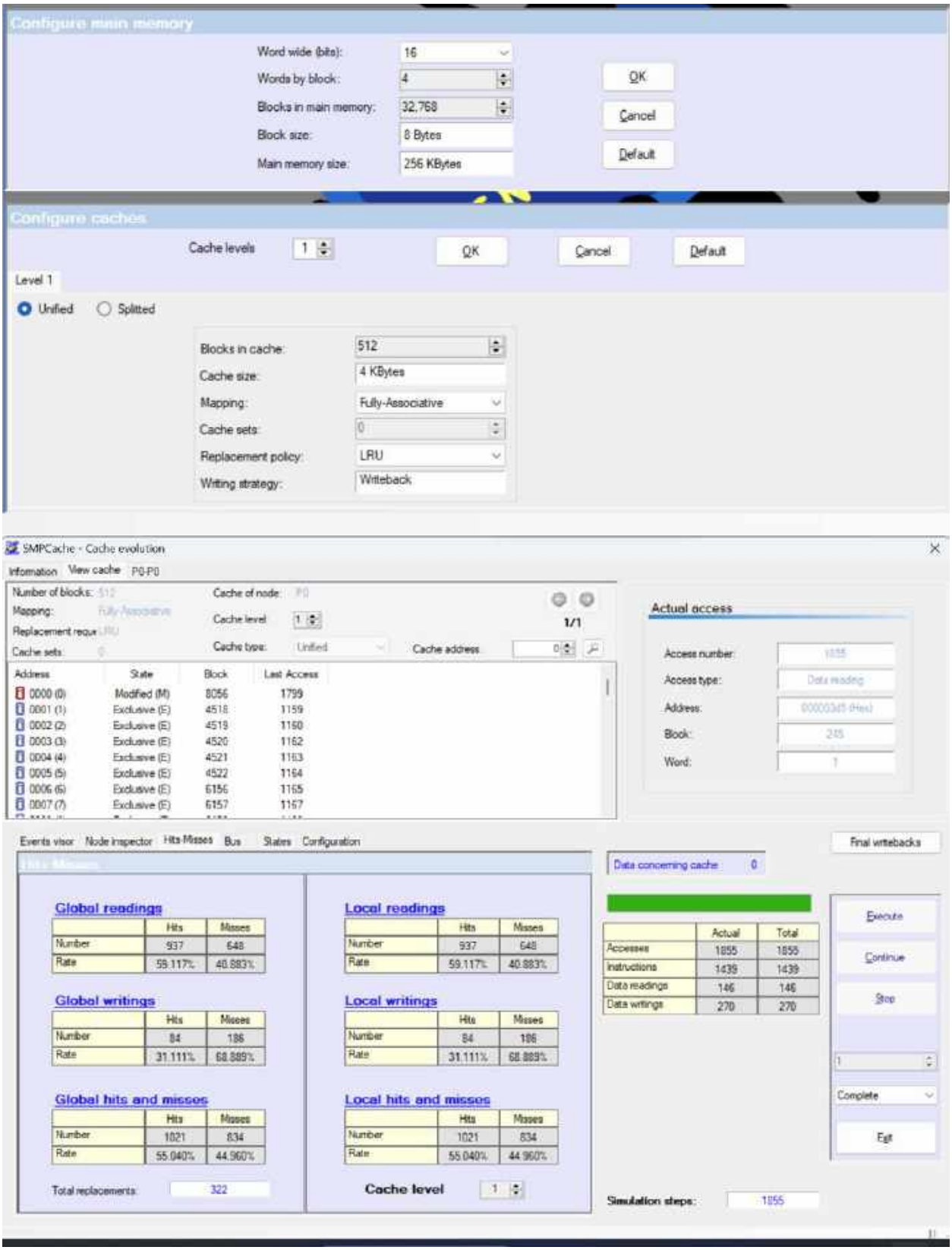
Configure main memory
Word wide (bits):
16
Words by block:
1,024
Blocks in main memory:
128
Block size:
2 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default

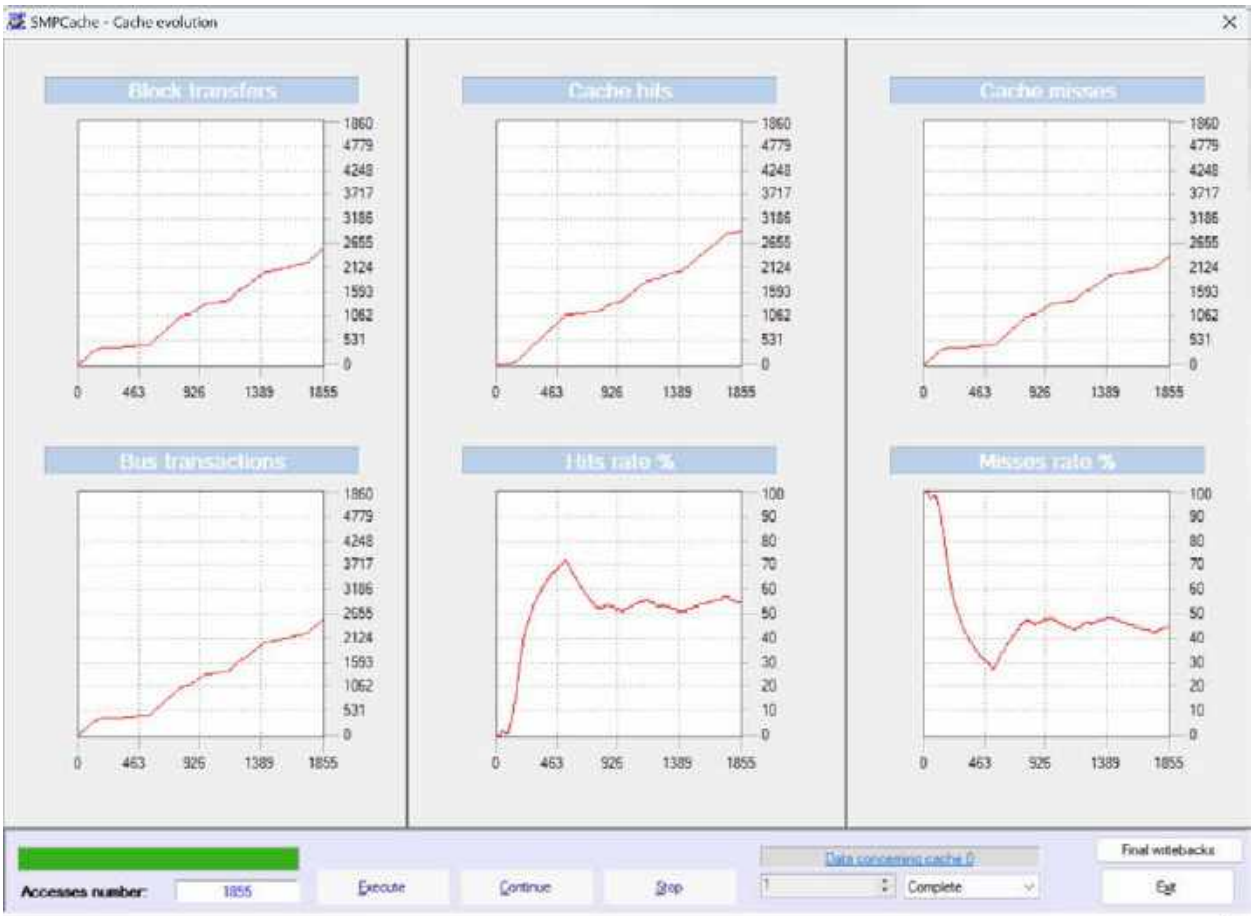

Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
2
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

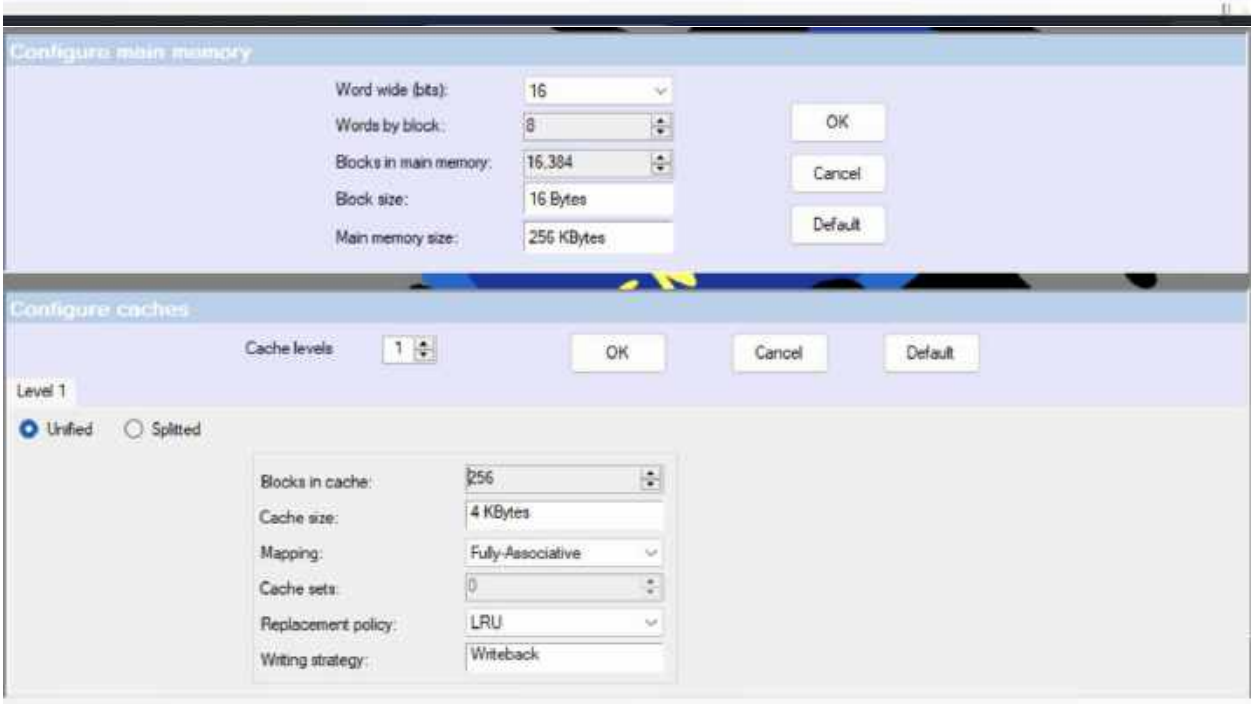

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requi
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Exclusive (E)
60
5307
0001 (1)
Exclusive (E)
9
5308
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viewr
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
4397
649
Rate
87.138%
12.862%
Local readings
Hits
Misses
Number
4397
649
Rate
87.138%
12.862%
Actual
Total
Accesses
5308
5308
Instructions
4336
4336
Data readings
711
711
Data writings
262
262
Execute
Continue
Stop
Global writings
Hits
Misses
Number
172
90
Rate
65.649%
34.351%
Local writings
Hits
Misses
Number
172
90
Rate
65.649%
34.351%
Complete
Exit
Global hits and misses
Hits
Misses
Number
4569
739
Rate
86.078%
13.922%
Local hits and misses
Hits
Misses
Number
4569
739
Rate
86.078%
13.922%
Total replacements
737
Cache level
1
Simulation steps:
5308

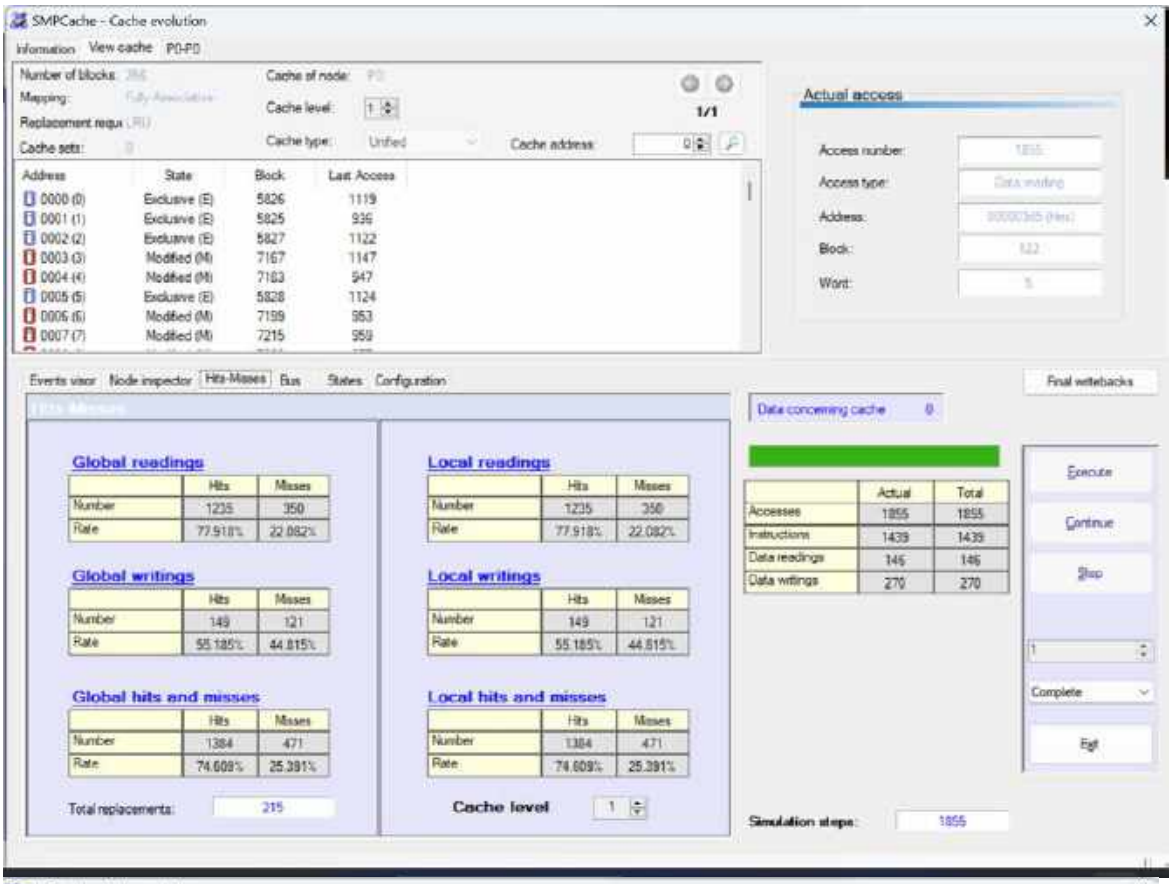

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

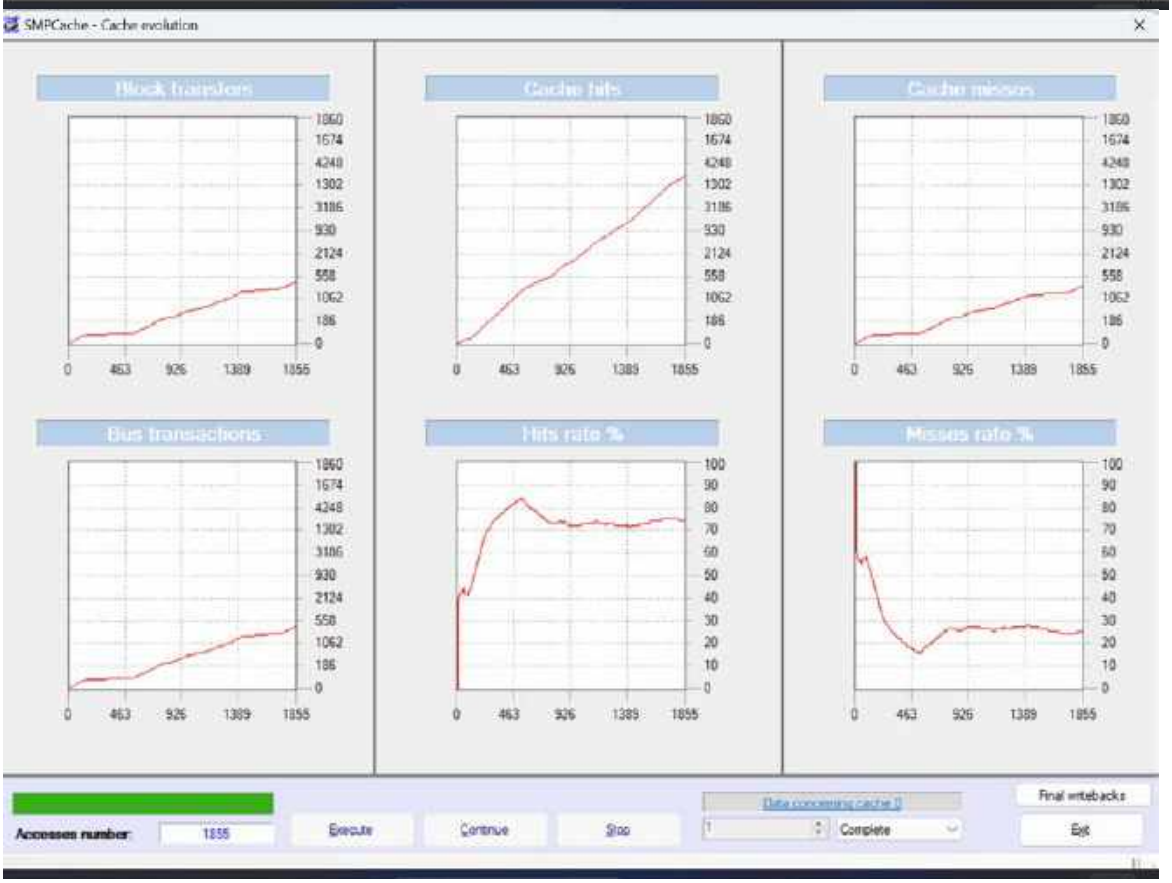
NASA7

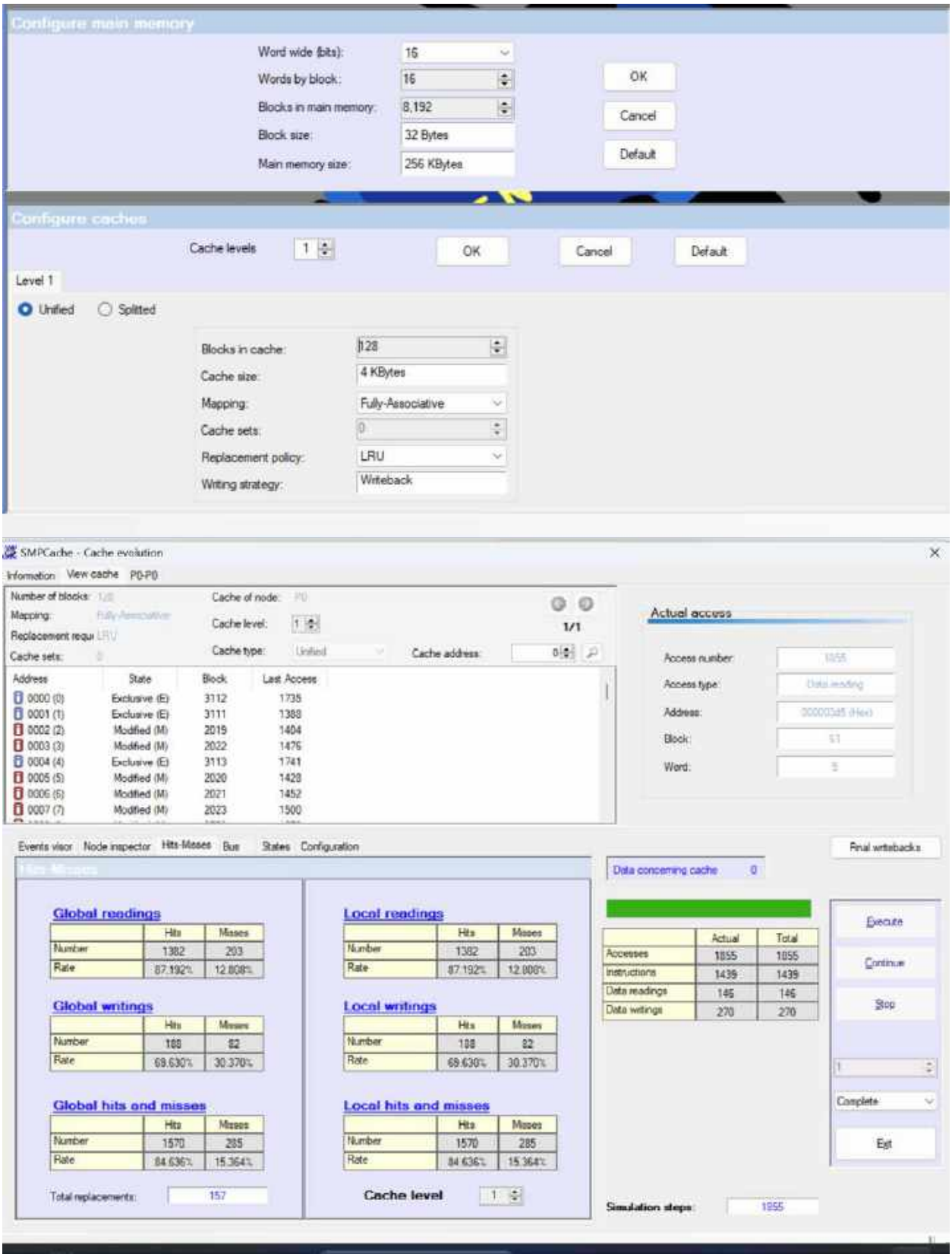

Configure main memory
Word wide (bits): 16
Words by block: 4
Blocks in main memory: 32,768
Block size: 8 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 512
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 512
Mapping: Fully-Associative
Replacement requ: LRU
Cache sets: 0
Cache of node: P0
Cache level 1
Cache type: Unified
Cache address 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 8056 1799
0001 (1) Exclusive (E) 4518 1159
0002 (2) Exclusive (E) 4519 1160
0003 (3) Exclusive (E) 4520 1162
0004 (4) Exclusive (E) 4521 1163
0005 (5) Exclusive (E) 4522 1164
0006 (6) Exclusive (E) 6156 1165
0007 (7) Exclusive (E) 6157 1167
Actual access
Access number: 1855
Access type: Data reading
Address: 00000345 (Hex)
Block: 215
Word: 1
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 937 648
Rate 59.117% 40.883%
Global writings
Hits Misses
Number 84 186
Rate 31.111% 68.889%
Global hits and misses
Hits Misses
Number 1021 834
Rate 55.040% 44.960%
Total replacements: 322
Local readings
Hits Misses
Number 937 648
Rate 59.117% 40.883%
Local writings
Hits Misses
Number 84 186
Rate 31.111% 68.889%
Local hits and misses
Hits Misses
Number 1021 834
Rate 55.040% 44.960%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 1855

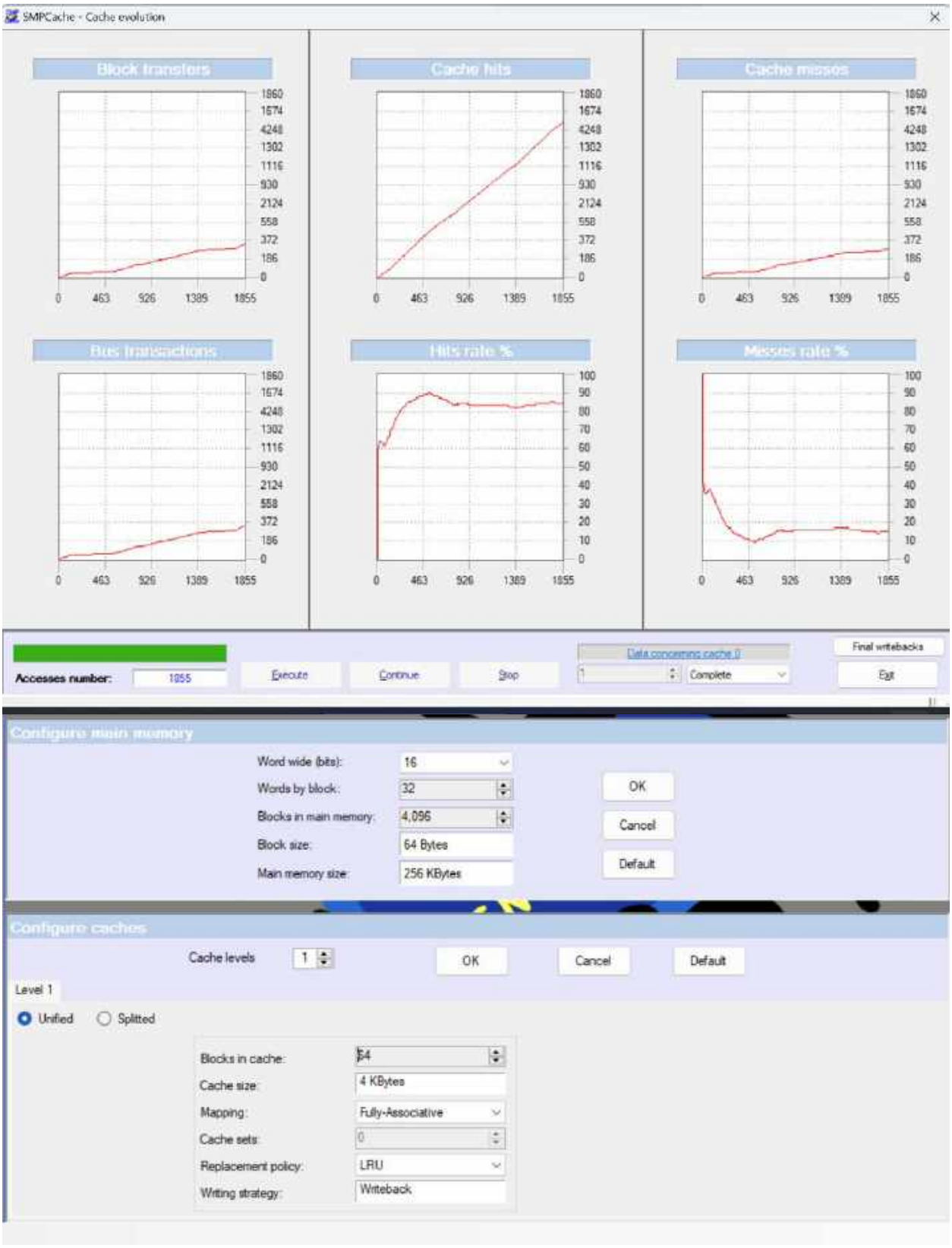

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 463 926 1389 1855
1860 4779 4248 3717 3186 2655 2124 1593 1062 531 0
100 90 80 70 60 50 40 30 20 10 0
Accesses number:
1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

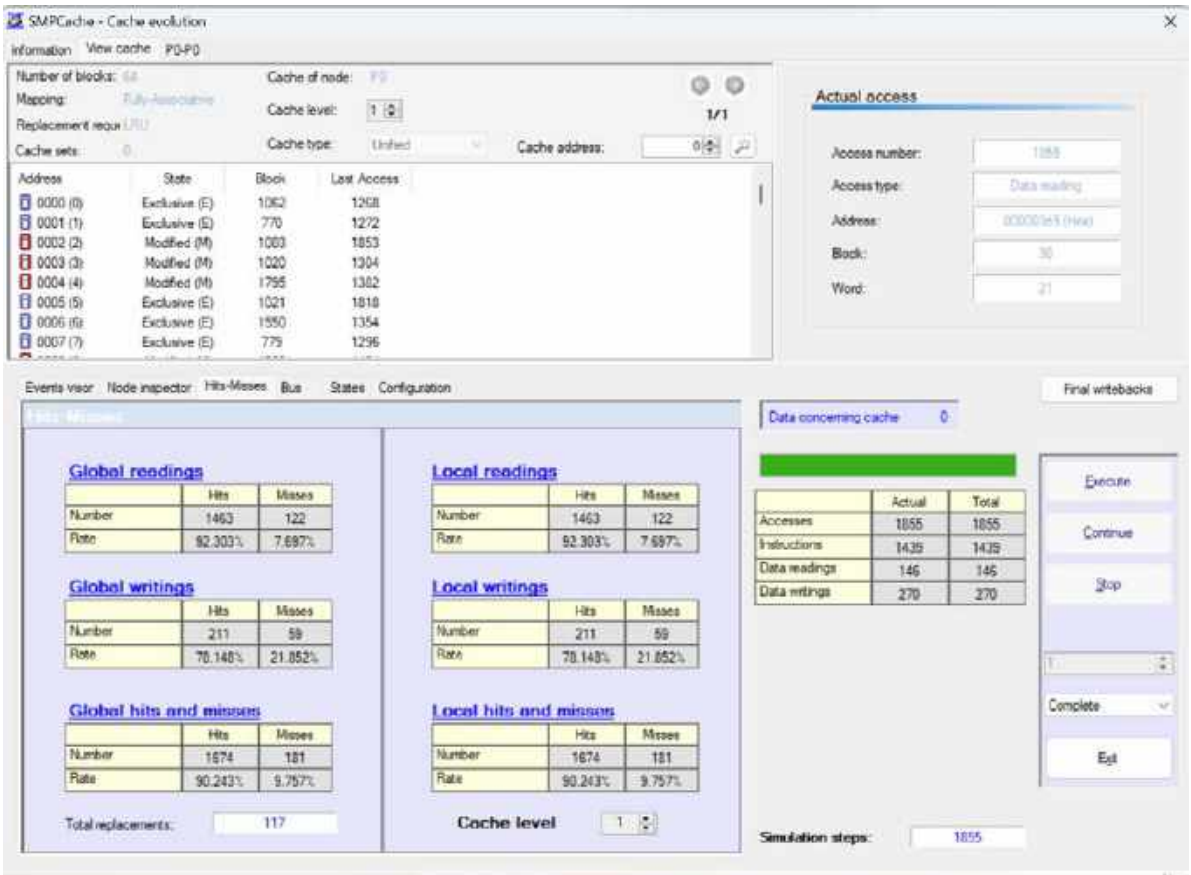

Configure main memory
Word wide (bits):
16
Words by block:
8
Blocks in main memory:
16,384
Block size:
16 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
256
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

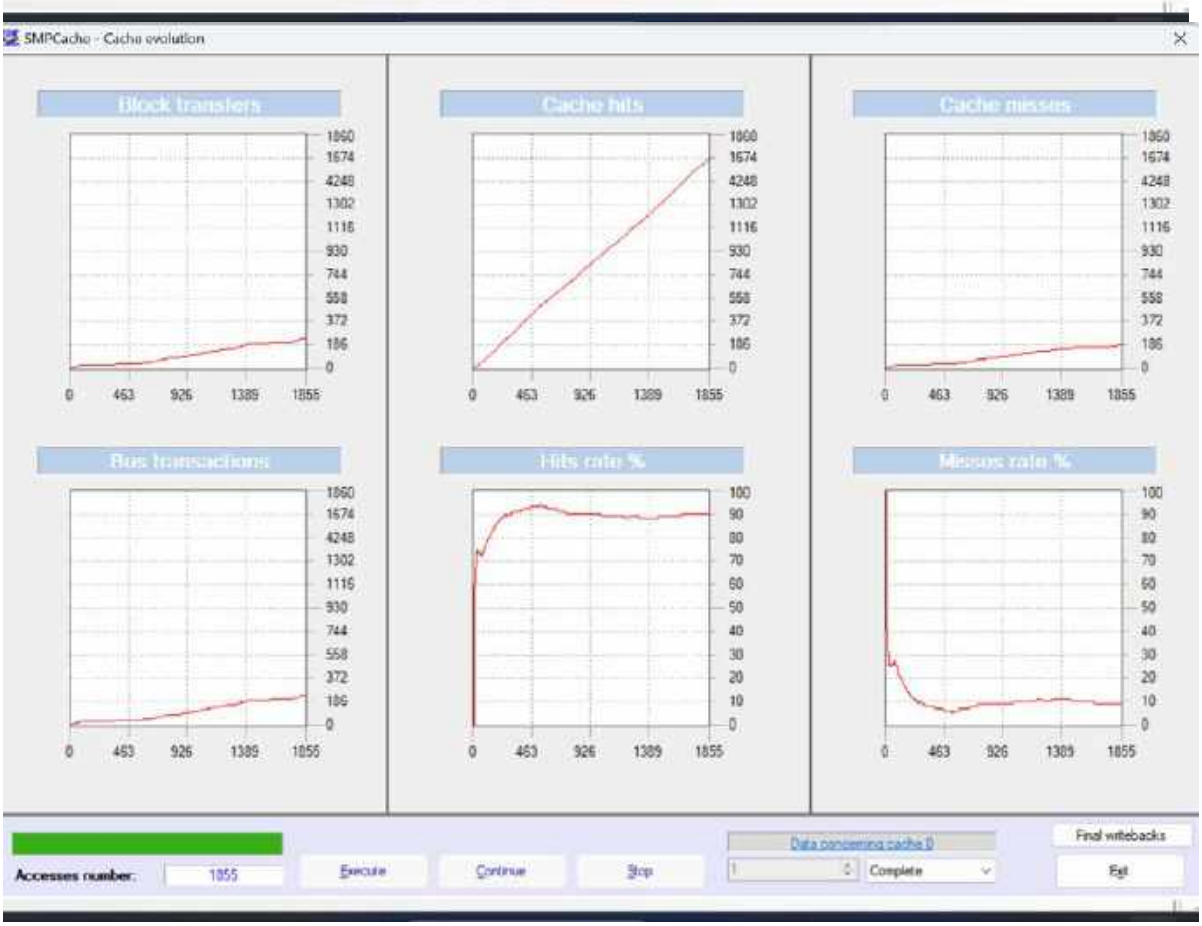

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Actual access
Access number:
Access type:
Address:
Block:
Word:
Address
State
Block
Last Access
0000 (0) Exclusive (E) 5826 1119
0001 (1) Exclusive (E) 5825 939
0002 (2) Exclusive (E) 5827 1122
0003 (3) Modified (M) 7167 1147
0004 (4) Modified (M) 7183 947
0005 (5) Exclusive (E) 5828 1124
0006 (6) Modified (M) 7199 953
0007 (7) Modified (M) 7215 959
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
Global readings
Hits
Misses
Number 1235 350
Rate 77.918% 22.082%
Global writings
Number 149 121
Rate 55.185% 44.815%
Global hits and misses
Number 1384 471
Rate 74.609% 25.391%
Total replacements: 215
Local readings
Number 1235 350
Rate 77.918% 22.082%
Local writings
Number 149 121
Rate 55.185% 44.815%
Local hits and misses
Number 1384 471
Rate 74.609% 25.391%
Cache level
Actual
Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
Complete
Exit
Simulation steps:
1855

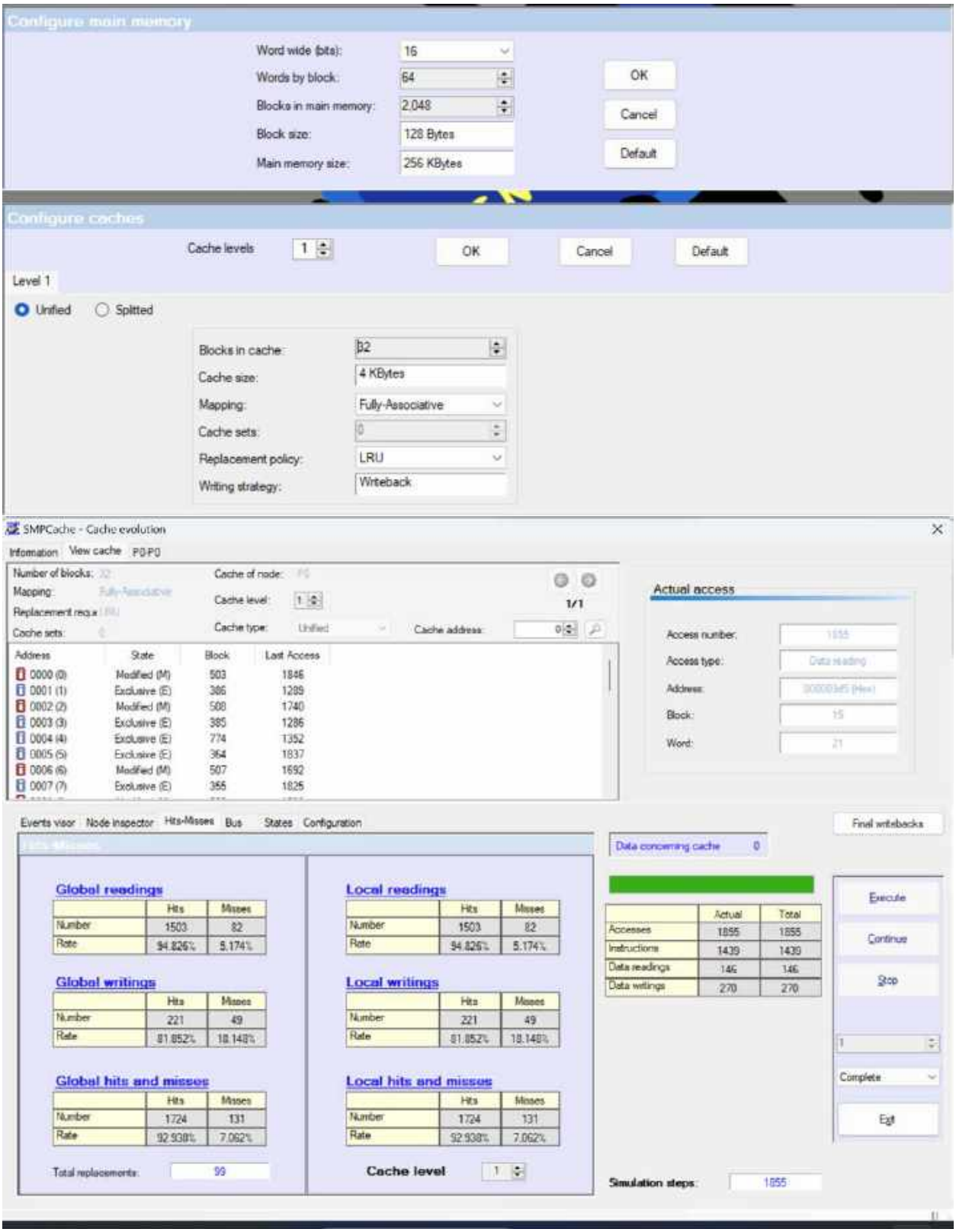

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0
463
926
1389
1855
Accesses number:
1855
Execute
Continue
Stop
Complete
Final writebacks
Exit

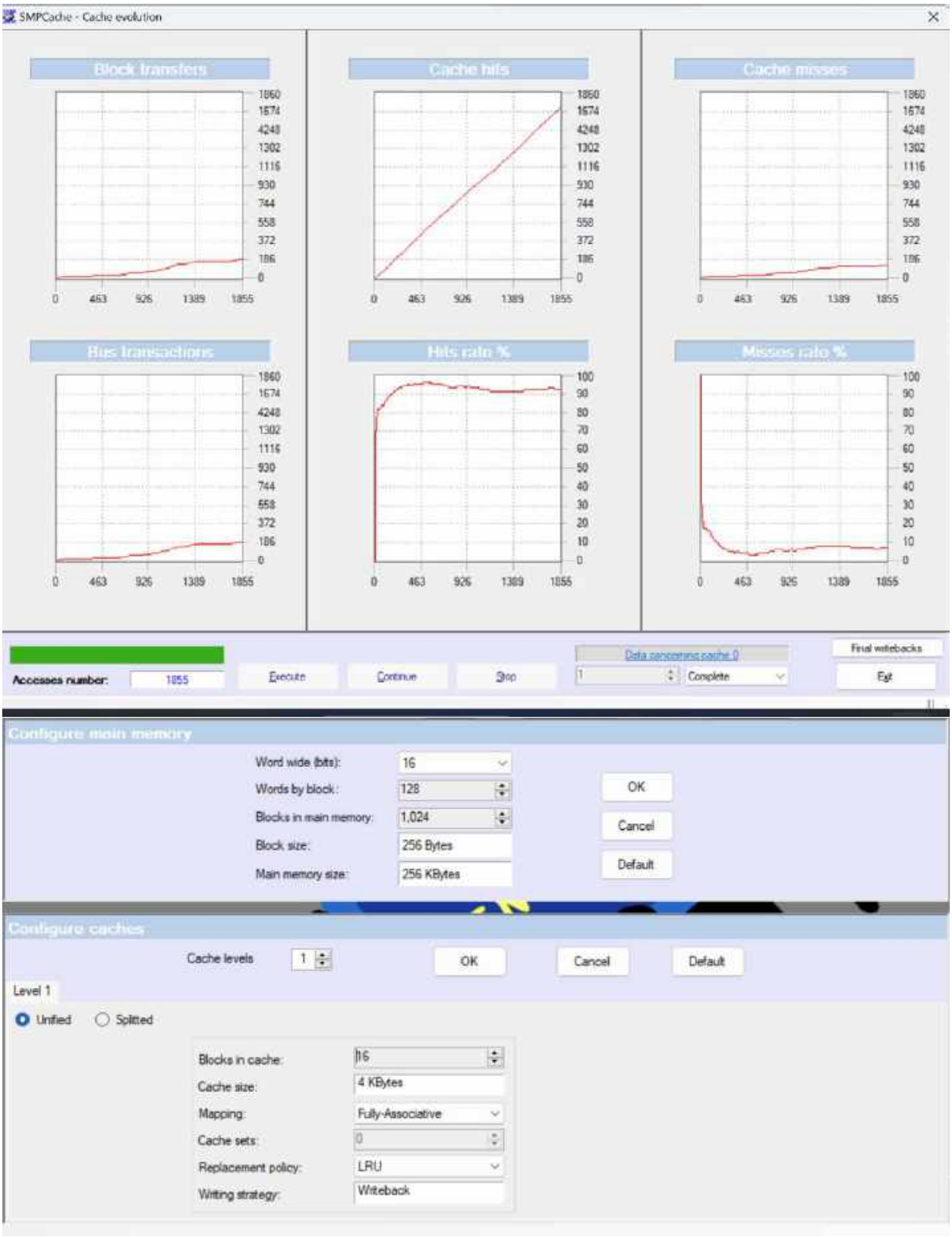

Configure main memory
Word wide (bits): 16
Words by block: 16
Blocks in main memory: 8,192
Block size: 32 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 128
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 128
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 3112 1735
0001 (1) Exclusive (E) 3111 1388
0002 (2) Modified (M) 2019 1404
0003 (3) Modified (M) 2022 1476
0004 (4) Exclusive (E) 3113 1741
0005 (5) Modified (M) 2020 1428
0006 (6) Modified (M) 2021 1452
0007 (7) Modified (M) 2023 1500
Actual access
Access number: 1855
Access type: Data reading
Address: 00000345 (Hex)
Block: 51
Word: 5
Events visor Node inspector Hits-Misses Bus States Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits Misses
Number 1382 203
Rate 87.192% 12.808%
Global writings
Hits Misses
Number 188 82
Rate 69.630% 30.370%
Global hits and misses
Hits Misses
Number 1570 285
Rate 84.636% 15.364%
Total replacements: 157
Local readings
Hits Misses
Number 1382 203
Rate 87.192% 12.808%
Local writings
Hits Misses
Number 188 82
Rate 69.630% 30.370%
Local hits and misses
Hits Misses
Number 1570 285
Rate 84.636% 15.364%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 1855

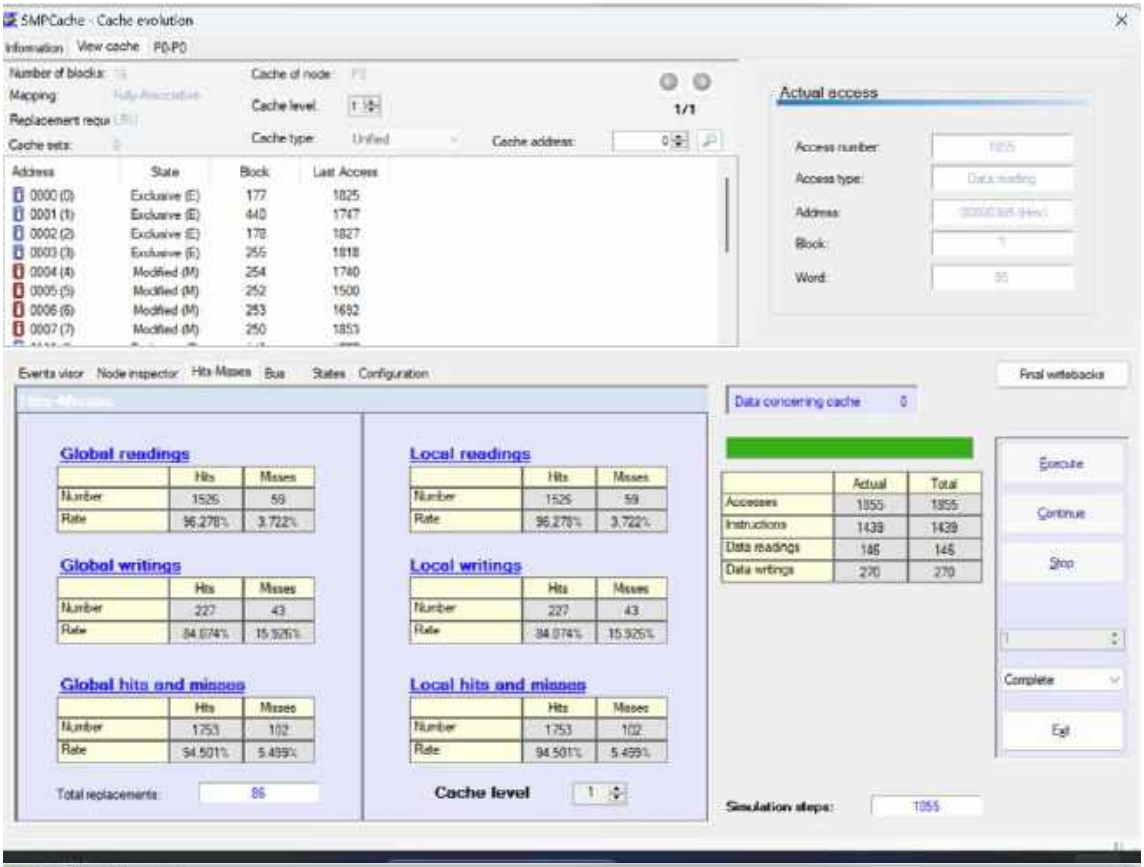

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
32
Blocks in main memory:
4,096
Block size:
64 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
64
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

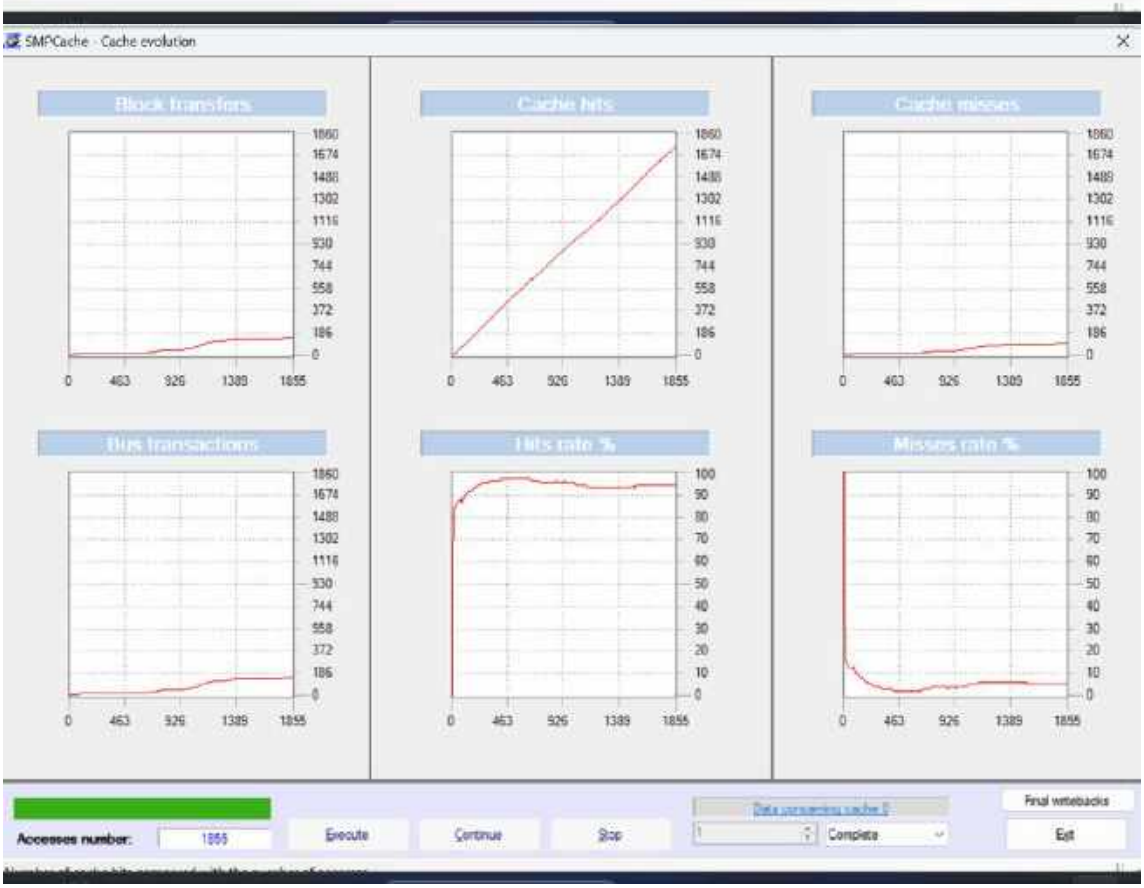

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 1062 1268
0001 (1) Exclusive (E) 770 1272
0002 (2) Modified (M) 1003 1853
0003 (3) Modified (M) 1020 1304
0004 (4) Modified (M) 1795 1302
0005 (5) Exclusive (E) 1021 1818
0006 (6) Exclusive (E) 1550 1354
0007 (7) Exclusive (E) 779 1296
Actual access
Access number:
Access type:
Data reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1463 122
Rate 92.303% 7.697%
Global writings
Hits Misses
Number 211 59
Rate 78.148% 21.852%
Global hits and misses
Hits Misses
Number 1674 181
Rate 90.243% 9.757%
Total replacements: 117
Local readings
Hits Misses
Number 1463 122
Rate 92.303% 7.697%
Local writings
Hits Misses
Number 211 59
Rate 78.148% 21.852%
Local hits and misses
Hits Misses
Number 1674 181
Rate 90.243% 9.757%
Coche level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
Complete
Exit
Simulation steps: 1855

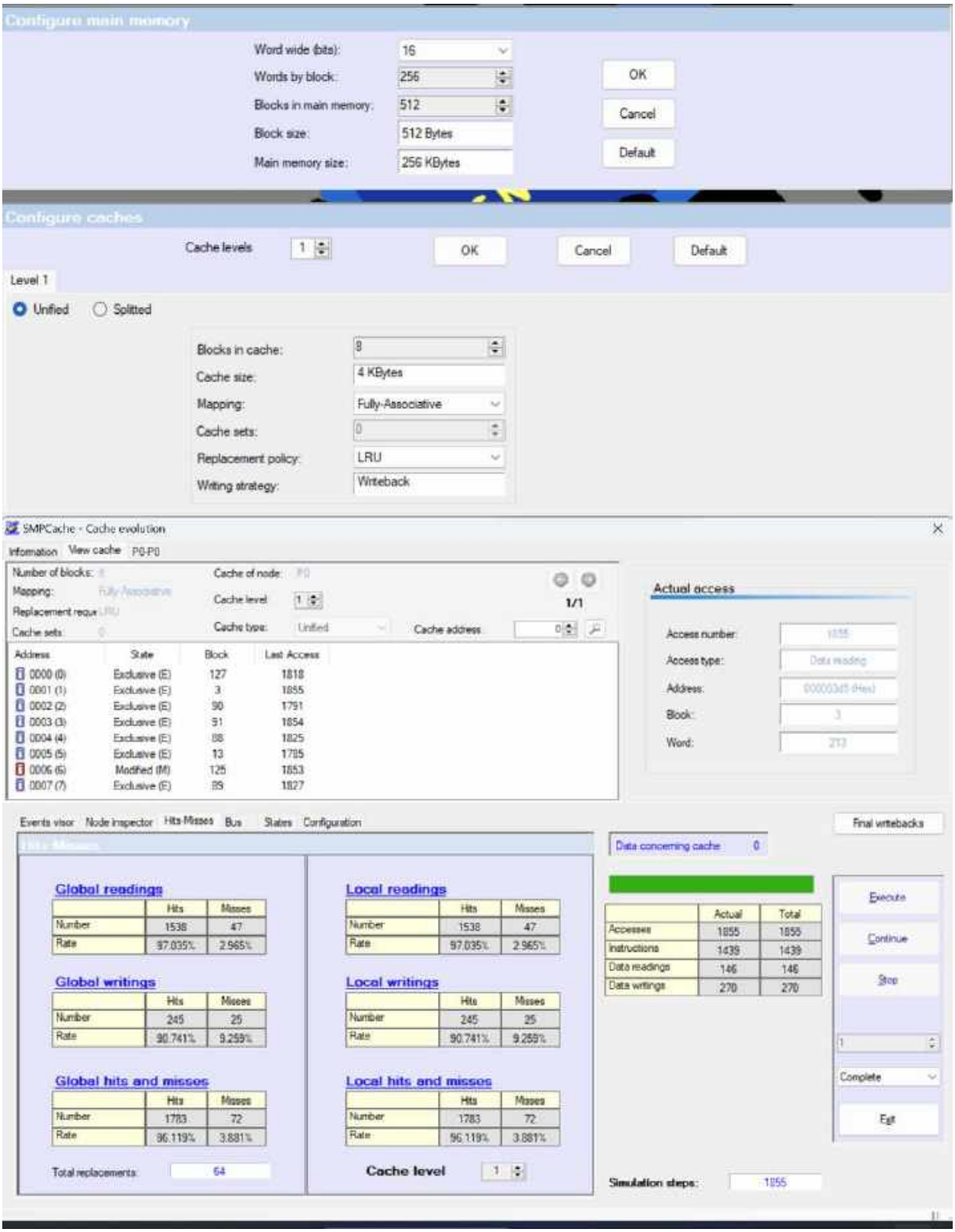

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 463 926 1389 1855
Accesses number: 1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

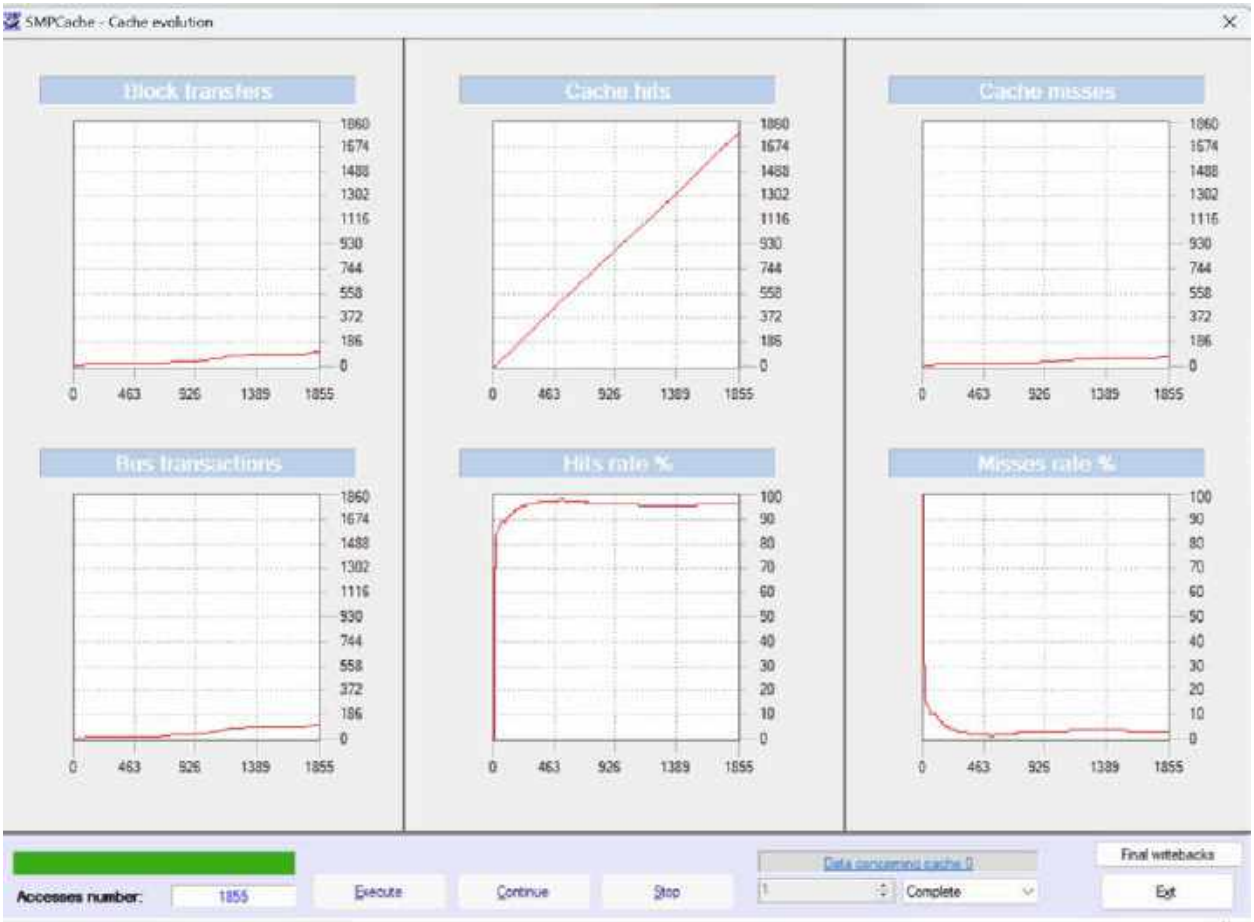

Configure main memory
Word wide (bits): 16
Words by block: 64
Blocks in main memory: 2,048
Block size: 128 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 32
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 32
Mapping: Fully-Associative
Replacement policy: LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 503 1846
0001 (1) Exclusive (E) 386 1289
0002 (2) Modified (M) 508 1740
0003 (3) Exclusive (E) 385 1286
0004 (4) Exclusive (E) 774 1352
0005 (5) Exclusive (E) 364 1837
0006 (6) Modified (M) 507 1692
0007 (7) Exclusive (E) 355 1825
Actual access
Access number: 1855
Access type: Data reading
Address: 00000bf5 (Hex)
Block: 15
Word: 21
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1503 82
Rate 94.826% 5.174%
Global writings
Hits Misses
Number 221 49
Rate 81.852% 18.148%
Global hits and misses
Hits Misses
Number 1724 131
Rate 92.938% 7.062%
Total replacements: 99
Local readings
Hits Misses
Number 1503 82
Rate 94.826% 5.174%
Local writings
Hits Misses
Number 221 49
Rate 81.852% 18.148%
Local hits and misses
Hits Misses
Number 1724 131
Rate 92.938% 7.062%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 1855


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
128
Blocks in main memory:
1,024
Block size:
256 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
16
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

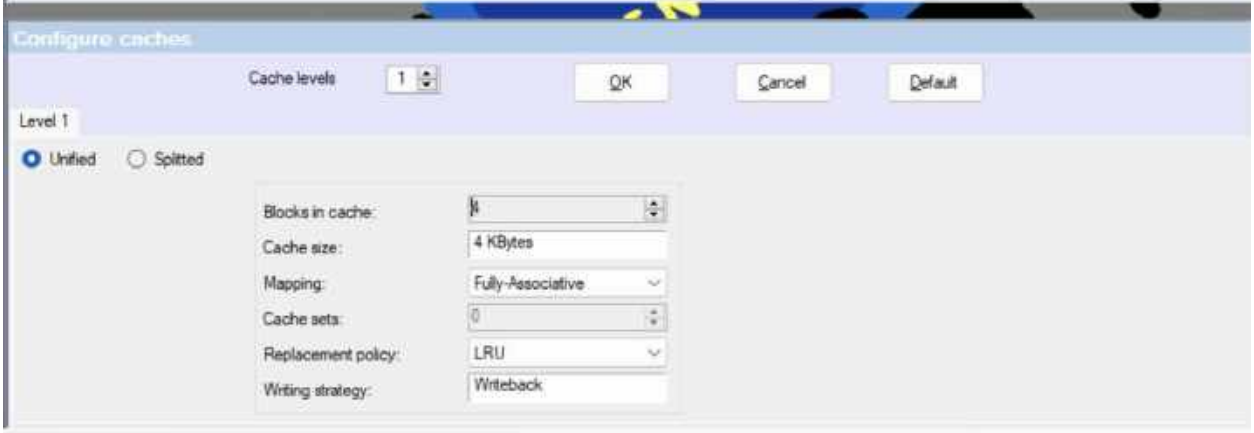

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Actual access
Access number:
Access type:
Address:
Block:
Word:
Address
State
Block
Last Access
0000 (0) Exclusive (E) 177 1825
0001 (1) Exclusive (E) 440 1747
0002 (2) Exclusive (E) 178 1827
0003 (3) Exclusive (E) 255 1818
0004 (4) Modified (M) 254 1740
0005 (5) Modified (M) 252 1500
0006 (6) Modified (M) 253 1692
0007 (7) Modified (M) 250 1853
Events visor
Node inspector
Hits Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1526 59
Rate 96.278% 3.722%
Global writings
Hits Misses
Number 227 43
Rate 84.074% 15.926%
Global hits and misses
Hits Misses
Number 1753 102
Rate 94.501% 5.499%
Total replacements: 86
Local readings
Hits Misses
Number 1526 59
Rate 96.278% 3.722%
Local writings
Hits Misses
Number 227 43
Rate 84.074% 15.926%
Local hits and misses
Hits Misses
Number 1753 102
Rate 94.501% 5.499%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
Complete
Exit
Simulation steps: 1855

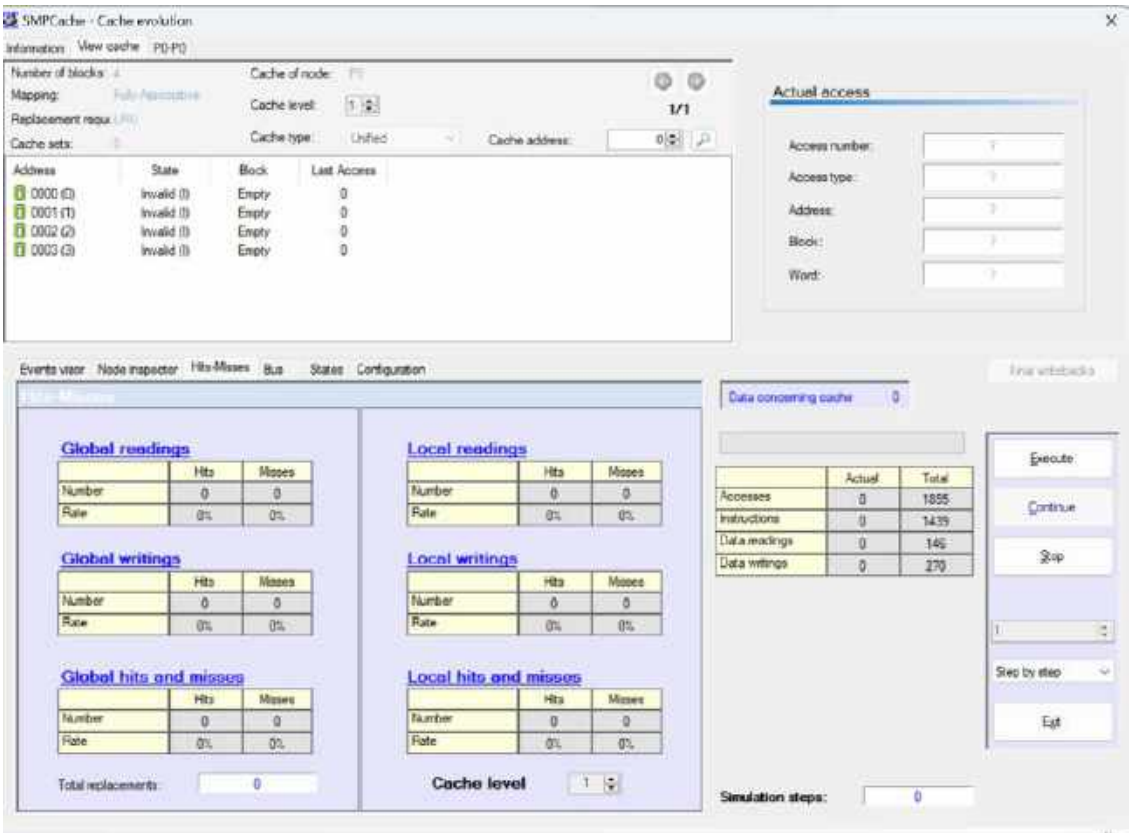

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 463 926 1389 1855
Accesses number: 1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

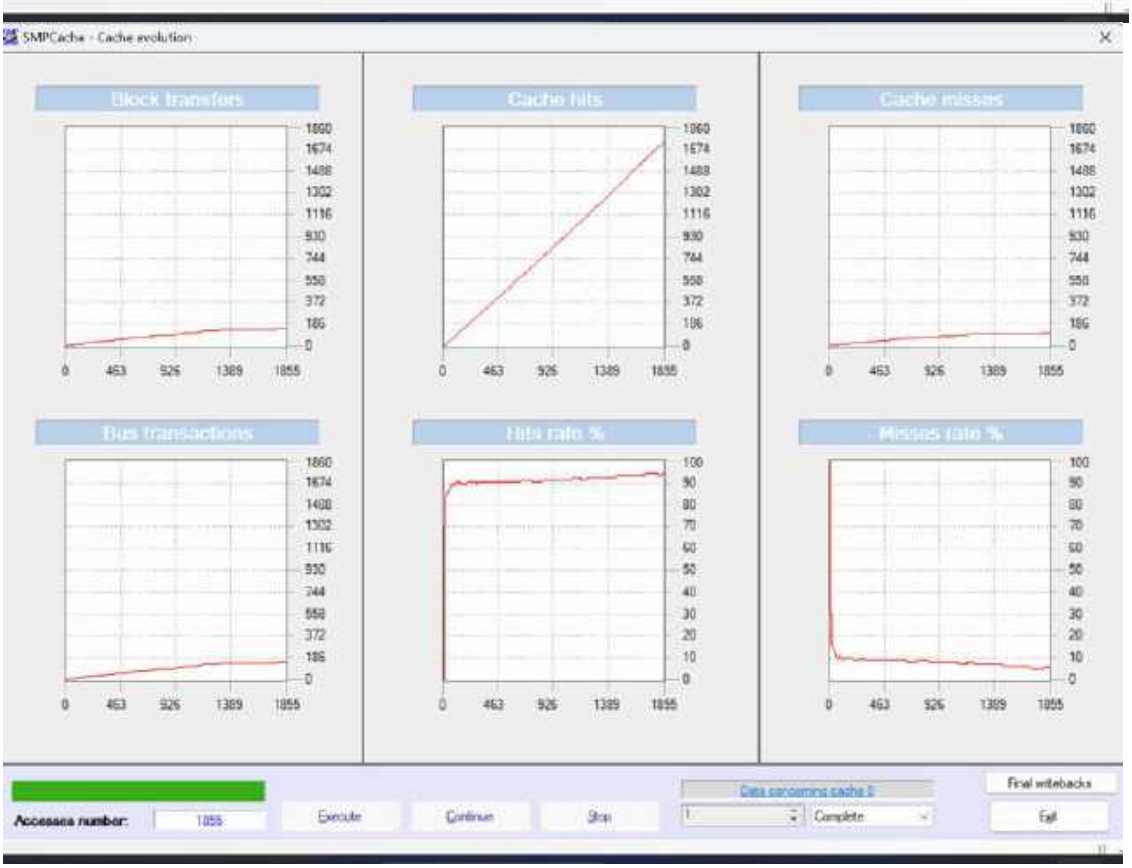

Configure main memory
Word wide (bits): 16
Words by block: 256
Blocks in main memory: 512
Block size: 512 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 8
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requir
Cache sets:
Cache of node: P0
Cache level 1
Cache type: Unified
Cache address 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 127 1818
0001 (1) Exclusive (E) 3 1855
0002 (2) Exclusive (E) 90 1791
0003 (3) Exclusive (E) 91 1854
0004 (4) Exclusive (E) 88 1825
0005 (5) Exclusive (E) 13 1715
0006 (6) Modified (M) 125 1853
0007 (7) Exclusive (E) 89 1827
Actual access
Access number: 1855
Access type: Data reading
Address: 000003d5 (Hex)
Block: 3
Word: 213
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1538 47
Rate 97.035% 2.965%
Global writings
Hits Misses
Number 245 25
Rate 90.741% 9.259%
Global hits and misses
Hits Misses
Number 1783 72
Rate 96.119% 3.881%
Total replacements: 64
Local readings
Hits Misses
Number 1538 47
Rate 97.035% 2.965%
Local writings
Hits Misses
Number 245 25
Rate 90.741% 9.259%
Local hits and misses
Hits Misses
Number 1783 72
Rate 96.119% 3.881%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 1855

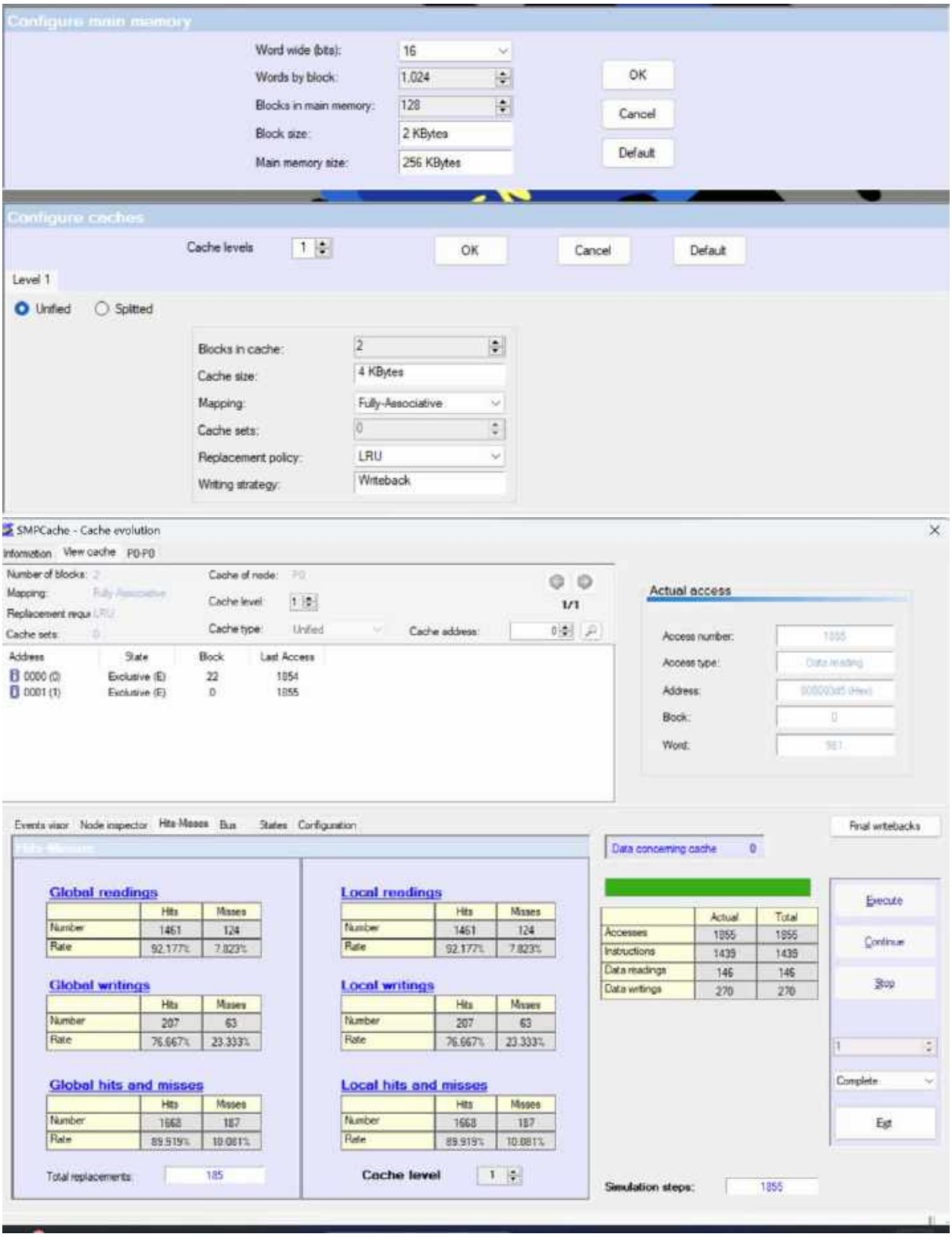

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
1855
Execute
Continue
Stop
Complete
Final writebacks
Exit

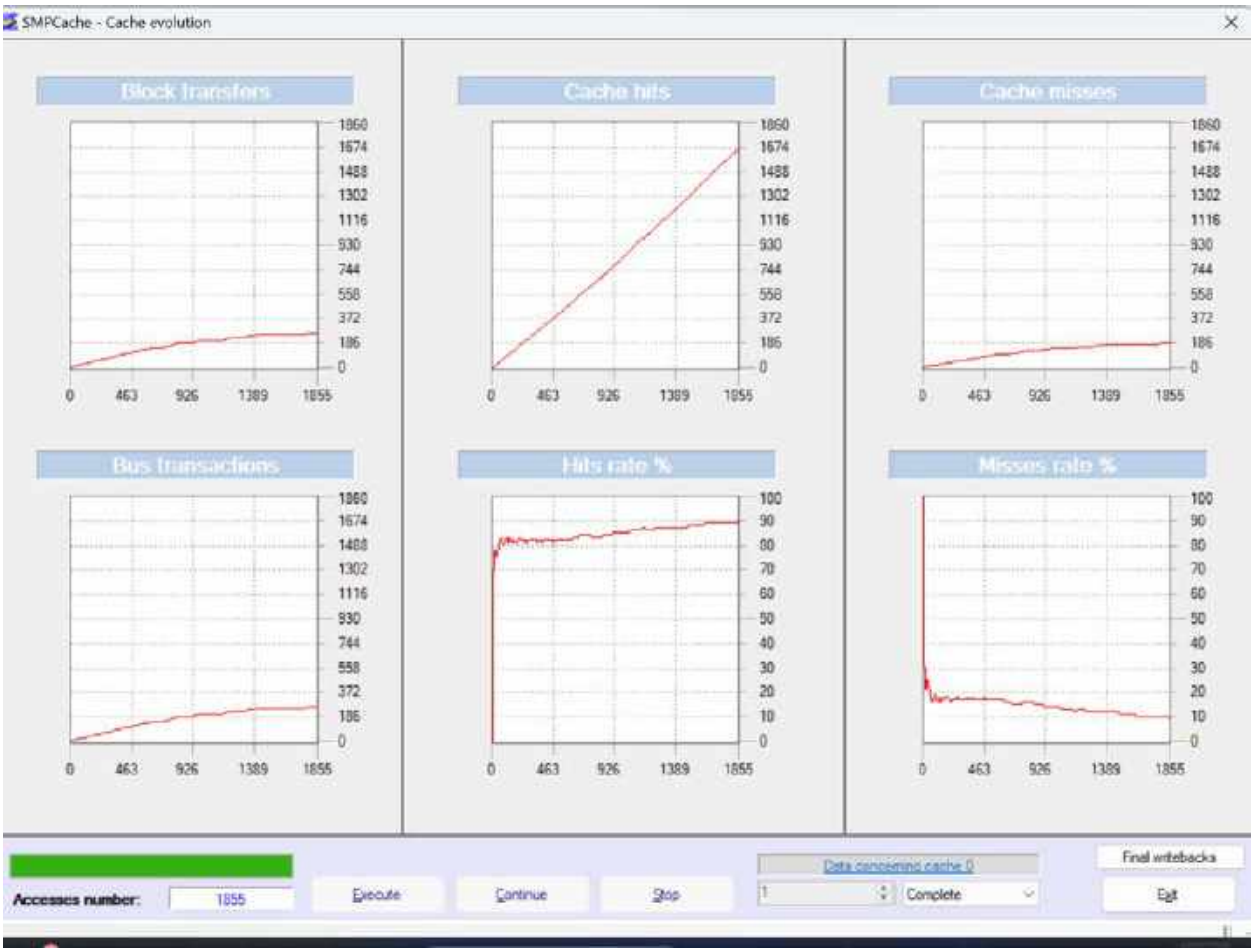
Configure main memory
Word wide (bits):
16
Words by block:
512
Blocks in main memory:
256
Block size:
1 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default


Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
4
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

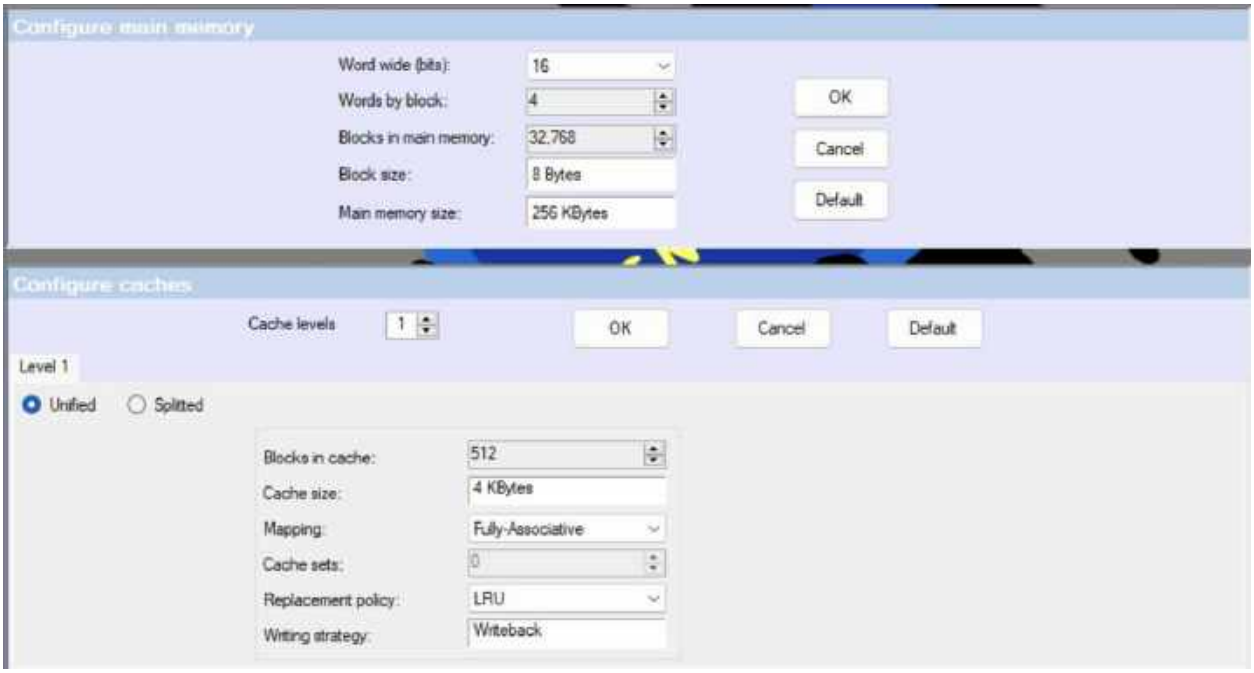

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
0001 (1)
0002 (2)
0003 (3)
Invalid (I)
Empty
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viewr
Node inspector
Hits-Misses
Bus
States
Configuration
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Hits
Misses
Number
Rate
Total replacements:
Cache level
Data concerning cache
Actual
Total
Accesses
Instructions
Data readings
Data writings
Execute
Continue
Stop
Step by step
Exit
Simulation steps:

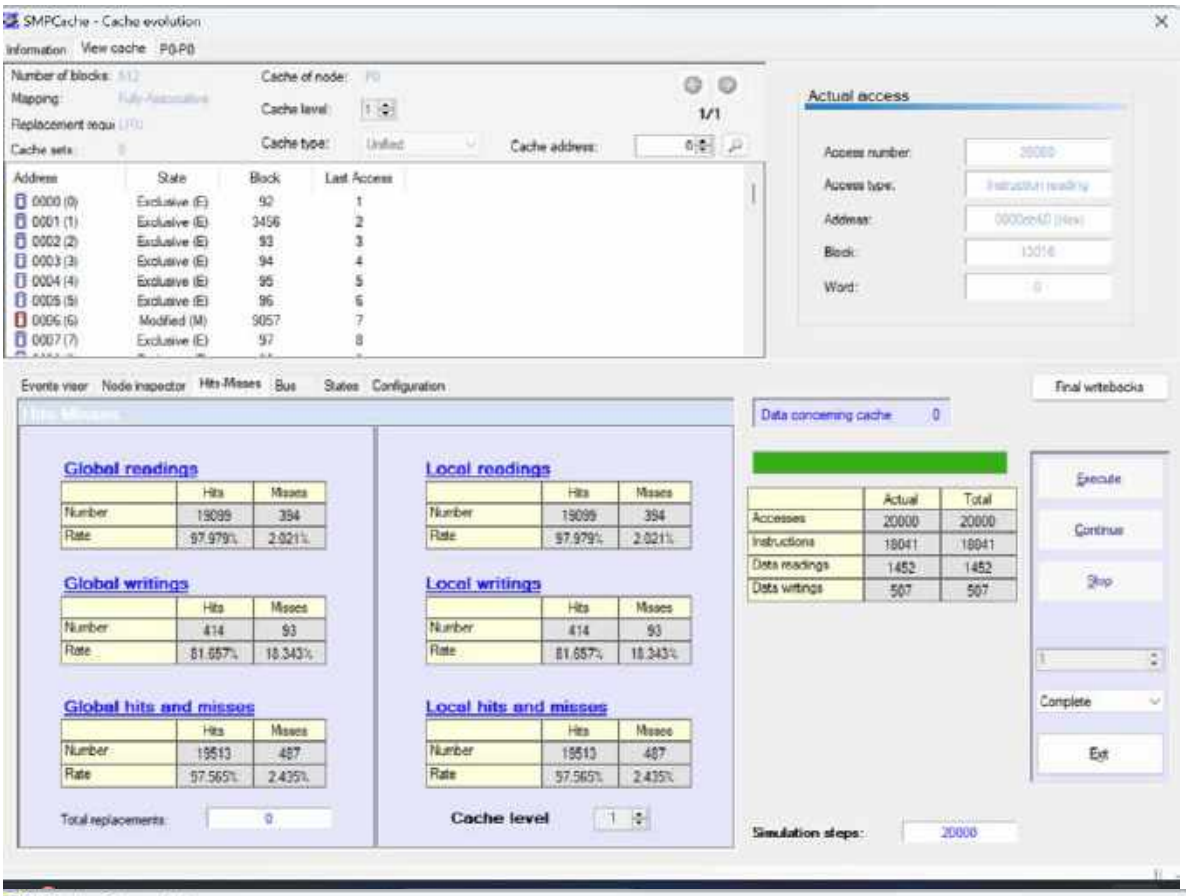

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
Execute
Continue
Stop
Complete
Final writebacks
Exit

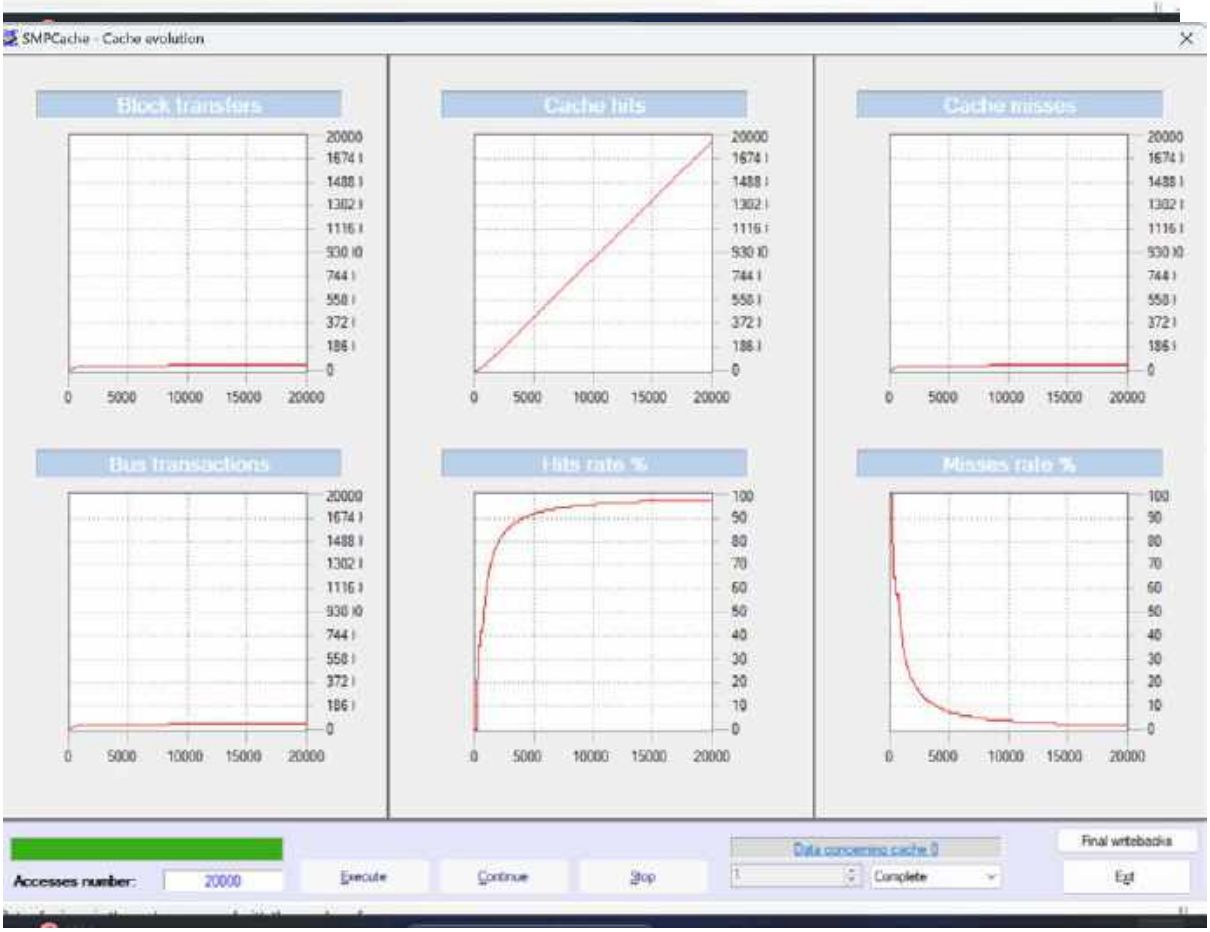

Configure main memory
Word wide (bits): 16
Words by block: 1,024
Blocks in main memory: 128
Block size: 2 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 2
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 2
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 22 1854
0001 (1) Exclusive (E) 0 1855
Actual access
Access number: 1855
Access type: Data reading
Address: 00000305 (Hex)
Block: 0
Word: 961
Events viewr
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1461 124
Rate 92.177% 7.823%
Global writings
Hits Misses
Number 207 63
Rate 76.667% 23.333%
Global hits and misses
Hits Misses
Number 1668 187
Rate 89.919% 10.081%
Total replacements: 185
Local readings
Hits Misses
Number 1461 124
Rate 92.177% 7.823%
Local writings
Hits Misses
Number 207 63
Rate 76.667% 23.333%
Local hits and misses
Hits Misses
Number 1668 187
Rate 89.919% 10.081%
Cache level 1
Actual Total
Accesses 1855 1855
Instructions 1439 1439
Data readings 146 146
Data writings 270 270
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 1855

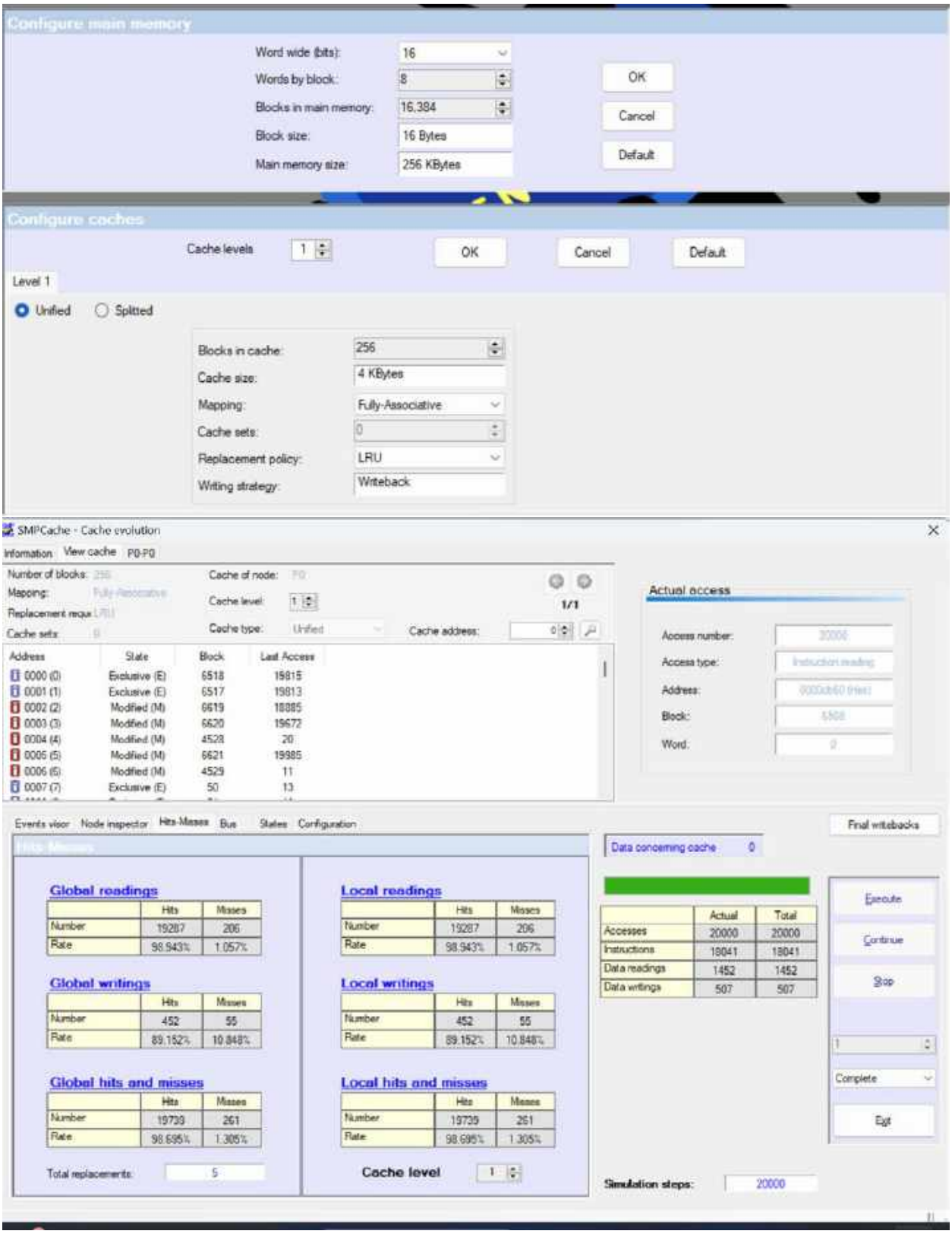

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
1855
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

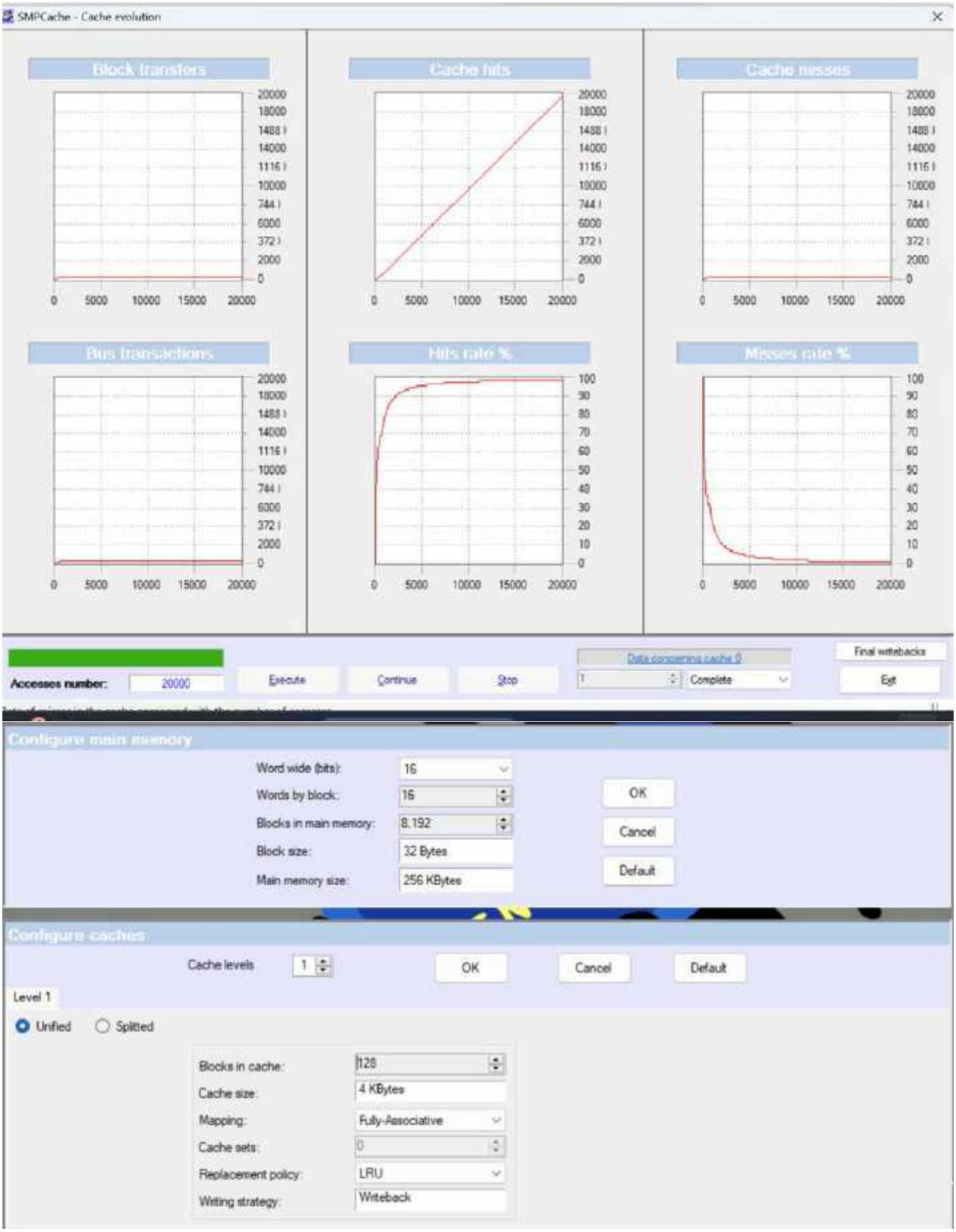
CEXP

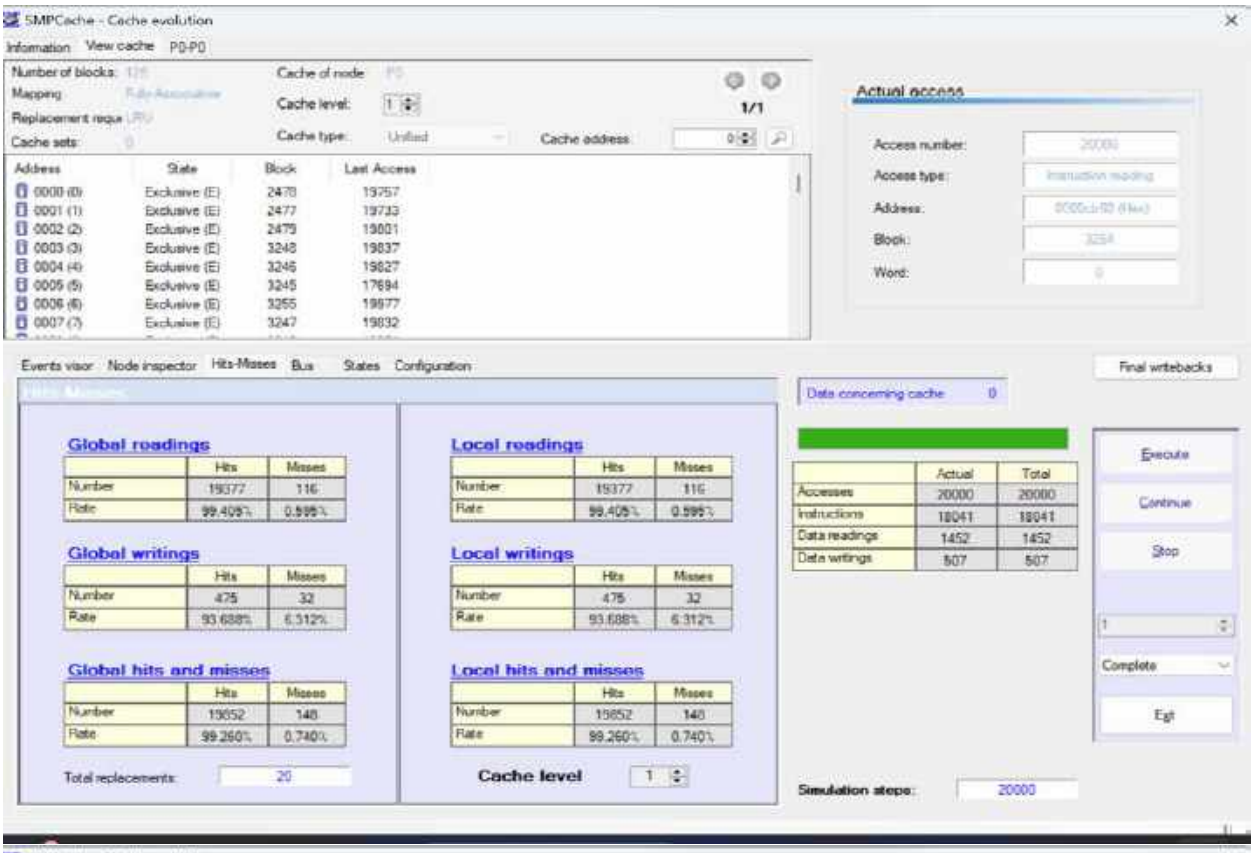

Configure main memory
Word wide (bits):
16
Words by block:
4
Blocks in main memory:
32,768
Block size:
8 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
512
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

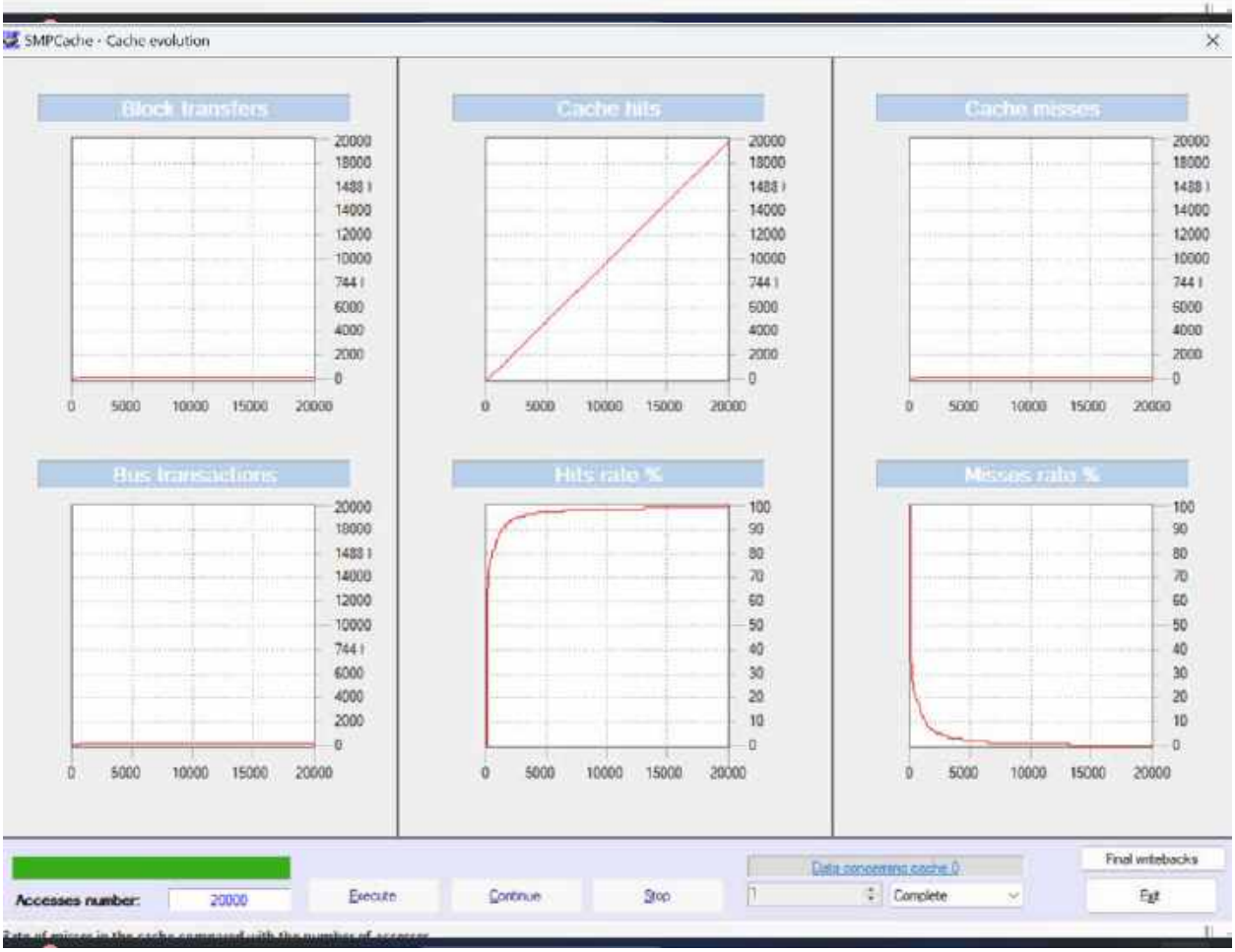

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 92 1
0001 (1) Exclusive (E) 3456 2
0002 (2) Exclusive (E) 93 3
0003 (3) Exclusive (E) 94 4
0004 (4) Exclusive (E) 95 5
0005 (5) Exclusive (E) 96 6
0006 (6) Modified (M) 9057 7
0007 (7) Exclusive (E) 97 8
Actual access
Access number:
Access type:
Address:
Block:
Word:
Evente visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 19099 394
Rate 97.979% 2.021%
Global writings
Hits Misses
Number 414 93
Rate 81.657% 18.343%
Global hits and misses
Hits Misses
Number 19513 487
Rate 97.565% 2.435%
Total replacements: 0
Local readings
Hits Misses
Number 19099 394
Rate 97.979% 2.021%
Local writings
Hits Misses
Number 414 93
Rate 81.657% 18.343%
Local hits and misses
Hits Misses
Number 19513 487
Rate 97.565% 2.435%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000

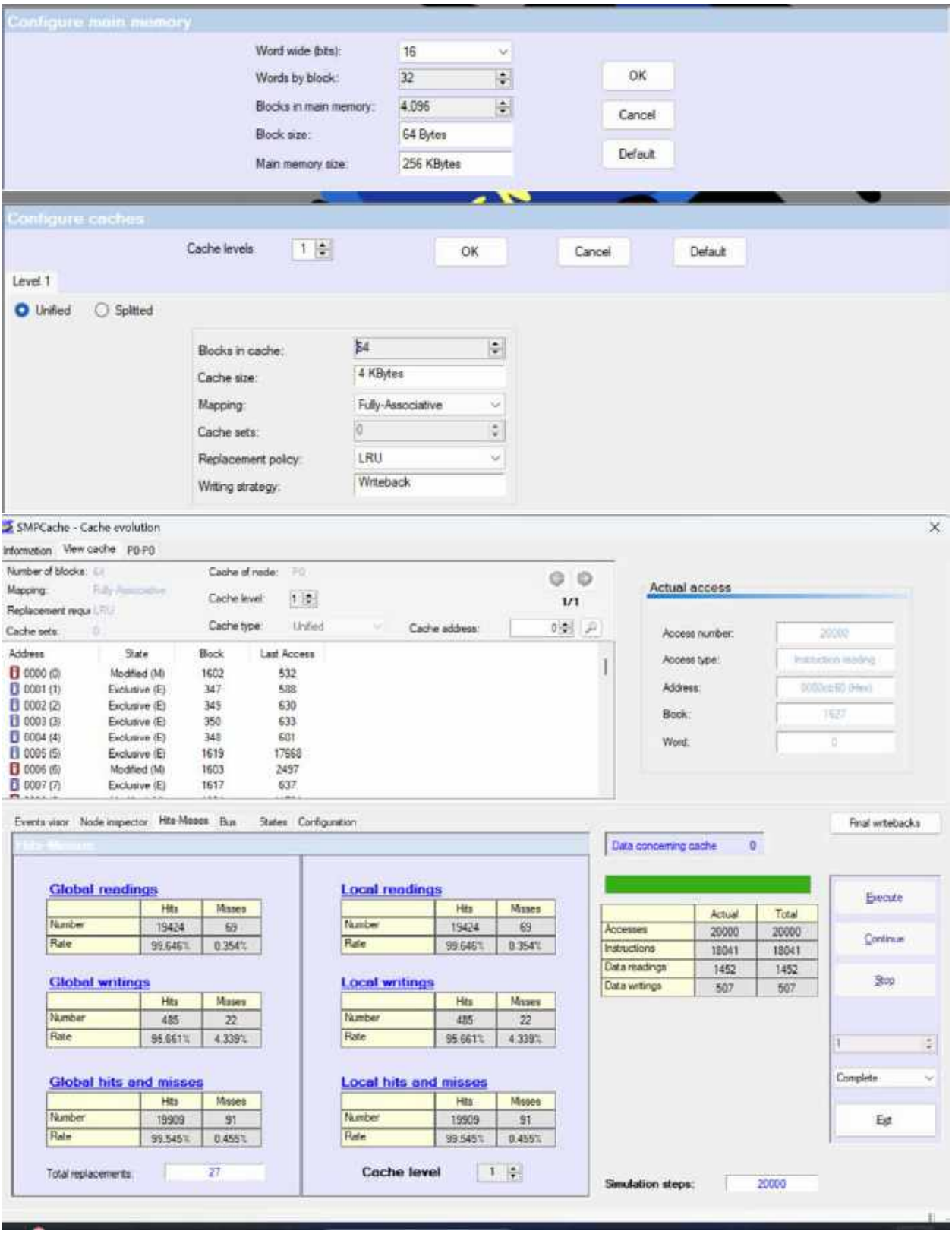

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 5000 10000 15000 20000
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

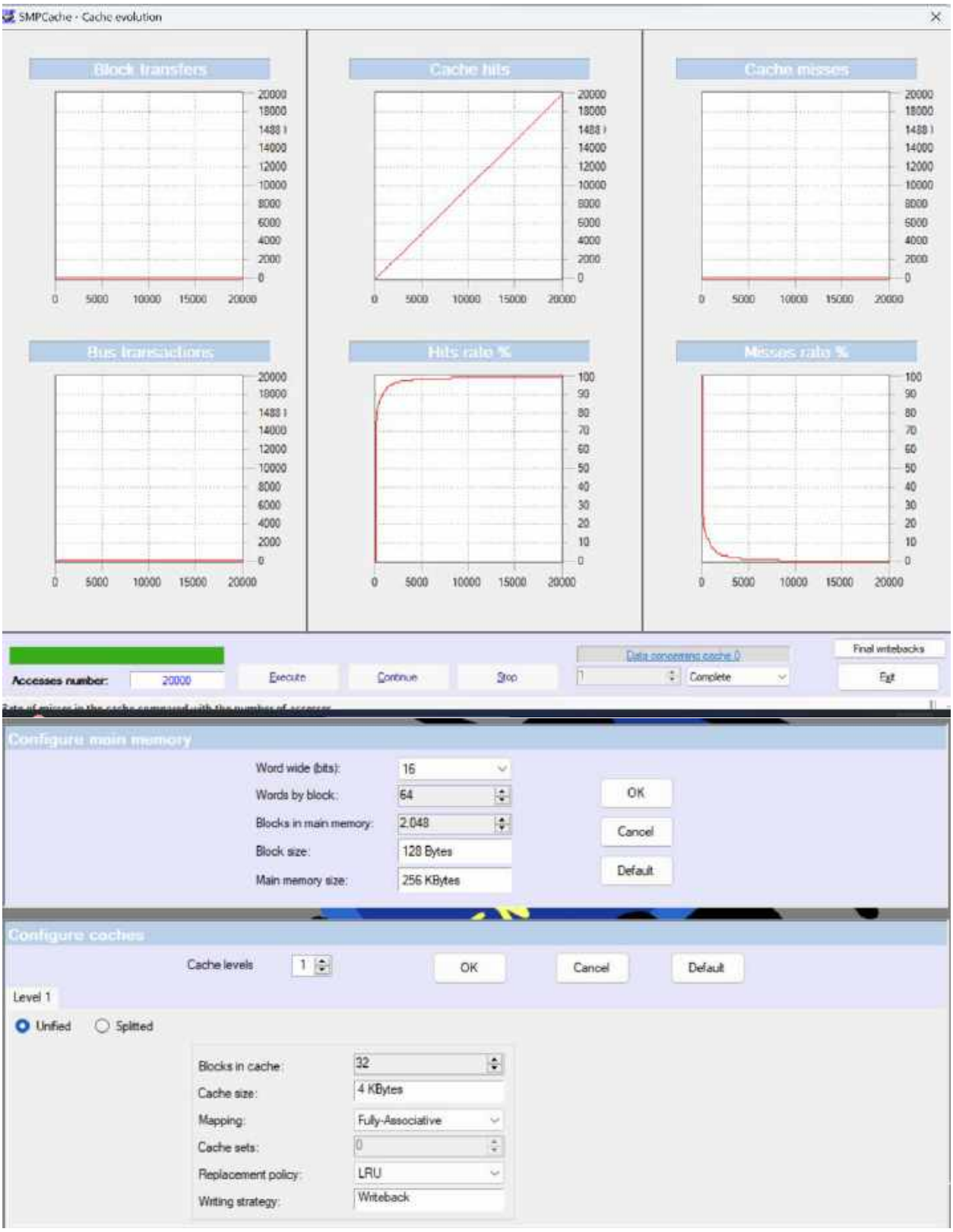

Configure main memory
Word wide (bits): 16
Words by block: 8
Blocks in main memory: 16,384
Block size: 16 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 256
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 6518 19815
0001 (1) Exclusive (E) 6517 19813
0002 (2) Modified (M) 6619 18885
0003 (3) Modified (M) 6620 19672
0004 (4) Modified (M) 4528 20
0005 (5) Modified (M) 6621 19985
0006 (6) Modified (M) 4529 11
0007 (7) Exclusive (E) 50 13
Actual access
Access number: 20000
Access type: Instruction reading
Address:
Block:
Word: 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 19287 206
Rate 98.943% 1.057%
Global writings
Hits Misses
Number 452 55
Rate 89.152% 10.848%
Global hits and misses
Hits Misses
Number 19739 261
Rate 98.695% 1.305%
Total replacements: 5
Local readings
Hits Misses
Number 19287 206
Rate 98.943% 1.057%
Local writings
Hits Misses
Number 452 55
Rate 89.152% 10.848%
Local hits and misses
Hits Misses
Number 19739 261
Rate 98.695% 1.305%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

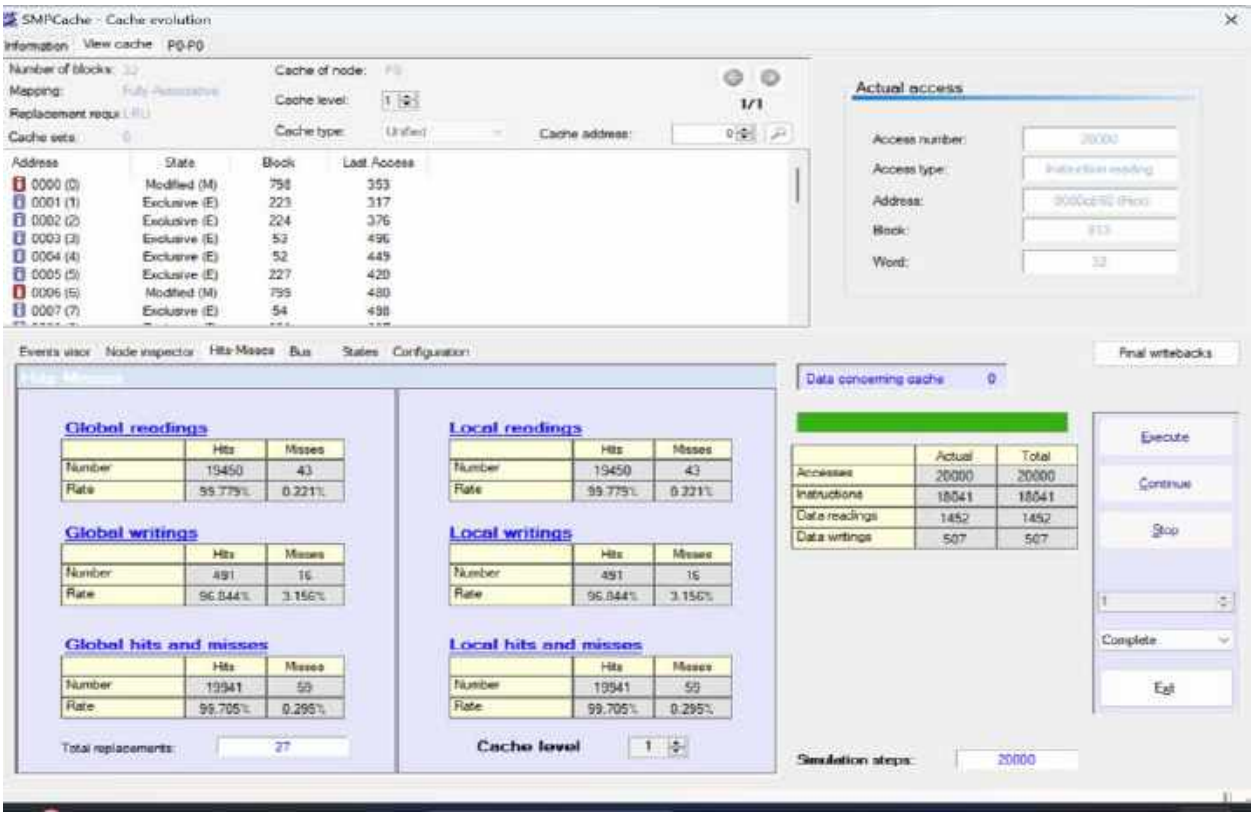

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8.192
Block size:
32 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

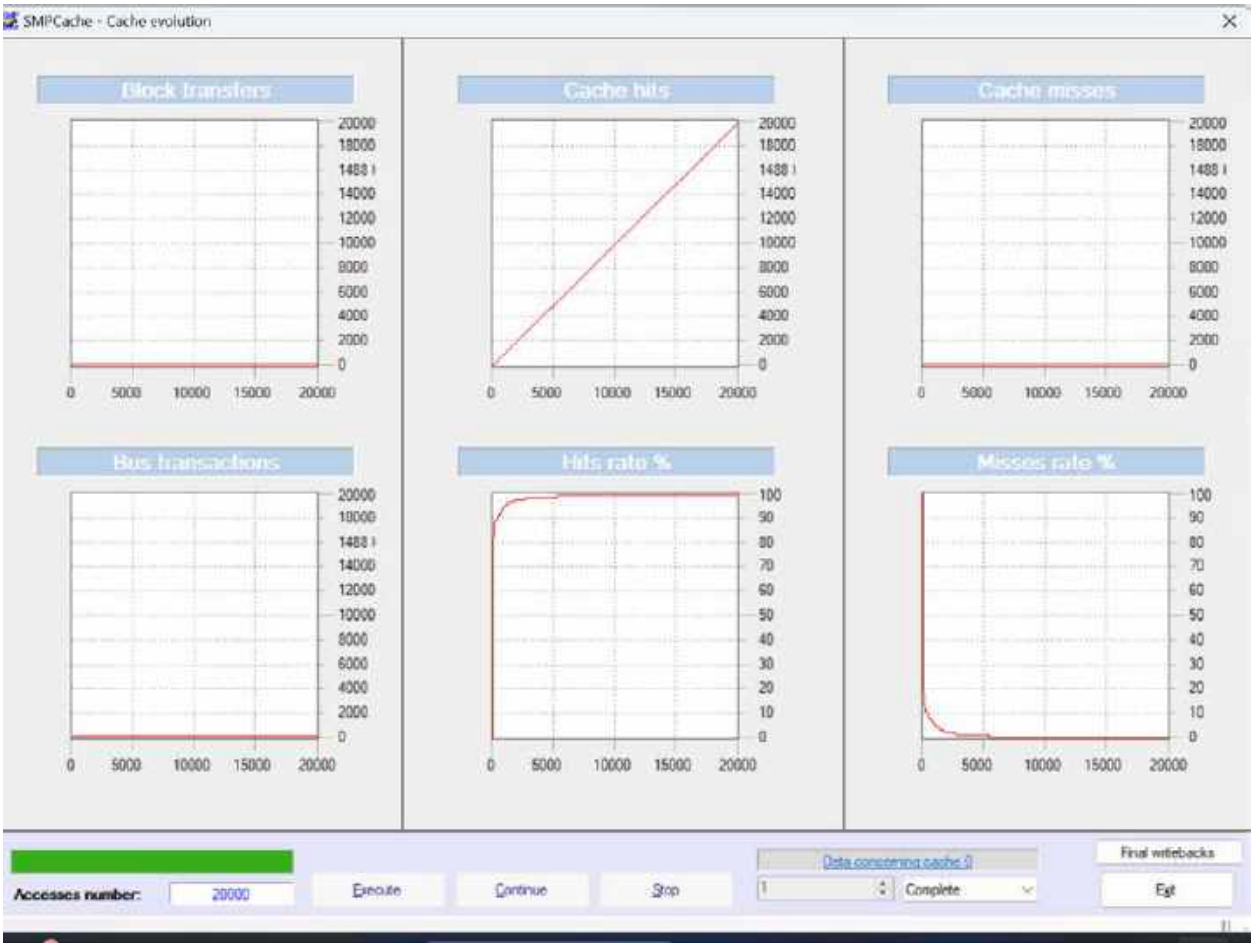

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node
Cache level:
Cache type:
Unified
Cache address
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 2478 19757
0001 (1) Exclusive (E) 2477 19733
0002 (2) Exclusive (E) 2479 19801
0003 (3) Exclusive (E) 3248 19837
0004 (4) Exclusive (E) 3246 19827
0005 (5) Exclusive (E) 3245 17694
0006 (6) Exclusive (E) 3255 19877
0007 (7) Exclusive (E) 3247 19832
Actual access
Access number:
Access type:
Instruction reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Global readings
Hits
Misses
Number 19377 116
Rate 99.405% 0.595%
Local readings
Number 19377 116
Rate 99.405% 0.595%
Data concerning cache 0
Actual
Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
Complete
Exit
Global writings
Number 475 32
Rate 93.688% 6.312%
Local writings
Number 475 32
Rate 93.688% 6.312%
Global hits and misses
Number 19852 148
Rate 99.260% 0.740%
Local hits and misses
Number 19852 148
Rate 99.260% 0.740%
Total replacements: 20
Cache level
Simulation steps: 20000

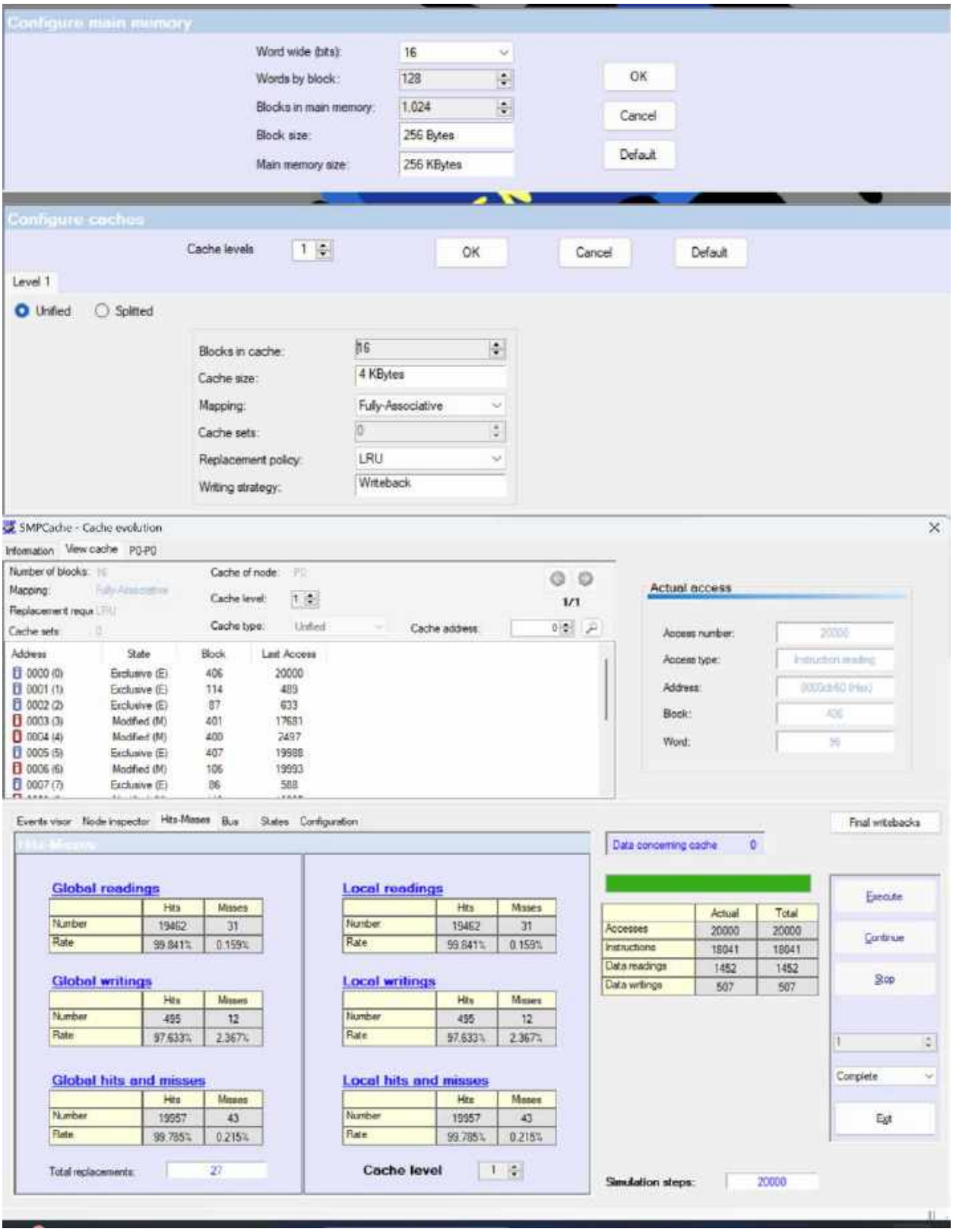

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

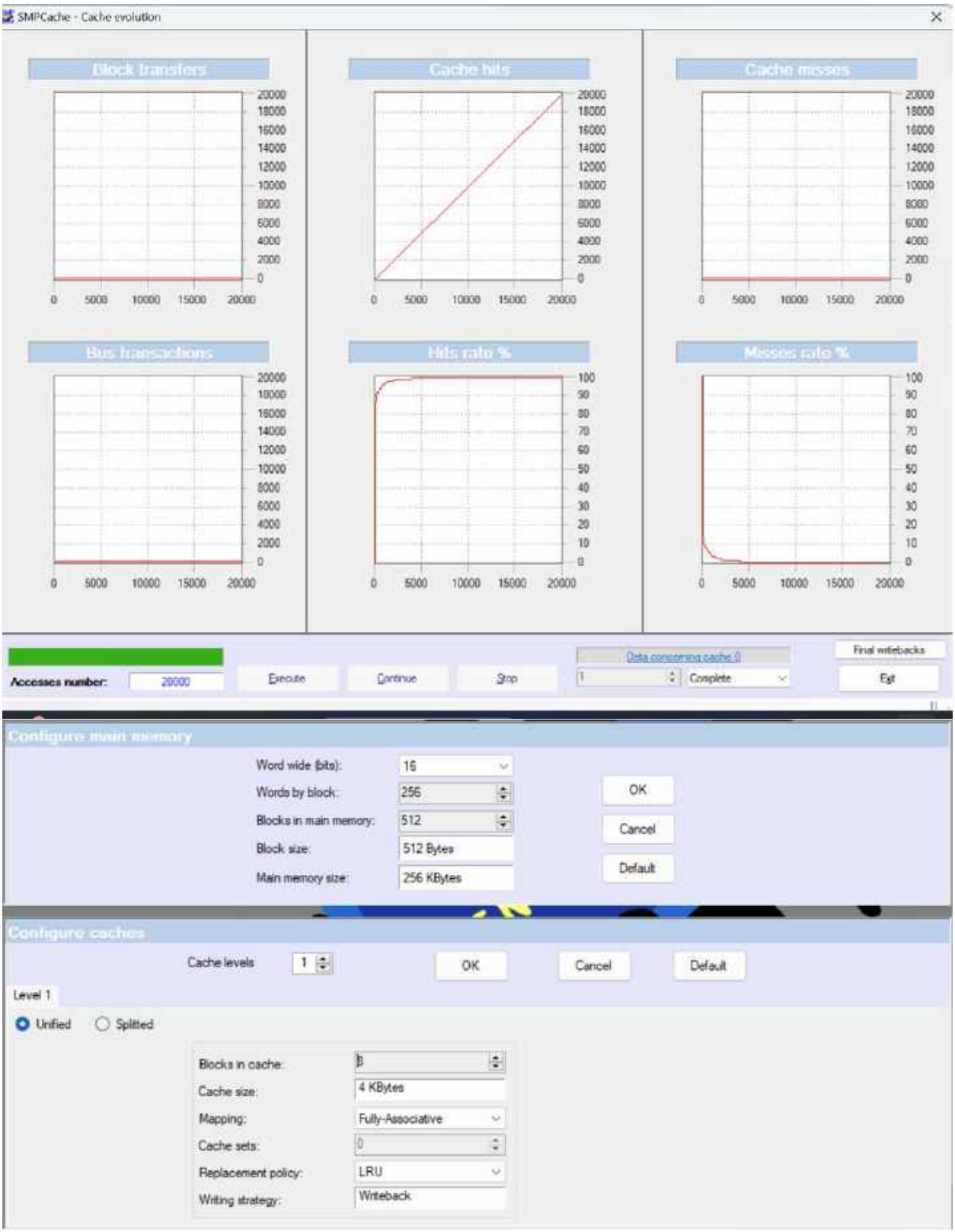

Configure main memory
Word wide (bits): 16
Words by block: 32
Blocks in main memory: 4,096
Block size: 64 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels: 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 64
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 64
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 1602 532
0001 (1) Exclusive (E) 347 588
0002 (2) Exclusive (E) 345 630
0003 (3) Exclusive (E) 350 633
0004 (4) Exclusive (E) 348 601
0005 (5) Exclusive (E) 1619 17968
0006 (6) Modified (M) 1603 2497
0007 (7) Exclusive (E) 1617 637
Actual access
Access number: 20000
Access type: Instruction reading
Address: 0000cc60 (Hex)
Block: 1627
Word: 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 19424 69
Rate 99.646% 0.354%
Global writings
Hits Misses
Number 485 22
Rate 95.661% 4.339%
Global hits and misses
Hits Misses
Number 19909 91
Rate 99.545% 0.455%
Total replacements: 27
Local readings
Hits Misses
Number 19424 69
Rate 99.646% 0.354%
Local writings
Hits Misses
Number 485 22
Rate 95.661% 4.339%
Local hits and misses
Hits Misses
Number 19909 91
Rate 99.545% 0.455%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

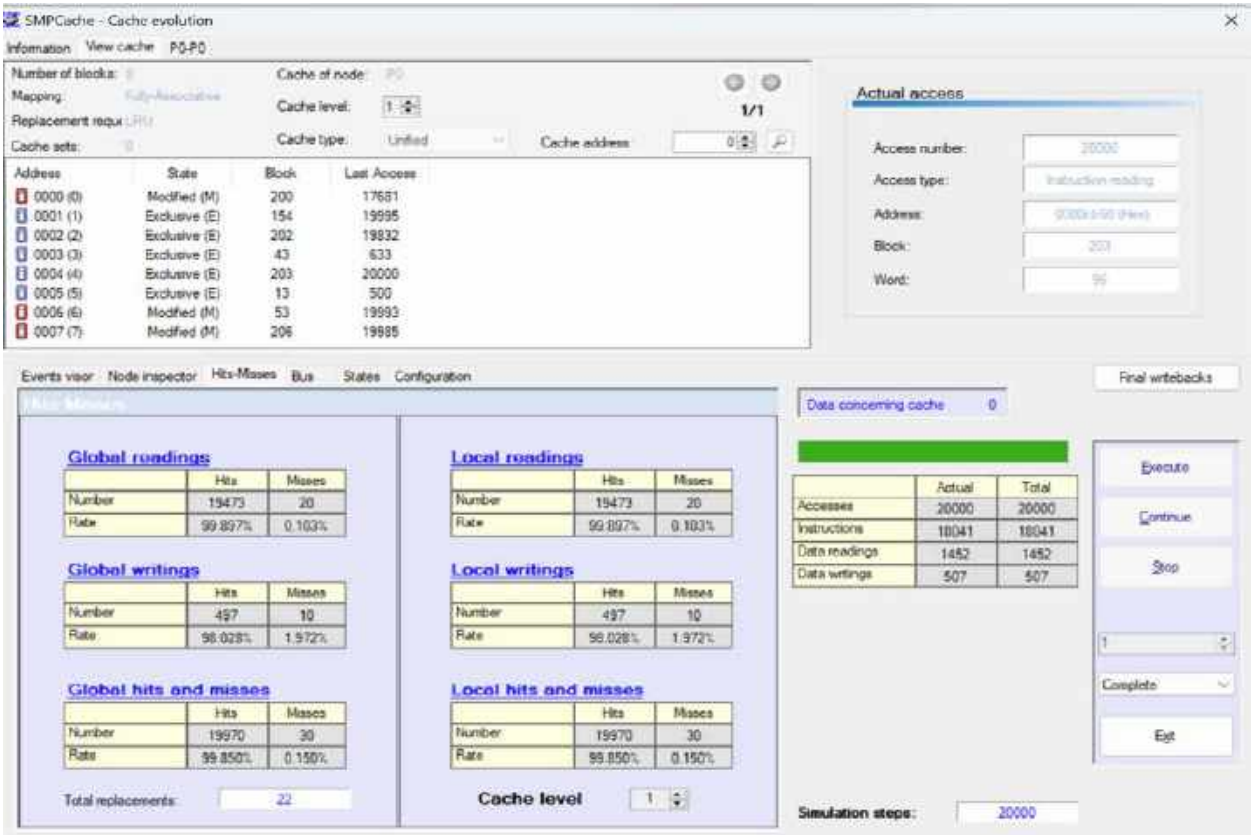

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
64
Blocks in main memory:
2.048
Block size:
128 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
32
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

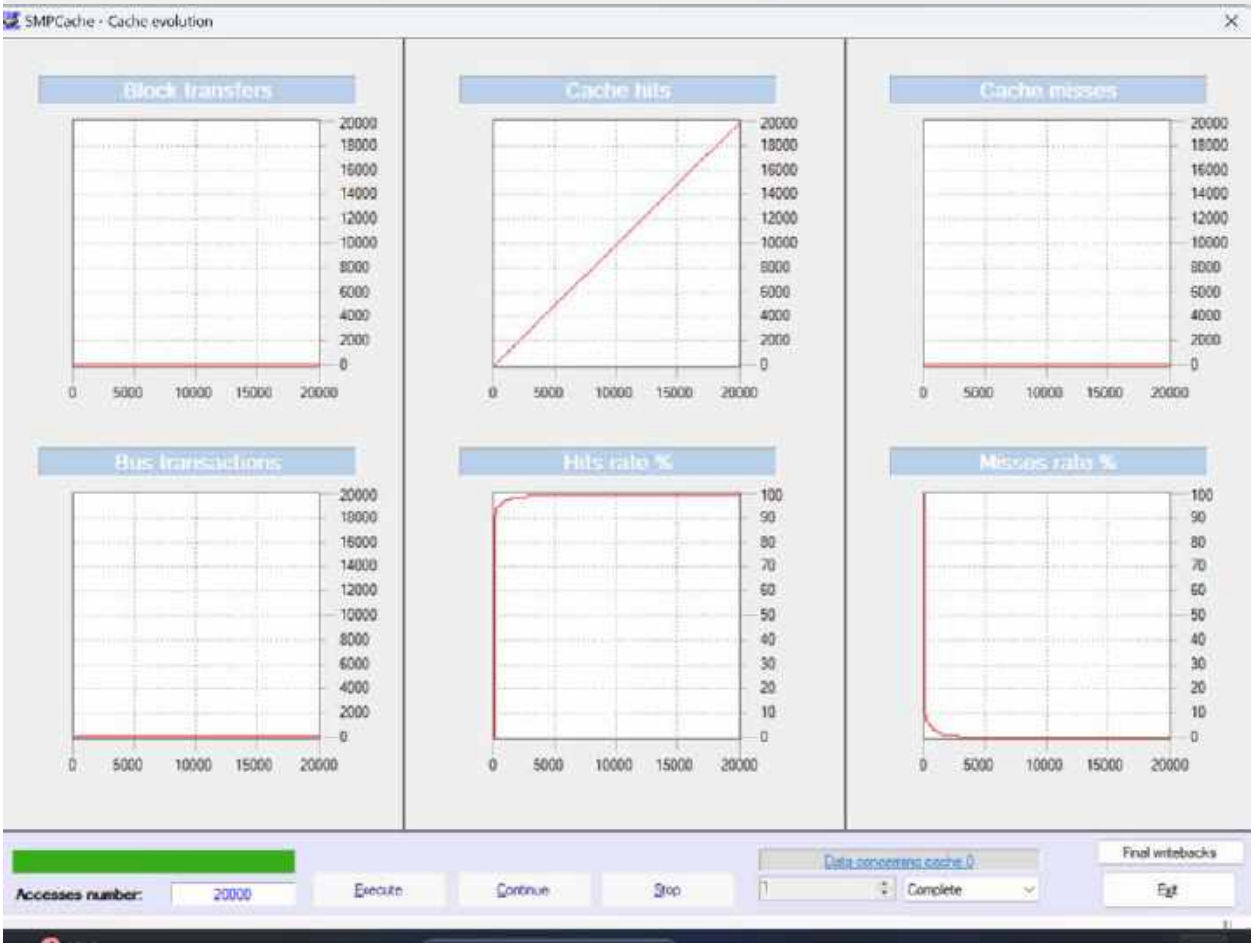

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Cache address:
1/1
Actual access
Access number:
Access type:
Address:
Block:
Word:
Address
State
Block
Last Access
0000 (0) Modified (M) 758 353
0001 (1) Exclusive (E) 223 317
0002 (2) Exclusive (E) 224 376
0003 (3) Exclusive (E) 53 496
0004 (4) Exclusive (E) 52 449
0005 (5) Exclusive (E) 227 420
0006 (6) Modified (M) 759 480
0007 (7) Exclusive (E) 54 498
Events view
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 19450 43
Rate 99.779% 0.221%
Global writings
Number 491 16
Rate 96.844% 3.156%
Global hits and misses
Number 19941 59
Rate 99.705% 0.295%
Total replacements: 27
Local readings
Number 19450 43
Rate 99.779% 0.221%
Local writings
Number 491 16
Rate 96.844% 3.156%
Local hits and misses
Number 19941 59
Rate 99.705% 0.295%
Cache level 1
Actual
Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000

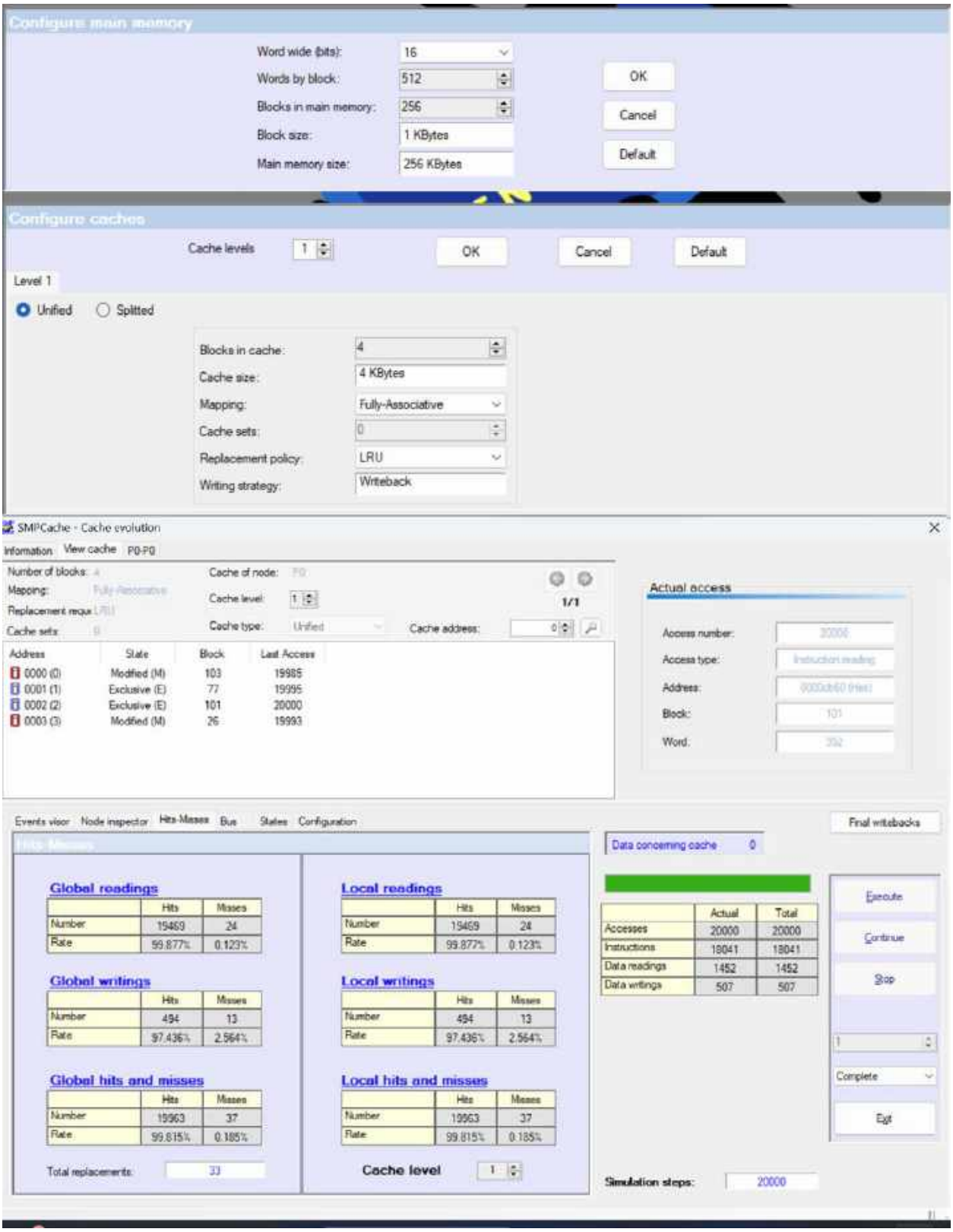

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

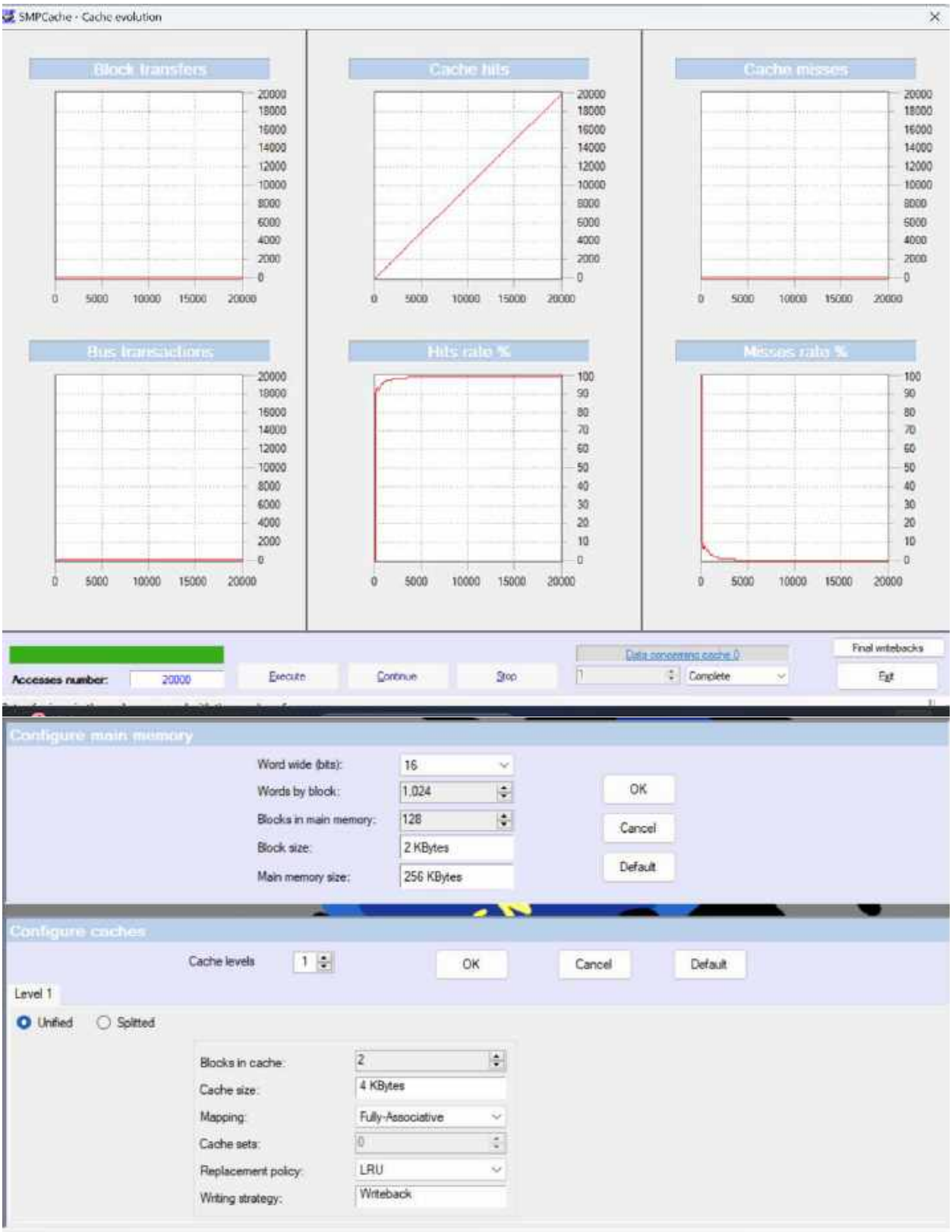

Configure main memory
Word wide (bits): 16
Words by block: 128
Blocks in main memory: 1,024
Block size: 256 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 16
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 406 20000
0001 (1) Exclusive (E) 114 489
0002 (2) Exclusive (E) 87 633
0003 (3) Modified (M) 401 17681
0004 (4) Modified (M) 400 2497
0005 (5) Exclusive (E) 407 19988
0006 (6) Modified (M) 106 19993
0007 (7) Exclusive (E) 86 588
Actual access
Access number: 20000
Access type: Instruction reading
Address: 0000c640 (Hex)
Block: 406
Word: 56
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 19462 31
Rate 99.841% 0.159%
Global writings
Hits Misses
Number 455 12
Rate 97.633% 2.367%
Global hits and misses
Hits Misses
Number 19957 43
Rate 99.785% 0.215%
Total replacements: 27
Local readings
Hits Misses
Number 19462 31
Rate 99.841% 0.159%
Local writings
Hits Misses
Number 455 12
Rate 97.633% 2.367%
Local hits and misses
Hits Misses
Number 19957 43
Rate 99.785% 0.215%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

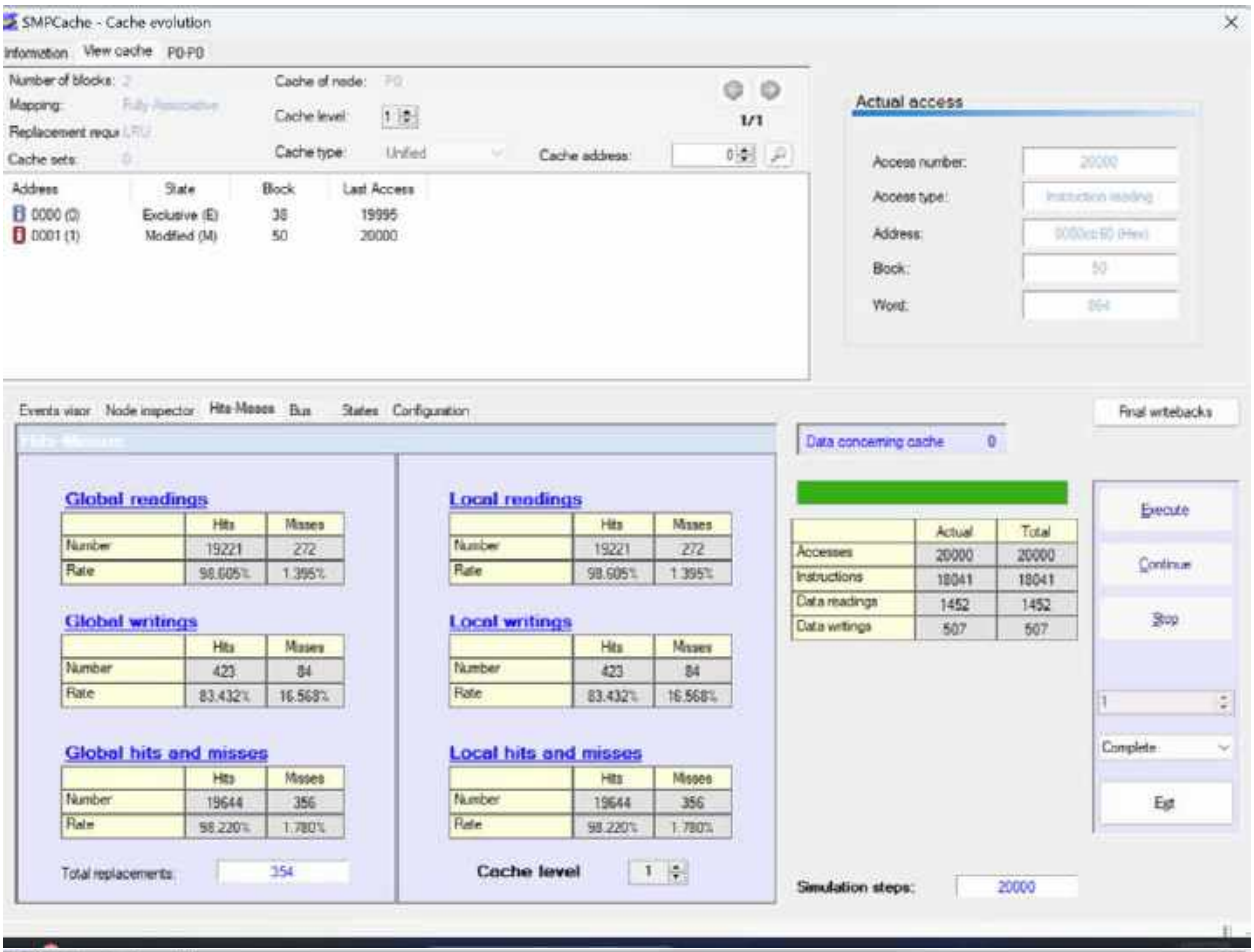

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
256
Blocks in main memory:
512
Block size:
512 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

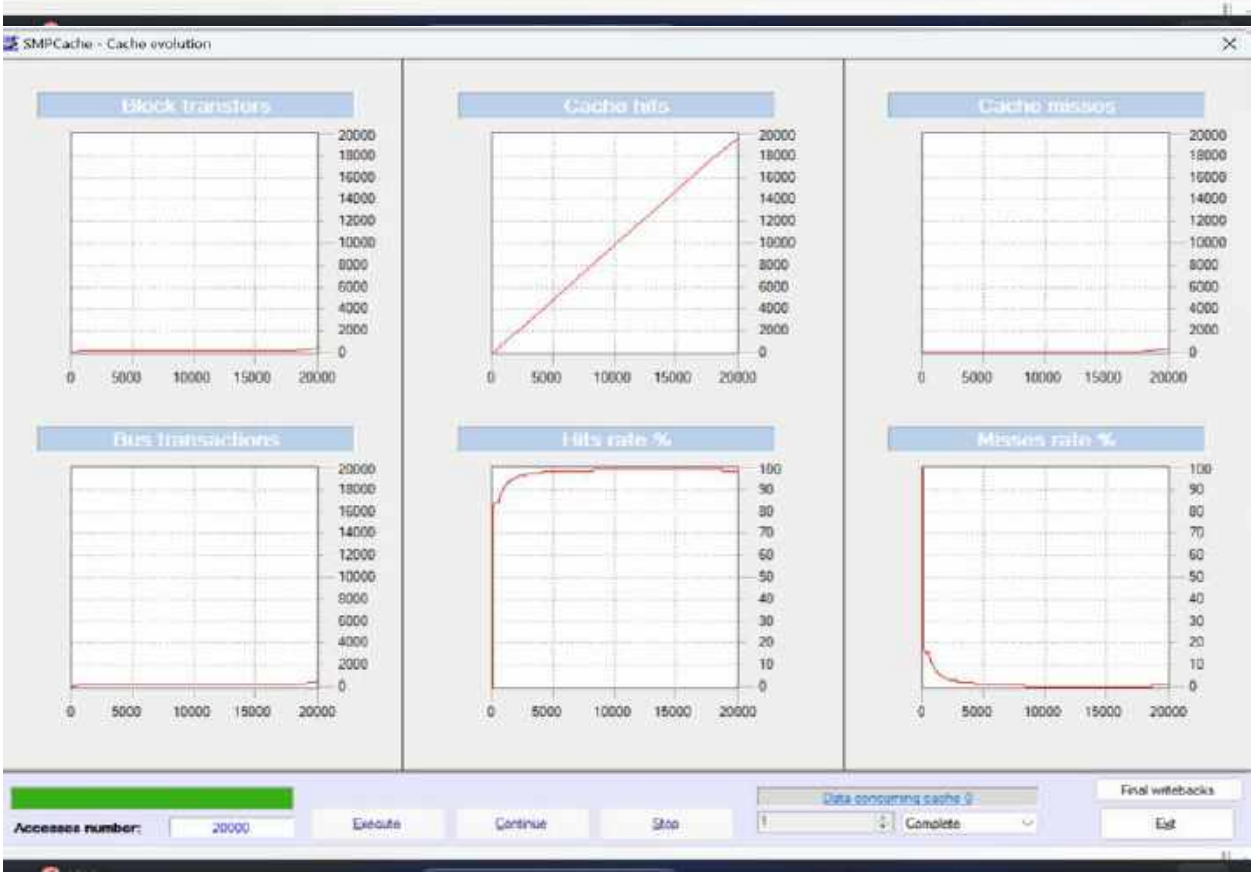

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 200 17681
0001 (1) Exclusive (E) 154 19995
0002 (2) Exclusive (E) 202 19832
0003 (3) Exclusive (E) 43 633
0004 (4) Exclusive (E) 203 20000
0005 (5) Exclusive (E) 13 500
0006 (6) Modified (M) 53 19993
0007 (7) Modified (M) 206 19885
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 19473 20
Rate 99.897% 0.103%
Global writings
Number 497 10
Rate 98.028% 1.972%
Global hits and misses
Number 19970 30
Rate 99.850% 0.150%
Total replacements: 22
Local readings
Number 19473 20
Rate 99.897% 0.103%
Local writings
Number 497 10
Rate 98.028% 1.972%
Local hits and misses
Number 19970 30
Rate 99.850% 0.150%
Cache level
Actual
Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

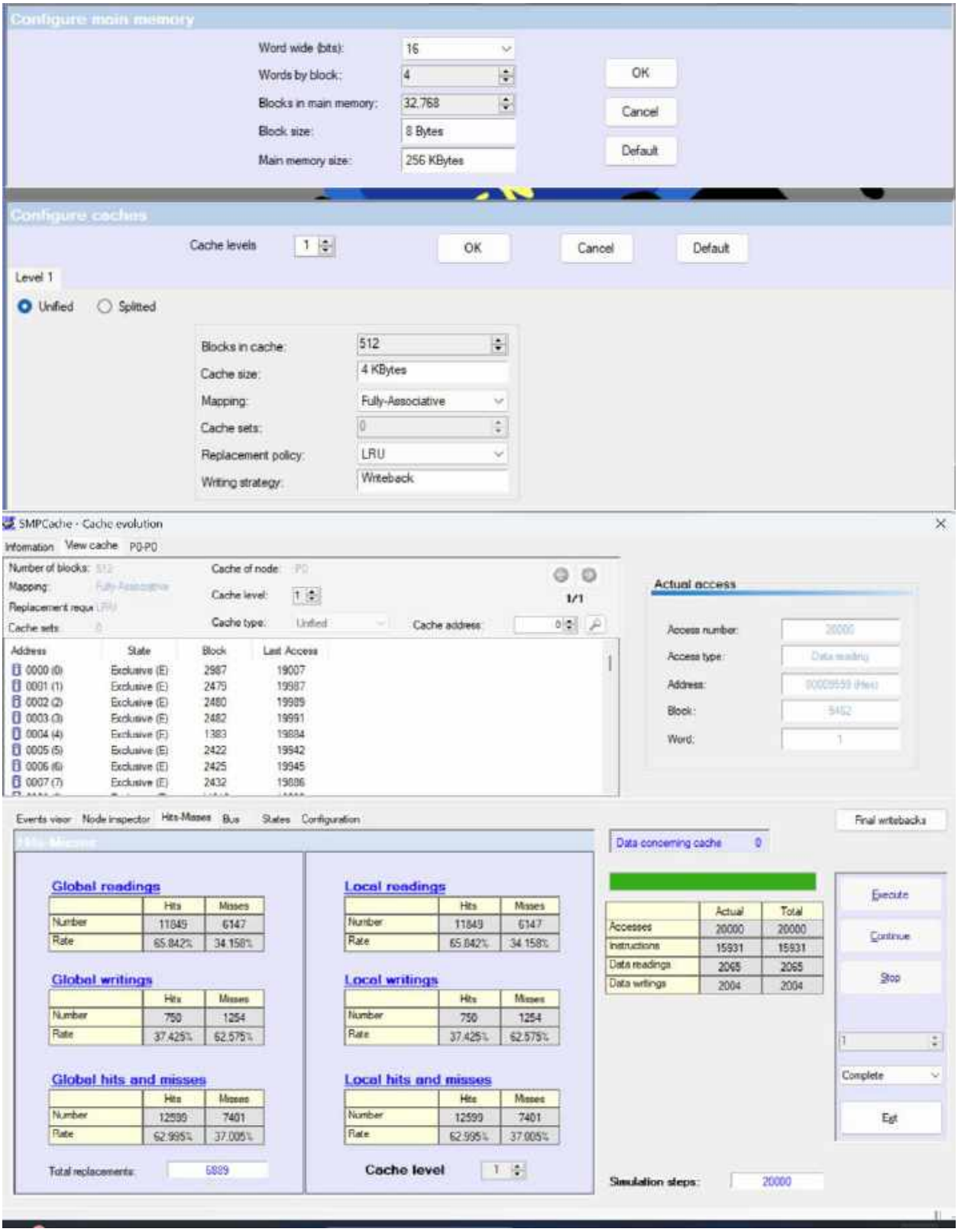

Configure main memory
Word wide (bits): 16
Words by block: 512
Blocks in main memory: 256
Block size: 1 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 4
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 4
Mapping:
Replacement requ
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 103 19985
0001 (1) Exclusive (E) 77 19995
0002 (2) Exclusive (E) 101 20000
0003 (3) Modified (M) 26 19993
Actual access
Access number:
Access type:
Address:
Block: 101
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 19469 24
Rate 99.877% 0.123%
Global writings
Hits Misses
Number 494 13
Rate 97.436% 2.564%
Global hits and misses
Hits Misses
Number 19963 37
Rate 99.815% 0.185%
Total replacements: 33
Local readings
Hits Misses
Number 19469 24
Rate 99.877% 0.123%
Local writings
Hits Misses
Number 494 13
Rate 97.436% 2.564%
Local hits and misses
Hits Misses
Number 19963 37
Rate 99.815% 0.185%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 18041 18041
Data readings 1452 1452
Data writings 507 507
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
1,024
Blocks in main memory:
128
Block size:
2 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
2
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

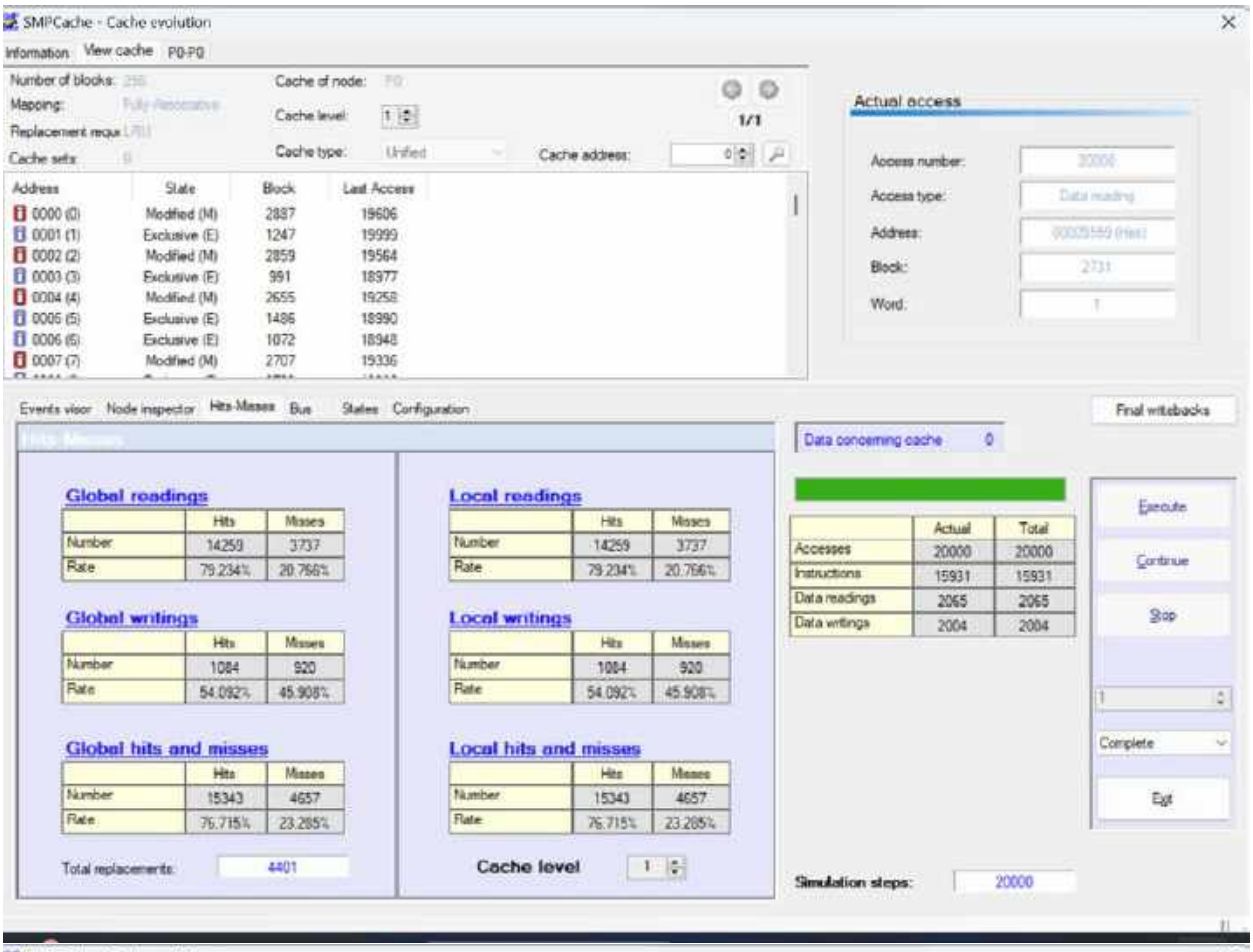

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Exclusive (E)
38
19995
0001 (1)
Modified (M)
50
20000
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
19221
272
Rate
98.605%
1.395%
Global writings
423
84
83.432%
16.568%
Global hits and misses
19644
356
98.220%
1.780%
Total replacements:
354
Local readings
Local writings
Local hits and misses
Cache level
Actual
Total
Accesses
20000
Instructions
18041
Data readings
1452
Data writings
507
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000

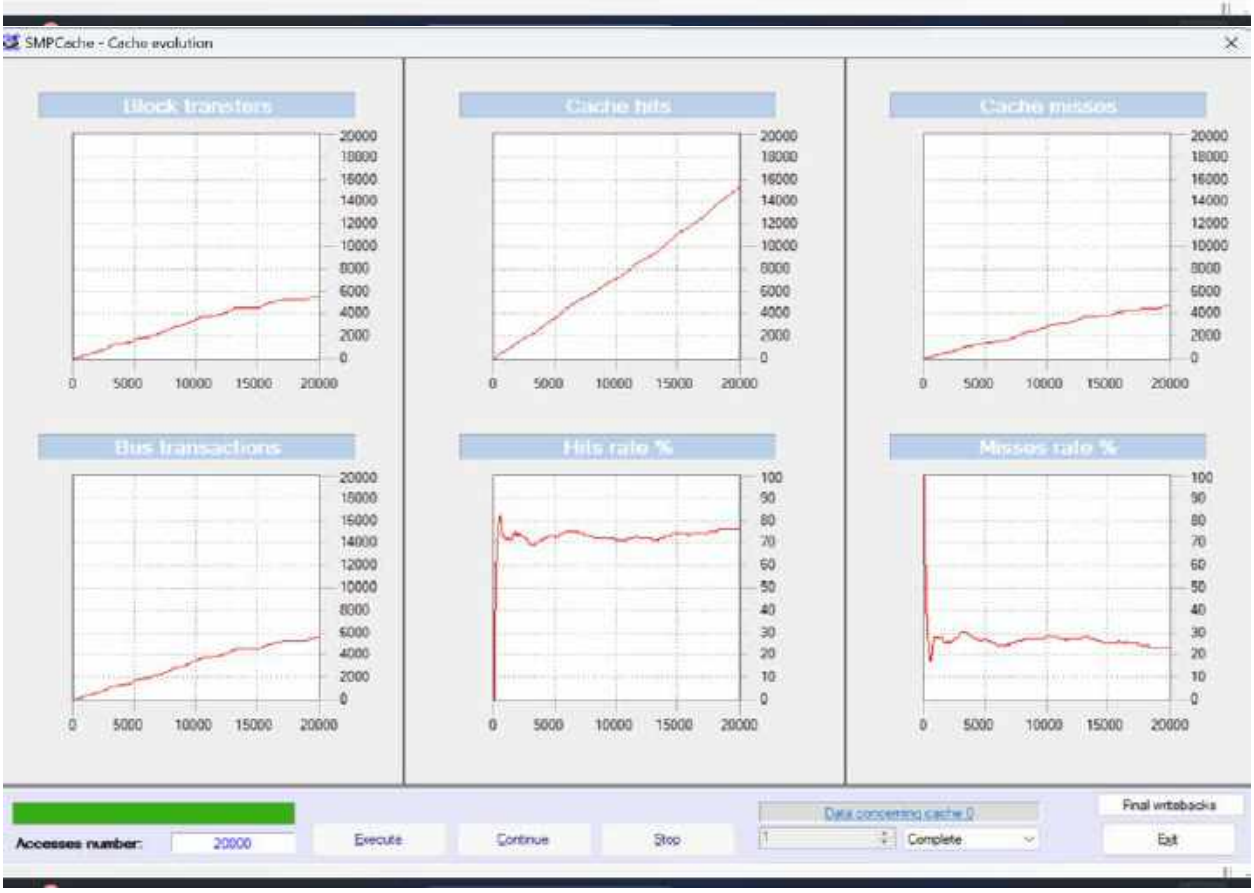

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

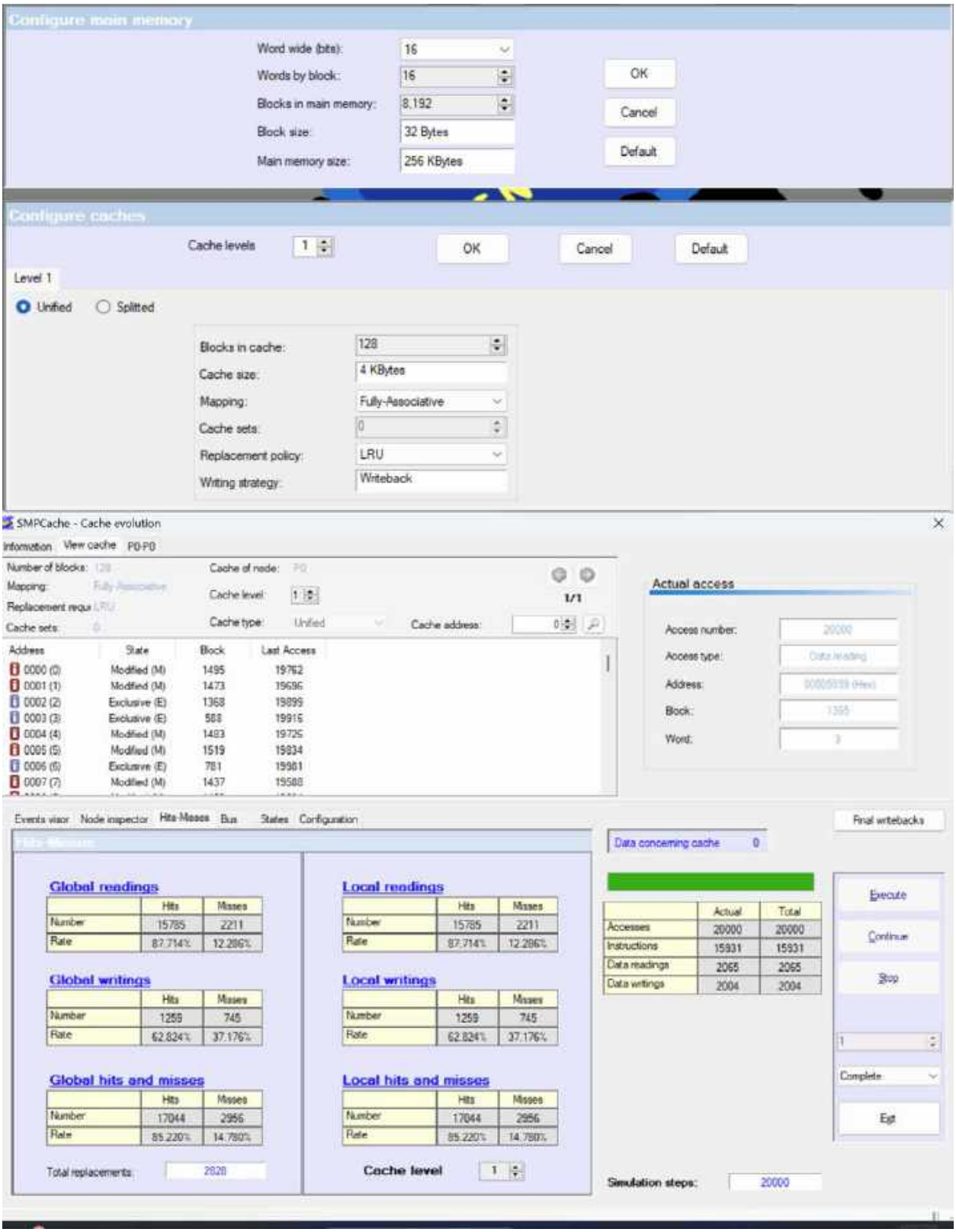
MDLJD

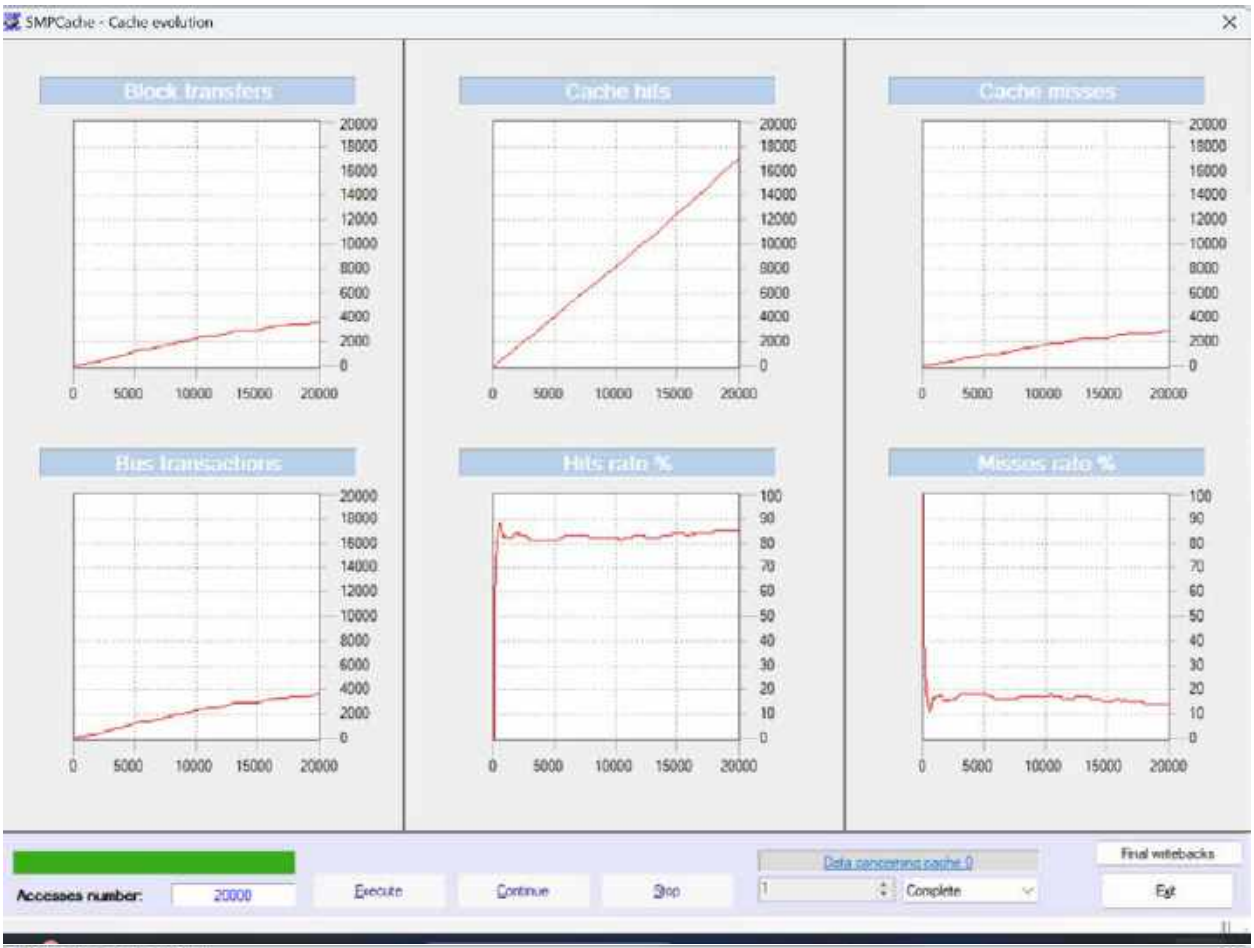

Configure main memory
Word wide (bits): 16
Words by block: 4
Blocks in main memory: 32,768
Block size: 8 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 512
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 512
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 2987 19007
0001 (1) Exclusive (E) 2475 19987
0002 (2) Exclusive (E) 2480 19989
0003 (3) Exclusive (E) 2482 19991
0004 (4) Exclusive (E) 1383 19884
0005 (5) Exclusive (E) 2422 19942
0006 (6) Exclusive (E) 2425 19945
0007 (7) Exclusive (E) 2432 19886
Actual access
Access number: 20000
Access type: Data reading
Address: 00009559 (Hex)
Block: 5452
Word: 1
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 11849 6147
Rate 65.842% 34.158%
Global writings
Hits Misses
Number 750 1254
Rate 37.425% 62.575%
Global hits and misses
Hits Misses
Number 12599 7401
Rate 62.995% 37.005%
Total replacements: 5899
Local readings
Hits Misses
Number 11849 6147
Rate 65.842% 34.158%
Local writings
Hits Misses
Number 750 1254
Rate 37.425% 62.575%
Local hits and misses
Hits Misses
Number 12599 7401
Rate 62.995% 37.005%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

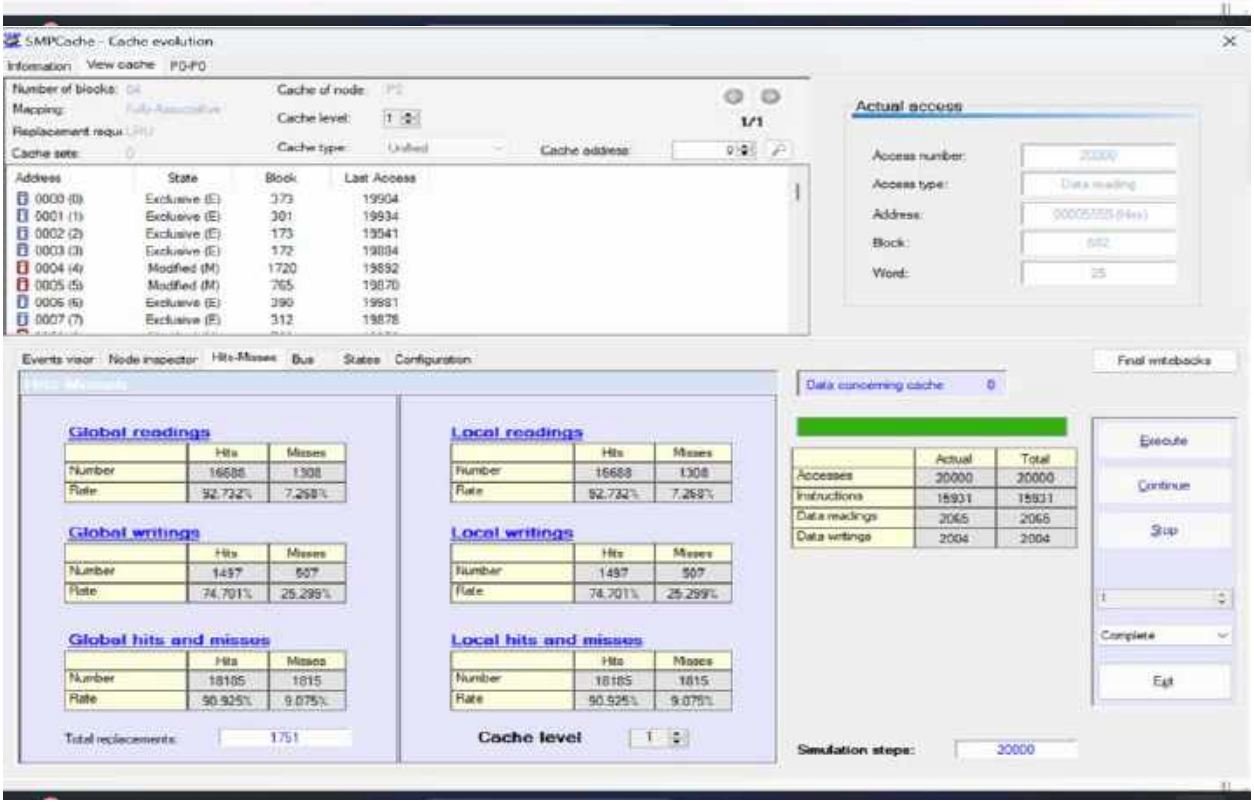
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
8
Blocks in main memory:
16,384
Block size:
16 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
256
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

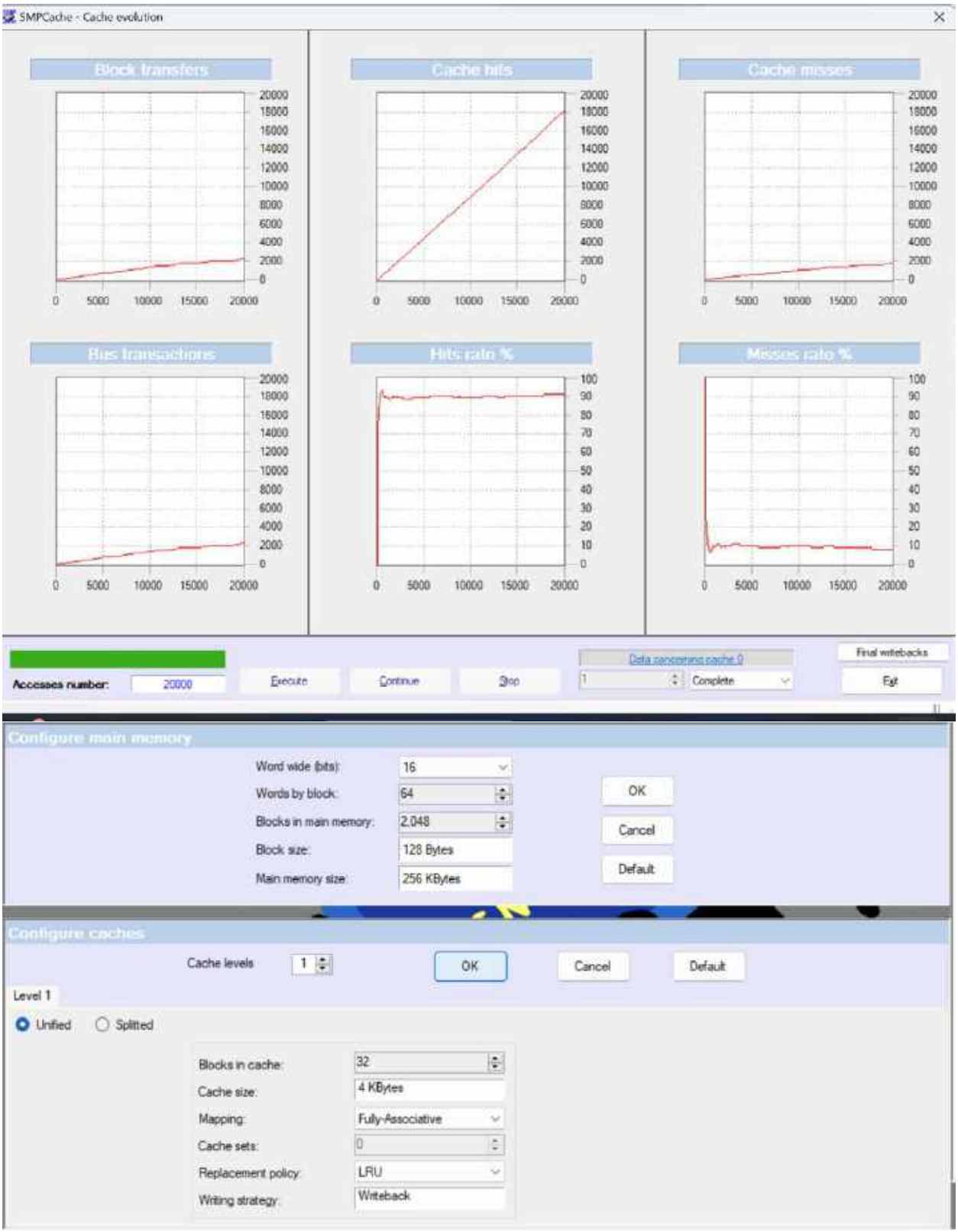

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 2887 19606
0001 (1) Exclusive (E) 1247 19999
0002 (2) Modified (M) 2859 19564
0003 (3) Exclusive (E) 991 18977
0004 (4) Modified (M) 2655 19258
0005 (5) Exclusive (E) 1486 18990
0006 (6) Exclusive (E) 1072 18948
0007 (7) Modified (M) 2707 19336
Actual access
Access number:
Access type:
Address:
Block:
2731
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 14259 3737
Rate 79.234% 20.766%
Global writings
Hits Misses
Number 1084 920
Rate 54.092% 45.908%
Global hits and misses
Hits Misses
Number 15343 4657
Rate 76.715% 23.285%
Total replacements: 4401
Local readings
Hits Misses
Number 14259 3737
Rate 79.234% 20.766%
Local writings
Hits Misses
Number 1084 920
Rate 54.092% 45.908%
Local hits and misses
Hits Misses
Number 15343 4657
Rate 76.715% 23.285%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000

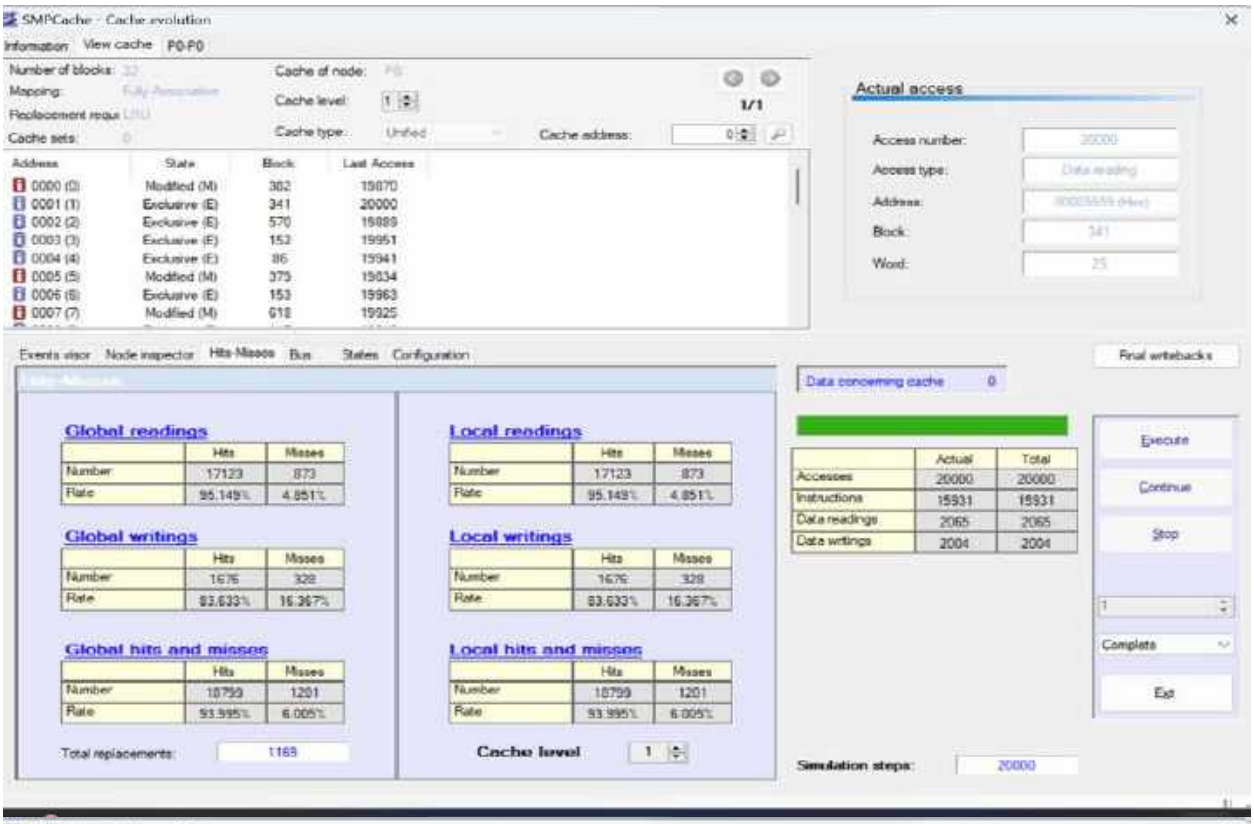

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits ratio %
Misses ratio %
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

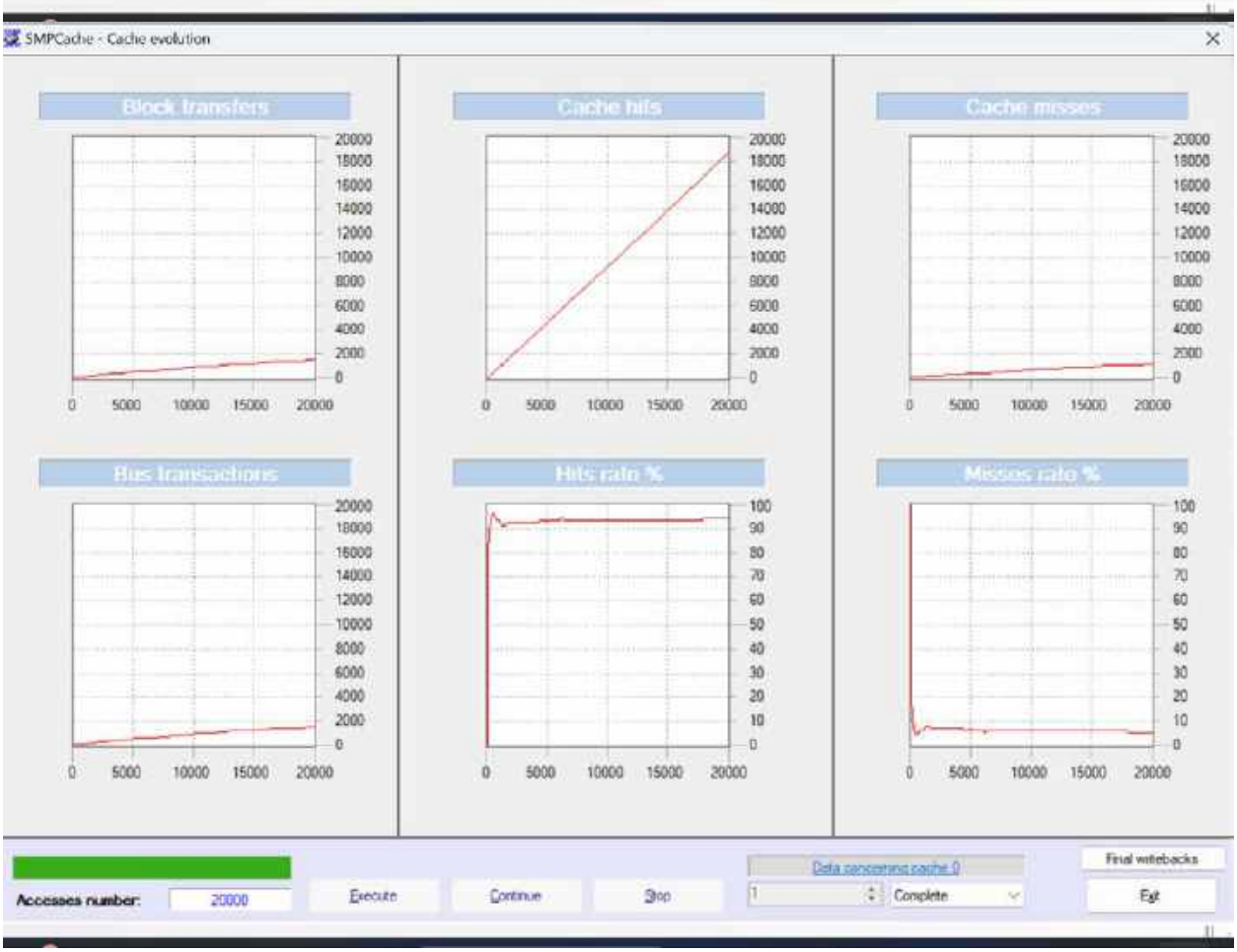

Configure main memory
Word wide (bits): 16
Words by block: 16
Blocks in main memory: 8,192
Block size: 32 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 128
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 128
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 1495 19762
0001 (1) Modified (M) 1473 19696
0002 (2) Exclusive (E) 1368 19899
0003 (3) Exclusive (E) 588 19915
0004 (4) Modified (M) 1483 19725
0005 (5) Modified (M) 1519 19834
0006 (6) Exclusive (E) 781 19981
0007 (7) Modified (M) 1437 19588
Actual access
Access number: 20000
Access type: Data reading
Address: 00000039 (Hex)
Block: 1365
Word: 3
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 15785 2211
Rate 87.714% 12.286%
Global writings
Hits Misses
Number 1259 745
Rate 62.824% 37.176%
Global hits and misses
Hits Misses
Number 17044 2956
Rate 85.220% 14.780%
Total replacements: 2828
Local readings
Hits Misses
Number 15785 2211
Rate 87.714% 12.286%
Local writings
Hits Misses
Number 1259 745
Rate 62.824% 37.176%
Local hits and misses
Hits Misses
Number 17044 2956
Rate 85.220% 14.780%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

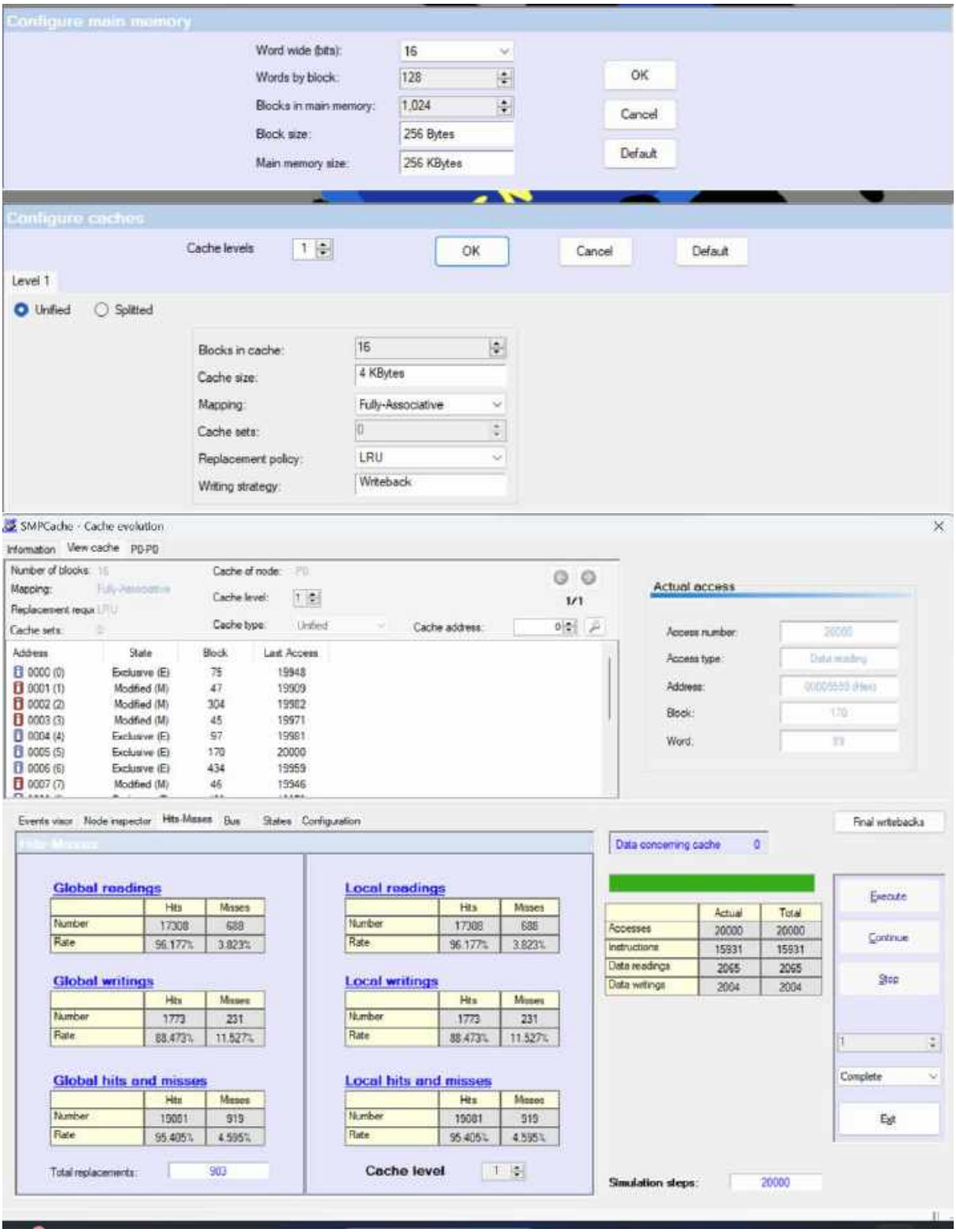

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit


SMPCache - Cache evolution
Information
View cache
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 373 19904
0001 (1) Exclusive (E) 301 19934
0002 (2) Exclusive (E) 173 19941
0003 (3) Exclusive (E) 172 19884
0004 (4) Modified (M) 1720 19892
0005 (5) Modified (M) 765 19870
0006 (6) Exclusive (E) 390 19881
0007 (7) Exclusive (E) 312 19878
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viewer
Node inspector
Hits-Misses
Bus
States
Configuration
Global readings
Hits
Misses
Number 16688 1308
Rate 92.732% 7.268%
Global writings
Number 1497 507
Rate 74.701% 25.299%
Global hits and misses
Number 18185 1815
Rate 90.925% 9.075%
Total replacements: 1751
Local readings
Number 16688 1308
Rate 92.732% 7.268%
Local writings
Number 1497 507
Rate 74.701% 25.299%
Local hits and misses
Number 18185 1815
Rate 90.925% 9.075%
Cache level
Data concerning cache 0
Actual
Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
Complete
Exit
Final writebacks
Simulation steps:
20000

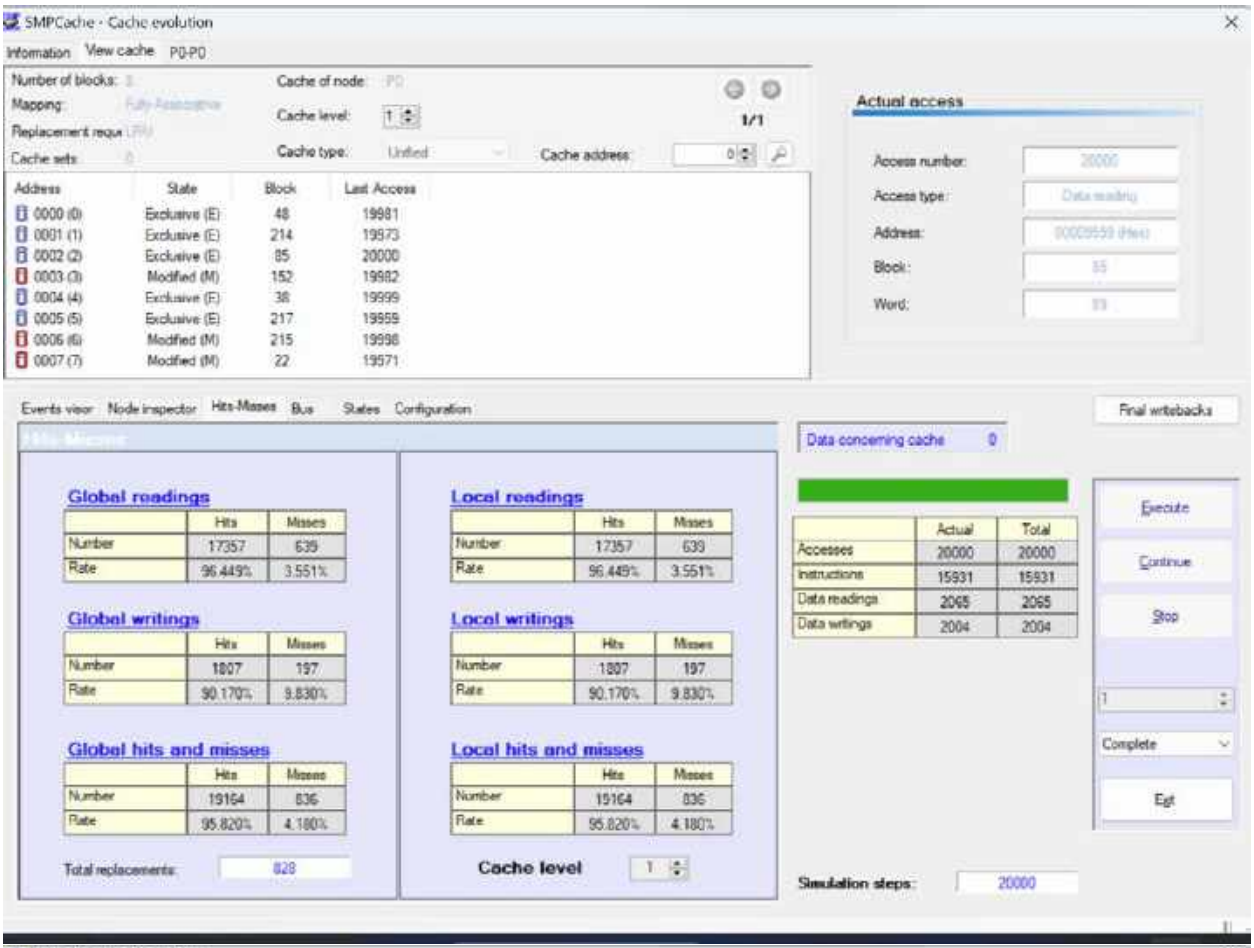

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
64
Blocks in main memory:
2.048
Block size:
128 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
32
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

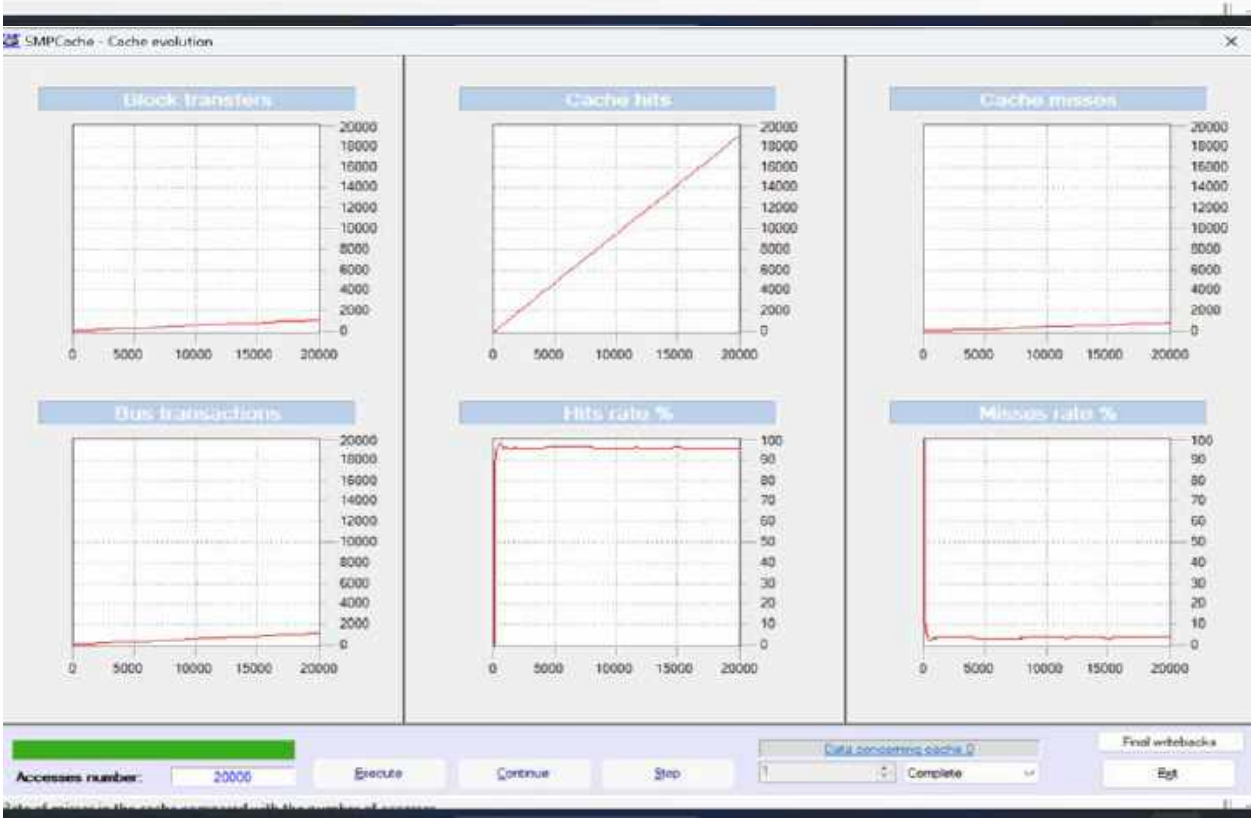

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Actual access
Access number:
Access type:
Address:
Block:
Word:
Address
State
Block
Last Access
0000 (0) Modified (M) 382 19870
0001 (1) Exclusive (E) 341 20000
0002 (2) Exclusive (E) 570 19889
0003 (3) Exclusive (E) 153 19951
0004 (4) Exclusive (E) 86 19941
0005 (5) Modified (M) 375 19834
0006 (6) Exclusive (E) 153 19963
0007 (7) Modified (M) 618 19925
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 17123 873
Rate 95.149% 4.851%
Global writings
Number 1676 328
Rate 83.633% 16.367%
Global hits and misses
Number 18799 1201
Rate 93.995% 6.005%
Total replacements: 1169
Local readings
Number 17123 873
Rate 95.149% 4.851%
Local writings
Number 1676 328
Rate 83.633% 16.367%
Local hits and misses
Number 18799 1201
Rate 93.995% 6.005%
Cache level 1
Actual
Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000

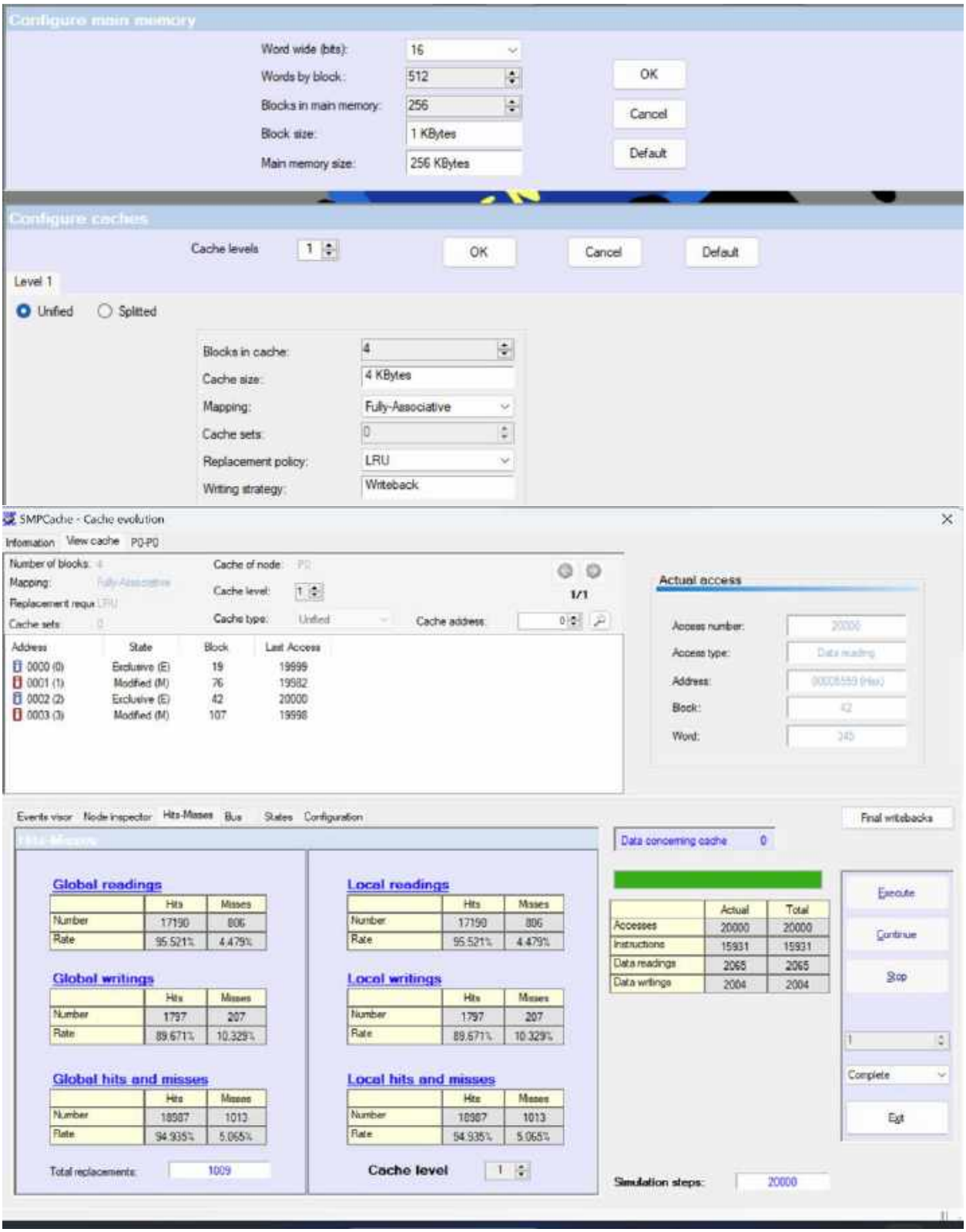

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0
2000
4000
6000
8000
10000
12000
14000
16000
18000
20000
0
5000
10000
15000
20000
0
10
20
30
40
50
60
70
80
90
100
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

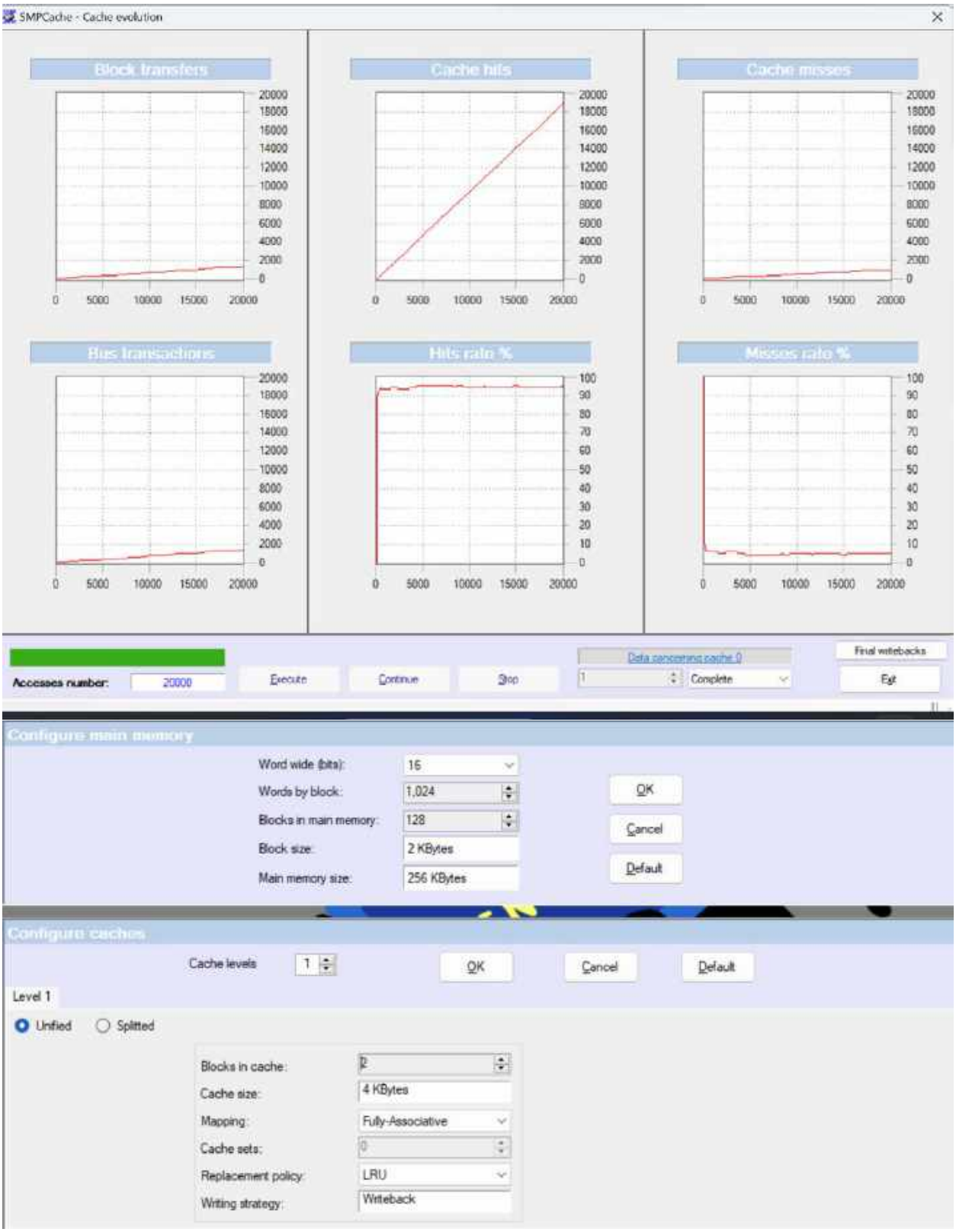

Configure main memory
Word wide (bits): 16
Words by block: 128
Blocks in main memory: 1,024
Block size: 256 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 16
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 16
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 75 19948
0001 (1) Modified (M) 47 19909
0002 (2) Modified (M) 304 19982
0003 (3) Modified (M) 45 19971
0004 (4) Exclusive (E) 97 19981
0005 (5) Exclusive (E) 170 20000
0006 (6) Exclusive (E) 434 19959
0007 (7) Modified (M) 46 19946
Actual access
Access number: 20000
Access type: Data reading
Address: 00000000 (Hex)
Block: 170
Word: 33
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 17308 688
Rate 96.177% 3.823%
Global writings
Hits Misses
Number 1773 231
Rate 88.473% 11.527%
Global hits and misses
Hits Misses
Number 19081 919
Rate 95.405% 4.595%
Total replacements: 903
Local readings
Hits Misses
Number 17308 688
Rate 96.177% 3.823%
Local writings
Hits Misses
Number 1773 231
Rate 88.473% 11.527%
Local hits and misses
Hits Misses
Number 19081 919
Rate 95.405% 4.595%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data consistency cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
256
Blocks in main memory:
512
Block size:
512 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback


SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 48 19981
0001 (1) Exclusive (E) 214 19973
0002 (2) Exclusive (E) 85 20000
0003 (3) Modified (M) 152 19982
0004 (4) Exclusive (E) 38 19999
0005 (5) Exclusive (E) 217 19999
0006 (6) Modified (M) 215 19998
0007 (7) Modified (M) 22 19971
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viewr
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 17357 639
Rate 96.449% 3.551%
Global writings
Number 1807 197
Rate 90.170% 9.830%
Global hits and misses
Number 19164 836
Rate 95.820% 4.180%
Total replacements: 828
Local readings
Number 17357 639
Rate 96.449% 3.551%
Local writings
Number 1807 197
Rate 90.170% 9.830%
Local hits and misses
Number 19164 836
Rate 95.820% 4.180%
Cache level
Actual
Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000

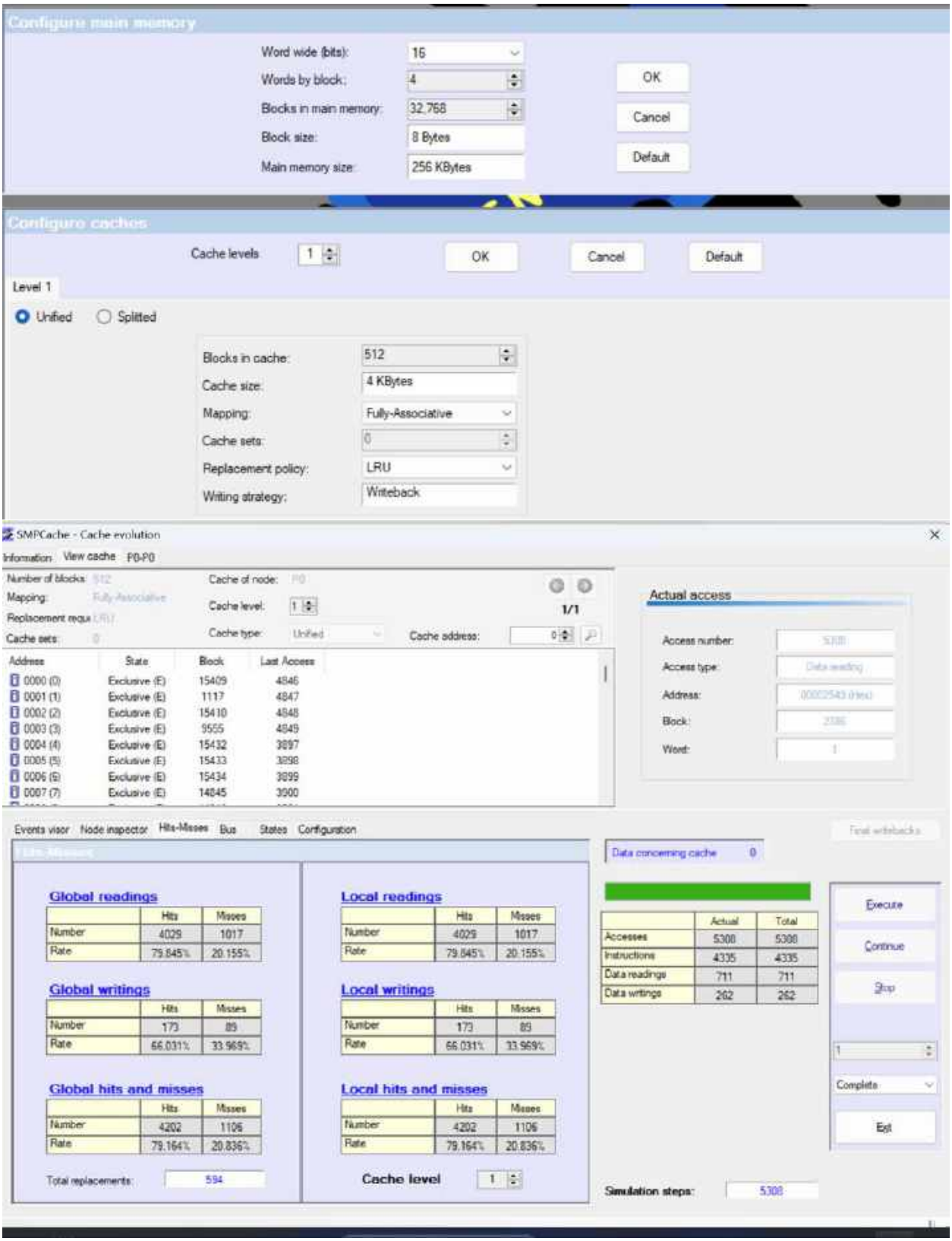

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits): 16
Words by block: 512
Blocks in main memory: 256
Block size: 1 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 4
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 4
Mapping: Fully-Associative
Replacement requ: LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 19 19999
0001 (1) Modified (M) 76 19982
0002 (2) Exclusive (E) 42 20000
0003 (3) Modified (M) 107 19998
Actual access
Access number: 20000
Access type: Data reading
Address: 00008550 (Hex)
Block: 42
Word: 245
Events visor Node inspector Hits-Misses Bus States Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits Misses
Number 17190 806
Rate 95.521% 4.479%
Local readings
Hits Misses
Number 17190 806
Rate 95.521% 4.479%
Global writings
Hits Misses
Number 1797 207
Rate 89.671% 10.329%
Local writings
Hits Misses
Number 1797 207
Rate 89.671% 10.329%
Global hits and misses
Hits Misses
Number 18987 1013
Rate 94.935% 5.065%
Local hits and misses
Hits Misses
Number 18987 1013
Rate 94.935% 5.065%
Total replacements: 1009
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15931 15931
Data readings 2065 2065
Data writings 2004 2004
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

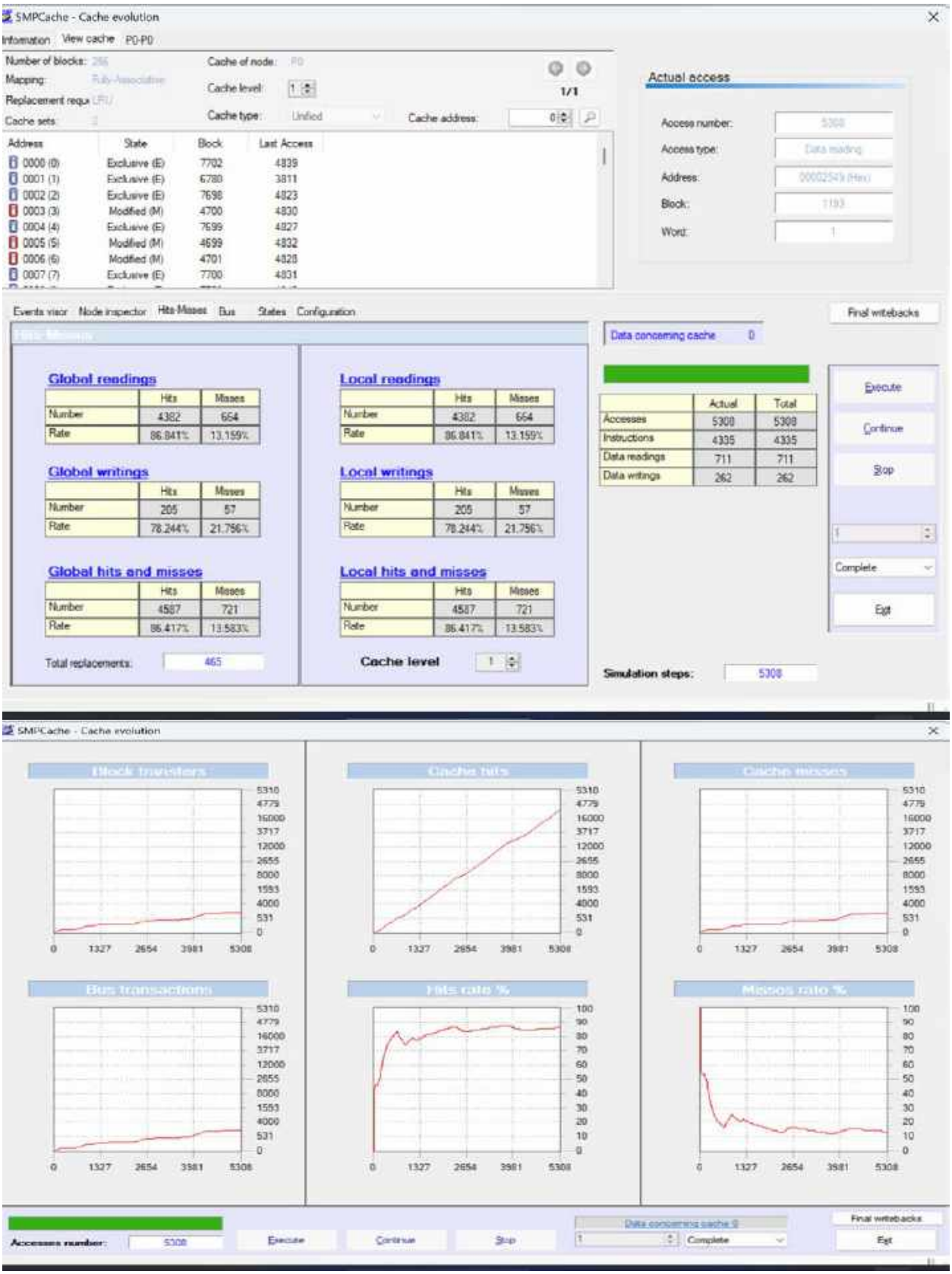

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
1,024
Blocks in main memory:
128
Block size:
2 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
2
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

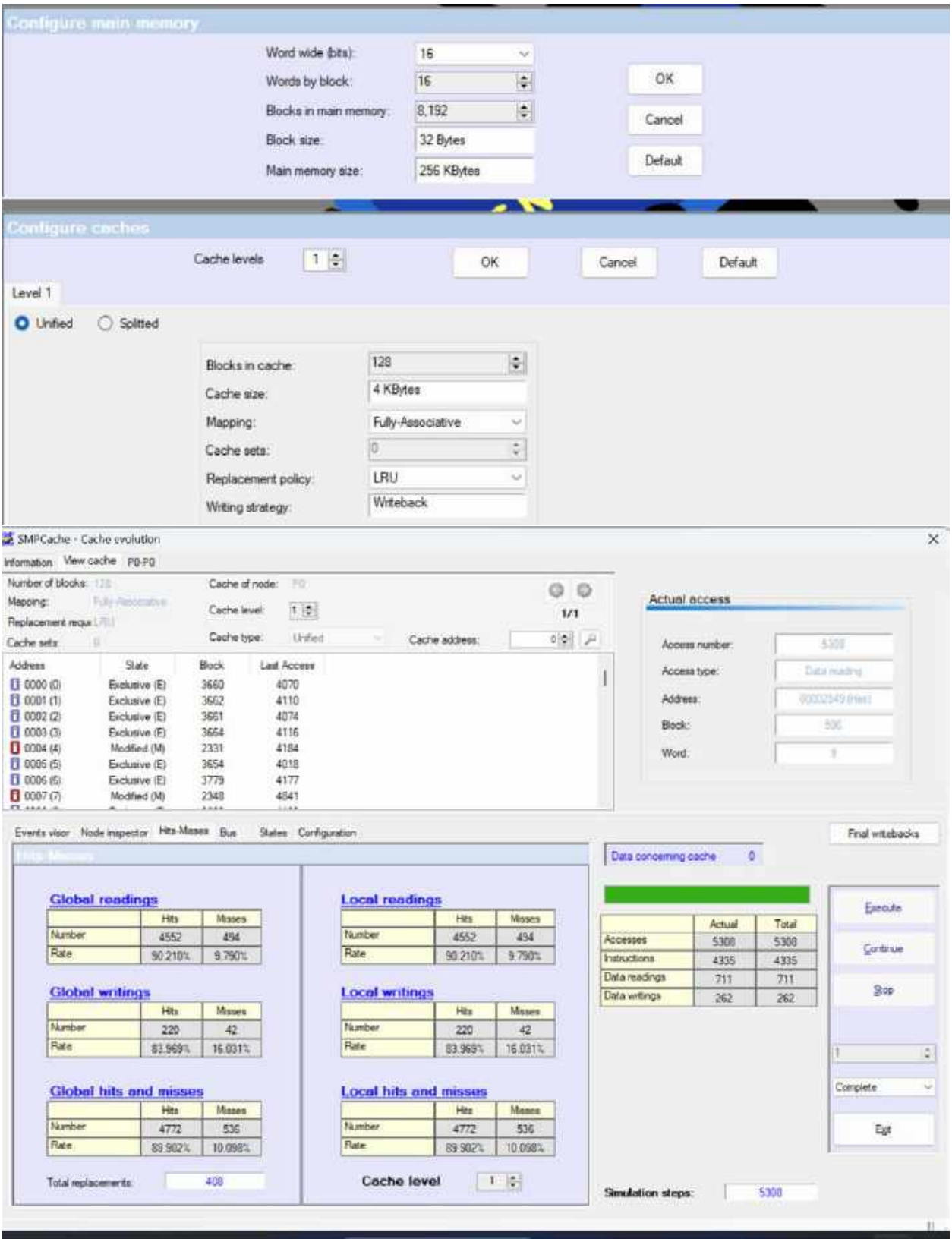
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Exclusive (E)
9
19999
0001 (1)
Exclusive (E)
21
20000
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
16621
1375
Rate
92.359%
7.641%
Local readings
Global writings
1317
687
65.719%
34.281%
Local writings
Global hits and misses
17938
2062
89.690%
10.310%
Local hits and misses
Total replacements:
2060
Cache level
Actual
Total
Accesses
20000
Instructions
15931
Data readings
2065
Data writings
2004
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits ratio %
Misses ratio %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

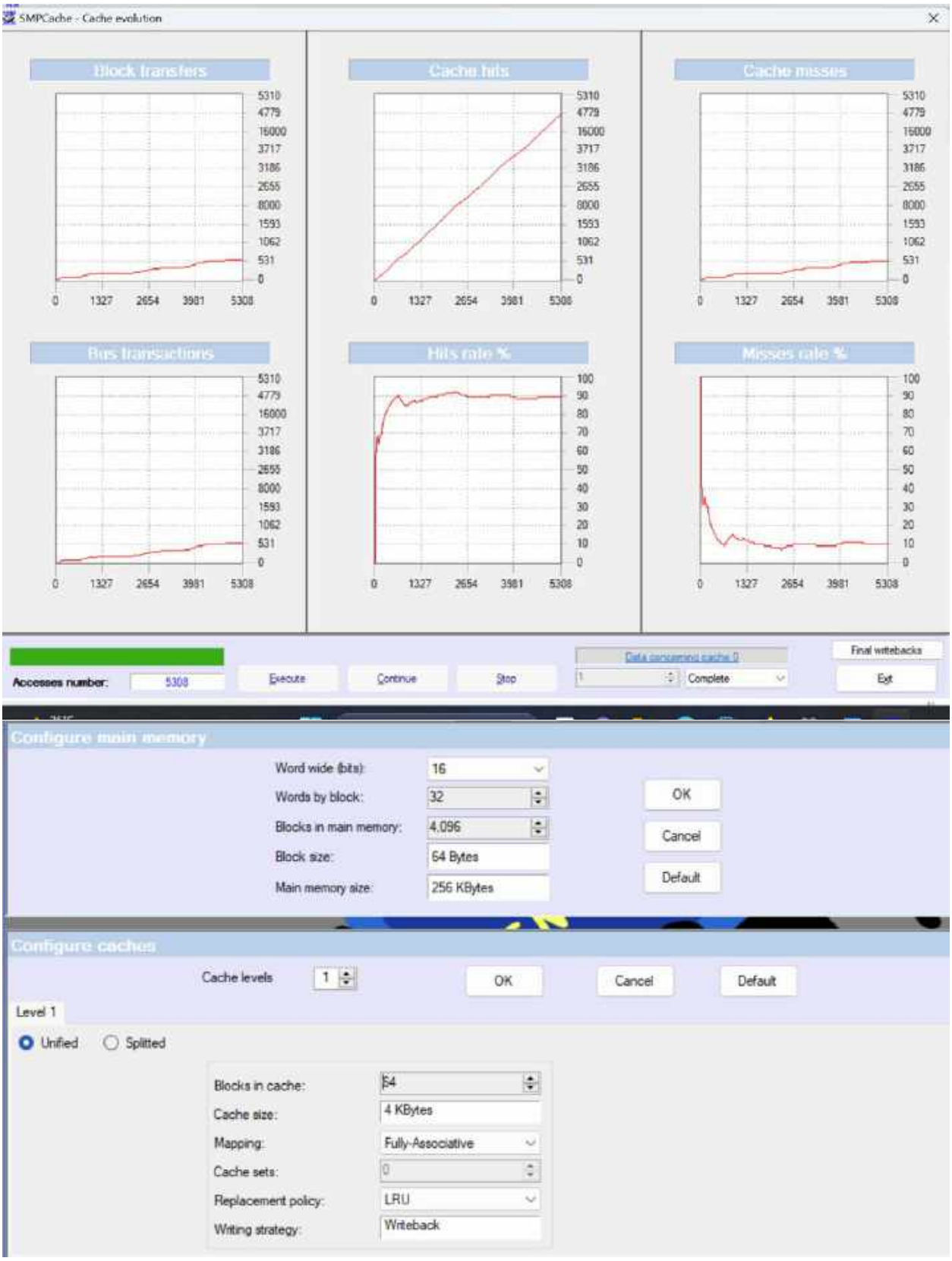
EAR

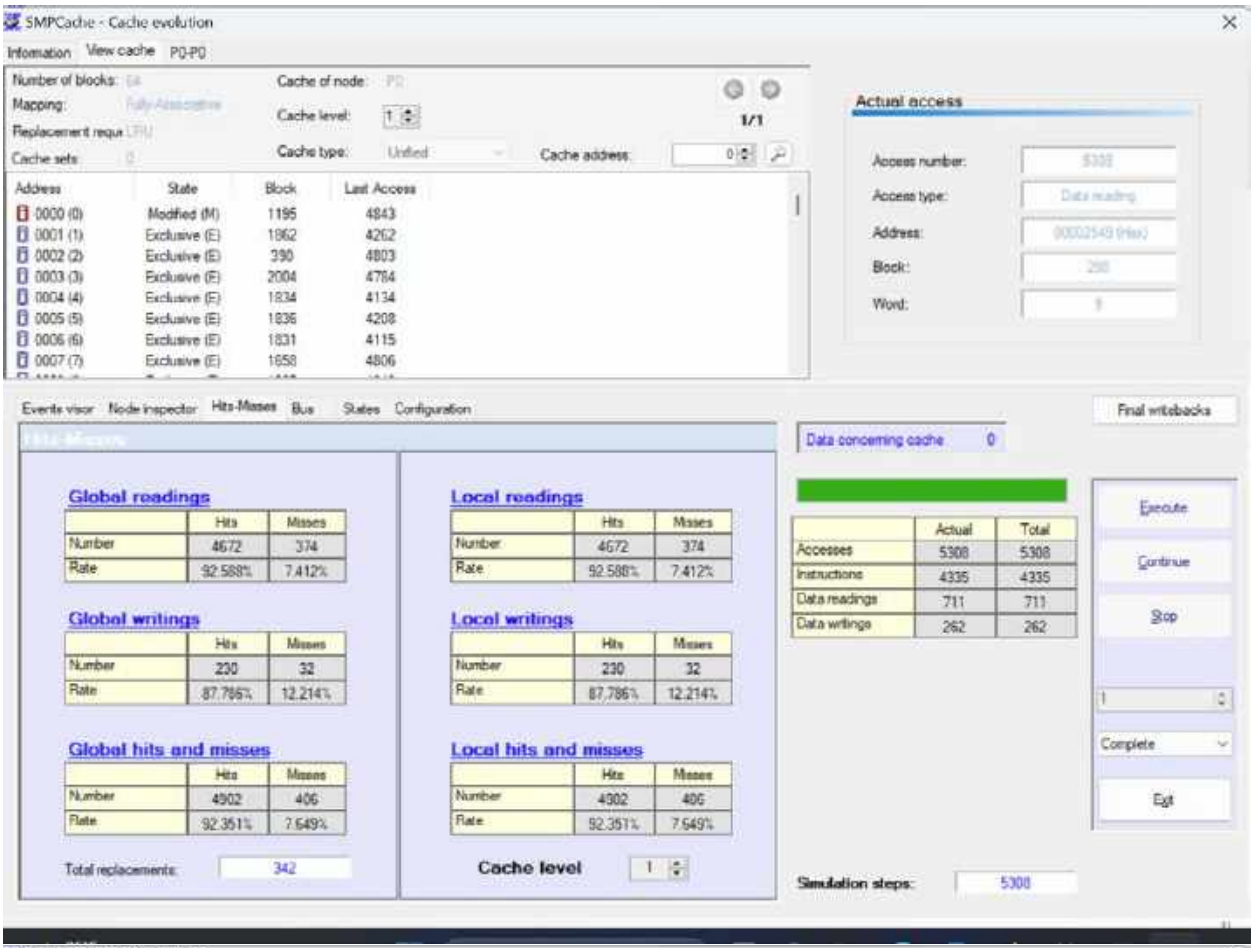

Configure main memory
Word wide (bits): 16
Words by block: 4
Blocks in main memory: 32,768
Block size: 8 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 512
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 512
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 15409 4846
0001 (1) Exclusive (E) 1117 4847
0002 (2) Exclusive (E) 15410 4848
0003 (3) Exclusive (E) 9555 4849
0004 (4) Exclusive (E) 15432 3897
0005 (5) Exclusive (E) 15433 3898
0006 (6) Exclusive (E) 15434 3899
0007 (7) Exclusive (E) 14845 3900
Actual access
Access number: 5300
Access type: Data reading
Address: 00002543 (Hex)
Block: 2386
Word: 1
Events visor Node inspector Hits-Misses Bus States Configuration
Data concerning cache 0
Global readings
Hits Misses
Number 4029 1017
Rate 79.845% 20.155%
Global writings
Hits Misses
Number 173 89
Rate 66.031% 33.969%
Global hits and misses
Hits Misses
Number 4202 1106
Rate 79.164% 20.836%
Total replacements: 594
Local readings
Hits Misses
Number 4029 1017
Rate 79.845% 20.155%
Local writings
Hits Misses
Number 173 89
Rate 66.031% 33.969%
Local hits and misses
Hits Misses
Number 4202 1106
Rate 79.164% 20.836%
Cache level 1
Actual Total
Accesses 5300 5300
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5300

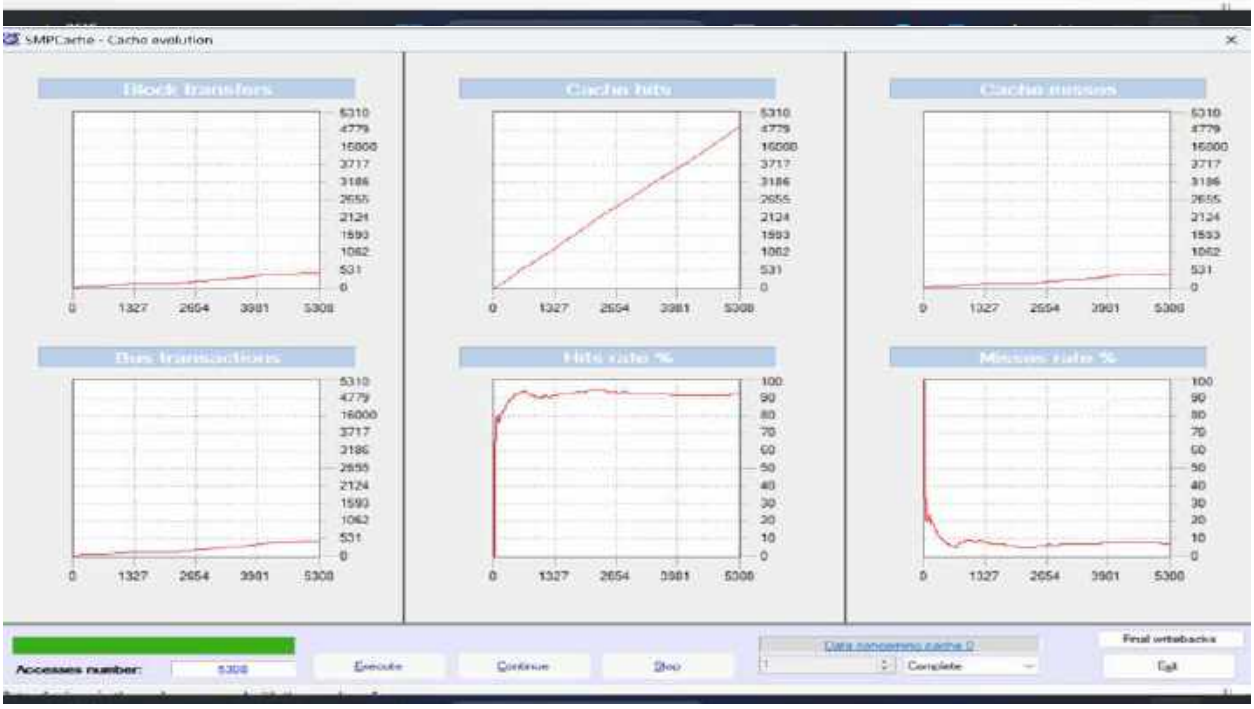
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
8
Blocks in main memory:
16.384
Block size:
16 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
256
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

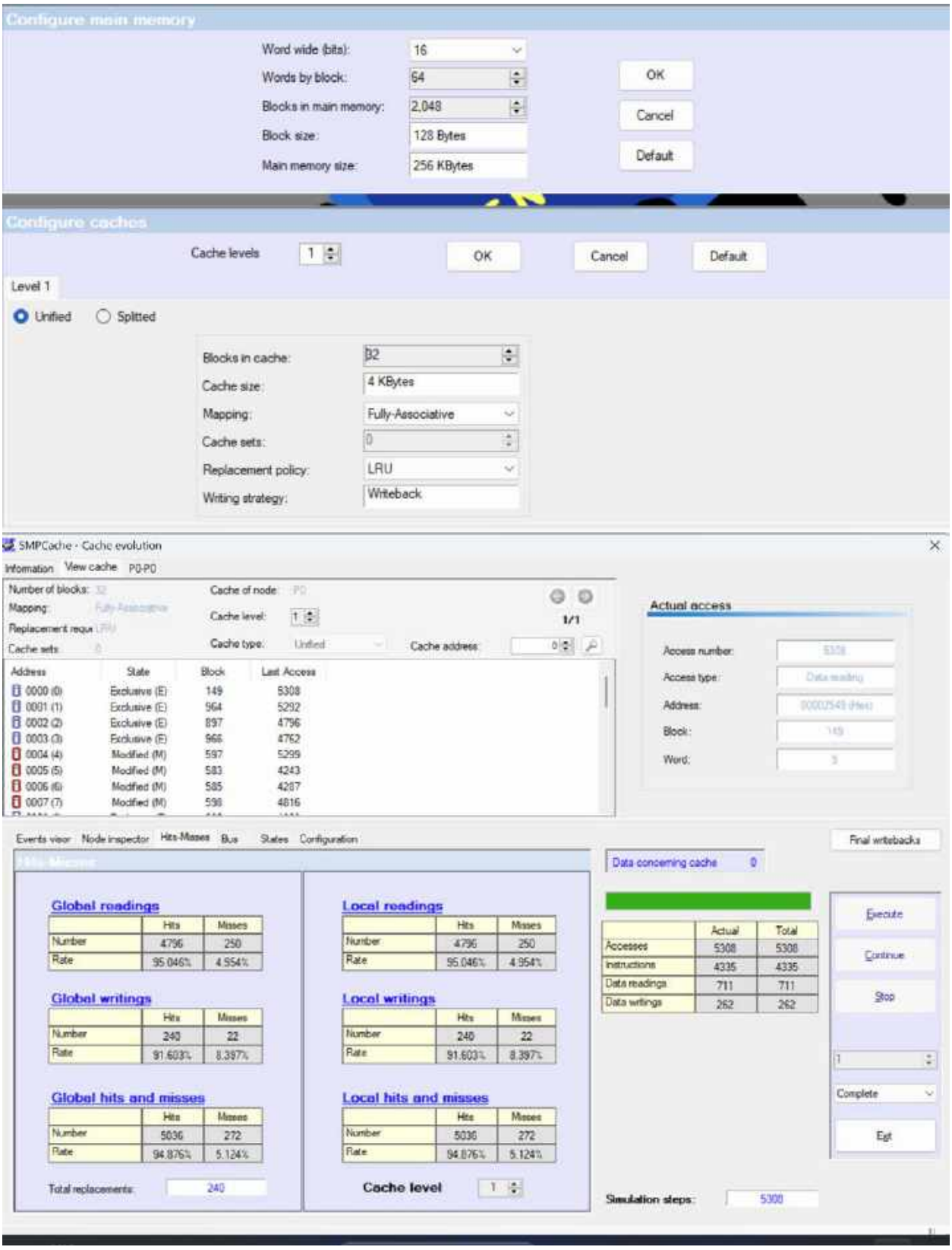

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 7702 4839
0001 (1) Exclusive (E) 6780 3811
0002 (2) Exclusive (E) 7698 4823
0003 (3) Modified (M) 4700 4830
0004 (4) Exclusive (E) 7699 4827
0005 (5) Modified (M) 4699 4832
0006 (6) Modified (M) 4701 4828
0007 (7) Exclusive (E) 7700 4831
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 4382 664
Rate 86.841% 13.159%
Global writings
Number 205 57
Rate 78.244% 21.756%
Global hits and misses
Number 4587 721
Rate 86.417% 13.583%
Total replacements: 465
Local readings
Number 4382 664
Rate 86.841% 13.159%
Local writings
Number 205 57
Rate 78.244% 21.756%
Local hits and misses
Number 4587 721
Rate 86.417% 13.583%
Cache level 1
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

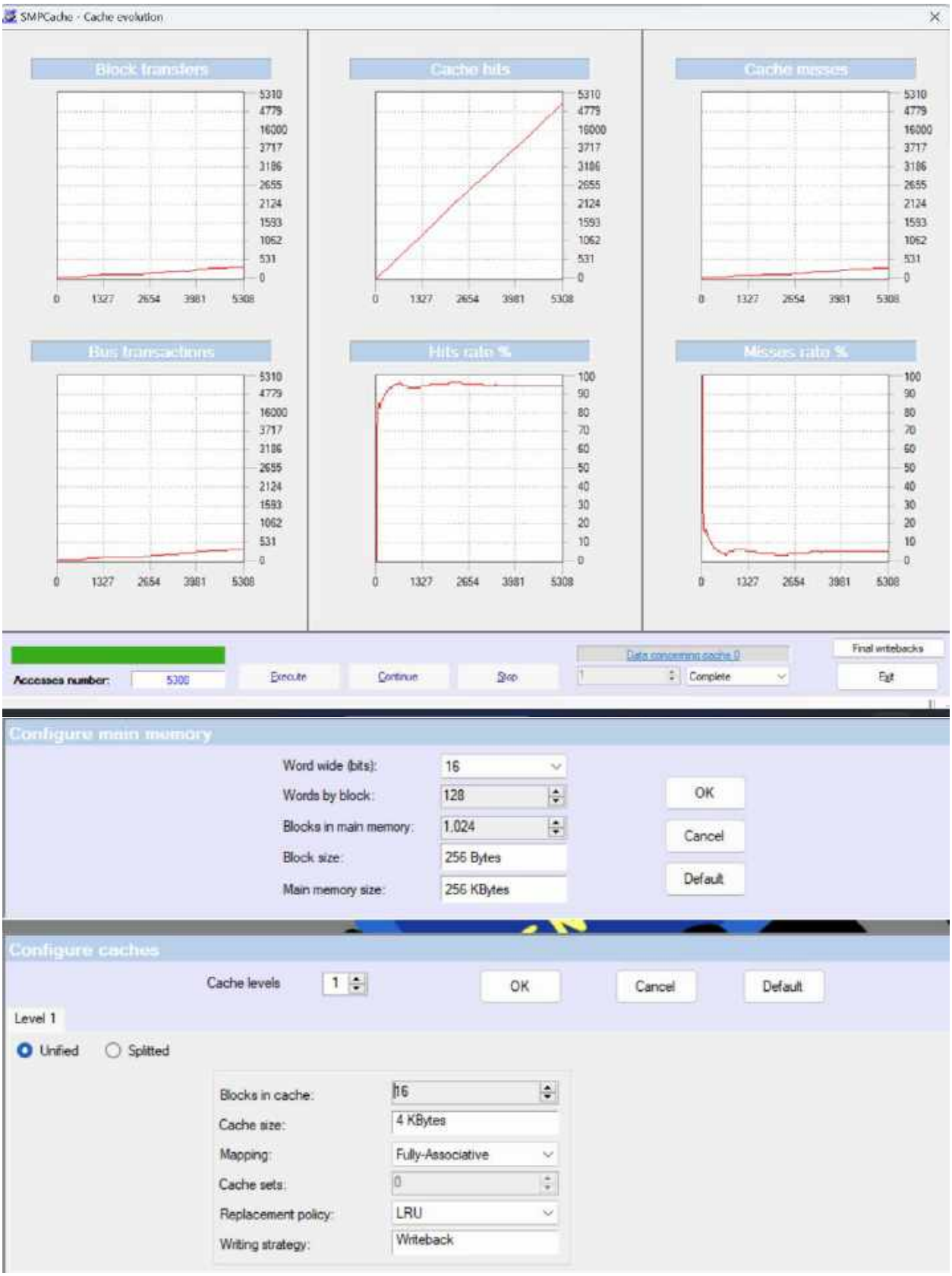

Configure main memory
Word wide (bits): 16
Words by block: 16
Blocks in main memory: 8,192
Block size: 32 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 128
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 128
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 3660 4070
0001 (1) Exclusive (E) 3662 4110
0002 (2) Exclusive (E) 3661 4074
0003 (3) Exclusive (E) 3664 4116
0004 (4) Modified (M) 2331 4184
0005 (5) Exclusive (E) 3654 4018
0006 (6) Exclusive (E) 3779 4177
0007 (7) Modified (M) 2348 4841
Actual access
Access number: 5308
Access type: Data reading
Address: 00002949 (hex)
Block: 536
Word: 9
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4552 494
Rate 90.210% 9.790%
Global writings
Hits Misses
Number 220 42
Rate 83.969% 16.031%
Global hits and misses
Hits Misses
Number 4772 536
Rate 89.902% 10.098%
Total replacements: 408
Local readings
Hits Misses
Number 4552 494
Rate 90.210% 9.790%
Local writings
Hits Misses
Number 220 42
Rate 83.969% 16.031%
Local hits and misses
Hits Misses
Number 4772 536
Rate 89.902% 10.098%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308

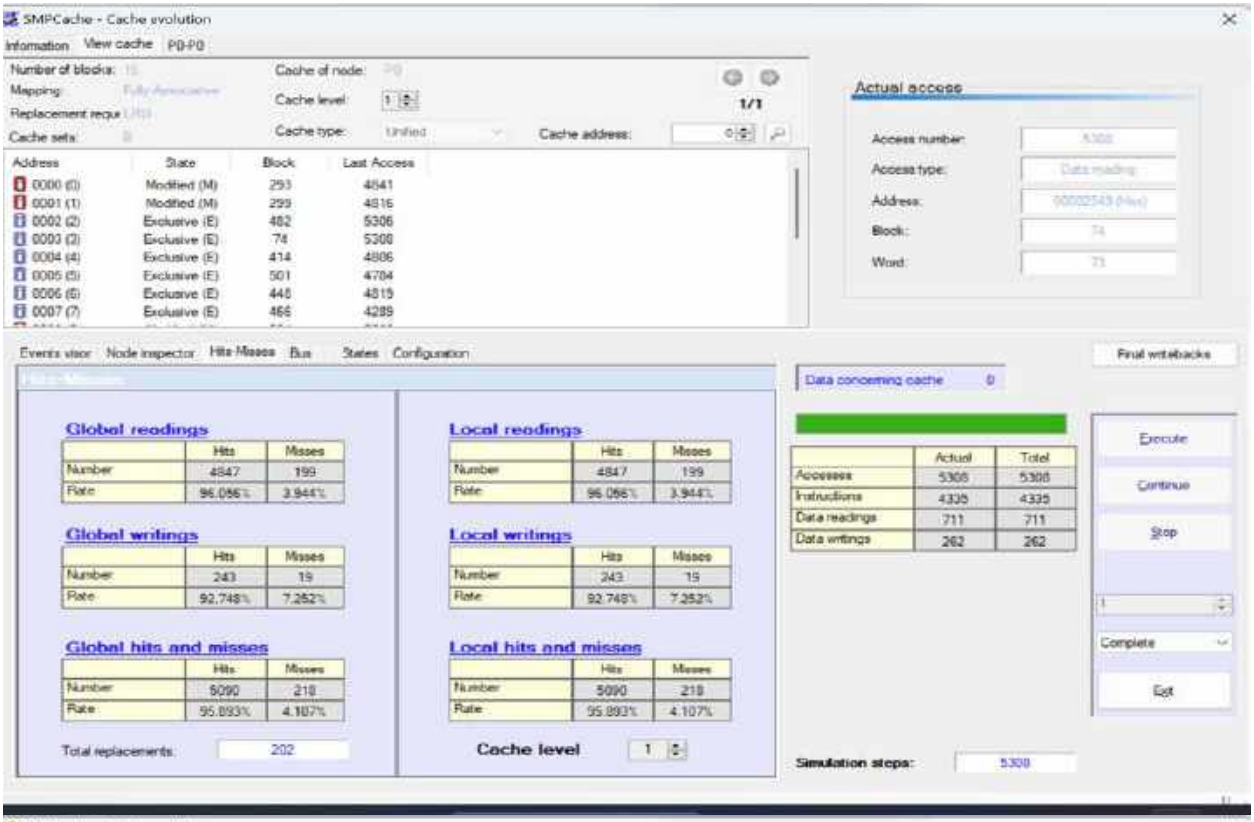

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
32
Blocks in main memory:
4.096
Block size:
64 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
64
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
Replacement policy:
LRU
Writing strategy:
Writeback

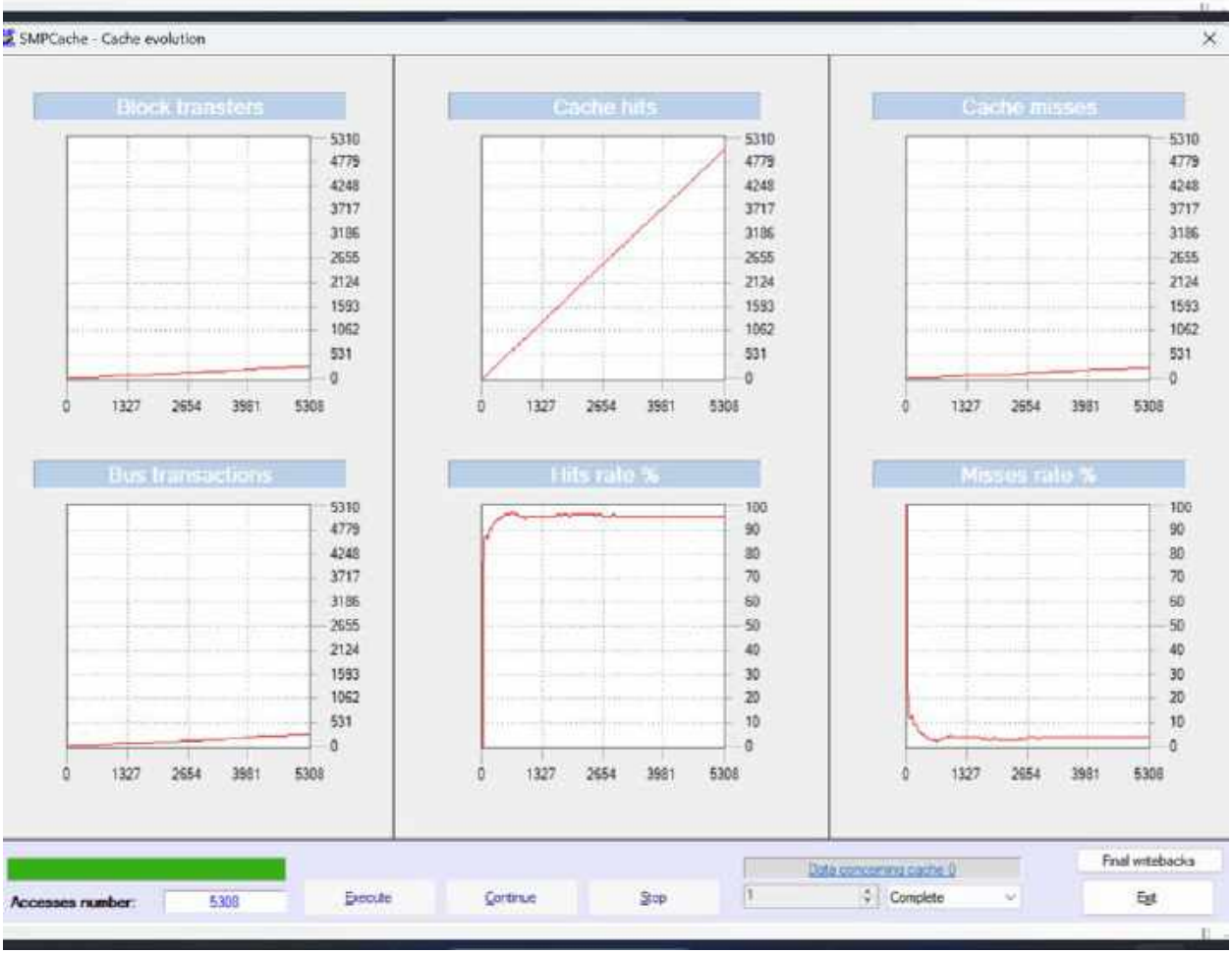

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 1195 4843
0001 (1) Exclusive (E) 1862 4262
0002 (2) Exclusive (E) 390 4803
0003 (3) Exclusive (E) 2004 4784
0004 (4) Exclusive (E) 1834 4134
0005 (5) Exclusive (E) 1836 4208
0006 (6) Exclusive (E) 1831 4115
0007 (7) Exclusive (E) 1658 4806
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4672 374
Rate 92.588% 7.412%
Global writings
Hits Misses
Number 230 32
Rate 87.786% 12.214%
Global hits and misses
Hits Misses
Number 4902 406
Rate 92.351% 7.649%
Total replacements: 342
Local readings
Hits Misses
Number 4672 374
Rate 92.588% 7.412%
Local writings
Hits Misses
Number 230 32
Rate 87.786% 12.214%
Local hits and misses
Hits Misses
Number 4902 406
Rate 92.351% 7.649%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308

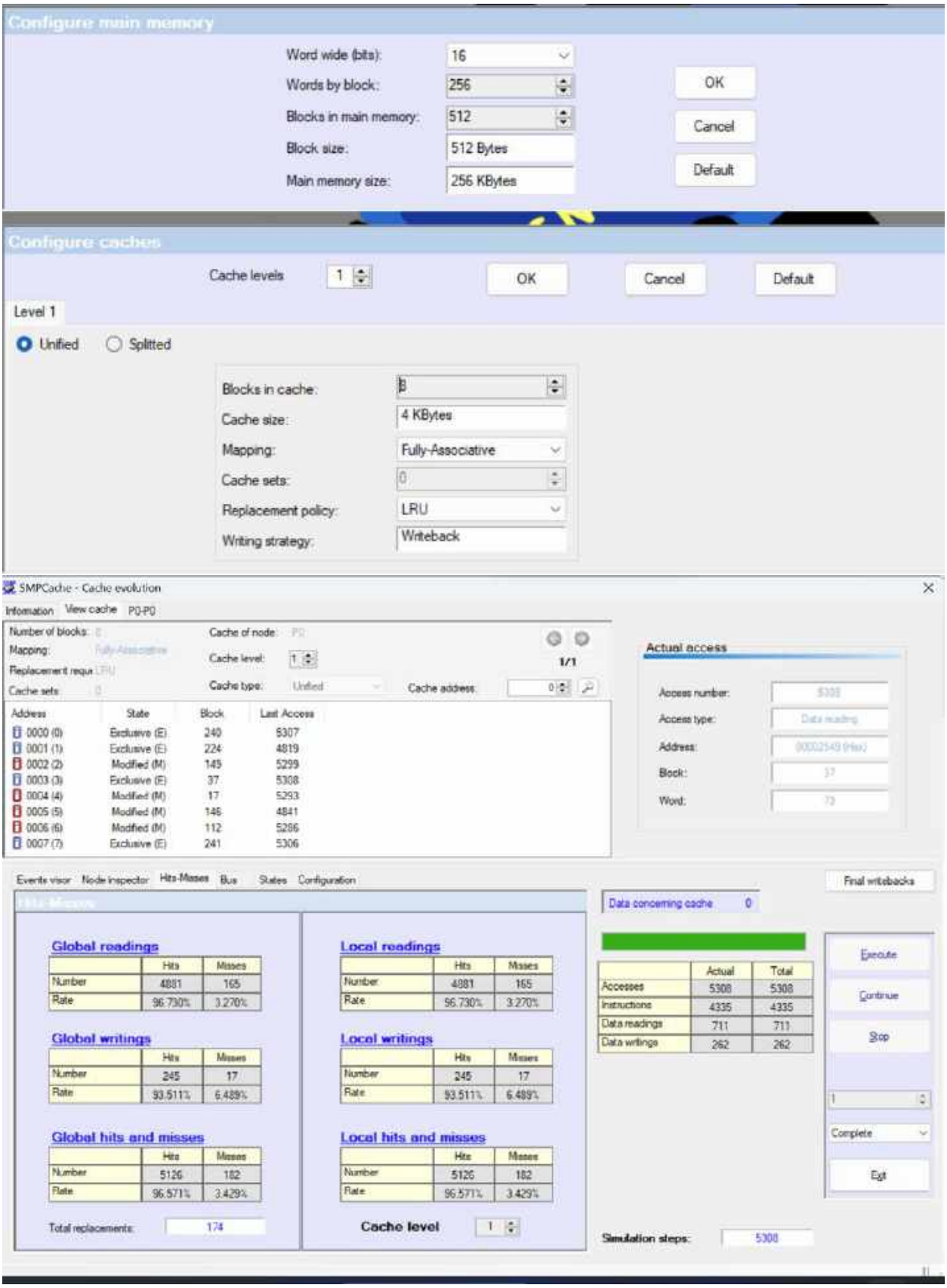

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0
1327
2654
3981
5308
Accesses number: 5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

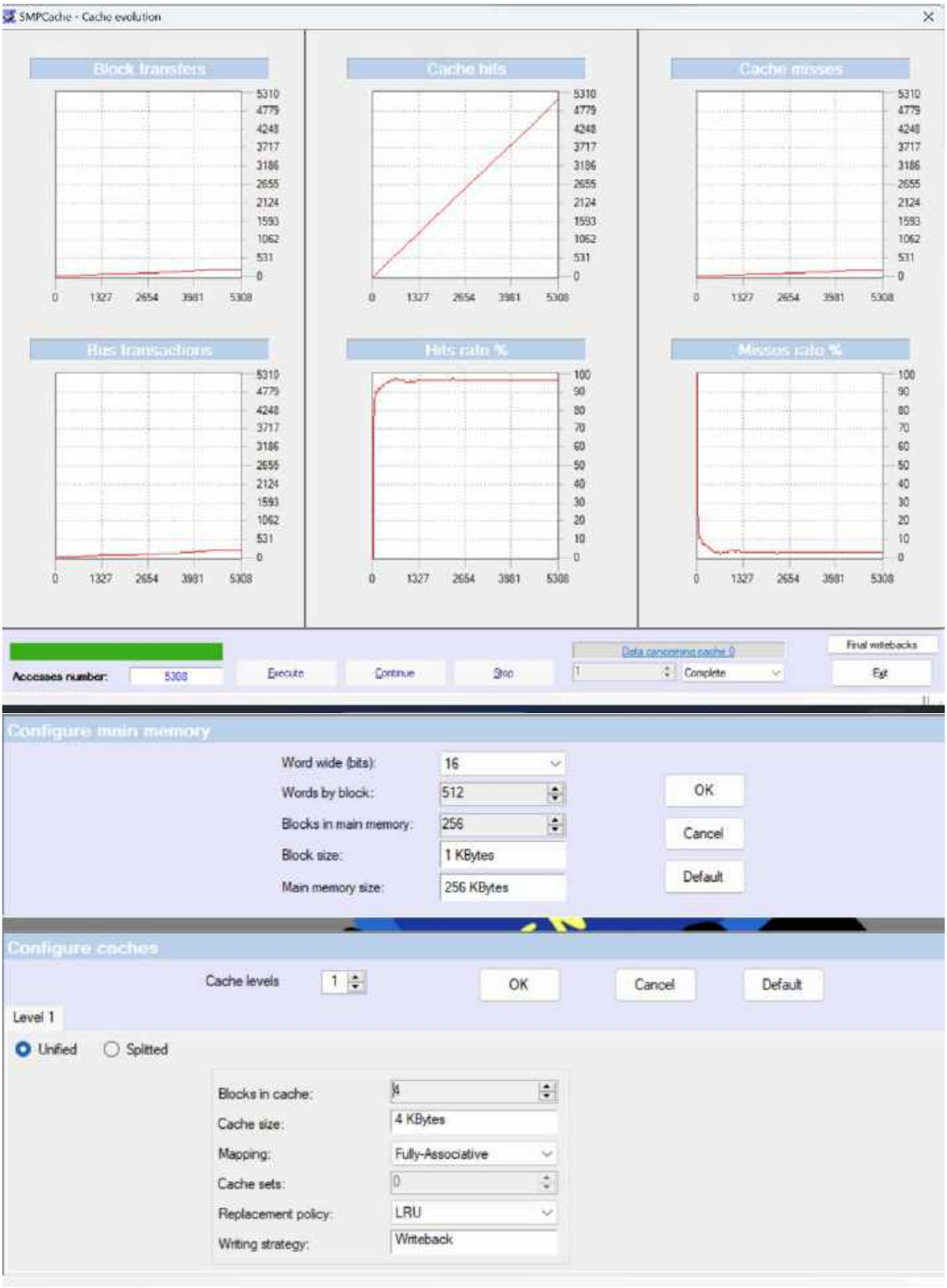

Configure main memory
Word wide (bits): 16
Words by block: 64
Blocks in main memory: 2,048
Block size: 128 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 32
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 32
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 149 5308
0001 (1) Exclusive (E) 964 5292
0002 (2) Exclusive (E) 897 4796
0003 (3) Exclusive (E) 966 4762
0004 (4) Modified (M) 597 5299
0005 (5) Modified (M) 583 4243
0006 (6) Modified (M) 585 4287
0007 (7) Modified (M) 598 4816
Actual access
Access number: 5308
Access type: Data reading
Address: 00002540 (hex)
Block: 149
Word: 3
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4796 250
Rate 95.046% 4.954%
Global writings
Hits Misses
Number 240 22
Rate 91.603% 8.397%
Global hits and misses
Hits Misses
Number 5036 272
Rate 94.876% 5.124%
Total replacements: 240
Local readings
Hits Misses
Number 4796 250
Rate 95.046% 4.954%
Local writings
Hits Misses
Number 240 22
Rate 91.603% 8.397%
Local hits and misses
Hits Misses
Number 5036 272
Rate 94.876% 5.124%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
128
Blocks in main memory:
1,024
Block size:
256 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
16
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

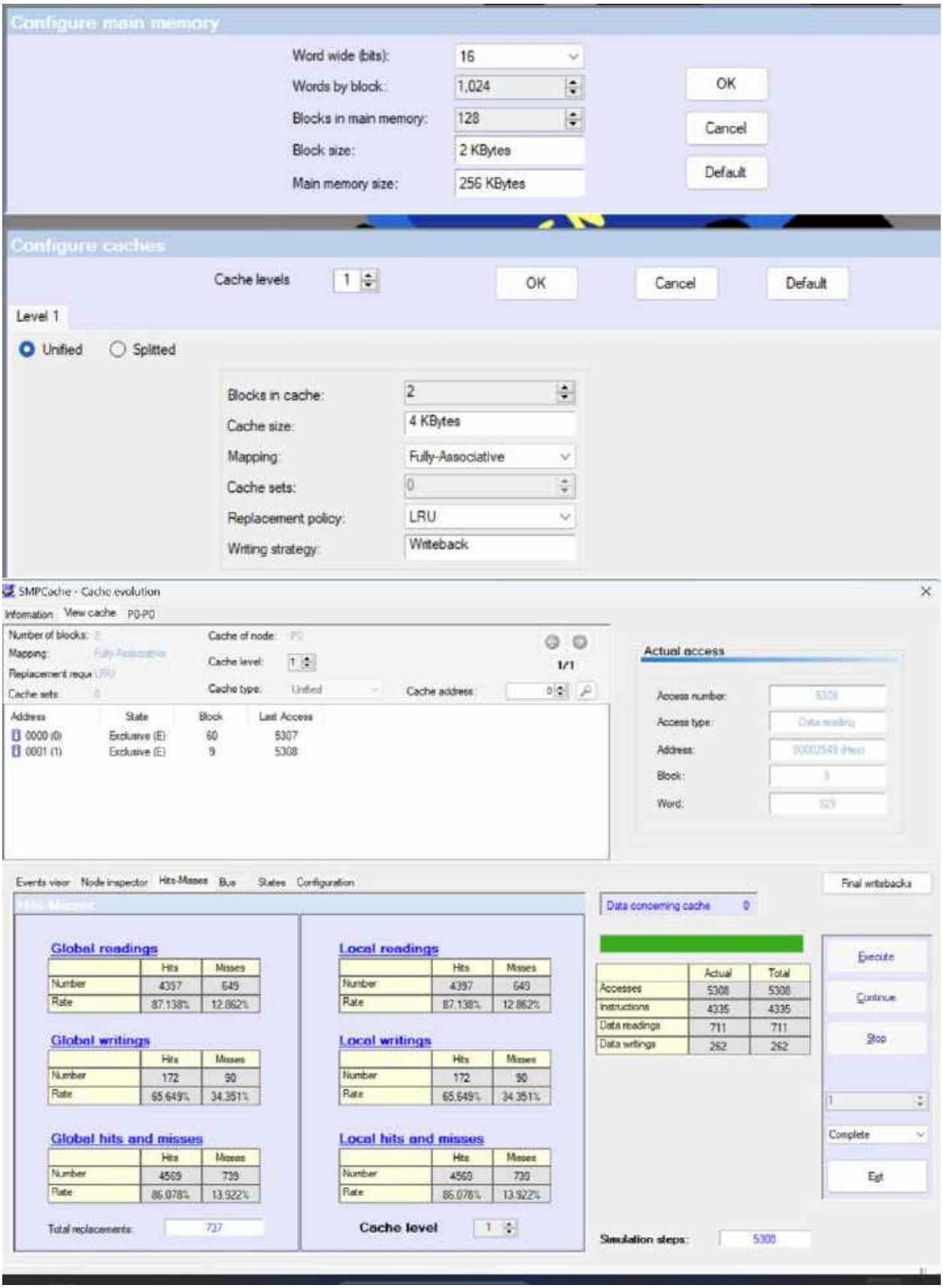

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Actual access
Access number:
Access type:
Address:
Block:
Word:
Address
State
Block
Last Access
0000 (0) Modified (M) 253 4841
0001 (1) Modified (M) 299 4816
0002 (2) Exclusive (E) 482 5306
0003 (3) Exclusive (E) 74 5308
0004 (4) Exclusive (E) 414 4806
0005 (5) Exclusive (E) 501 4784
0006 (6) Exclusive (E) 448 4815
0007 (7) Exclusive (E) 466 4289
Events view
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 4847 199
Rate 96.056% 3.944%
Global writings
Number 243 19
Rate 92.748% 7.252%
Global hits and misses
Number 5090 218
Rate 95.893% 4.107%
Total replacements: 202
Local readings
Number 4847 199
Rate 96.056% 3.944%
Local writings
Number 243 19
Rate 92.748% 7.252%
Local hits and misses
Number 5090 218
Rate 95.893% 4.107%
Cache level 1
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
5310
4779
4248
3717
3186
2655
2124
1593
1062
531
0
1327
2654
3981
5308
100
90
80
70
60
50
40
30
20
10
Accesses number: 5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

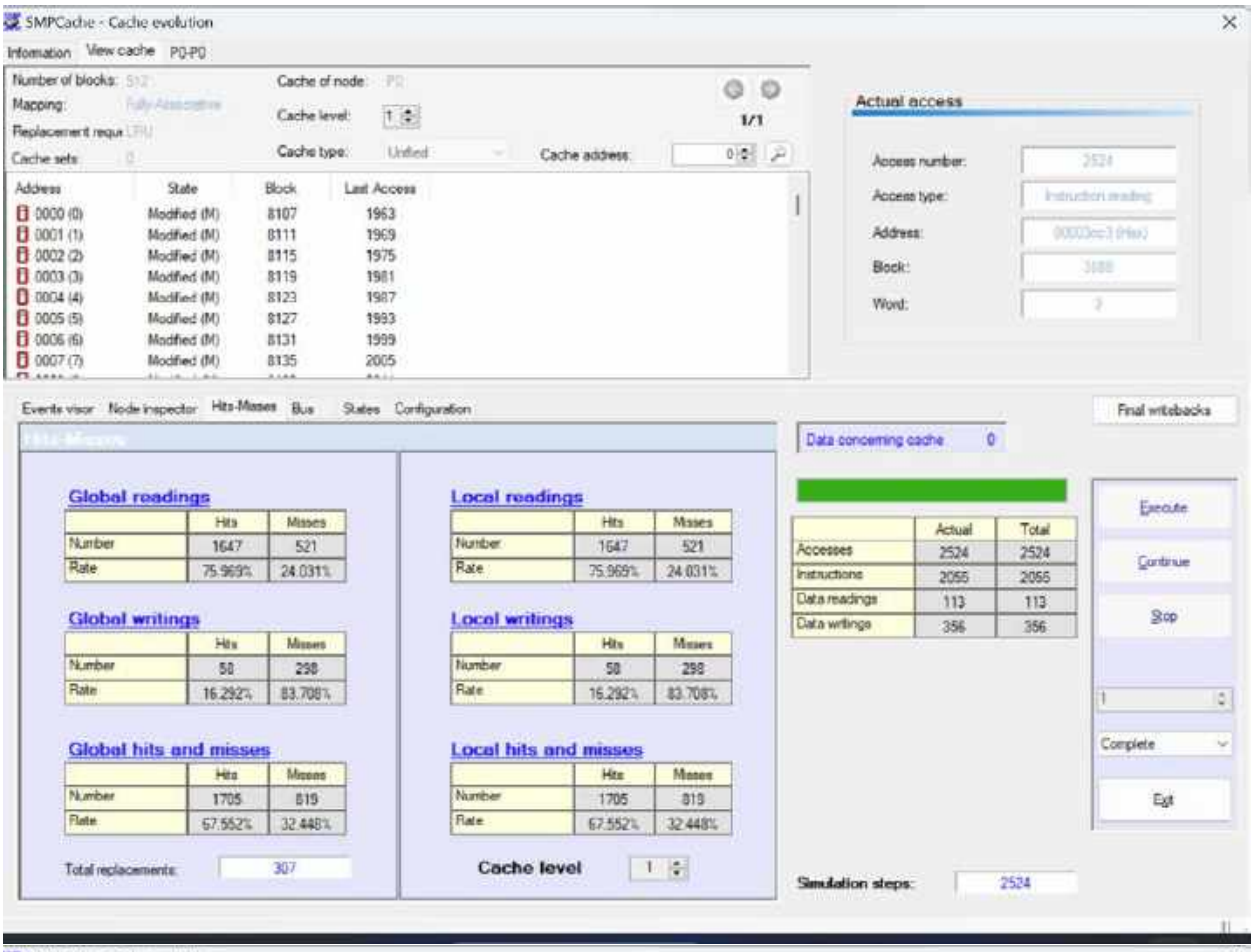

Configure main memory
Word wide (bits): 16
Words by block: 256
Blocks in main memory: 512
Block size: 512 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 8
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 240 5307
0001 (1) Exclusive (E) 224 4819
0002 (2) Modified (M) 145 5299
0003 (3) Exclusive (E) 37 5308
0004 (4) Modified (M) 17 5293
0005 (5) Modified (M) 146 4841
0006 (6) Modified (M) 112 5286
0007 (7) Exclusive (E) 241 5306
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4881 165
Rate 96.730% 3.270%
Global writings
Hits Misses
Number 245 17
Rate 93.511% 6.489%
Global hits and misses
Hits Misses
Number 5126 182
Rate 96.571% 3.429%
Total replacements: 174
Local readings
Hits Misses
Number 4881 165
Rate 96.730% 3.270%
Local writings
Hits Misses
Number 245 17
Rate 93.511% 6.489%
Local hits and misses
Hits Misses
Number 5126 182
Rate 96.571% 3.429%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308

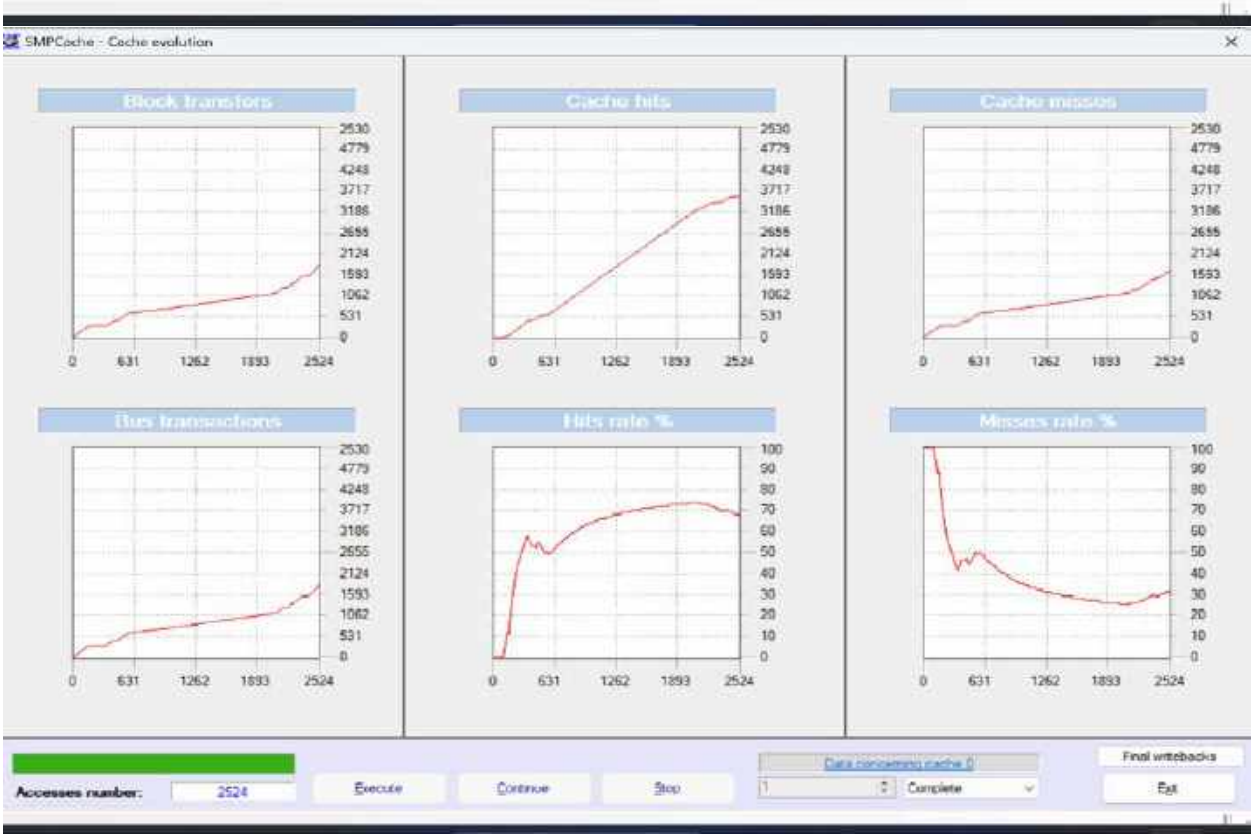

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
512
Blocks in main memory:
256
Block size:
1 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
4
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 4
Mapping:
Replacement requ
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 120 5307
0001 (1) Modified (M) 8 5293
0002 (2) Modified (M) 74 5299
0003 (3) Exclusive (E) 18 5308
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 4782 264
Rate 94.768% 5.232%
Global writings
Number 153 69
Rate 73.664% 26.336%
Global hits and misses
Number 4975 333
Rate 93.726% 6.274%
Total replacements: 329
Local readings
Number 4782 264
Rate 94.768% 5.232%
Local writings
Number 153 69
Rate 73.664% 26.336%
Local hits and misses
Number 4975 333
Rate 93.726% 6.274%
Cache level 1
Actual
Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
Complete
Exit
Simulation steps: 5308
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

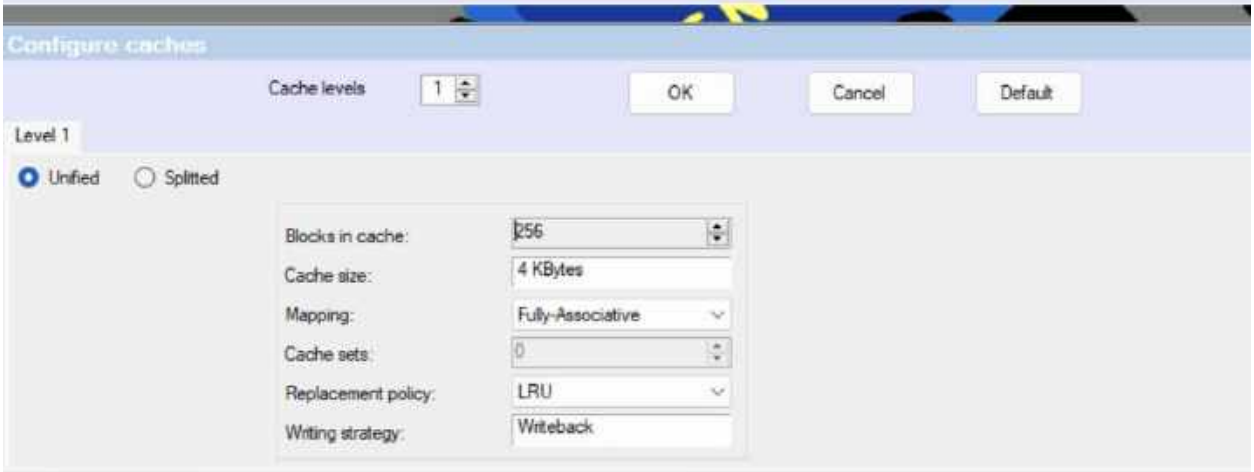

Configure main memory
Word wide (bits): 16
Words by block: 1,024
Blocks in main memory: 128
Block size: 2 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 2
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 60 5307
0001 (1) Exclusive (E) 9 5308
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor Node inspector Hits-Misses Bus States Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 4397 649
Rate 87.138% 12.862%
Global writings
Hits Misses
Number 172 90
Rate 65.649% 34.351%
Global hits and misses
Hits Misses
Number 4569 739
Rate 86.078% 13.922%
Total replacements: 737
Local readings
Hits Misses
Number 4397 649
Rate 87.138% 12.862%
Local writings
Hits Misses
Number 172 90
Rate 65.649% 34.351%
Local hits and misses
Hits Misses
Number 4569 739
Rate 86.078% 13.922%
Cache level 1
Actual Total
Accesses 5308 5308
Instructions 4335 4335
Data readings 711 711
Data writings 262 262
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 5308

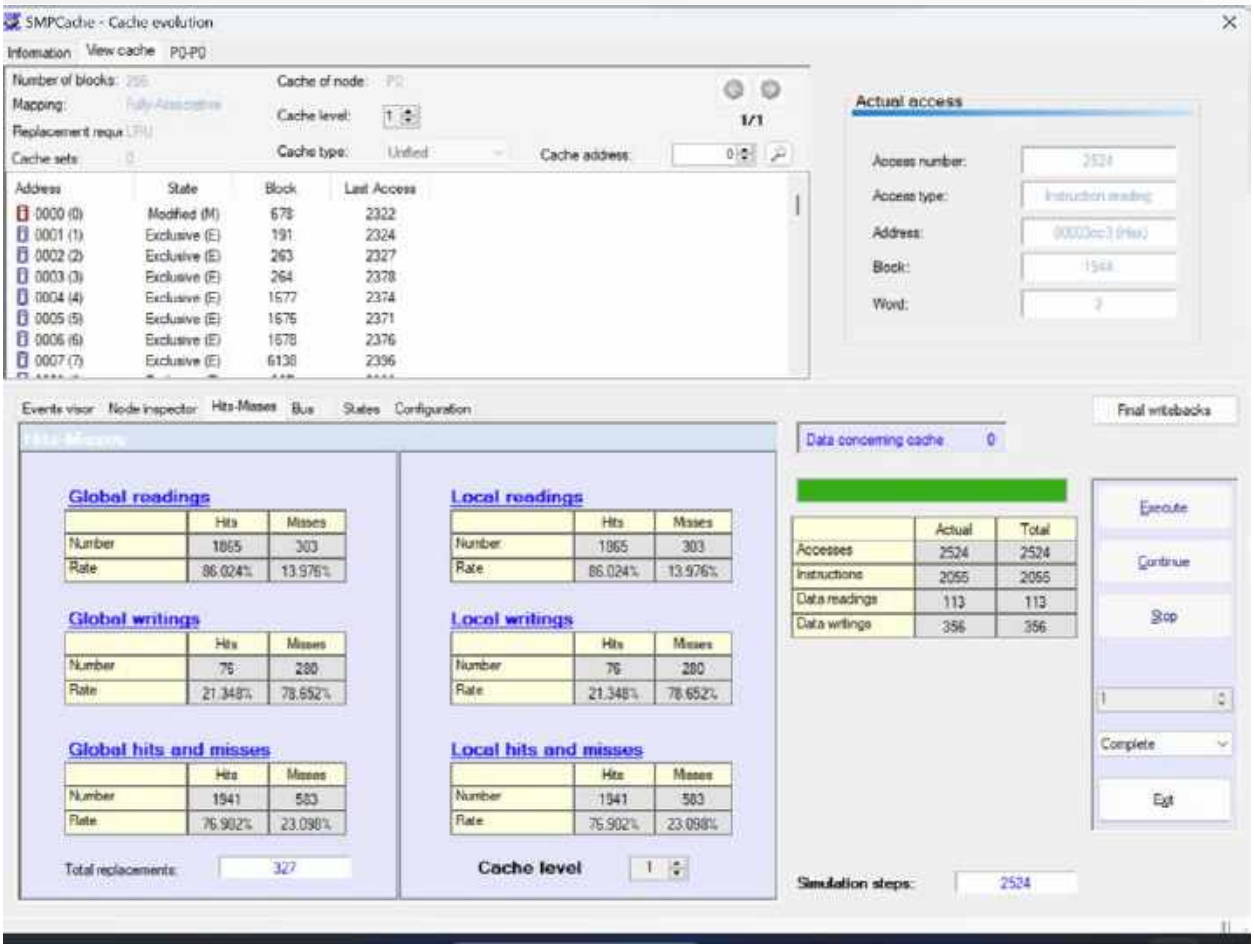
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
5308
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
4
Blocks in main memory:
32,768
Block size:
8 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
512
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

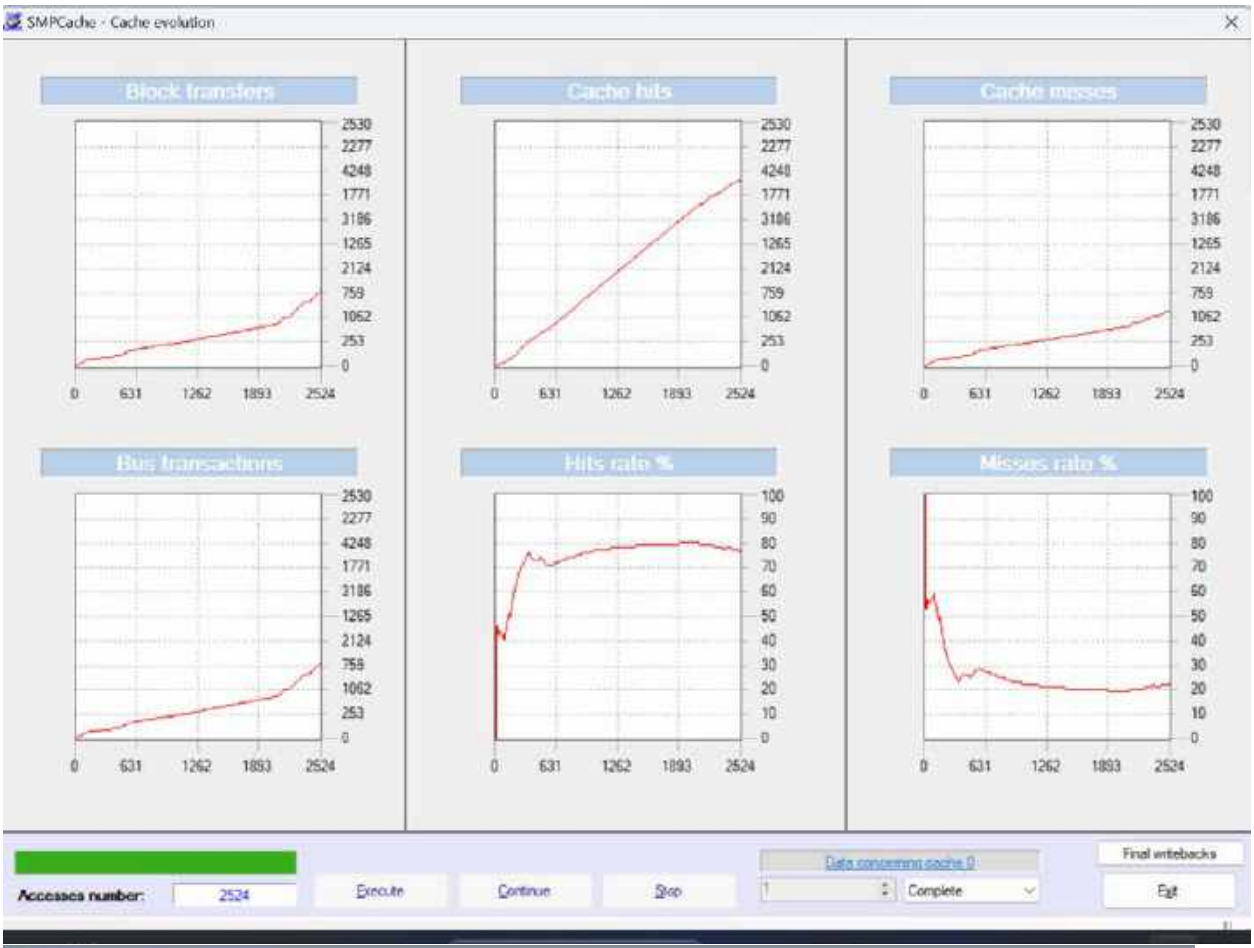

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 8107 1963
0001 (1) Modified (M) 8111 1969
0002 (2) Modified (M) 8115 1975
0003 (3) Modified (M) 8119 1981
0004 (4) Modified (M) 8123 1987
0005 (5) Modified (M) 8127 1993
0006 (6) Modified (M) 8131 1999
0007 (7) Modified (M) 8135 2005
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 1647 521
Rate 75.969% 24.031%
Global writings
Number 58 298
Rate 16.292% 83.708%
Global hits and misses
Number 1705 819
Rate 67.552% 32.448%
Total replacements: 307
Local readings
Number 1647 521
Rate 75.969% 24.031%
Local writings
Number 58 298
Rate 16.292% 83.708%
Local hits and misses
Number 1705 819
Rate 67.552% 32.448%
Cache level 1
Actual
Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2524

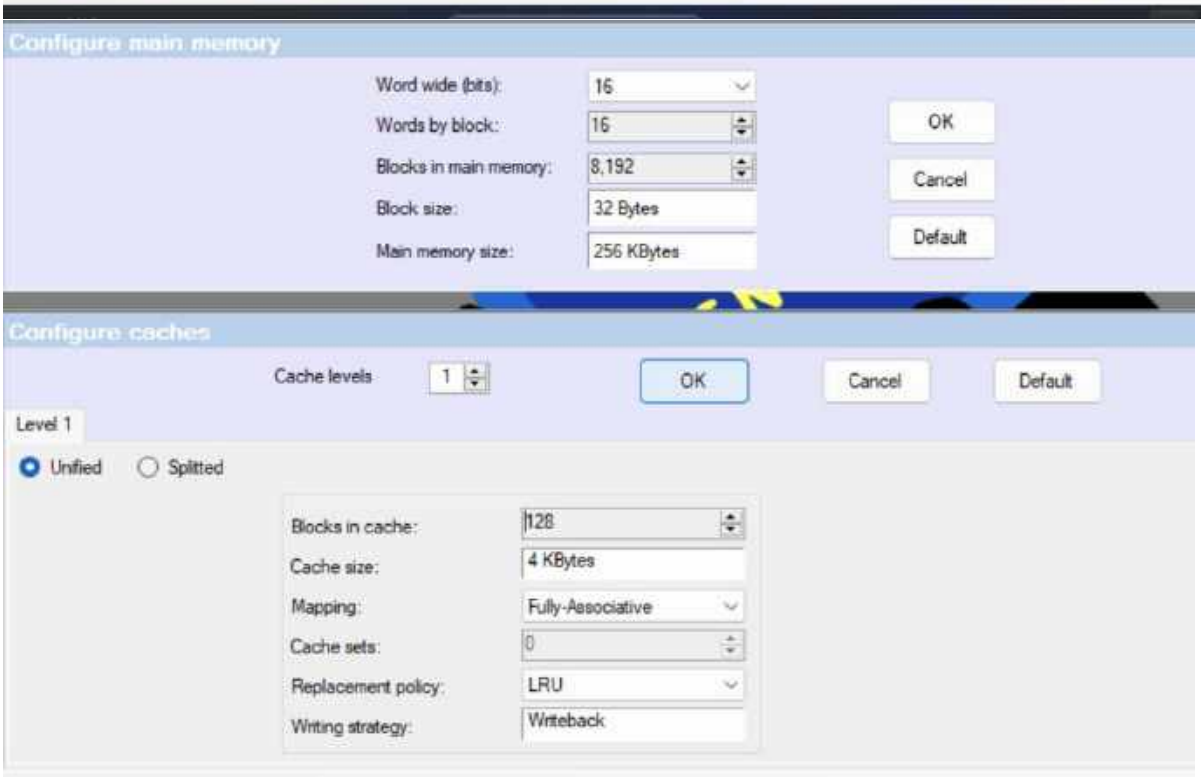

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 631 1262 1893 2524
Accesses number: 2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

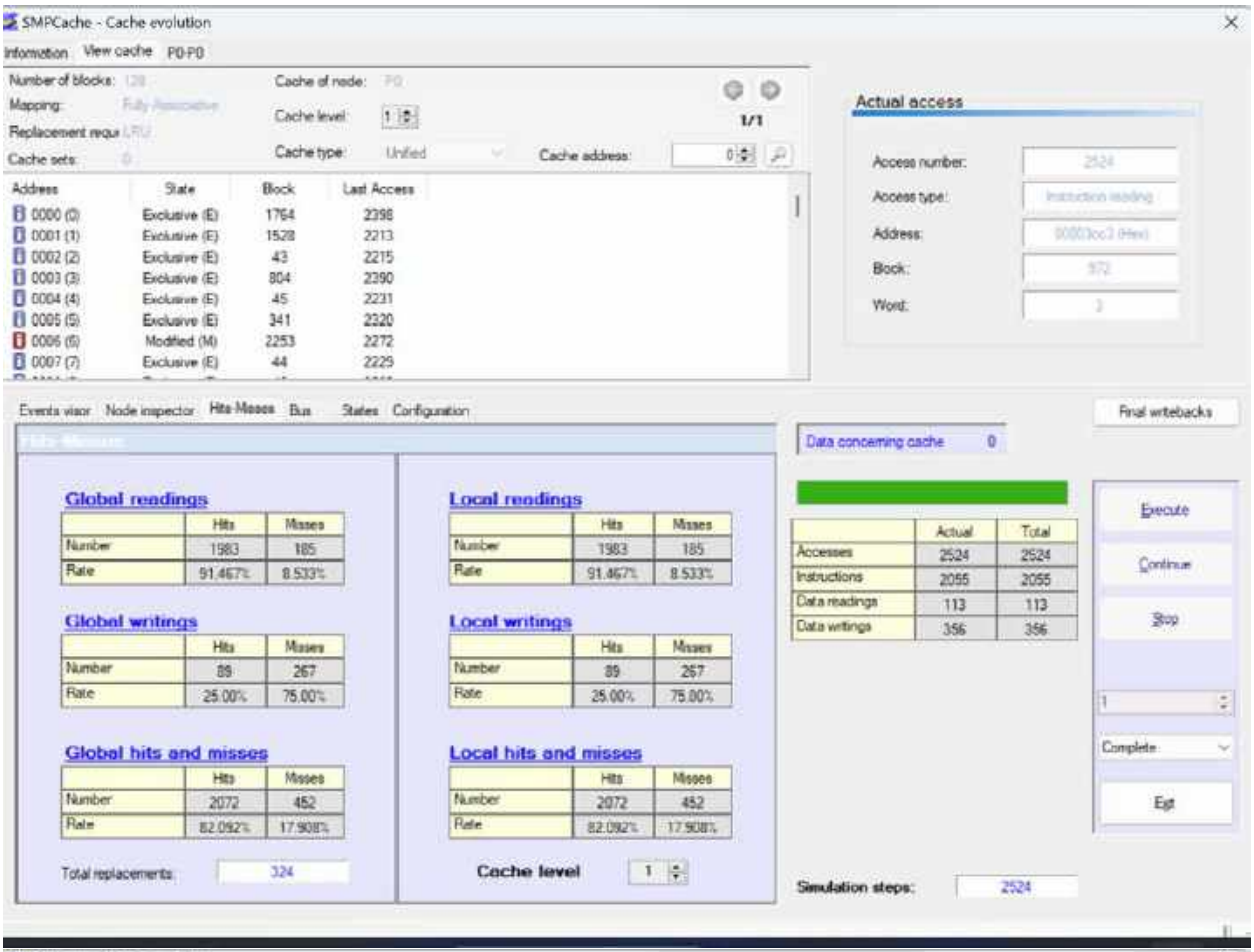
Configure main memory
Word wide (bits): 16
Words by block: 8
Blocks in main memory: 16.384
Block size: 16 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default

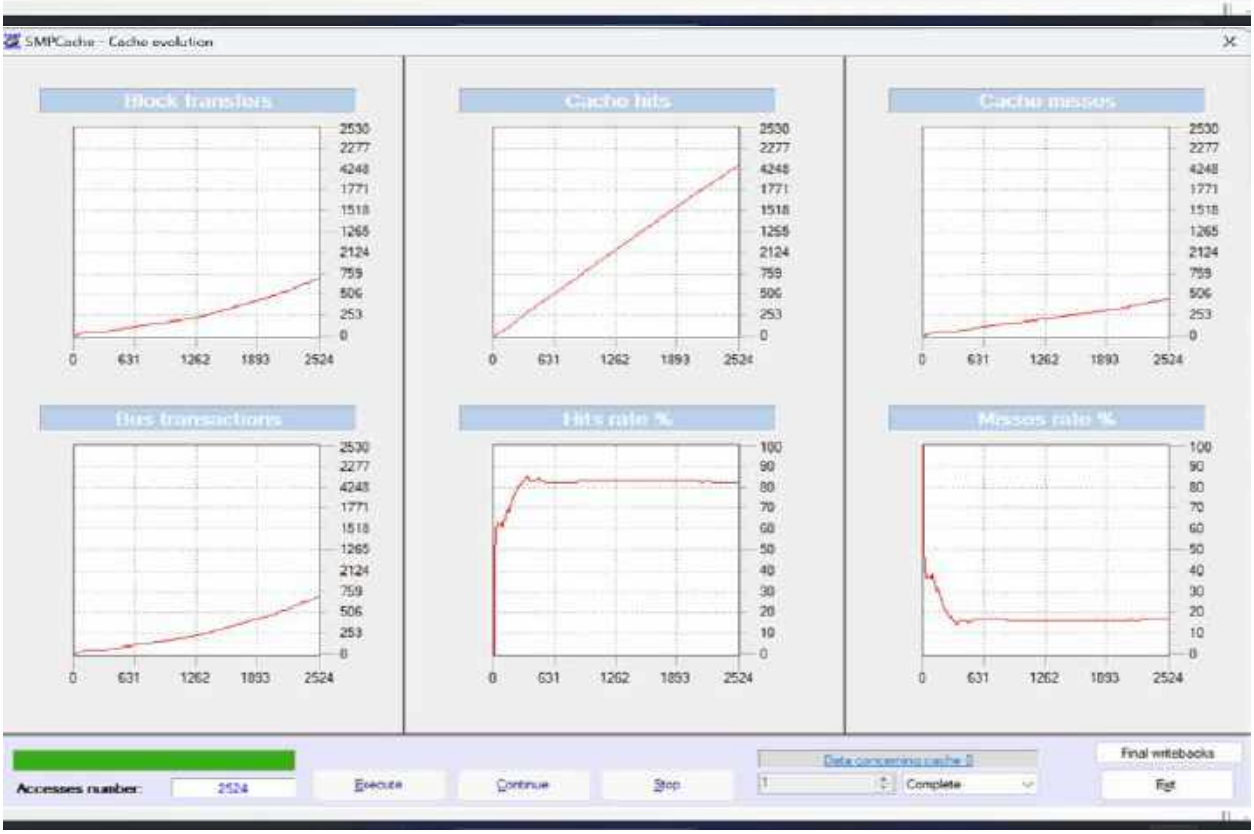

Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 256
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

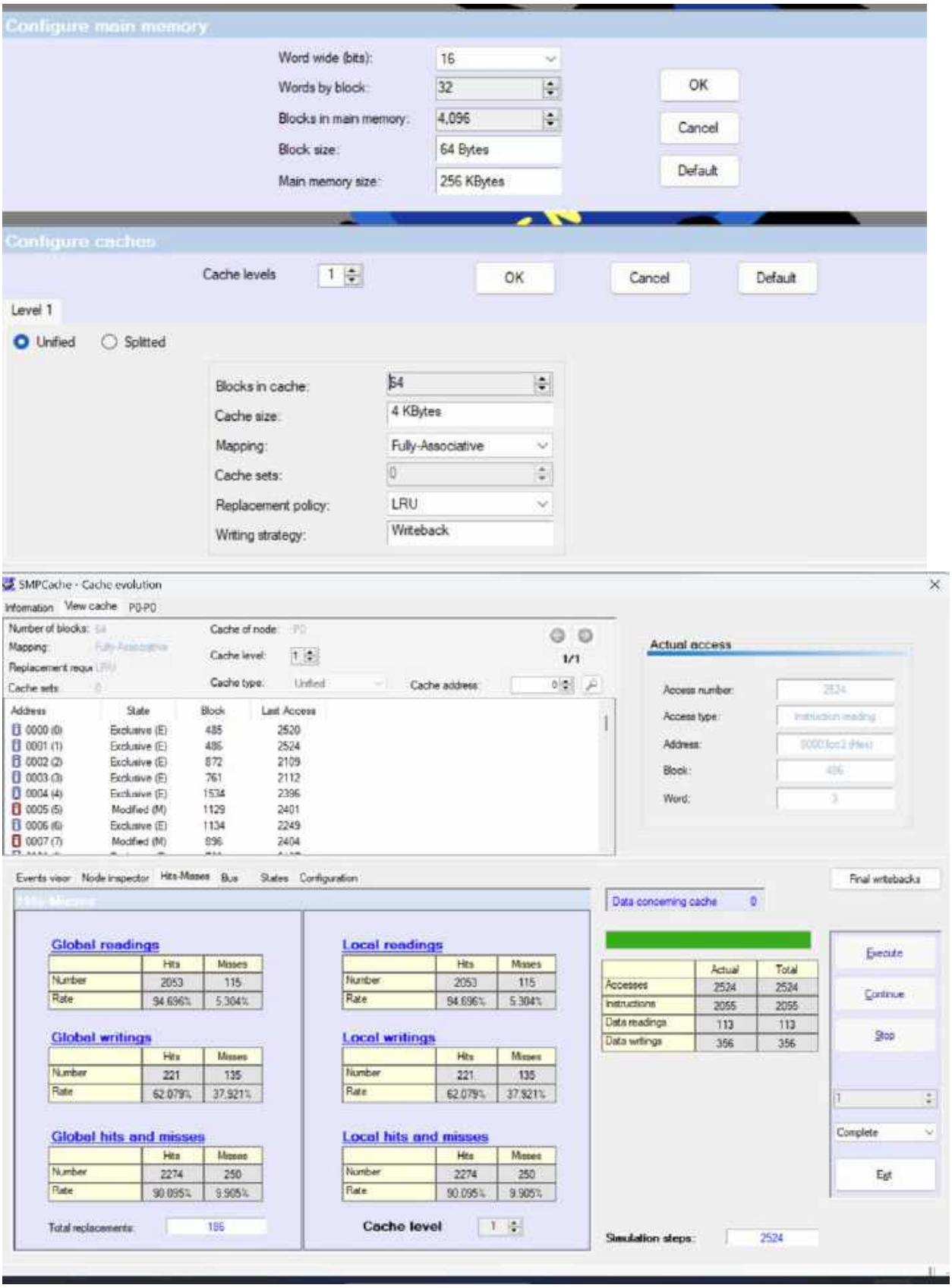

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 256
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 678 2322
0001 (1) Exclusive (E) 191 2324
0002 (2) Exclusive (E) 263 2327
0003 (3) Exclusive (E) 264 2378
0004 (4) Exclusive (E) 1677 2374
0005 (5) Exclusive (E) 1676 2371
0006 (6) Exclusive (E) 1678 2376
0007 (7) Exclusive (E) 6138 2396
Actual access
Access number: 2524
Access type: Instruction reading
Address: 0000ec3 (Hex)
Block: 1544
Word: 2
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Hits-Misses
Global readings
Hits Misses
Number 1865 303
Rate 86.024% 13.976%
Global writings
Hits Misses
Number 76 280
Rate 21.348% 78.652%
Global hits and misses
Hits Misses
Number 1941 583
Rate 76.902% 23.098%
Total replacements: 327
Local readings
Hits Misses
Number 1865 303
Rate 86.024% 13.976%
Local writings
Hits Misses
Number 76 280
Rate 21.348% 78.652%
Local hits and misses
Hits Misses
Number 1941 583
Rate 76.902% 23.098%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Final writebacks
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2524

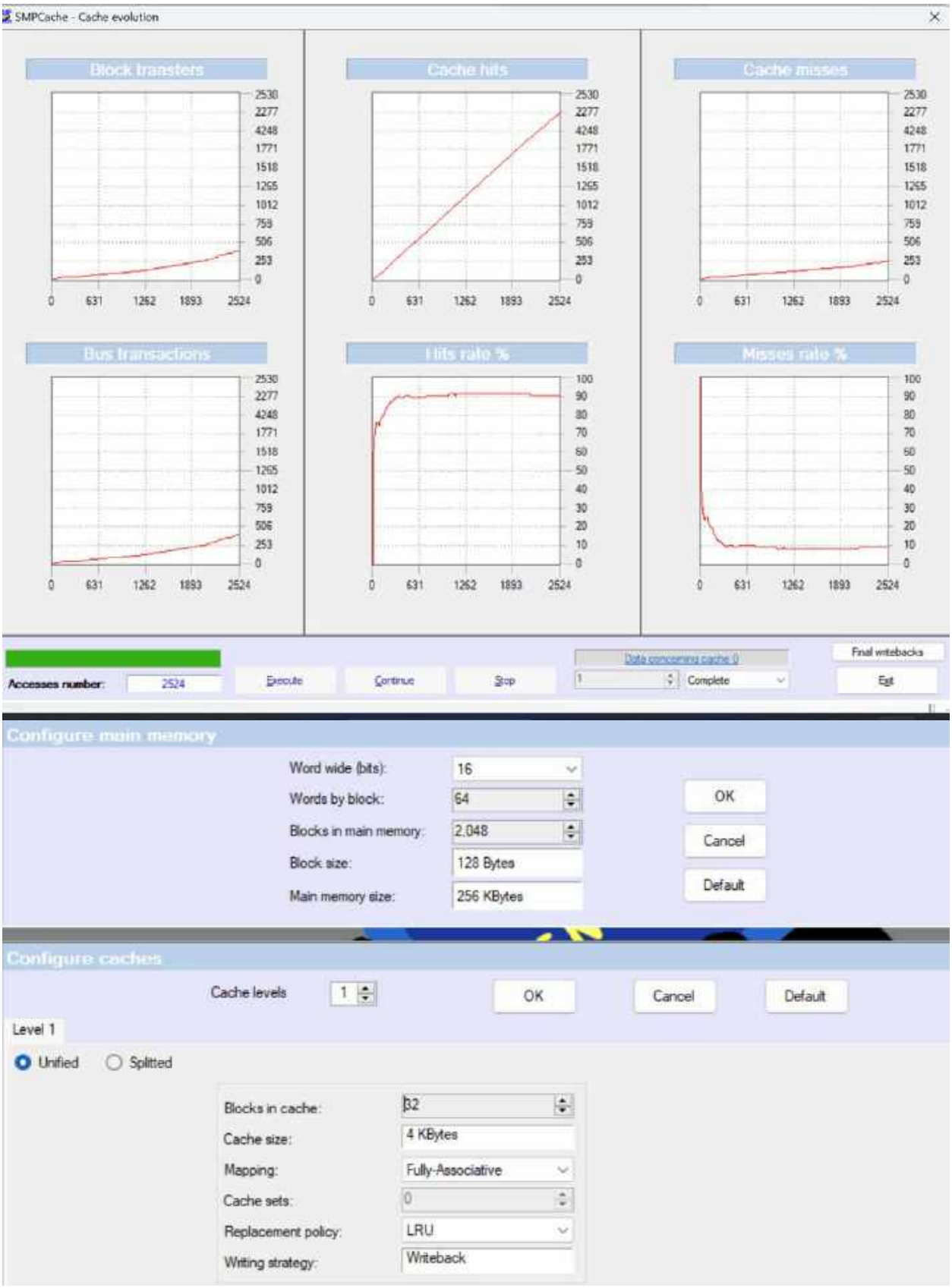

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

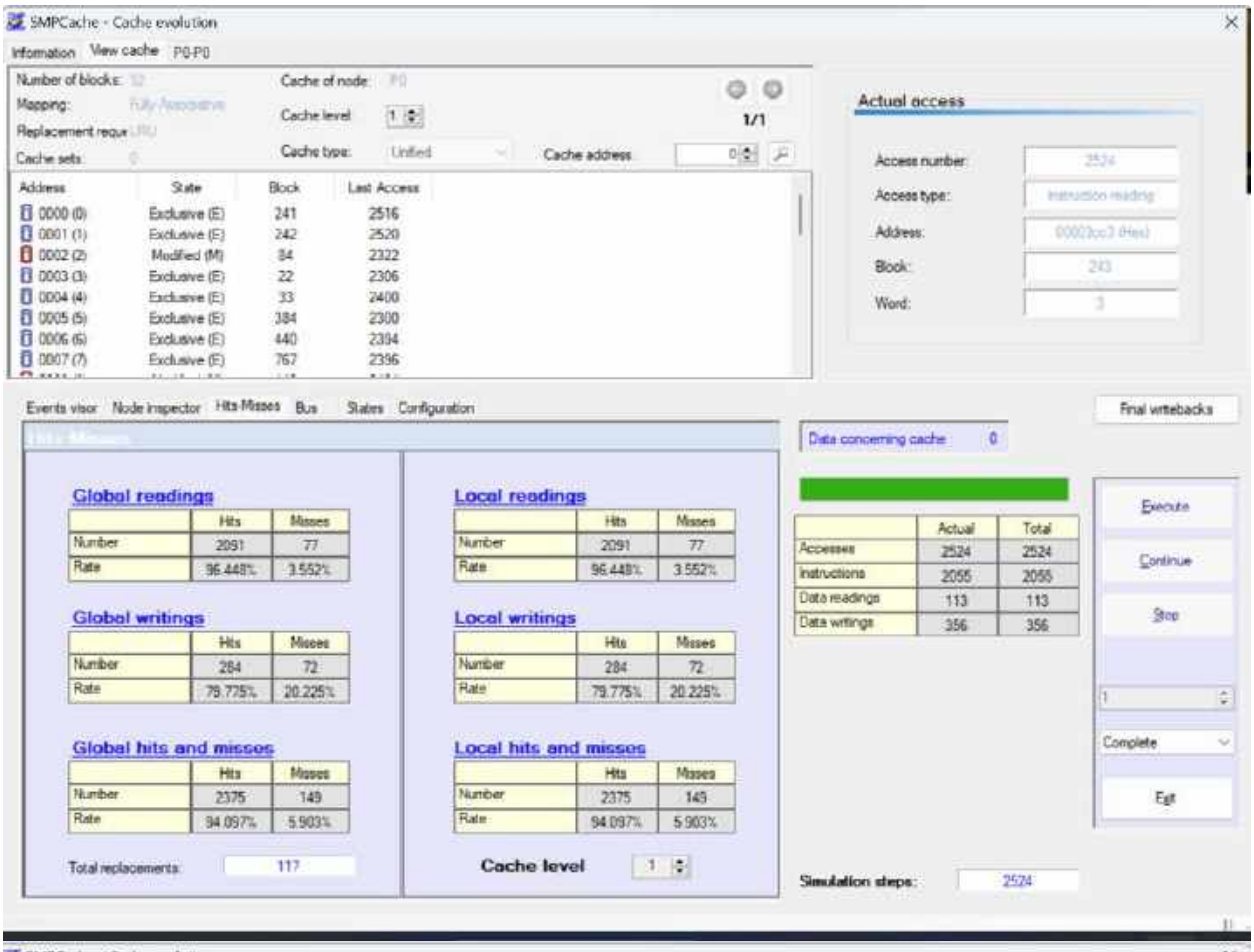

Configure main memory
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8,192
Block size:
32 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

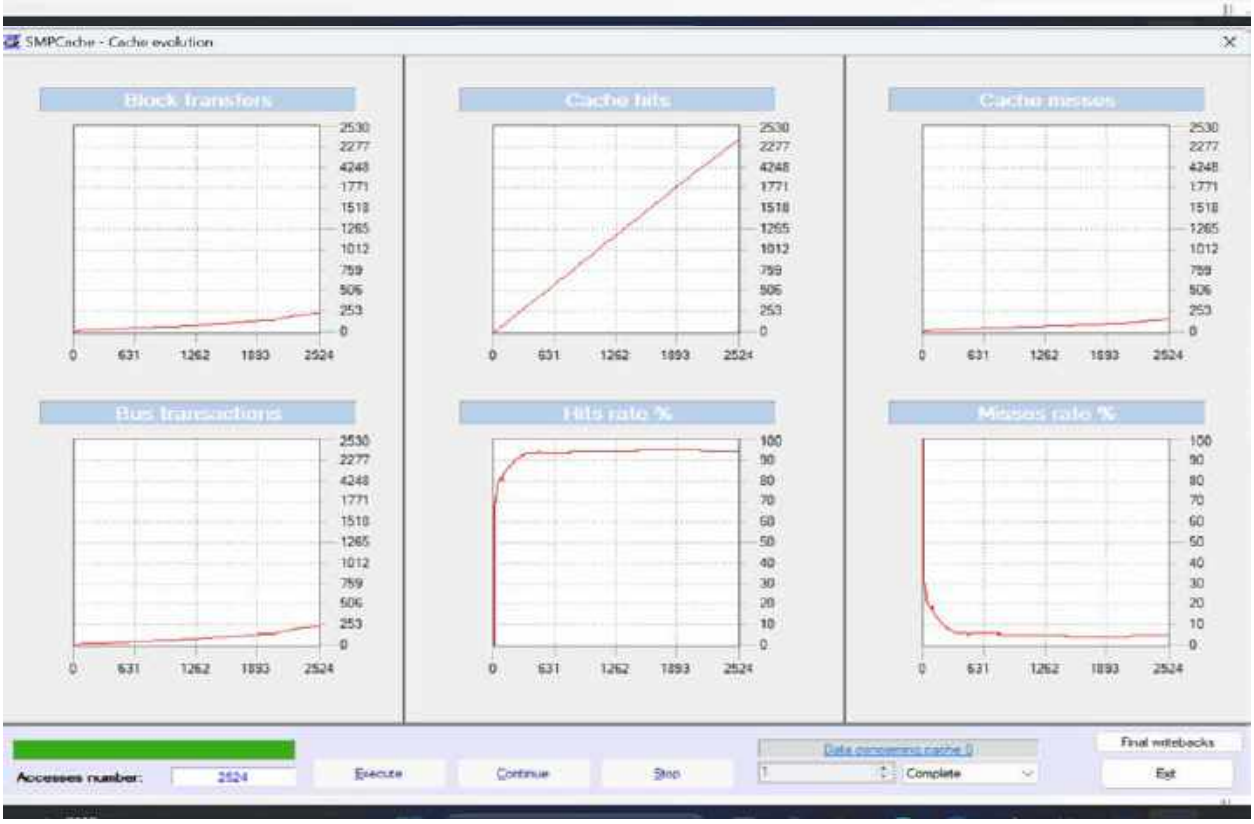

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 1764 2398
0001 (1) Exclusive (E) 1528 2213
0002 (2) Exclusive (E) 43 2215
0003 (3) Exclusive (E) 804 2390
0004 (4) Exclusive (E) 45 2231
0005 (5) Exclusive (E) 341 2320
0006 (6) Modified (M) 2253 2272
0007 (7) Exclusive (E) 44 2229
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1983 185
Rate 91.467% 8.533%
Global writings
Hits Misses
Number 89 267
Rate 25.00% 75.00%
Global hits and misses
Hits Misses
Number 2072 452
Rate 82.092% 17.908%
Total replacements: 324
Local readings
Hits Misses
Number 1983 185
Rate 91.467% 8.533%
Local writings
Hits Misses
Number 89 267
Rate 25.00% 75.00%
Local hits and misses
Hits Misses
Number 2072 452
Rate 82.092% 17.908%
Cache level 1
Actual Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2524

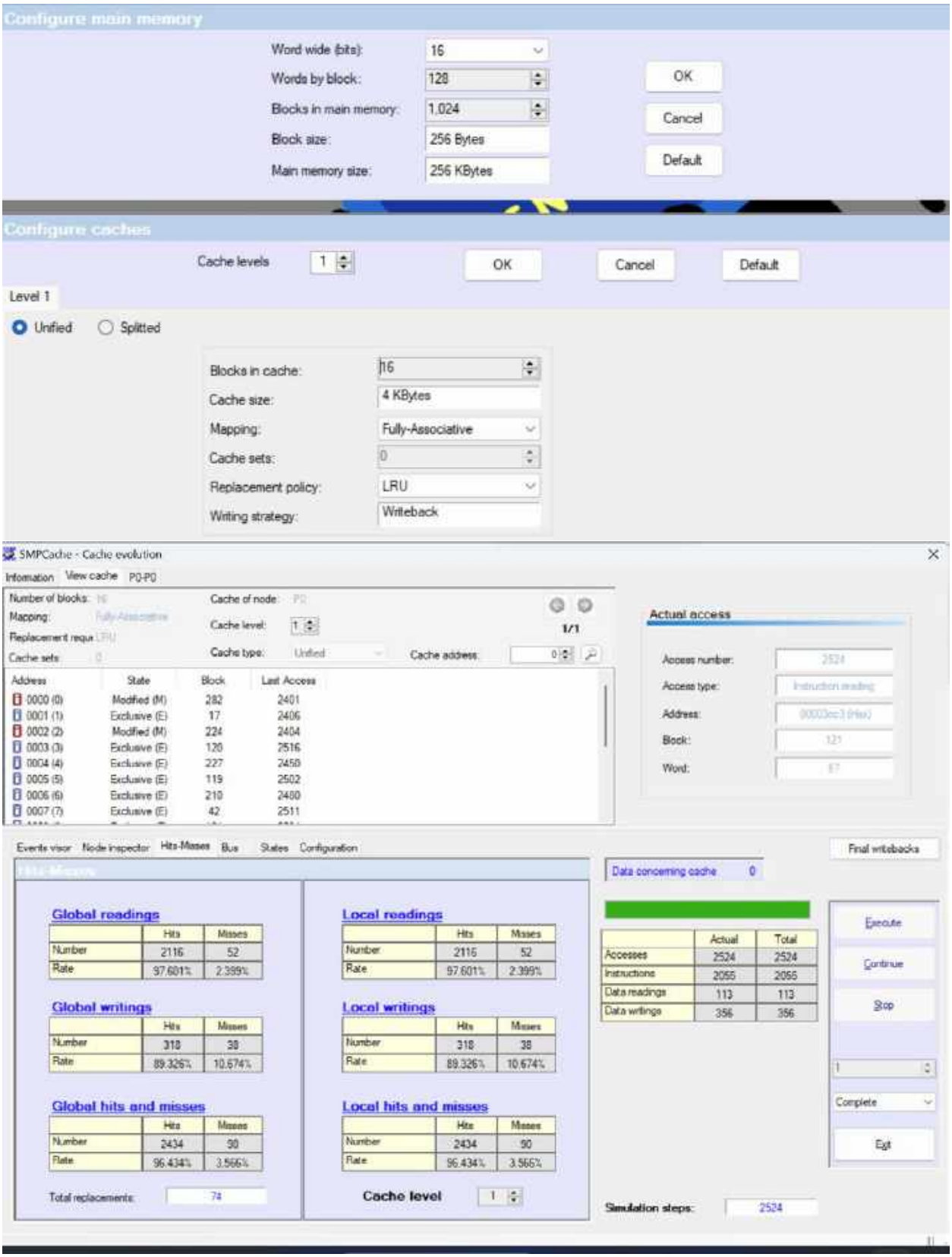

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 631 1262 1893 2524
Accesses number: 2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

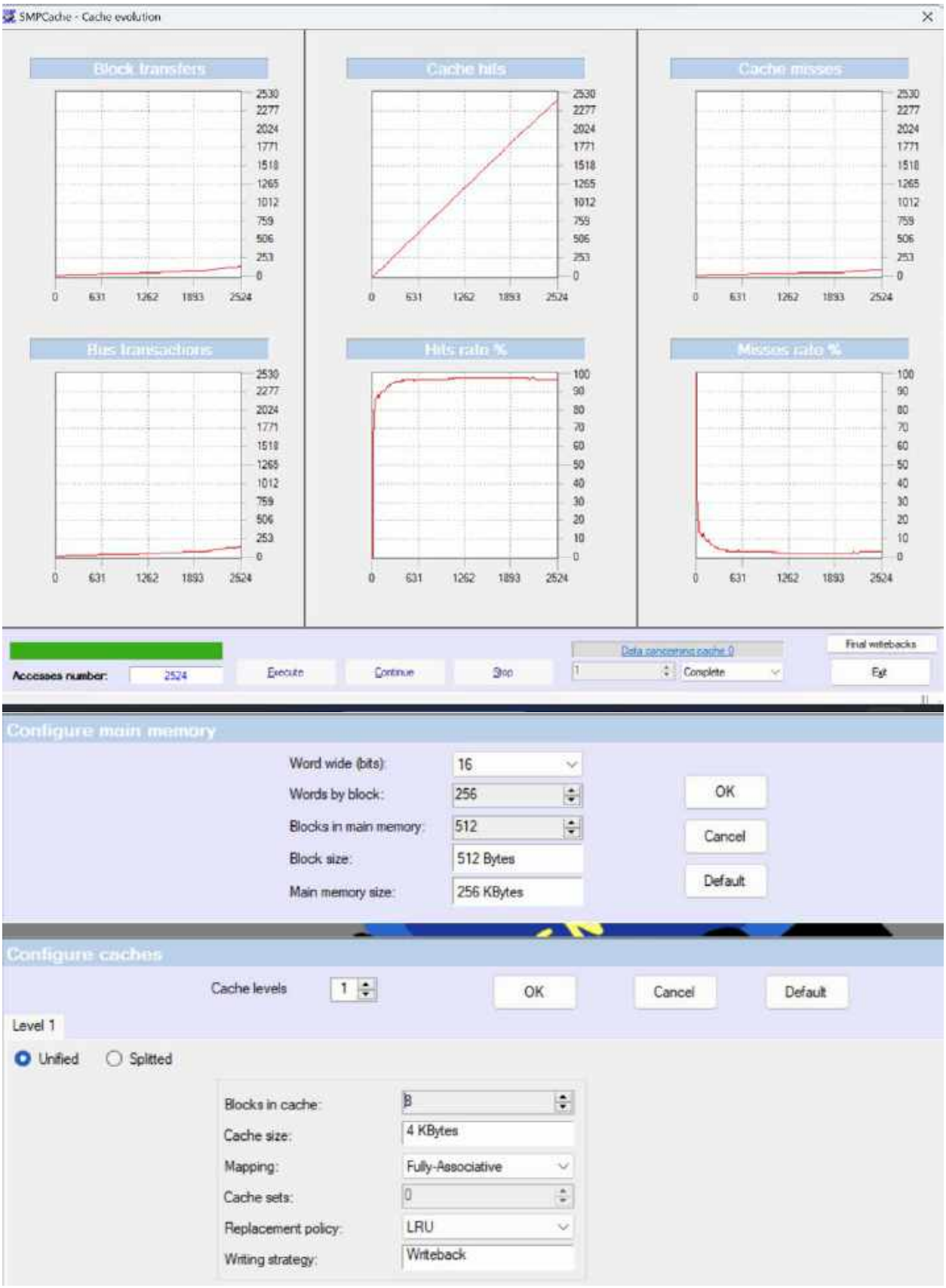

Configure main memory
Word wide (bits): 16
Words by block: 32
Blocks in main memory: 4,096
Block size: 64 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 64
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 64
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 485 2520
0001 (1) Exclusive (E) 486 2524
0002 (2) Exclusive (E) 872 2109
0003 (3) Exclusive (E) 761 2112
0004 (4) Exclusive (E) 1534 2396
0005 (5) Modified (M) 1129 2401
0006 (6) Exclusive (E) 1134 2249
0007 (7) Modified (M) 896 2404
Actual access
Access number: 2524
Access type: Instruction reading
Address: 0000fcc2 (Hex)
Block: 486
Word: 3
Events view Node inspector Hits-Misses Bus States Configuration
Final writebacks
Global readings
Hits Misses
Number 2053 115
Rate 94.696% 5.304%
Global writings
Hits Misses
Number 221 135
Rate 62.079% 37.921%
Global hits and misses
Hits Misses
Number 2274 250
Rate 90.095% 9.905%
Total replacements: 186
Local readings
Hits Misses
Number 2053 115
Rate 94.696% 5.304%
Local writings
Hits Misses
Number 221 135
Rate 62.079% 37.921%
Local hits and misses
Hits Misses
Number 2274 250
Rate 90.095% 9.905%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2524


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
64
Blocks in main memory:
2.048
Block size:
128 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
32
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback


SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requir.
Cache sets:
Cache of node:
Cache level
Cache type:
Unified
Cache address
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 241 2516
0001 (1) Exclusive (E) 242 2520
0002 (2) Modified (M) 84 2322
0003 (3) Exclusive (E) 22 2306
0004 (4) Exclusive (E) 33 2400
0005 (5) Exclusive (E) 384 2300
0006 (6) Exclusive (E) 440 2394
0007 (7) Exclusive (E) 767 2396
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
Global readings
Hits
Misses
Number 2091 77
Rate 96.448% 3.552%
Local readings
Number 2091 77
Rate 96.448% 3.552%
Global writings
Number 284 72
Rate 79.775% 20.225%
Local writings
Number 284 72
Rate 79.775% 20.225%
Global hits and misses
Number 2375 149
Rate 94.097% 5.903%
Local hits and misses
Number 2375 149
Rate 94.097% 5.903%
Total replacements: 117
Cache level
Actual
Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2524


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 2524
Execute
Continue
Stop
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits): 16
Words by block: 128
Blocks in main memory: 1,024
Block size: 256 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 16
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 282 2401
0001 (1) Exclusive (E) 17 2406
0002 (2) Modified (M) 224 2404
0003 (3) Exclusive (E) 120 2516
0004 (4) Exclusive (E) 227 2458
0005 (5) Exclusive (E) 119 2502
0006 (6) Exclusive (E) 210 2480
0007 (7) Exclusive (E) 42 2511
Actual access
Access number: 2524
Access type: Instruction reading
Address:
Block: 121
Word: 67
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2116 52
Rate 97.601% 2.399%
Global writings
Hits Misses
Number 318 38
Rate 89.326% 10.674%
Global hits and misses
Hits Misses
Number 2434 90
Rate 96.434% 3.566%
Total replacements: 74
Local readings
Hits Misses
Number 2116 52
Rate 97.601% 2.399%
Local writings
Hits Misses
Number 318 38
Rate 89.326% 10.674%
Local hits and misses
Hits Misses
Number 2434 90
Rate 96.434% 3.566%
Cache level 1
Actual Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2524


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
256
Blocks in main memory:
512
Block size:
512 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

SMPCache - Cache evolution

Information | View cache | P0-P0

Number of blocks: 8
Mapping: Fully Associative
Replacement requ LRU
Cache sets: 8

Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0

1/1

Address	State	Block	Last Access
0000 (0)	Exclusive (E)	59	2502
0001 (1)	Modified (M)	140	2523
0002 (2)	Exclusive (E)	36	2488
0003 (3)	Exclusive (E)	21	2511
0004 (4)	Modified (M)	7	2509
0005 (5)	Exclusive (E)	60	2524
0006 (6)	Exclusive (E)	104	2470
0007 (7)	Exclusive (E)	105	2480

Actual access

Access number:	2524
Access type:	Instruction reading
Address:	0000bcc3 (Hex)
Block:	60
Word:	195

Events visor | Node inspector | Hits-Misses | Bus | States | Configuration

Final writebacks

Data concerning cache 0

Global readings

	Hits	Misses
Number	2108	60
Rate	97.232%	2.768%

Global writings

	Hits	Misses
Number	333	23
Rate	93.539%	6.461%

Global hits and misses

	Hits	Misses
Number	2441	83
Rate	96.712%	3.288%

Total replacements: 75

Local readings

	Hits	Misses
Number	2108	60
Rate	97.232%	2.768%

Local writings

	Hits	Misses
Number	333	23
Rate	93.539%	6.461%

Local hits and misses

	Hits	Misses
Number	2441	83
Rate	96.712%	3.288%

Cache level 1

	Actual	Total
Accesses	2524	2524
Instructions	2055	2055
Data readings	113	113
Data writings	356	356

Execute
Continue
Stop
1
Complete
Exit

Simulation steps: 2524

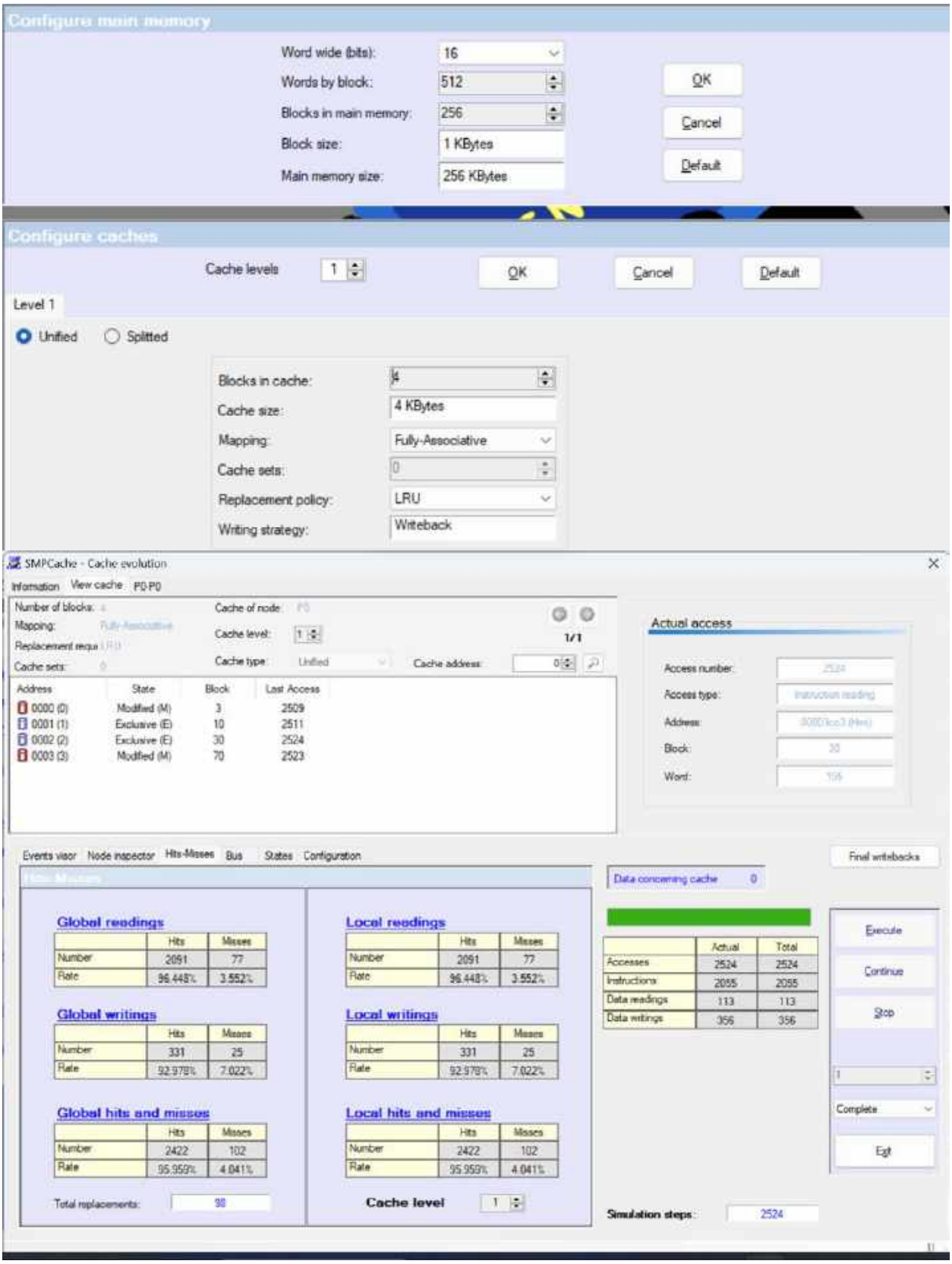
SMPCache - Cache evolution

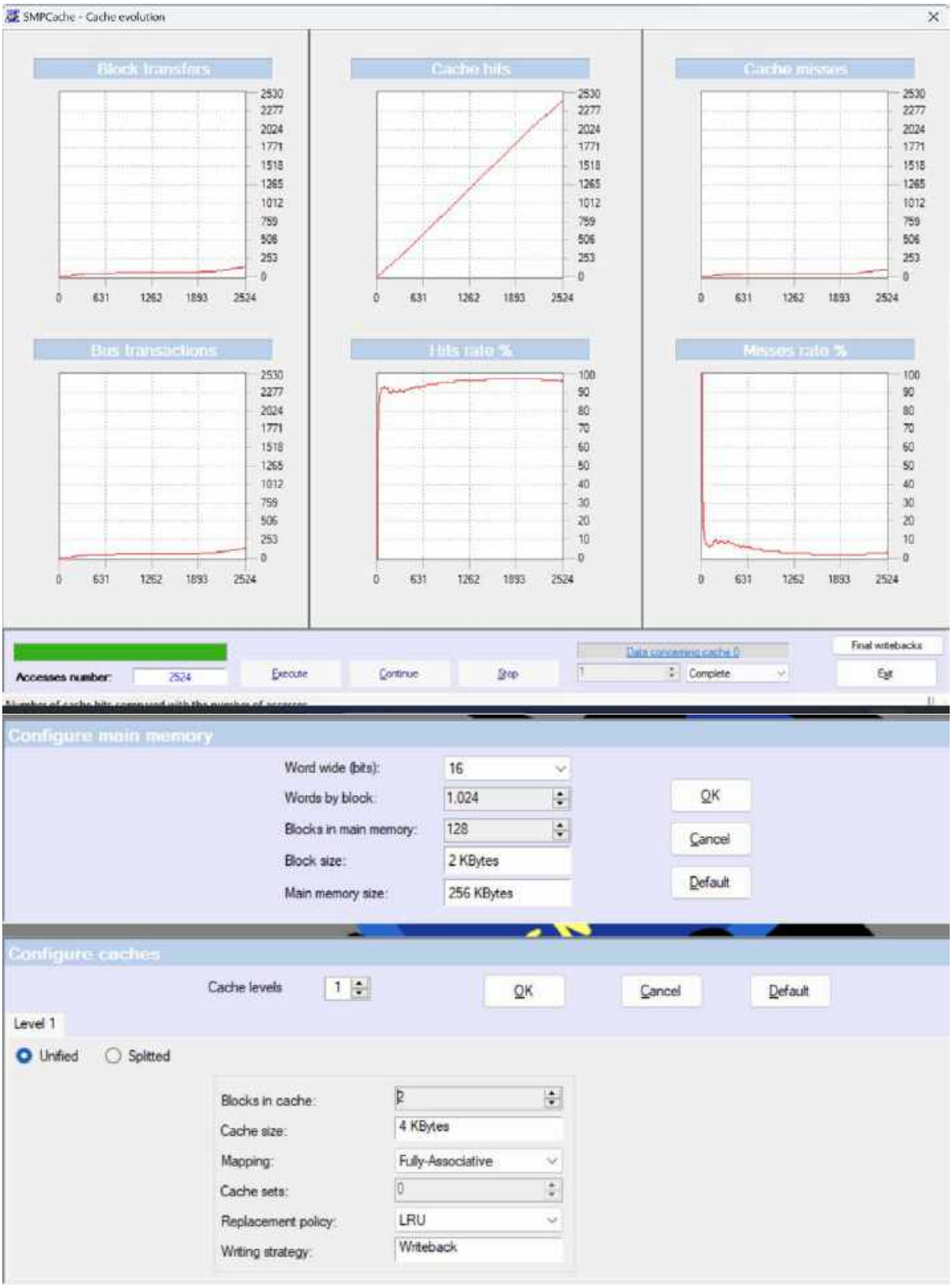
Block transfers | Cache hits | Cache misses

Bus transactions | Hits ratio % | Misses ratio %

0 631 1262 1893 2524

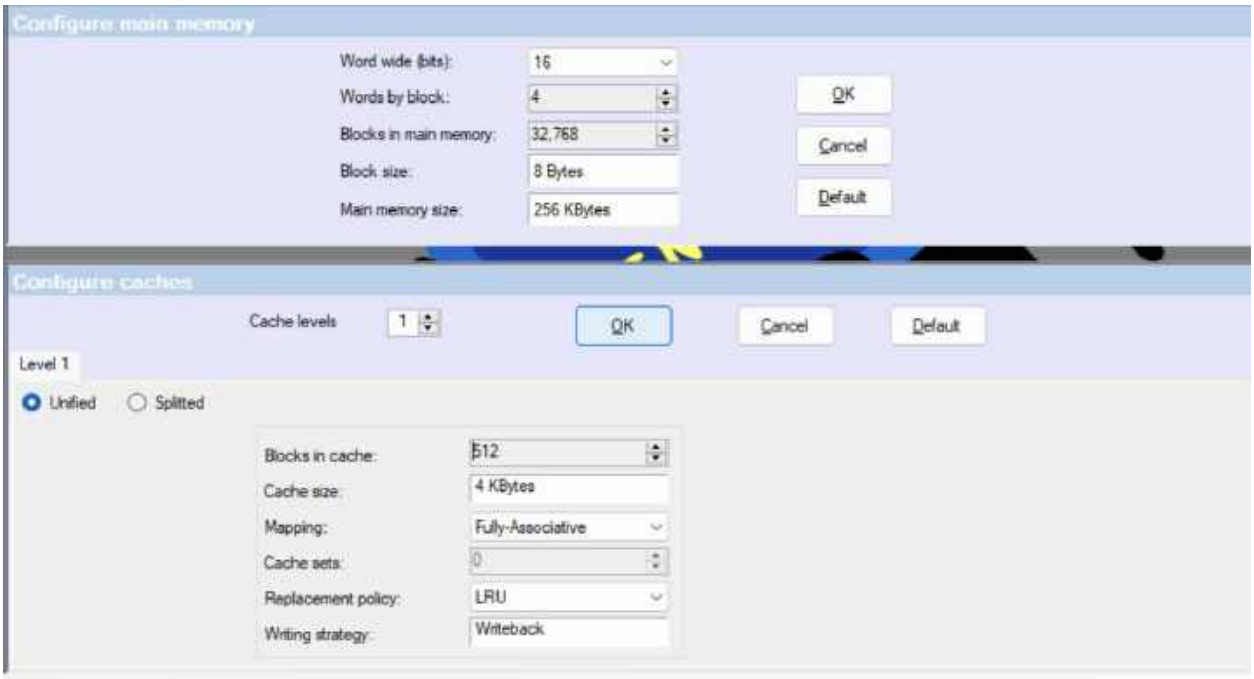
Accesses number: 2524 | Execute | Continue | Stop | Data concerning cache 0 | 1 | Complete | Final writebacks | Exit

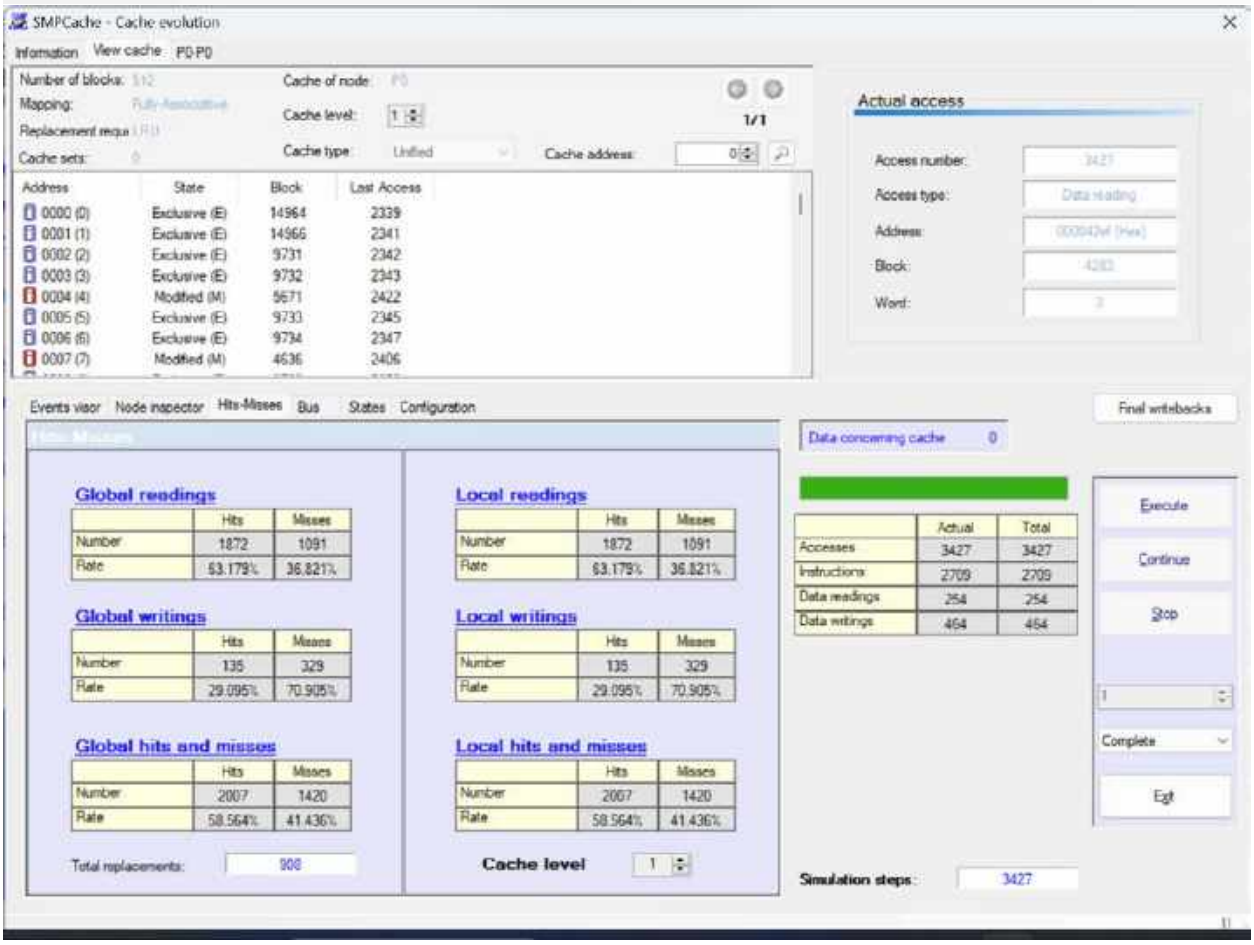

Configure main memory
Word wide (bits): 16
Words by block: 512
Blocks in main memory: 256
Block size: 1 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 4
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 3 2509
0001 (1) Exclusive (E) 10 2511
0002 (2) Exclusive (E) 30 2524
0003 (3) Modified (M) 70 2523
Actual access
Access number: 2524
Access type: Instruction reading
Address:
Block: 30
Word: 156
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2091 77
Rate 96.448% 3.552%
Global writings
Hits Misses
Number 331 25
Rate 92.978% 7.022%
Global hits and misses
Hits Misses
Number 2422 102
Rate 95.959% 4.041%
Total replacements: 98
Local readings
Hits Misses
Number 2091 77
Rate 96.448% 3.552%
Local writings
Hits Misses
Number 331 25
Rate 92.978% 7.022%
Local hits and misses
Hits Misses
Number 2422 102
Rate 95.959% 4.041%
Cache level 1
Actual Total
Accesses 2524 2524
Instructions 2055 2055
Data readings 113 113
Data writings 356 356
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2524

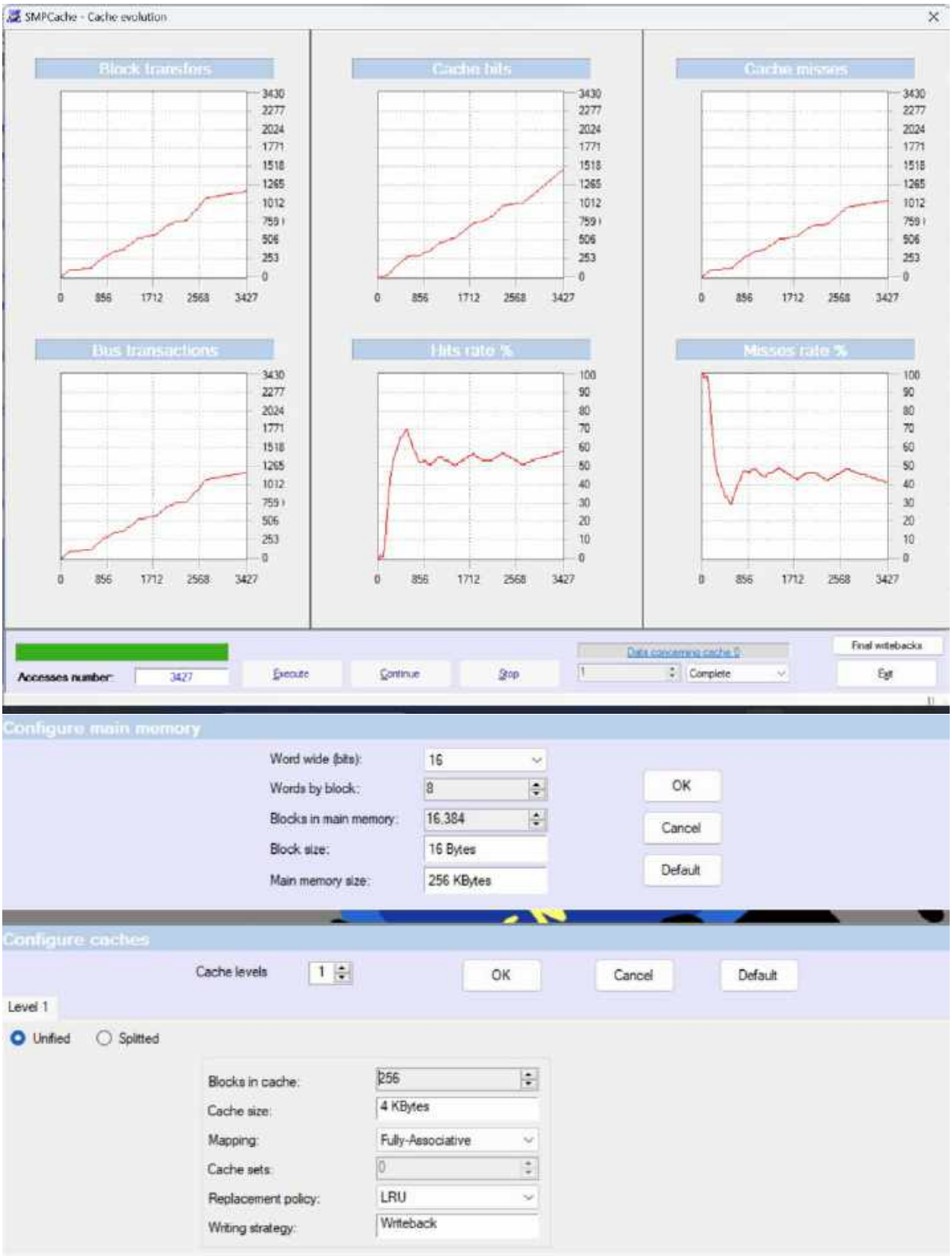

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
1,024
Blocks in main memory:
128
Block size:
2 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
2
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

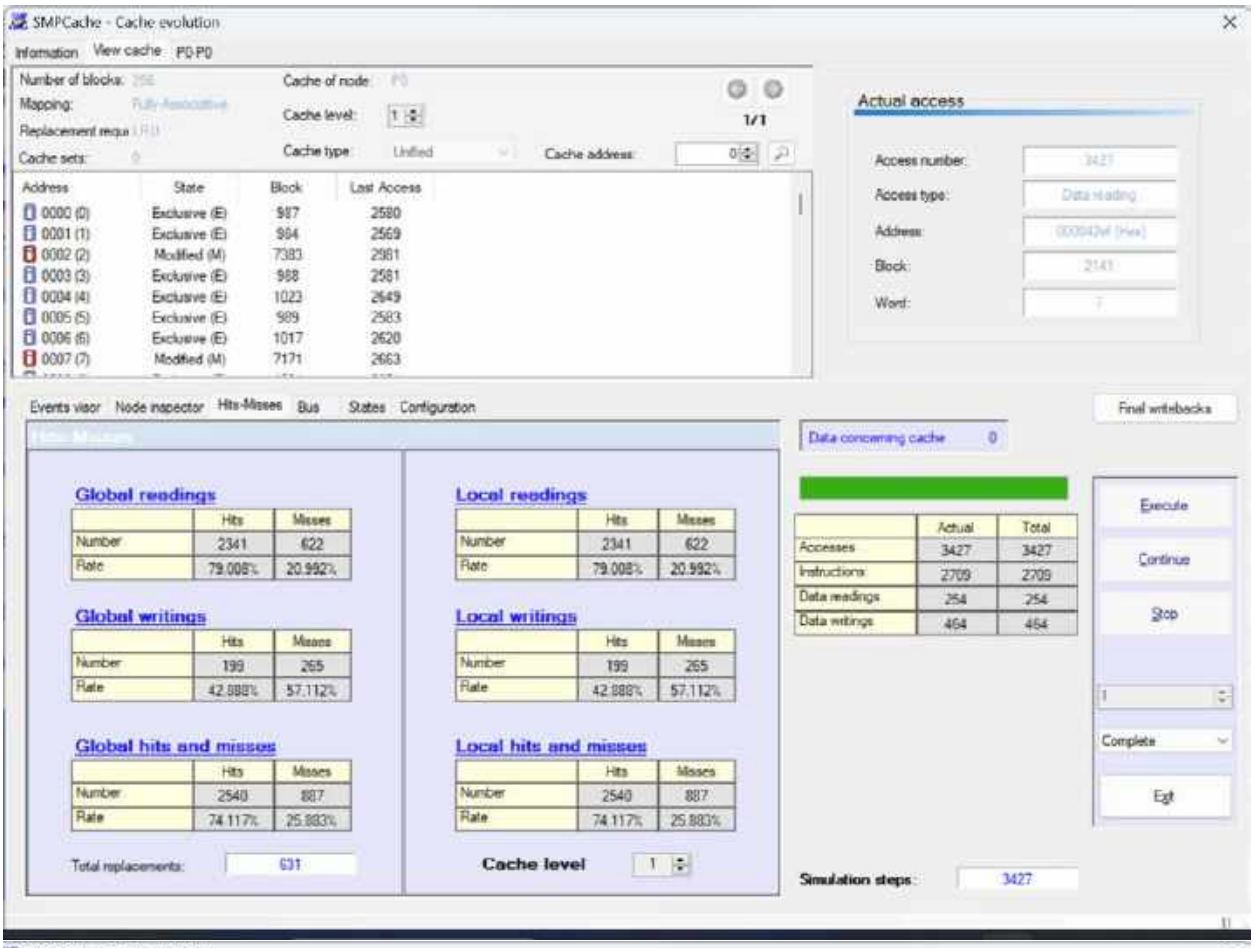
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Modified (M)
35
2523
0001 (1)
Exclusive (E)
15
2524
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
2047
121
Rate
94.419%
5.581%
Global writings
302
54
84.831%
15.169%
Global hits and misses
2349
175
93.067%
6.933%
Total replacements:
173
Local readings
Local writings
Local hits and misses
Cache level
Actual
Total
Accesses
2524
2524
Instructions
2055
2055
Data readings
113
113
Data writings
356
356
Execute
Continue
Stop
Complete
Exit
Simulation steps:
2524
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Complete
Final writebacks
Exit

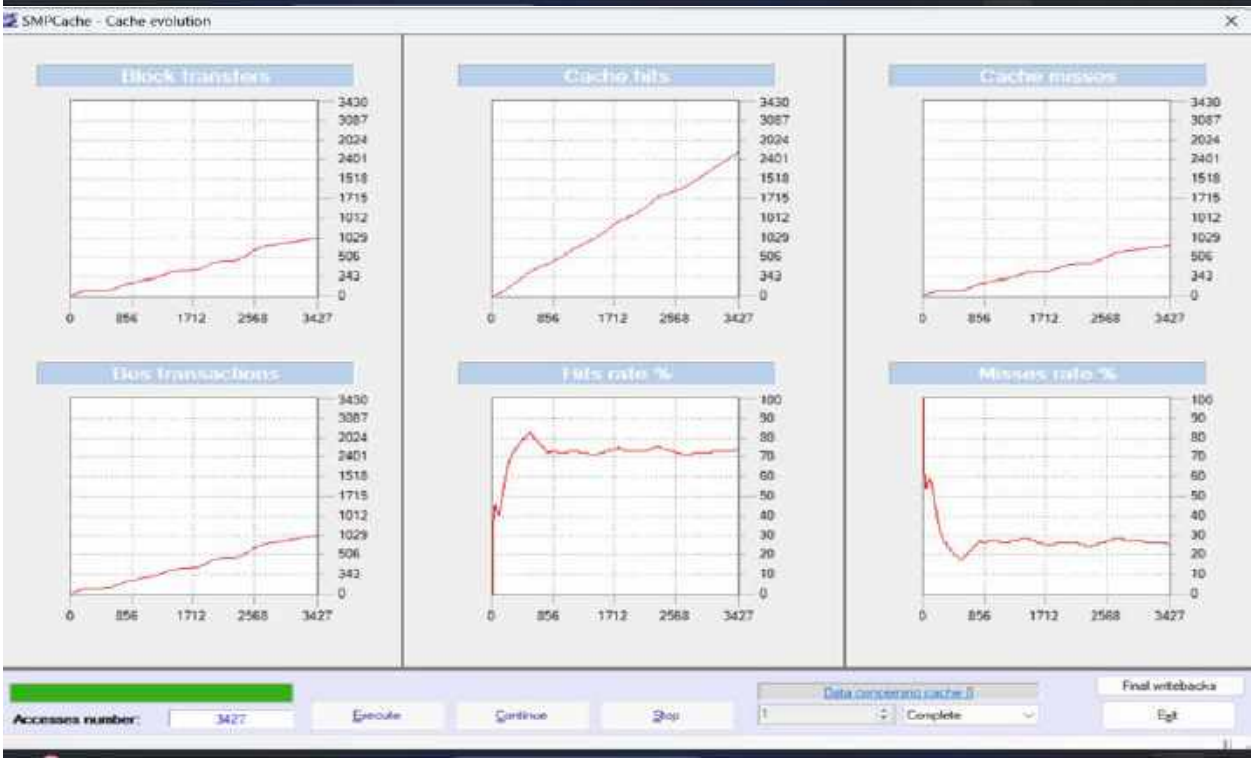
WAVE

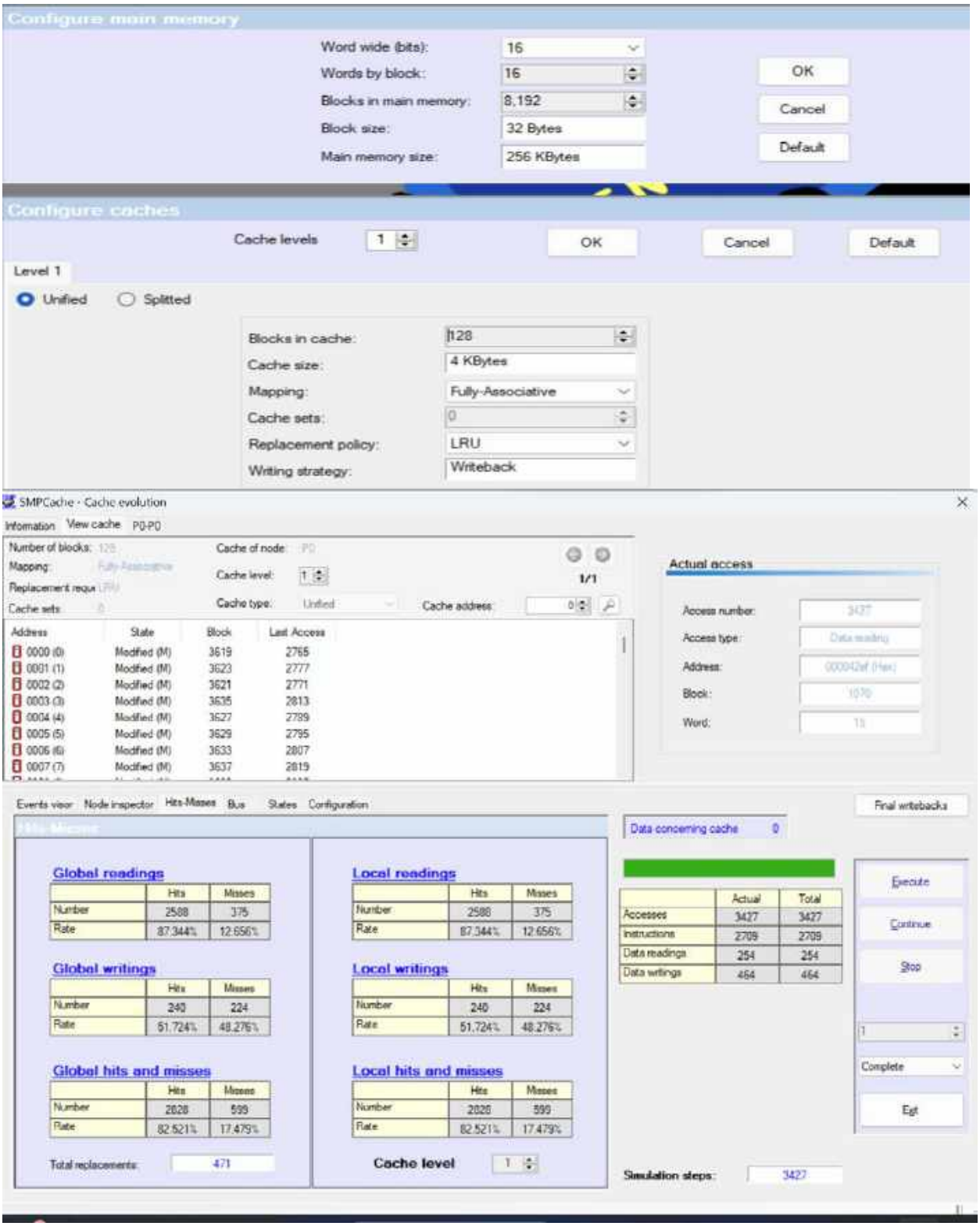

Configure main memory
Word wide (bits): 16
Words by block: 4
Blocks in main memory: 32,768
Block size: 8 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 512
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

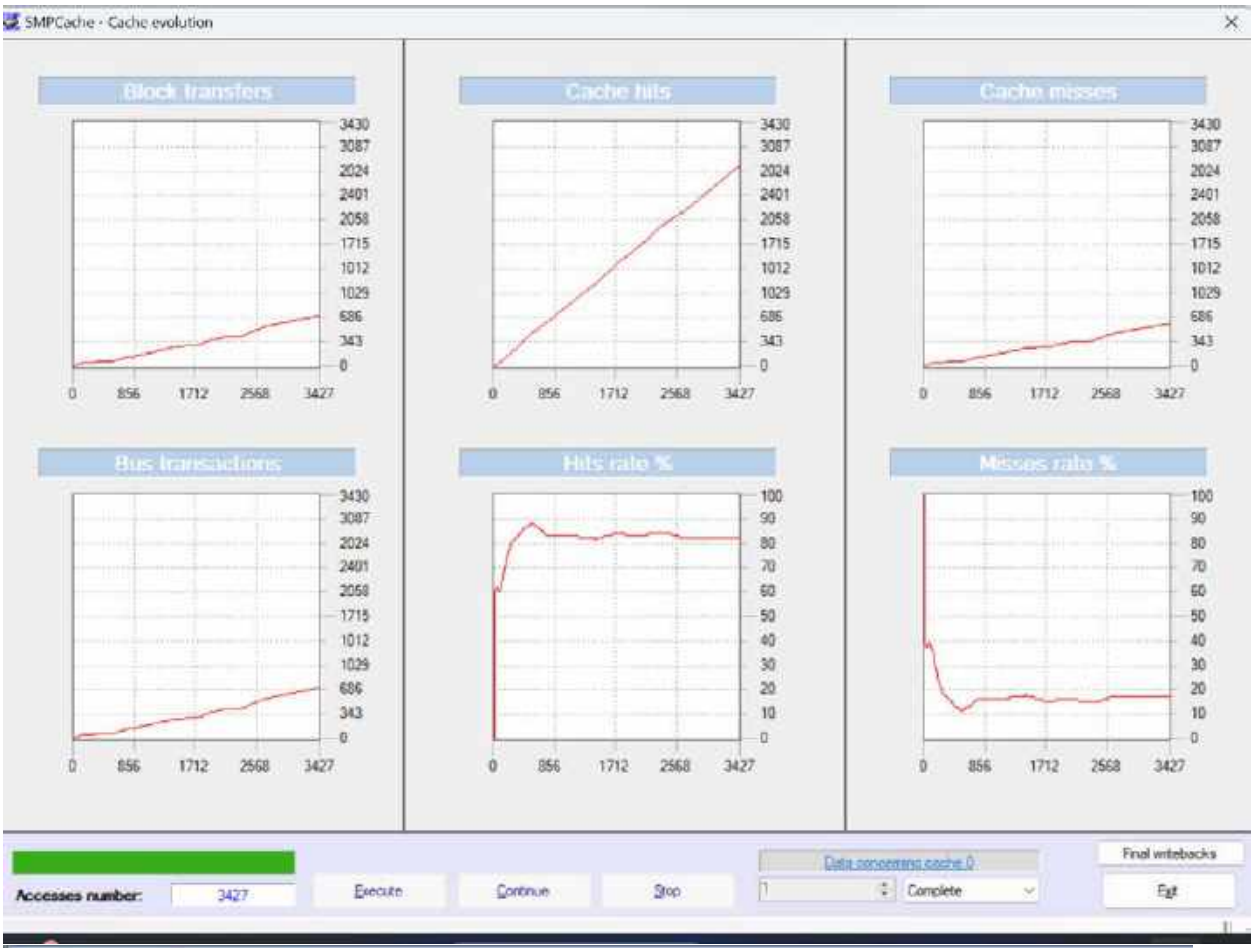

SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 512
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 14964 2339
0001 (1) Exclusive (E) 14966 2341
0002 (2) Exclusive (E) 9731 2342
0003 (3) Exclusive (E) 9732 2343
0004 (4) Modified (M) 5671 2422
0005 (5) Exclusive (E) 9733 2345
0006 (6) Exclusive (E) 9734 2347
0007 (7) Modified (M) 4636 2406
Actual access
Access number: 3427
Access type: Data reading
Address: 000042af (hex)
Block: 4283
Word: 3
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1872 1091
Rate 63.179% 36.821%
Global writings
Hits Misses
Number 135 329
Rate 29.095% 70.905%
Global hits and misses
Hits Misses
Number 2007 1420
Rate 58.564% 41.436%
Total replacements: 908
Local readings
Hits Misses
Number 1872 1091
Rate 63.179% 36.821%
Local writings
Hits Misses
Number 135 329
Rate 29.095% 70.905%
Local hits and misses
Hits Misses
Number 2007 1420
Rate 58.564% 41.436%
Cache level 1
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3427

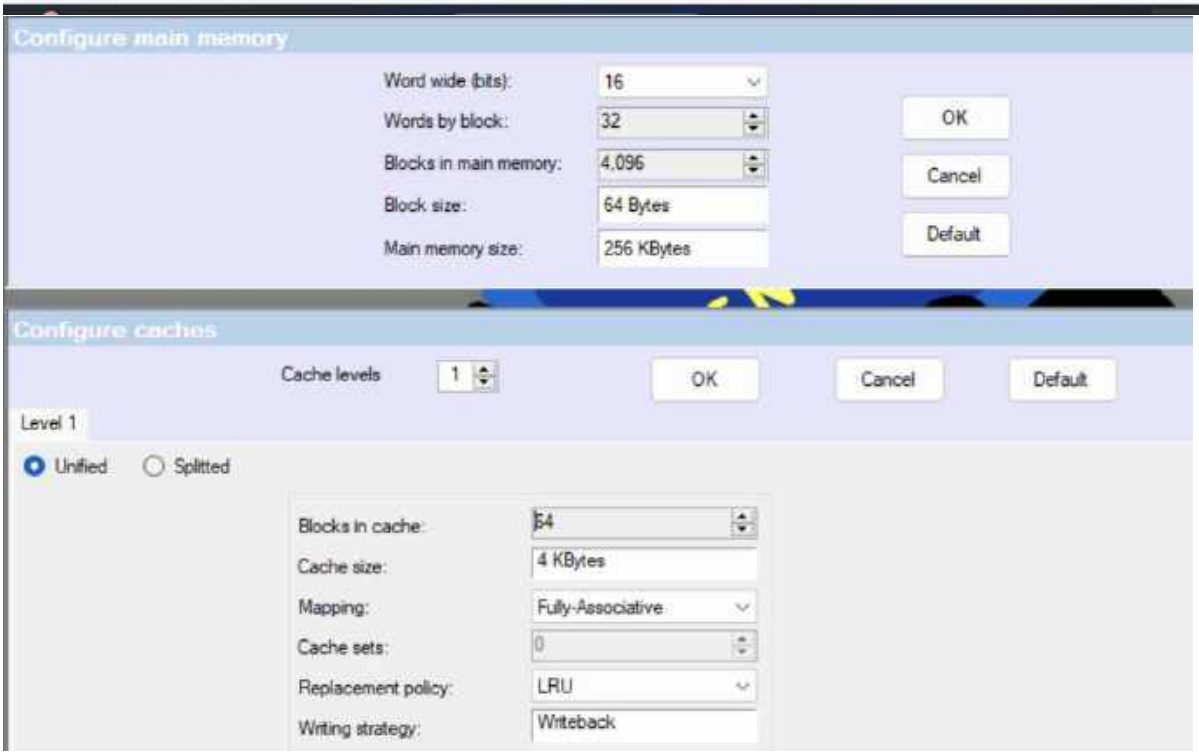

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
Continue
Stop
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
8
Blocks in main memory:
16.384
Block size:
16 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
Level 1
Unified
Splitted
Blocks in cache:
256
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

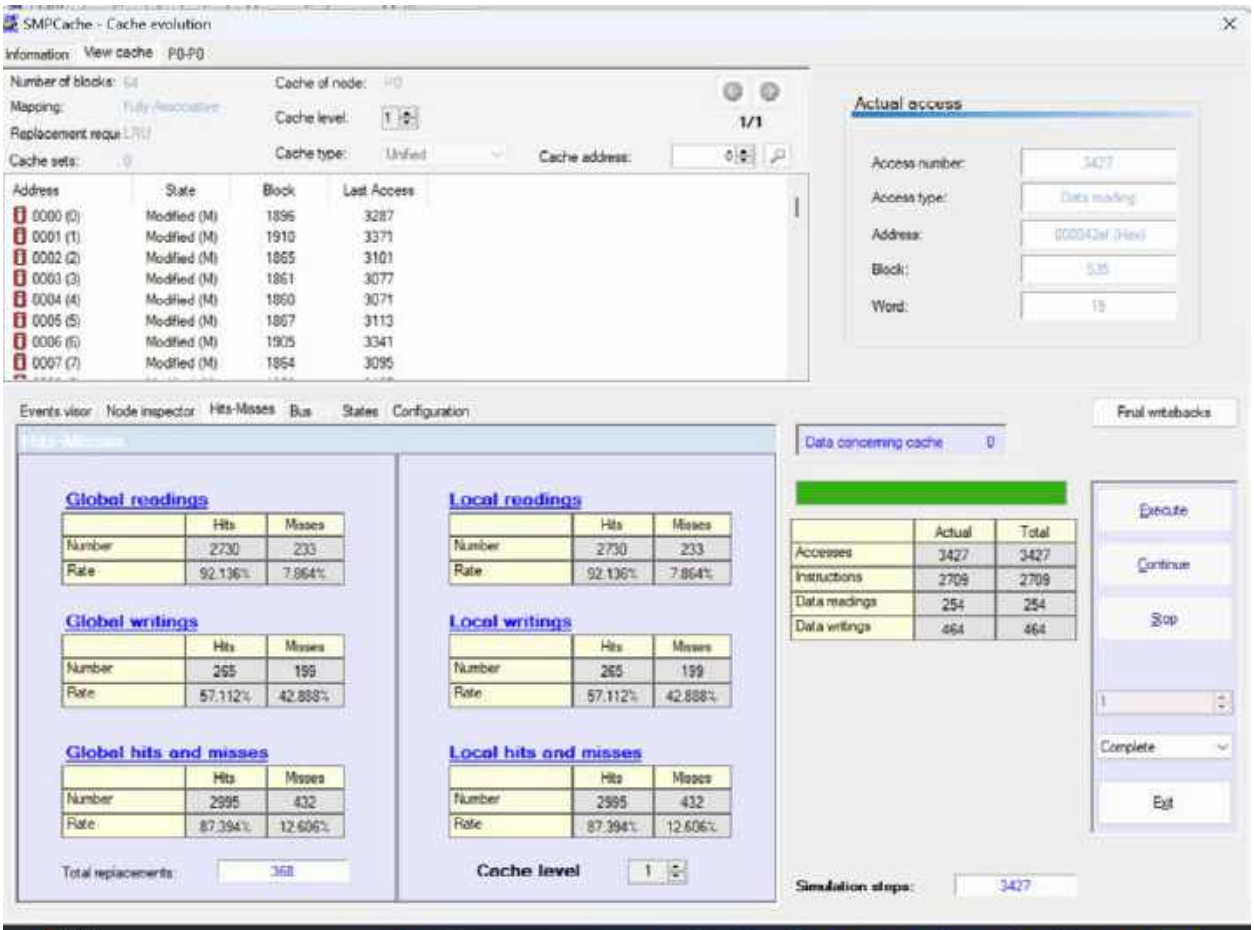

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 987 2580
0001 (1) Exclusive (E) 984 2569
0002 (2) Modified (M) 7383 2981
0003 (3) Exclusive (E) 988 2581
0004 (4) Exclusive (E) 1023 2649
0005 (5) Exclusive (E) 989 2583
0006 (6) Exclusive (E) 1017 2620
0007 (7) Modified (M) 7171 2663
Actual access
Access number:
Access type:
Data reading
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 2341 622
Rate 79.008% 20.992%
Global writings
Number 199 265
Rate 42.888% 57.112%
Global hits and misses
Number 2540 887
Rate 74.117% 25.883%
Total replacements: 631
Local readings
Number 2341 622
Rate 79.008% 20.992%
Local writings
Number 199 265
Rate 42.888% 57.112%
Local hits and misses
Number 2540 887
Rate 74.117% 25.883%
Cache level 1
Actual
Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
Complete
Exit
Simulation steps: 3427

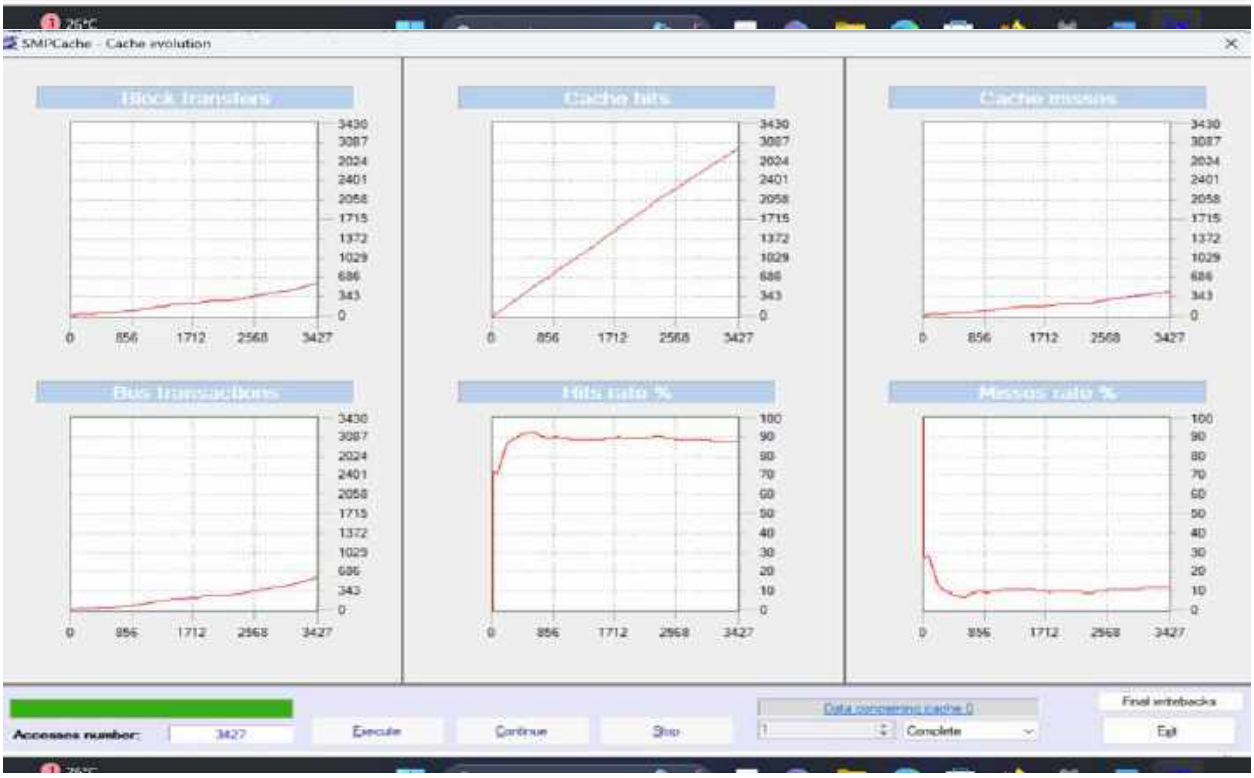

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0
856
1712
2568
3427
Accesses number:
Execute
Continue
Stop
Complete
Final writebacks
Exit

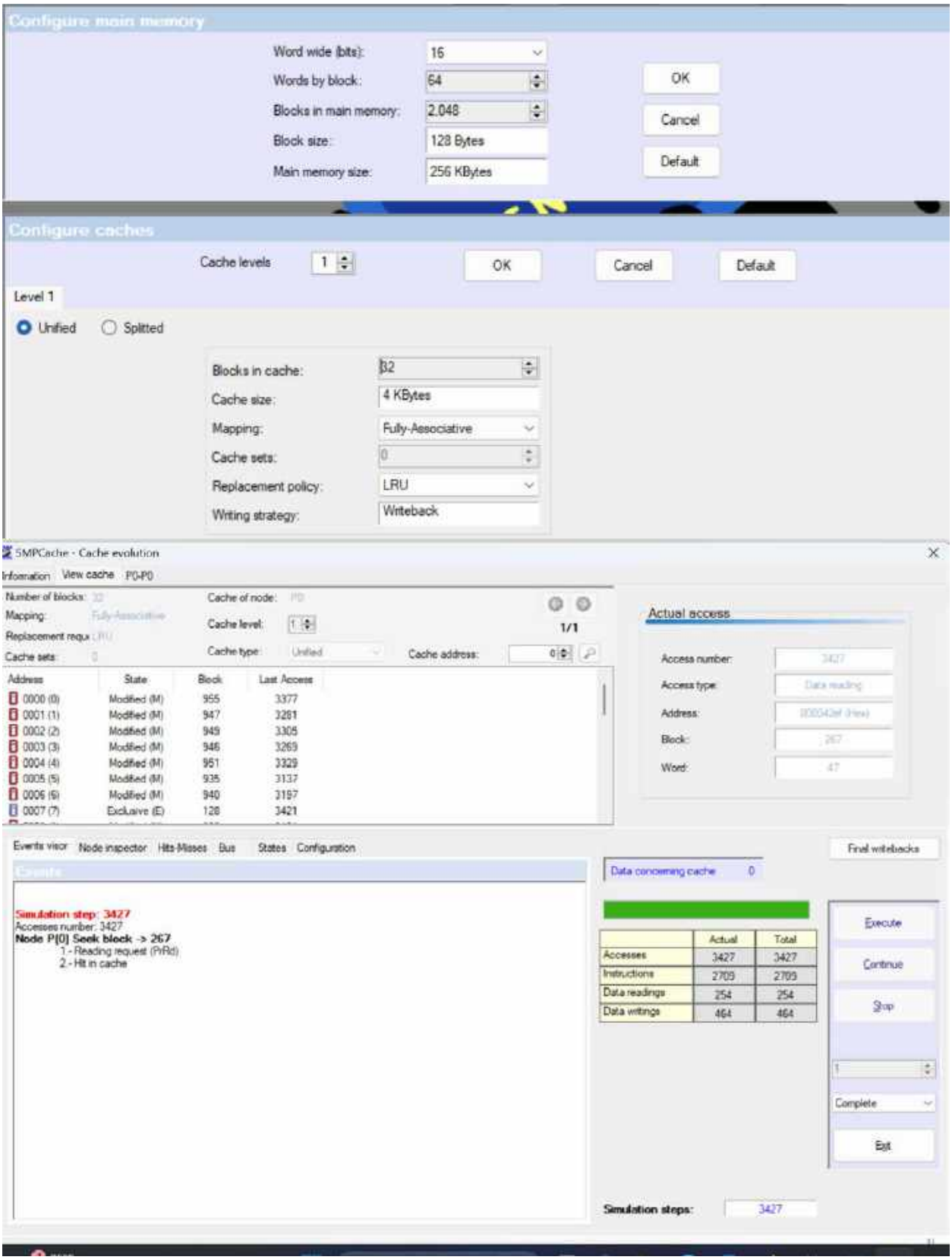

Configure main memory
Word wide (bits): 16
Words by block: 16
Blocks in main memory: 8,192
Block size: 32 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 128
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 128
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 3619 2765
0001 (1) Modified (M) 3623 2777
0002 (2) Modified (M) 3621 2771
0003 (3) Modified (M) 3635 2813
0004 (4) Modified (M) 3627 2789
0005 (5) Modified (M) 3629 2795
0006 (6) Modified (M) 3633 2807
0007 (7) Modified (M) 3637 2819
Actual access
Access number: 3427
Access type: Data reading
Address: 000042af (Hex)
Block: 1070
Word: 15
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2588 375
Rate 87.344% 12.656%
Global writings
Hits Misses
Number 240 224
Rate 51.724% 48.276%
Global hits and misses
Hits Misses
Number 2828 599
Rate 82.521% 17.479%
Total replacements: 471
Local readings
Hits Misses
Number 2588 375
Rate 87.344% 12.656%
Local writings
Hits Misses
Number 240 224
Rate 51.724% 48.276%
Local hits and misses
Hits Misses
Number 2828 599
Rate 82.521% 17.479%
Cache level 1
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3427

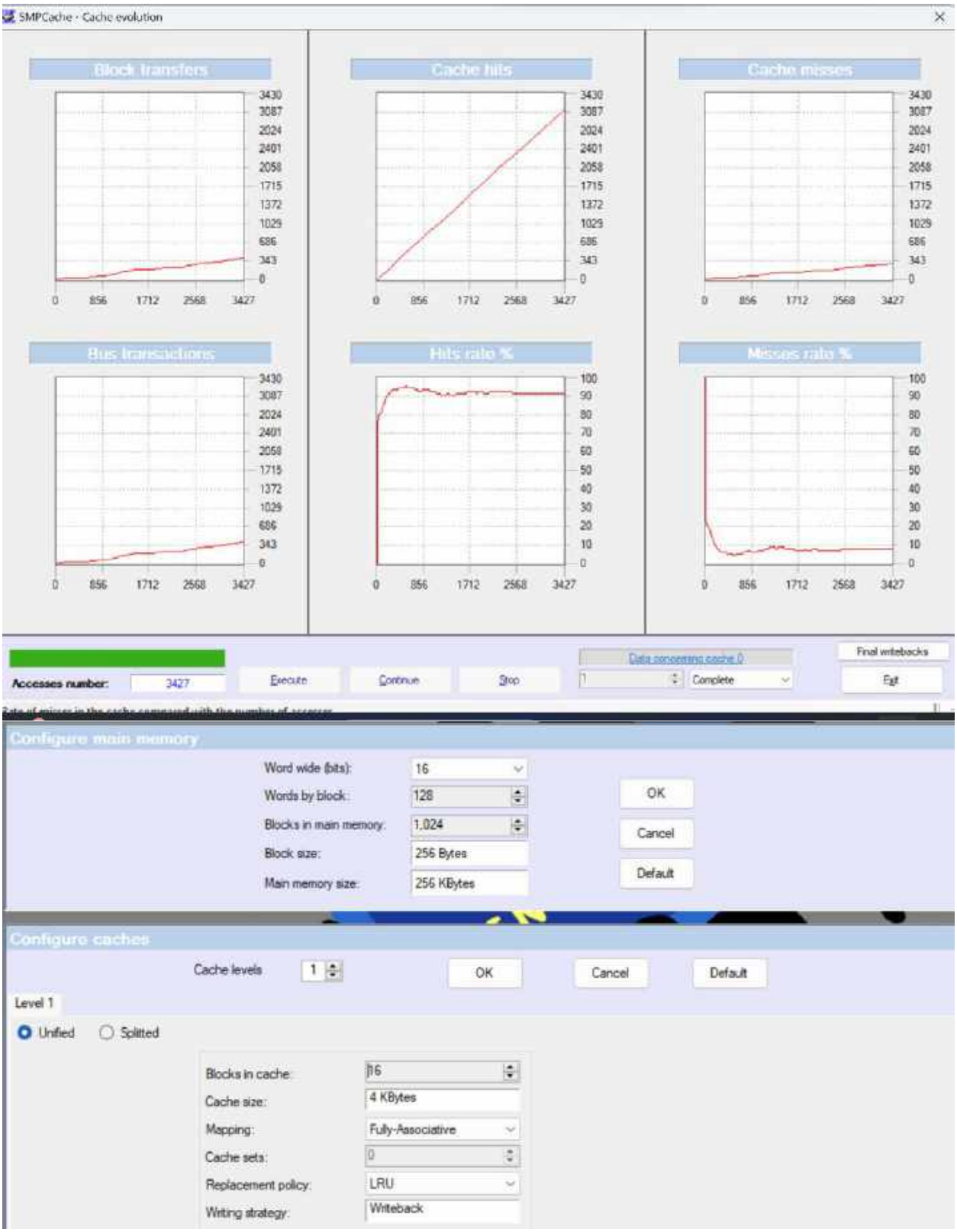

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
Continue
Stop
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits):
16
Words by block:
32
Blocks in main memory:
4,096
Block size:
64 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
64
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

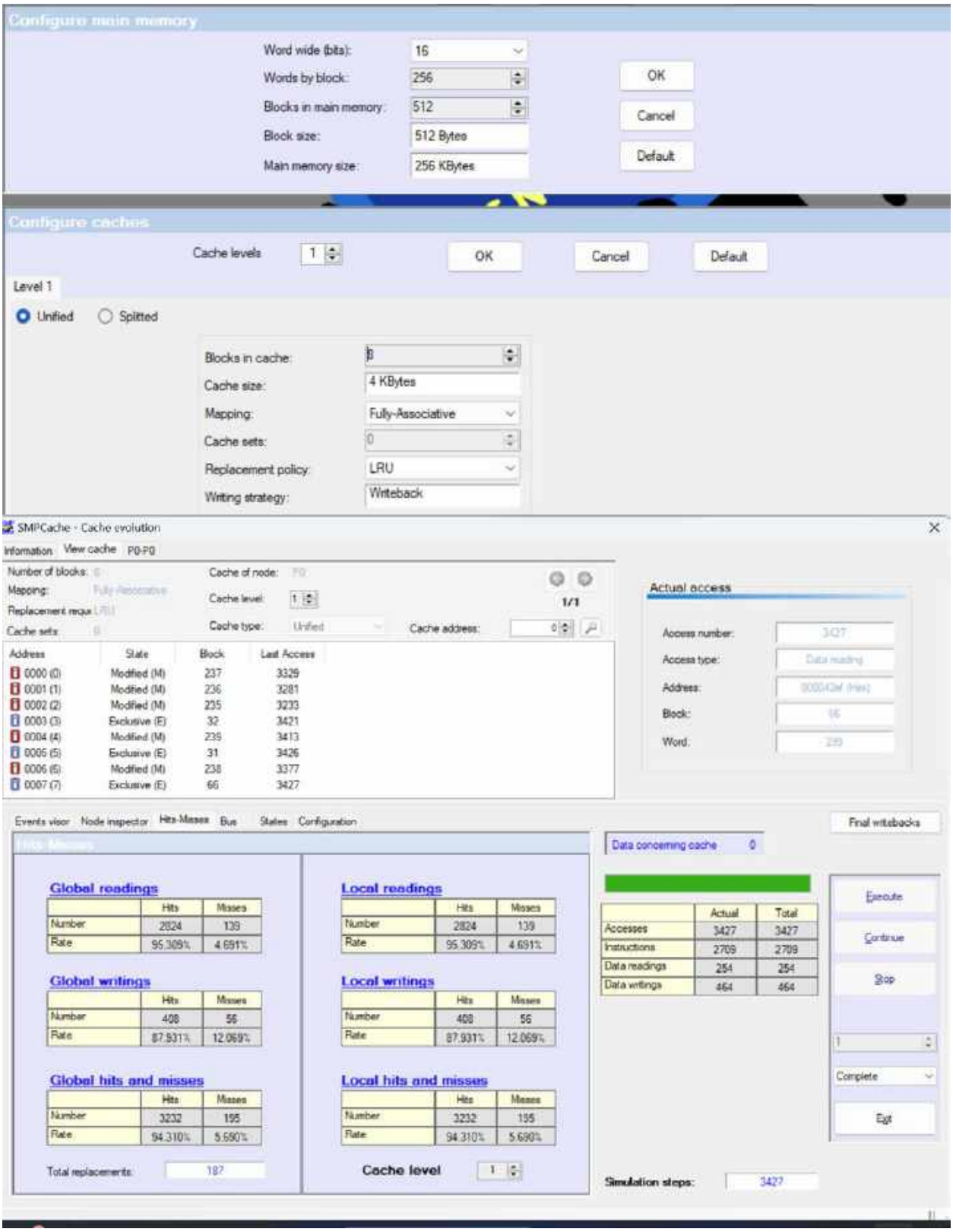

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 1896 3287
0001 (1) Modified (M) 1910 3371
0002 (2) Modified (M) 1865 3101
0003 (3) Modified (M) 1861 3077
0004 (4) Modified (M) 1860 3071
0005 (5) Modified (M) 1867 3113
0006 (6) Modified (M) 1905 3341
0007 (7) Modified (M) 1864 3095
Actual access
Access number: 3427
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2730 233
Rate 92.136% 7.864%
Global writings
Hits Misses
Number 265 199
Rate 57.112% 42.888%
Global hits and misses
Hits Misses
Number 2995 432
Rate 87.394% 12.606%
Total replacements: 368
Local readings
Hits Misses
Number 2730 233
Rate 92.136% 7.864%
Local writings
Hits Misses
Number 265 199
Rate 57.112% 42.888%
Local hits and misses
Hits Misses
Number 2995 432
Rate 87.394% 12.606%
Cache level 1
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
Complete
Exit
Simulation steps: 3427

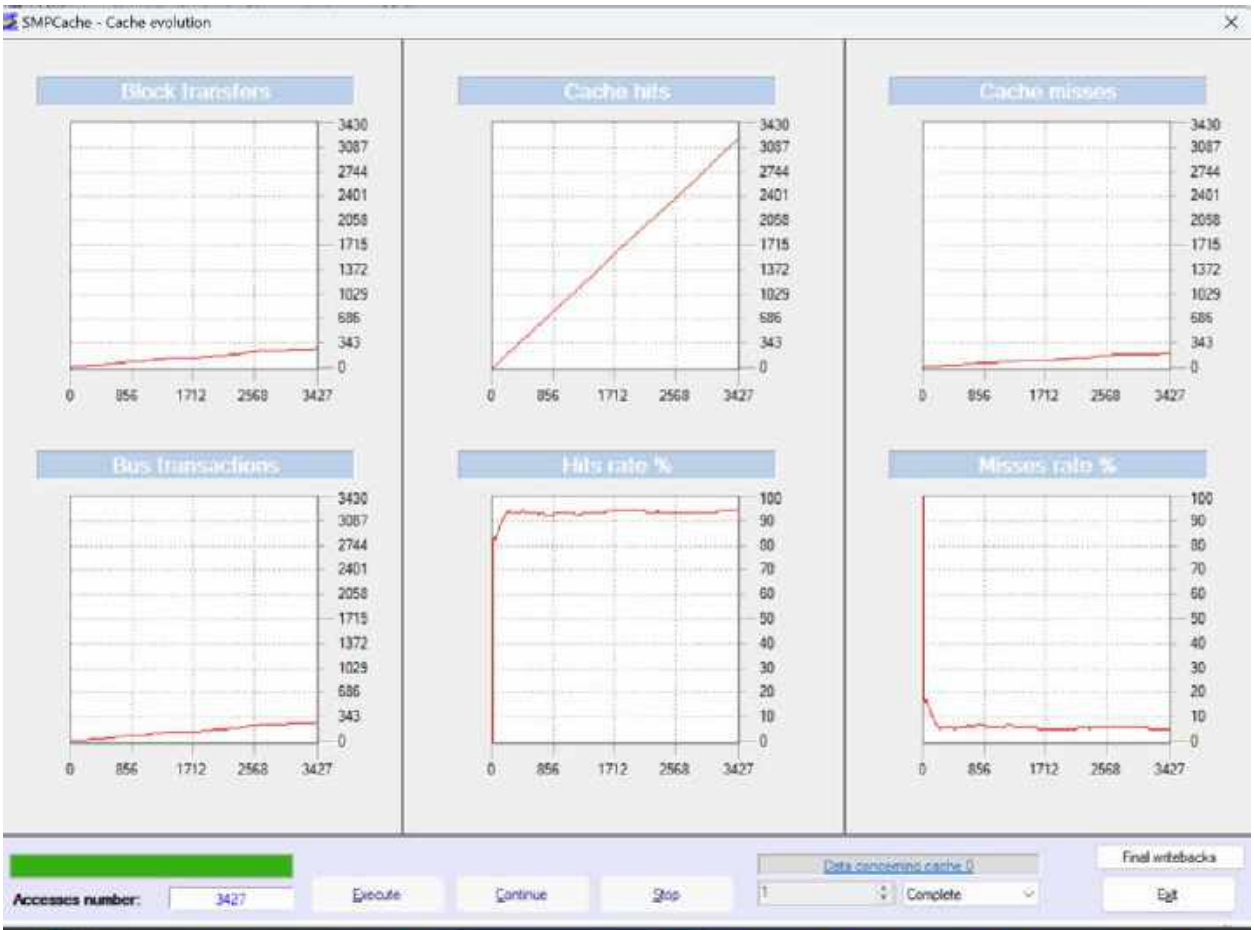

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits ratio %
Misses ratio %
0 856 1712 2568 3427
Accesses number: 3427
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits): 16
Words by block: 64
Blocks in main memory: 2,048
Block size: 128 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 32
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache P0-P0
Number of blocks: 32
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 955 3377
0001 (1) Modified (M) 947 3281
0002 (2) Modified (M) 949 3305
0003 (3) Modified (M) 946 3269
0004 (4) Modified (M) 951 3329
0005 (5) Modified (M) 935 3137
0006 (6) Modified (M) 940 3197
0007 (7) Exclusive (E) 128 3421
Actual access
Access number: 3427
Access type: Data reading
Address: 000042ef (hex)
Block: 267
Word: 47
Events viewer
Node inspector
Hits-Misses
Bus
States
Configuration
Events
Simulation step: 3427
Accesses number: 3427
Node P[0] Seek block -> 267
1 - Reading request (PrRd)
2 - Hit in cache
Final writebacks
Data concerning cache 0
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3427

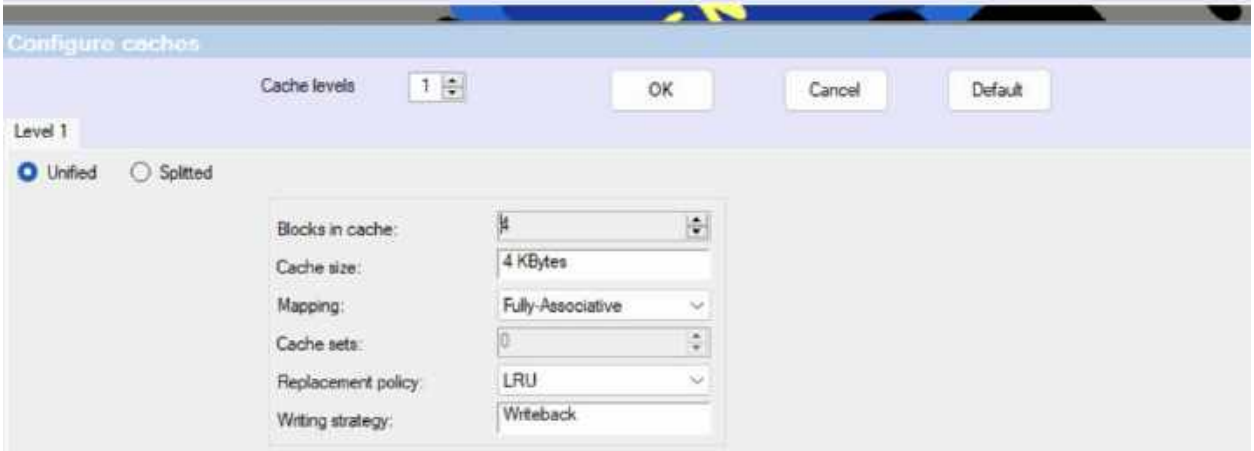

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
Continue
Stop
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
128
Blocks in main memory:
1.024
Block size:
256 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
16
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 478 3401
0001 (1) Exclusive (E) 133 3427
0002 (2) Modified (M) 474 3305
0003 (3) Modified (M) 473 3281
0004 (4) Modified (M) 475 3329
0005 (5) Modified (M) 477 3377
0006 (6) Modified (M) 469 3185
0007 (7) Exclusive (E) 62 3426
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
Global readings
Hits
Misses
Number 2823 140
Rate 95.275% 4.725%
Global writings
Number 377 87
Rate 81.250% 18.750%
Global hits and misses
Number 3200 227
Rate 93.376% 6.624%
Total replacements: 211
Local readings
Number 2823 140
Rate 95.275% 4.725%
Local writings
Number 377 87
Rate 81.250% 18.750%
Local hits and misses
Number 3200 227
Rate 93.376% 6.624%
Cache level
Actual
Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
Complete
Exit
Simulation steps: 3427
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 856 1712 2568 3427
Accesses number: 3427
Execute
Continue
Stop
Complete
Final writebacks
Exit

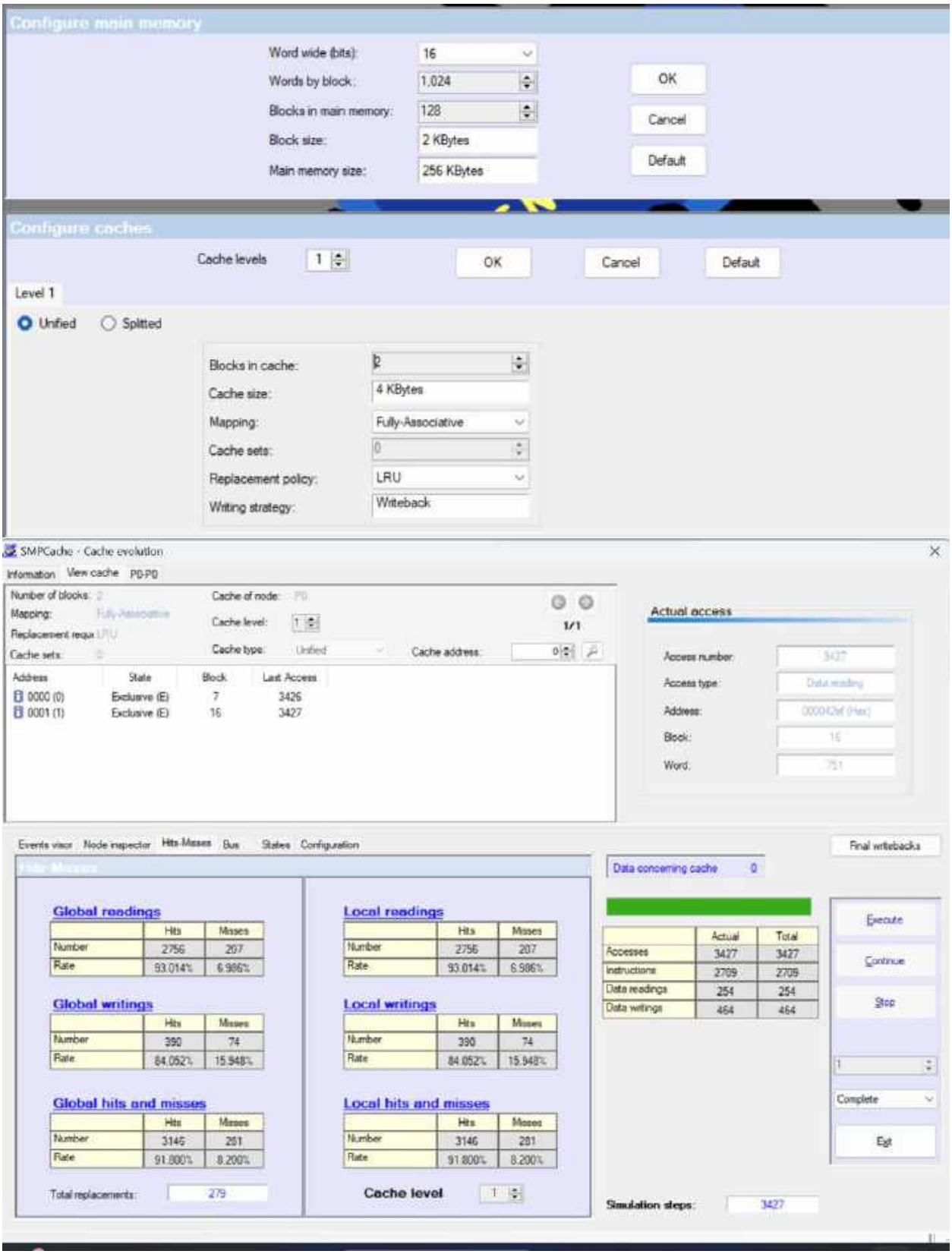

Configure main memory
Word wide (bits): 16
Words by block: 256
Blocks in main memory: 512
Block size: 512 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 8
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 237 3329
0001 (1) Modified (M) 236 3281
0002 (2) Modified (M) 235 3233
0003 (3) Exclusive (E) 32 3421
0004 (4) Modified (M) 239 3413
0005 (5) Exclusive (E) 31 3426
0006 (6) Modified (M) 238 3377
0007 (7) Exclusive (E) 66 3427
Actual access
Access number: 3427
Access type: Data reading
Address: 000042af (Hex)
Block: 66
Word: 239
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2824 139
Rate 95.309% 4.691%
Global writings
Hits Misses
Number 408 56
Rate 87.931% 12.069%
Global hits and misses
Hits Misses
Number 3232 195
Rate 94.310% 5.690%
Total replacements: 187
Local readings
Hits Misses
Number 2824 139
Rate 95.309% 4.691%
Local writings
Hits Misses
Number 408 56
Rate 87.931% 12.069%
Local hits and misses
Hits Misses
Number 3232 195
Rate 94.310% 5.690%
Cache level 1
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3427

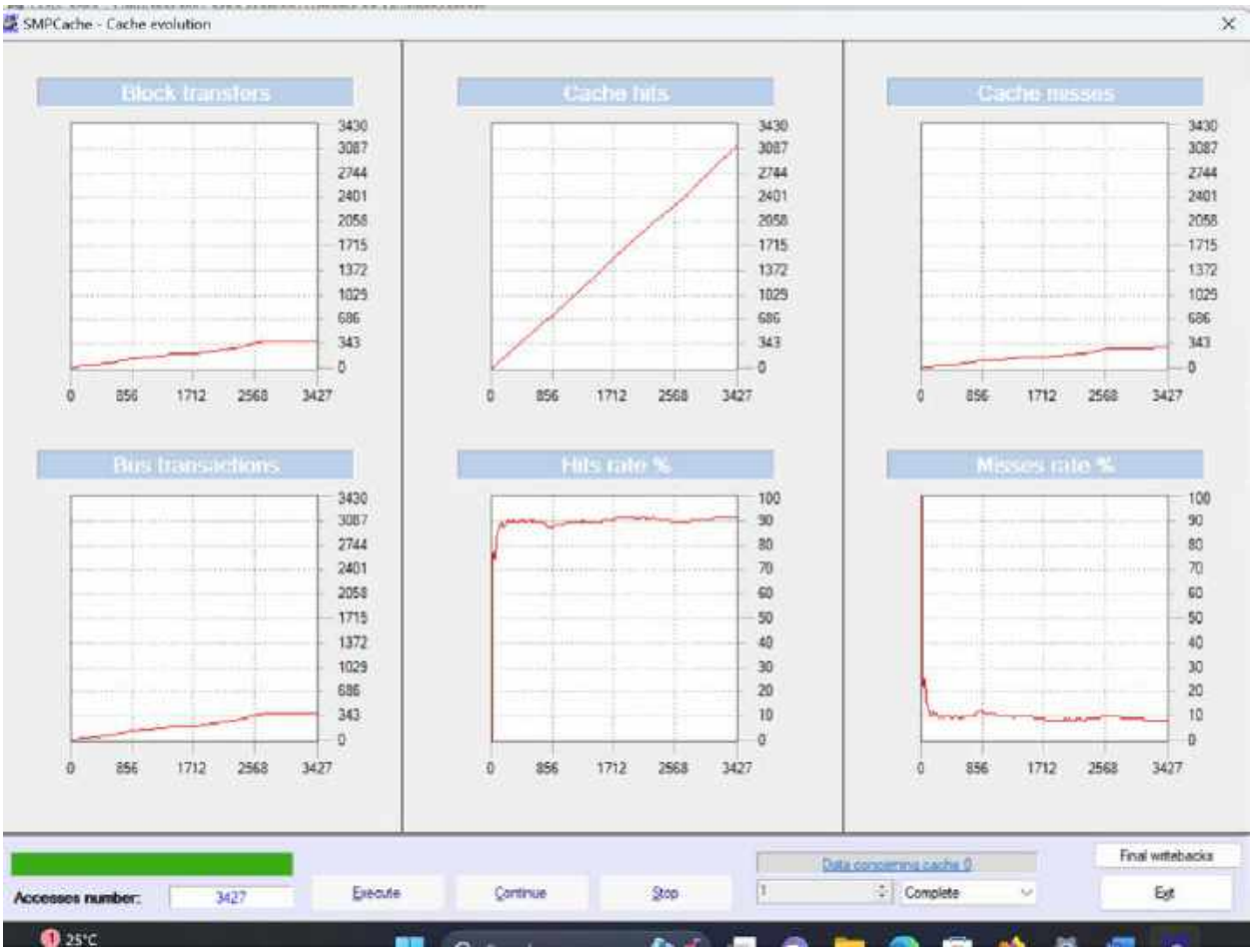

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

Configure main memory
Word wide (bits):
16
Words by block:
512
Blocks in main memory:
256
Block size:
1 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default

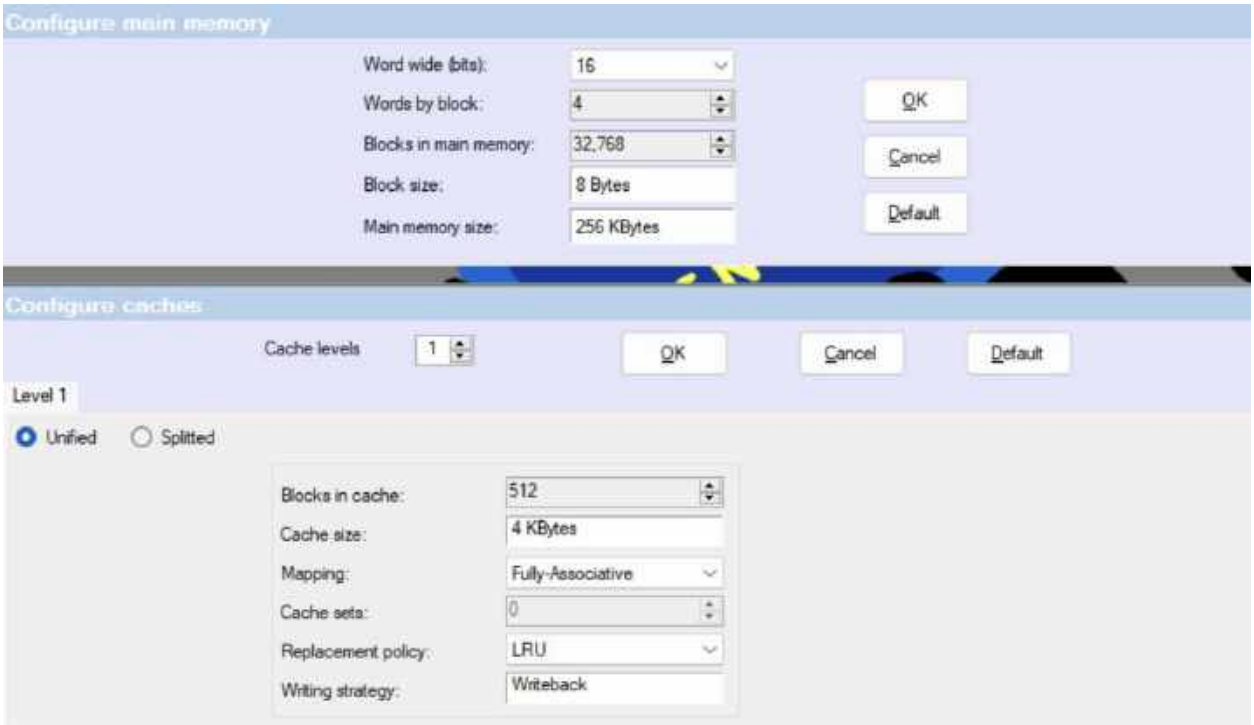

Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
4
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Modified (M)
118
3413
0001 (1)
Exclusive (E)
33
3427
0002 (2)
Exclusive (E)
15
3426
0003 (3)
Exclusive (E)
16
3421
Actual access
Access number:
3427
Access type:
Data reading
Address:
Block:
33
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
2791
172
Rate
94.195%
5.805%
Local readings
Global writings
415
49
89.440%
10.560%
Local writings
Global hits and misses
3206
221
93.551%
6.449%
Local hits and misses
Total replacements:
217
Cache level
Simulation steps:
Actual
Total
Accesses
Instructions
2709
Data readings
254
Data writings
464
Execute
Continue
Stop
Complete
Exit
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:

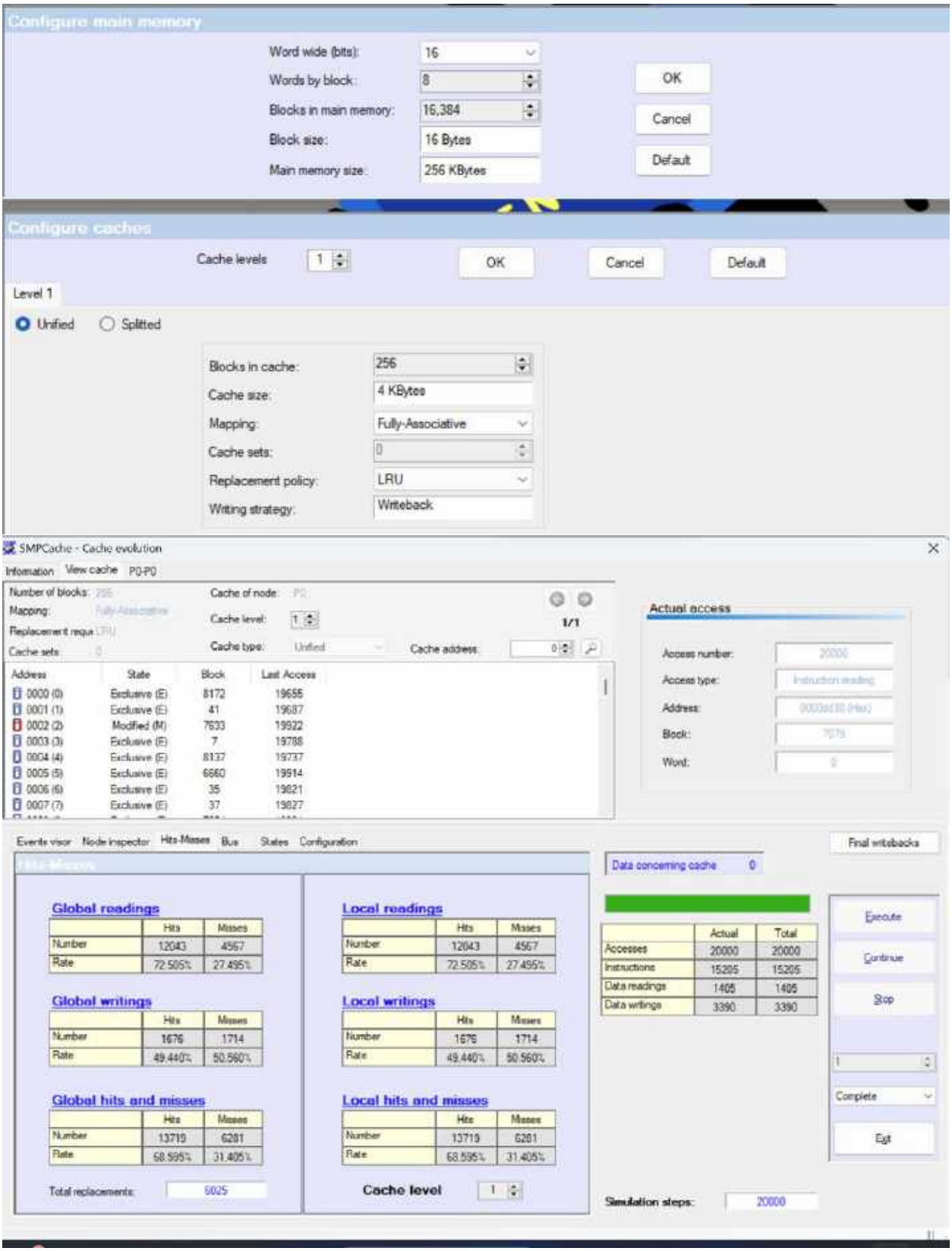

Configure main memory
Word wide (bits): 16
Words by block: 1,024
Blocks in main memory: 128
Block size: 2 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 2
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks: 2
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 7 3426
0001 (1) Exclusive (E) 16 3427
Actual access
Access number: 3427
Access type: Data reading
Address: 000042bf (Hex)
Block: 16
Word: 751
Events view
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2756 207
Rate 93.014% 6.986%
Global writings
Hits Misses
Number 390 74
Rate 84.052% 15.948%
Global hits and misses
Hits Misses
Number 3146 281
Rate 91.800% 8.200%
Total replacements: 279
Local readings
Hits Misses
Number 2756 207
Rate 93.014% 6.986%
Local writings
Hits Misses
Number 390 74
Rate 84.052% 15.948%
Local hits and misses
Hits Misses
Number 3146 281
Rate 91.800% 8.200%
Cache level 1
Actual Total
Accesses 3427 3427
Instructions 2709 2709
Data readings 254 254
Data writings 464 464
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3427

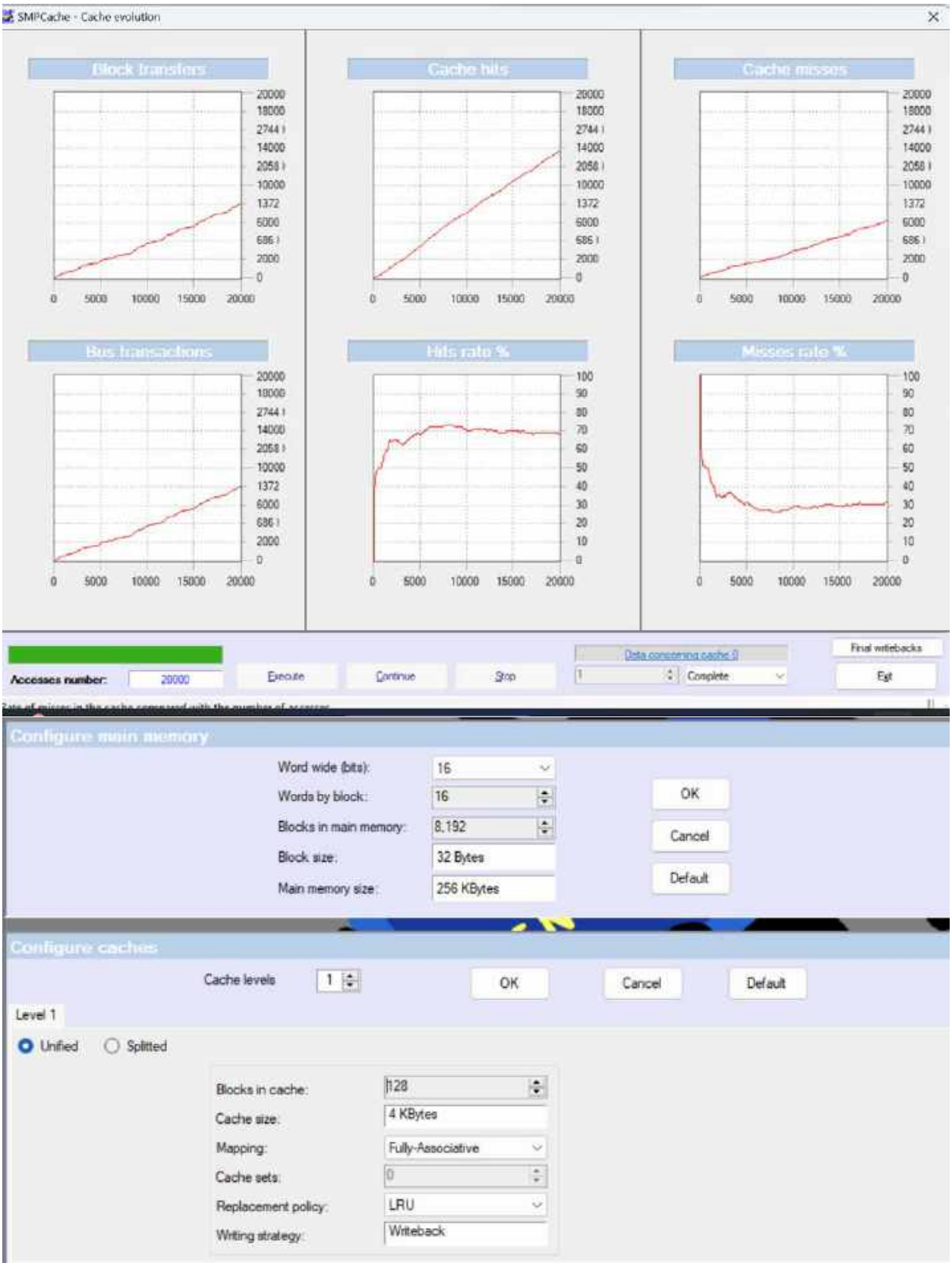

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

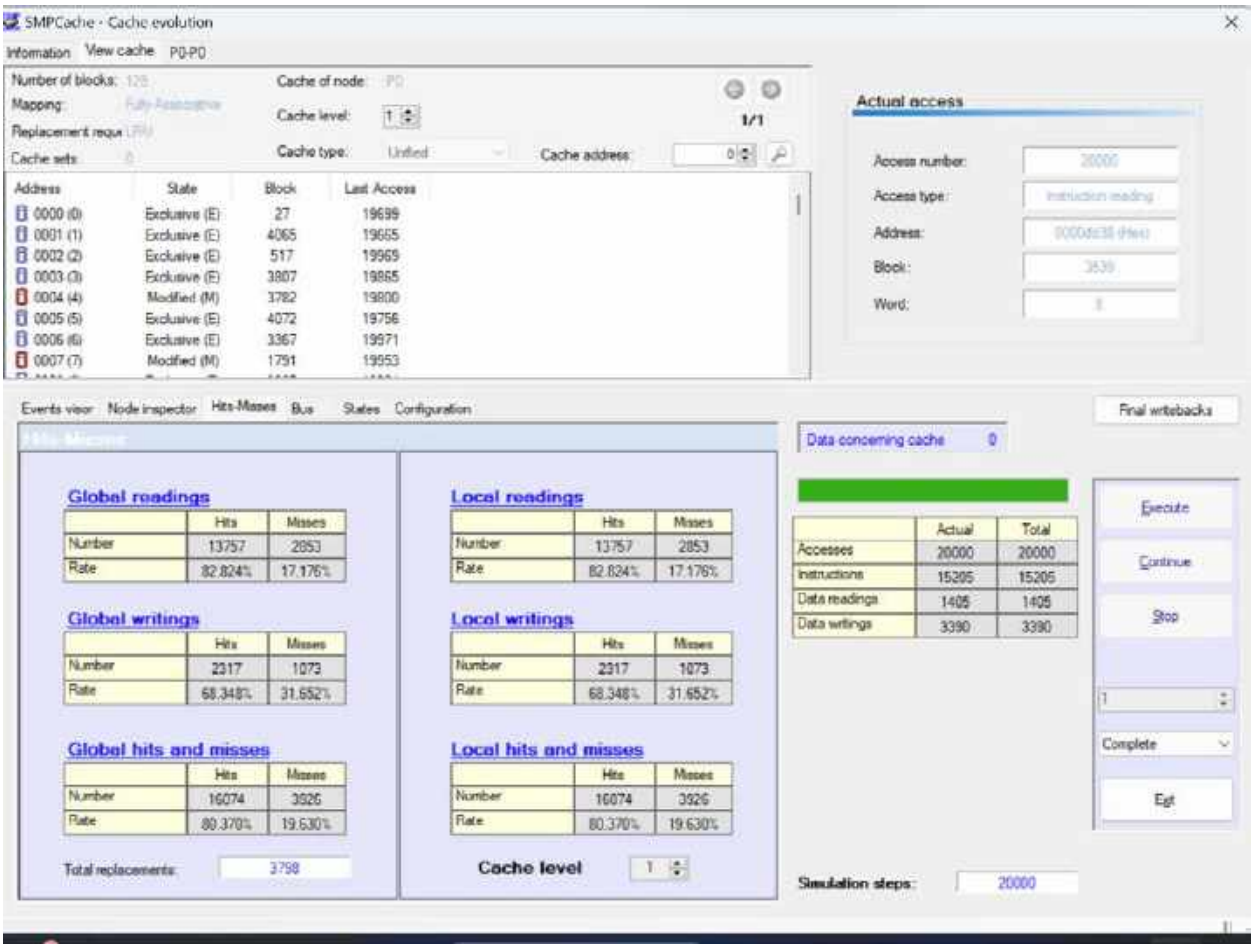
SWM

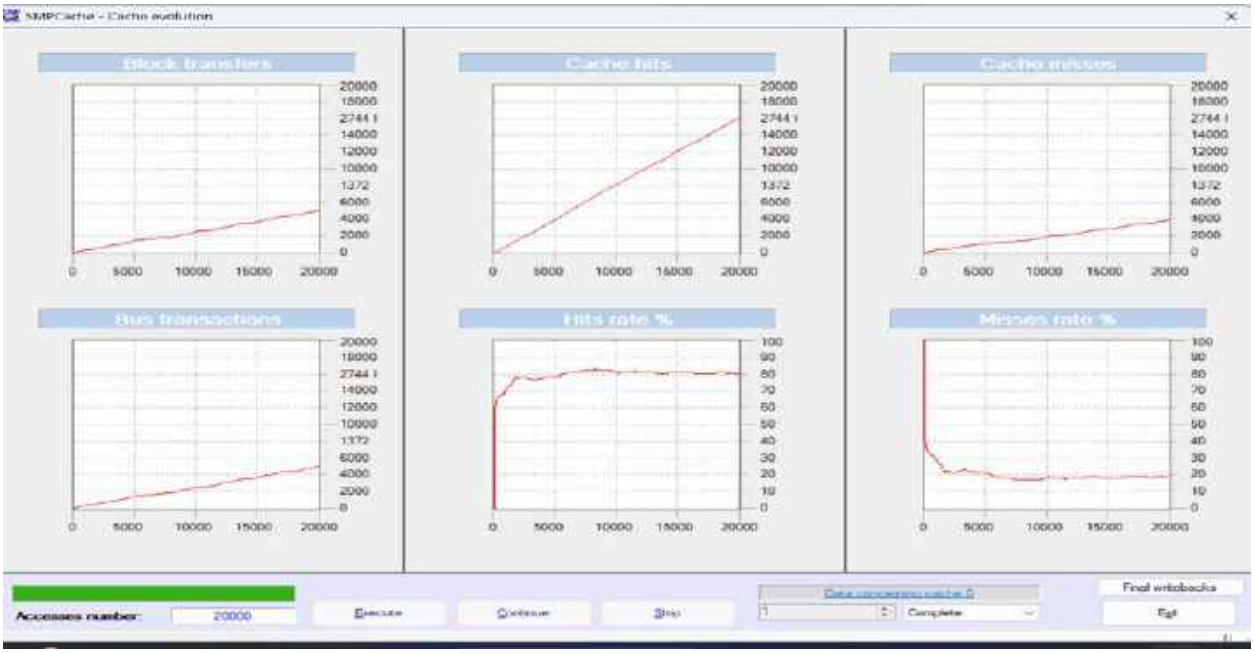

Configure main memory
Word wide (bits):
16
Words by block:
4
Blocks in main memory:
32,768
Block size:
8 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
512
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

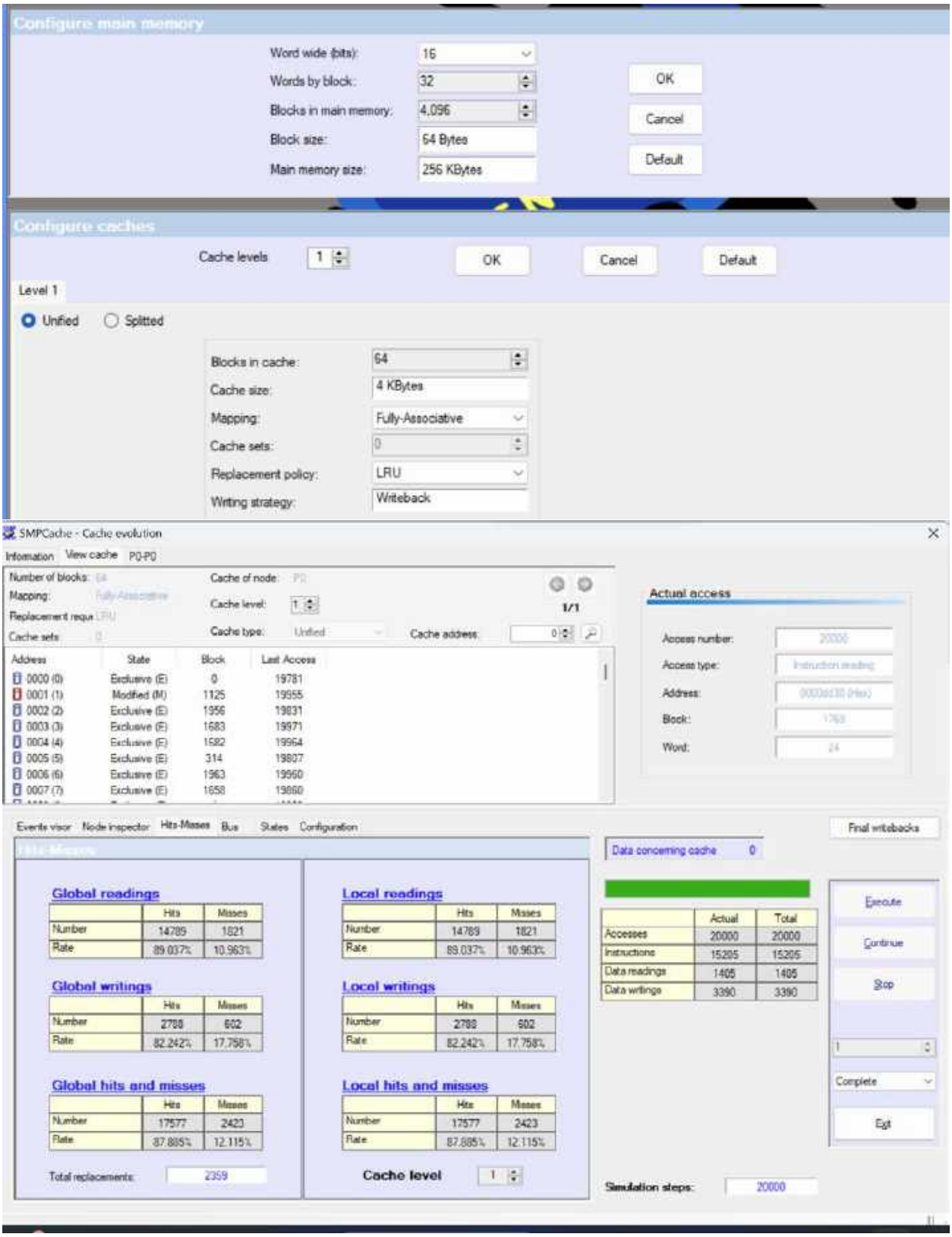
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 15466 19592
0001 (1) Exclusive (E) 14697 19591
0002 (2) Exclusive (E) 14155 19989
0003 (3) Exclusive (E) 5753 19622
0004 (4) Modified (M) 15130 19430
0005 (5) Exclusive (E) 15706 19930
0006 (6) Exclusive (E) 16276 19738
0007 (7) Exclusive (E) 16147 15487
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
Global readings
Hits
Misses
Number 8924 7686
Rate 53.727% 46.273%
Global writings
Number 427 2963
Rate 12.596% 87.404%
Global hits and misses
Number 9351 10649
Rate 46.755% 53.245%
Total replacements: 10137
Local readings
Number 8924 7686
Rate 53.727% 46.273%
Local writings
Number 427 2963
Rate 12.596% 87.404%
Local hits and misses
Number 9351 10649
Rate 46.755% 53.245%
Cache level
Actual
Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Final writebacks
Exit

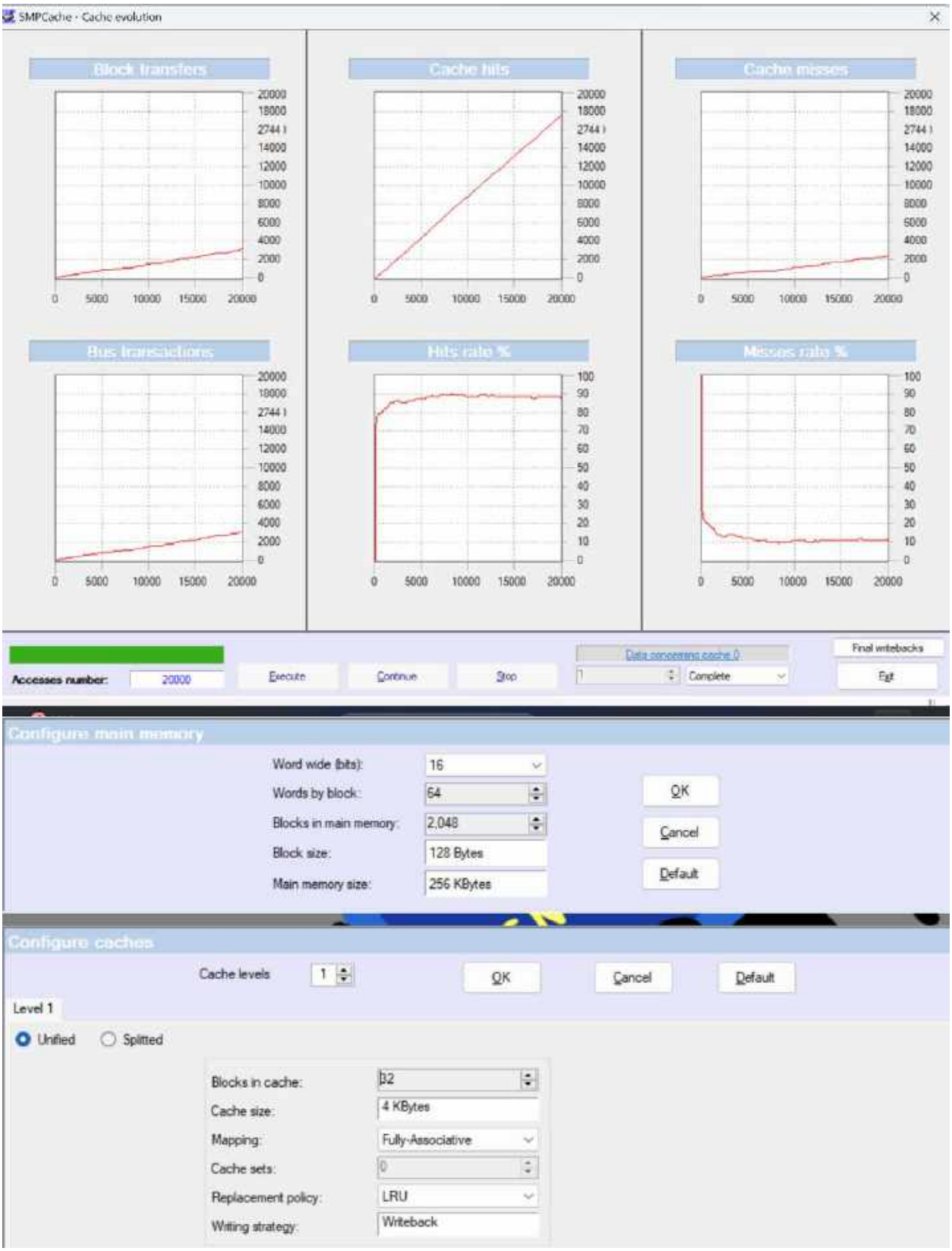

Configure main memory
Word wide (bits): 16
Words by block: 8
Blocks in main memory: 16,384
Block size: 16 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 256
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 8172 19655
0001 (1) Exclusive (E) 41 19687
0002 (2) Modified (M) 7633 19922
0003 (3) Exclusive (E) 7 19788
0004 (4) Exclusive (E) 8137 19737
0005 (5) Exclusive (E) 6660 19914
0006 (6) Exclusive (E) 35 19821
0007 (7) Exclusive (E) 37 19827
Actual access
Access number: 20000
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 12043 4567
Rate 72.505% 27.495%
Global writings
Hits Misses
Number 1676 1714
Rate 49.440% 50.560%
Global hits and misses
Hits Misses
Number 13719 6281
Rate 68.595% 31.405%
Total replacements: 6025
Local readings
Hits Misses
Number 12043 4567
Rate 72.505% 27.495%
Local writings
Hits Misses
Number 1676 1714
Rate 49.440% 50.560%
Local hits and misses
Hits Misses
Number 13719 6281
Rate 68.595% 31.405%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8,192
Block size:
32 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback


SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 27 19699
0001 (1) Exclusive (E) 4065 19665
0002 (2) Exclusive (E) 517 19969
0003 (3) Exclusive (E) 3807 19865
0004 (4) Modified (M) 3782 19800
0005 (5) Exclusive (E) 4072 19756
0006 (6) Exclusive (E) 3367 19971
0007 (7) Modified (M) 1791 19953
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 13757 2853
Rate 82.824% 17.176%
Global writings
Number 2317 1073
Rate 68.348% 31.652%
Global hits and misses
Number 16074 3926
Rate 80.370% 19.630%
Total replacements: 3798
Local readings
Number 13757 2853
Rate 82.824% 17.176%
Local writings
Number 2317 1073
Rate 68.348% 31.652%
Local hits and misses
Number 16074 3926
Rate 80.370% 19.630%
Cache level 1
Actual
Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
Complete
Exit
Simulation steps: 20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number: 20000
Execute
Continue
Stop
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits): 16
Words by block: 32
Blocks in main memory: 4,096
Block size: 64 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 64
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type: Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 0 19781
0001 (1) Modified (M) 1125 19955
0002 (2) Exclusive (E) 1956 19831
0003 (3) Exclusive (E) 1683 19971
0004 (4) Exclusive (E) 1582 19964
0005 (5) Exclusive (E) 314 19807
0006 (6) Exclusive (E) 1963 19960
0007 (7) Exclusive (E) 1658 19860
Actual access
Access number: 20000
Access type: Instruction reading
Address:
Block:
Word: 24
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 14789 1821
Rate 89.037% 10.963%
Global writings
Hits Misses
Number 2788 602
Rate 82.242% 17.758%
Global hits and misses
Hits Misses
Number 17577 2423
Rate 87.885% 12.115%
Total replacements: 2359
Local readings
Hits Misses
Number 14789 1821
Rate 89.037% 10.963%
Local writings
Hits Misses
Number 2788 602
Rate 82.242% 17.758%
Local hits and misses
Hits Misses
Number 17577 2423
Rate 87.885% 12.115%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
64
Blocks in main memory:
2,048
Block size:
128 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
32
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

SMPCache - Cache evolution

Information | View cache | P0-P0

Number of blocks: 32
Mapping: Fully Associative
Replacement requ: LRU
Cache sets: 0

Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0

1/1

Address	State	Block	Last Access
0000 (0)	Modified (M)	950	19915
0001 (1)	Exclusive (E)	883	19979
0002 (2)	Exclusive (E)	947	19839
0003 (3)	Exclusive (E)	981	19960
0004 (4)	Modified (M)	562	19955
0005 (5)	Exclusive (E)	952	19905
0006 (6)	Modified (M)	954	19966
0007 (7)	Exclusive (E)	100	19992

Actual access

Access number: 20000
Access type: Instruction reading
Address: 0000d030 (Hex)
Block: 884
Word: 56

Events visor | Node inspector | Hits-Misses | Bus | States | Configuration

Final writebacks

Data concerning cache 0

Global readings

	Hits	Misses
Number	15333	1277
Rate	92.312%	7.688%

Global writings

	Hits	Misses
Number	3041	349
Rate	89.705%	10.295%

Global hits and misses

	Hits	Misses
Number	18374	1626
Rate	91.870%	8.130%

Total replacements: 1594

Local readings

	Hits	Misses
Number	15333	1277
Rate	92.312%	7.688%

Local writings

	Hits	Misses
Number	3041	349
Rate	89.705%	10.295%

Local hits and misses

	Hits	Misses
Number	18374	1626
Rate	91.870%	8.130%

Cache level 1

	Actual	Total
Accesses	20000	20000
Instructions	15205	15205
Data readings	1405	1405
Data writings	3390	3390

Execute
Continue
Stop
1
Complete
Exit

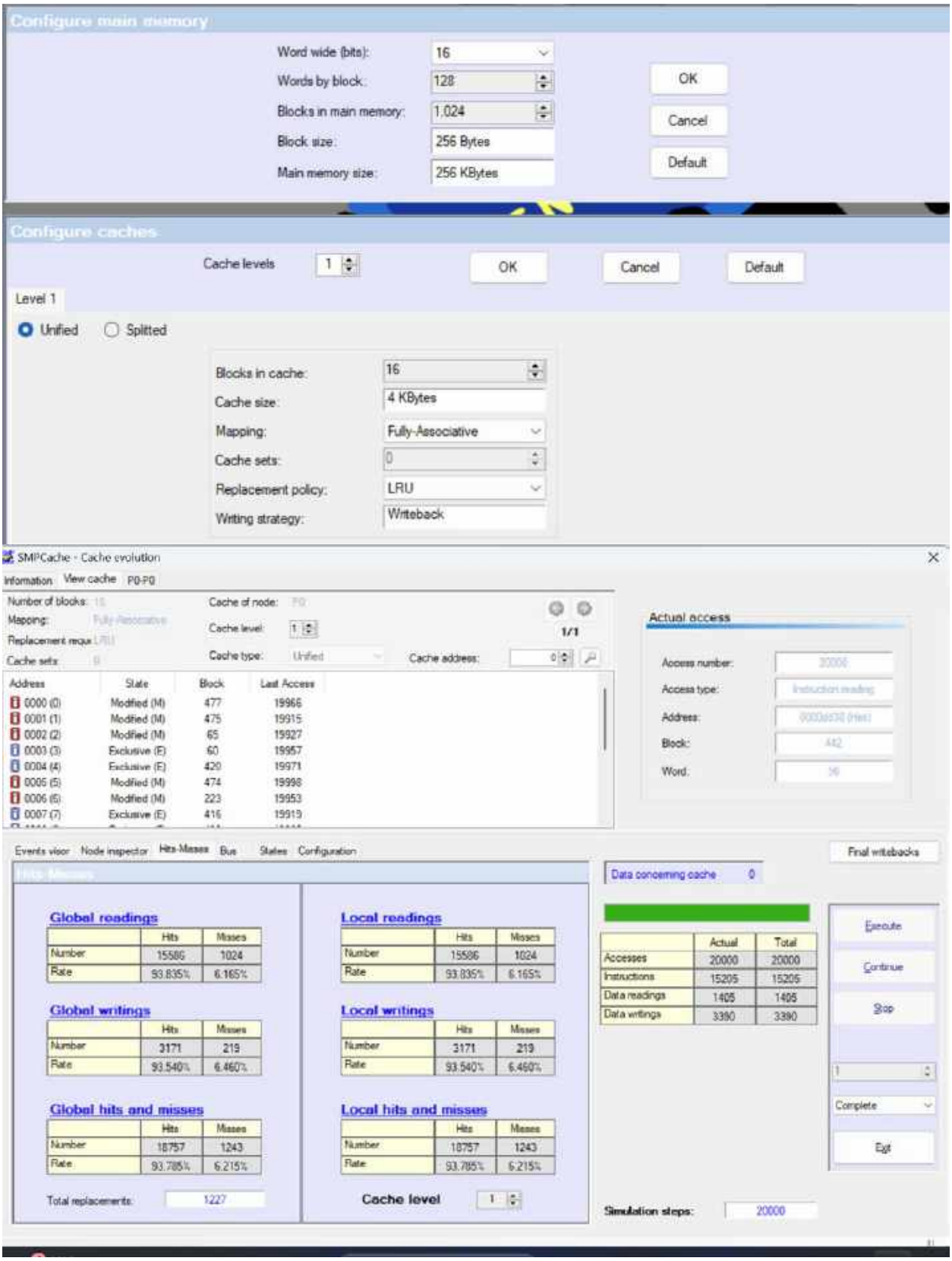
Simulation steps: 20000

SMPCache - Cache evolution

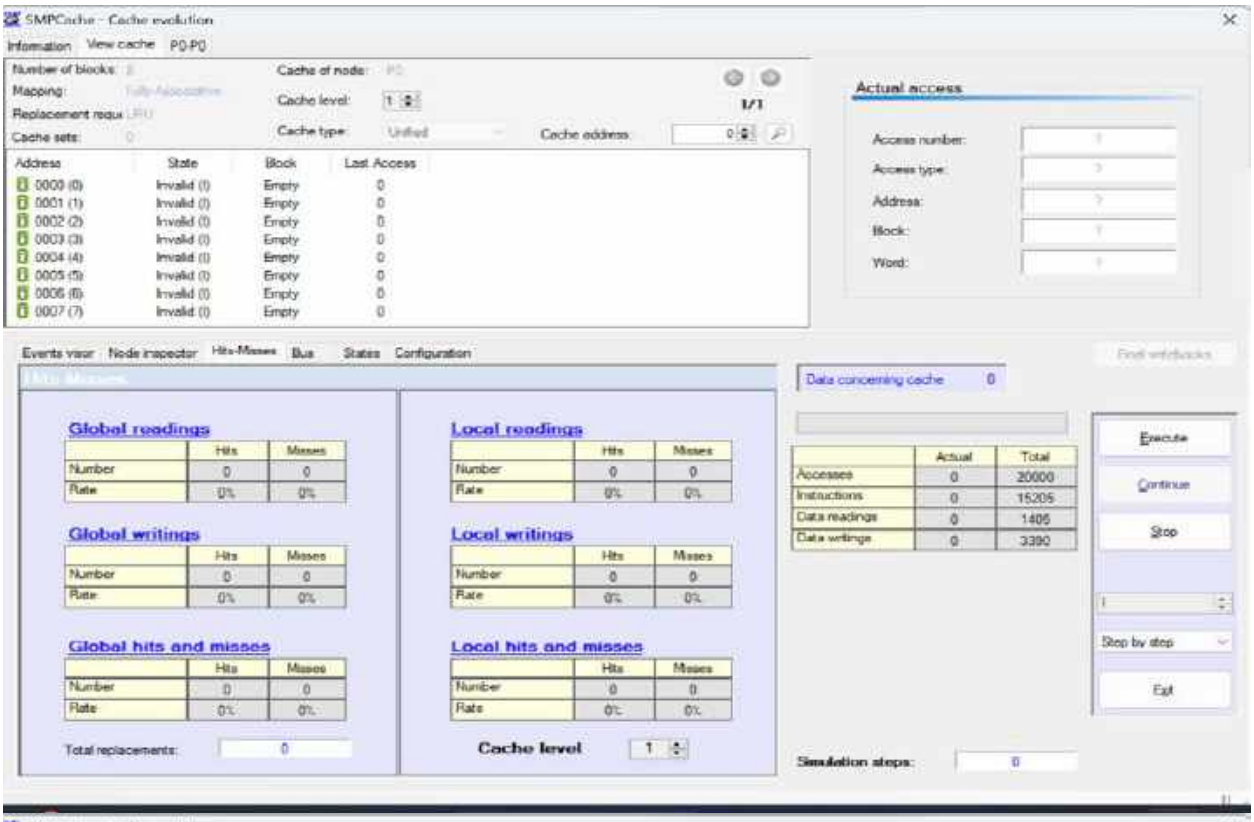
Block transfers | Cache hits | Cache misses

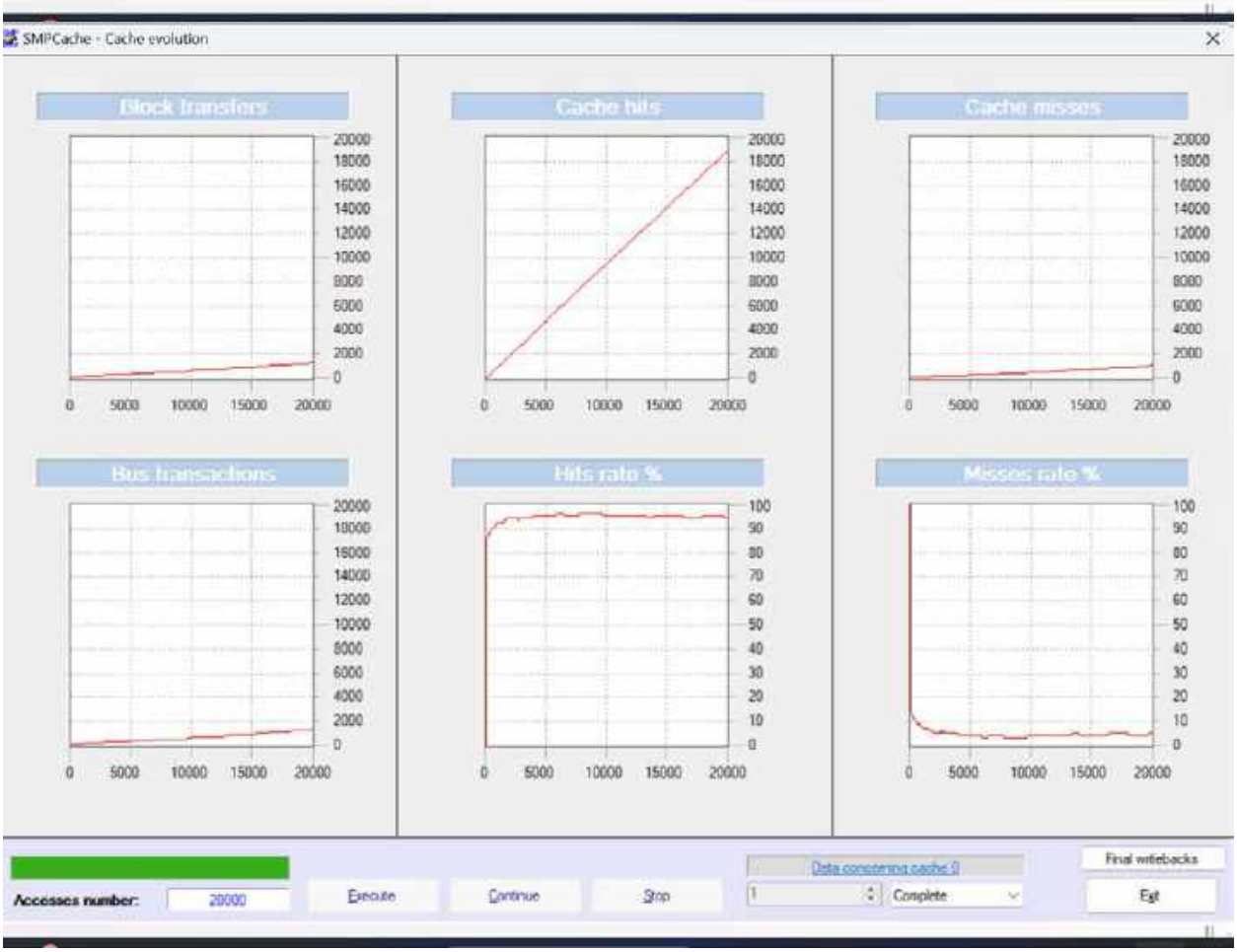
Bus transactions | Hits ratio % | Misses ratio %

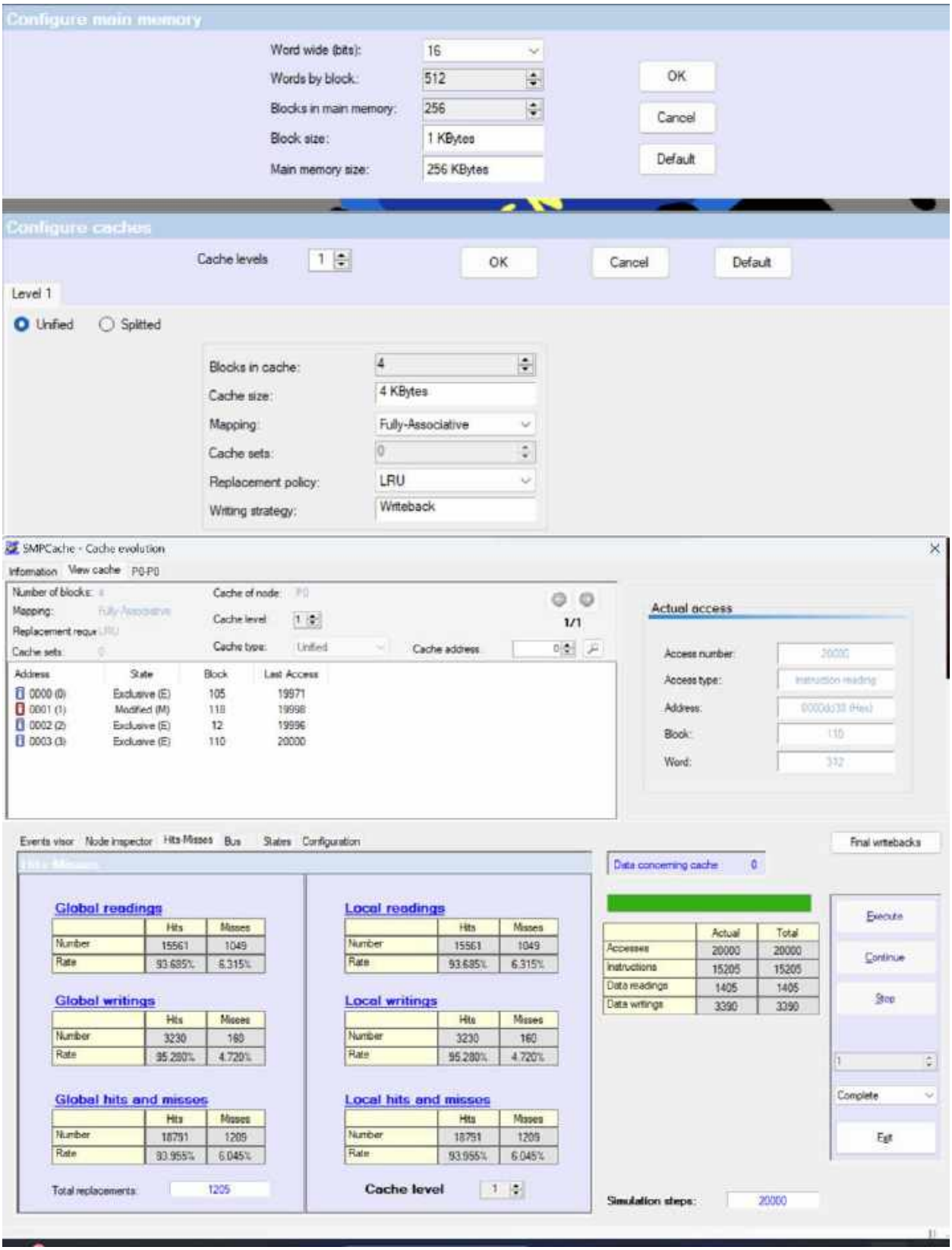
Accesses number: 20000 | Execute | Continue | Stop | Data concerning cache 0 | 1 | Complete | Final writebacks | Exit

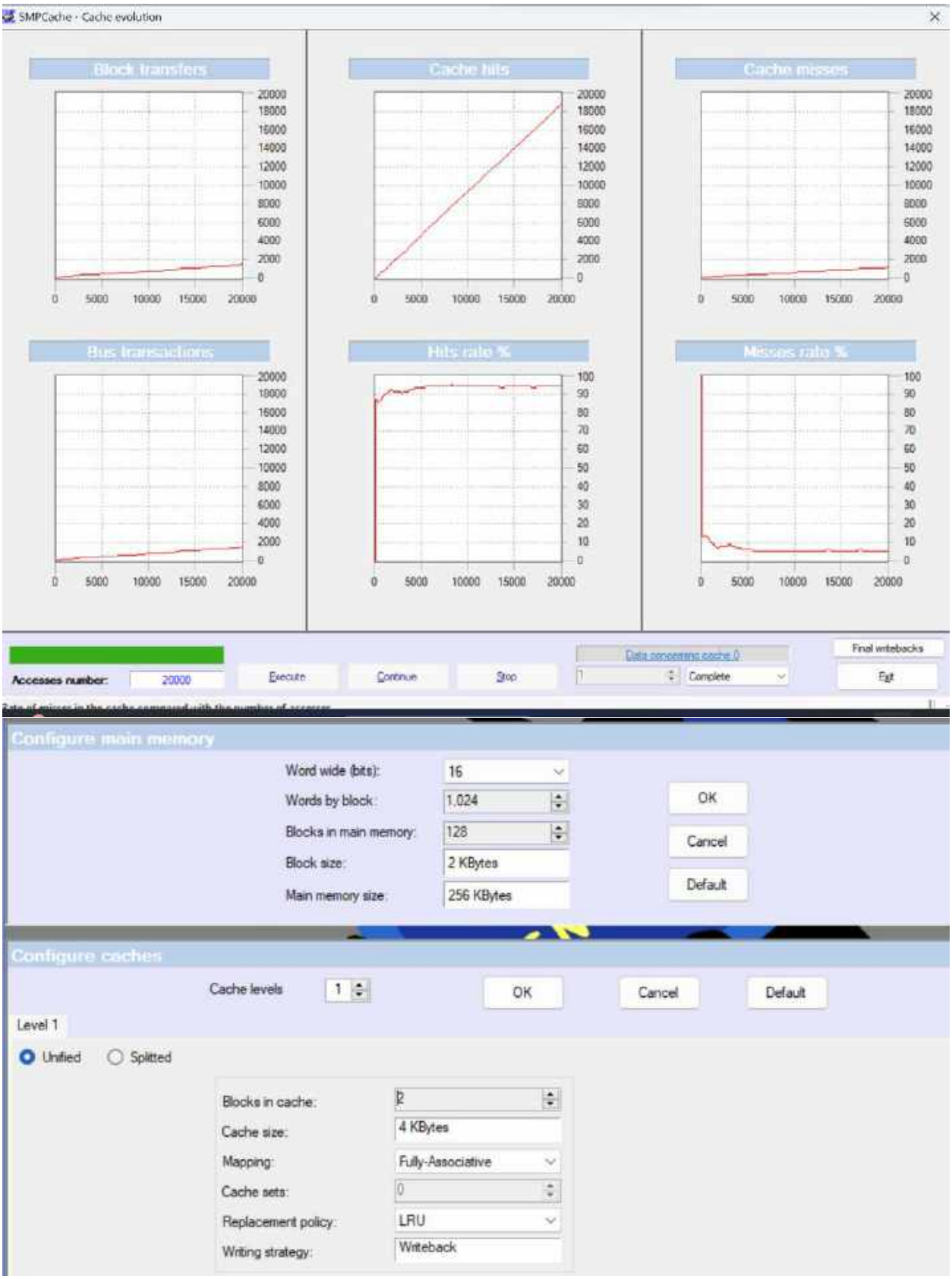

Configure main memory
Word wide (bits): 16
Words by block: 128
Blocks in main memory: 1,024
Block size: 256 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 16
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 477 19966
0001 (1) Modified (M) 475 19915
0002 (2) Modified (M) 65 19927
0003 (3) Exclusive (E) 60 19957
0004 (4) Exclusive (E) 420 19971
0005 (5) Modified (M) 474 19998
0006 (6) Modified (M) 223 19953
0007 (7) Exclusive (E) 416 19919
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 15586 1024
Rate 93.835% 6.165%
Global writings
Hits Misses
Number 3171 219
Rate 93.540% 6.460%
Global hits and misses
Hits Misses
Number 18757 1243
Rate 93.785% 6.215%
Total replacements: 1227
Local readings
Hits Misses
Number 15586 1024
Rate 93.835% 6.165%
Local writings
Hits Misses
Number 3171 219
Rate 93.540% 6.460%
Local hits and misses
Hits Misses
Number 18757 1243
Rate 93.785% 6.215%
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000

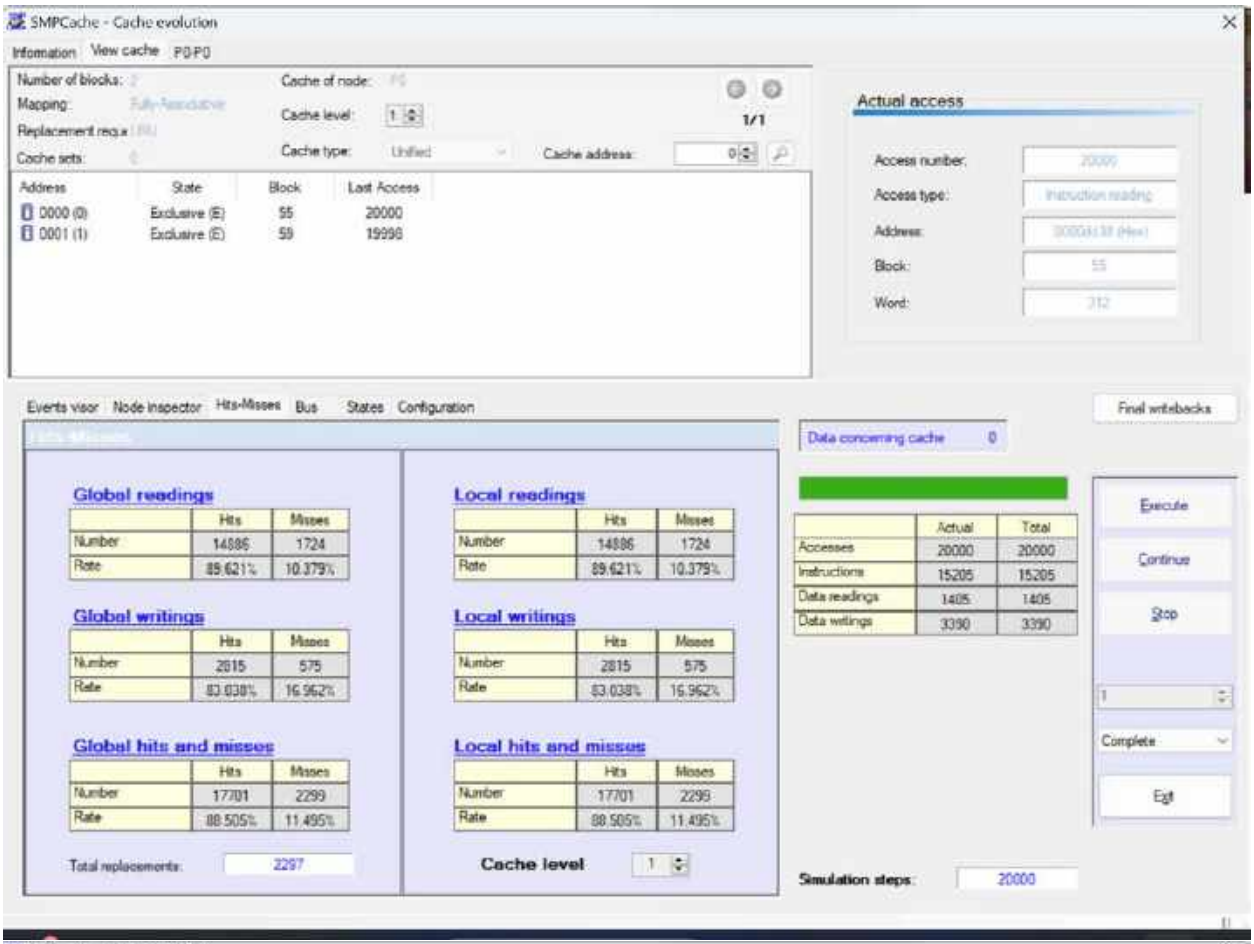
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
256
Blocks in main memory:
512
Block size:
512 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

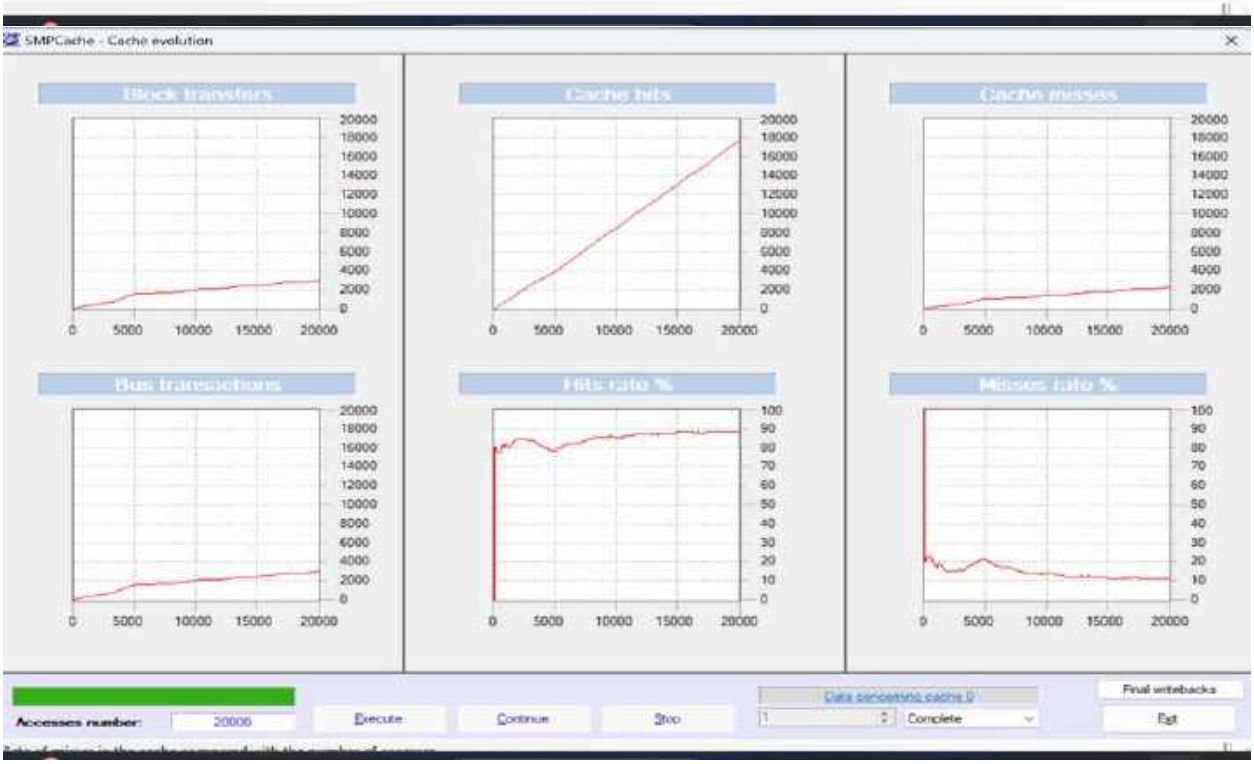

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.:
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Invalid (I) Empty 0
0001 (1) Invalid (I) Empty 0
0002 (2) Invalid (I) Empty 0
0003 (3) Invalid (I) Empty 0
0004 (4) Invalid (I) Empty 0
0005 (5) Invalid (I) Empty 0
0006 (6) Invalid (I) Empty 0
0007 (7) Invalid (I) Empty 0
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events viewer
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits
Misses
Number 0 0
Rate 0% 0%
Global writings
Number 0 0
Rate 0% 0%
Global hits and misses
Number 0 0
Rate 0% 0%
Total replacements: 0
Local readings
Number 0 0
Rate 0% 0%
Local writings
Number 0 0
Rate 0% 0%
Local hits and misses
Number 0 0
Rate 0% 0%
Cache level 1
Actual
Total
Accesses 0 20000
Instructions 0 15205
Data readings 0 1406
Data writings 0 3390
Execute
Continue
Stop
Stop by step
Exit
Simulation steps: 0


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 5000 10000 15000 20000
0 2000 4000 6000 8000 10000 12000 14000 16000 18000 20000
0 10 20 30 40 50 60 70 80 90 100
Accesses number: 20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

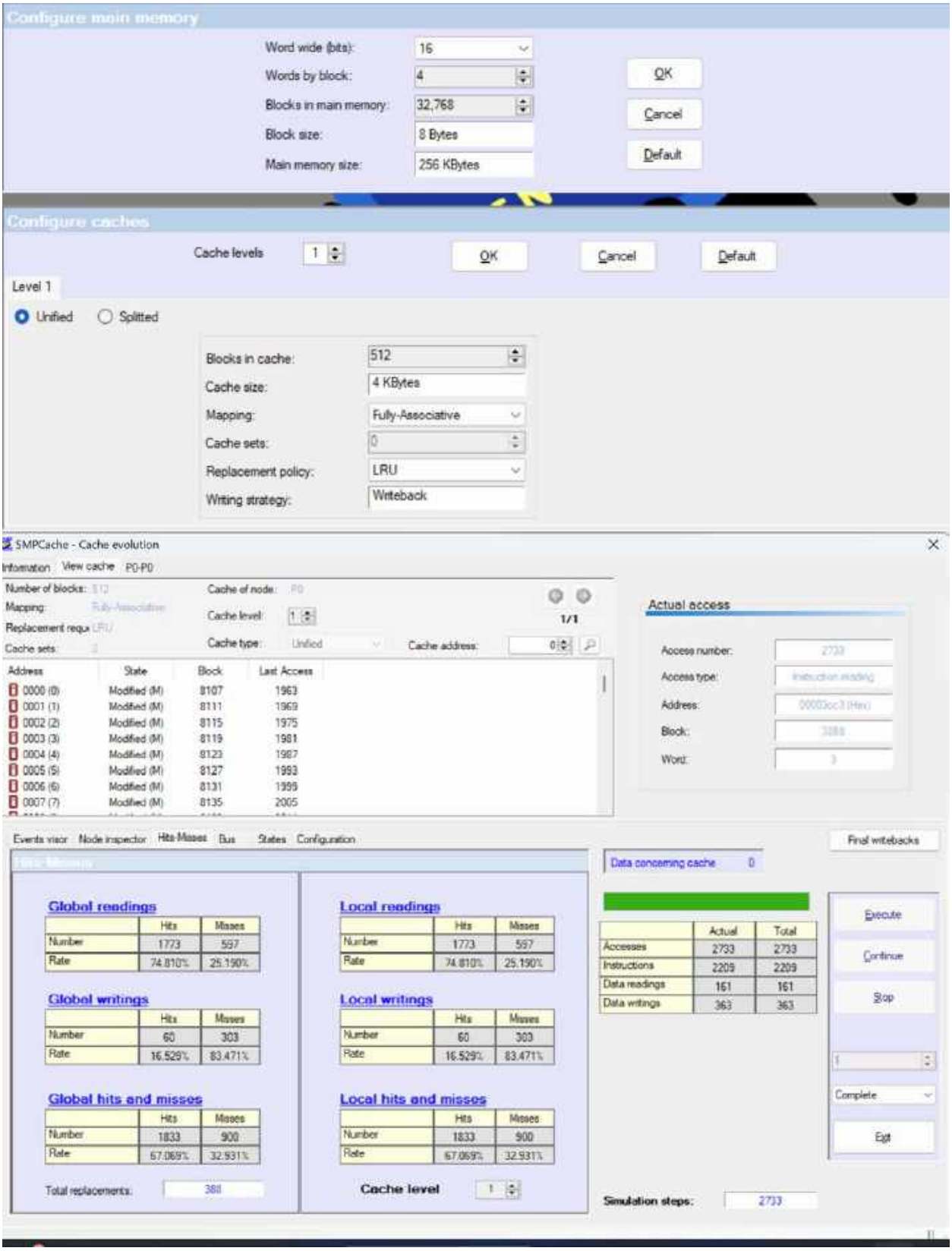

Configure main memory
Word wide (bits): 16
Words by block: 512
Blocks in main memory: 256
Block size: 1 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 4
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node: P0
Cache level 1
Cache type: Unified
Cache address 0
1/1
Address State Block Last Access
0000 (0) Exclusive (E) 105 19971
0001 (1) Modified (M) 110 19998
0002 (2) Exclusive (E) 12 19996
0003 (3) Exclusive (E) 110 20000
Actual access
Access number: 20000
Access type: Instruction reading
Address: 0000da38 (Hex)
Block: 110
Word: 332
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 15561 1049
Rate 93.685% 6.315%
Local readings
Hits Misses
Number 15561 1049
Rate 93.685% 6.315%
Global writings
Hits Misses
Number 3230 160
Rate 95.280% 4.720%
Local writings
Hits Misses
Number 3230 160
Rate 95.280% 4.720%
Global hits and misses
Hits Misses
Number 18791 1209
Rate 93.955% 6.045%
Local hits and misses
Hits Misses
Number 18791 1209
Rate 93.955% 6.045%
Total replacements: 1205
Cache level 1
Actual Total
Accesses 20000 20000
Instructions 15205 15205
Data readings 1405 1405
Data writings 3390 3390
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
1,024
Blocks in main memory:
128
Block size:
2 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
2
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback


SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ.:
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0)
Exclusive (E)
55
20000
0001 (1)
Exclusive (E)
59
19998
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number
14886
1724
Rate
89.621%
10.379%
Global writings
2815
575
83.038%
16.962%
Global hits and misses
17701
2299
88.505%
11.495%
Total replacements:
2297
Local readings
Local writings
Local hits and misses
Cache level
Actual
Total
Accesses
20000
Instructions
15205
Data readings
1405
Data writings
3390
Execute
Continue
Stop
Complete
Exit
Simulation steps:
20000


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

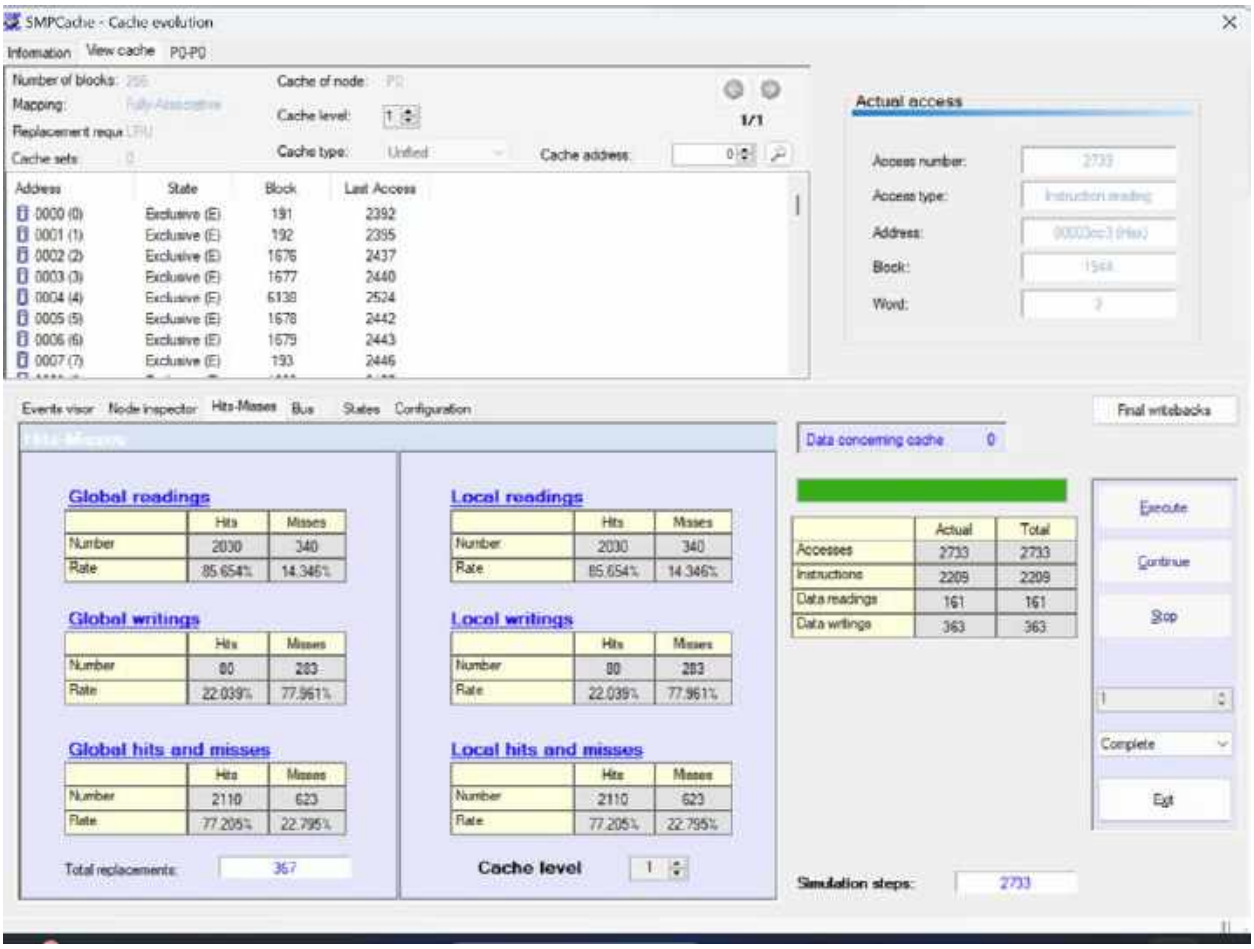
UCOMP

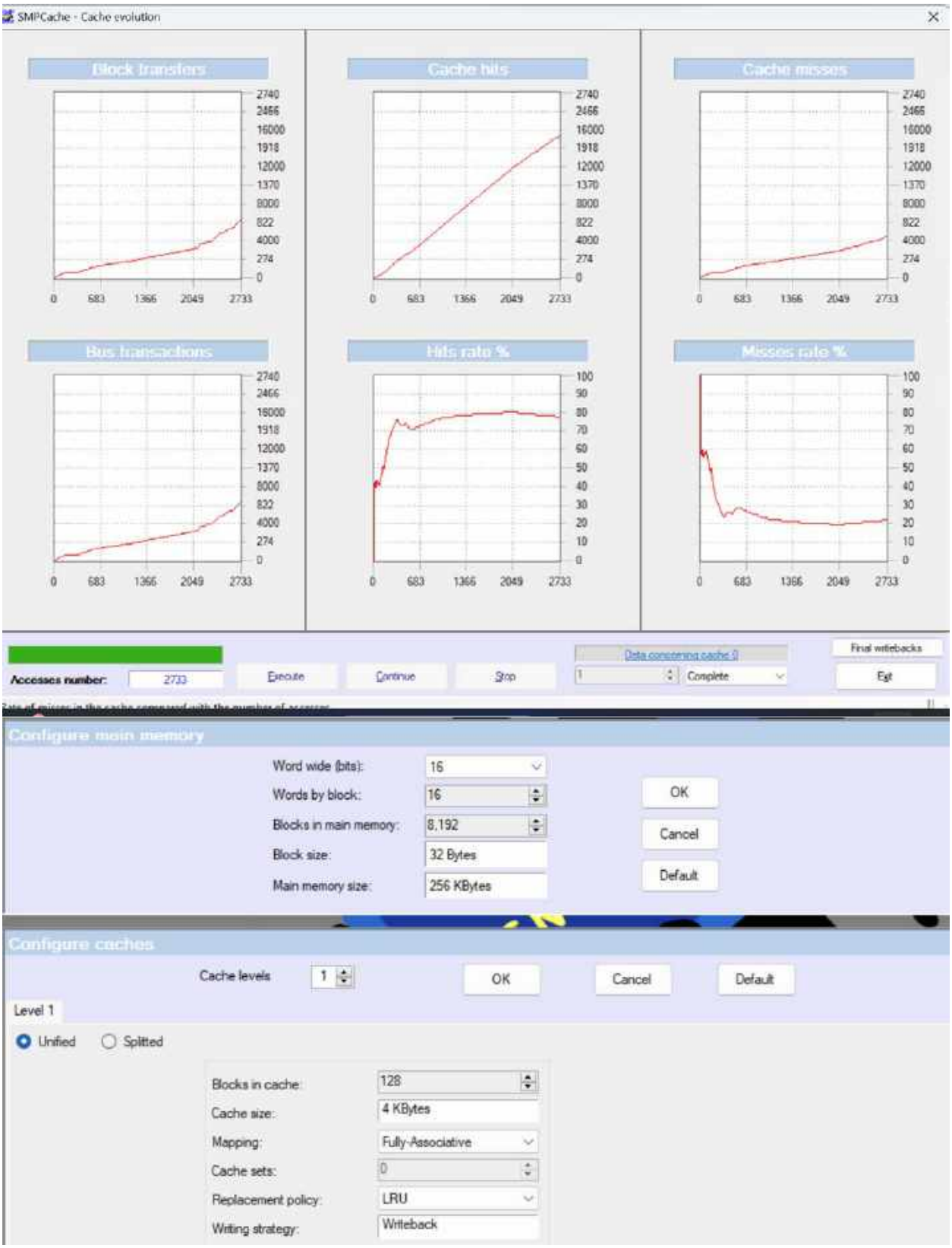

Configure main memory
Word wide (bits): 16
Words by block: 4
Blocks in main memory: 32,768
Block size: 8 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 512
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 512
Mapping: Fully-Associative
Replacement requ LRU
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 8107 1963
0001 (1) Modified (M) 8111 1969
0002 (2) Modified (M) 8115 1975
0003 (3) Modified (M) 8119 1981
0004 (4) Modified (M) 8123 1987
0005 (5) Modified (M) 8127 1993
0006 (6) Modified (M) 8131 1999
0007 (7) Modified (M) 8135 2005
Actual access
Access number: 2733
Access type: Instruction reading
Address: 0000ac3 (Hex)
Block: 3888
Word: 3
Events visor Node inspector Hits-Misses Bus States Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 1773 597
Rate 74.810% 25.190%
Global writings
Hits Misses
Number 60 303
Rate 16.529% 83.471%
Global hits and misses
Hits Misses
Number 1833 900
Rate 67.069% 32.931%
Total replacements: 388
Local readings
Hits Misses
Number 1773 597
Rate 74.810% 25.190%
Local writings
Hits Misses
Number 60 303
Rate 16.529% 83.471%
Local hits and misses
Hits Misses
Number 1833 900
Rate 67.069% 32.931%
Cache level 1
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2733

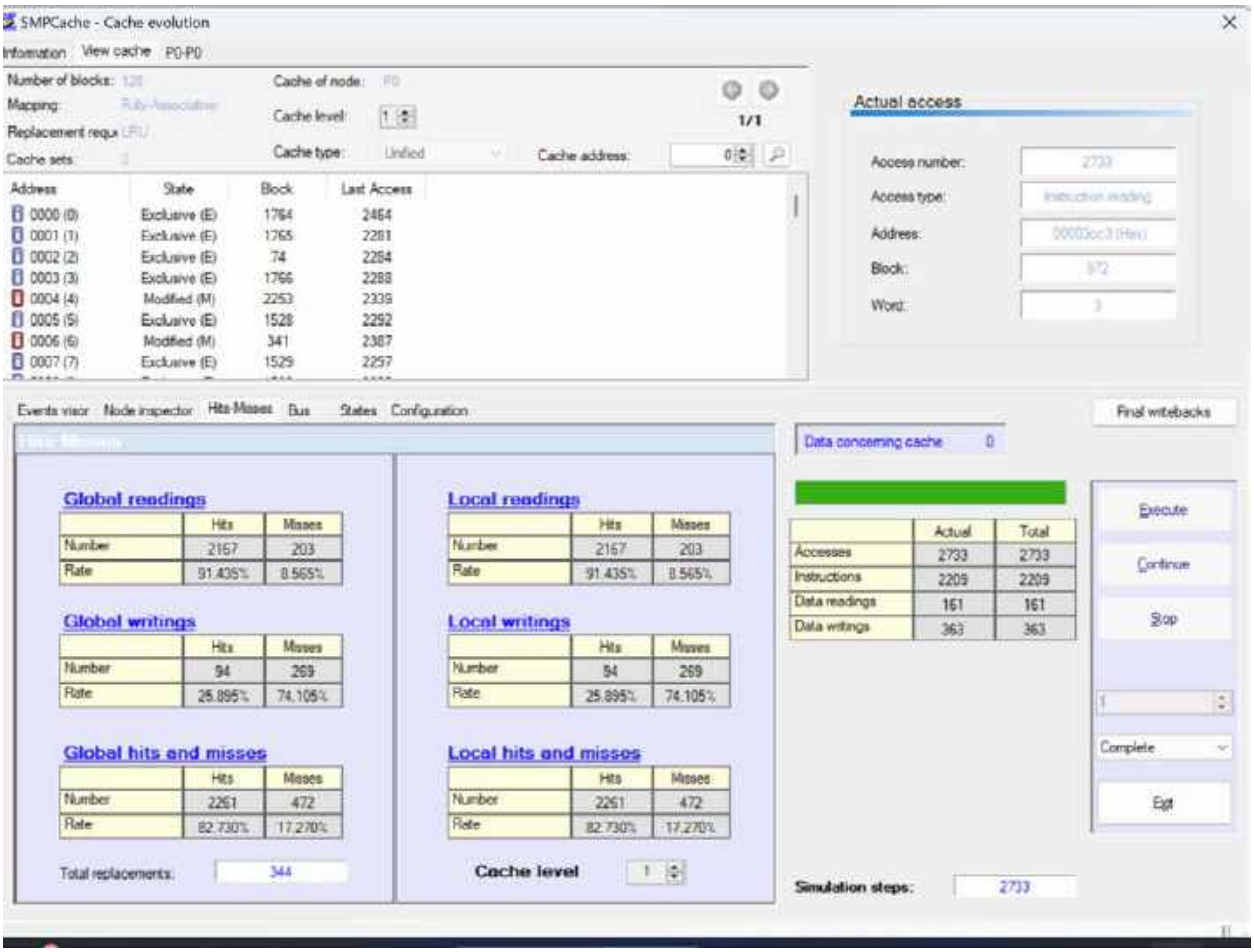
SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

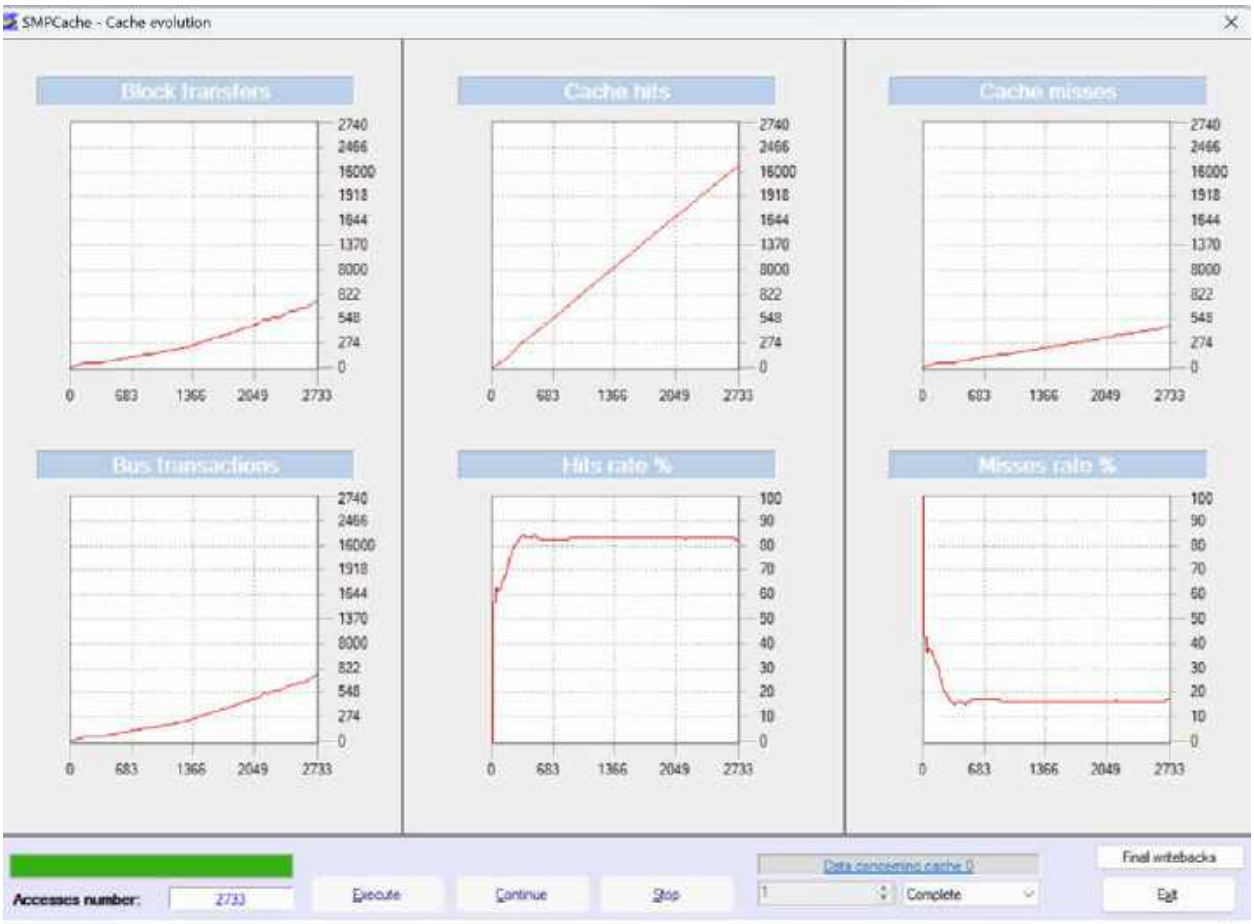
UCOMP

Configure main memory
Word wide (bits): 16
Words by block: 8
Blocks in main memory: 16.384
Block size: 16 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 256
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

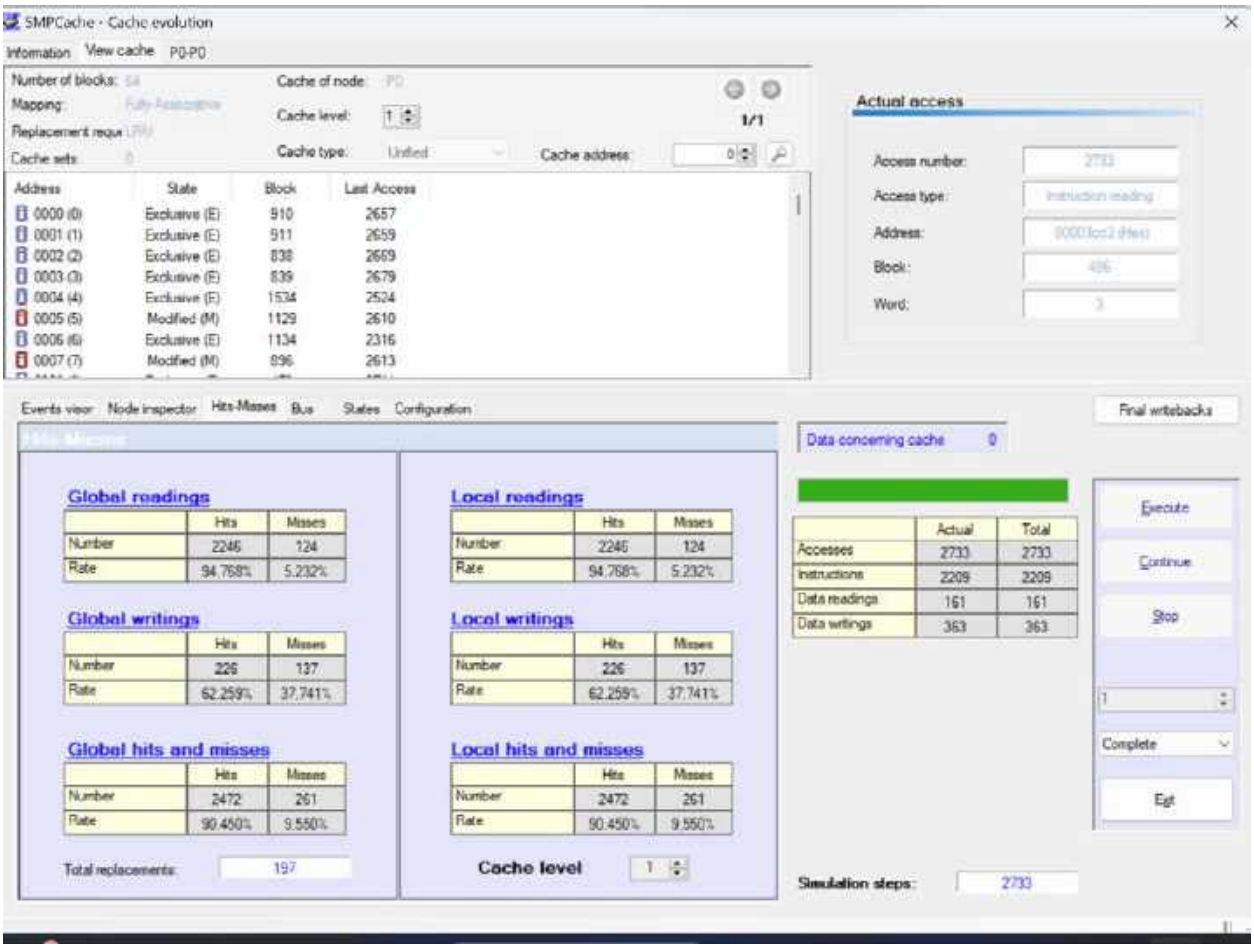

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 191 2392
0001 (1) Exclusive (E) 192 2395
0002 (2) Exclusive (E) 1676 2437
0003 (3) Exclusive (E) 1677 2440
0004 (4) Exclusive (E) 6138 2524
0005 (5) Exclusive (E) 1678 2442
0006 (6) Exclusive (E) 1679 2443
0007 (7) Exclusive (E) 193 2446
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2030 340
Rate 85.654% 14.346%
Global writings
Hits Misses
Number 80 283
Rate 22.039% 77.961%
Global hits and misses
Hits Misses
Number 2110 623
Rate 77.205% 22.795%
Total replacements: 367
Local readings
Hits Misses
Number 2030 340
Rate 85.654% 14.346%
Local writings
Hits Misses
Number 80 283
Rate 22.039% 77.961%
Local hits and misses
Hits Misses
Number 2110 623
Rate 77.205% 22.795%
Cache level 1
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2733

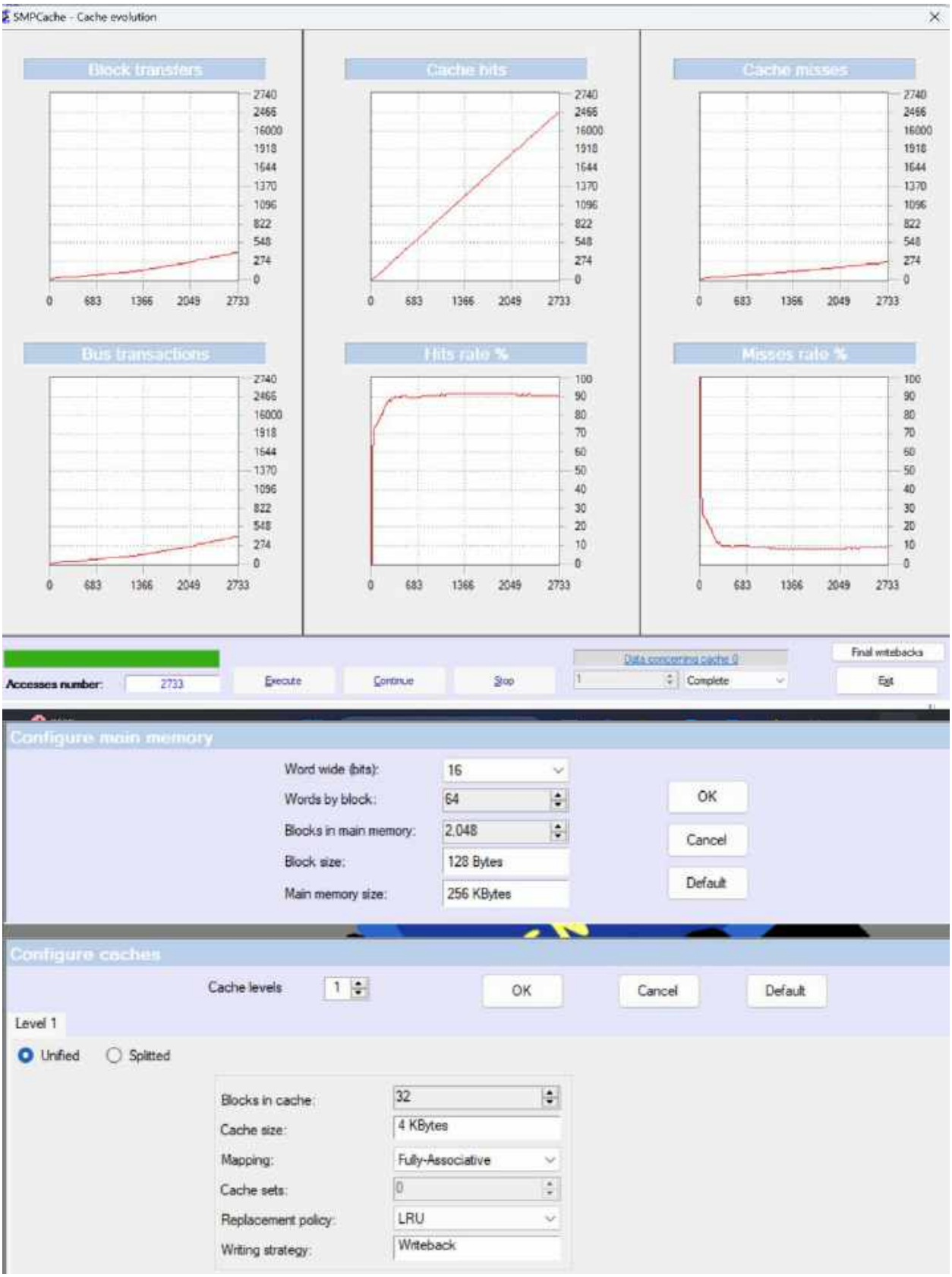

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8,192
Block size:
32 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

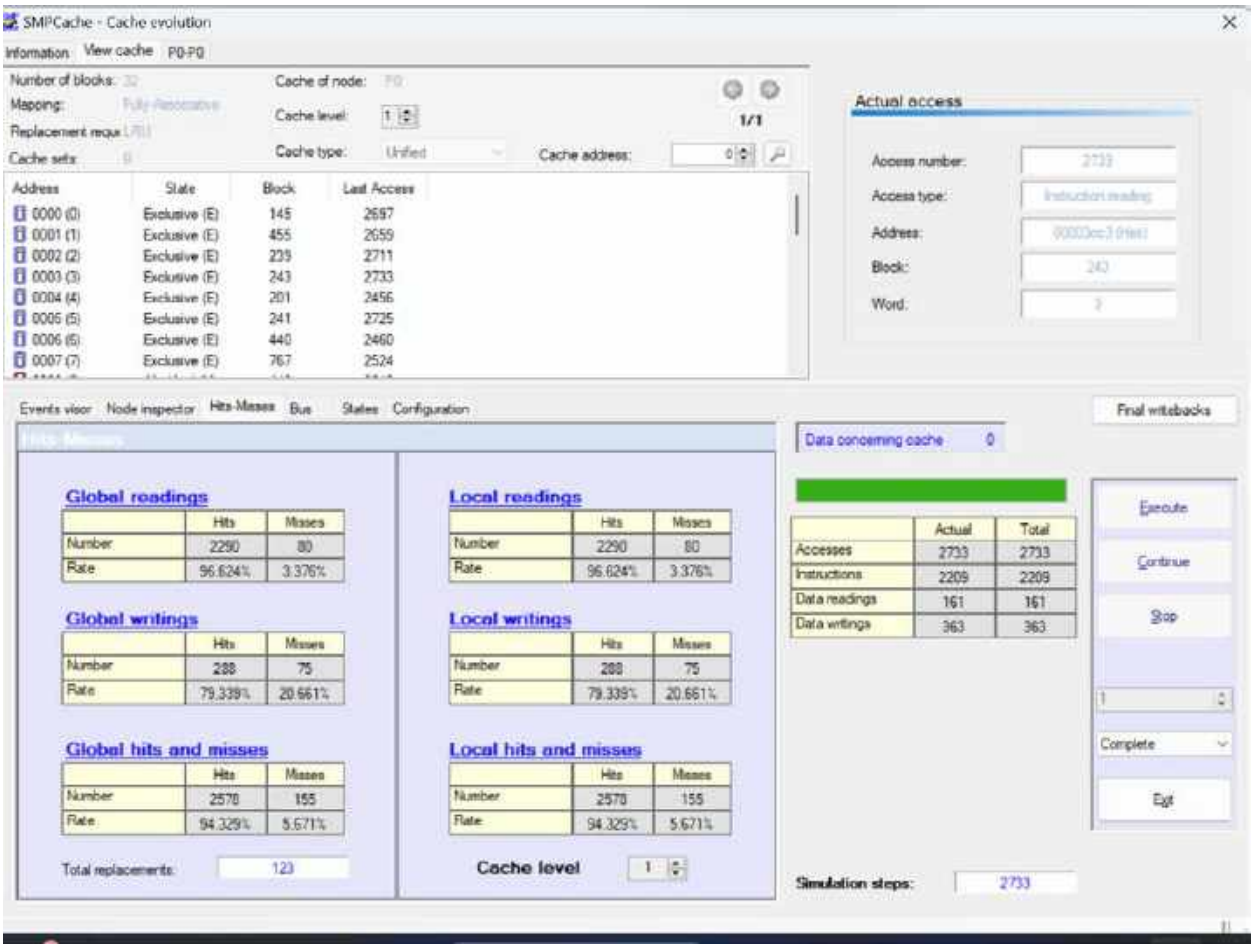

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 1764 2464
0001 (1) Exclusive (E) 1765 2281
0002 (2) Exclusive (E) 74 2284
0003 (3) Exclusive (E) 1766 2288
0004 (4) Modified (M) 2253 2339
0005 (5) Exclusive (E) 1528 2292
0006 (6) Modified (M) 341 2387
0007 (7) Exclusive (E) 1529 2257
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number 2157 203
Rate 91.435% 8.565%
Global writings
Number 94 269
Rate 25.895% 74.105%
Global hits and misses
Number 2261 472
Rate 82.730% 17.270%
Total replacements:
344
Local readings
Number 2157 203
Rate 91.435% 8.565%
Local writings
Number 94 269
Rate 25.895% 74.105%
Local hits and misses
Number 2261 472
Rate 82.730% 17.270%
Cache level
1
Actual
Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps:
2733

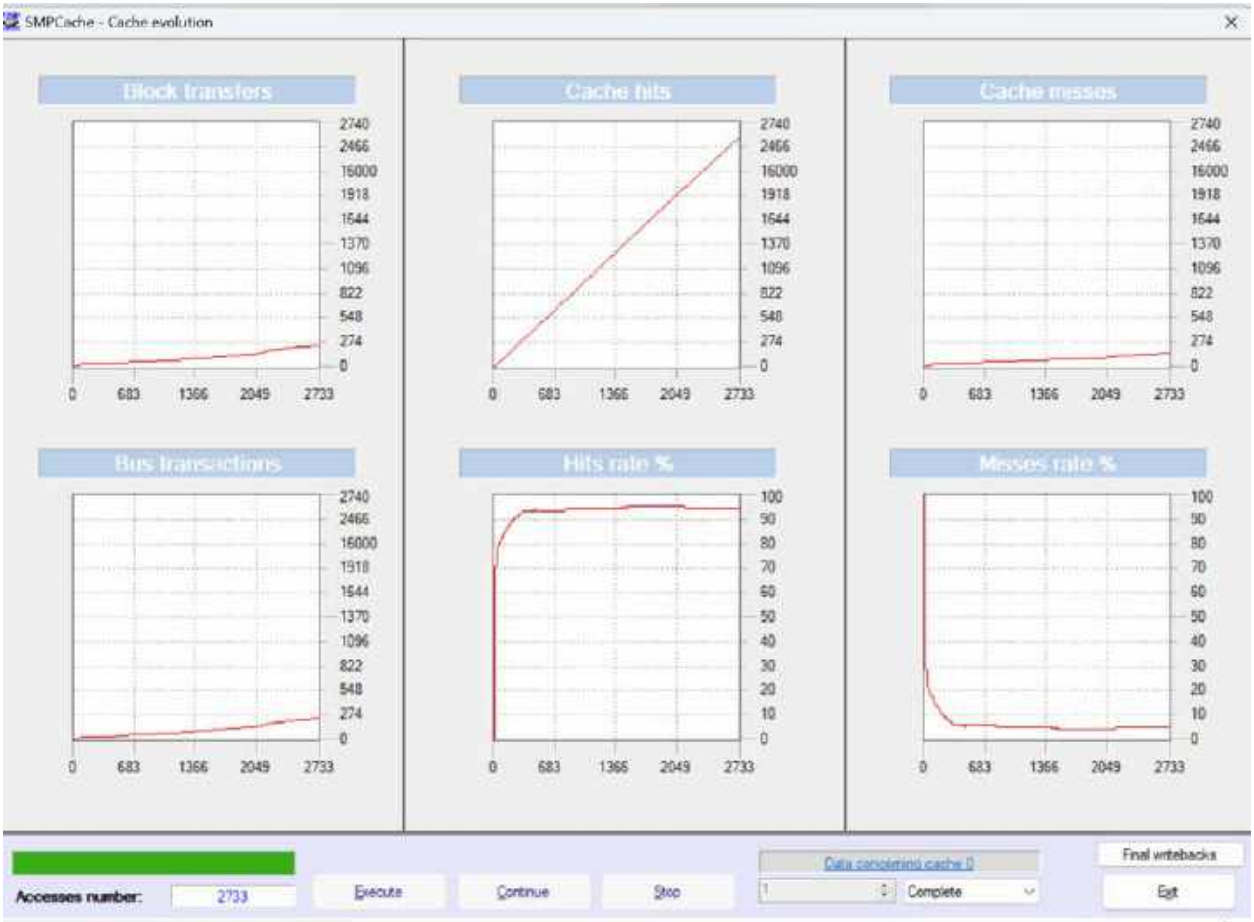

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit

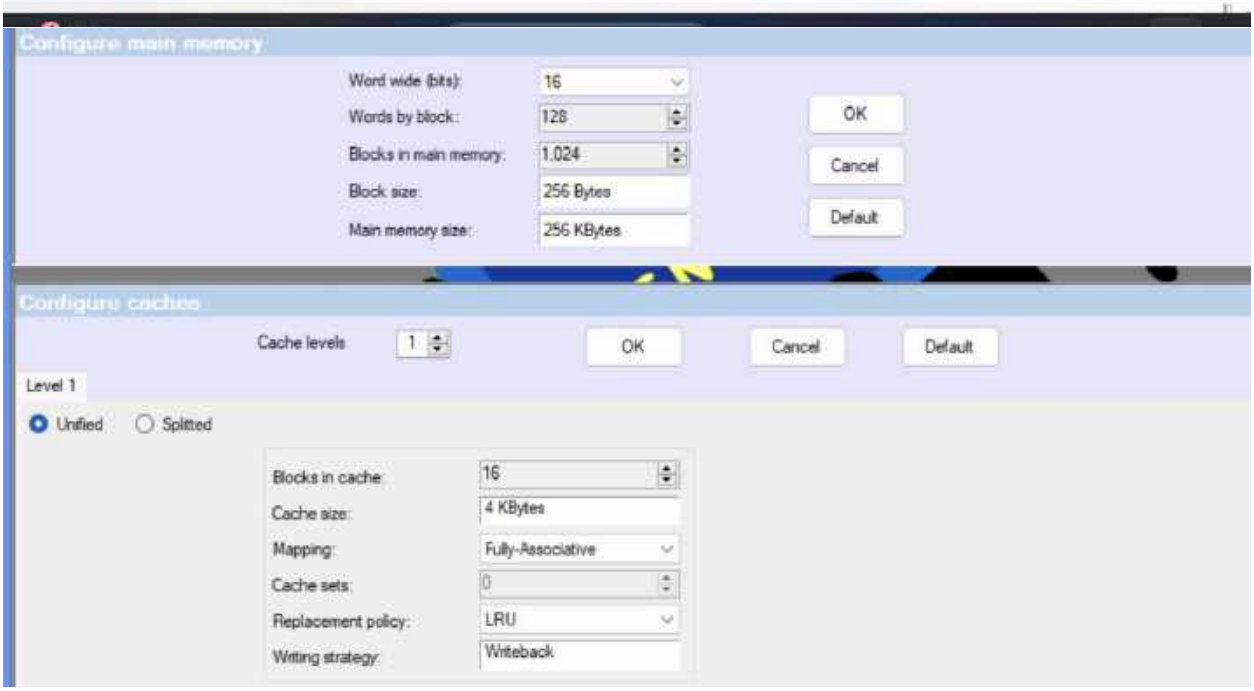
Configure main memory
Word wide (bits):
16
Words by block:
32
Blocks in main memory:
4,096
Block size:
64 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
64
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

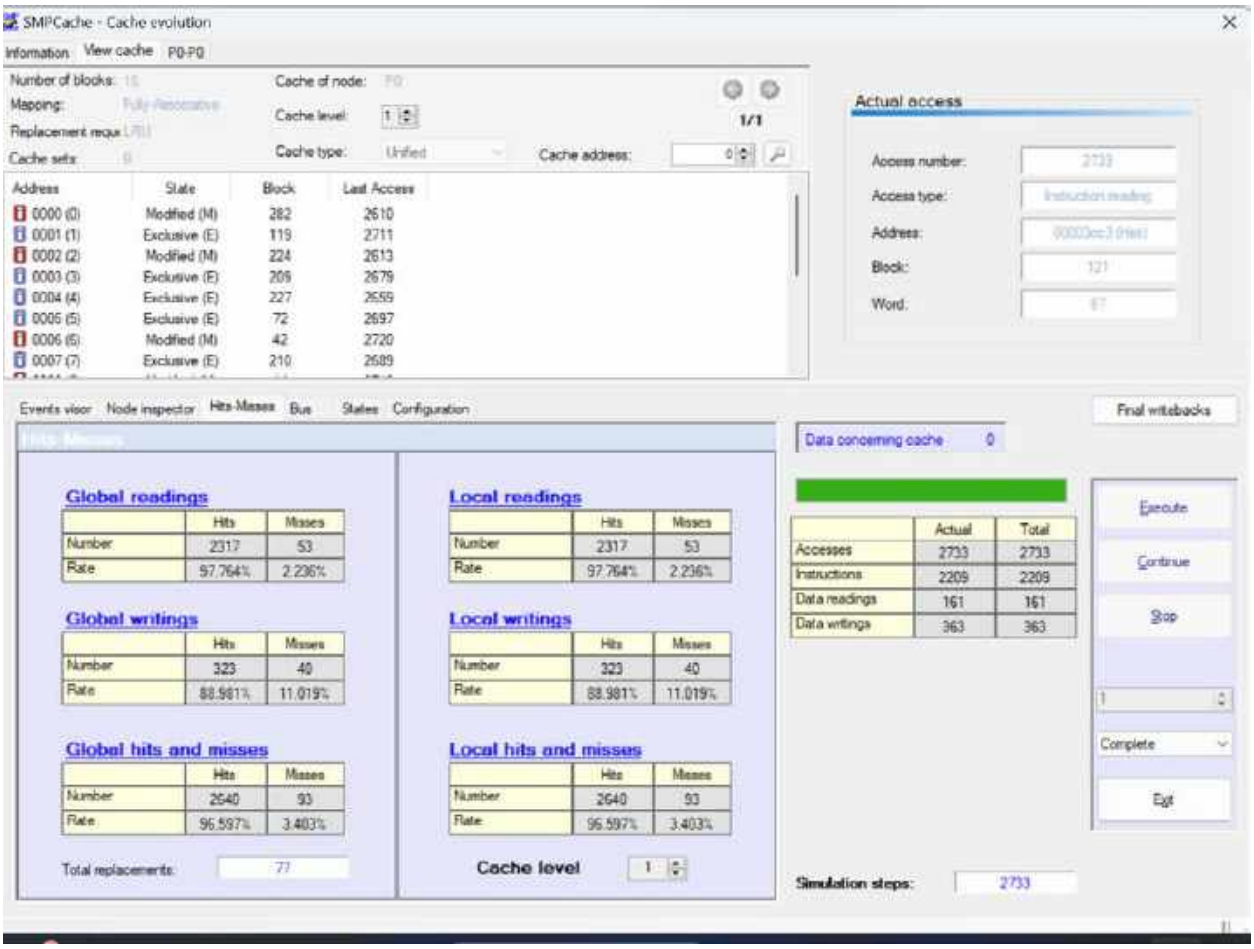

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 910 2657
0001 (1) Exclusive (E) 911 2659
0002 (2) Exclusive (E) 838 2669
0003 (3) Exclusive (E) 839 2679
0004 (4) Exclusive (E) 1534 2524
0005 (5) Modified (M) 1129 2610
0006 (6) Exclusive (E) 1134 2316
0007 (7) Modified (M) 896 2613
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number 2246 124
Rate 94.768% 5.232%
Global writings
Number 226 137
Rate 62.259% 37.741%
Global hits and misses
Number 2472 261
Rate 90.450% 9.550%
Total replacements: 197
Local readings
Number 2246 124
Rate 94.768% 5.232%
Local writings
Number 226 137
Rate 62.259% 37.741%
Local hits and misses
Number 2472 261
Rate 90.450% 9.550%
Cache level
1
Actual
Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps:
2733

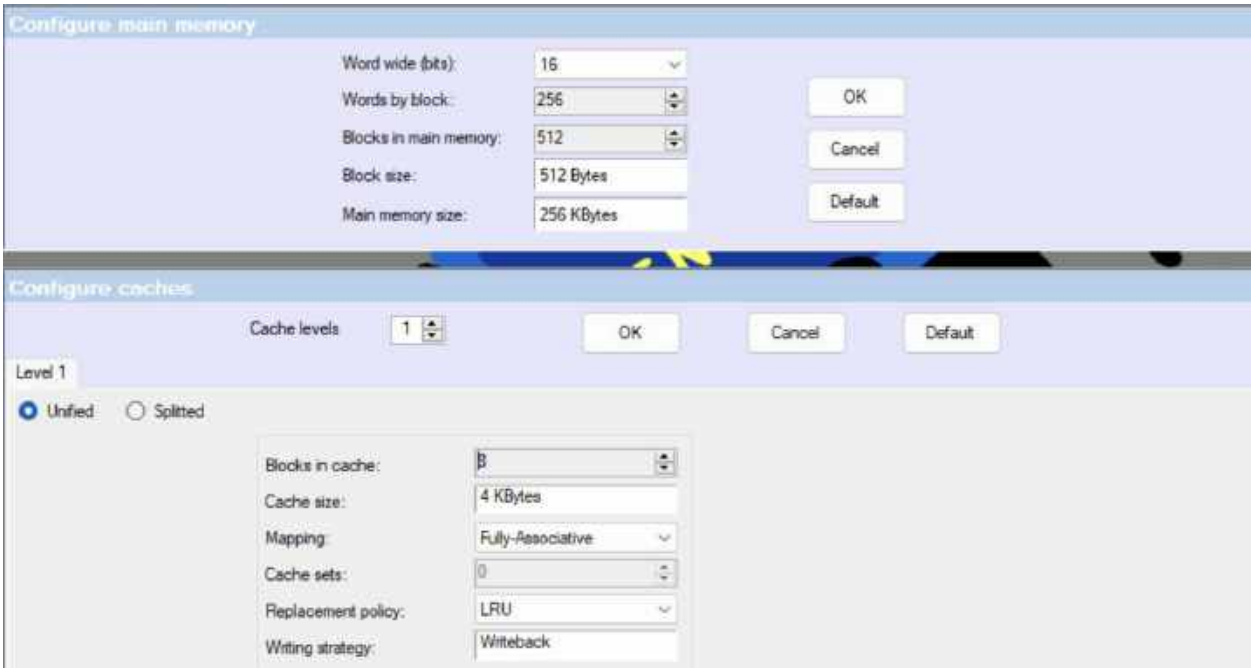

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
64
Blocks in main memory:
2.048
Block size:
128 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
32
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

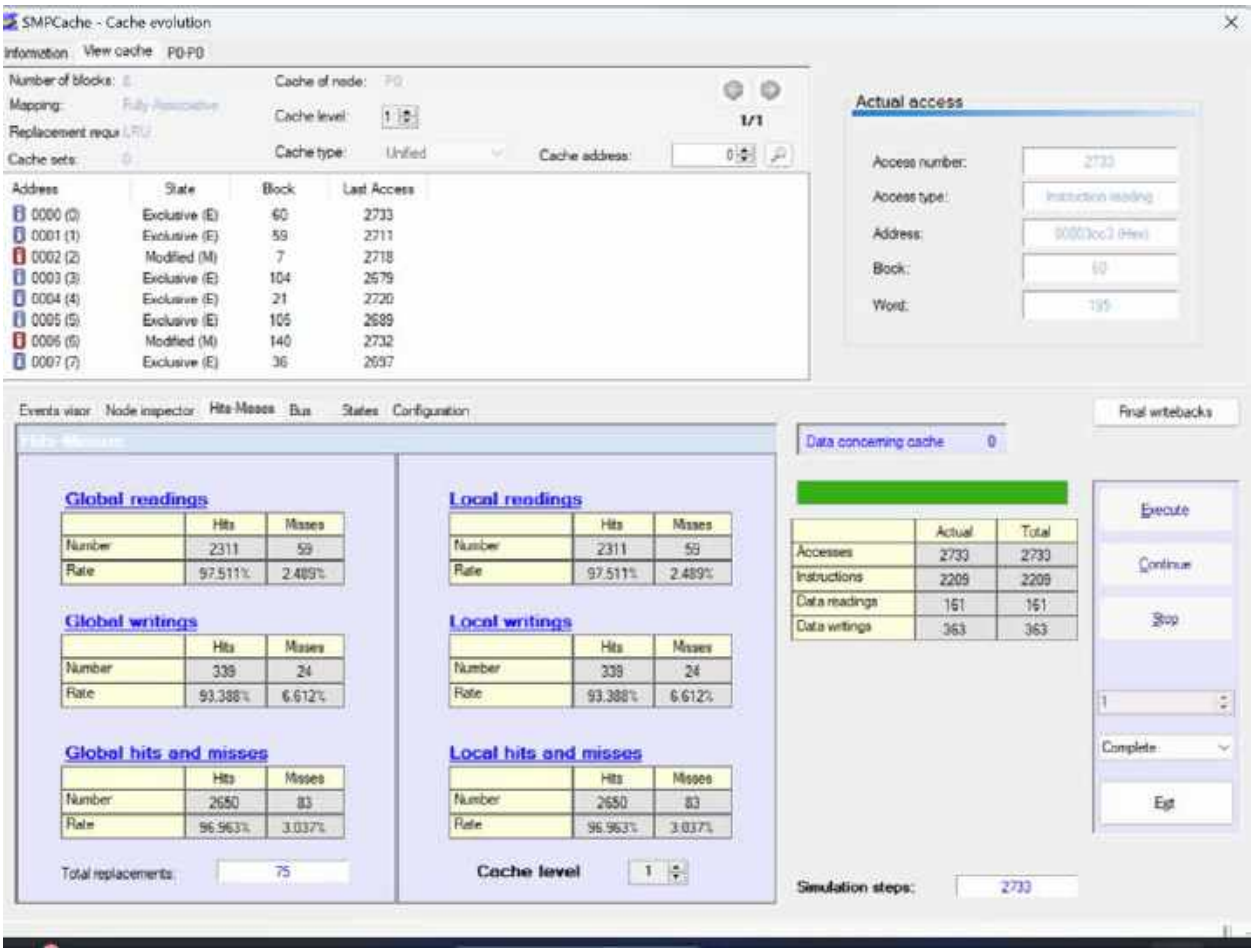

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 145 2697
0001 (1) Exclusive (E) 455 2659
0002 (2) Exclusive (E) 239 2711
0003 (3) Exclusive (E) 243 2733
0004 (4) Exclusive (E) 201 2456
0005 (5) Exclusive (E) 241 2725
0006 (6) Exclusive (E) 440 2460
0007 (7) Exclusive (E) 767 2524
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2290 80
Rate 96.624% 3.376%
Global writings
Hits Misses
Number 288 75
Rate 79.339% 20.661%
Global hits and misses
Hits Misses
Number 2578 155
Rate 94.329% 5.671%
Total replacements: 123
Local readings
Hits Misses
Number 2290 80
Rate 96.624% 3.376%
Local writings
Hits Misses
Number 288 75
Rate 79.339% 20.661%
Local hits and misses
Hits Misses
Number 2578 155
Rate 94.329% 5.671%
Cache level 1
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2733

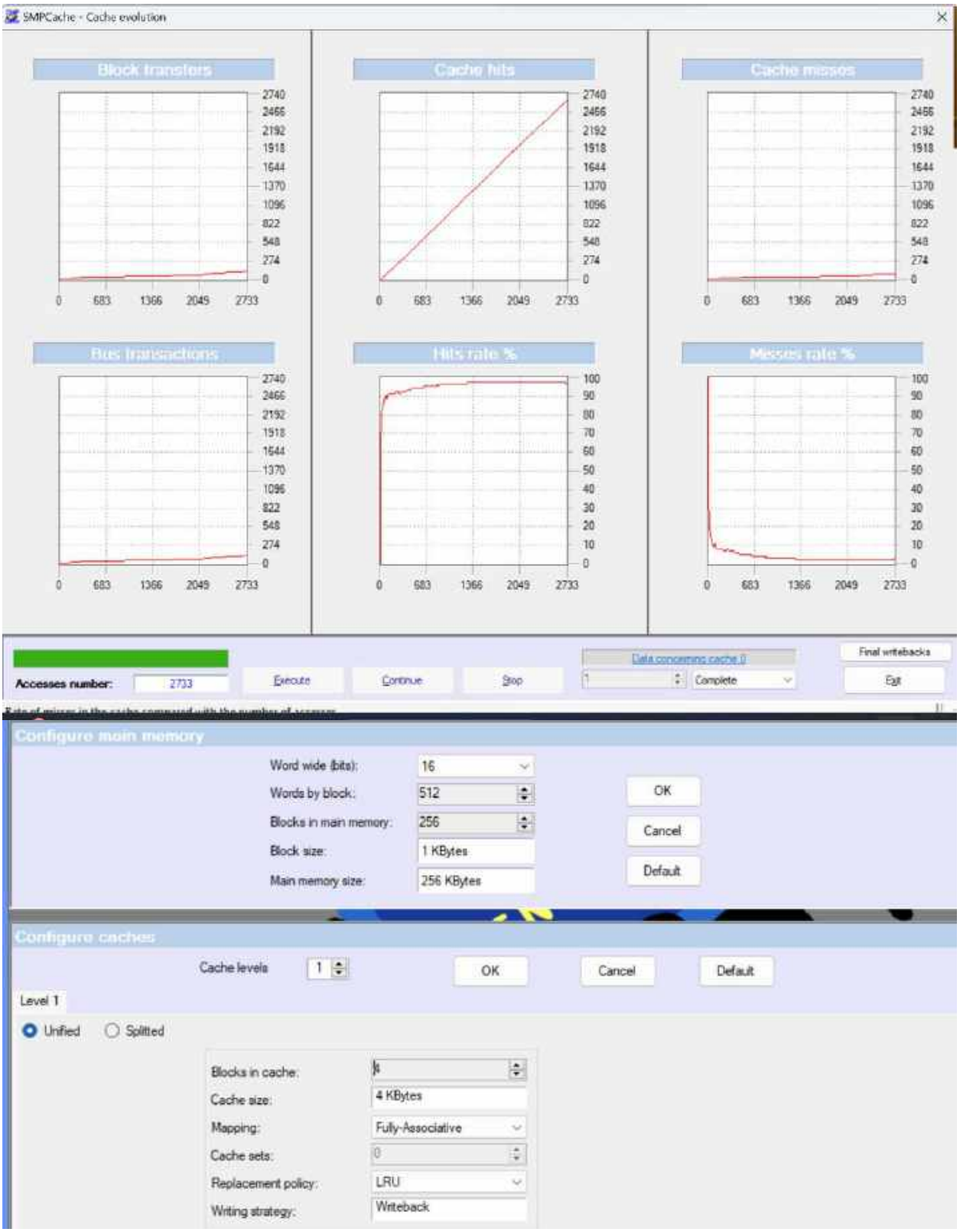

SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data consistent cache 0
Complete
Final writebacks
Exit

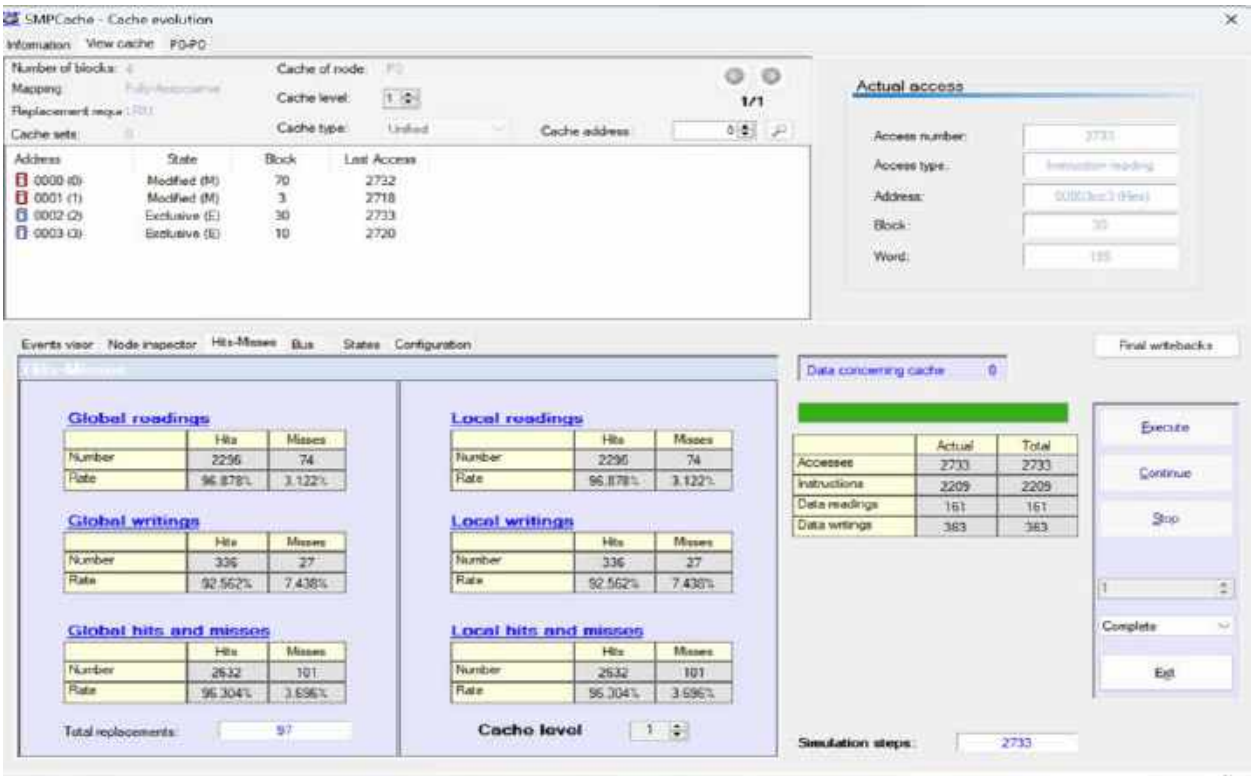

Configure main memory
Word wide (bits):
16
Words by block:
128
Blocks in main memory:
1.024
Block size:
256 Bytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
16
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback

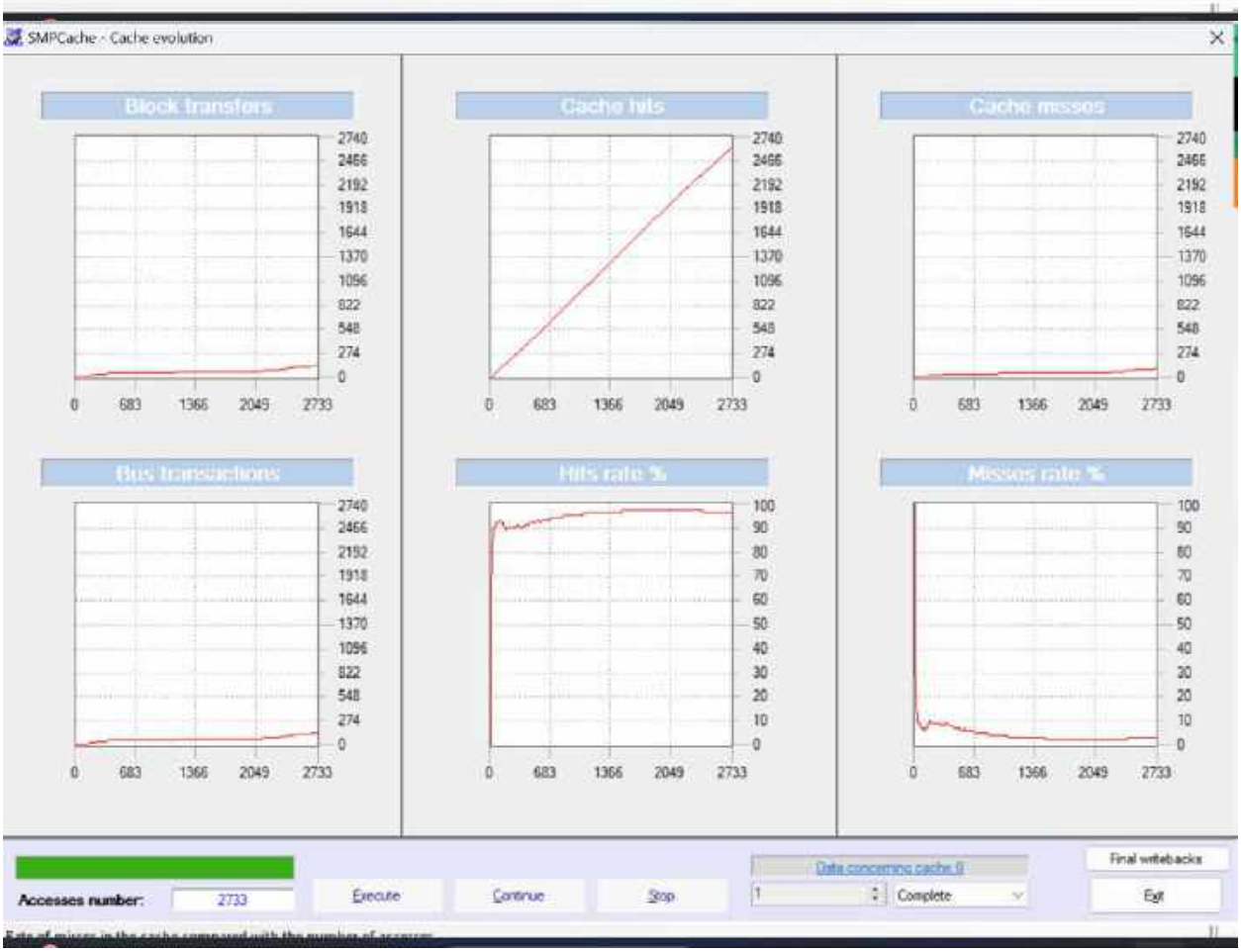

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Modified (M) 282 2610
0001 (1) Exclusive (E) 119 2711
0002 (2) Modified (M) 224 2613
0003 (3) Exclusive (E) 209 2679
0004 (4) Exclusive (E) 227 2559
0005 (5) Exclusive (E) 72 2697
0006 (6) Modified (M) 42 2720
0007 (7) Exclusive (E) 210 2689
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2317 53
Rate 97.764% 2.236%
Global writings
Hits Misses
Number 323 40
Rate 88.981% 11.019%
Global hits and misses
Hits Misses
Number 2640 93
Rate 96.597% 3.403%
Total replacements: 77
Local readings
Hits Misses
Number 2317 53
Rate 97.764% 2.236%
Local writings
Hits Misses
Number 323 40
Rate 88.981% 11.019%
Local hits and misses
Hits Misses
Number 2640 93
Rate 96.597% 3.403%
Cache level 1
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps: 2733

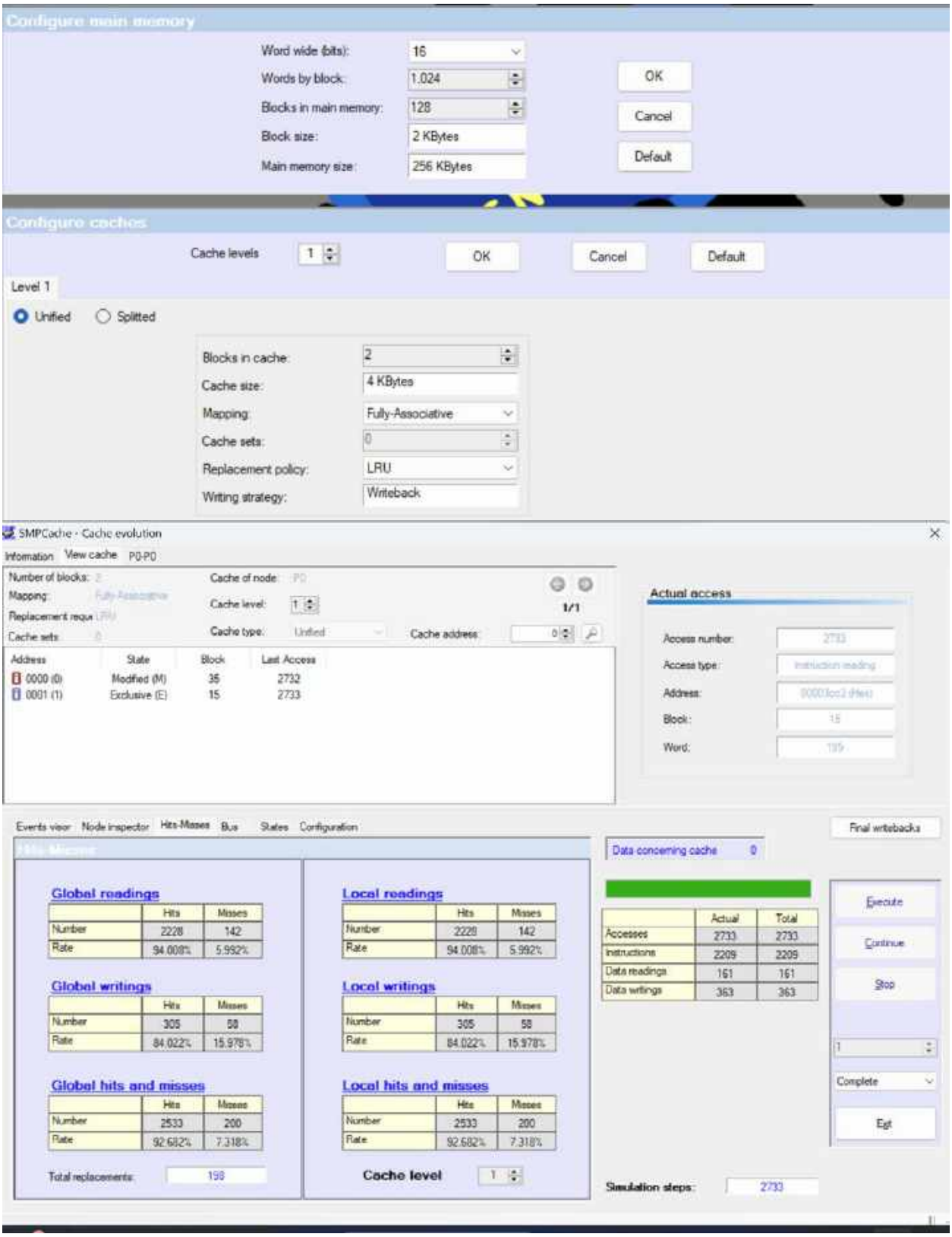

Configure main memory
Word wide (bits): 16
Words by block: 256
Blocks in main memory: 512
Block size: 512 Bytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 8
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback

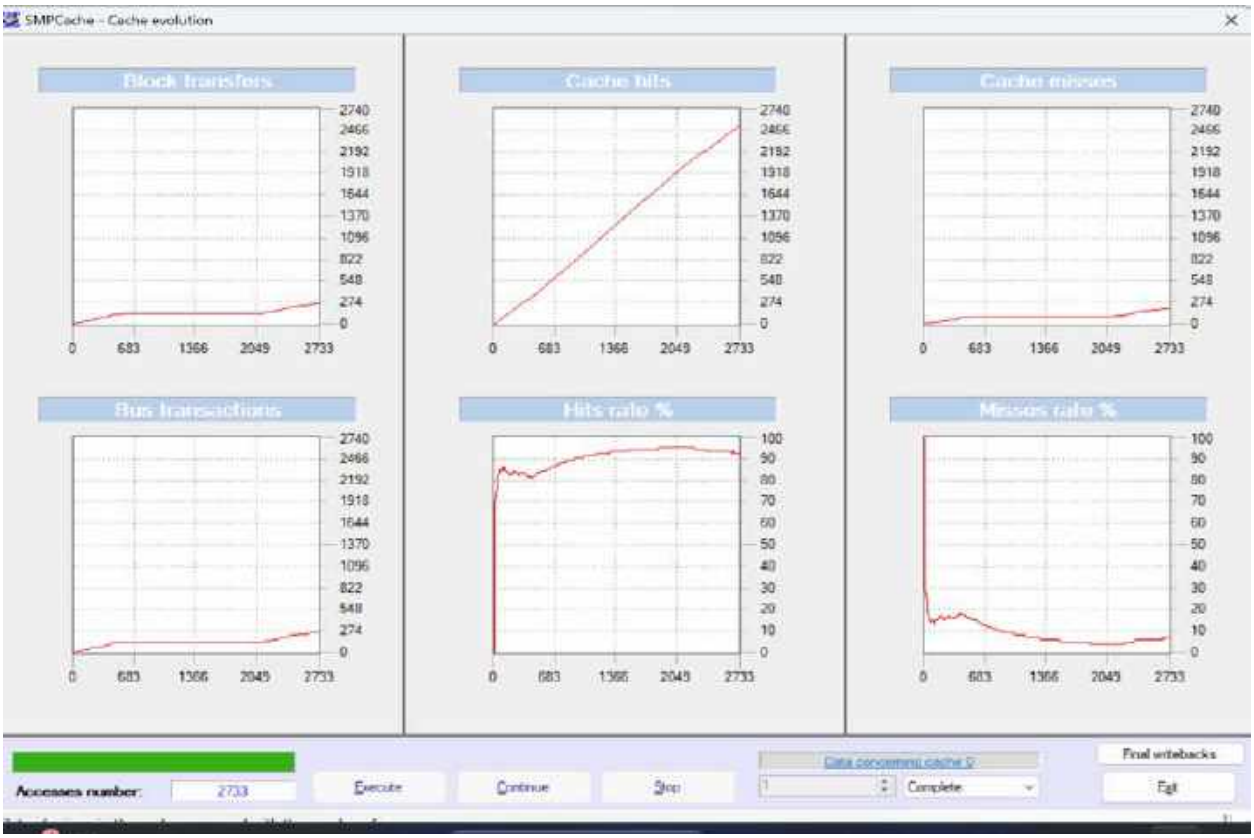

SMPCache - Cache evolution
Information
View cache
P0-P0
Number of blocks:
Mapping:
Replacement requ
Cache sets:
Cache of node:
Cache level:
Cache type:
Unified
Cache address:
1/1
Address
State
Block
Last Access
0000 (0) Exclusive (E) 60 2733
0001 (1) Exclusive (E) 59 2711
0002 (2) Modified (M) 7 2718
0003 (3) Exclusive (E) 104 2679
0004 (4) Exclusive (E) 21 2720
0005 (5) Exclusive (E) 105 2689
0006 (6) Modified (M) 140 2732
0007 (7) Exclusive (E) 36 2697
Actual access
Access number:
Access type:
Address:
Block:
Word:
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Data concerning cache
0
Global readings
Hits
Misses
Number 2311 59
Rate 97.511% 2.489%
Global writings
Number 339 24
Rate 93.388% 6.612%
Global hits and misses
Number 2650 83
Rate 96.963% 3.037%
Total replacements:
75
Local readings
Number 2311 59
Rate 97.511% 2.489%
Local writings
Number 339 24
Rate 93.388% 6.612%
Local hits and misses
Number 2650 83
Rate 96.963% 3.037%
Cache level
1
Actual
Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
Complete
Exit
Simulation steps:
2733


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2733
Execute
Continue
Stop
Data concerning cache 0
Complete
Final writebacks
Exit
Configure main memory
Word wide (bits):
16
Words by block:
512
Blocks in main memory:
256
Block size:
1 KBytes
Main memory size:
256 KBytes
OK
Cancel
Default
Configure caches
Cache levels
1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache:
8
Cache size:
4 KBytes
Mapping:
Fully-Associative
Cache sets:
0
Replacement policy:
LRU
Writing strategy:
Writeback


SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 4
Mapping
Replacement repla
Cache sets
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 70 2732
0001 (1) Modified (M) 3 2718
0002 (2) Exclusive (E) 30 2733
0003 (3) Exclusive (E) 10 2720
Actual access
Access number: 2733
Access type: Instruction reading
Address: 0000ec3 (Hex)
Block: 30
Word: 195
Events visor Node inspector Hits-Misses Bus States Configuration
Final writebacks
Data concerning cache 0
Global readings
Hits Misses
Number 2296 74
Rate 96.878% 3.122%
Global writings
Hits Misses
Number 336 27
Rate 92.562% 7.438%
Global hits and misses
Hits Misses
Number 2632 101
Rate 96.304% 3.696%
Total replacements: 97
Local readings
Hits Misses
Number 2296 74
Rate 96.878% 3.122%
Local writings
Hits Misses
Number 336 27
Rate 92.562% 7.438%
Local hits and misses
Hits Misses
Number 2632 101
Rate 96.304% 3.696%
Cache level 1
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2733


SMPCache - Cache evolution
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
0 683 1366 2049 2733
0 274 548 822 1096 1370 1644 1918 2192 2466 2740
0 10 20 30 40 50 60 70 80 90 100
Accesses number: 2733
Execute
Continue
Stop
Data concerning cache 0
1
Complete
Final writebacks
Exit


Configure main memory
Word wide (bits): 16
Words by block: 1.024
Blocks in main memory: 128
Block size: 2 KBytes
Main memory size: 256 KBytes
OK
Cancel
Default
Configure caches
Cache levels 1
OK
Cancel
Default
Level 1
Unified
Splitted
Blocks in cache: 2
Cache size: 4 KBytes
Mapping: Fully-Associative
Cache sets: 0
Replacement policy: LRU
Writing strategy: Writeback
SMPCache - Cache evolution
Information View cache P0-P0
Number of blocks: 2
Mapping: Fully-Associative
Replacement requ.: FIFO
Cache sets: 0
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address State Block Last Access
0000 (0) Modified (M) 35 2732
0001 (1) Exclusive (E) 15 2733
Actual access
Access number: 2733
Access type: Instruction reading
Address: 0000fcc2 (hex)
Block: 15
Word: 199
Events viewer Node inspector Hits-Misses Bus States Configuration
Final writebacks
Hits-Misses
Global readings
Hits Misses
Number 2228 142
Rate 94.008% 5.992%
Global writings
Hits Misses
Number 305 58
Rate 84.022% 15.978%
Global hits and misses
Hits Misses
Number 2533 200
Rate 92.682% 7.318%
Total replacements: 198
Local readings
Hits Misses
Number 2228 142
Rate 94.008% 5.992%
Local writings
Hits Misses
Number 305 58
Rate 84.022% 15.978%
Local hits and misses
Hits Misses
Number 2533 200
Rate 92.682% 7.318%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 2733 2733
Instructions 2209 2209
Data readings 161 161
Data writings 363 363
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 2733



QUESTIONS

Q. Does the miss rate increase or decrease as the block size increases? Why? Does this increment or decrement happen for all the benchmarks or does it depend on the different locality grades? What does it happen with the compulsory misses when you enlarge the block size? What is the pollution point? Does it appear in these experiments?

A. The miss rate decreases as the block size increases. This is because there are more block sizes available to take advantage of spatial locality. This will lead to the decrease in miss rate.

Decrement takes place for all the benchmarks. Decrement also depends on the different locality grades. This is because all the data that we observed such as amounts of instructions, hit rate, miss rate and block size are different.

When the block size is enlarged, the compulsory misses remains unchanged. This is because the increase in block size will only cause more adjacent words to be fetched on each miss.

When the block size is too big compared to cache size, the point where this conditions occurs is known as a pollution point. A bigger block size causes a higher miss penalty and the system will take a longer time to load a new block to the next level. Yes, the pollution point appears in this experiment.

Q.In conclusion, does the increase of block size improve the system performance?

A. The increase of block size will improve the system performance. As the block size increases the miss rate decreases. The system performance can be improved by reducing the miss rate.

Task 4

Influence of the Block Size for Different Cache Sizes

Purpose

Show the influence of the block size on the miss rate, but in this case, for several cache sizes.

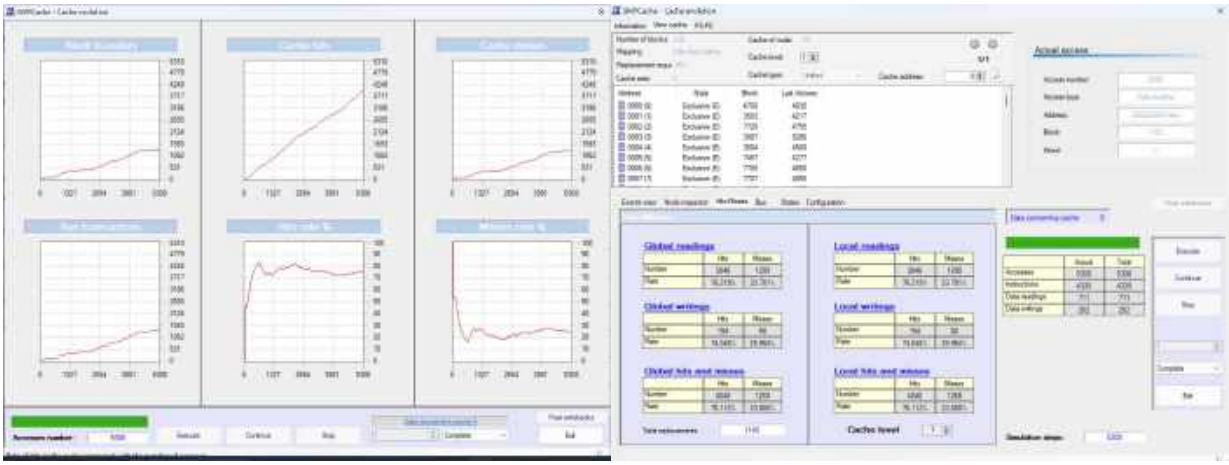
Configuration

Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 32.
Main memory size = 1024 KB (the number of blocks in main memory will vary).
Mapping = Fully-Associative.
Replacement policy = LRU.

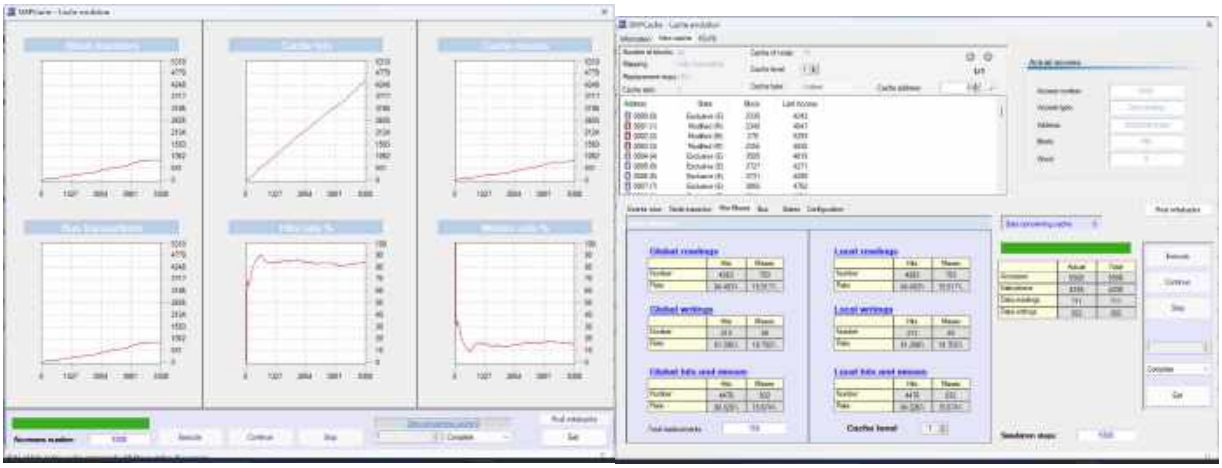
Experiment

Configure the words by block using the following configurations: 8 (block size = 32 bytes), 16, 32, 64, 128, 256, 512, and 1024 (block size = 4096 bytes). For each of the configurations of words by block, configure the number of blocks in cache in order to get the following cache sizes: 4 KB, 8 KB, 16 KB, and 32 KB. For each configuration obtain the miss rate using the memory trace: Ear.

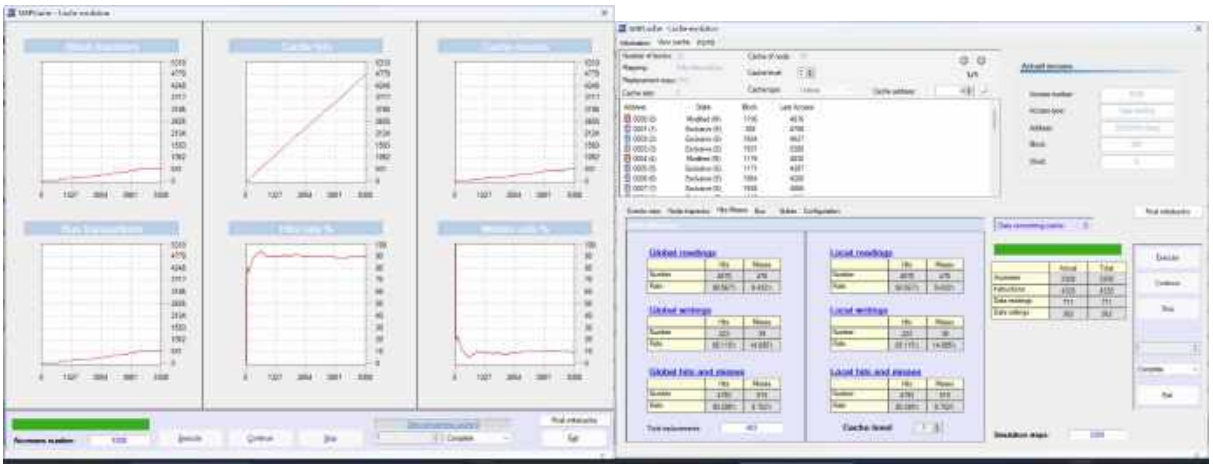
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
1 (4 KB)	8	32768	32	128



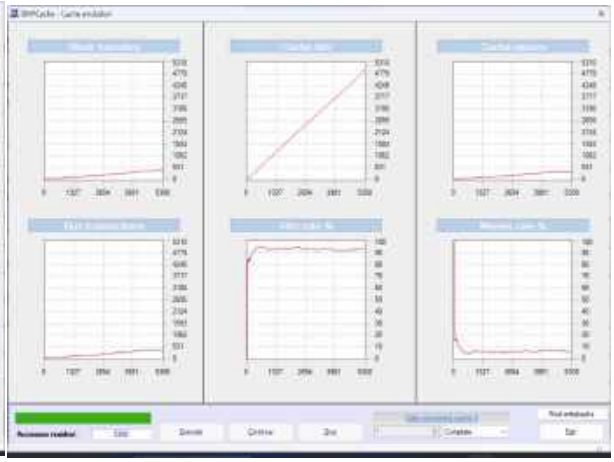
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
2 (4 KB)	16	16384	64	64



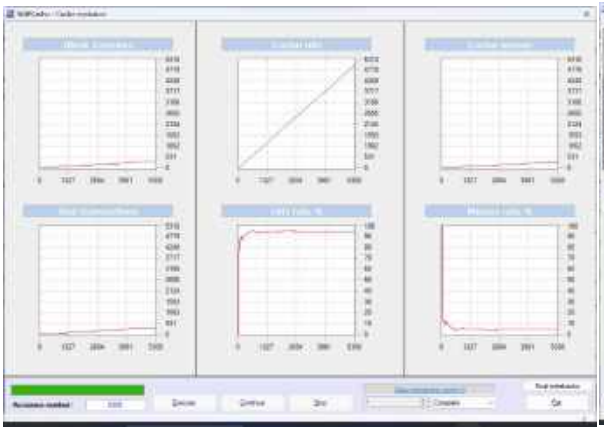
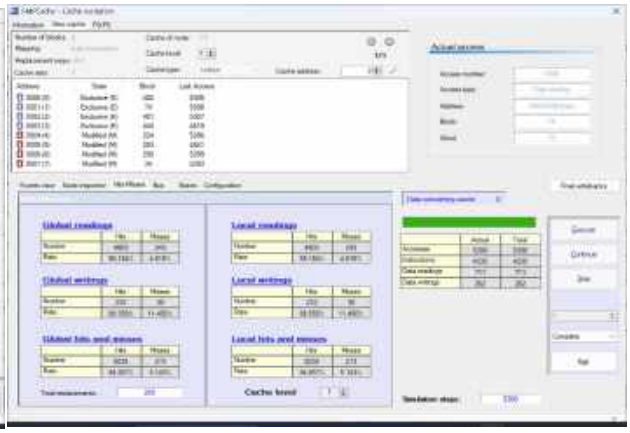
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
3 (4 KB)	32	8192	128	32



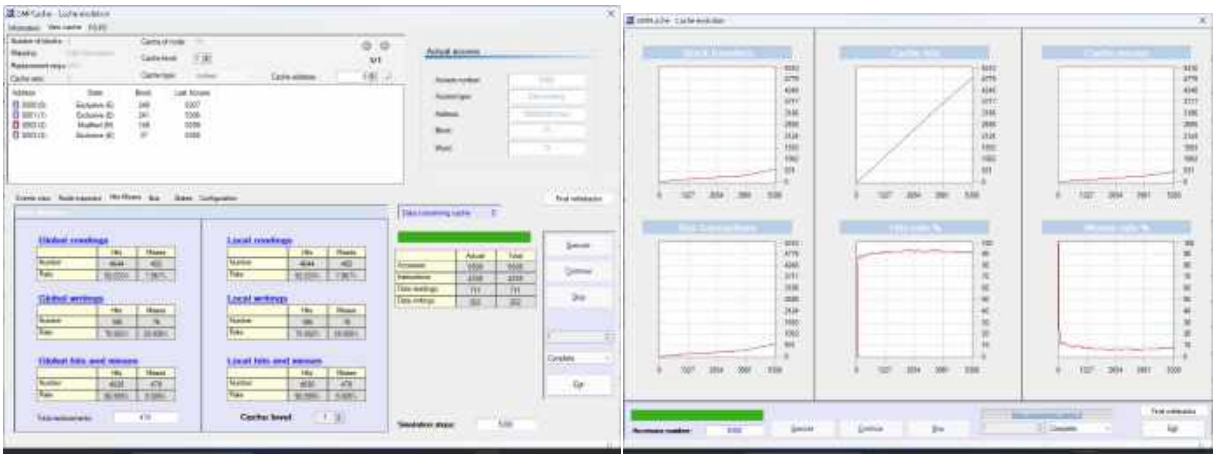
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
4 (4 KB)	64	4096	256	16



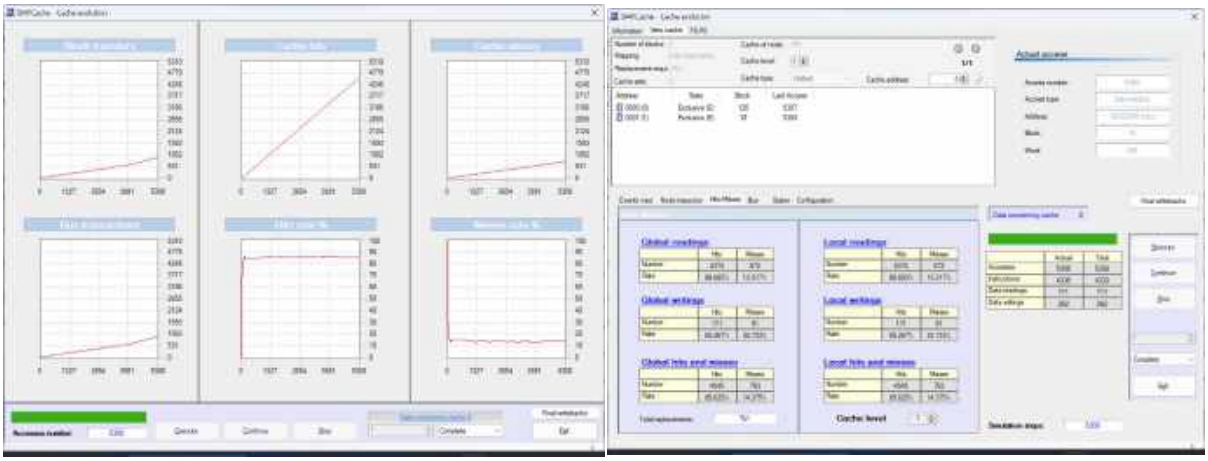
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
5 (4 KB)	128	2048	512	8

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
6 (4 KB)	256	1024	1024	4

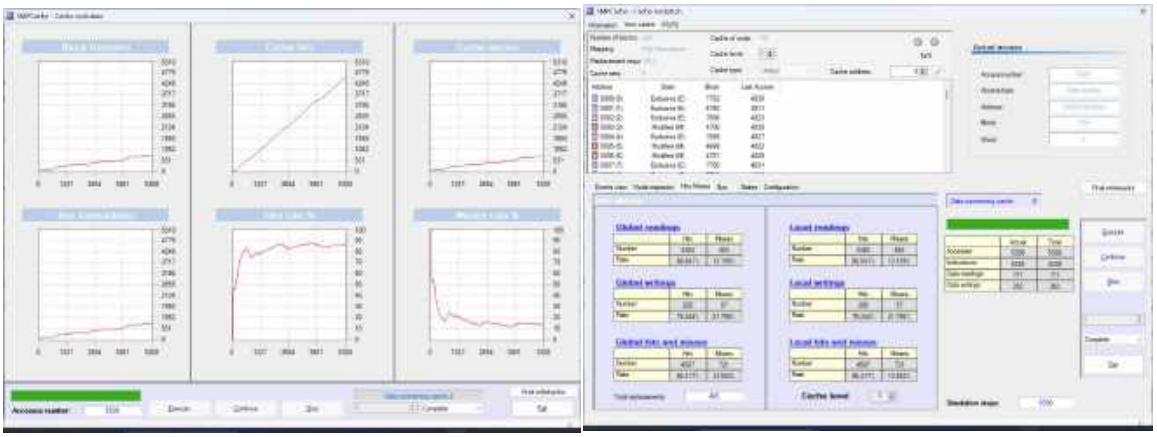


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
7 (4 KB)	512	512	2048	2

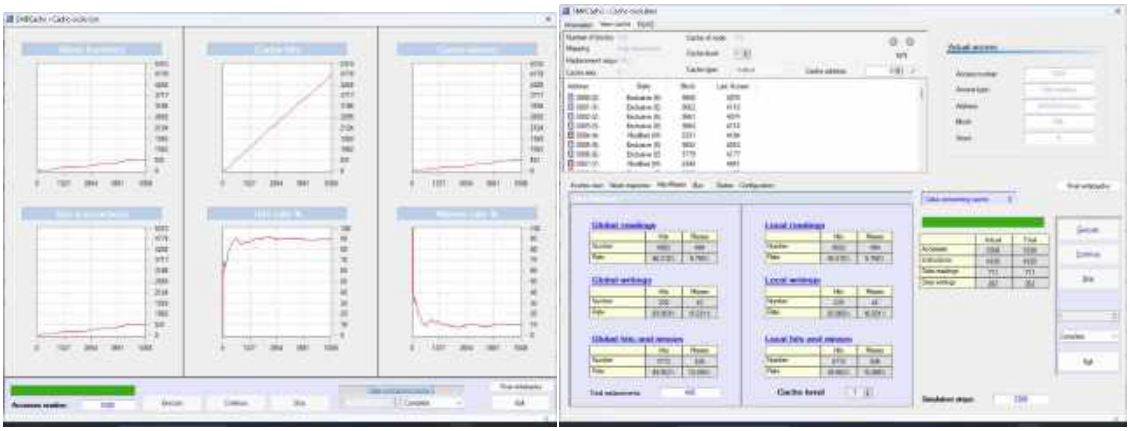


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
8 (4 KB)	1024	256	4096	1

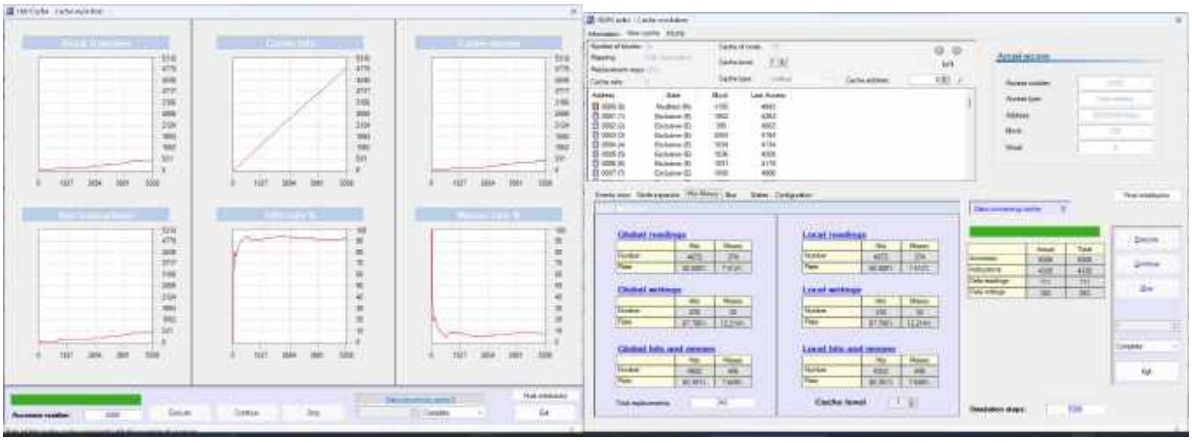
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
1 (8 KB)	8	32768	32	256



Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
2 (8 KB)	16	16384	64	128

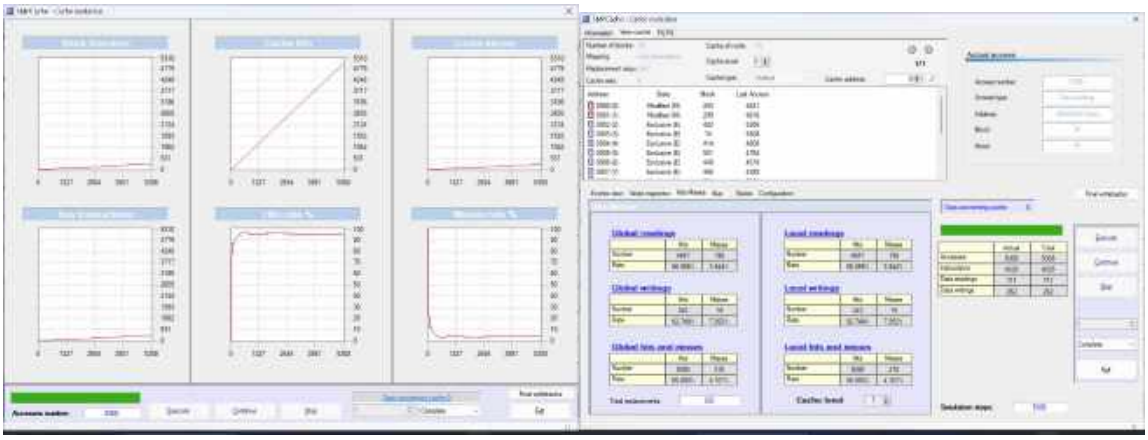


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
3 (8 KB)	32	8192	128	64



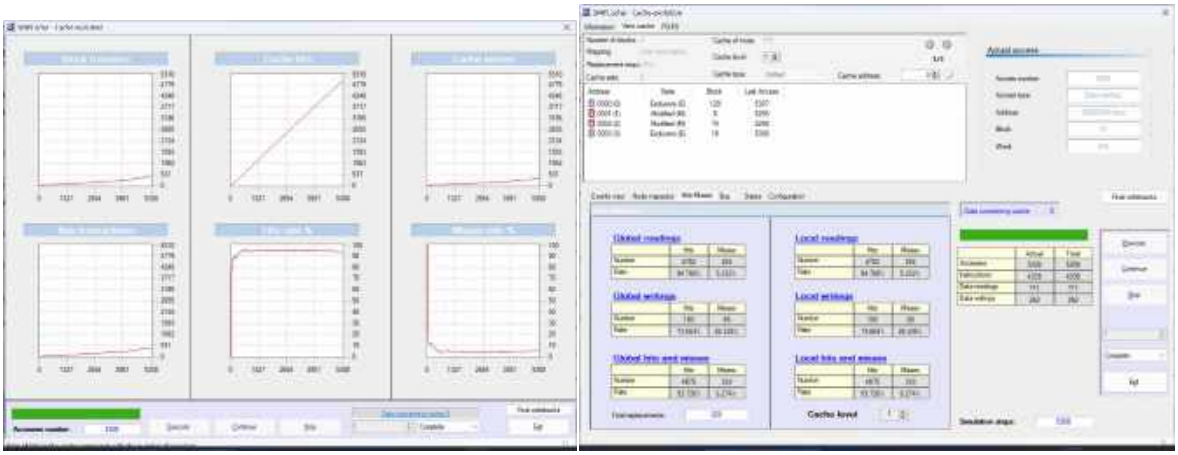
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
4 (8 KB)	64	4096	256	32

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
5 (8 KB)	128	2048	512	16



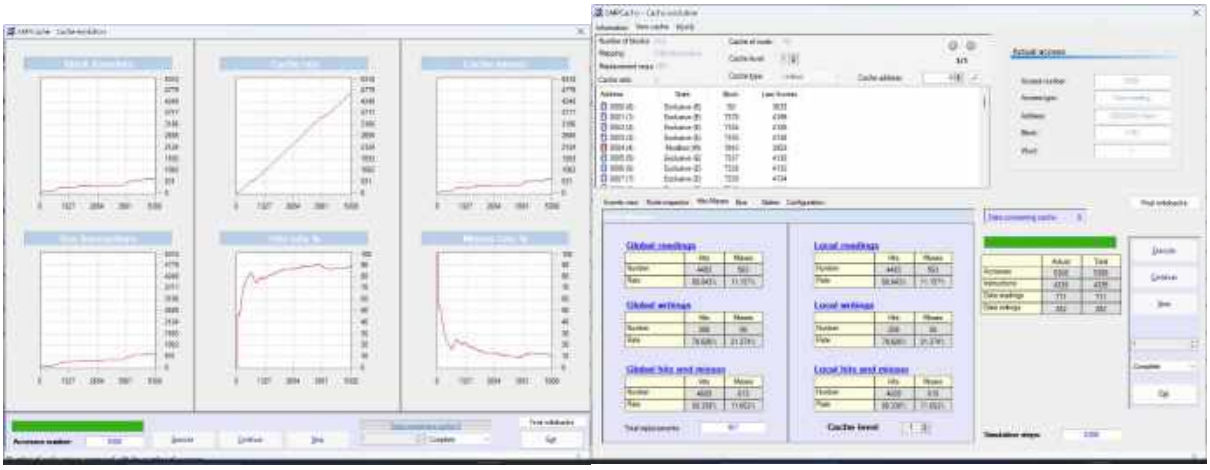
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
6 (8 KB)	256	1024	1024	8

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
7 (8 KB)	512	512	2048	4



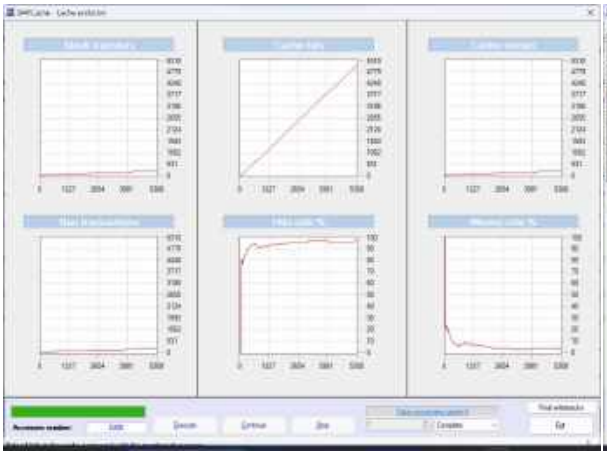
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
8 (8 KB)	1024	256	4096	2

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
1 (16 KB)	8	32768	32	512

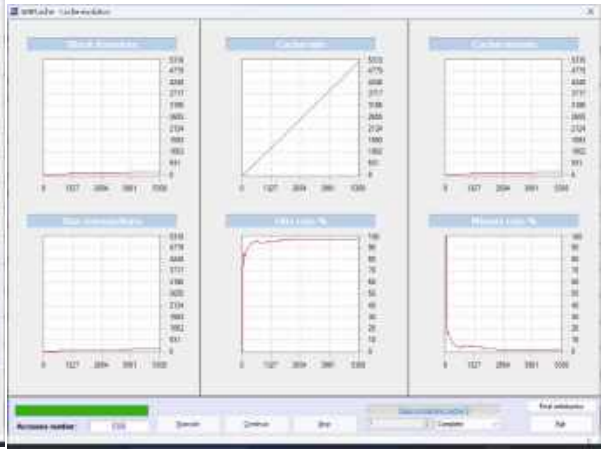


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
2 (16 KB)	16	16384	64	256

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
3 (16 KB)	32	8192	128	128

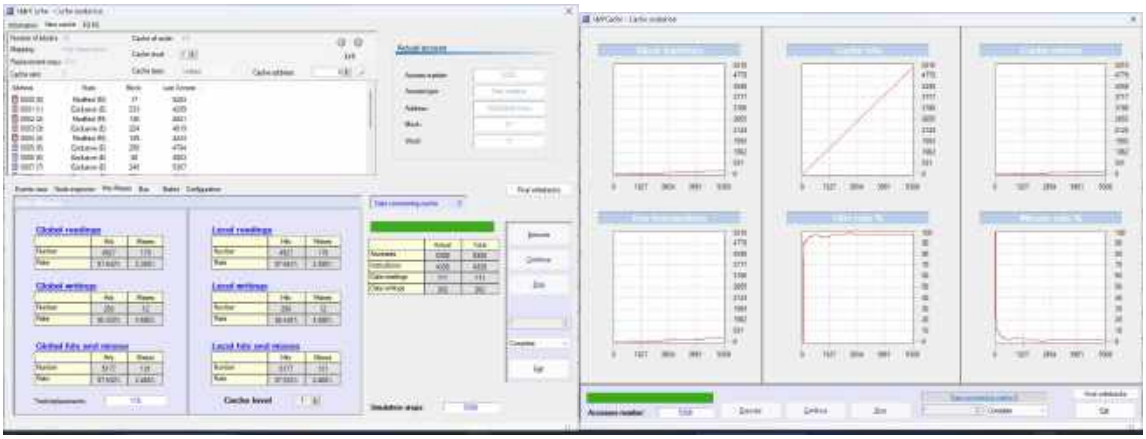


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
4 (16 KB)	64	4096	256	64

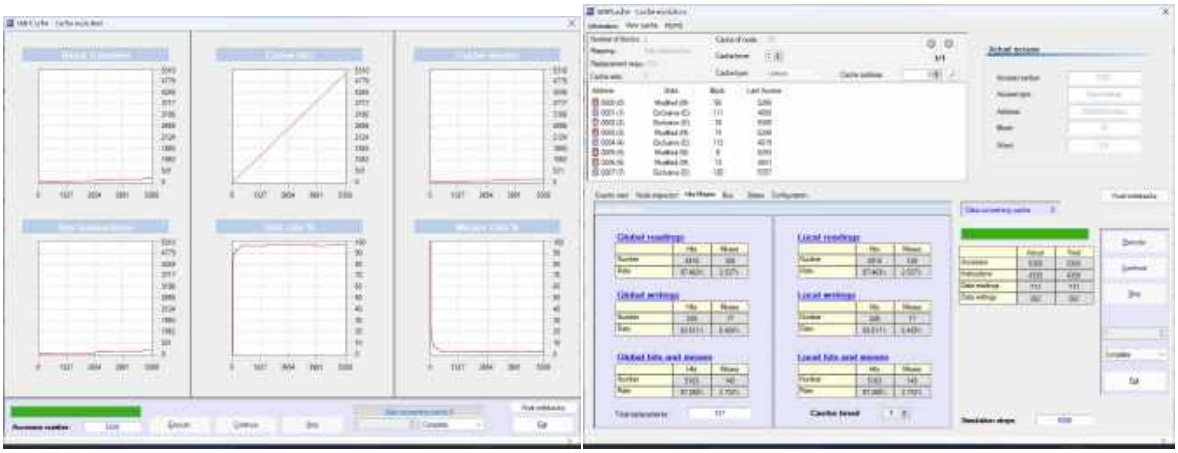


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
5 (16 KB)	128	2048	512	32

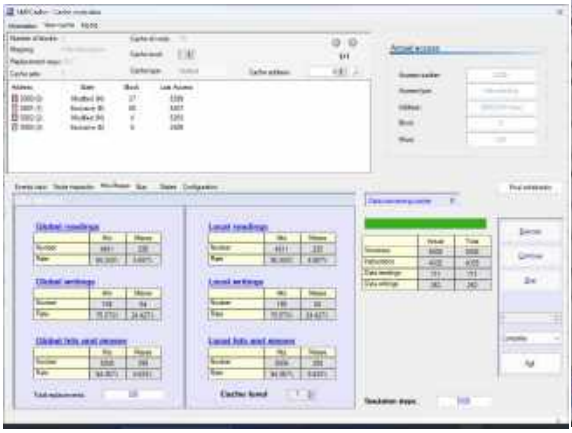
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
6 (16 KB)	256	1024	1024	16

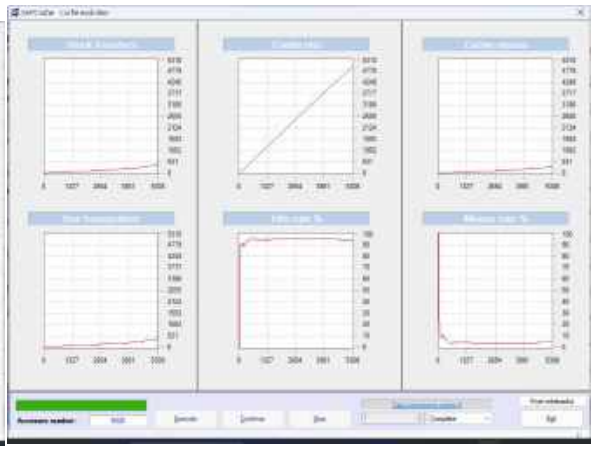


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
7 (16 KB)	512	512	2048	8

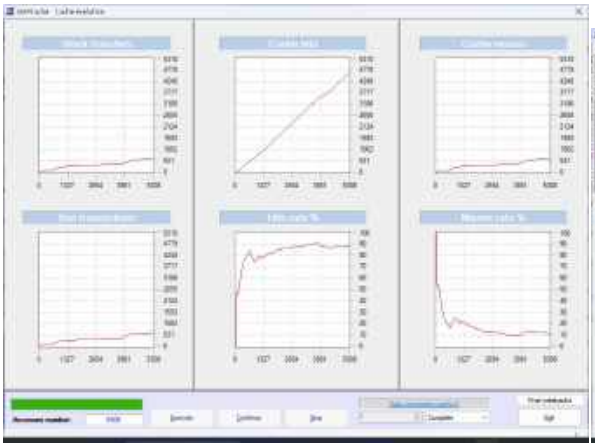


Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
8 (16 KB)	1024	256	4096	4





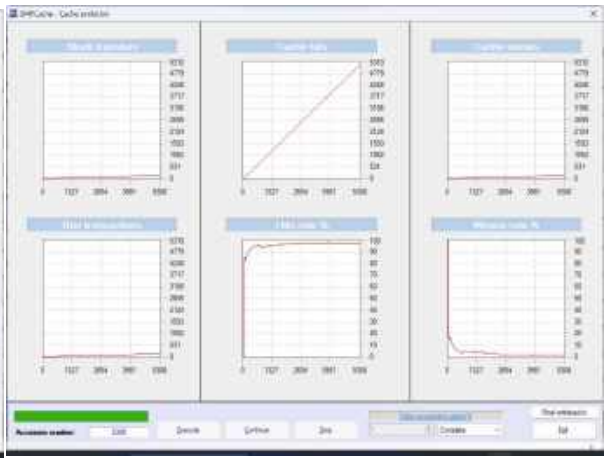
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
1 (32 KB)	8	32768	32	1024



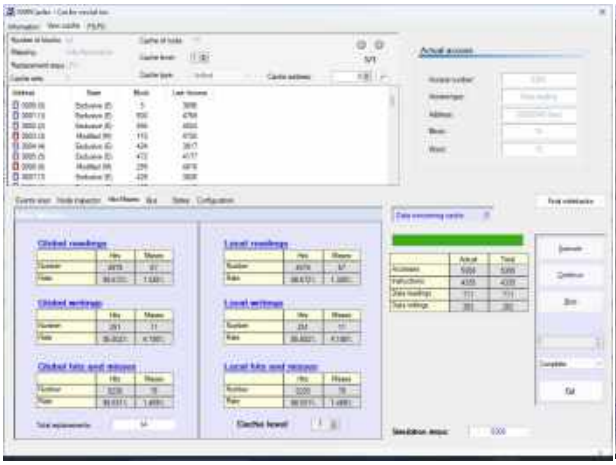
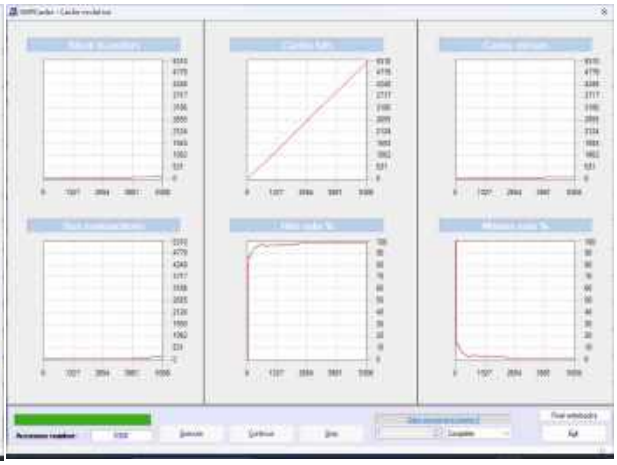
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
2 (32 KB)	16	16384	64	512

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
3 (32 KB)	32	8192	128	256

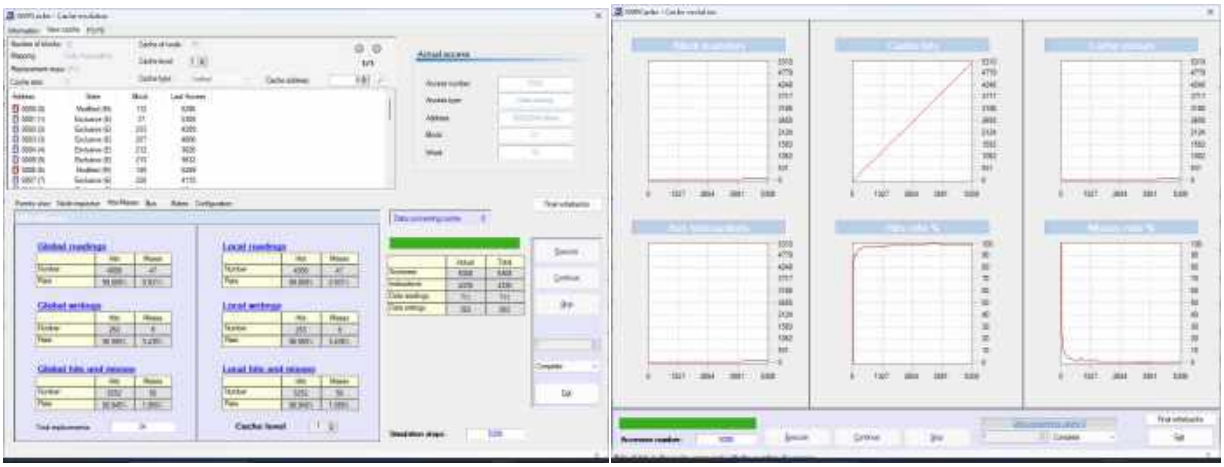
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
4 (32 KB)	64	4096	256	128



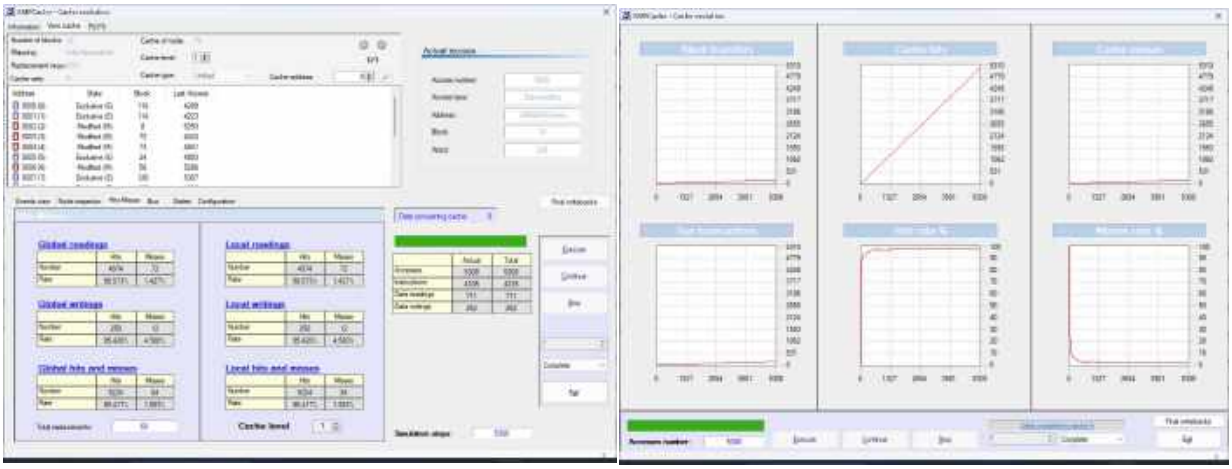
Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
5 (32 KB)	128	2048	512	64

Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
6 (32 KB)	256	1024	1024	32



Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
7 (32 KB)	512	512	2048	16



Configuration	Word by blocks	Blocks in memory	Block Size	Blocks in Cache
8 (32 KB)	1024	256	4096	8

Questions

Does the miss rate increase or decrease as the block size increases? Why?
As the size of blocks increases, there is an evident decrease in miss rates across various cache capacities, such as 4 KB, 8 KB, 16 KB, and 32 KB. The experimental graphs clearly depict that smaller block sizes result in occasional spikes in miss rates, ultimately leading to an overall higher miss rate compared to larger block sizes.

This decrease in miss rate remains consistent across all cache configurations in the EAR benchmark, regardless of the level of data locality. The graphical representations demonstrate a gradual decline in miss rates across all cache sizes for Configuration 1, Configuration 2, and Configuration 3. However, starting from Configuration 4, the miss rate experiences a sharp decline.The reduction in miss rates with larger block sizes is attributed to spatial locality. When more words are accommodated within a single block, the likelihood of finding the next reference within the same block significantly increases.

What does it happen with the compulsory misses when you enlarge the block size?
Increasing the block size allows for accommodating a greater number of words per block, consequently reducing the overall count of cache lines. This, in turn, leads to a notable decrease in compulsory misses. With larger block sizes, the initial data elements needed by the processor are often already present in the cache after a few misses. Conversely, smaller block sizes necessitate retrieving blocks more frequently, resulting in an increase in compulsory misses.

Does the pollution point appear in these experiments? Does the influence of the pollution point increase or decrease as the cache size increases? Why?
The problem of pollution becomes apparent in these experiments. As the block size increases, so does the number of words per block, potentially leading to the inclusion of unnecessary data within the blocks. If the requested data isn't found in the current block, the resulting miss penalty is higher. However, enlarging the cache size enables more blocks of a larger size to be accommodated, improving the likelihood of the requested data elements being present in the cache.

The graphs clearly demonstrate that as the cache size increases for a given block size, the occurrence of spikes diminishes. Additionally, the miss rate graph stabilizes beyond a certain point, showcasing an overall lower miss

rate. Thus, despite the larger block size presenting the drawback of an increased pollution point, expanding the cache size proves advantageous in alleviating this concern.

Task 5

Influence of the Mapping for Different Cache Sizes

Purpose

Analyze the influence of the mapping on the miss rate for several cache sizes.

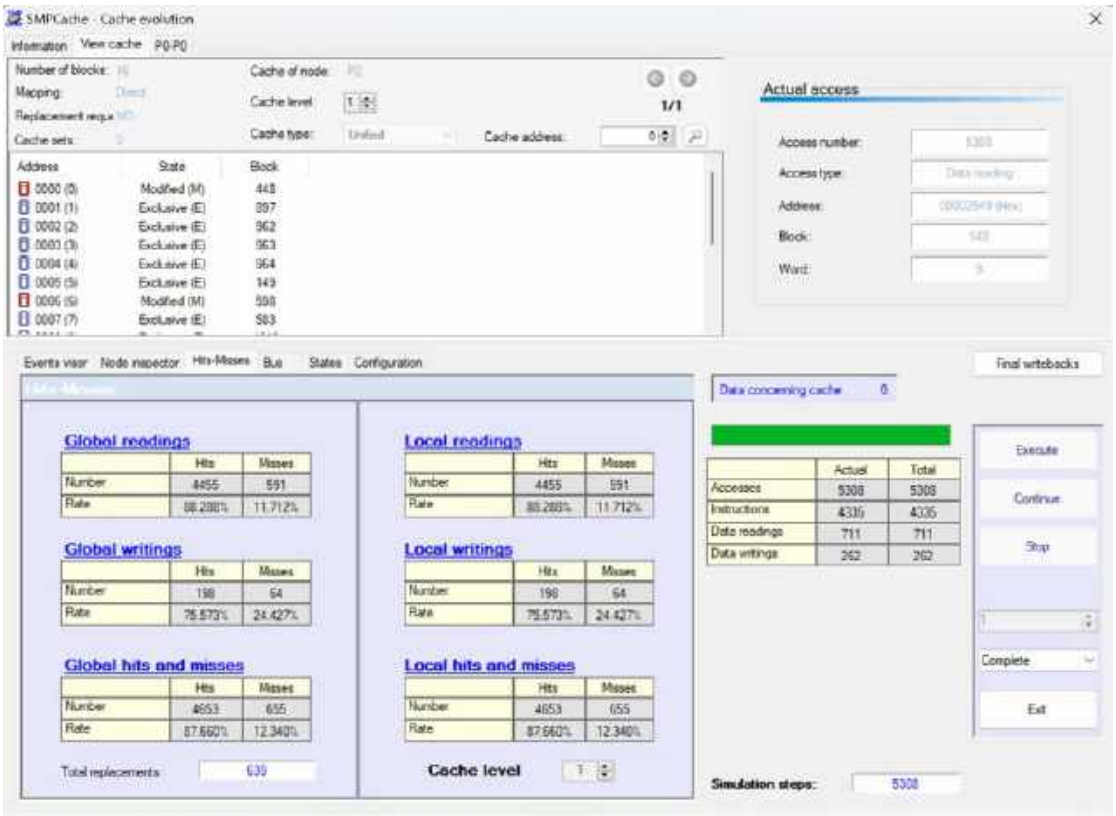
Configuration

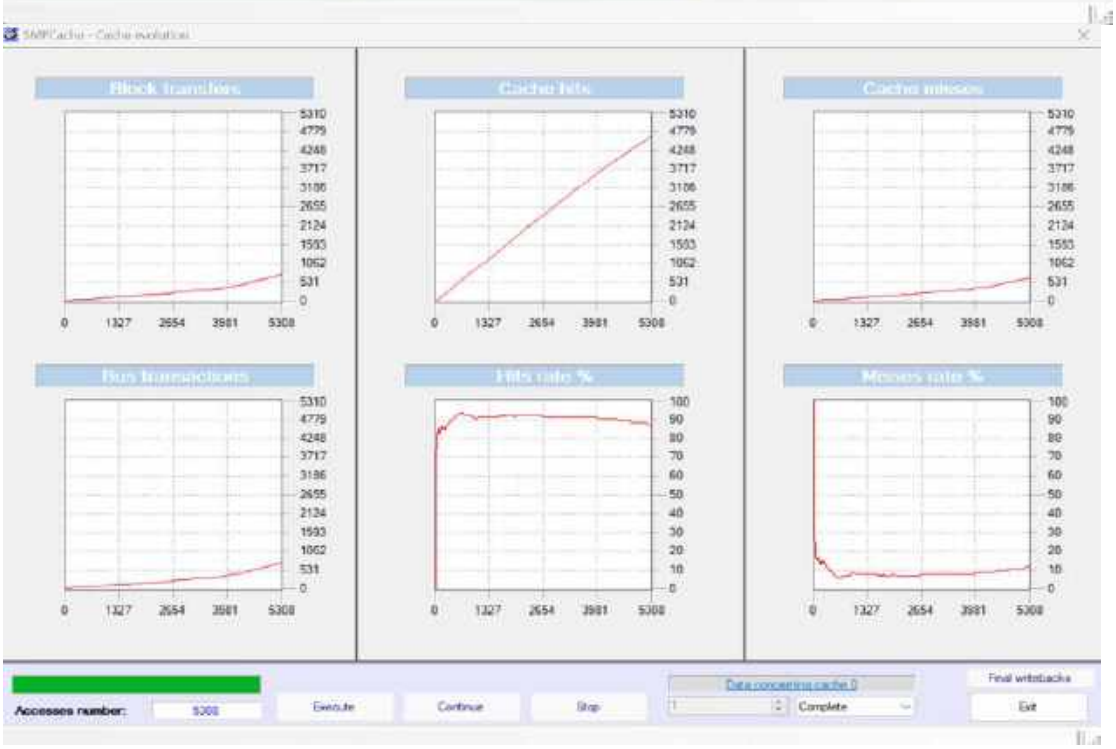
Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 32.
Words by block = 64 (block size = 256 bytes).
Blocks in main memory = 4096 (main memory size = 1024 KB).
Replacement policy = LRU.

Experiment

Configure the mapping using the following configurations: Direct, two-way set associative, four-way set associative, eight-way set associative, and fully-associative (remember: Number_of_ways = Number_of_blocks_in_cache / Number_of_cache_sets). For each of the configurations of mapping, configure the number of blocks in cache in order to get the following cache sizes: 4 KB (16 blocks in cache), 8 KB, 16 KB, and 32 KB (128 blocks in cache). For each configuration obtain the miss rate using the memory trace: Ear.

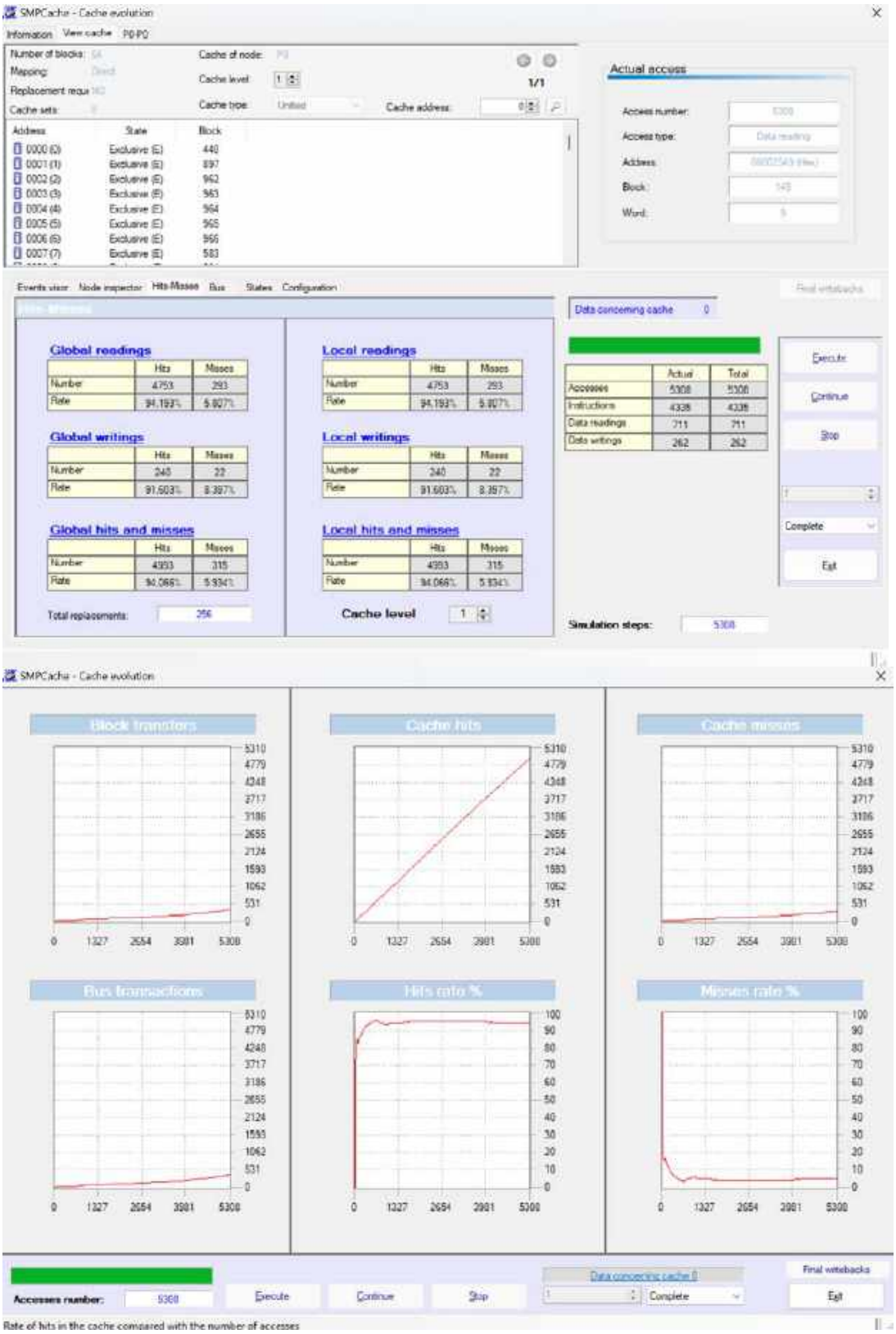
Cache Size = 4 KB	*Mapping = Direct*



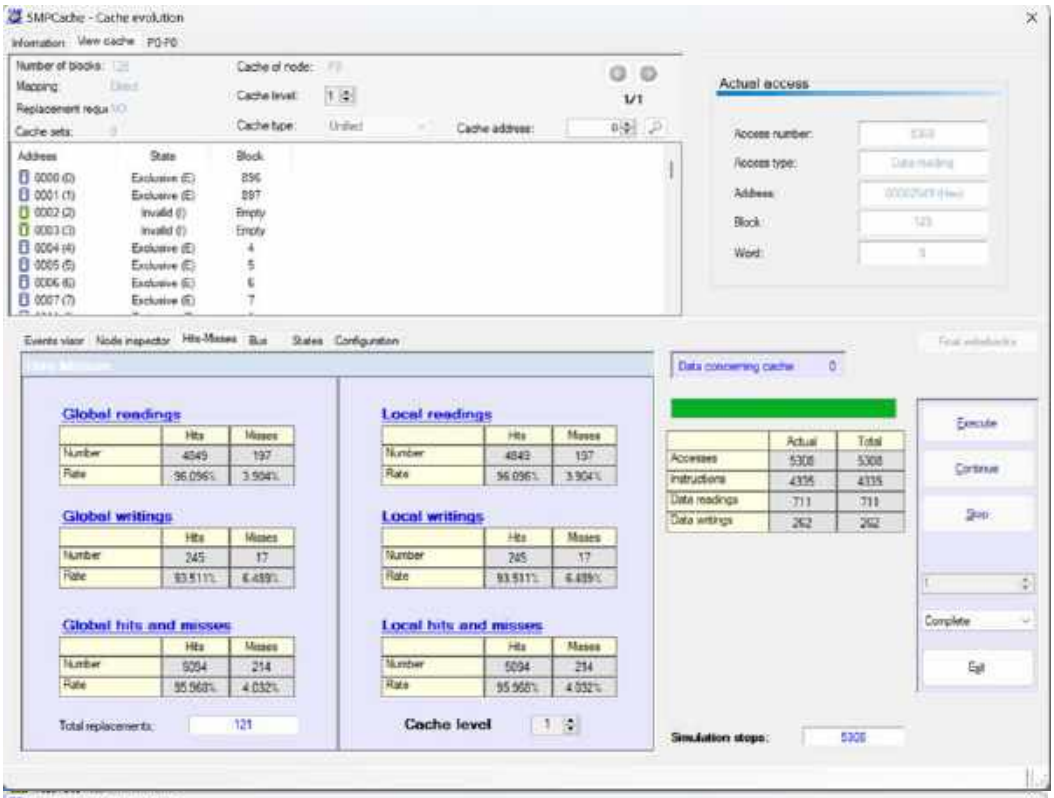


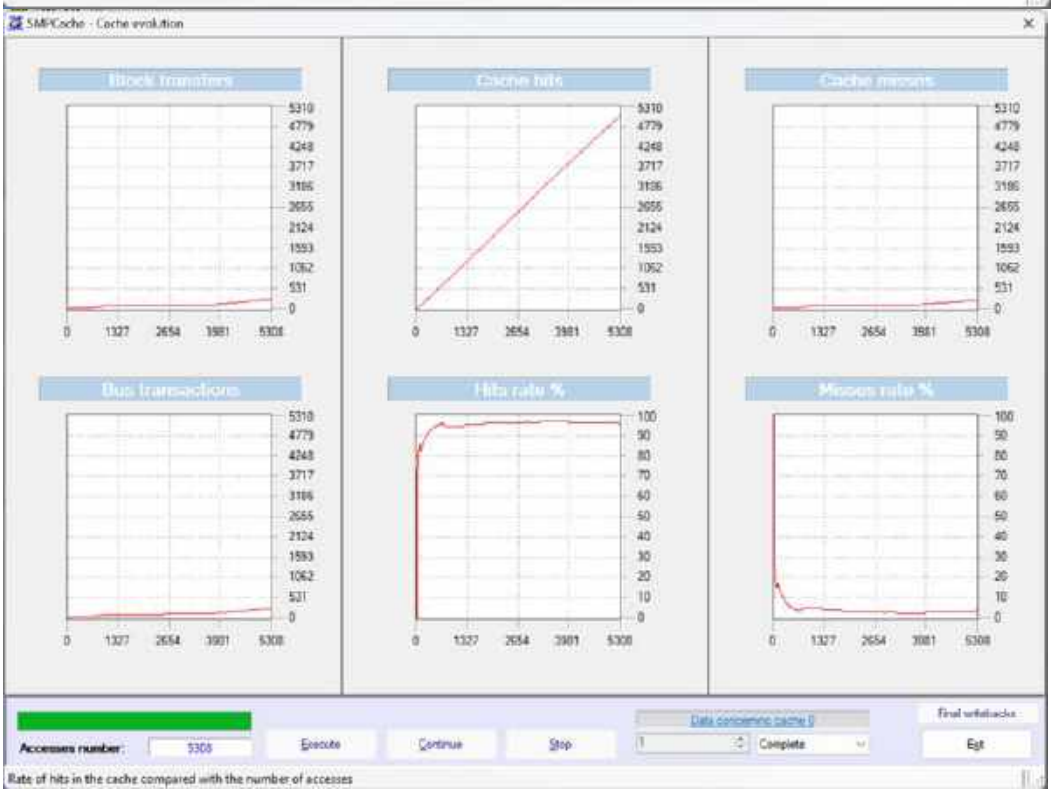
Cache Size = 8 KB	*Mapping = Direct*

Cache Size = 16 KB	*Mapping = Direct*



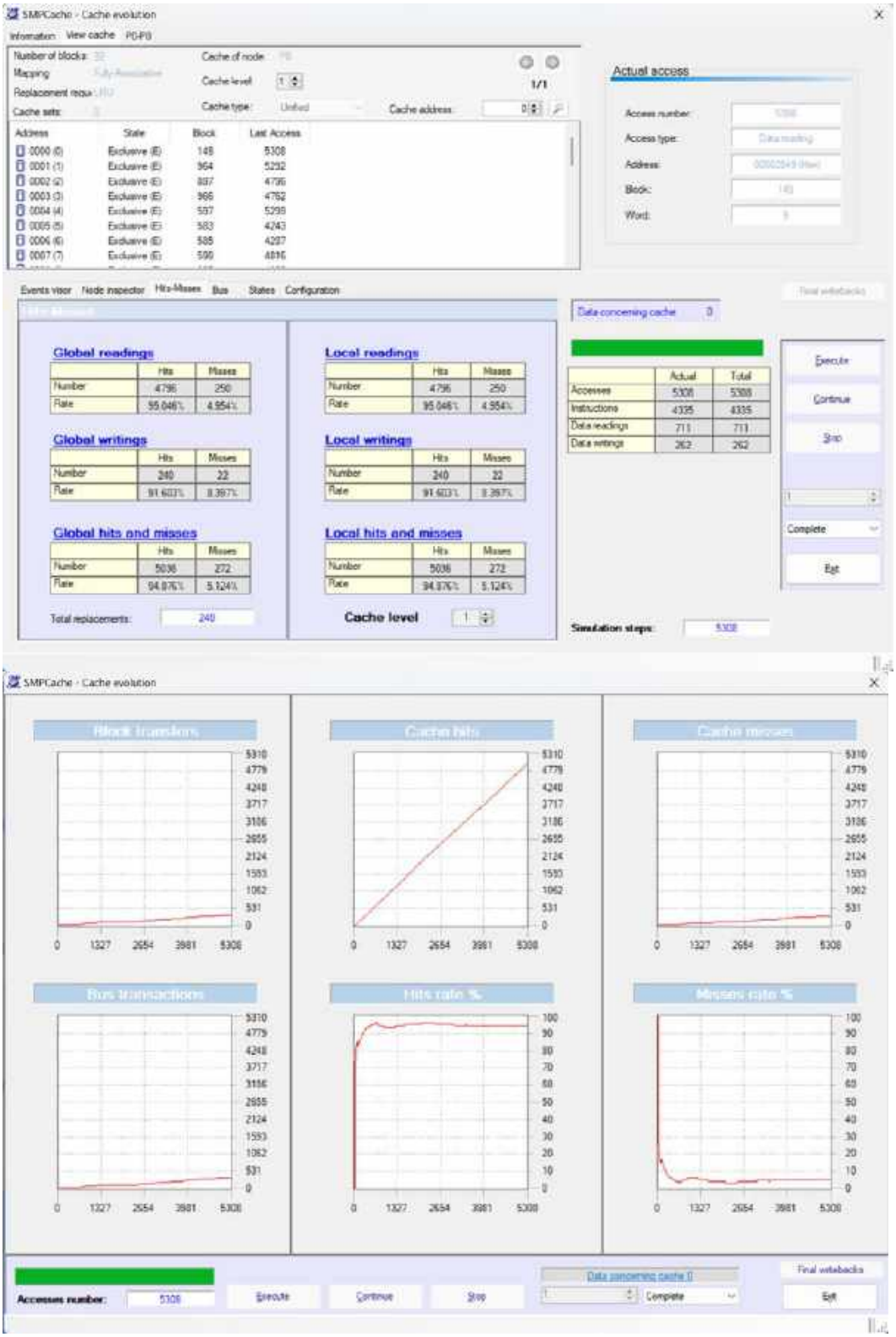
Cache Size = 32 KB	*Mapping = Direct*





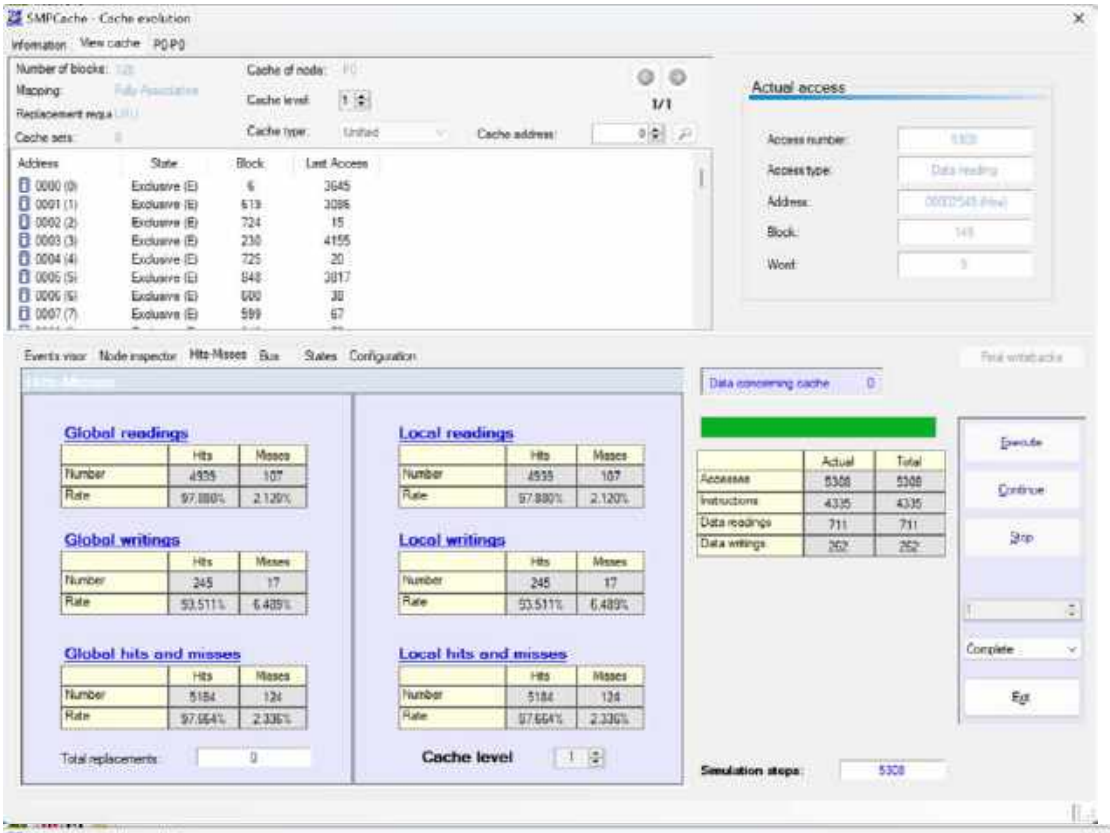
Cache Size = 4 KB	*Mapping = Fully Associative*

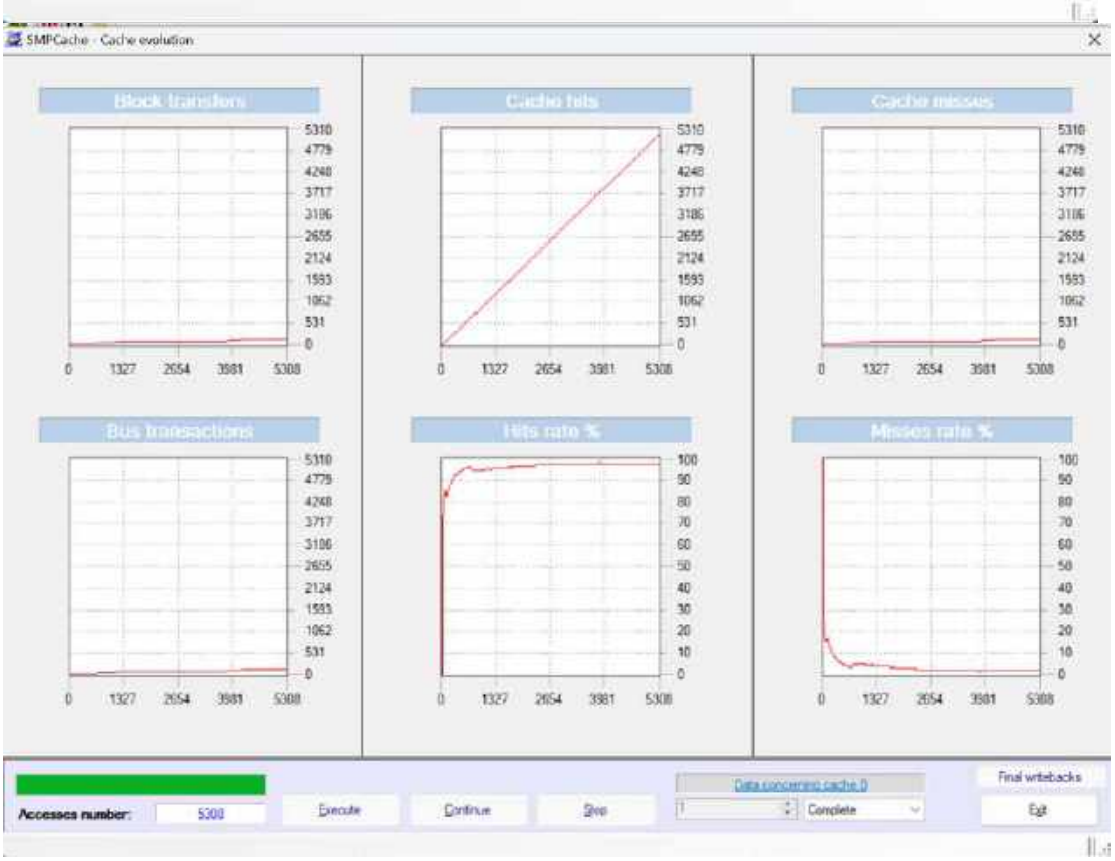
Cache Size = 8 KB	*Mapping = Fully Associative*



Cache Size = 16 KB	*Mapping = Fully Associative*

Cache Size = 32 KB	*Mapping = Fully Associative*



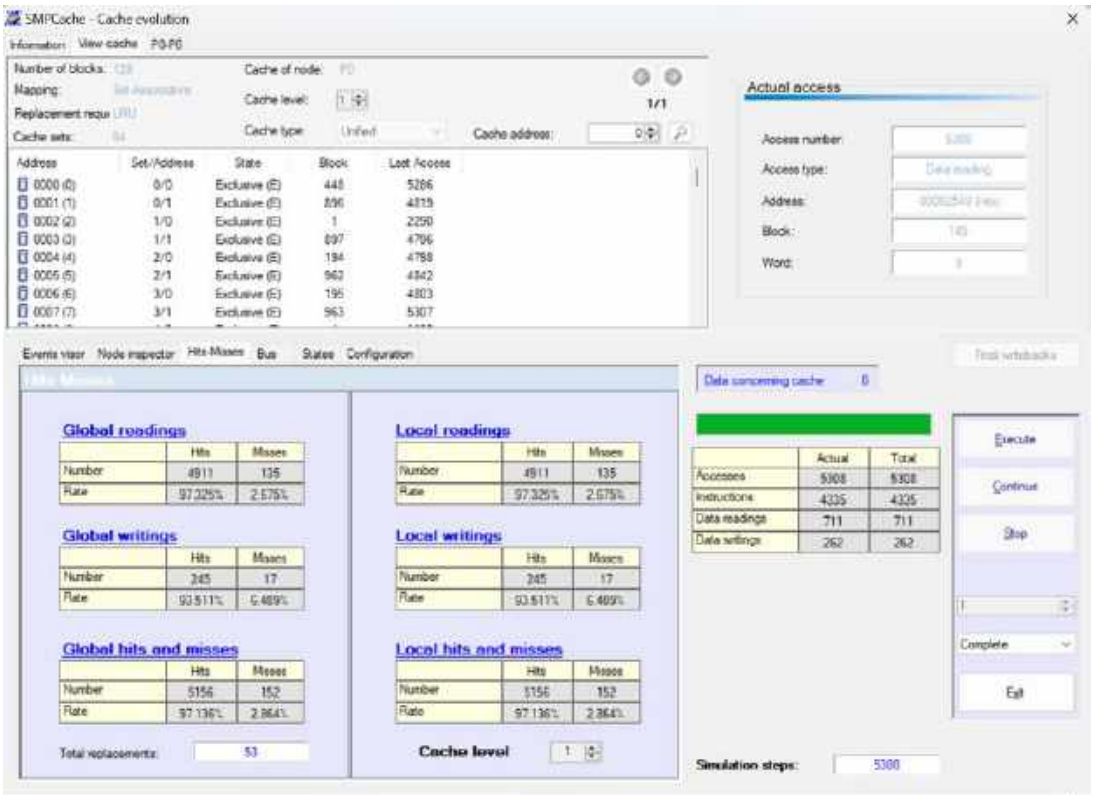


Cache Size = 4 KB	*Mapping = Two-Way Set Associative*

Cache Size = 8 KB	*Mapping = Two-Way Set Associative*

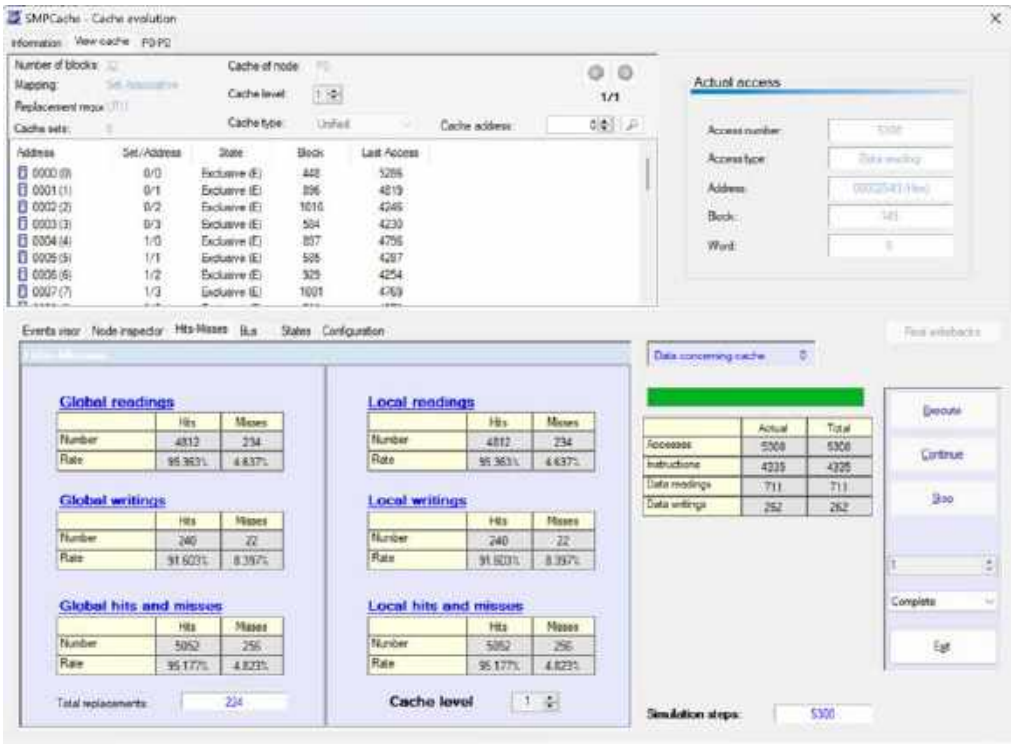
Cache Size = 16 KB	*Mapping = Two-Way Set Associative*

Cache Size = 32 KB	*Mapping = Two-Way Set Associative*

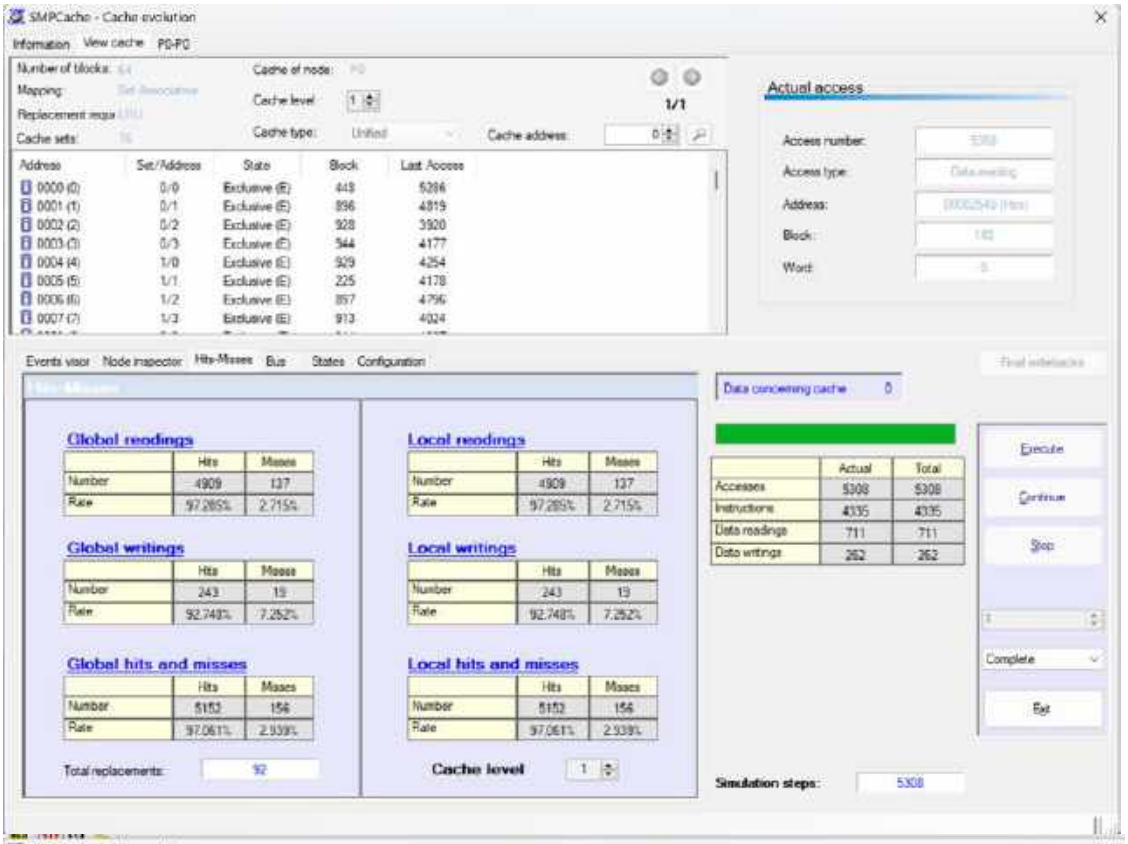


Cache Size = 4 KB	*Mapping = Four-Way Set Associative*

Cache Size = 8 KB	*Mapping = Four-Way Set Associative*



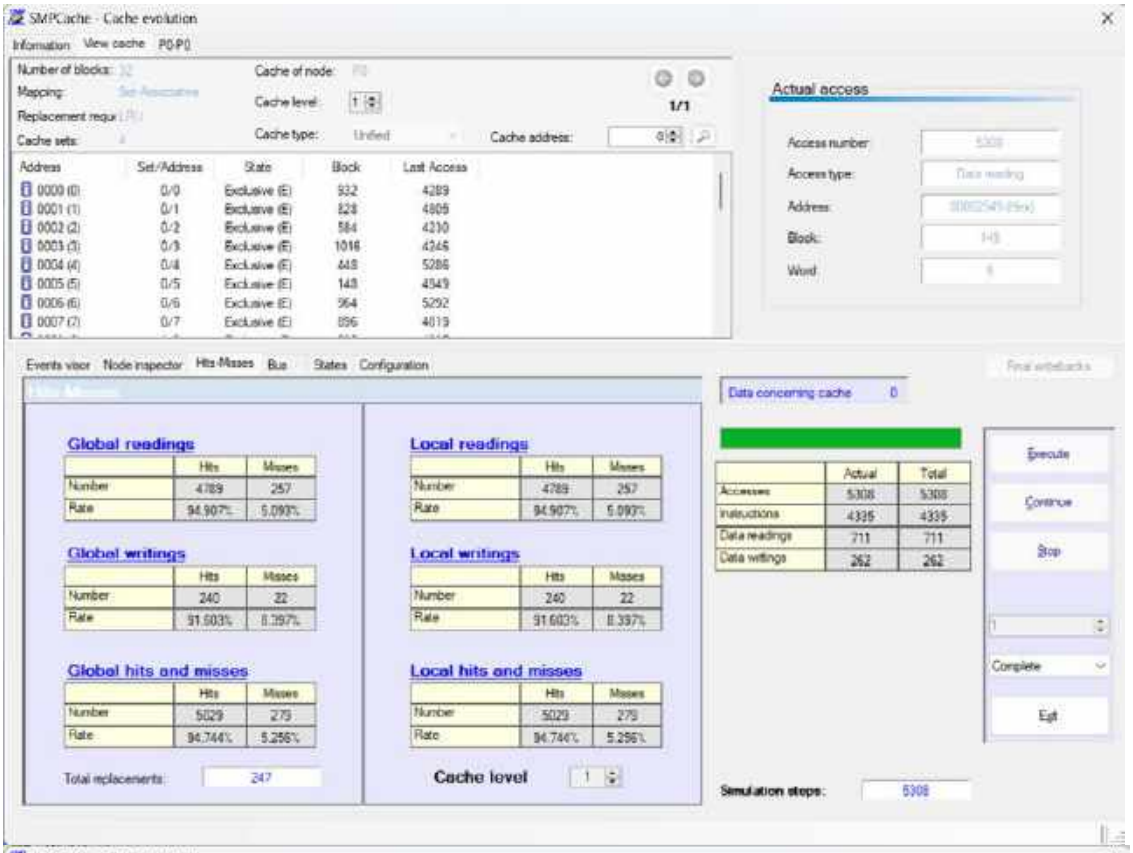
Cache Size = 16 KB	*Mapping = Four-Way Set Associative*

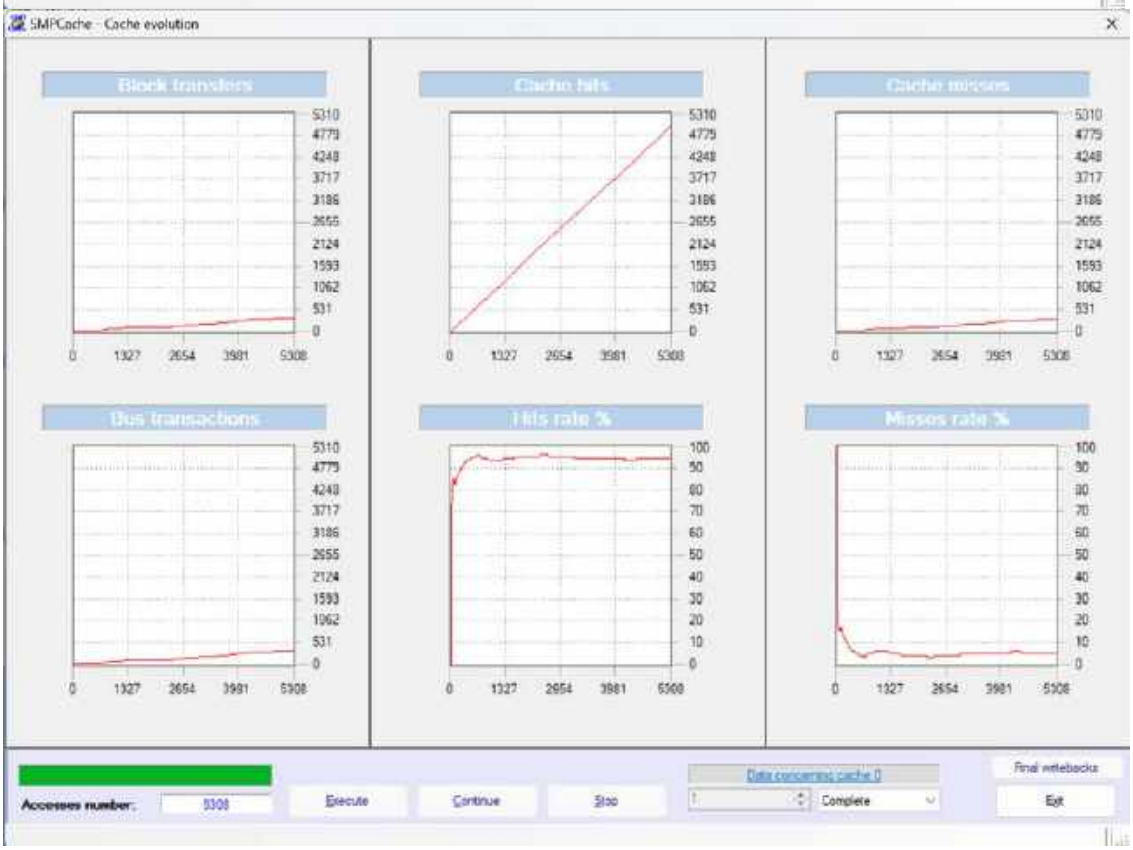


Cache Size = 32 KB	*Mapping = Four-Way Set Associative*

Cache Size = 4 KB	*Mapping = Eight-Way Set Associative*

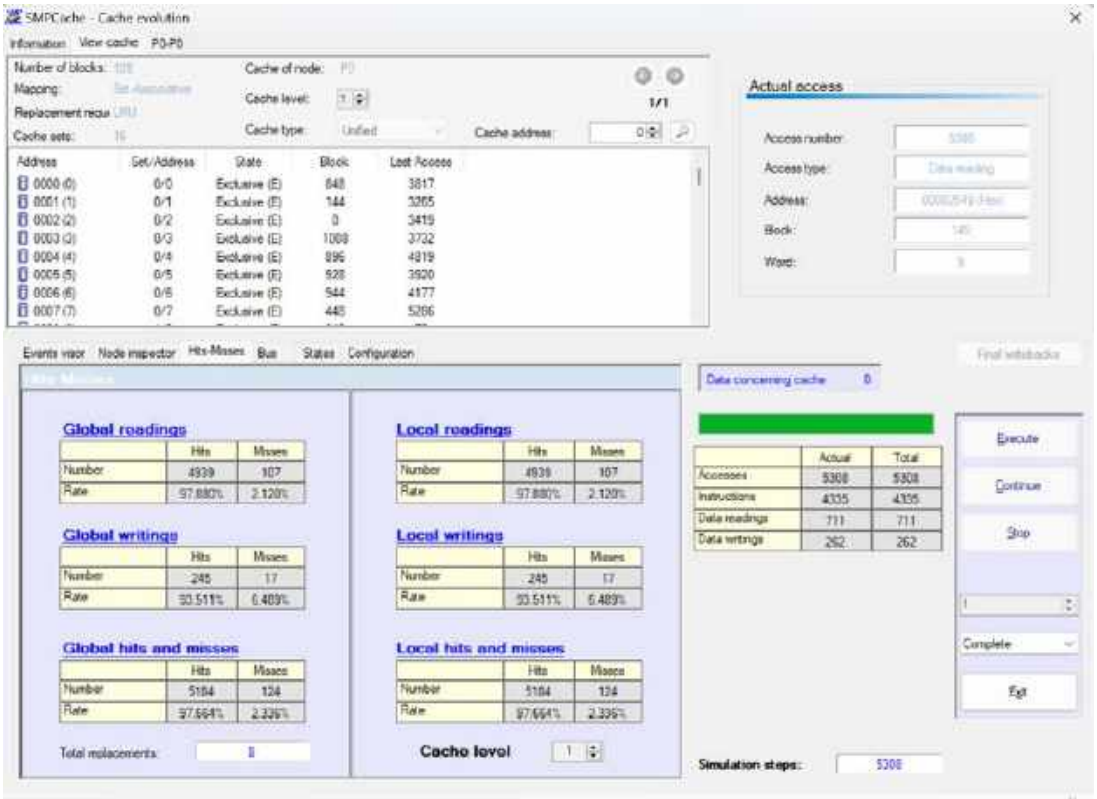
Cache Size = 8 KB	*Mapping = Eight-Way Set Associative*





Cache Size = 16 KB	*Mapping = Eight-Way Set Associative*

Cache Size = 32 KB	*Mapping = Eight-Way Set Associative*



Questions

Does the miss rate increase or decrease as the associativity increases? Why? What does it happen with the conflict misses when you enlarge the associativity grade?

Yes. When associativity advances, the miss rate decreases. Because associativity allows squares to travel some edges in reserve, and more squares per set are less prone to overwriting. When the associativity grade is increased, the conflict misses reduce dramatically. This is due to the fact that associativity will only effect struggle misses.

Does the influence of the associativity grade increase or decrease as the cache size increases? Why?

As cache capacity increases, the associative grade drops because advantages get shorter. This is consistent with the assumption that increasing associativity reduces conflict misses; but, as cache size increases, certain types of misses are less affected. Figure 1 shows how the rise in the association is remarkably similar between the eight-way association and the overall association.

In conclusion, does the increase of associativity improve the system performance? If the answer is yes, in general, which is the step with more benefits: from direct to 2-way, from 2-way to 4-way, from 4-way to 8-way, or from 8-way to fully-associative?

Yes, increasing associativity improves system performance. The transition from direct to 2-way set associative is the most advantageous. This is due to a drop in the maximum miss rate. The system will improve the greatest at this moment.

Task 6

Influence of the Replacement Policy

Purpose

Show the influence of the replacement policy on the miss rate.

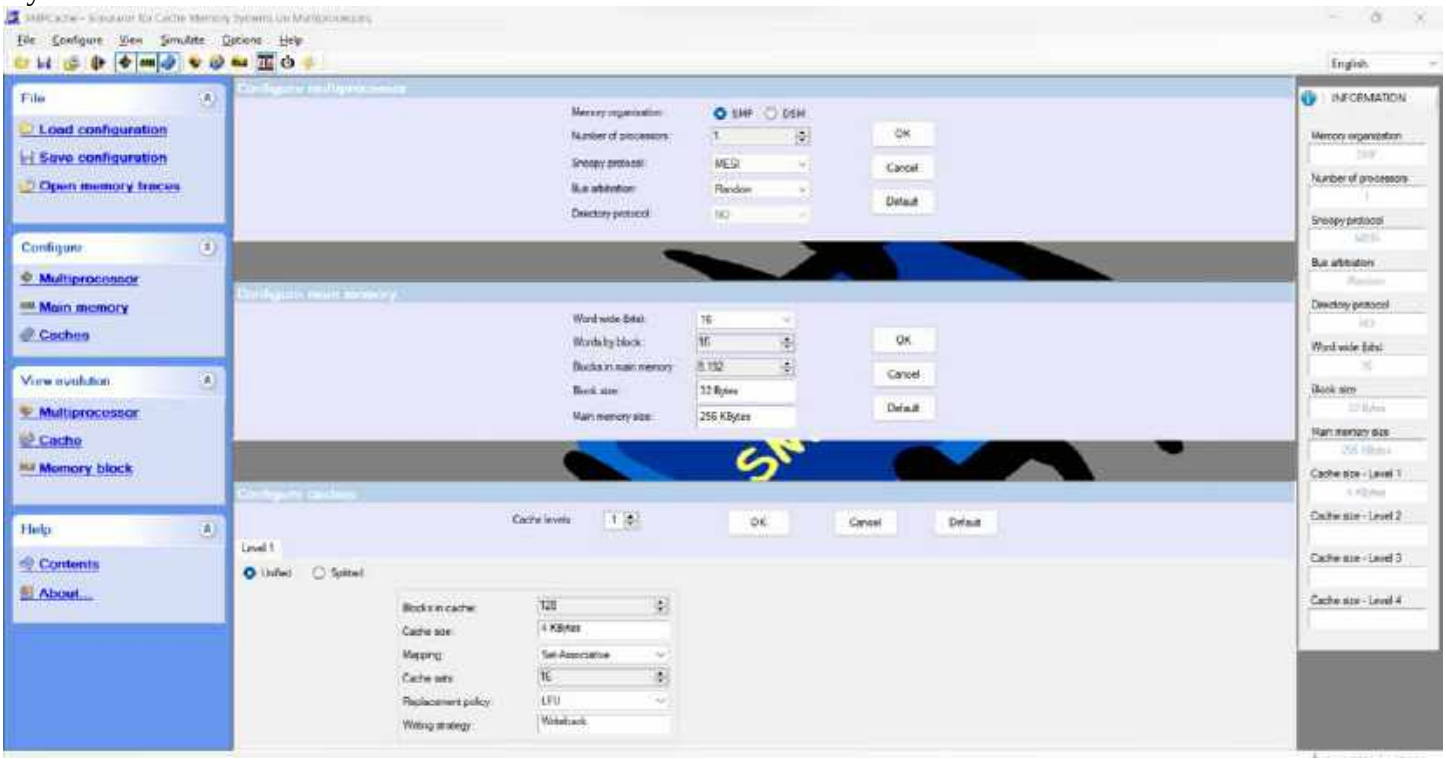
Configuration

Processors in SMP = 1.
Cache coherence protocol = MESI.
Scheme for bus arbitration = Random.
Word wide (bits) = 16.
Words by block = 16 (block size = 32 bytes).
Blocks in main memory = 8192 (main memory size = 256 KB).
Blocks in cache = 128 (cache size = 4 KB).
Mapping = 8-way set-associative (cache sets = 16).

Experiment

Configure the blocks in cache using the following configurations: 1 (cache size = 0,03 KB), 2, 4, 8, 16, 32, 64, 128, 256, and 512 (cache size = 16 KB). For each of the configurations, obtain the miss rate using the trace files (extension ".prg"): Hydro, Nasa7, Cexp, Mdljd, Ear, Comp, Wave, Swm and UComp.

Hydro LFU



File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION

File
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Save configuration
Open memory traces
Configure
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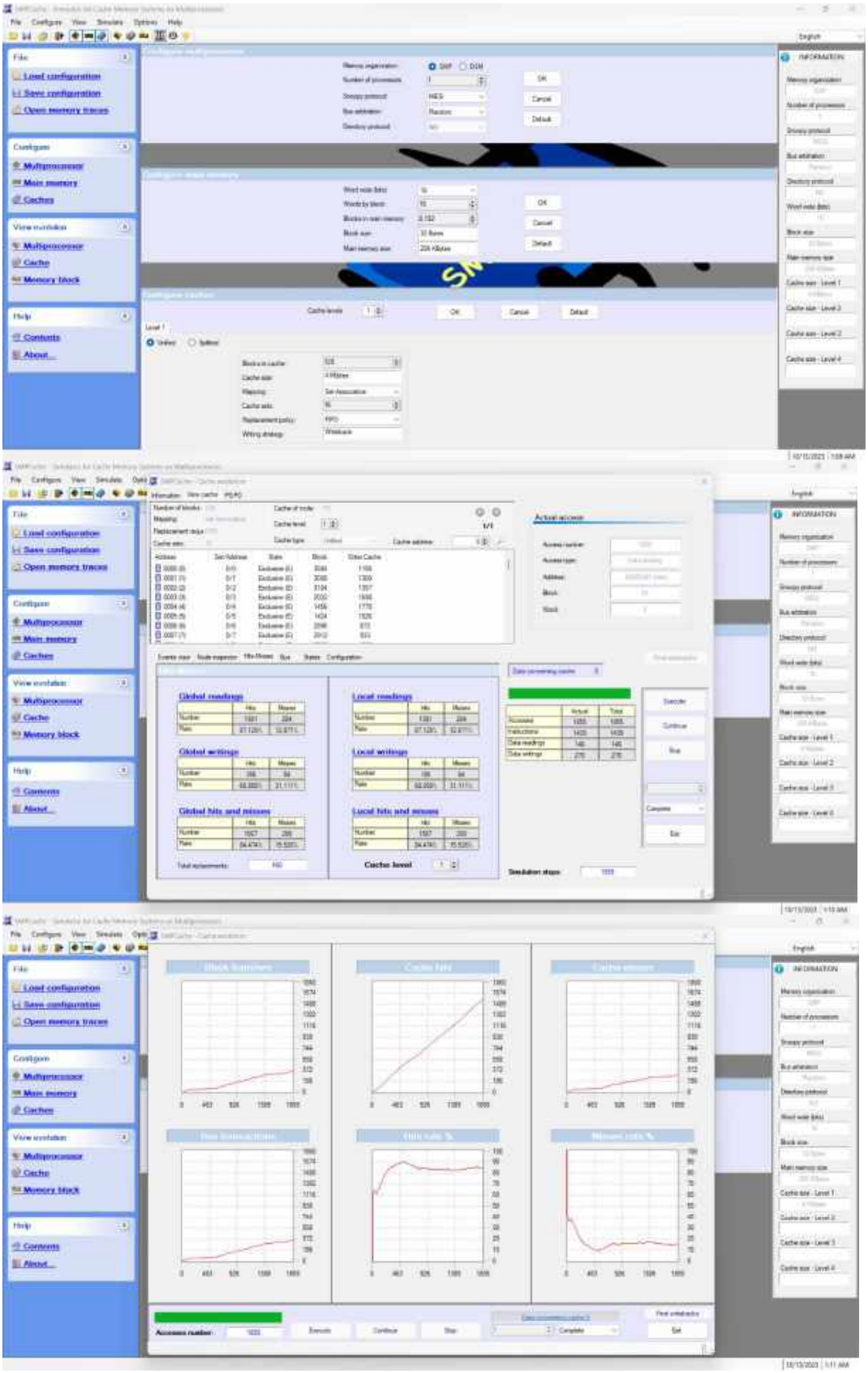
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Accesses number:
Execute
Continue
Stop
Exit
INFORMATION

Hydro FIFO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Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
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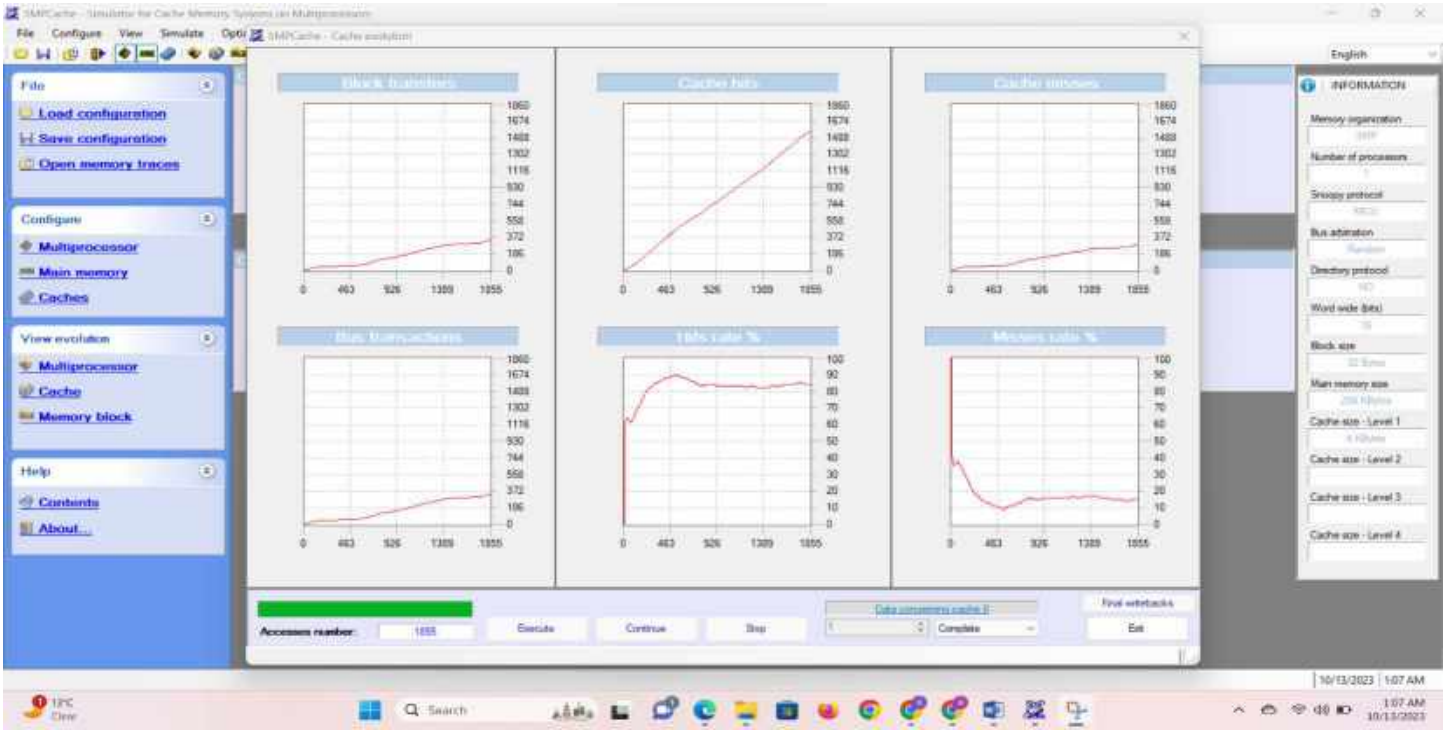
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Global readings
Global writings
Global hits and misses
Local readings
Local writings
Local hits and misses
Cache level
Actual access

Hydro LRU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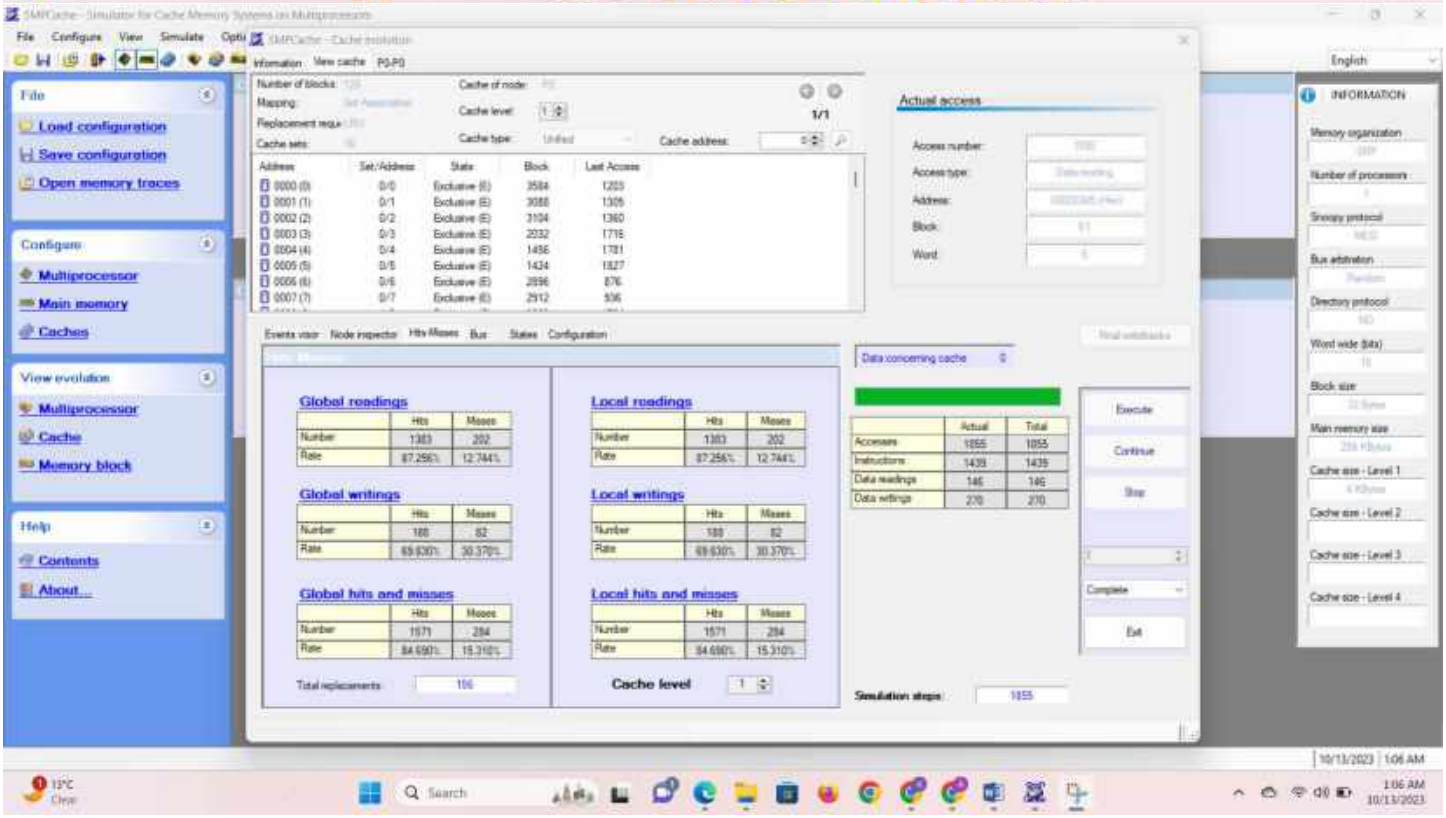
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number
Execute
Continue
Stop
Exit
INFORMATION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Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
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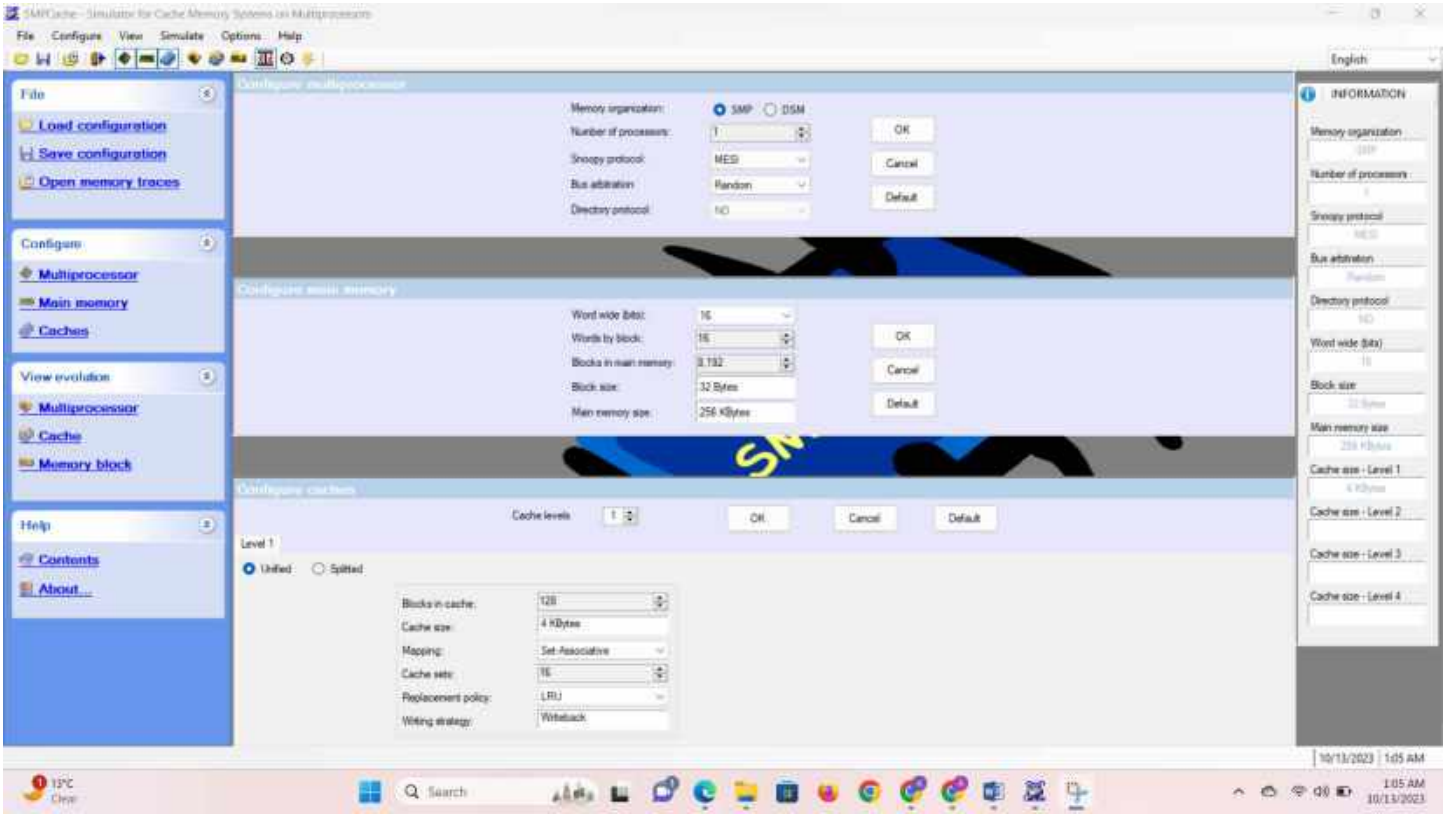
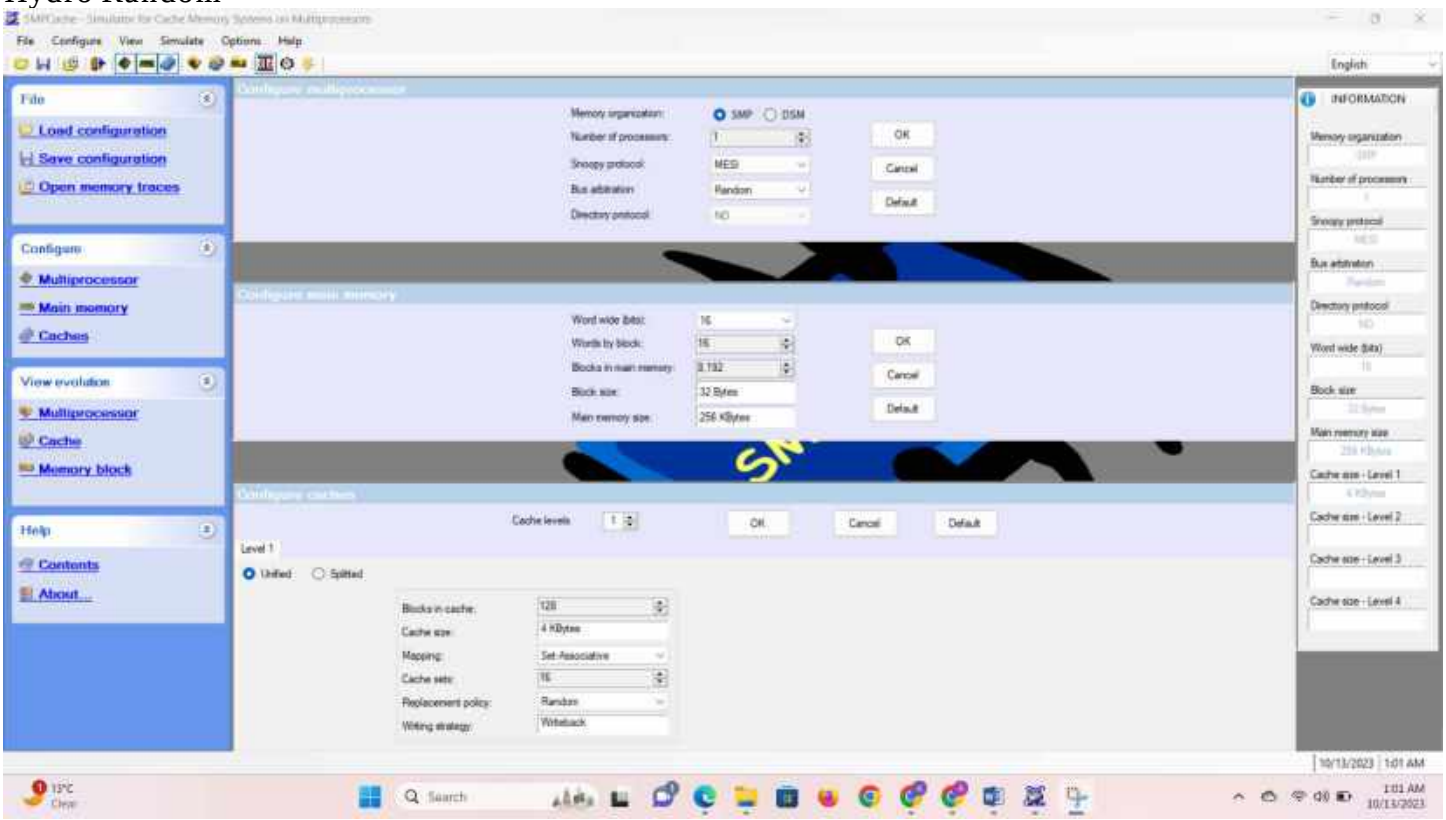
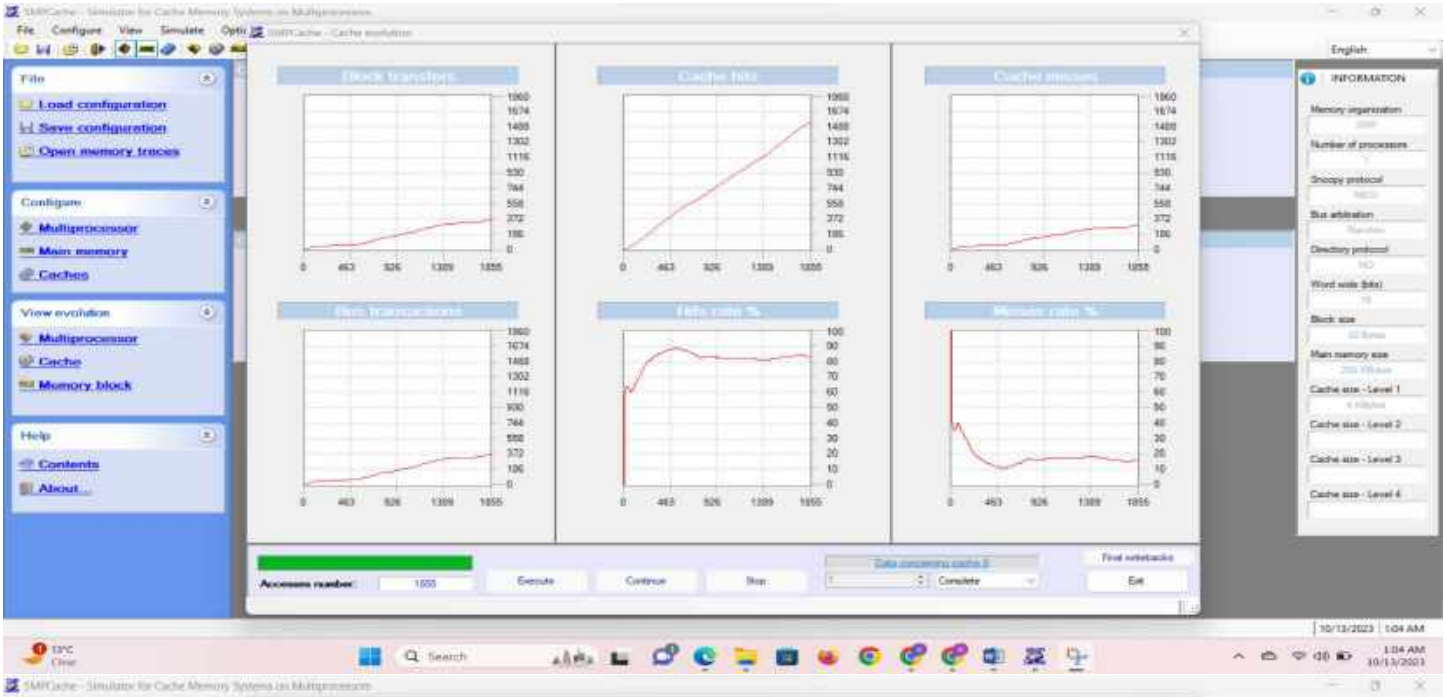
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION



Hydro Random

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Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
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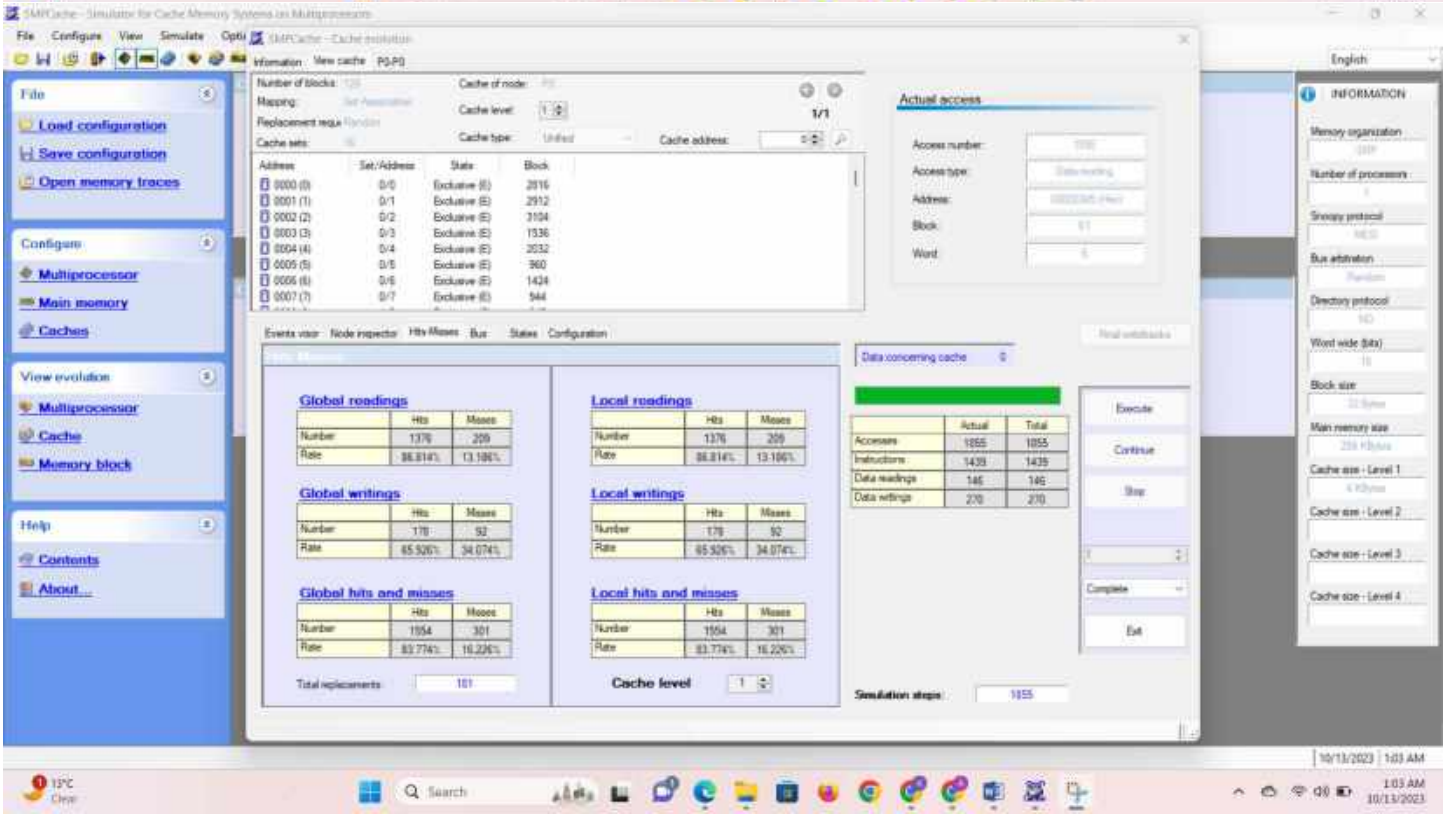
Block transfers
Cache hits
Cache misses
Hits ratio %
Misses ratio %
Accesses number:
Execute
Continue
Stop
Exit
INFORMATION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Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
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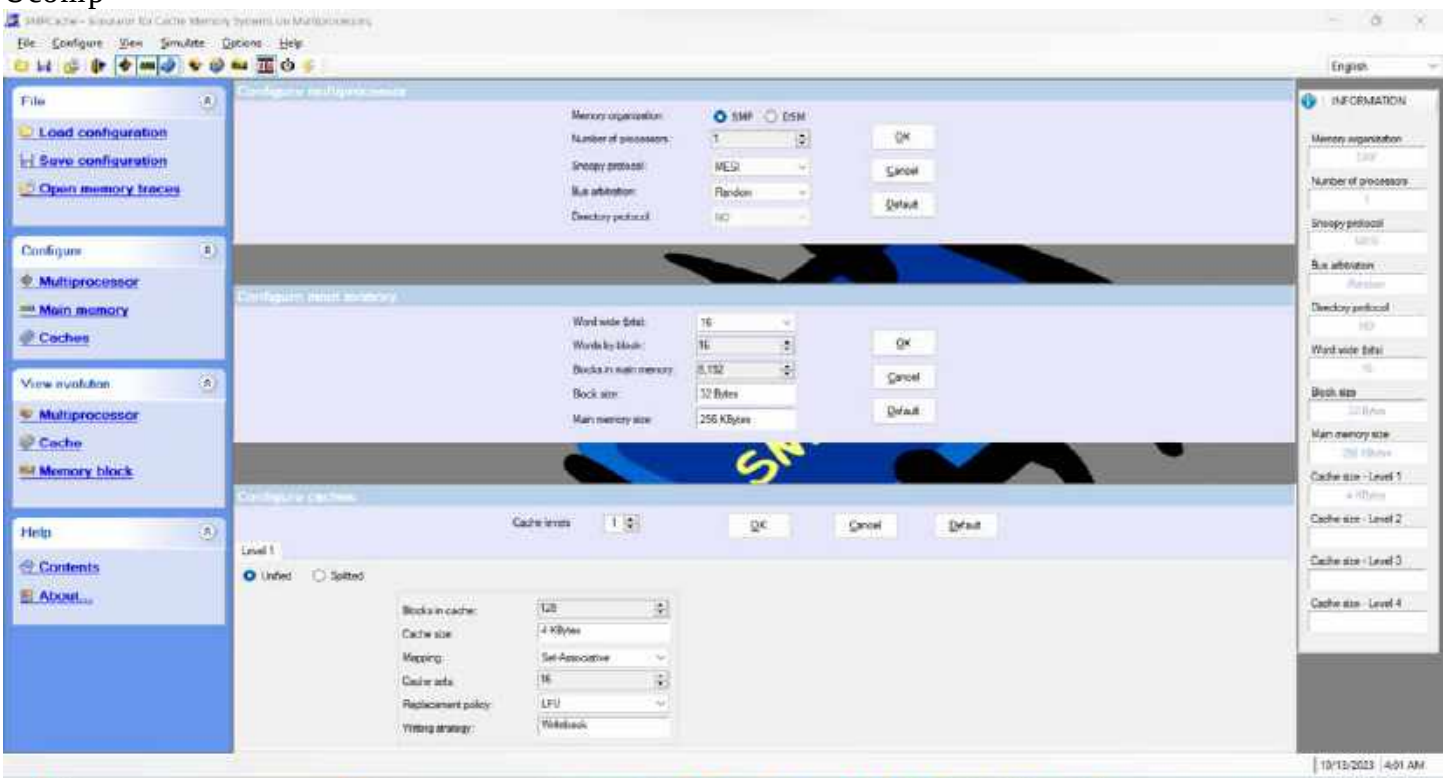
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Access number:
Access type:
Address:
Block:
Word:
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Total replacements
Cache level
Simulation steps:
Execute
Continue
Stop
Exit
INFORMATION

Ucomp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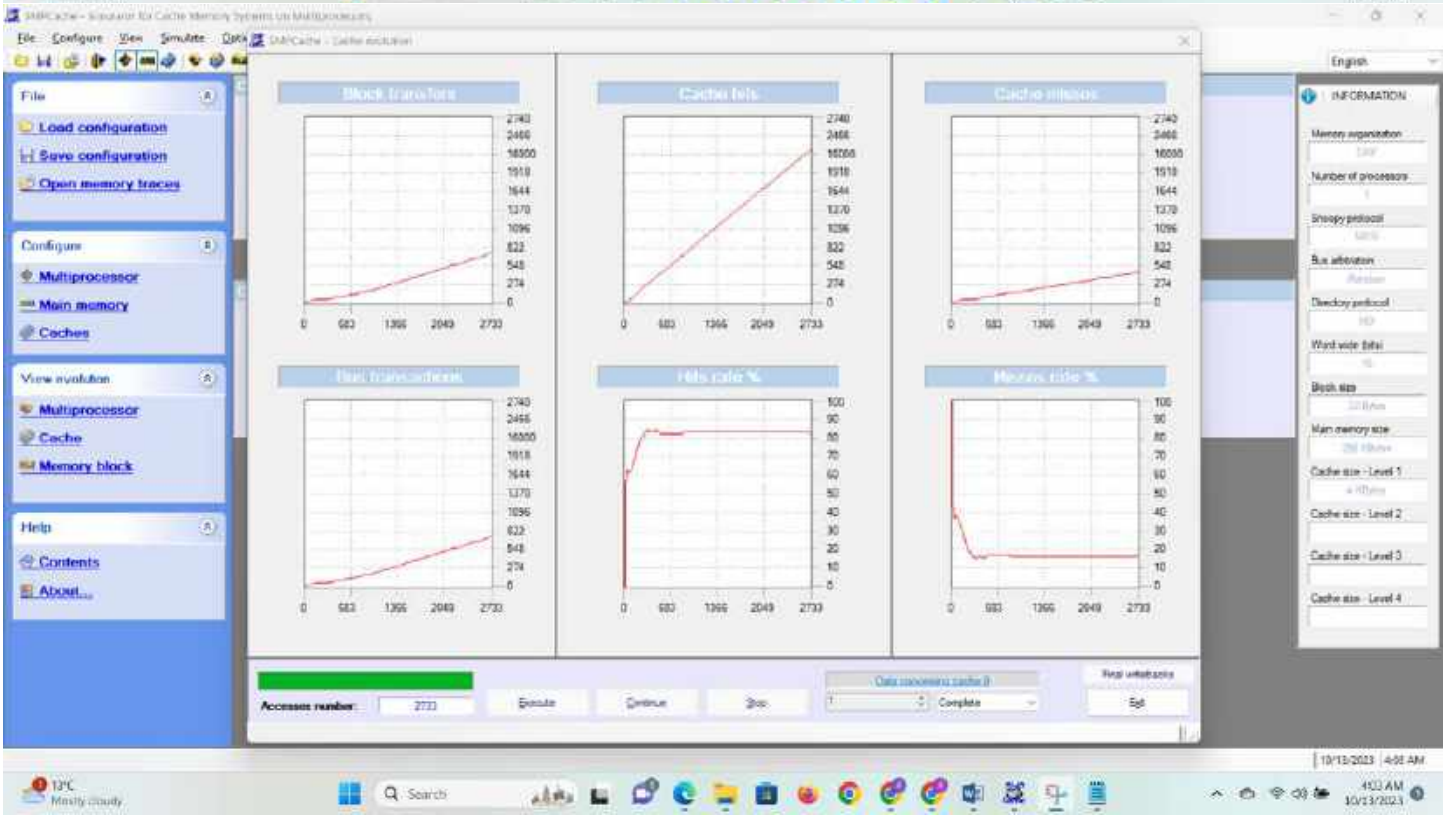
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION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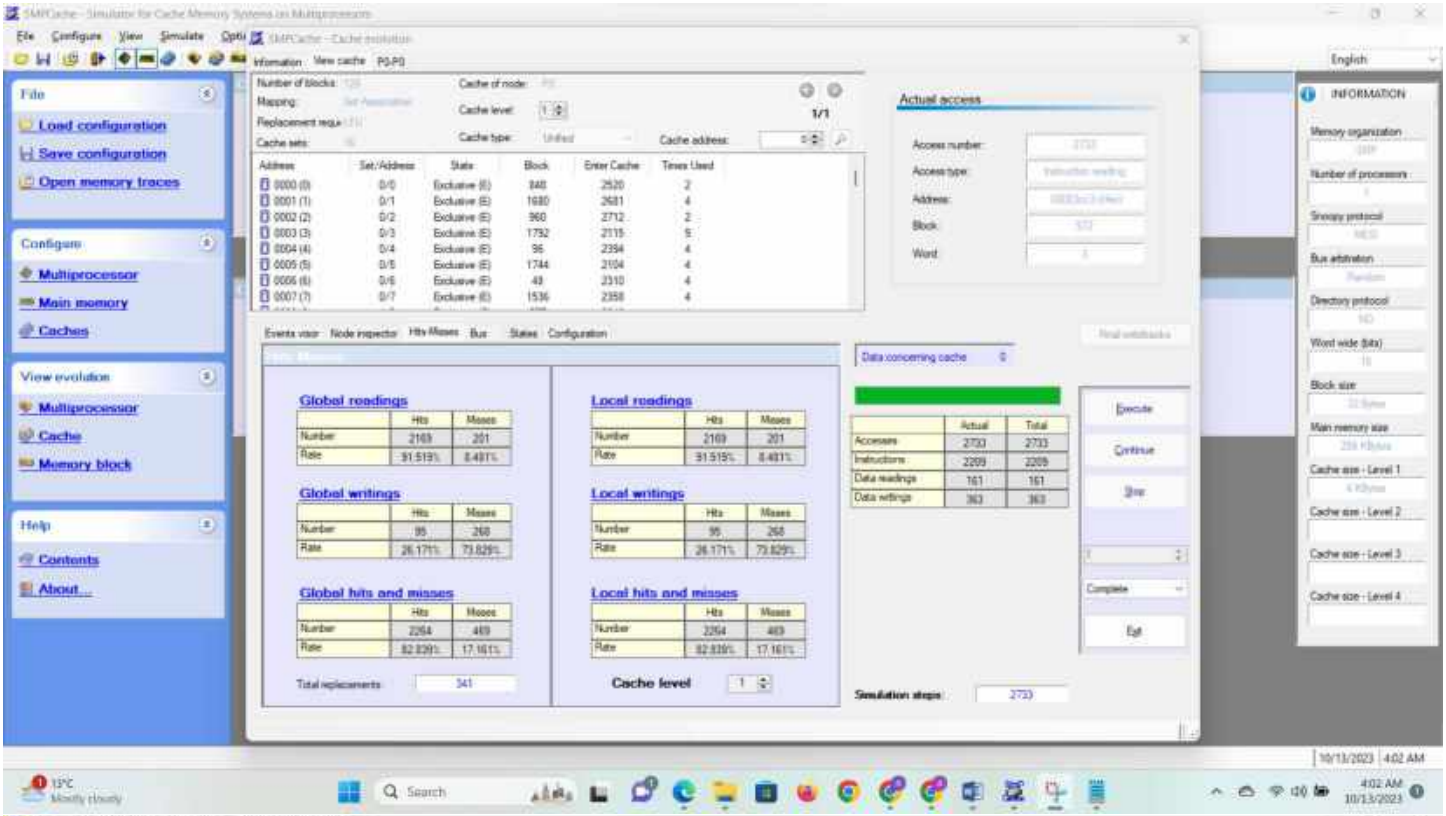
Help
Contents
About...
INFORMATION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Multiprocessor
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Local writings
Global hits and misses
Local hits and misses
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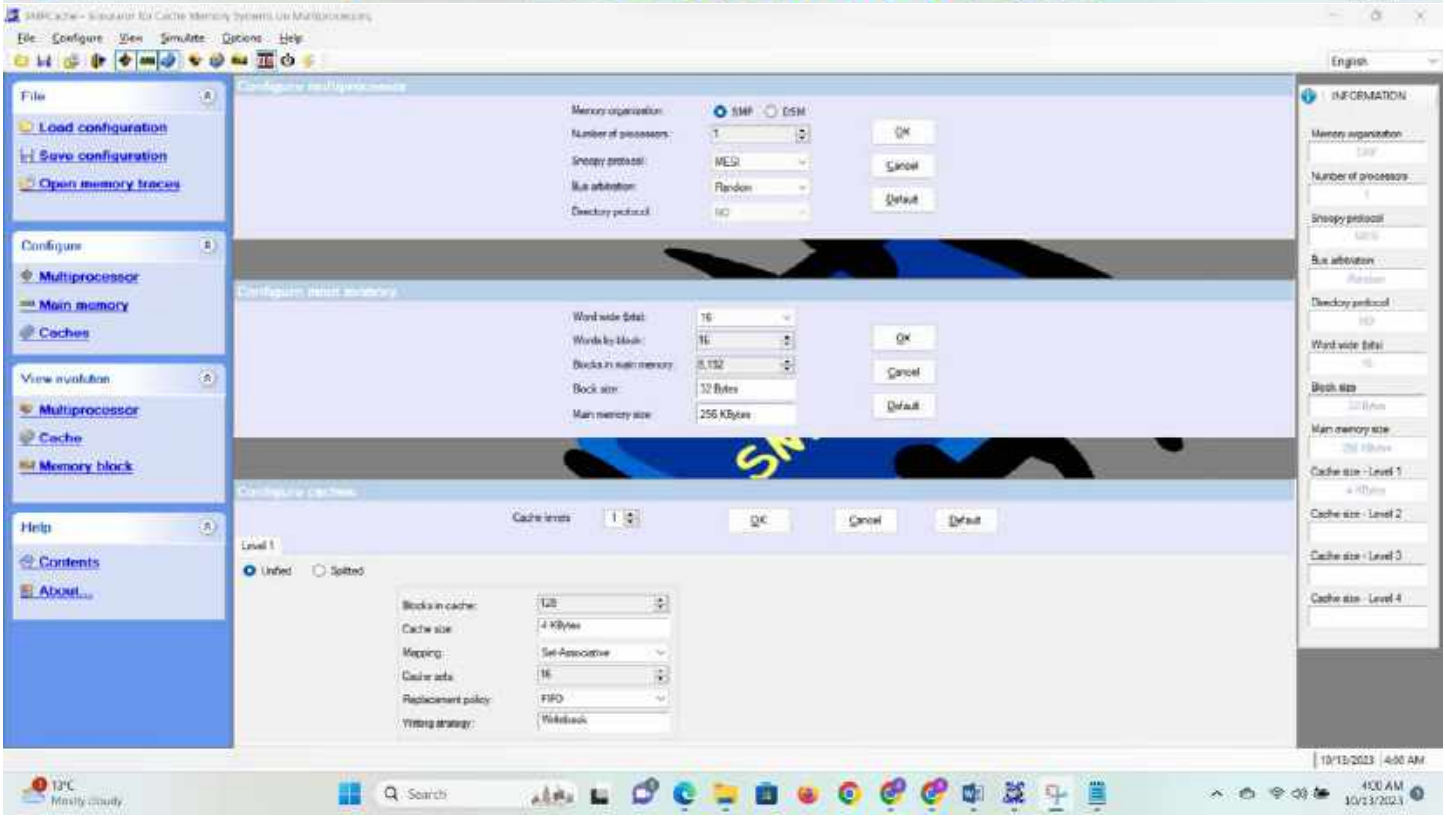
Exit
INFORMATION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Caches
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Cache
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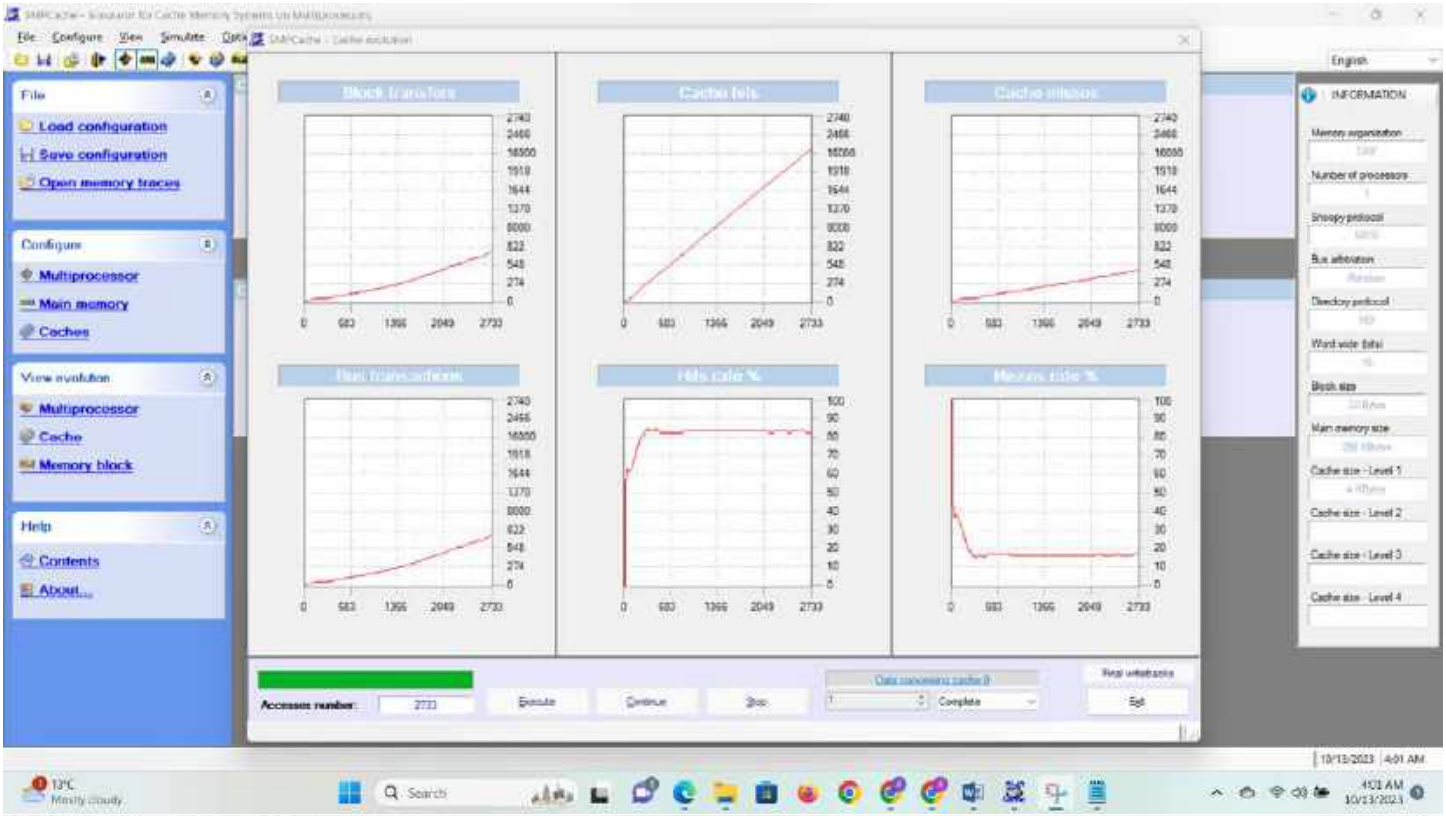
Help
Contents
About...
OK
Cancel
Default
INFORMATION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Open memory traces
Configure
Multiprocessor
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View evolution
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Contents
About...
Block transfers
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Misses rate %
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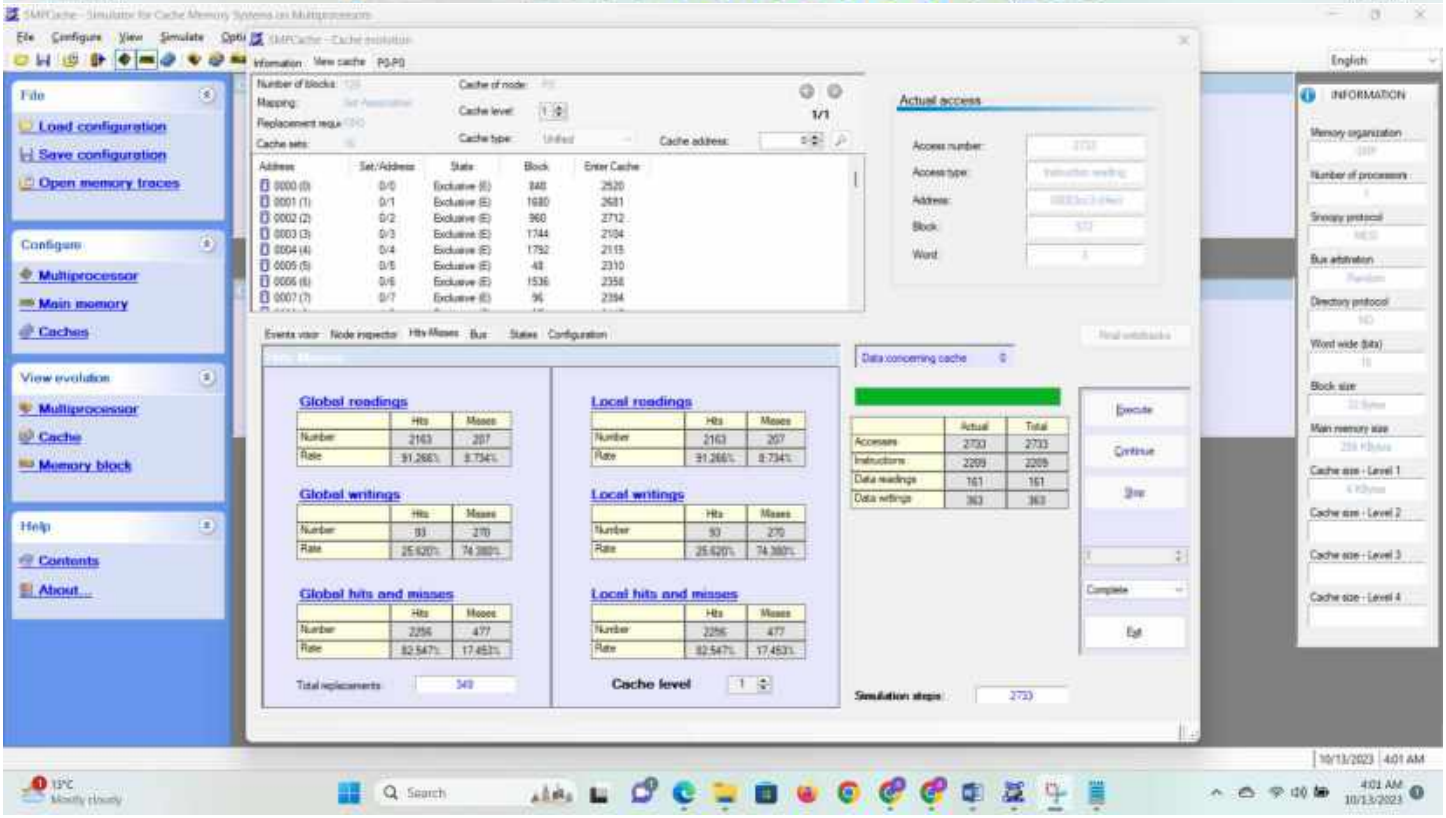
Number of processors
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4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Open memory traces
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About...
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Word:
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INFORMATION
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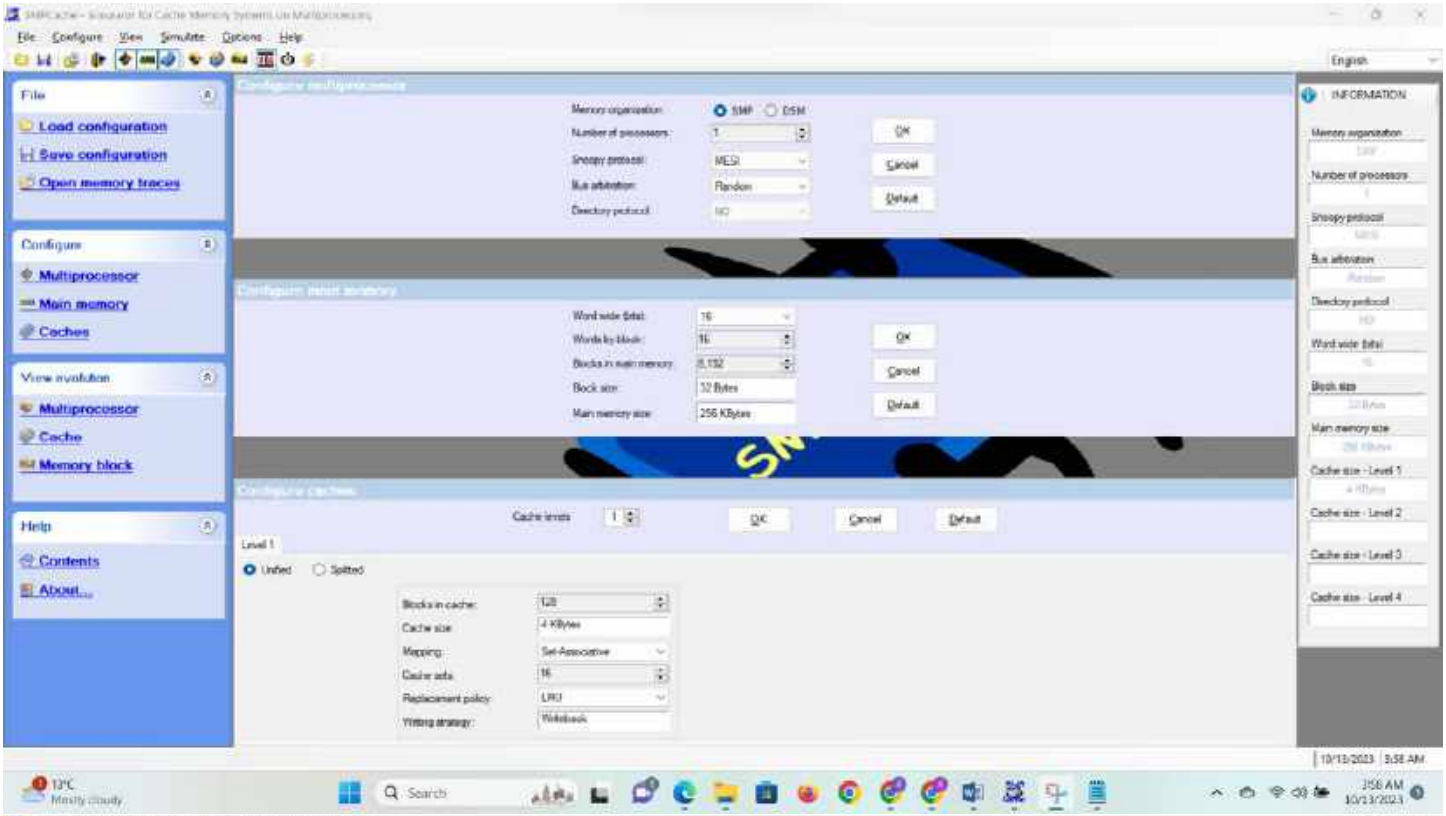
Number of processors
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4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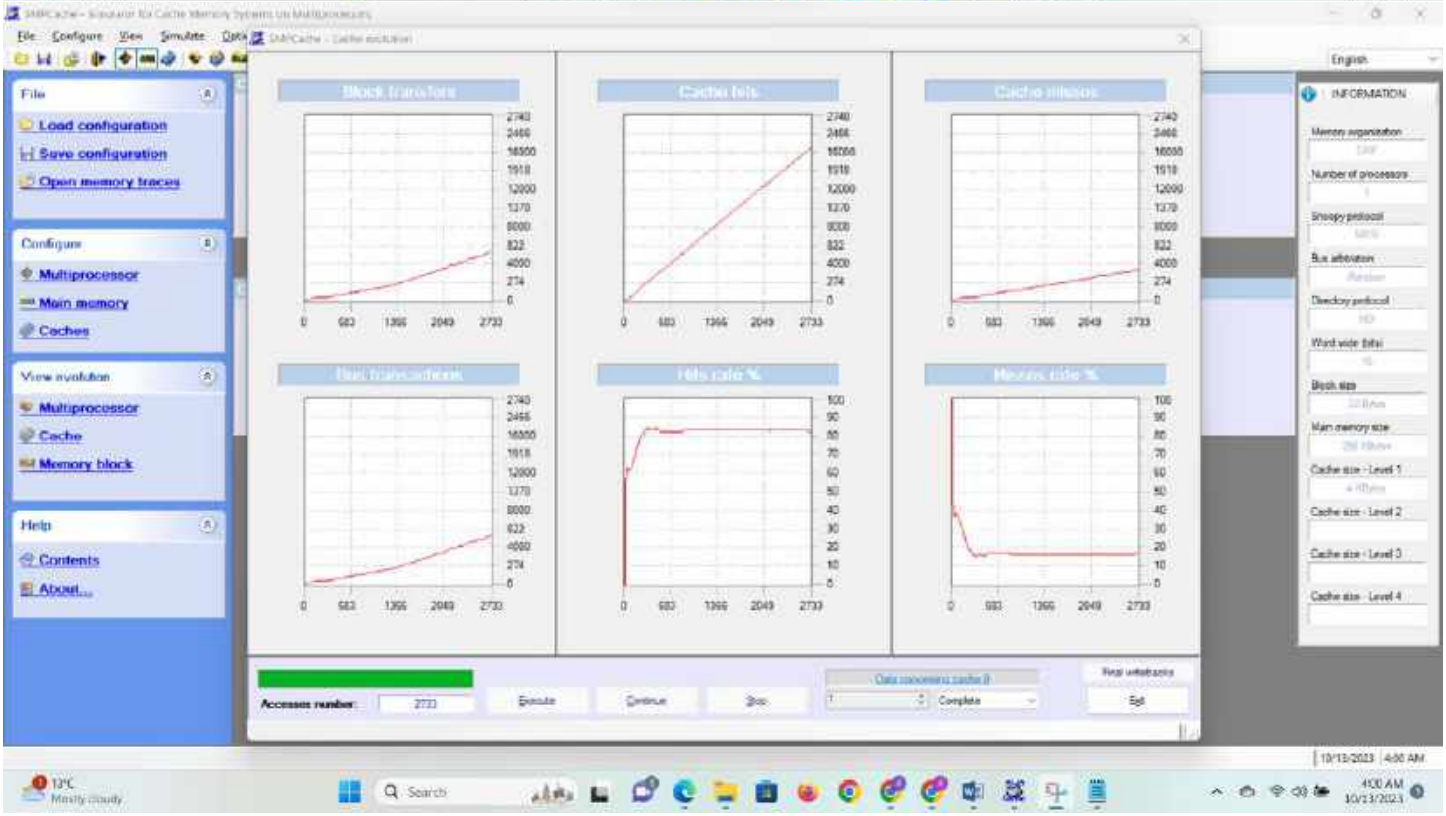
Help
Contents
About...
INFORMATION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Memory block
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Contents
About...
INFORMATION
Accesses number:
Execute
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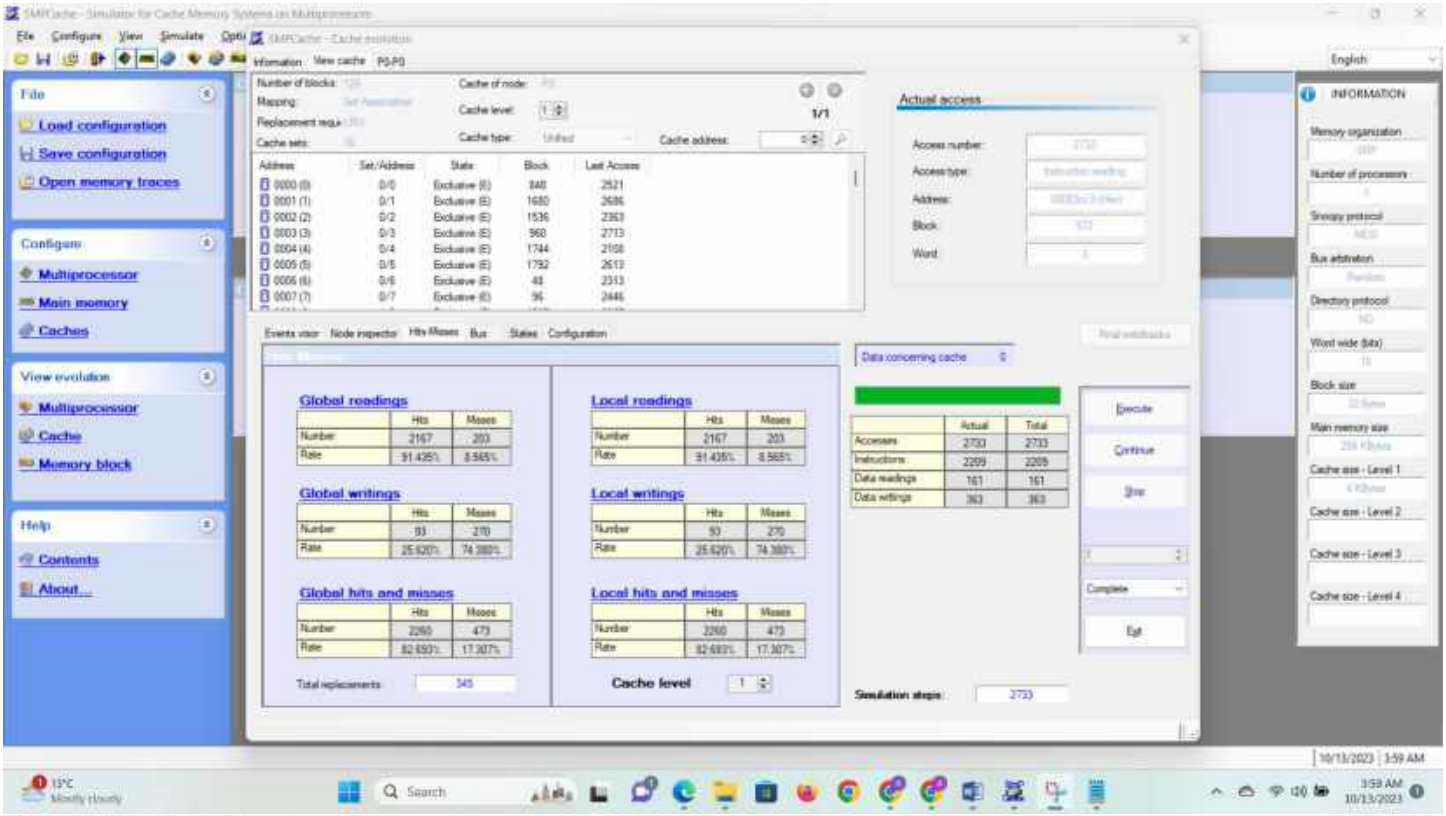
Stop
Exit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Local readings
Global writings
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Local hits and misses
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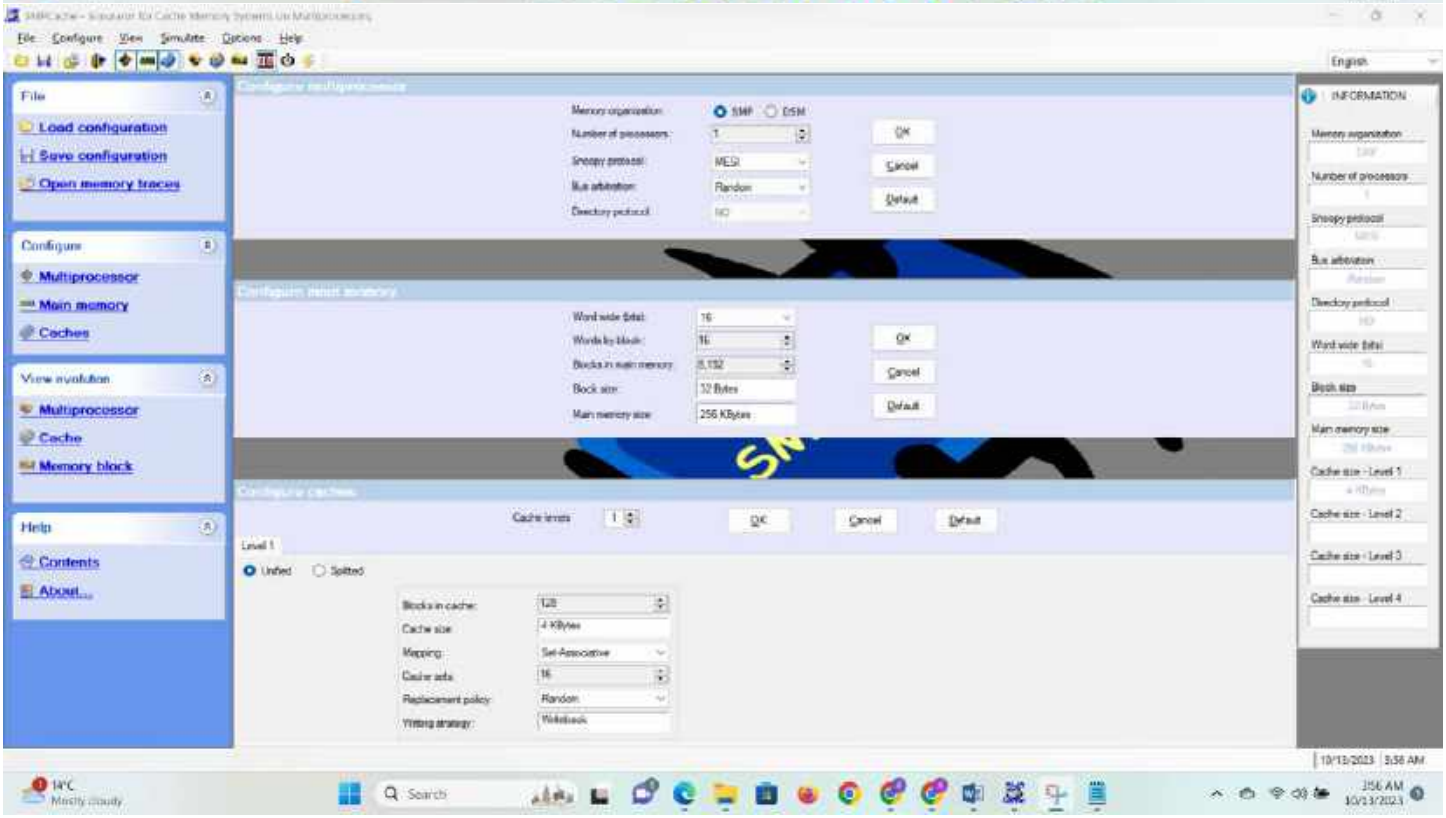
Stop
Exit
INFORMATION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Caches
View evolution
Multiprocessor
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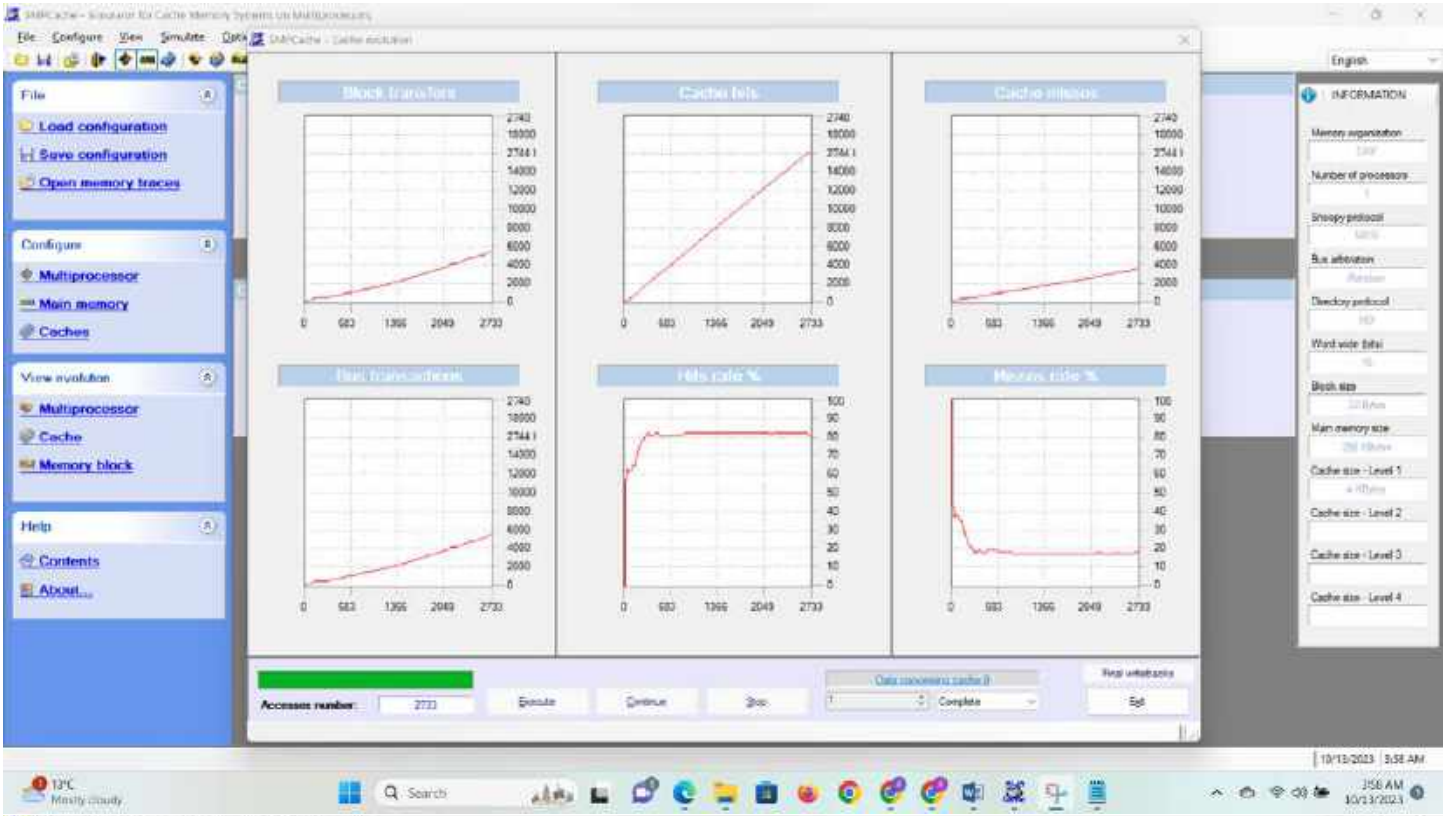
Help
Contents
About...
OK
Cancel
Default
INFORMATION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Open memory traces
Configure
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Main memory
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Cache hits
Cache misses
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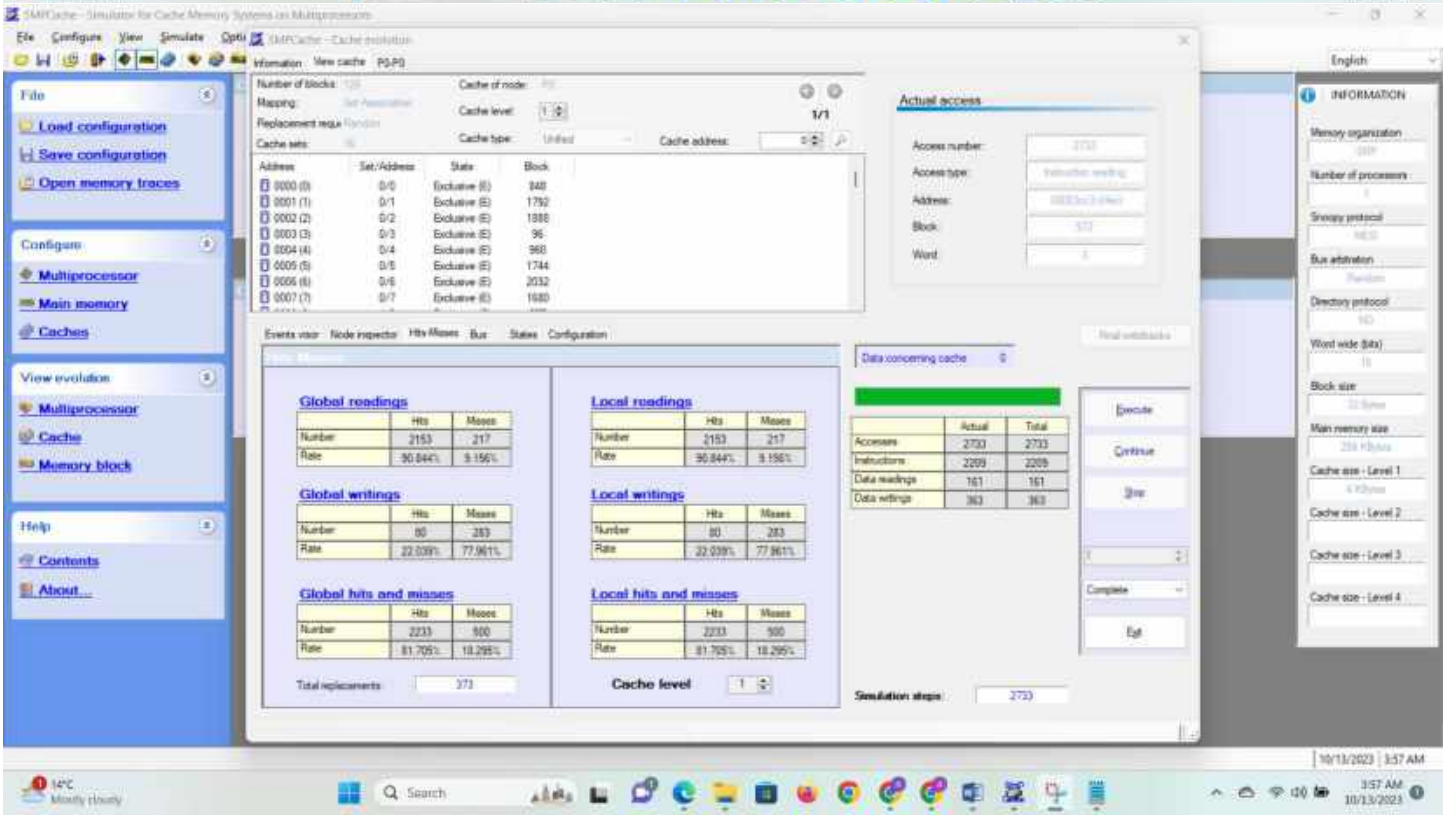
Hits rate %
Misses rate %
Accesses number:
Execute
Continue
Stop
Exit
INFORMATION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About...
Actual access
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Local writings
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Local hits and misses
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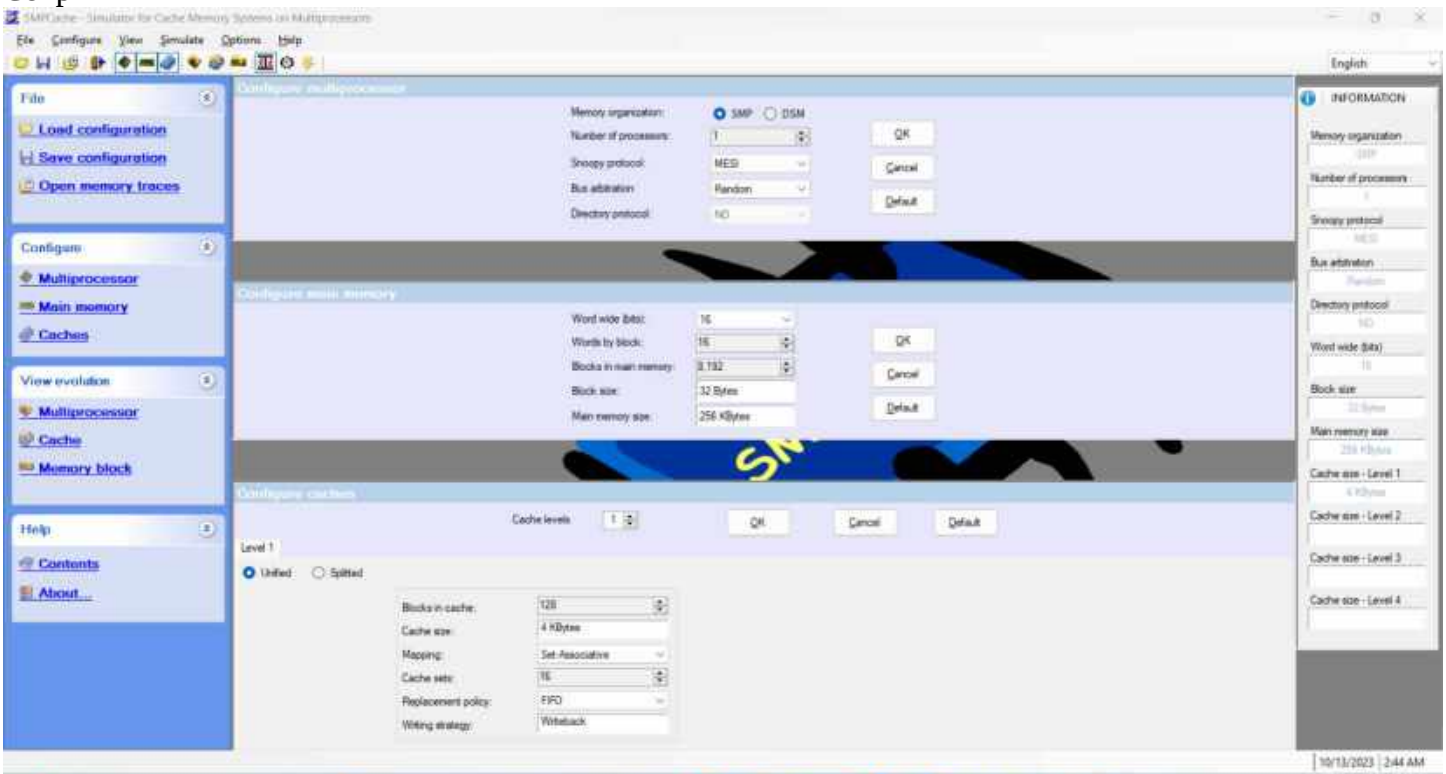
INFORMATION

Cexp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Open memory traces
Configure
Multiprocessor
Main memory
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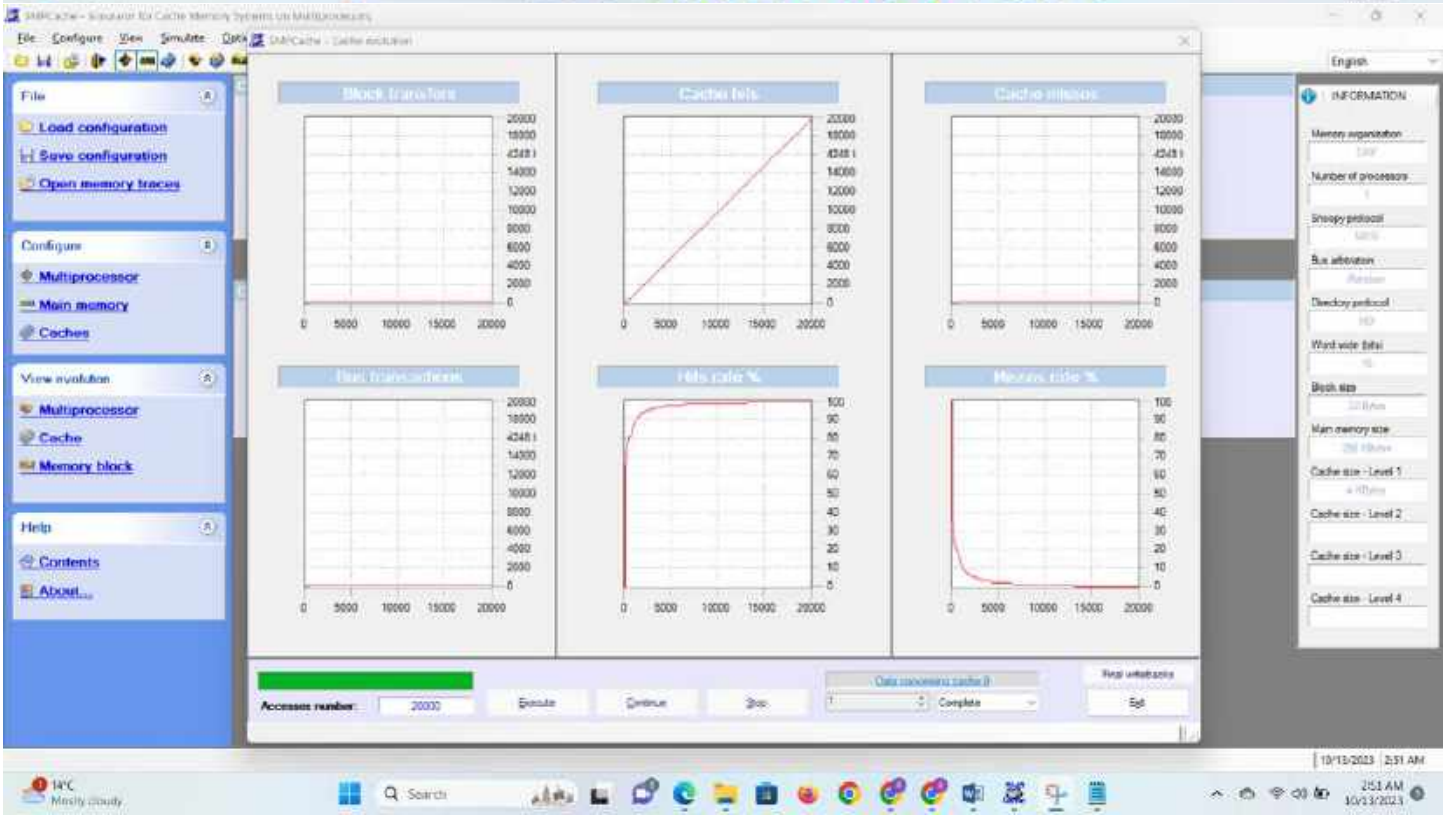
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Memory organization:
SMP
DSM
Number of processors:
Snoopy protocol:
MESI
Bus arbitration:
Random
Directory protocol:
OK
Cancel
Default
Word wide (bits):
Words by block:
Blocks in main memory:
Block size:
32 Bytes
Main memory size:
256 KBytes
Cache levels
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Set-Associative
Cache sets:
16
Replacement policy:
FIFO
Writing strategy:
Writeback
INFORMATION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Multiprocessor
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View evolution
Multiprocessor
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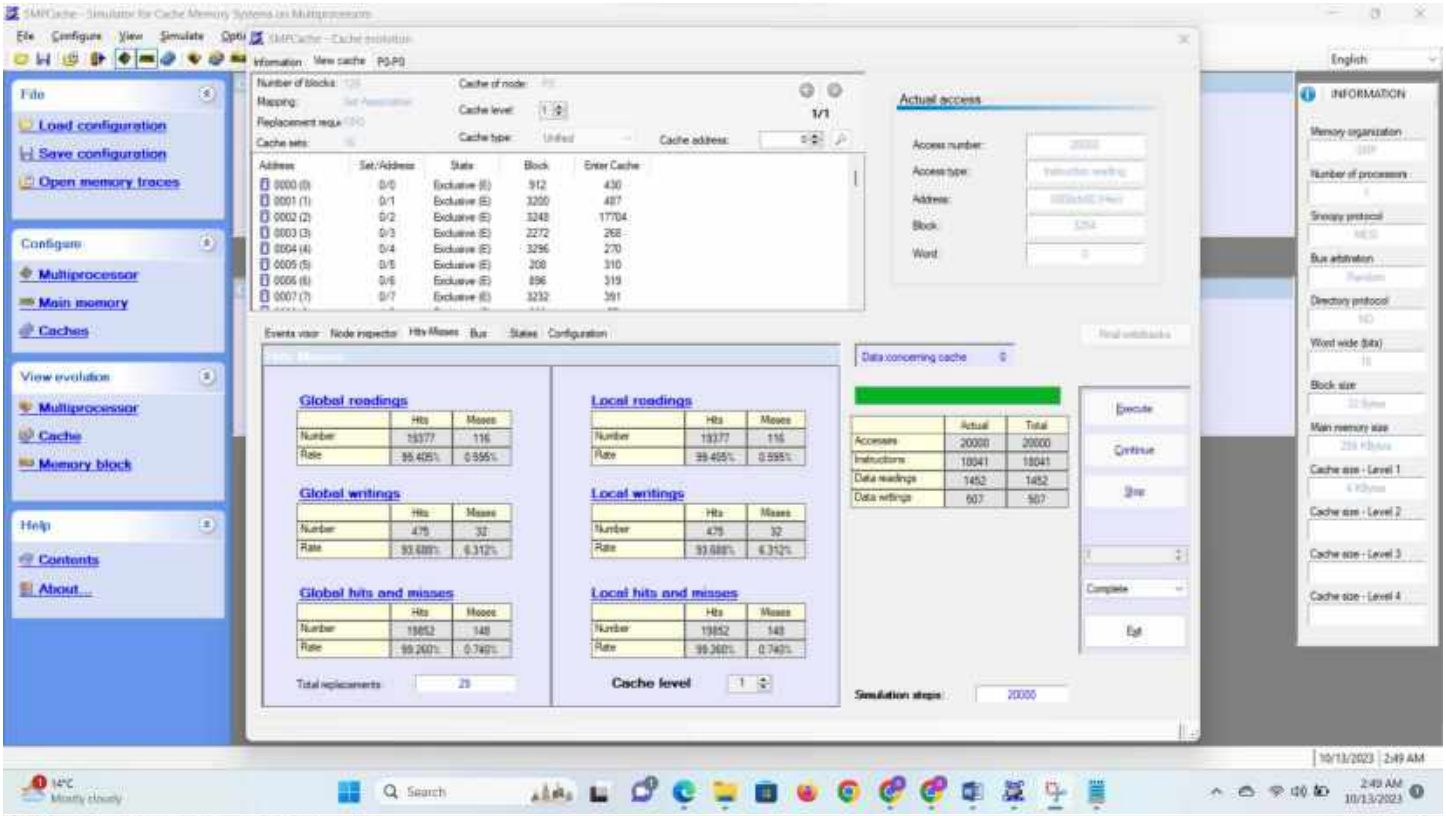
Memory block
Help
Contents
About...
Block transfers
Cache fails
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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Open memory traces
Configure
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Actual access
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Local readings
Global writings
Local writings
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Local hits and misses
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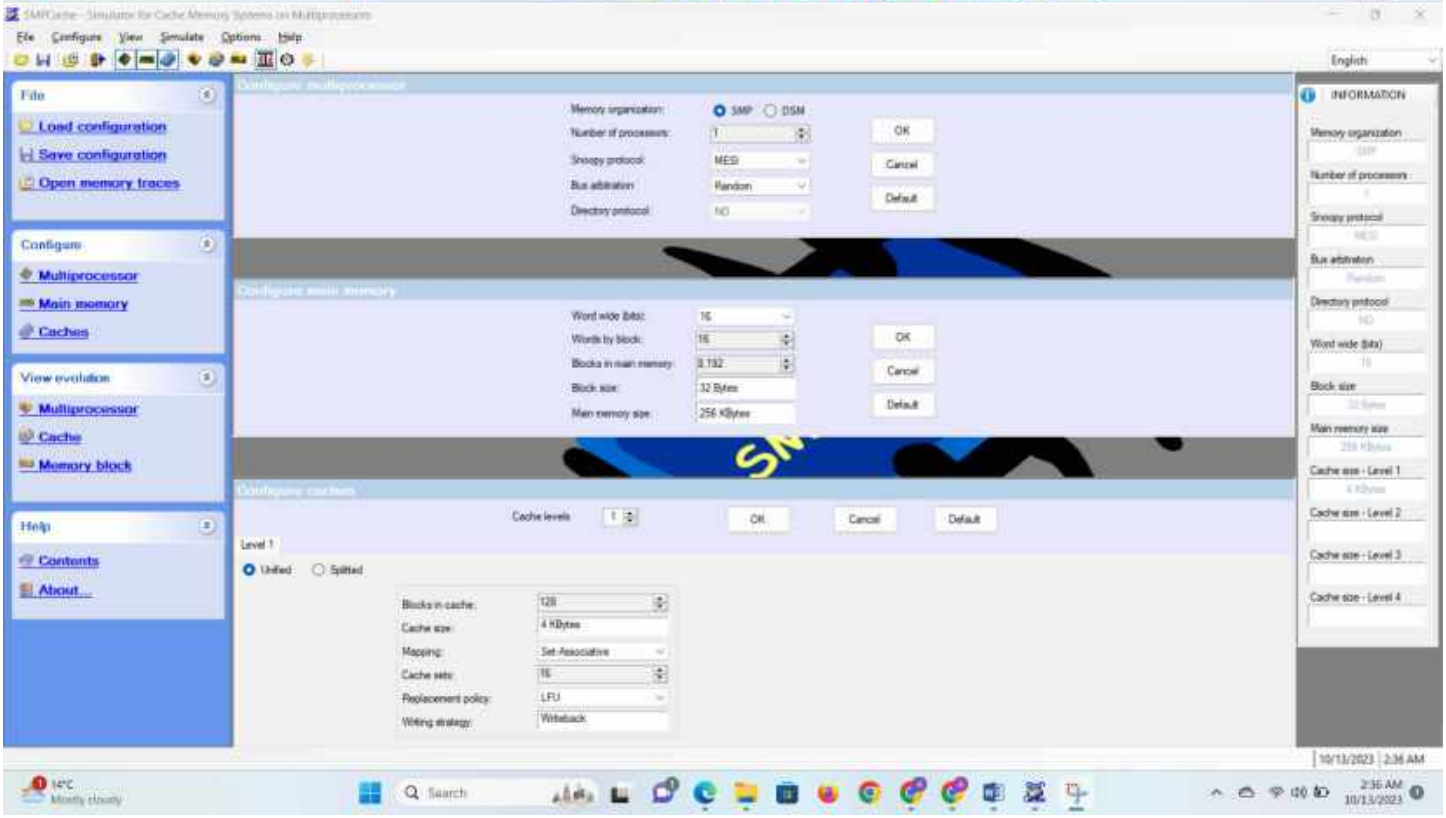
Execute
Continue
Stop
Exit
INFORMATION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Main memory
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Multiprocessor
Cache
Memory block
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Memory organization
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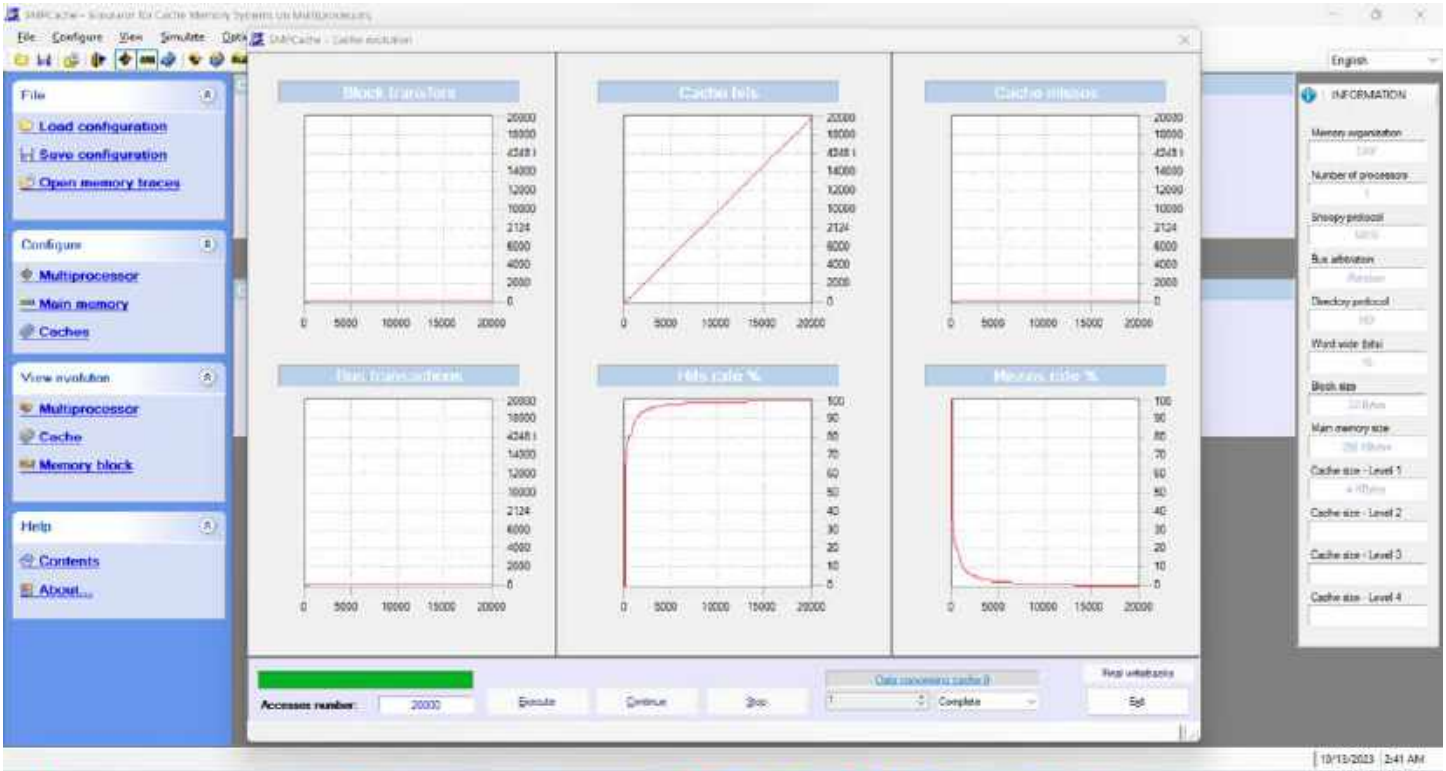
Level 1
Unified
Splitted
Blocks in cache
128
Cache size
4 KBytes
Mapping
Set-Associative
Cache sets
16
Replacement policy
LFU
Writing strategy
Writeback
INFORMATION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Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
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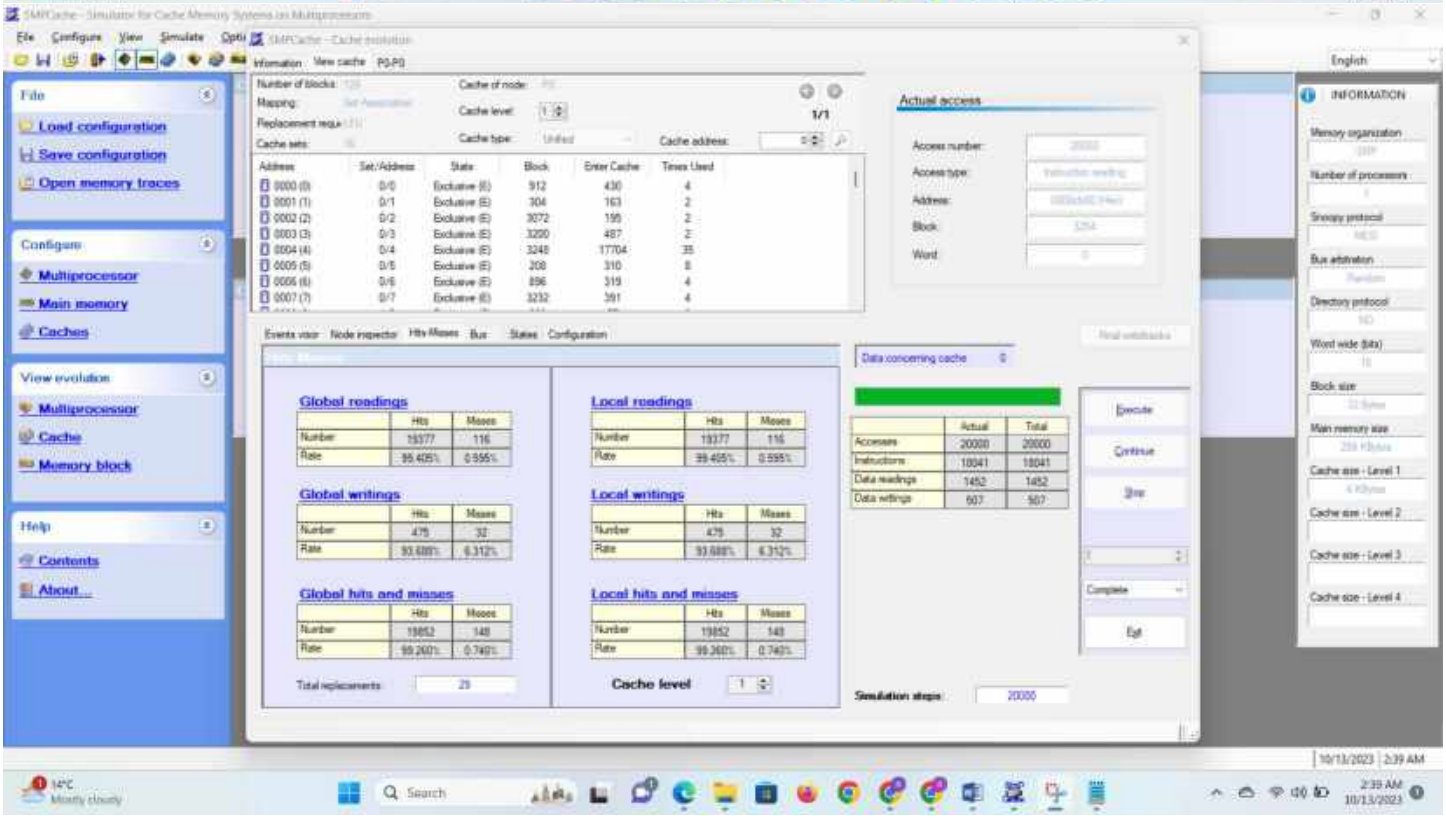
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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Open memory traces
Configure
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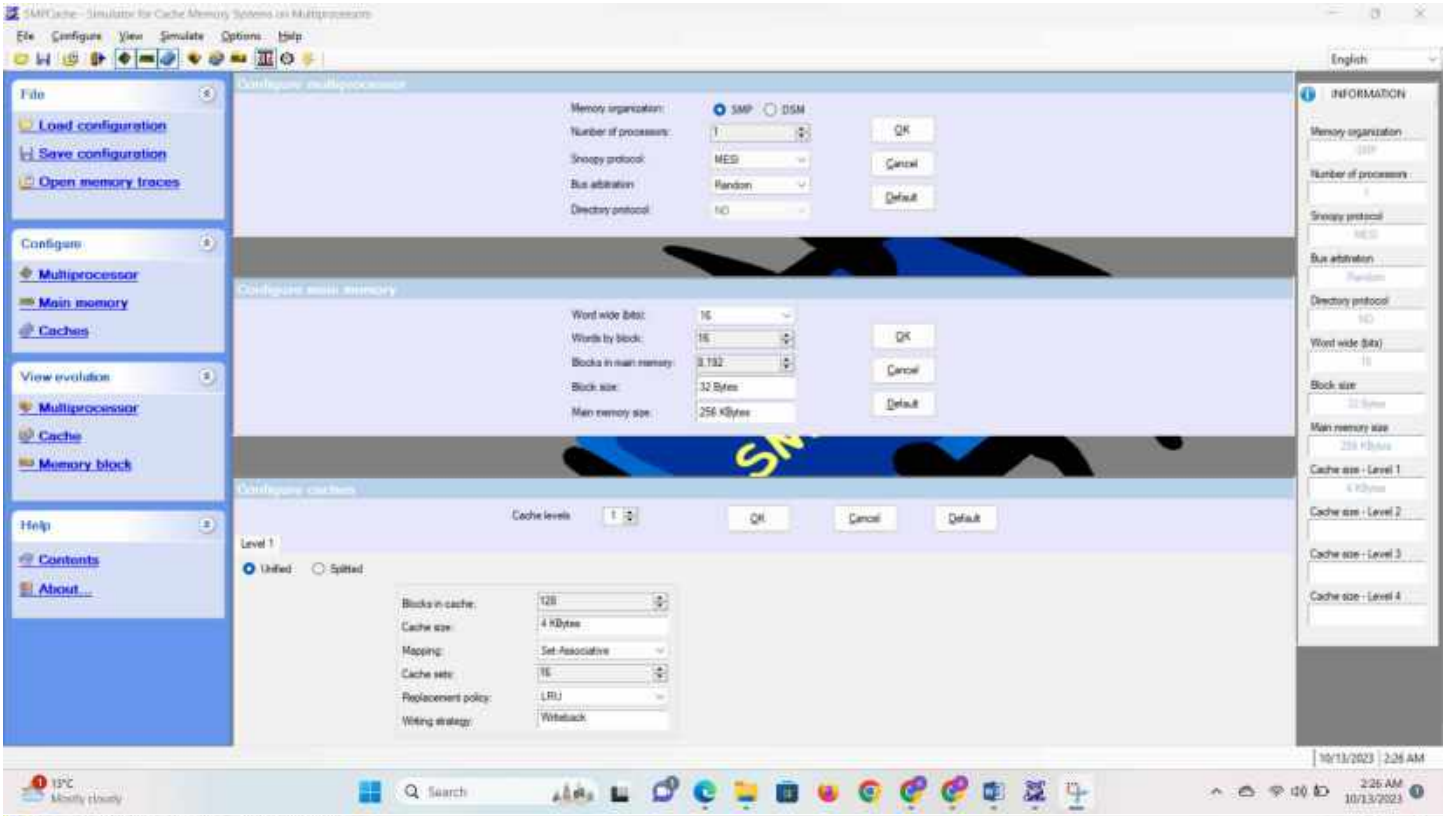
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION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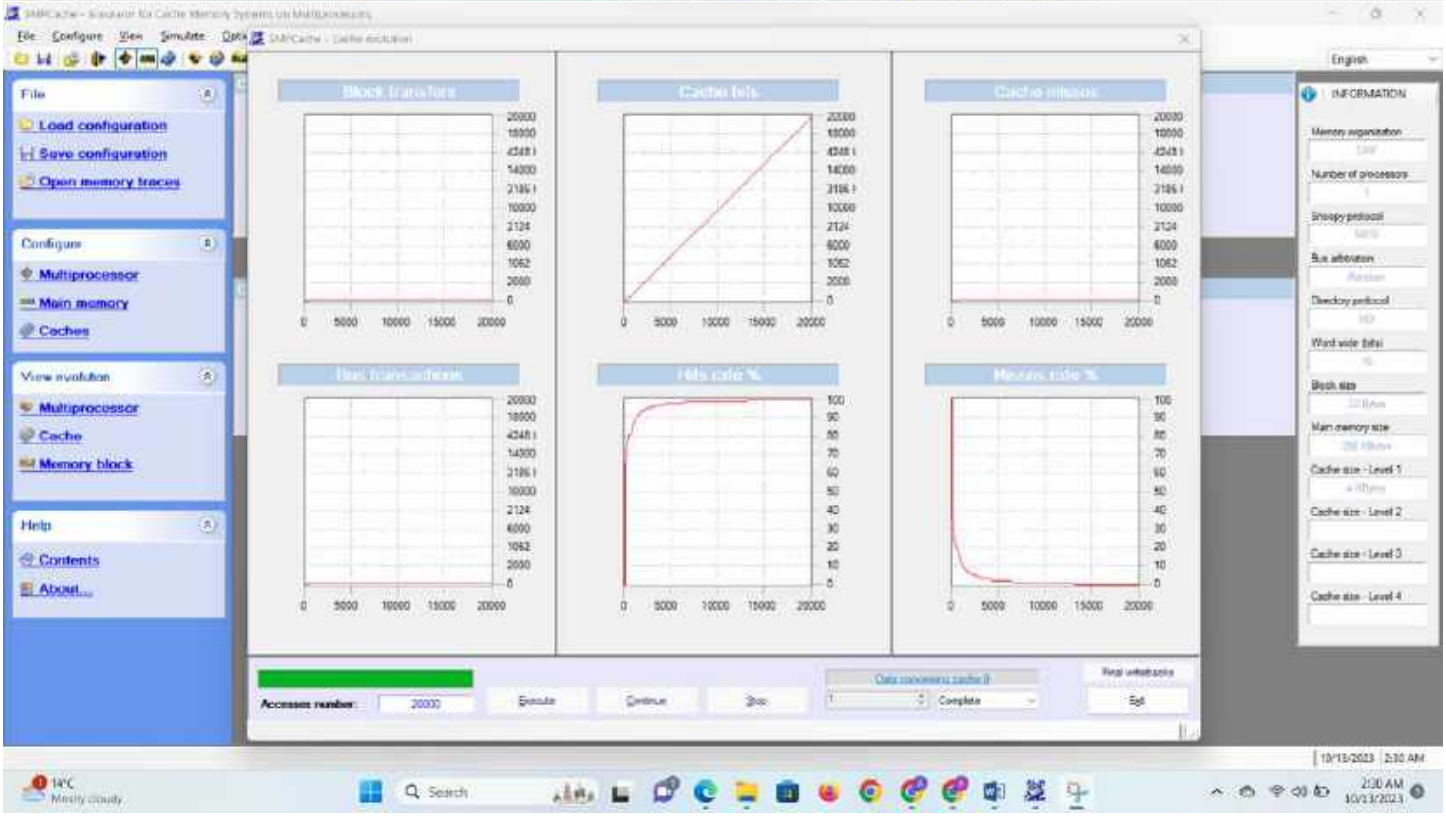
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Memory organization:
SMP
DSM
Number of processors:
Snoopy protocol:
MESI
Bus arbitration:
Random
Directory protocol:
NO
OK
Cancel
Default
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8.192
Block size:
32 Bytes
Main memory size:
256 KBytes
Cache levels
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Set-Associative
Cache sets:
16
Replacement policy:
LRU
Writing strategy:
Writeback
INFORMATION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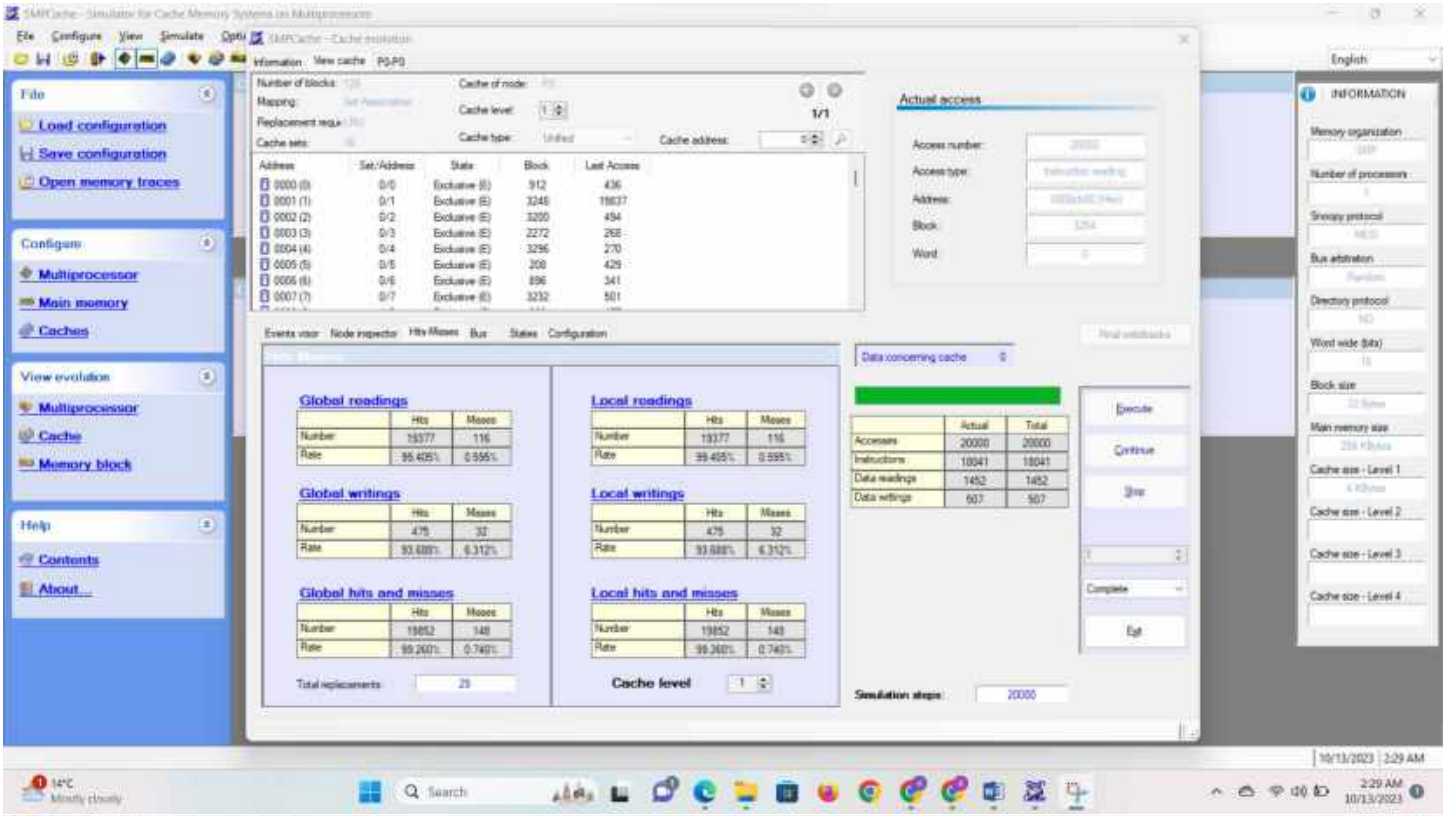
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache fails
Cache misses
Data transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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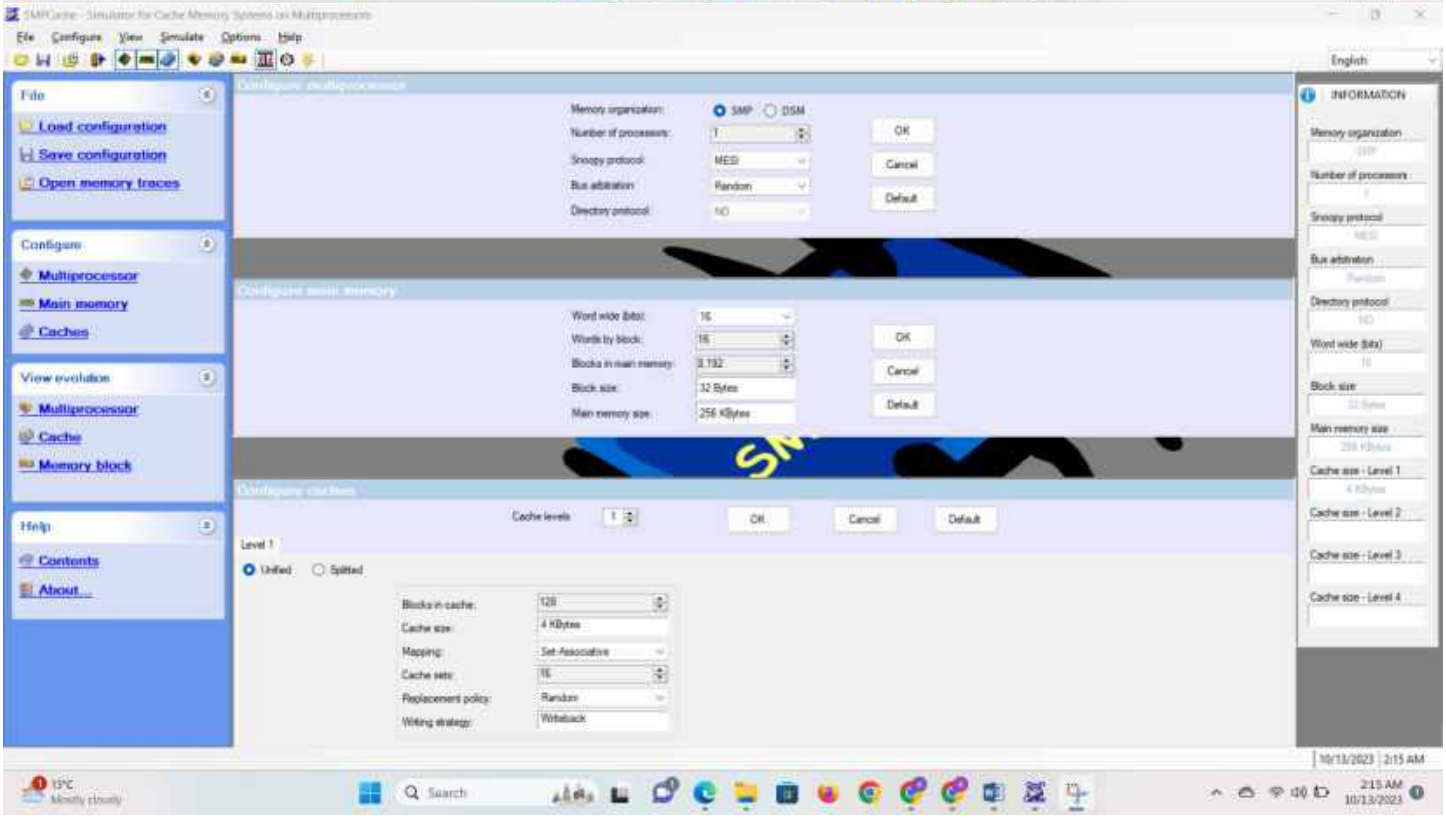
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION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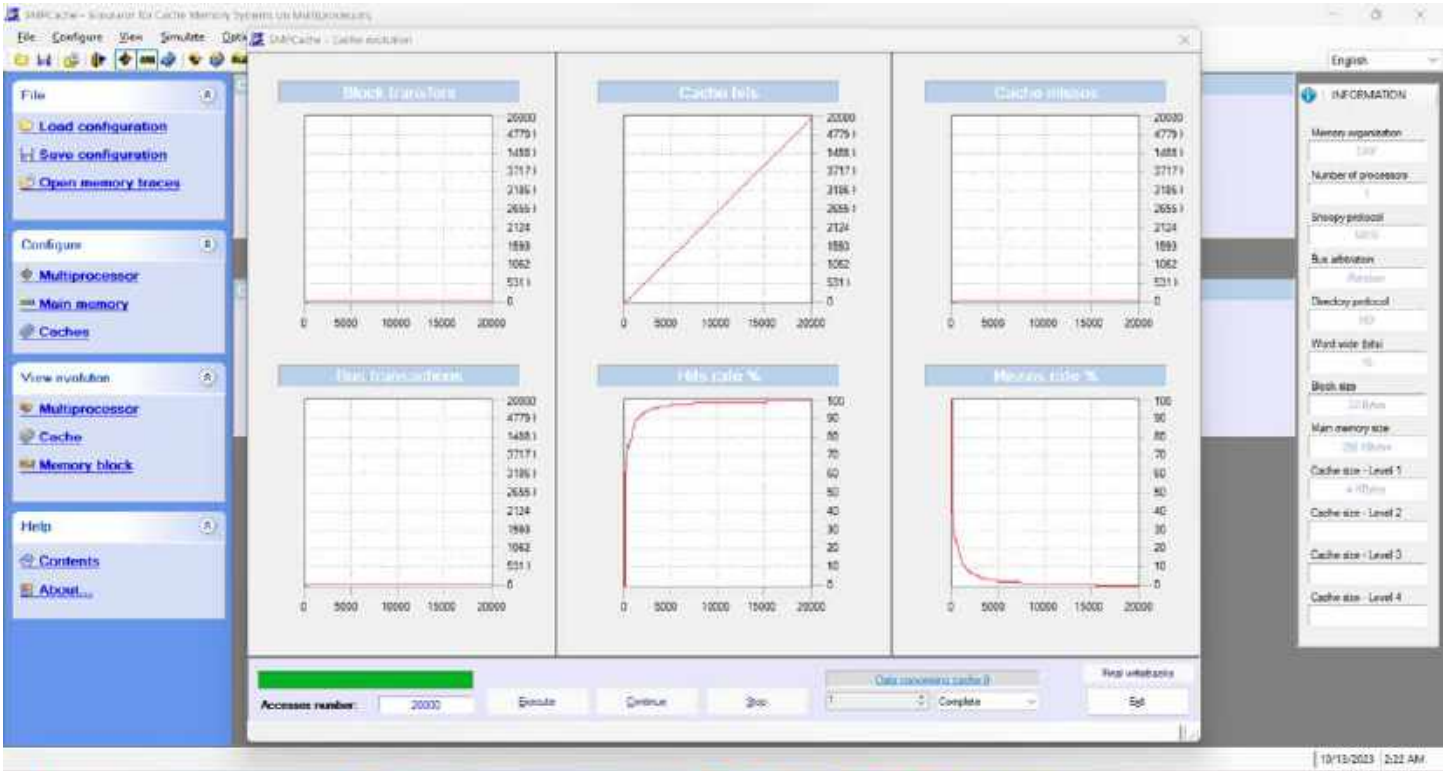
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Memory organization
SMP
DSM
Number of processors
Snoopy protocol
MESI
Bus arbitration
Random
Directory protocol
OK
Cancel
Default
Word wide (bits)
Words by block
Blocks in main memory
Block size
32 Bytes
Main memory size
256 KBytes
Cache levels
Level 1
Unified
Splitted
Blocks in cache
128
Cache size
4 KBytes
Mapping
Set-Associative
Cache sets
16
Replacement policy
Random
Writing strategy
Writeback
INFORMATION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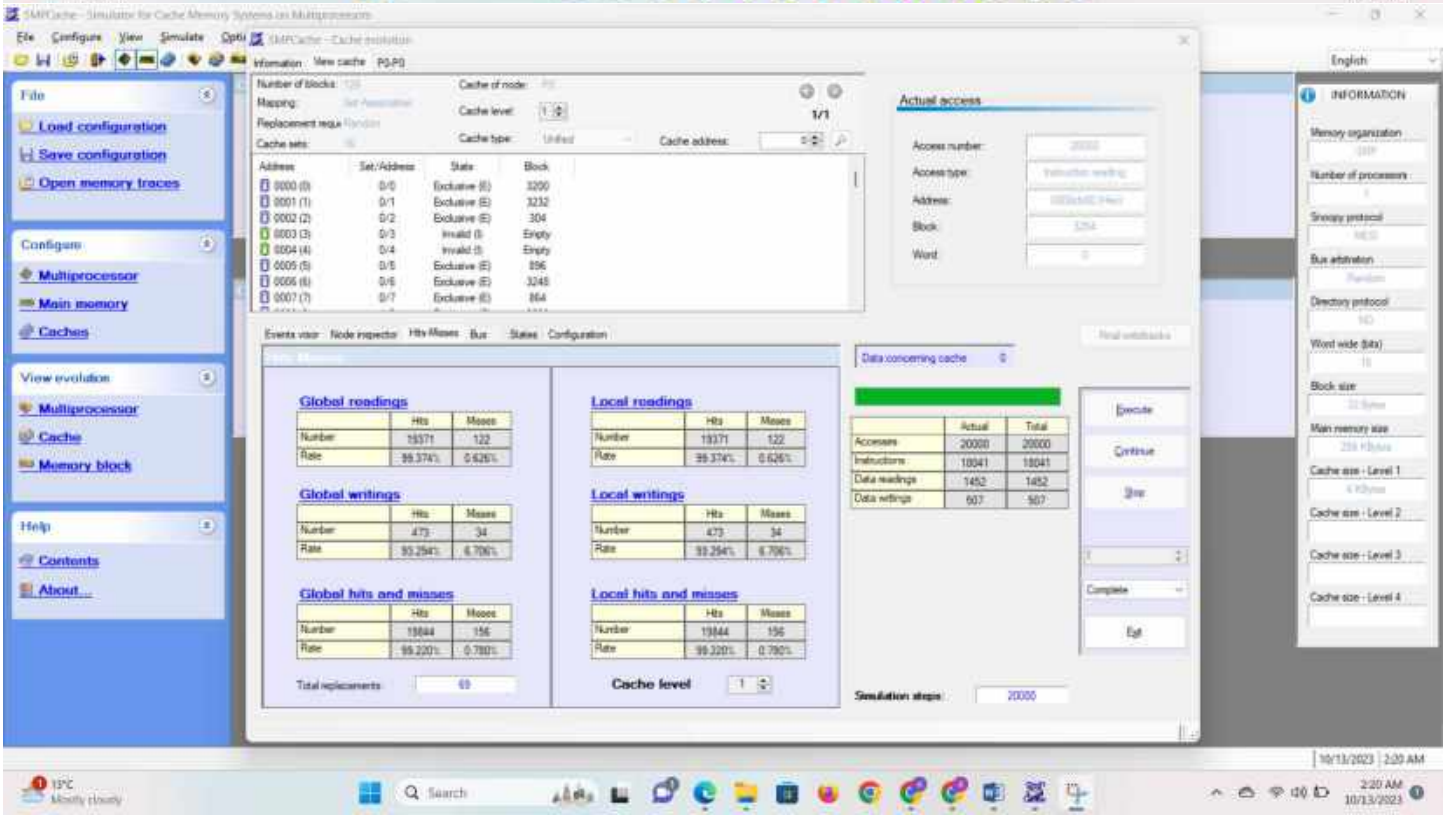
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Exit
INFORMATION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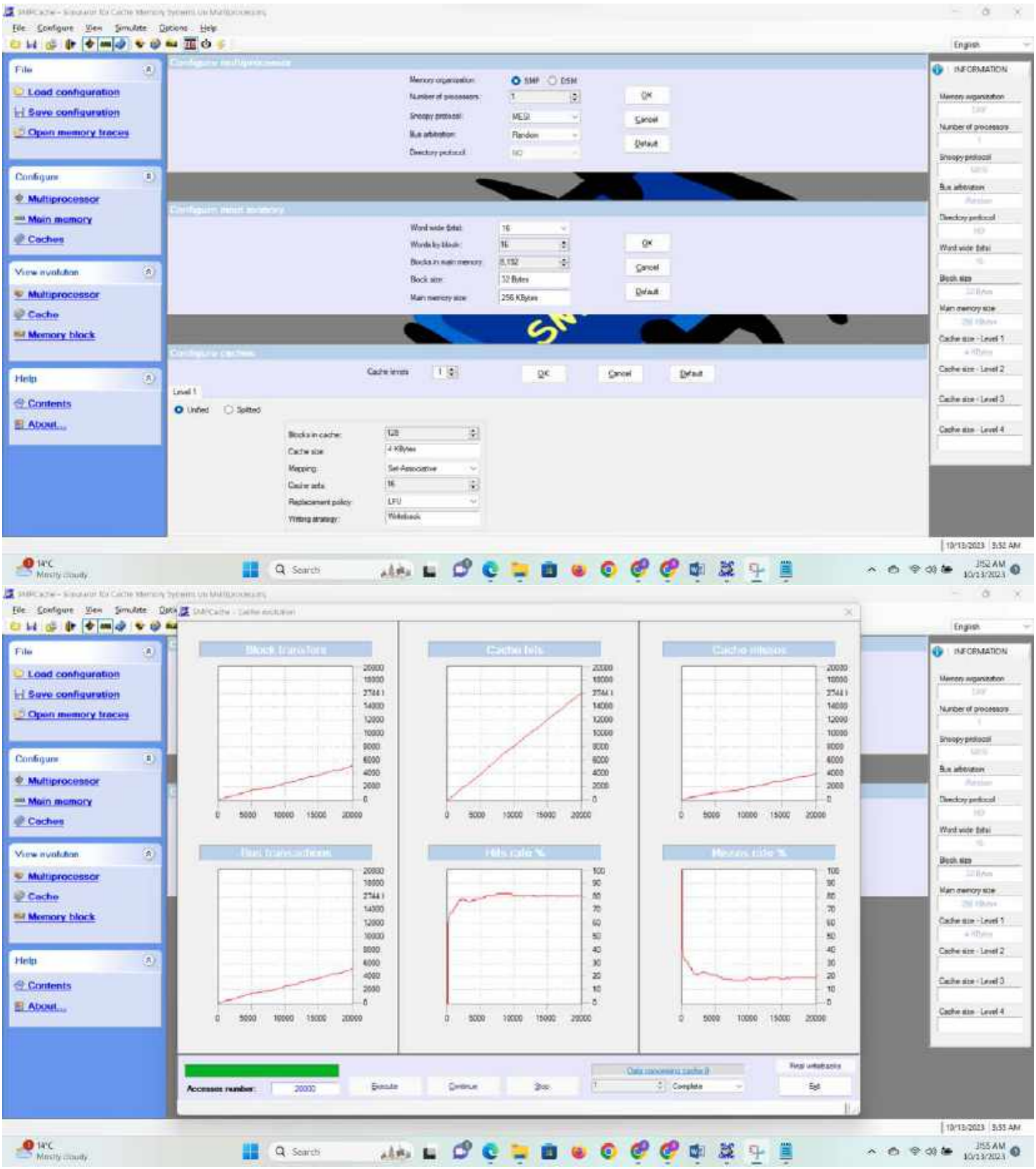
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Access number:
Access type:
Address:
Block:
Word:
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
20000
Execute
Continue
Stop
Exit
INFORMATION

SWM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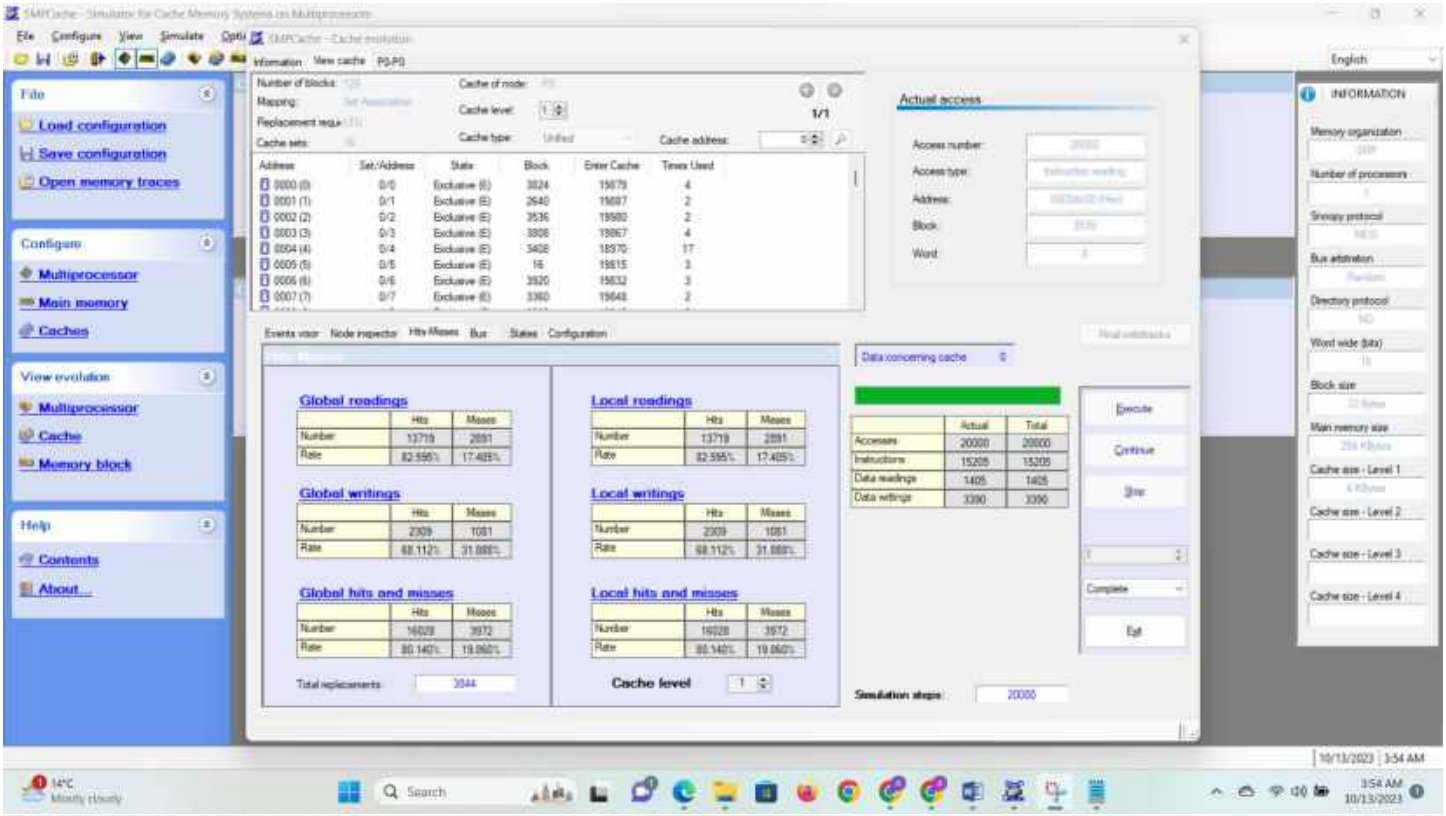
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Block transfers
Cache fails
Cache misses
Bus transactions
Hits cache %
Misses cache %
Accesses number:
Execute
Continue
Stop
Exit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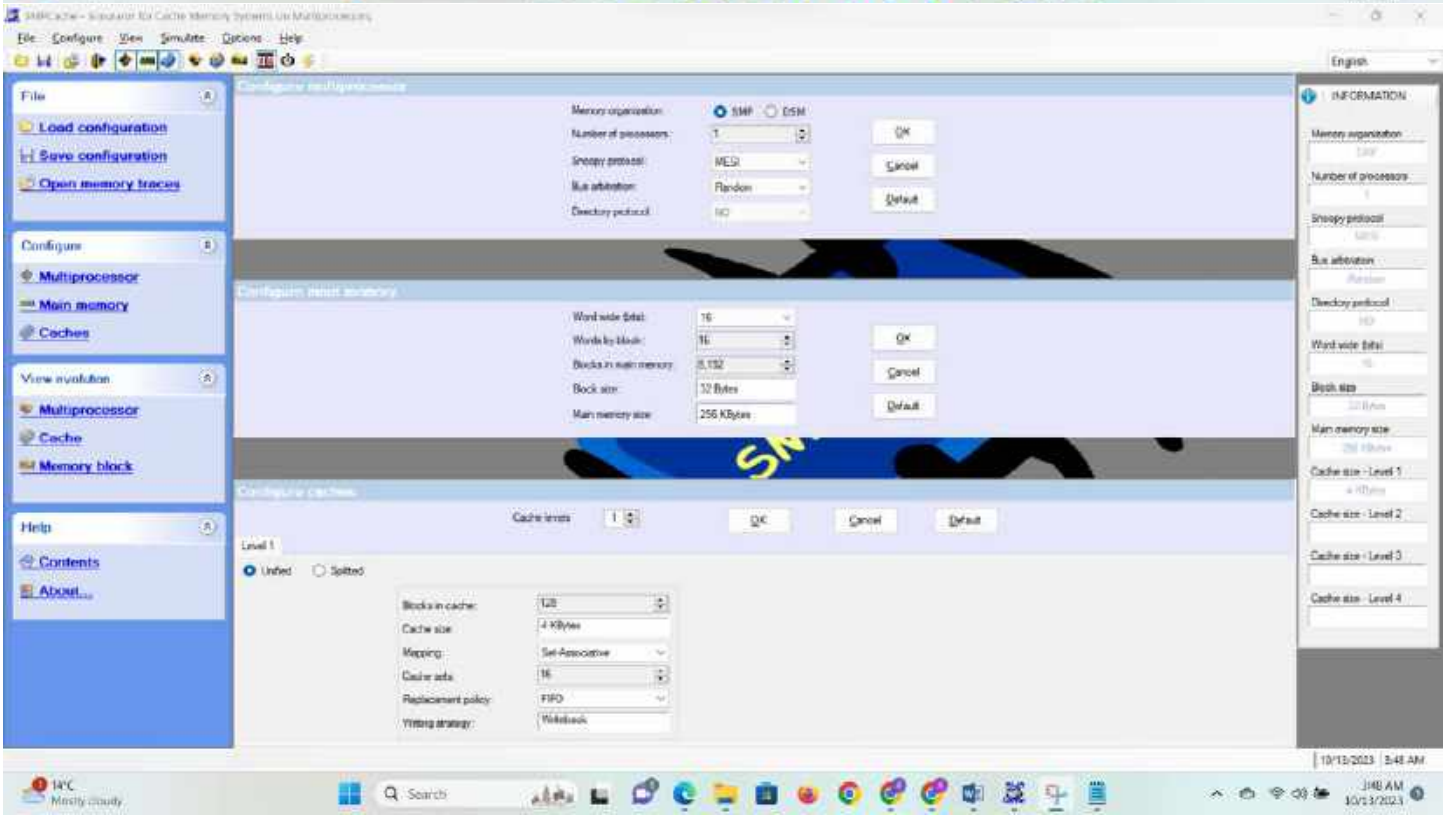
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION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Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
Default
INFORMATION

File
Load configuration
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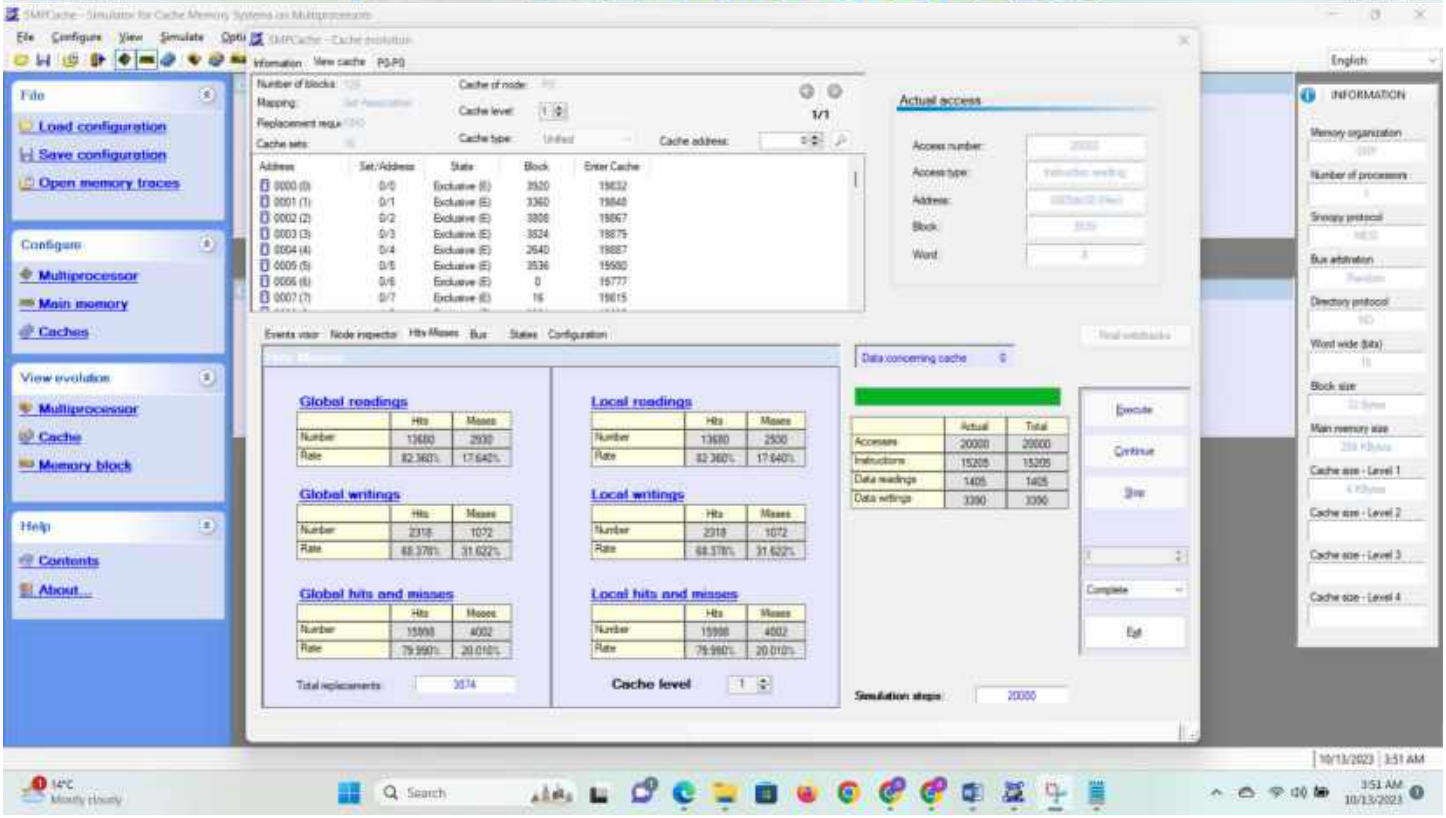
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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Open memory traces
Configure
Multiprocessor
Main memory
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View evolution
Multiprocessor
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Memory block
Help
Contents
About...
Actual access
Access number:
Access type:
Address:
Block:
Word:
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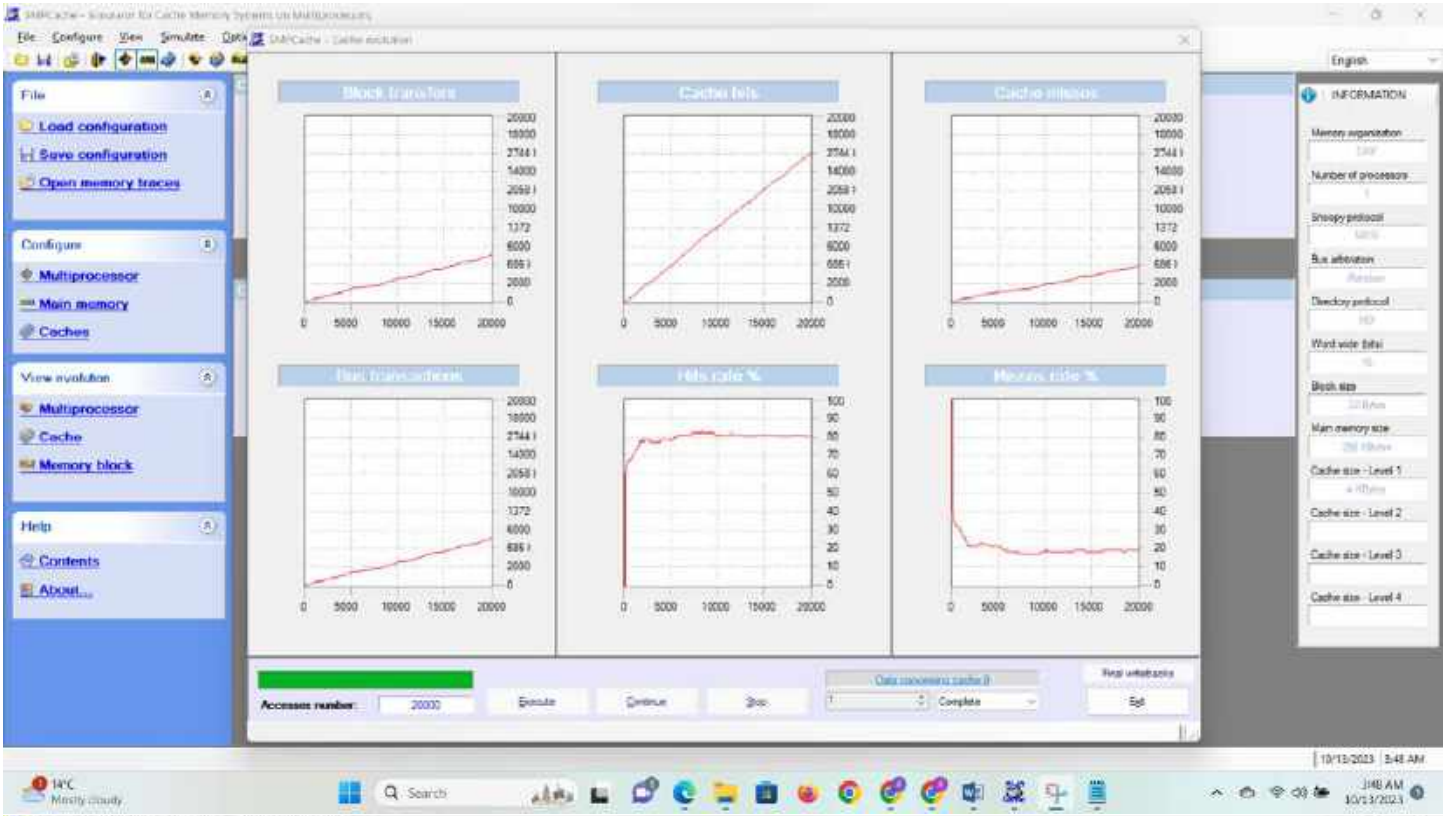
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Total replacements
Cache level
Simulation steps:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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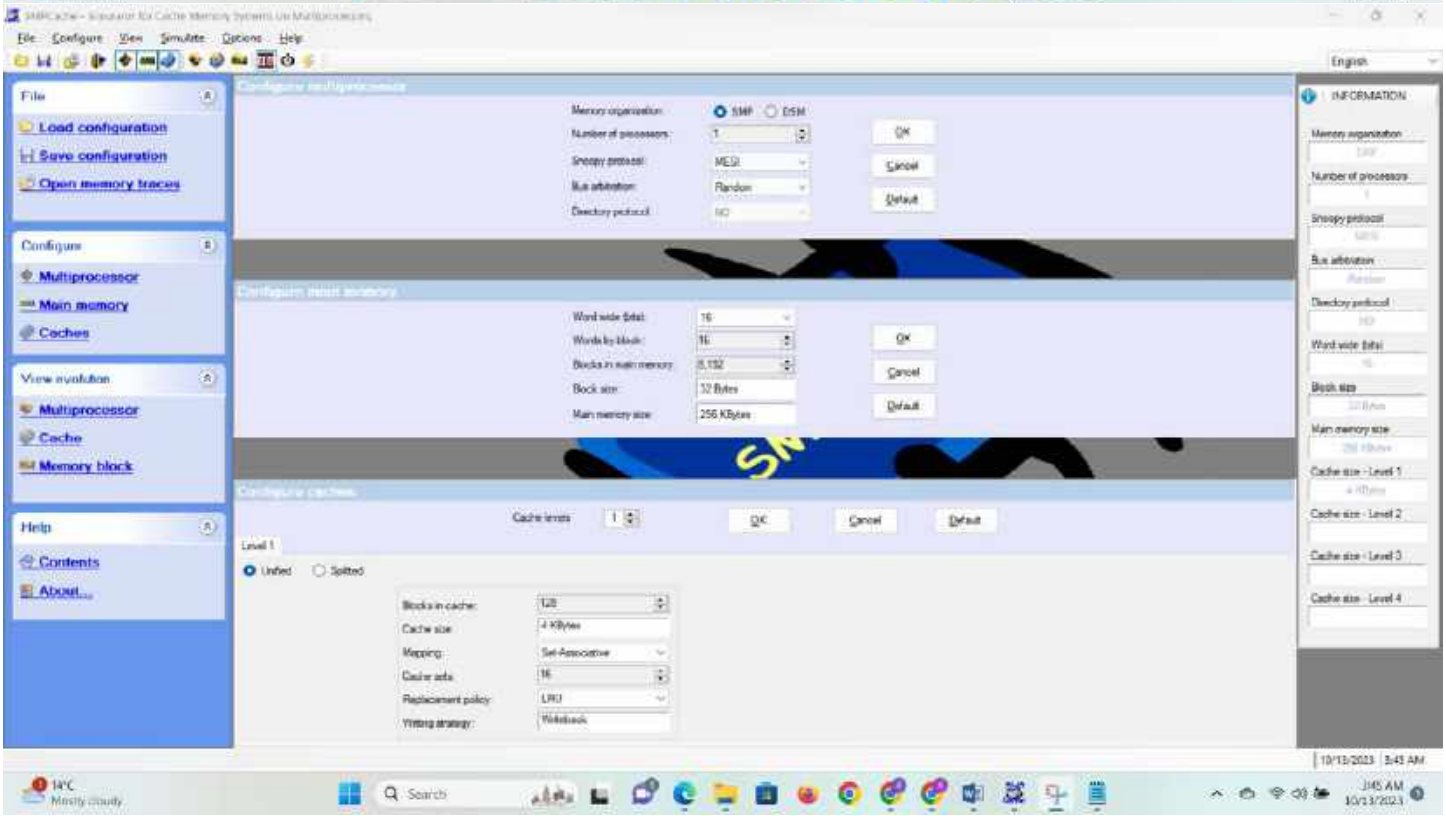
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache fetts
Cache misses
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Exit
INFORMATION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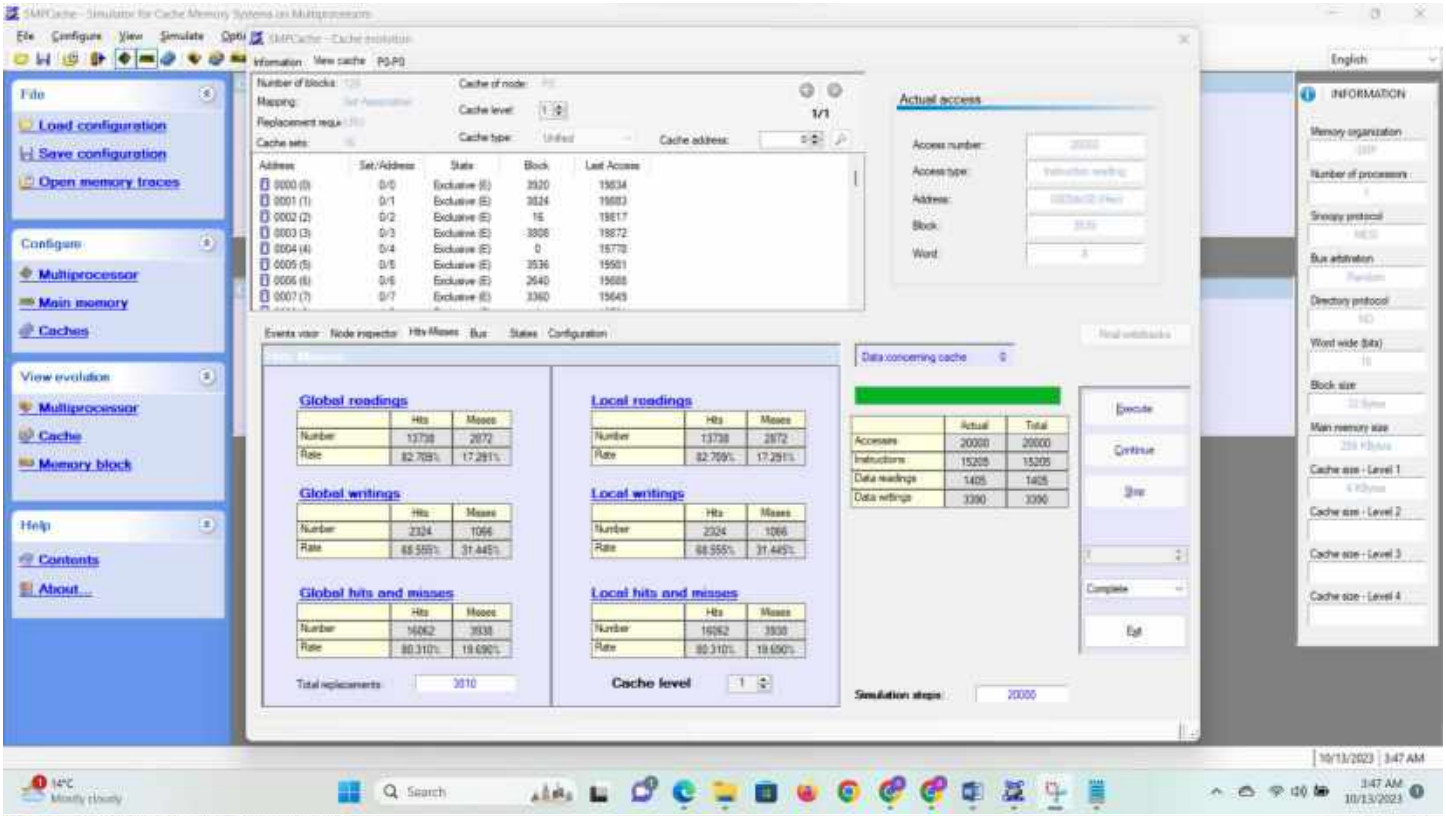
Cache levels
Level 1
Unified
Splitted
Blocks in cache
128
Cache size
4 KBytes
Mapping
Set-Associative
Cache sets
16
Replacement policy
LRU
Writing strategy
Write-back
INFORMATION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Actual access
Global readings
Local readings
Global writings
Local writings
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Local hits and misses
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Continue
Stop
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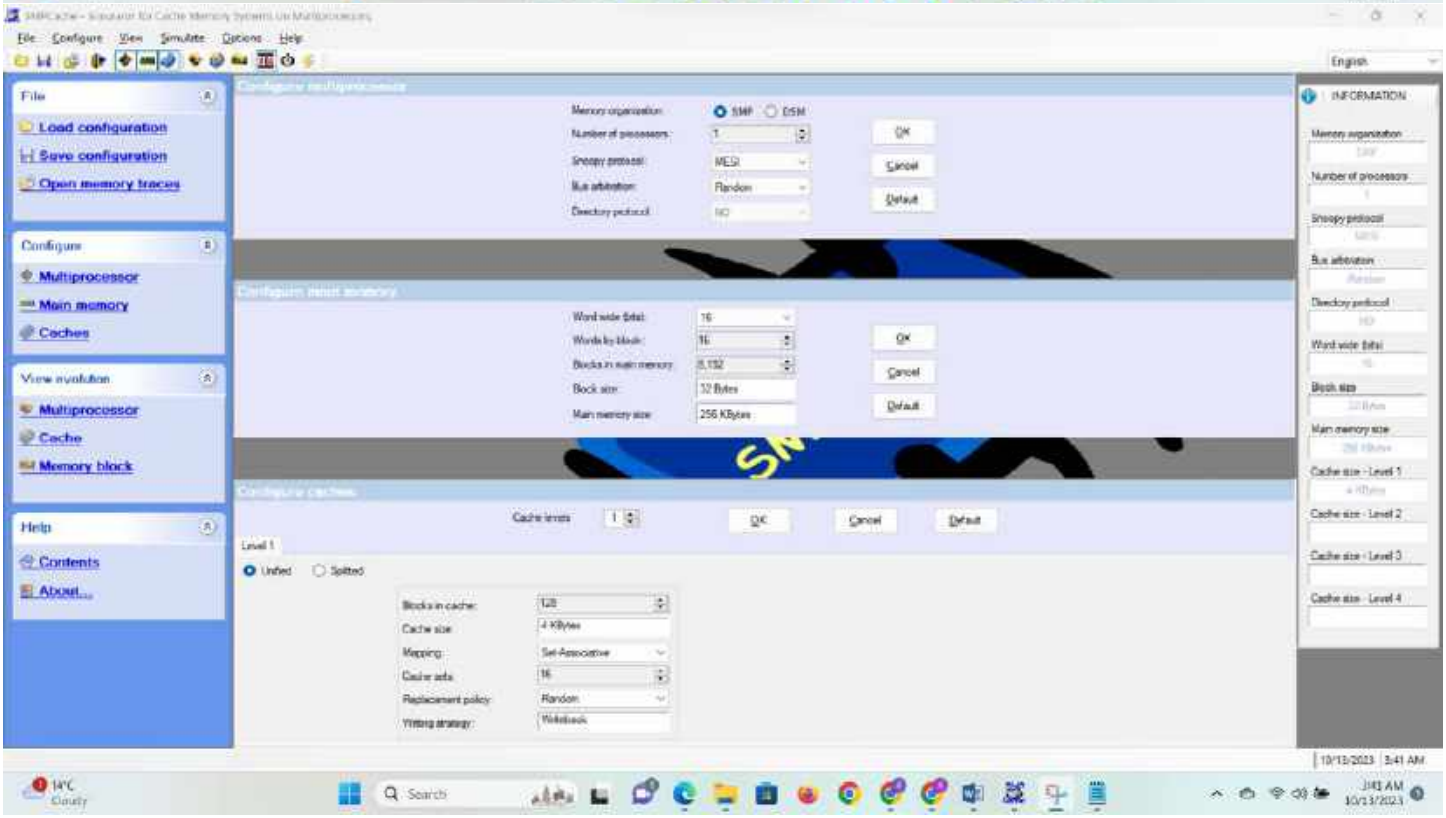
INFORMATION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Help
Contents
About...
OK
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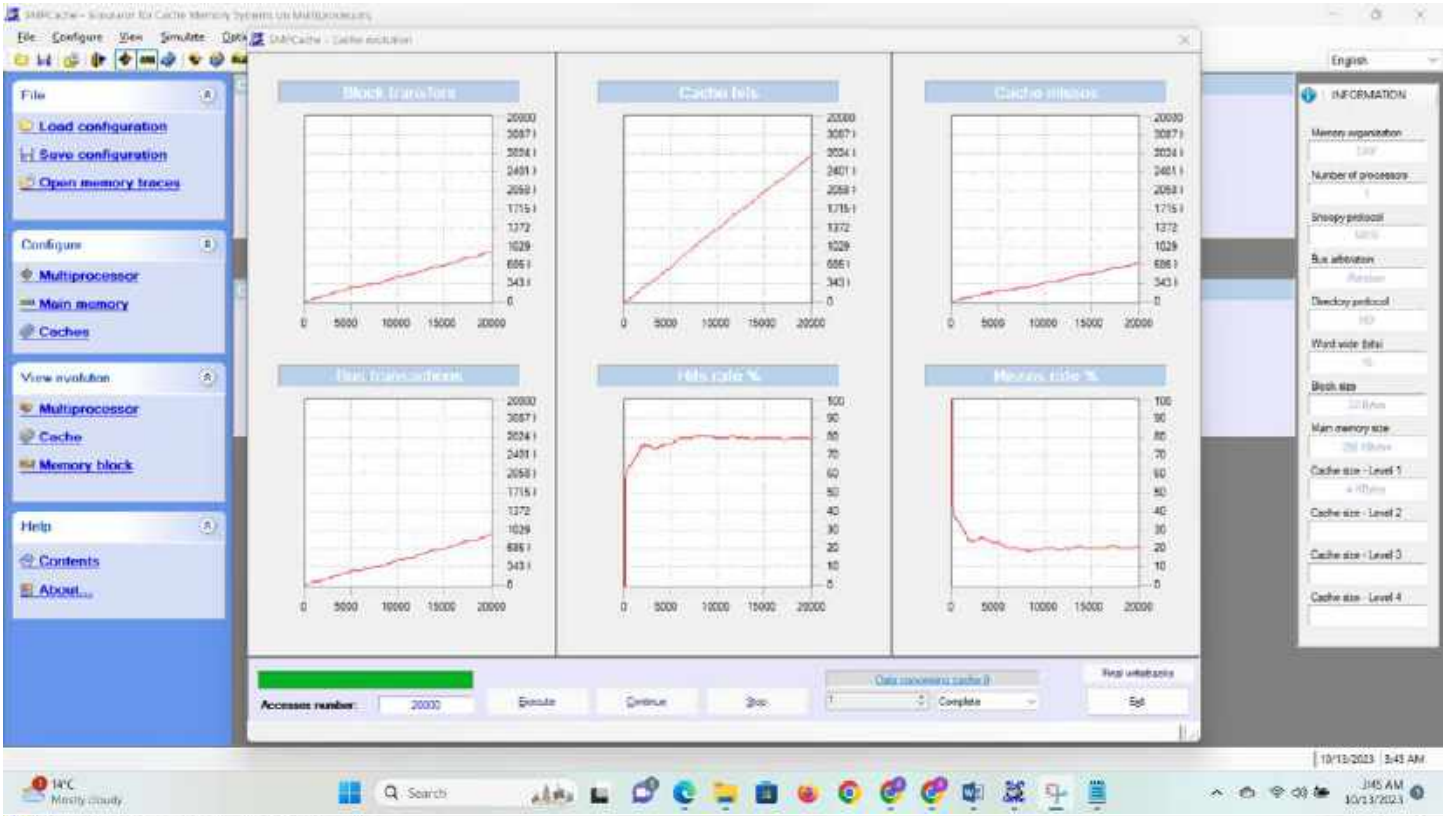
INFORMATION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Multiprocessor
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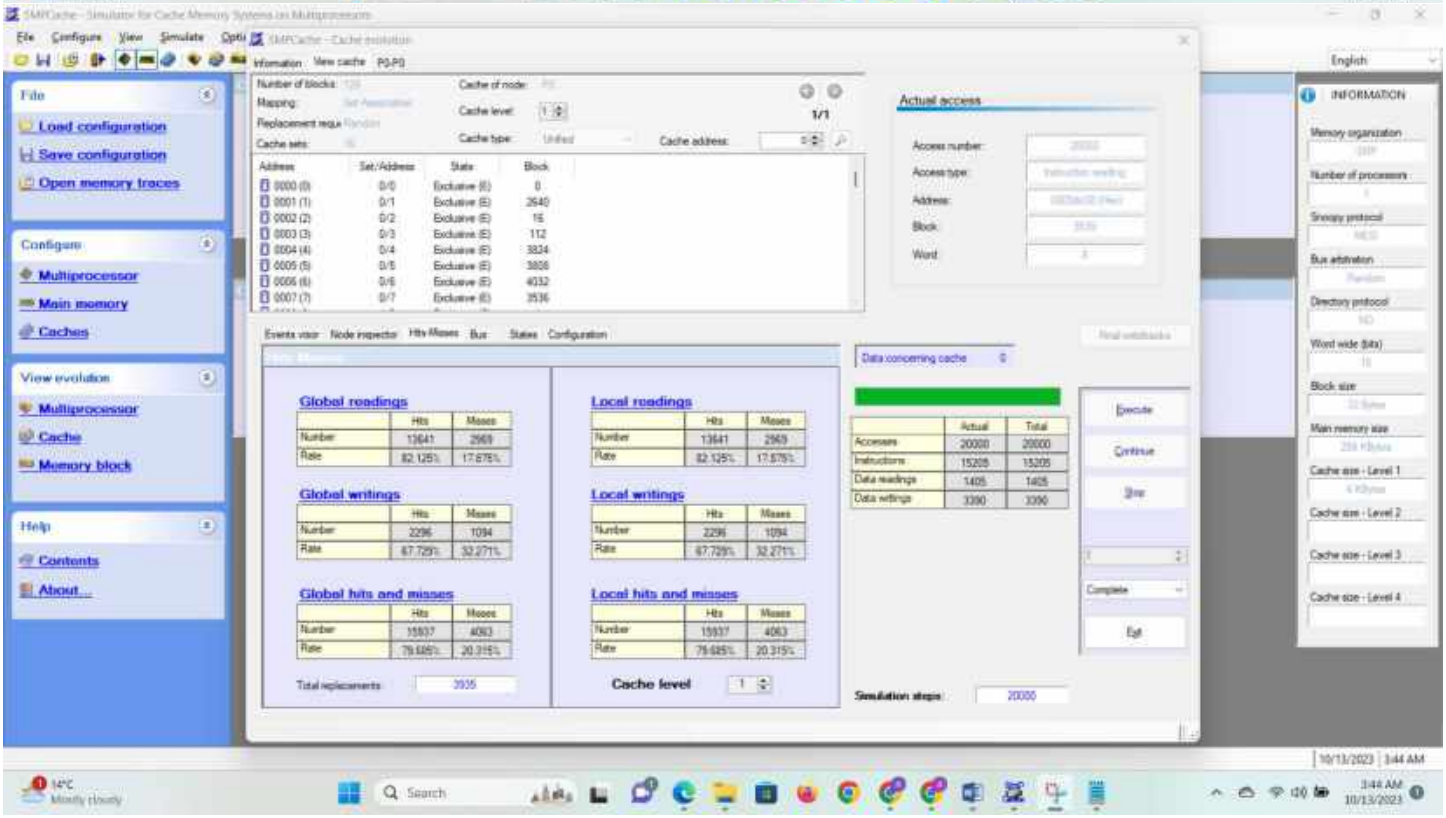
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
20000
Execute
Continue
Stop
Complete
Exit
INFORMATION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Multiprocessor
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About...
Actual access
Access number:
Access type:
Address:
Block:
Word:
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Local readings
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Local writings
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Local hits and misses
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Execute
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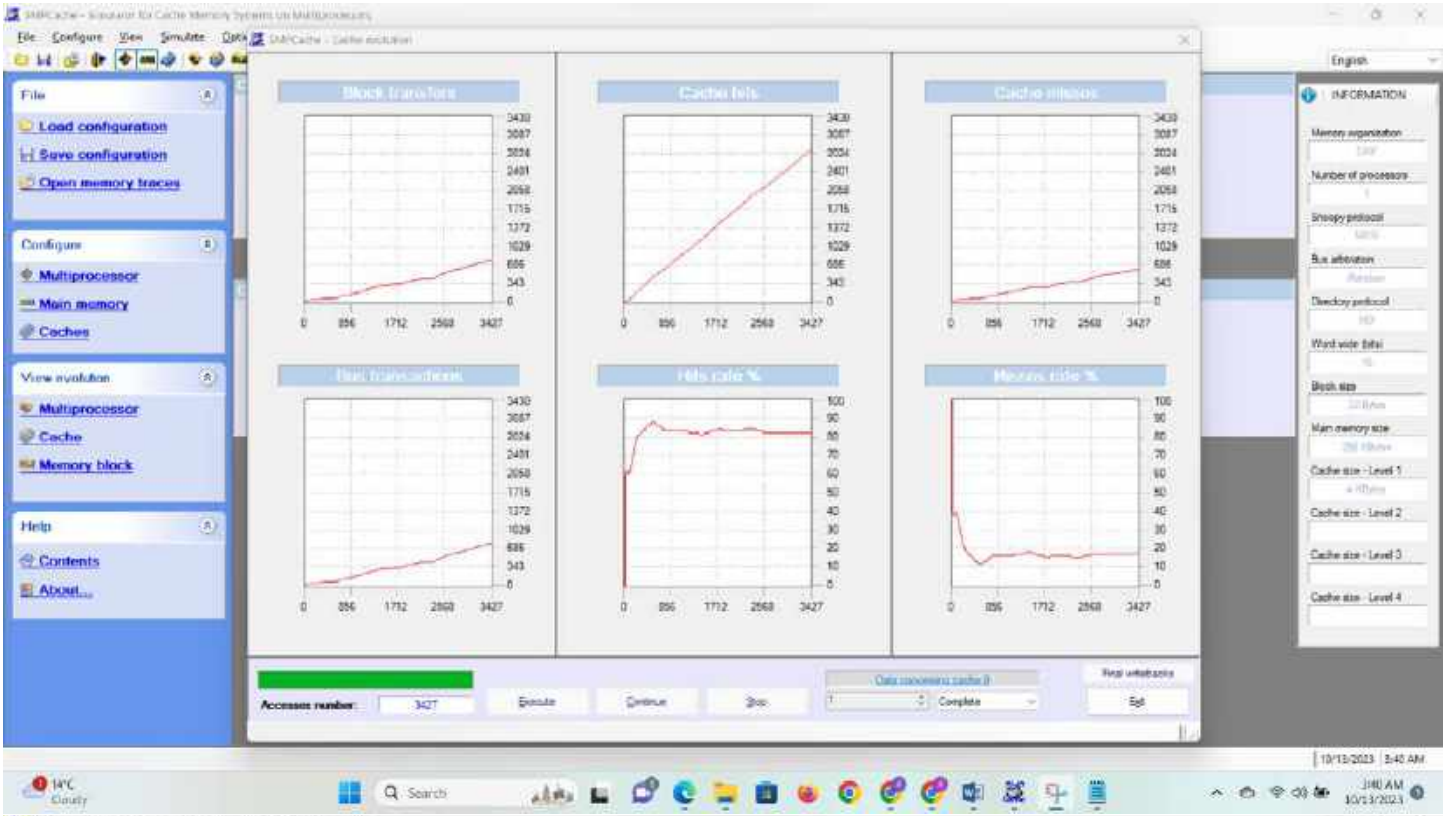
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Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
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Execute
Continue
Stop
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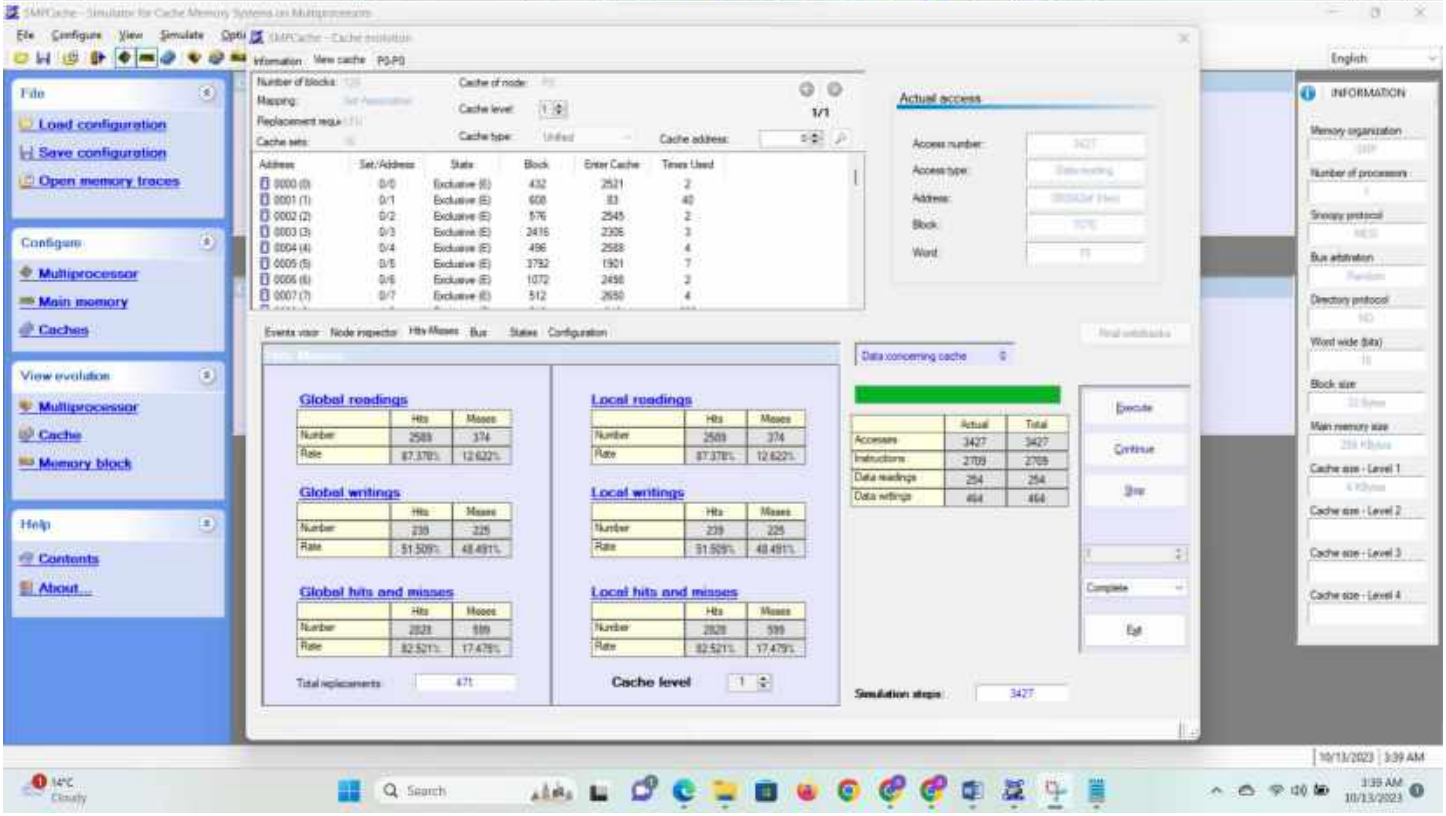
INFORMATION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Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
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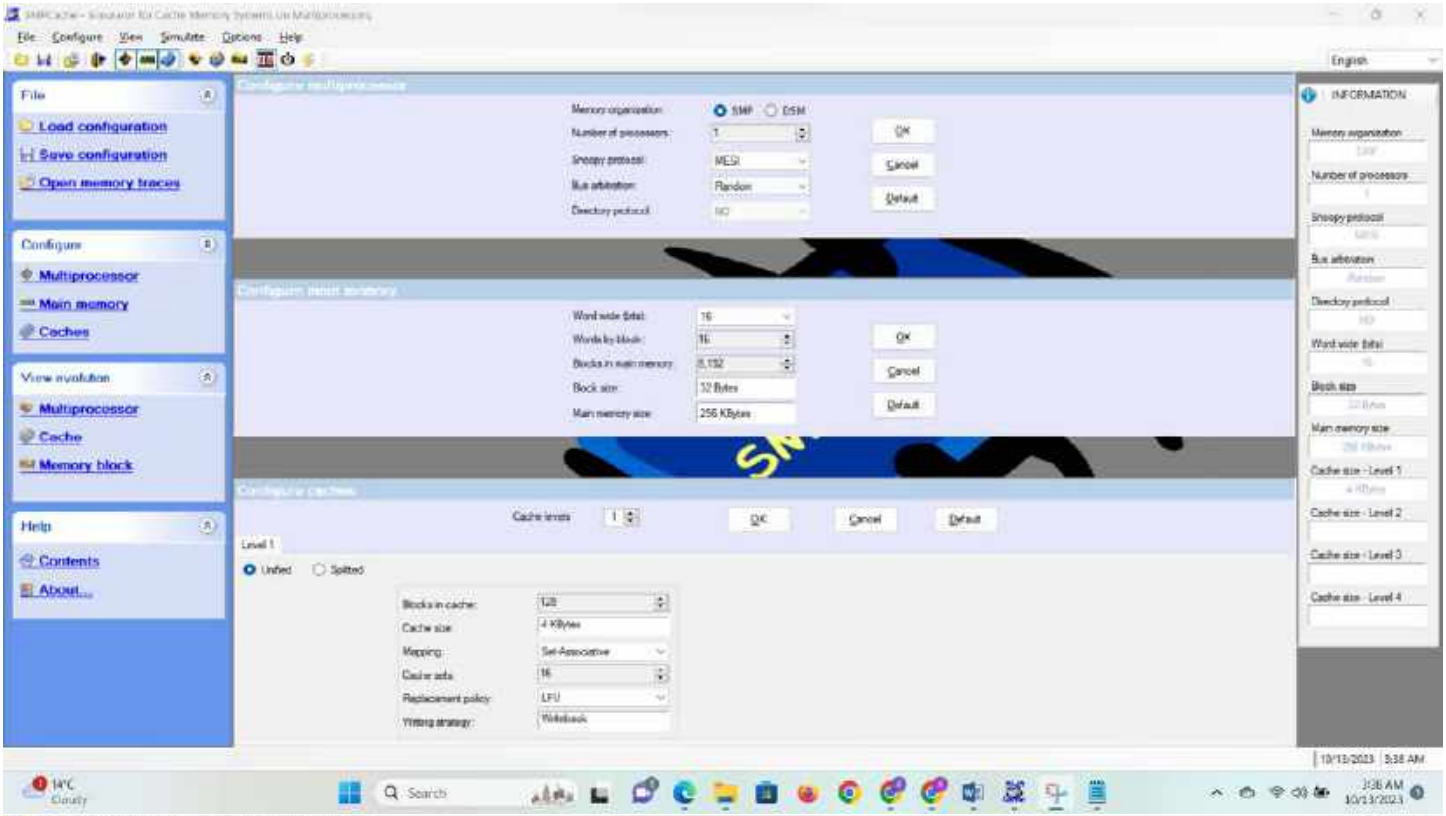
Continue
Stop
Exit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About...
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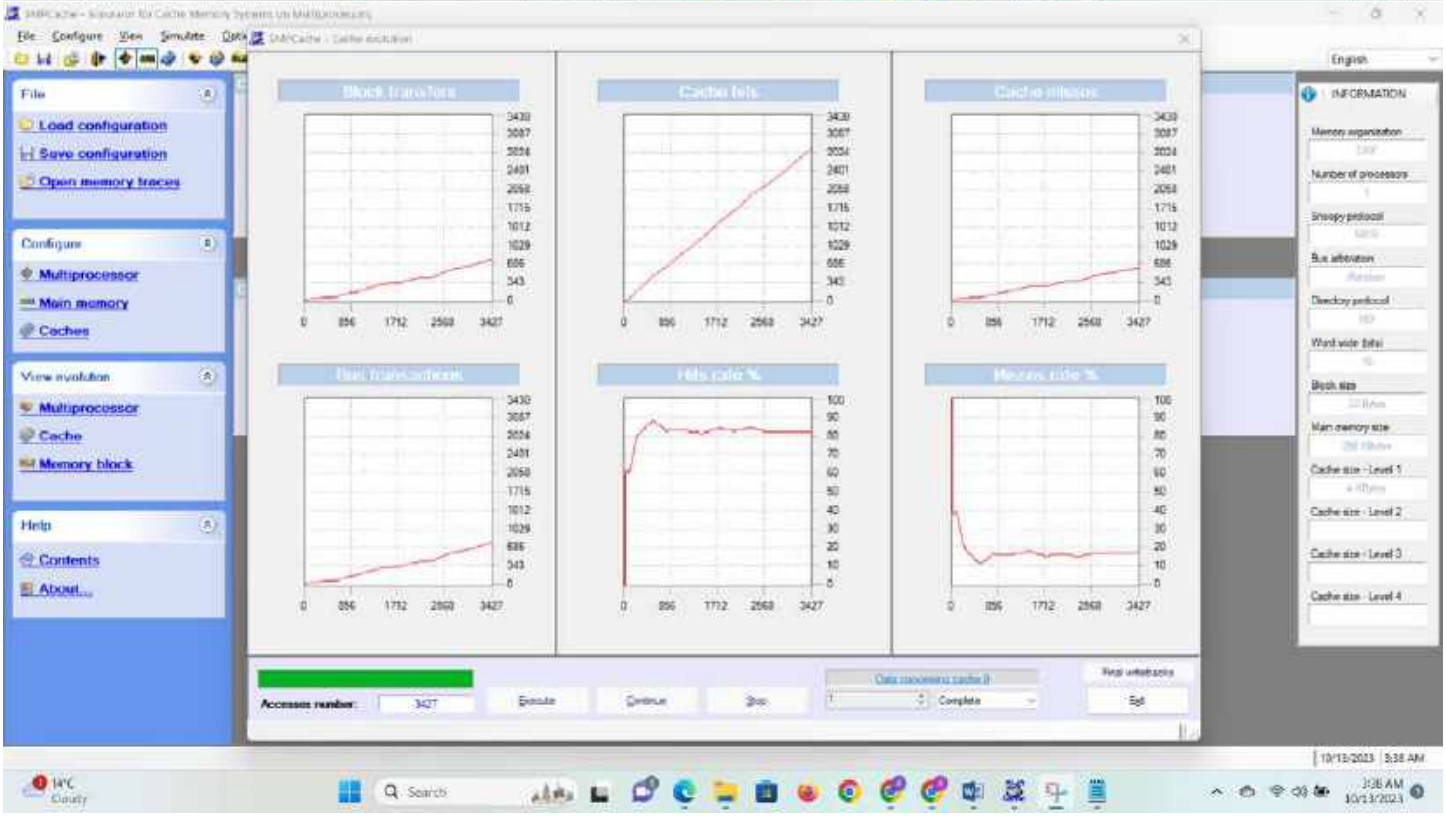
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Open memory traces
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About...
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Accesses number:
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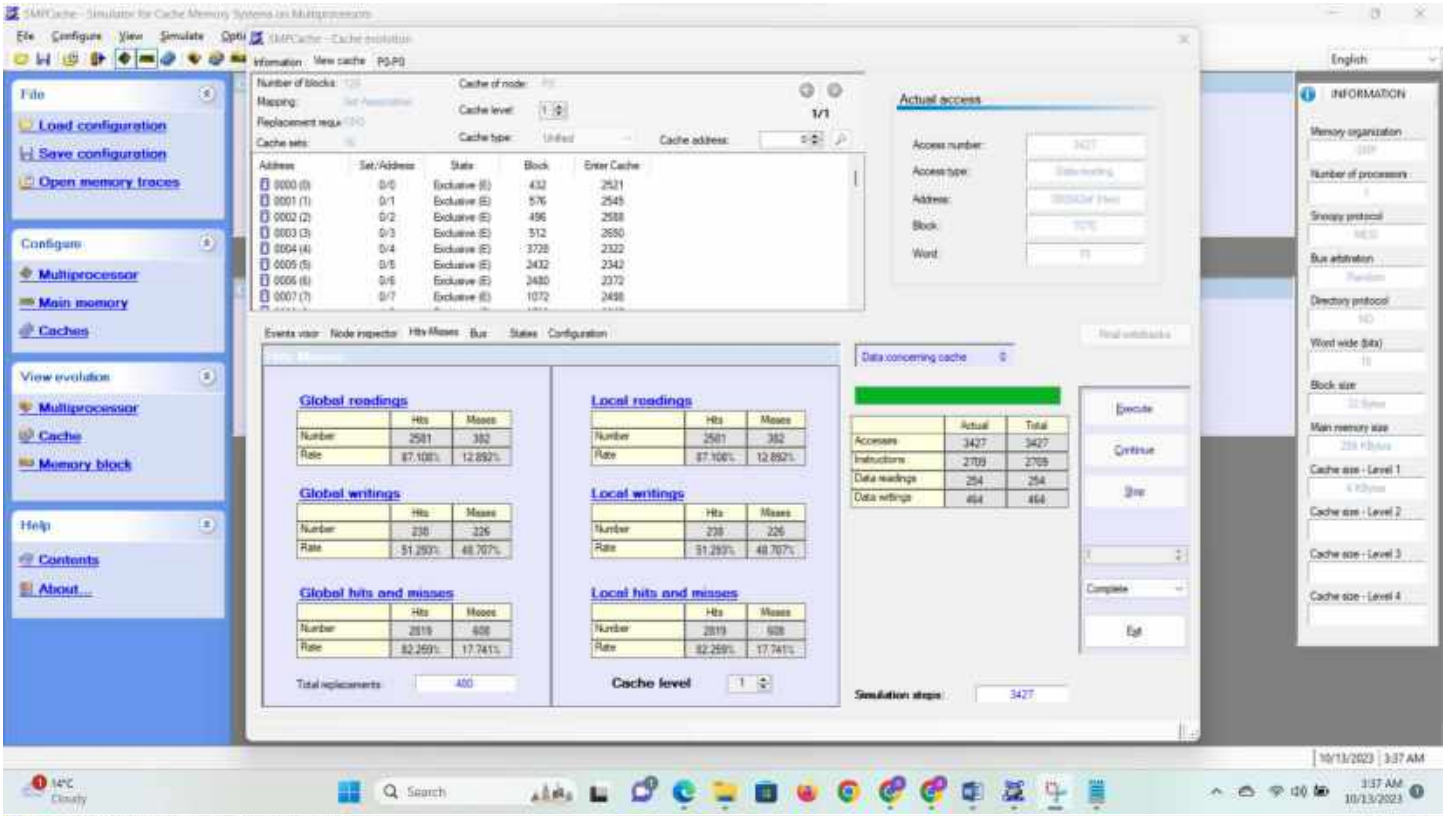
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Local hits and misses
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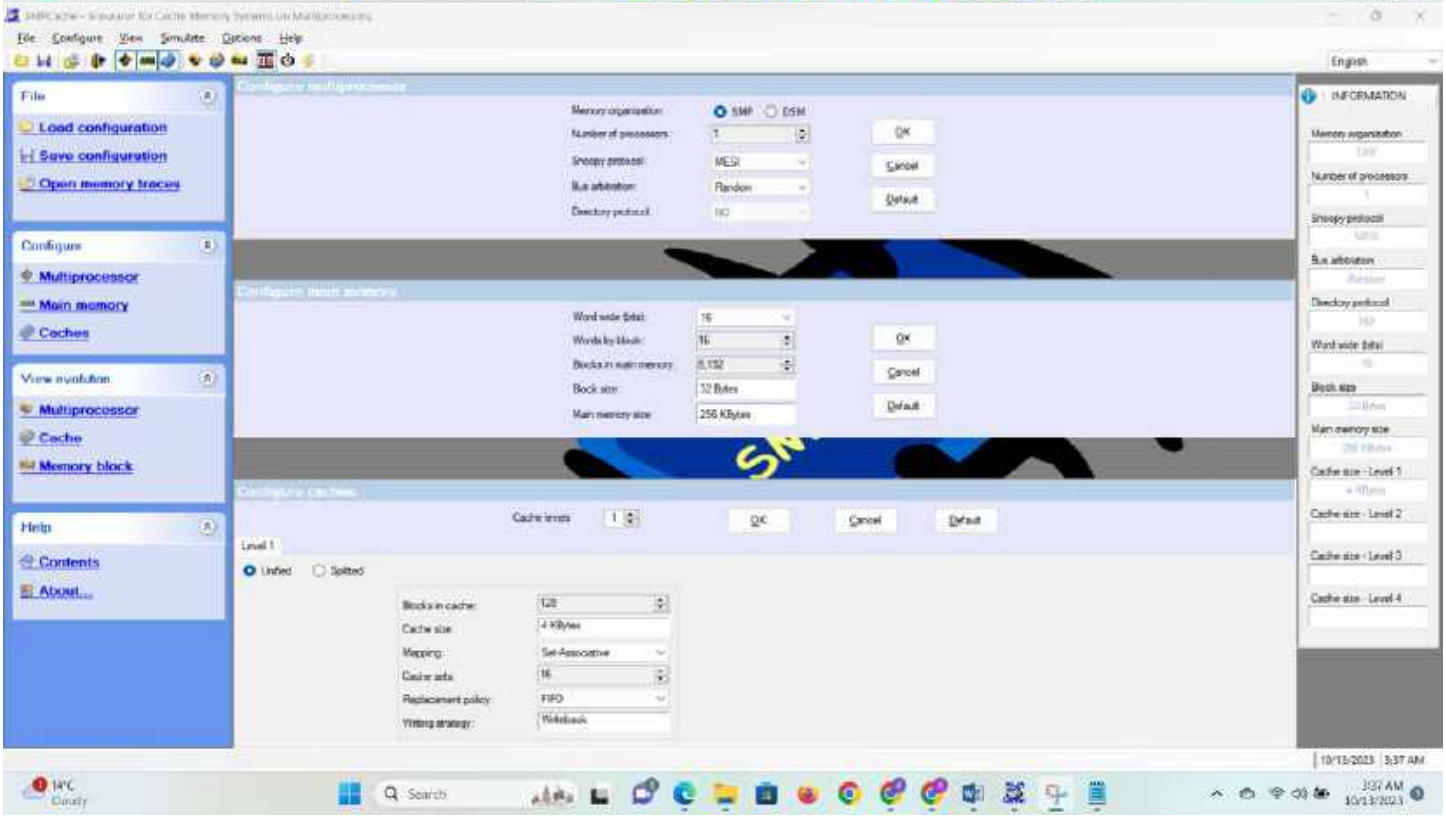
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Caches
View evolution
Multiprocessor
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Memory block
Help
Contents
About...
OK
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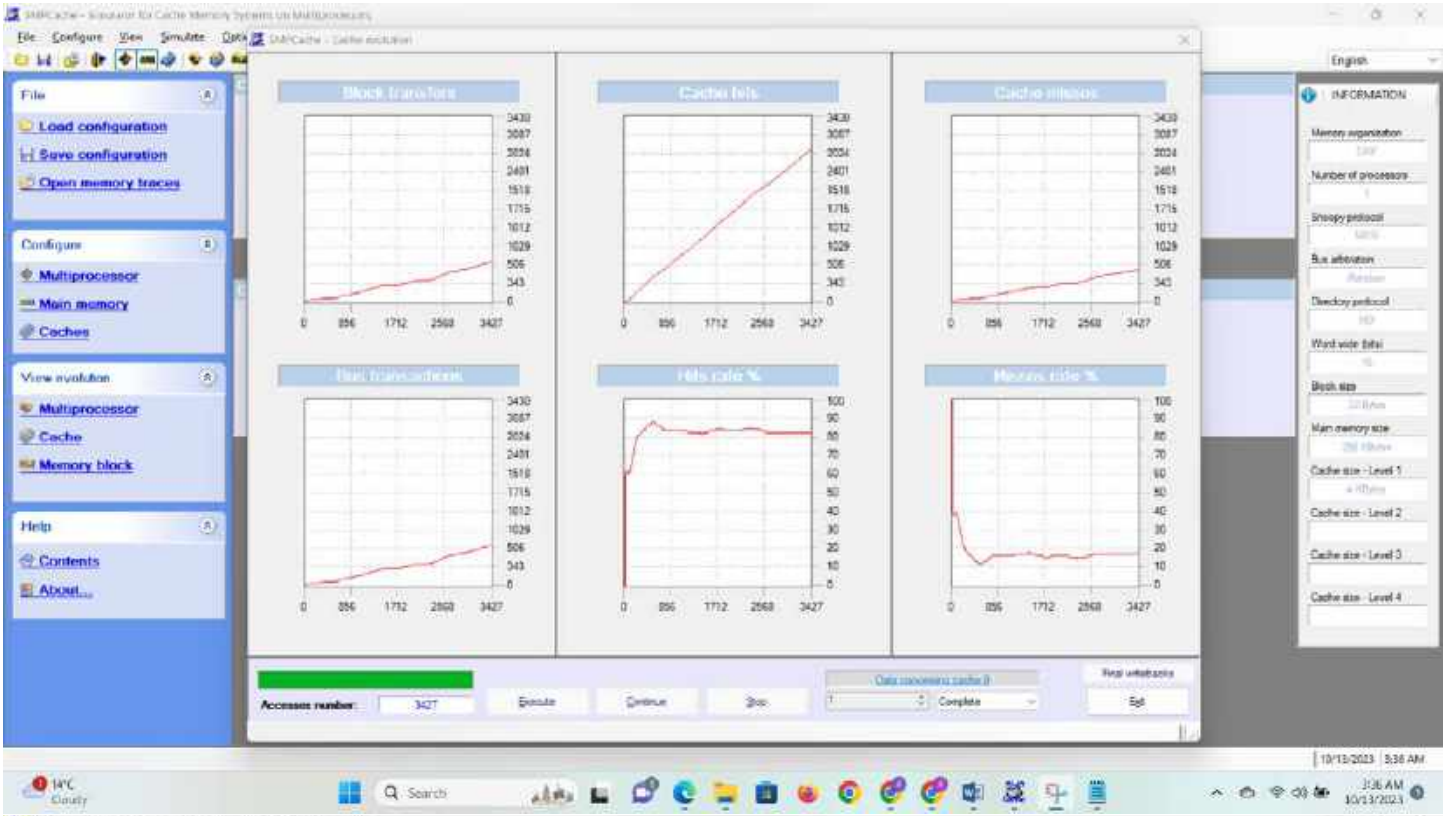
INFORMATION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Open memory traces
Configure
Multiprocessor
Main memory
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View evolution
Multiprocessor
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Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
3427
Execute
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Stop
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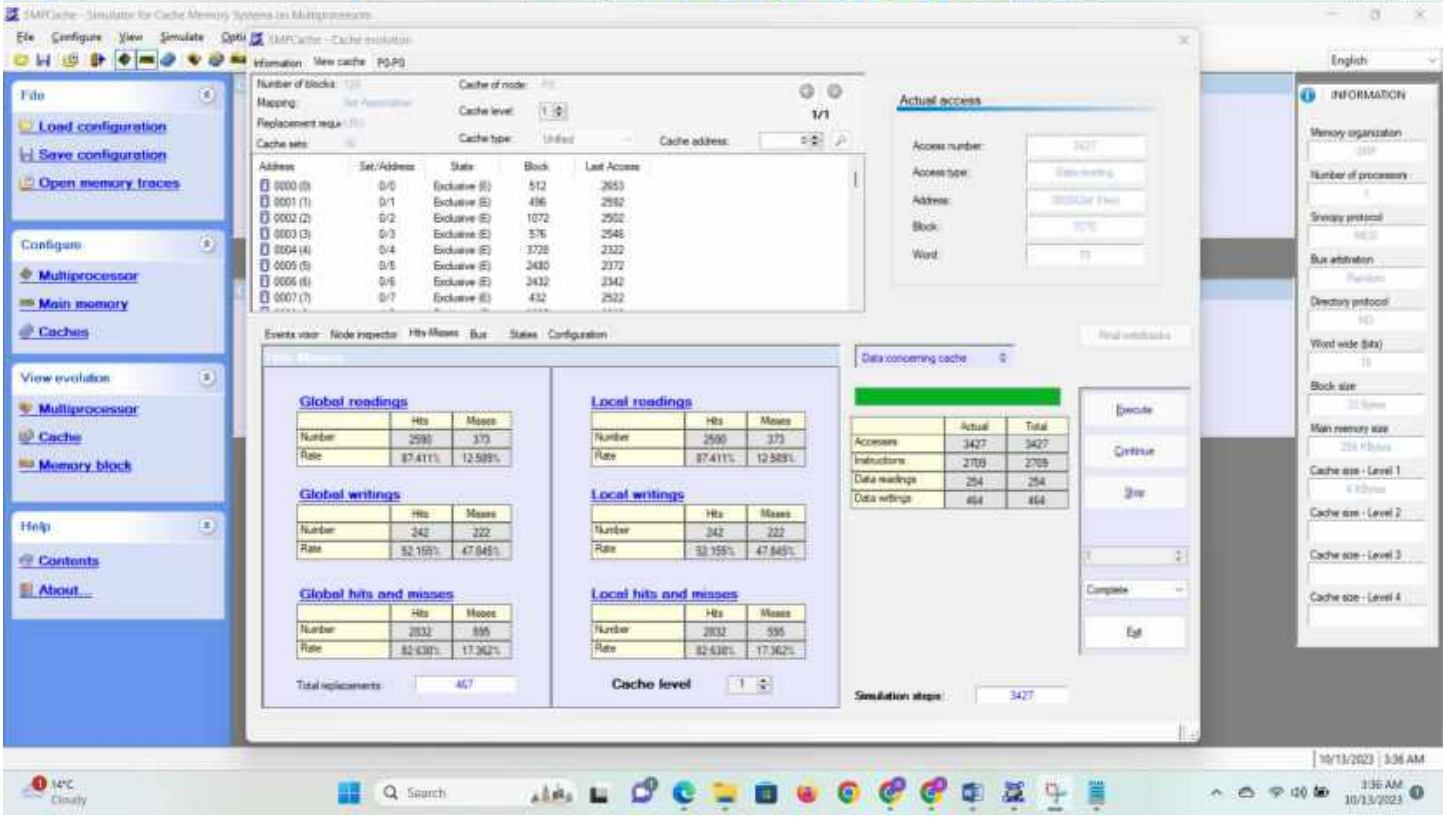
INFORMATION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Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
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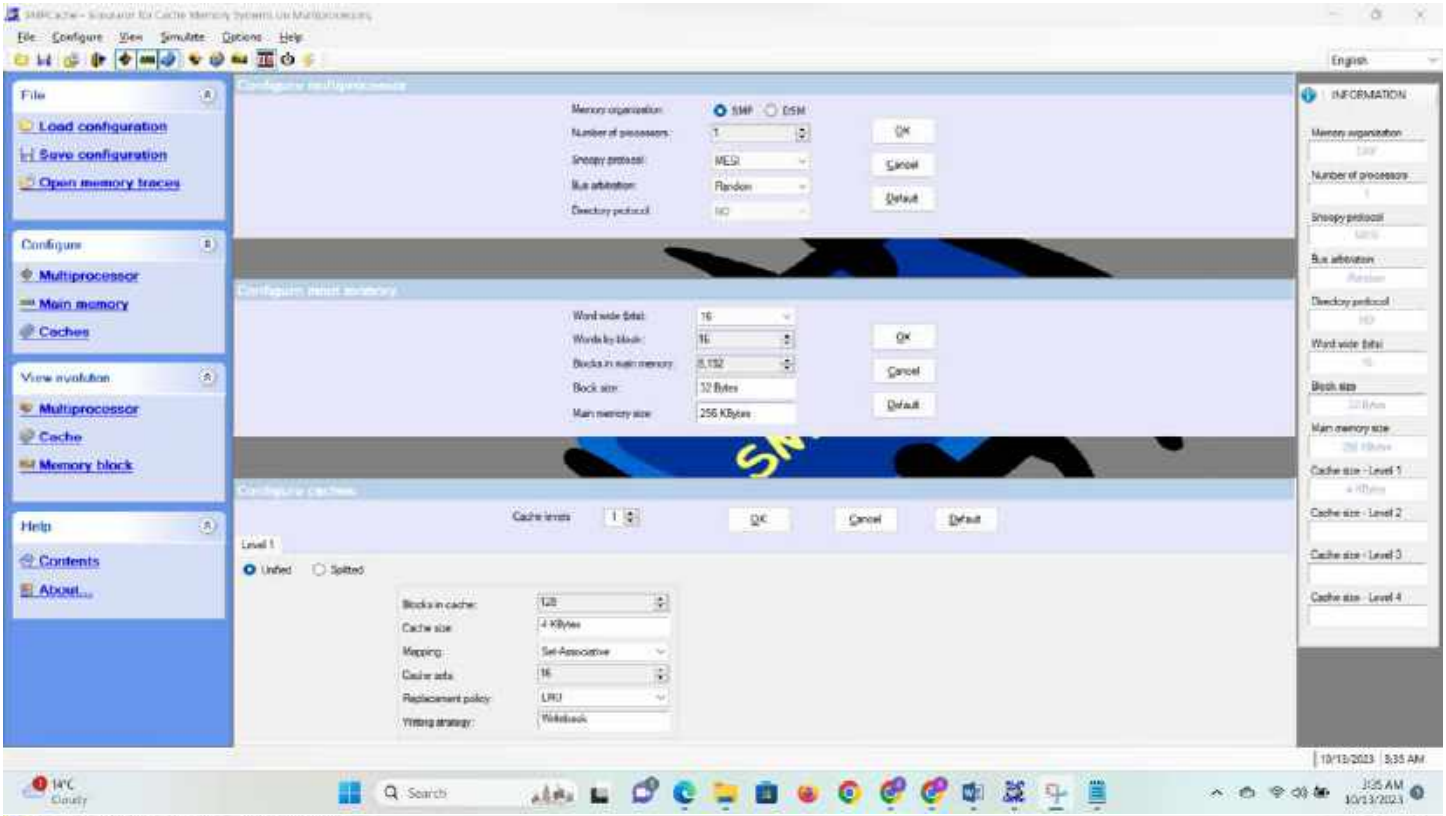
Execute
Continue
Stop
Exit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About...
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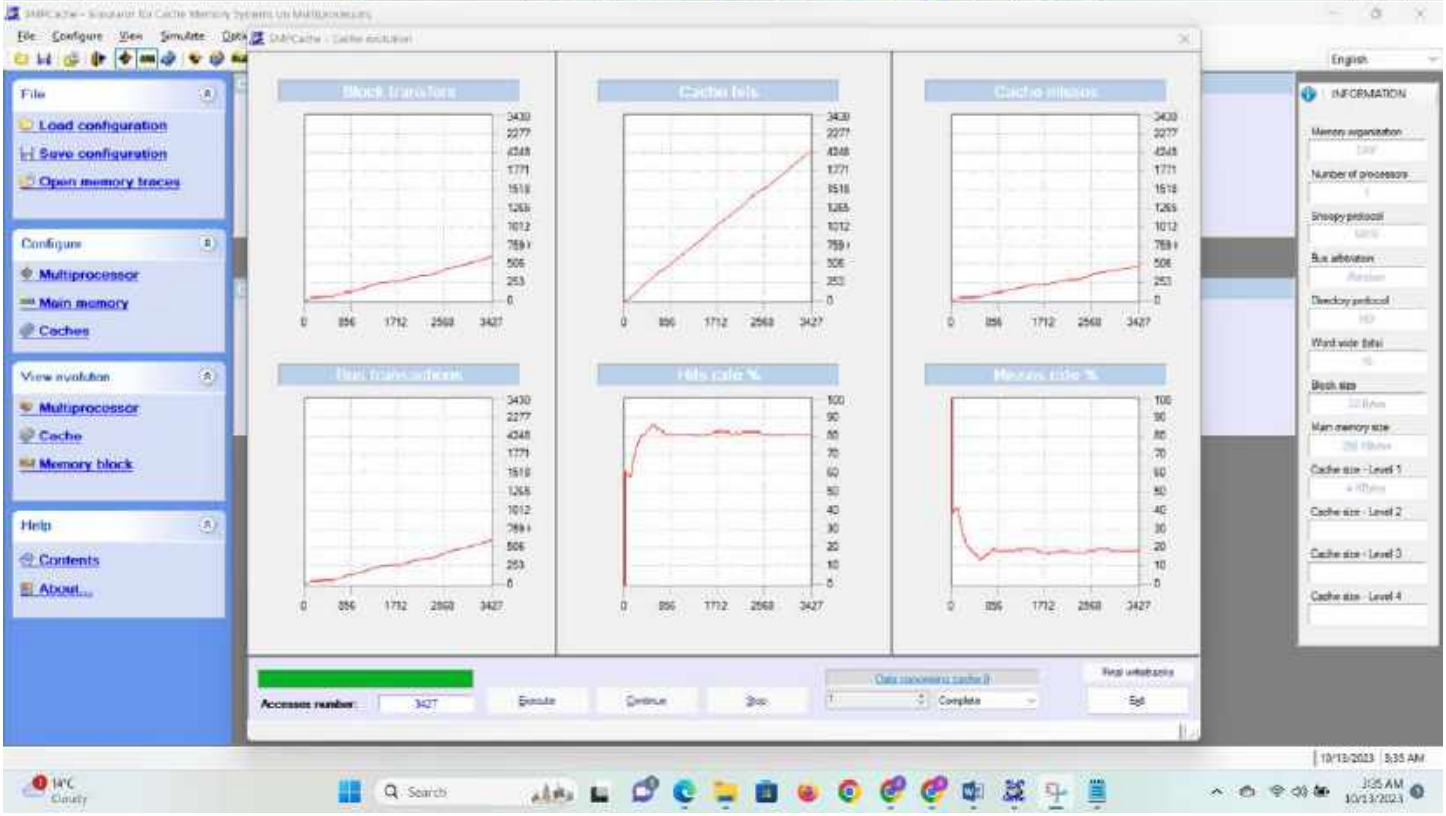
Default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Configure
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Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Accesses number:
3427
Execute
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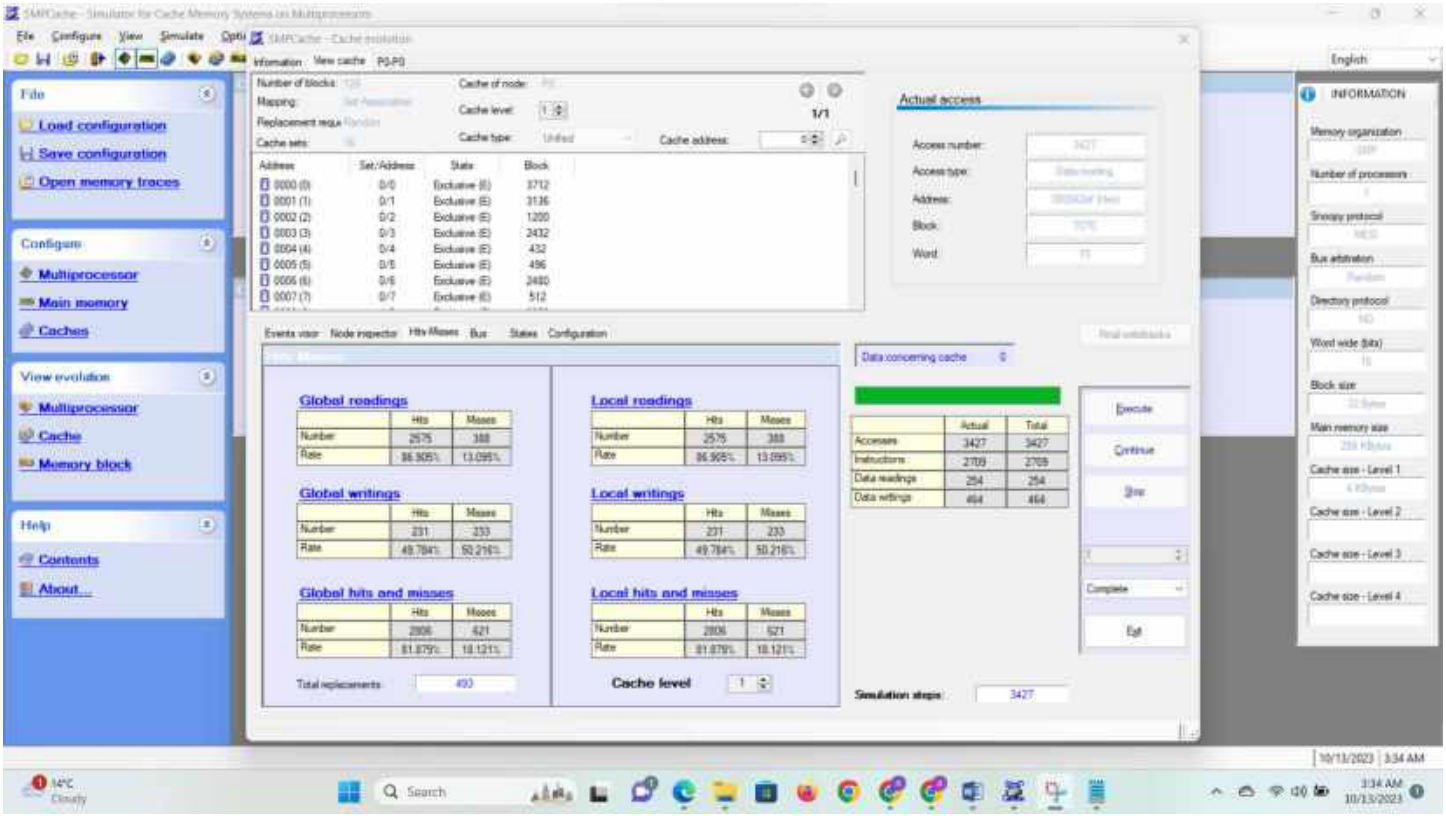
Stop
Exit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Open memory traces
Configure
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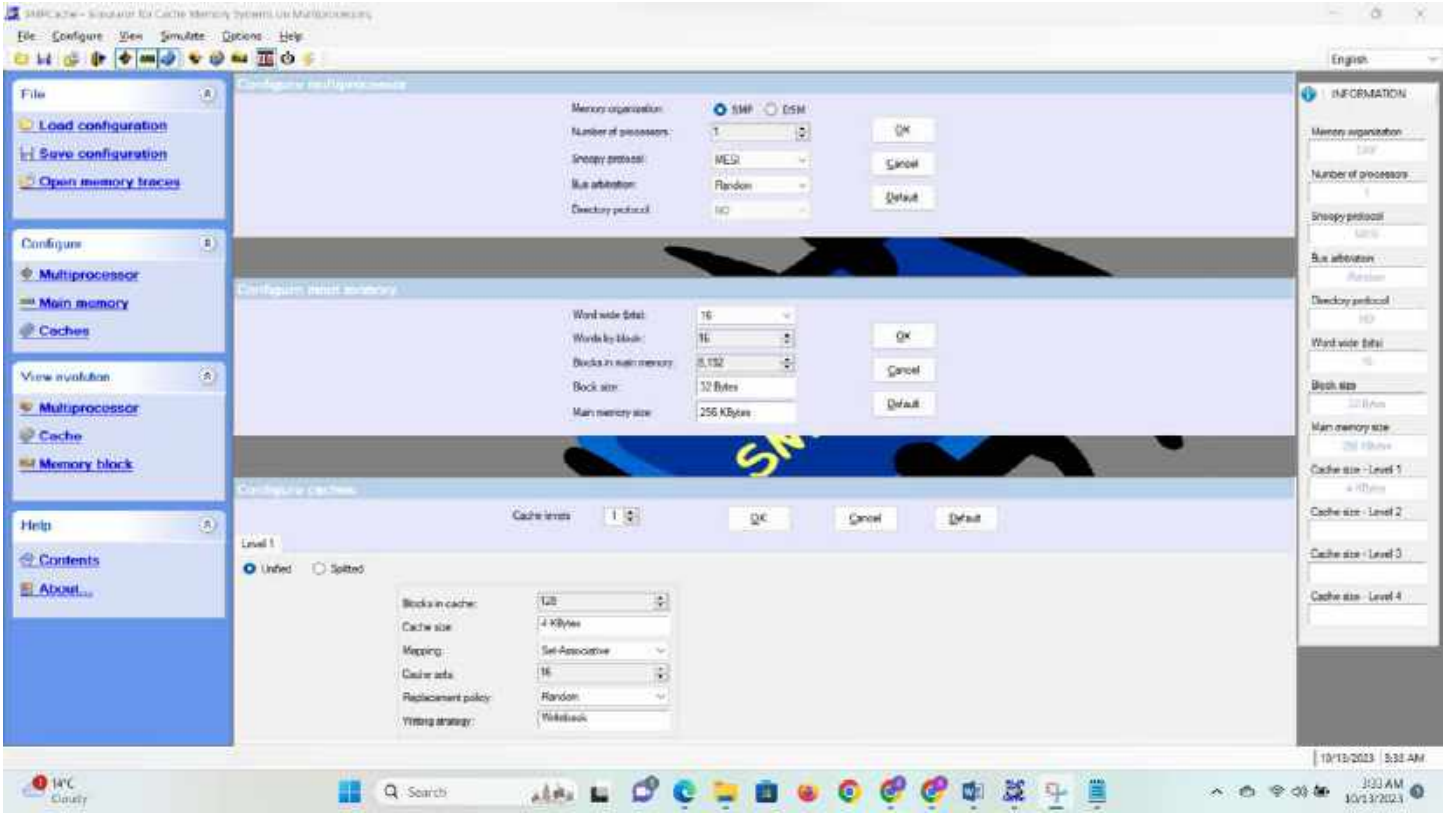
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION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Open memory traces
Configure
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Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
Default
INFORMATION

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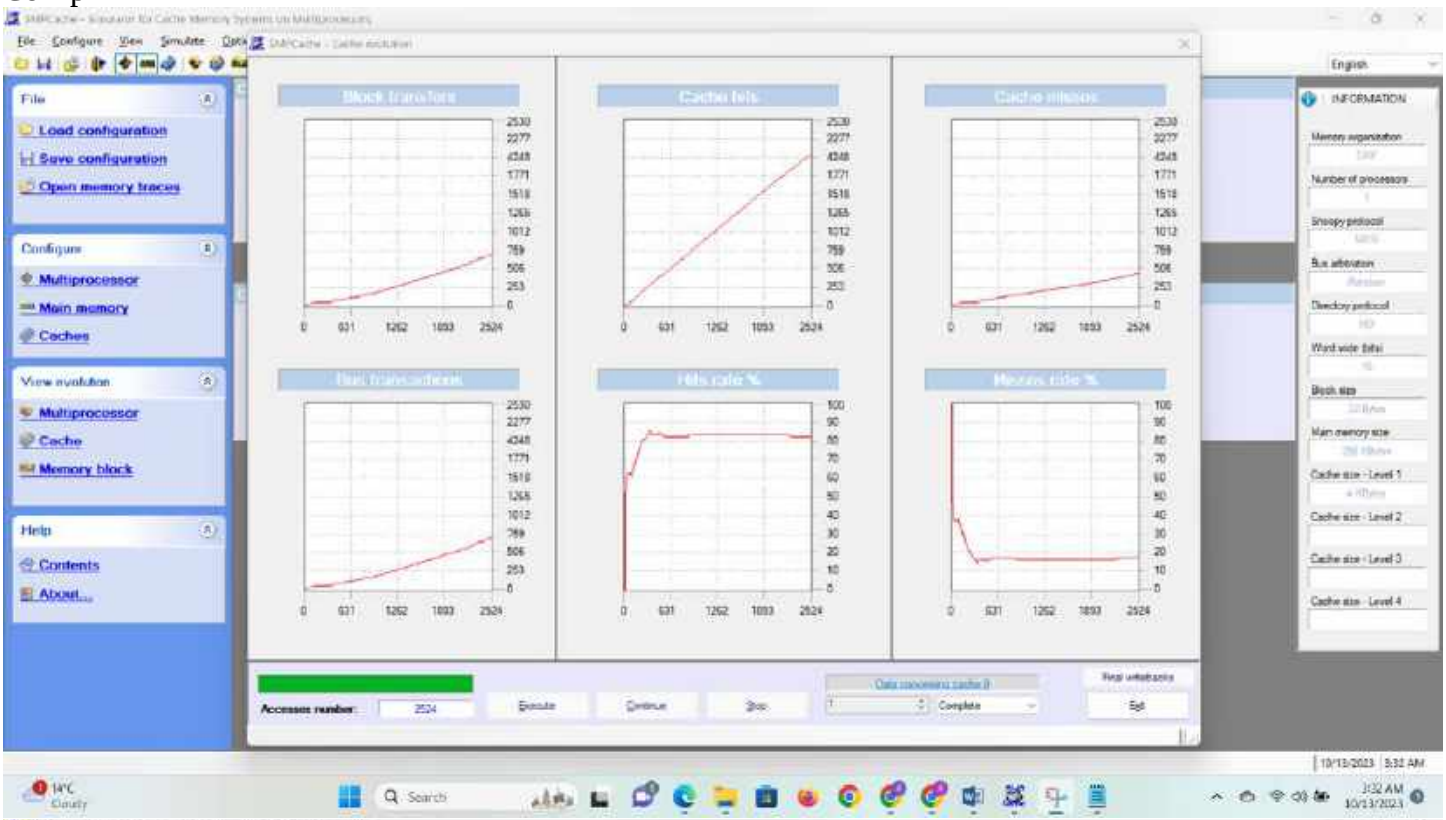
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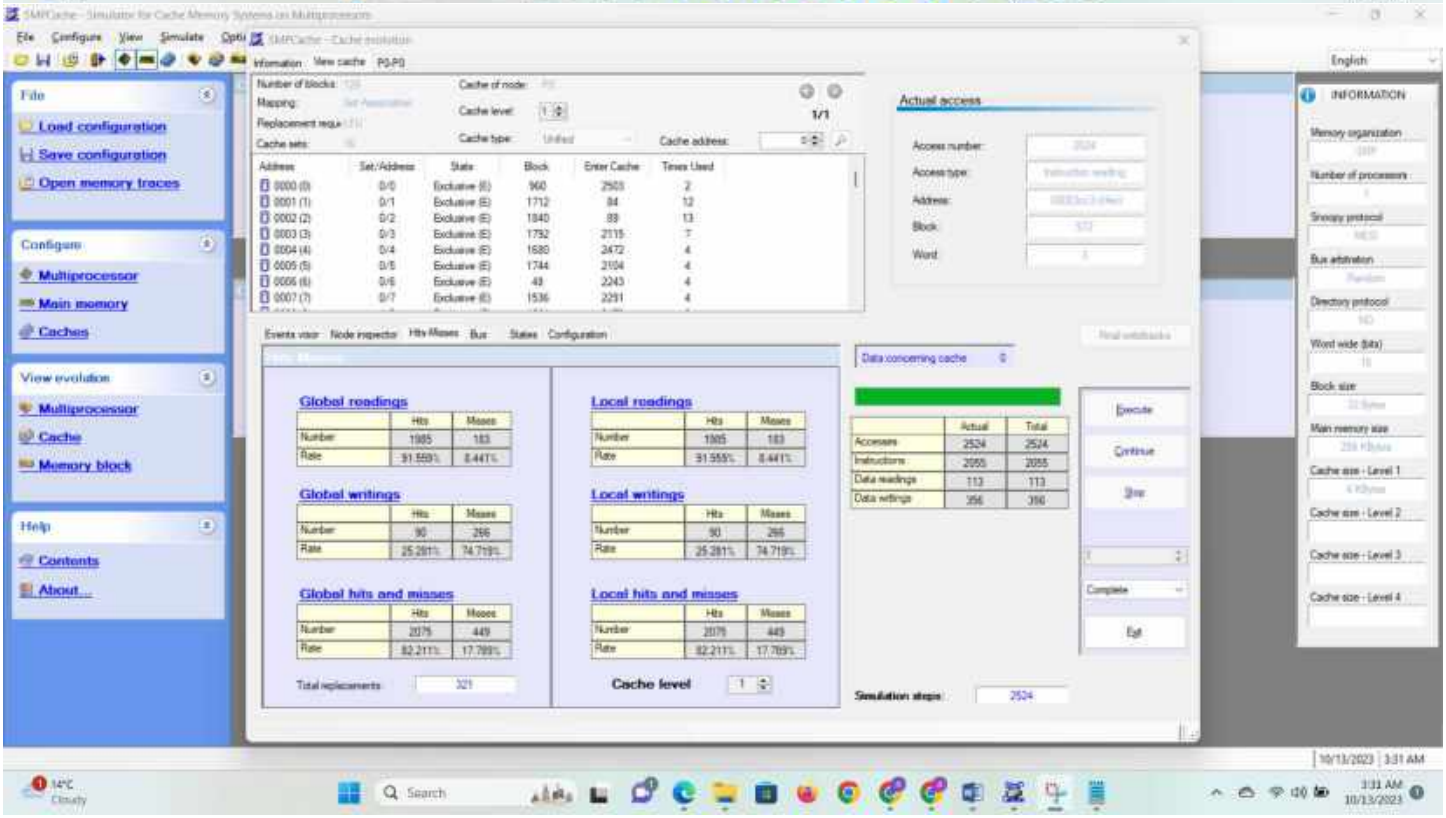
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Hits ratio %
Misses ratio %
Accesses number:
2524
Execute
Continue
Stop
Exit
INFORMATION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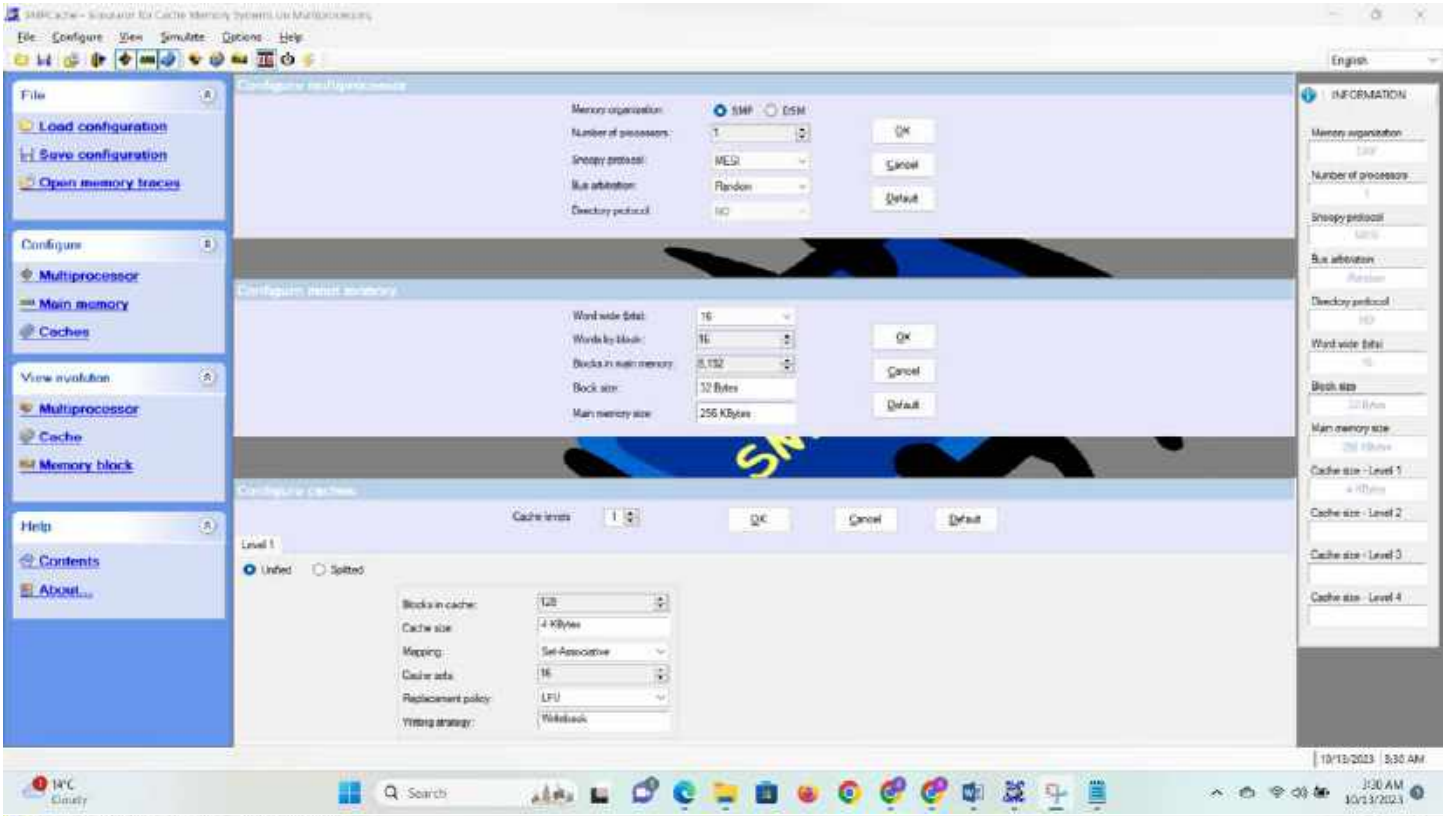
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
2524
Execute
Continue
Stop
Exit
INFORMATION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Save configuration
Open memory traces
Configure
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Main memory
Caches
View evolution
Multiprocessor
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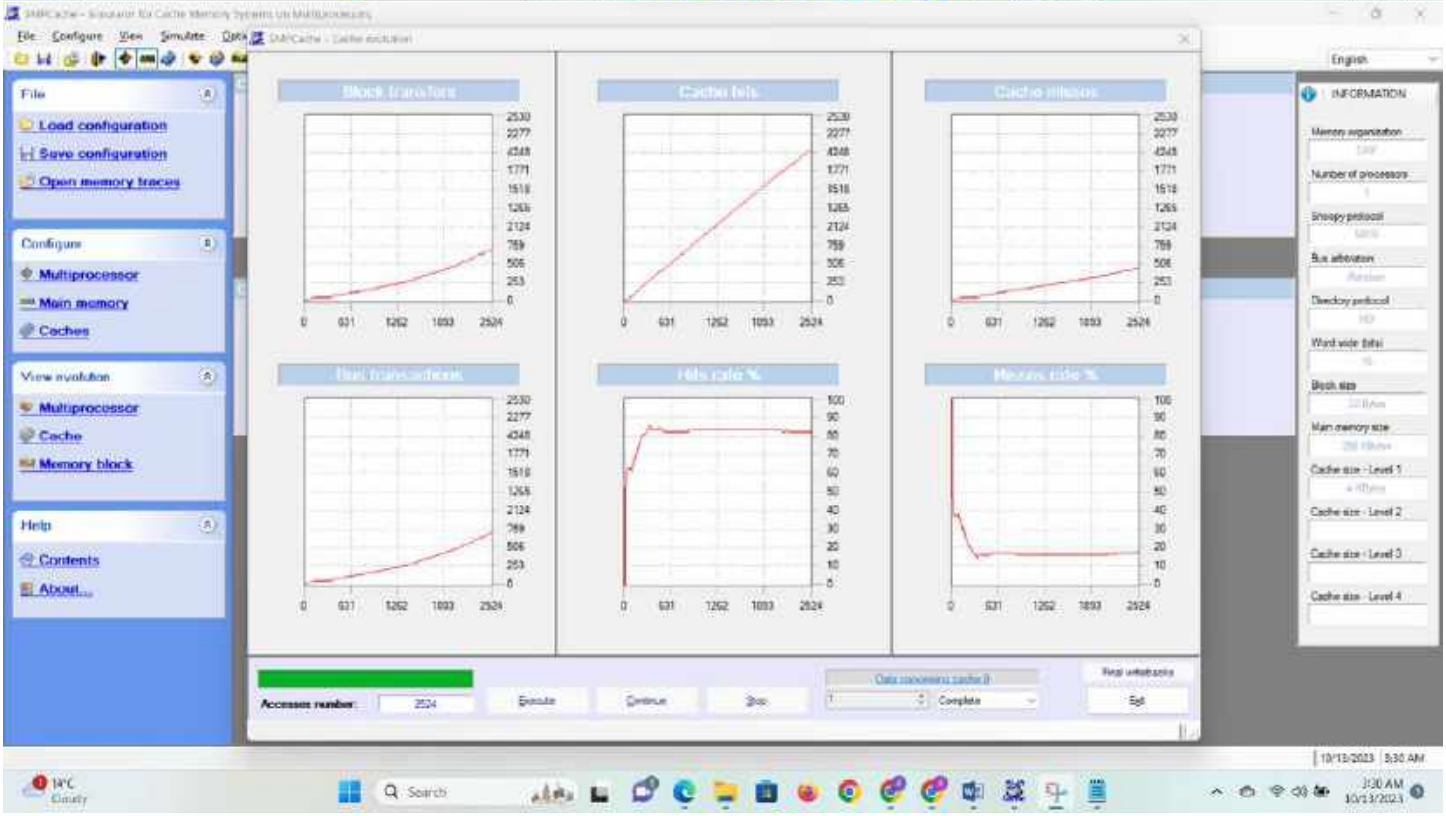
Help
Contents
About...
INFORMATION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Open memory traces
Configure
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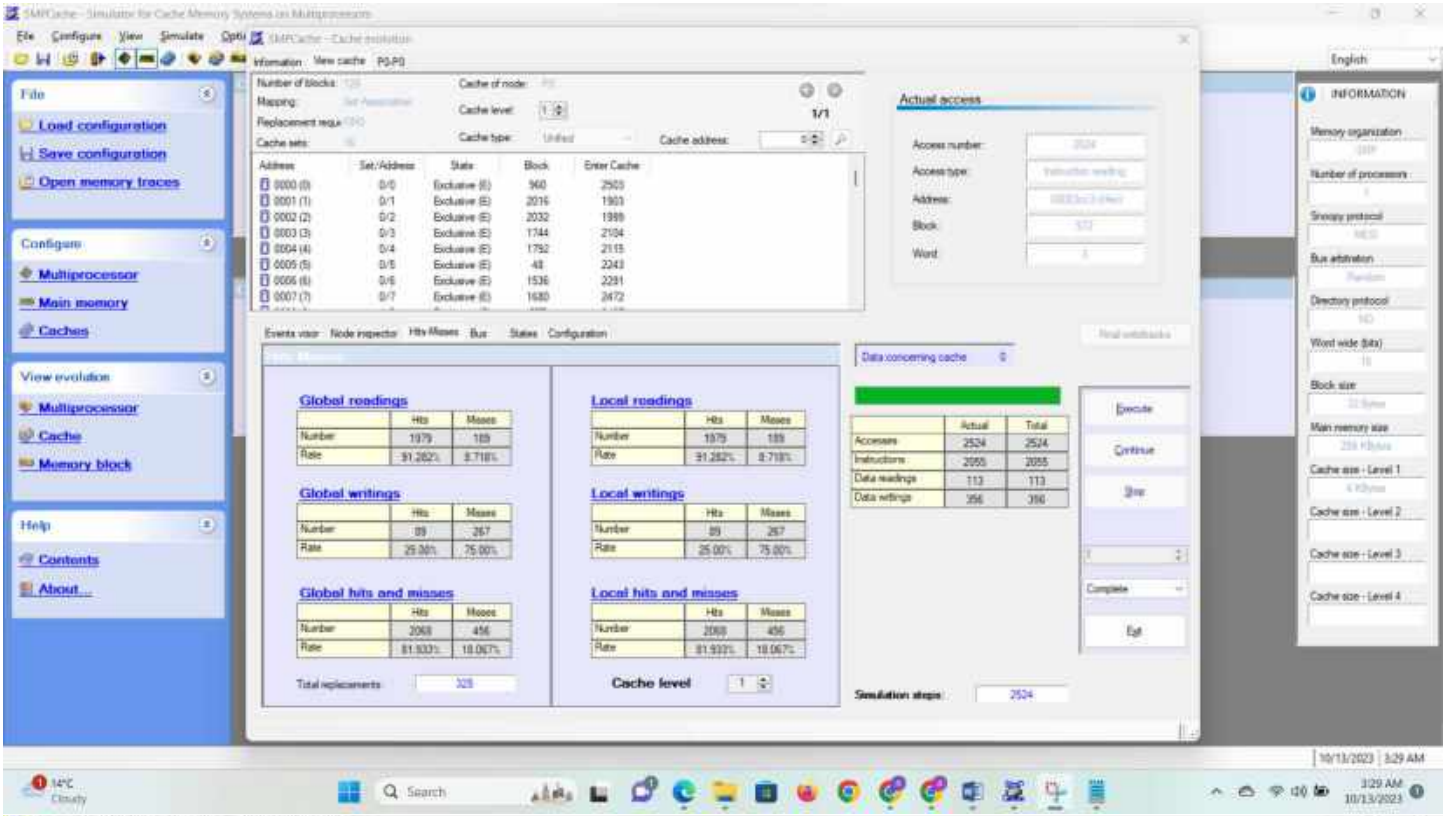
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Accesses number:
Execute
Continue
Stop
Exit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Open memory traces
Configure
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View evolution
Multiprocessor
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Memory block
Help
Contents
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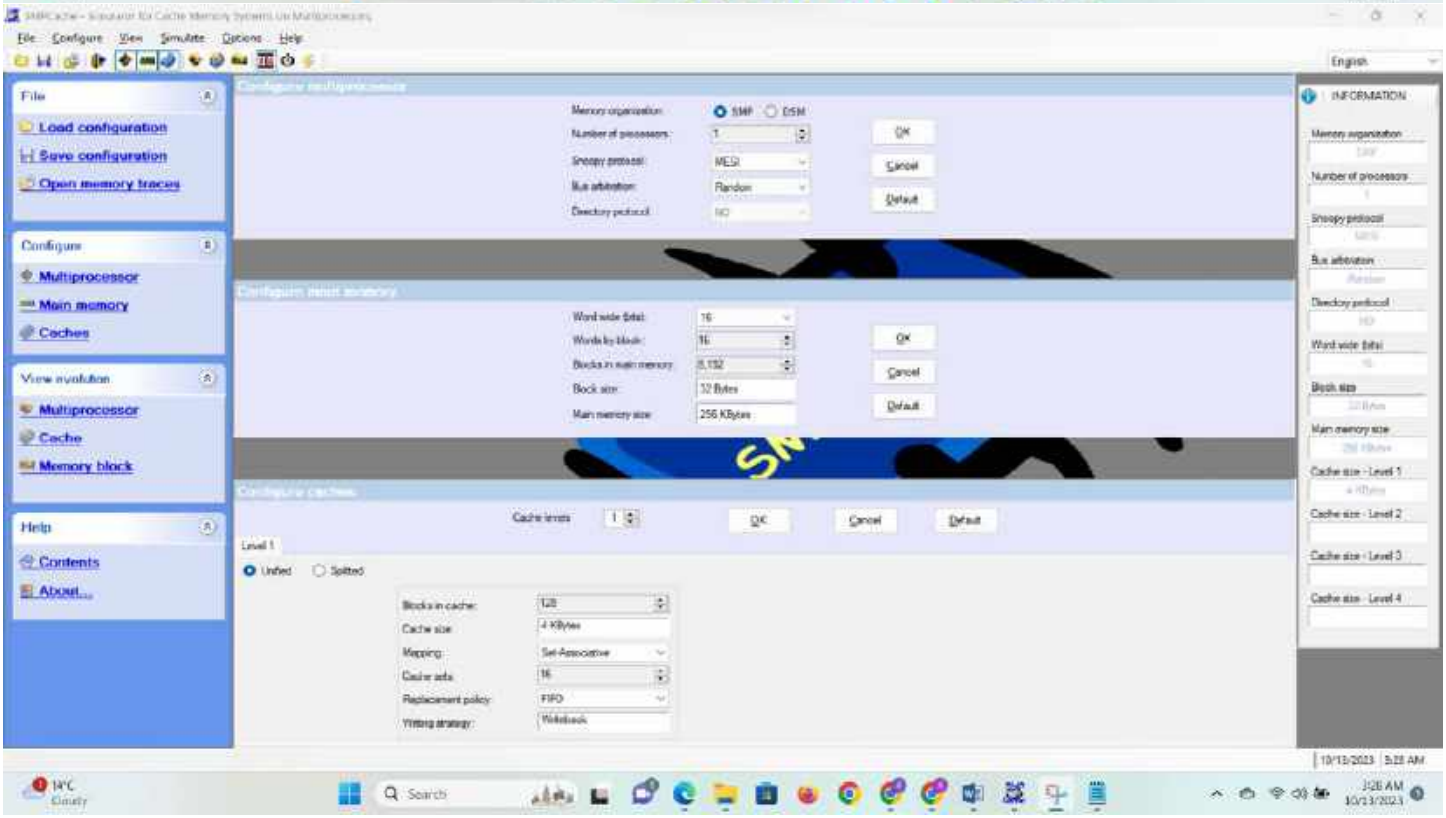
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Step
Exit
INFORMATION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Save configuration
Open memory traces
Configure
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Caches
View evolution
Multiprocessor
Cache
Memory block
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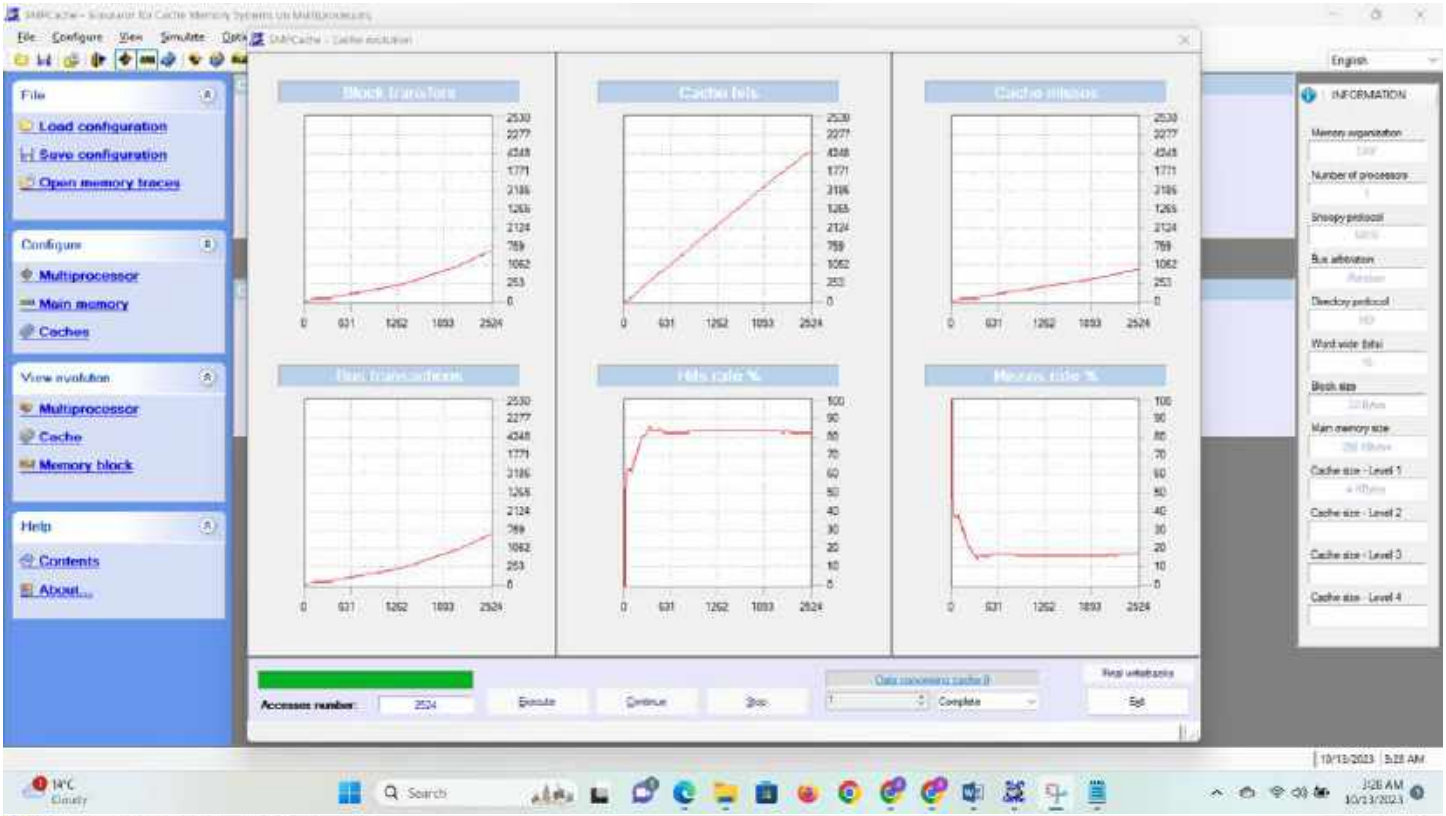
Contents
About...
OK
Cancel
Default
INFORMATION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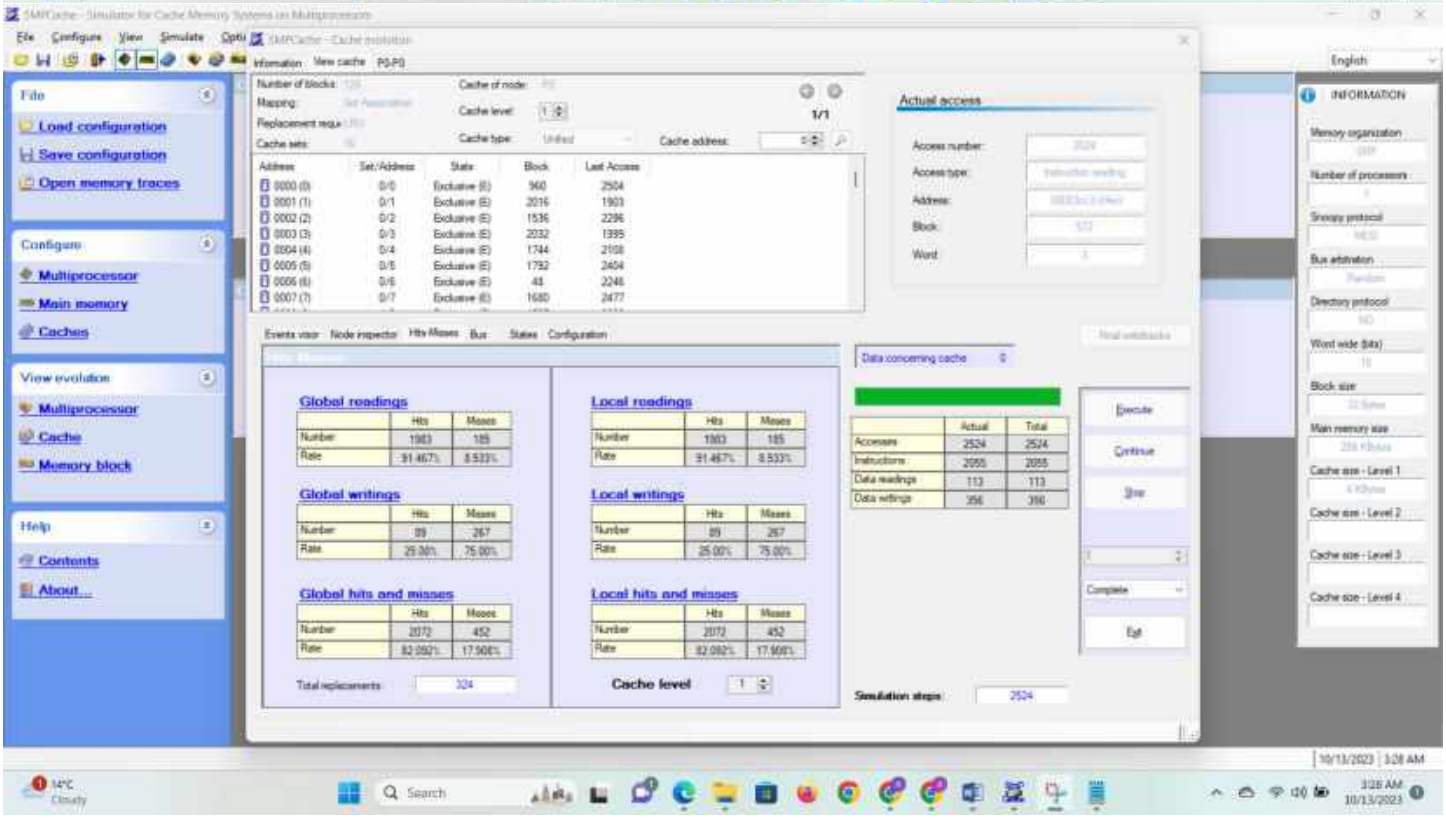
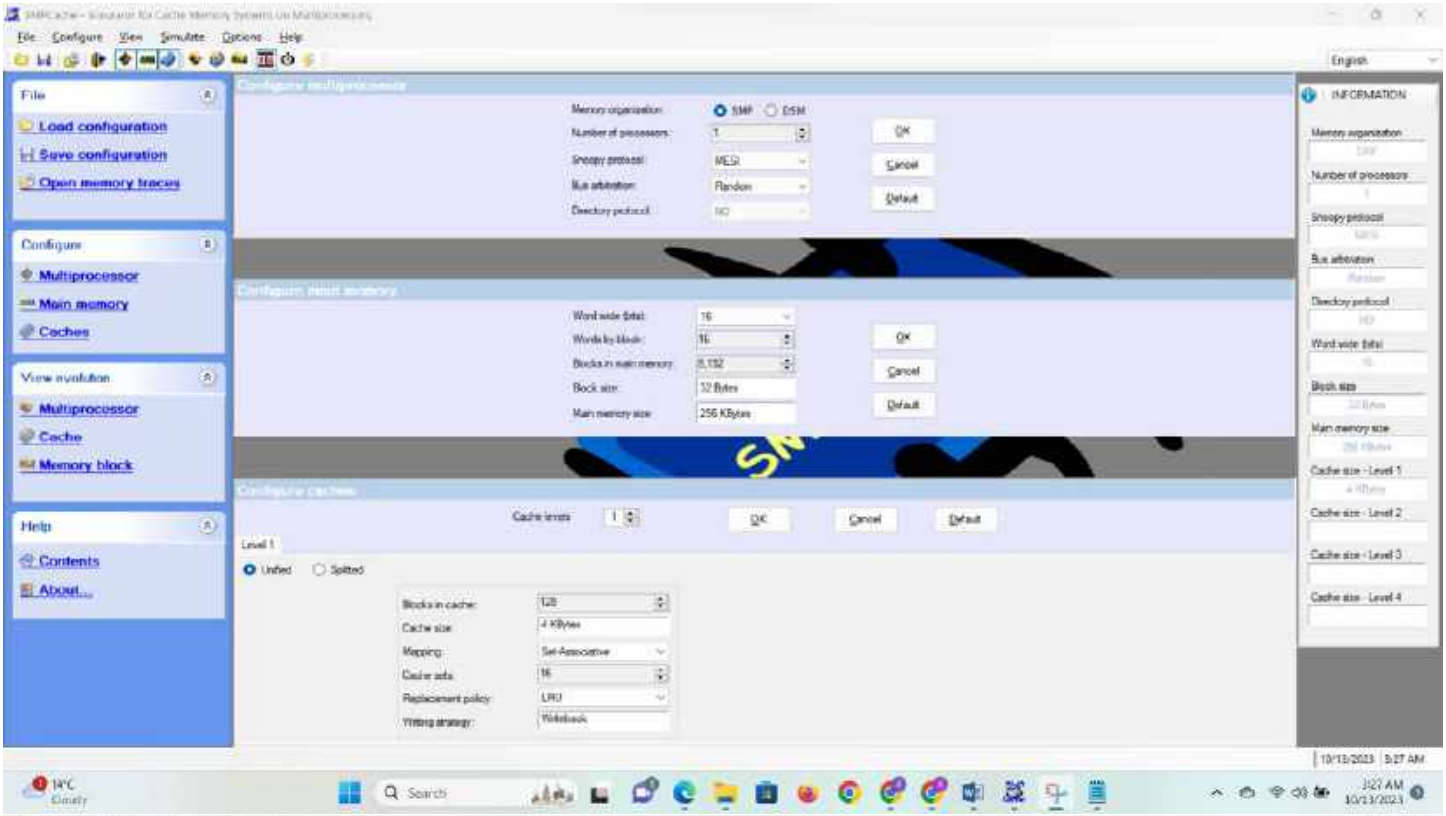
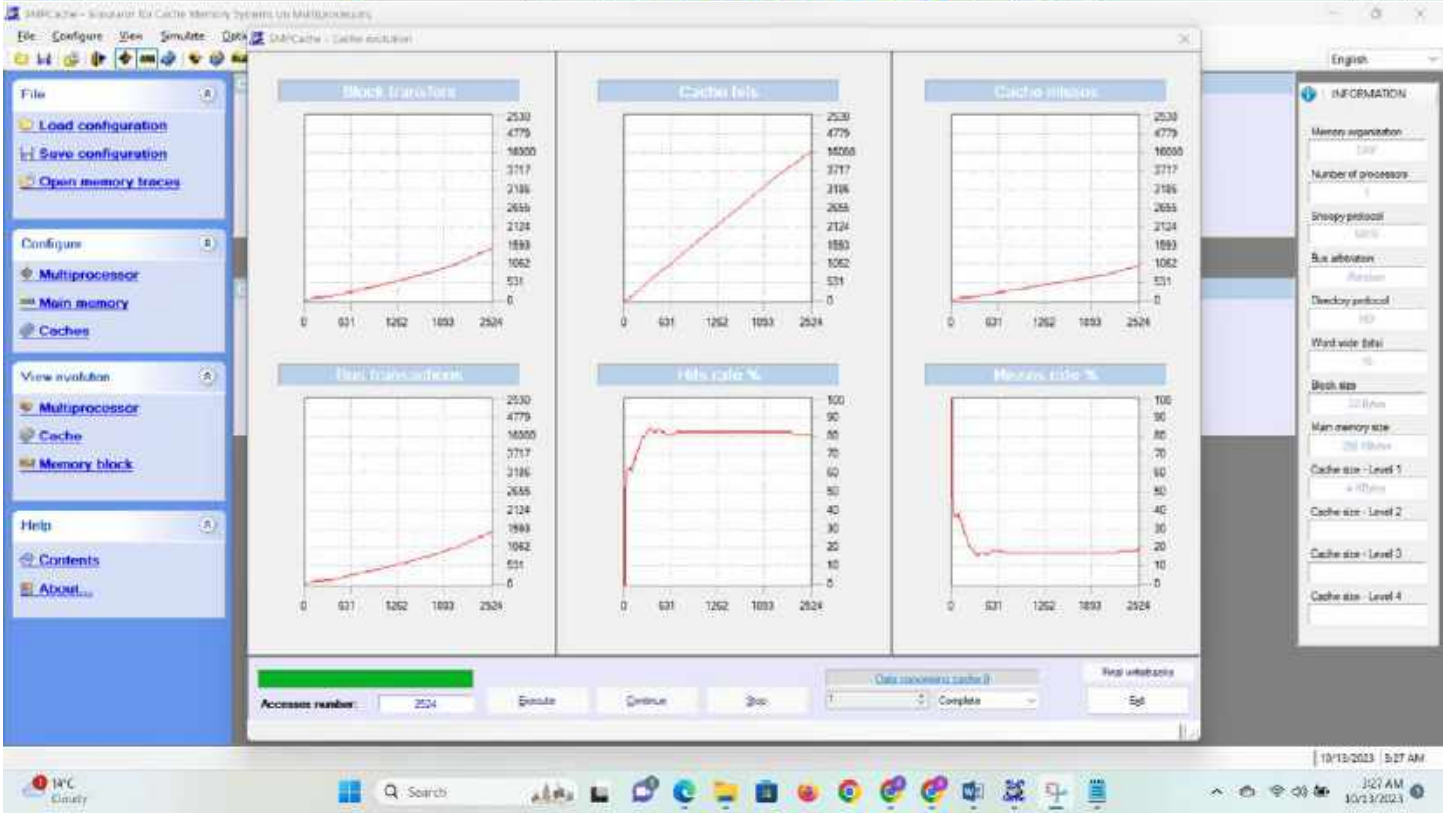
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
2524
Execute
Continue
Stop
Exit
INFORMATION


Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
2524
Execute
Continue
Stop
Exit


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
OK
Cancel
Default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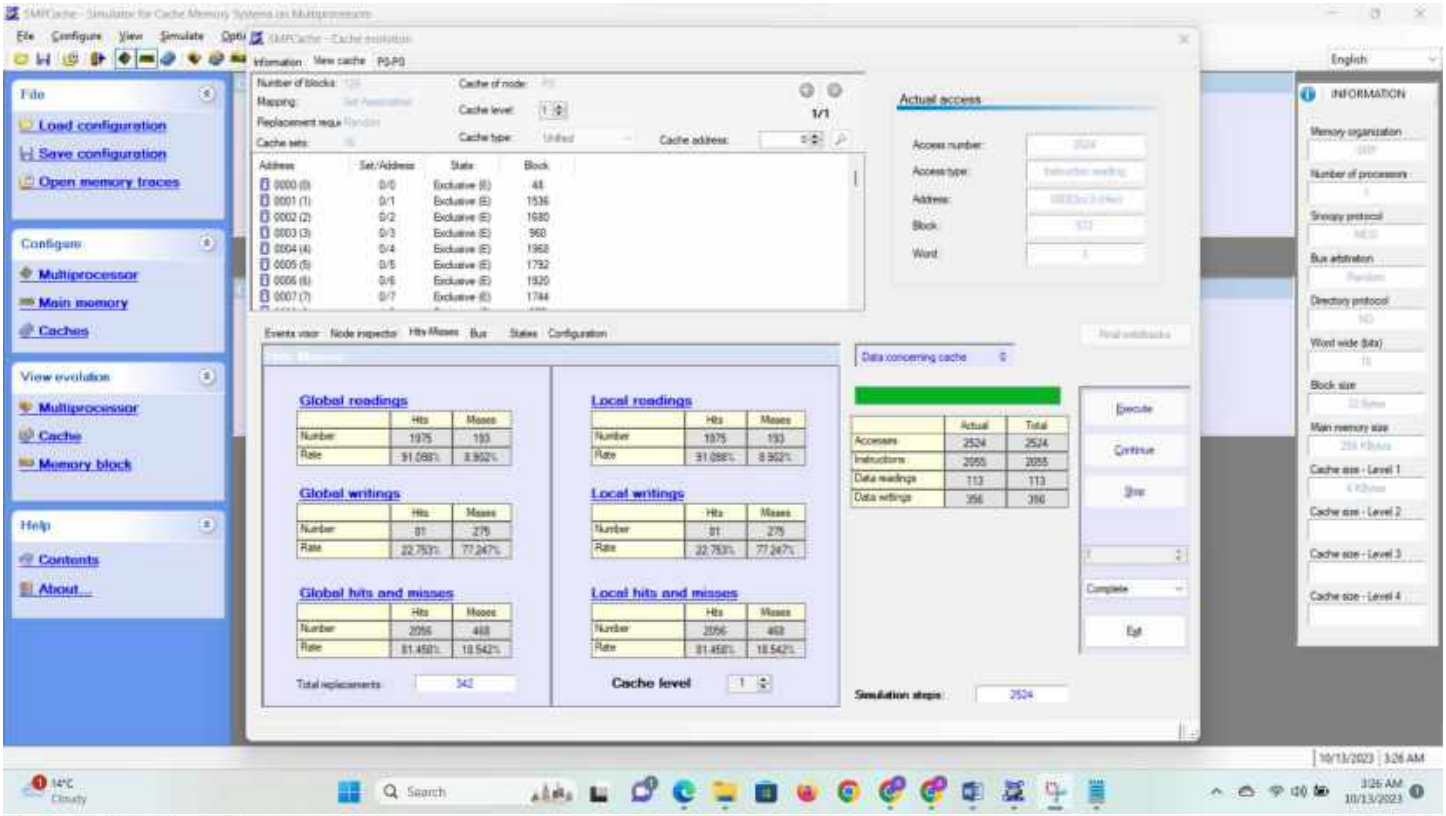
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Accesses number:
Execute
Continue
Stop
Exit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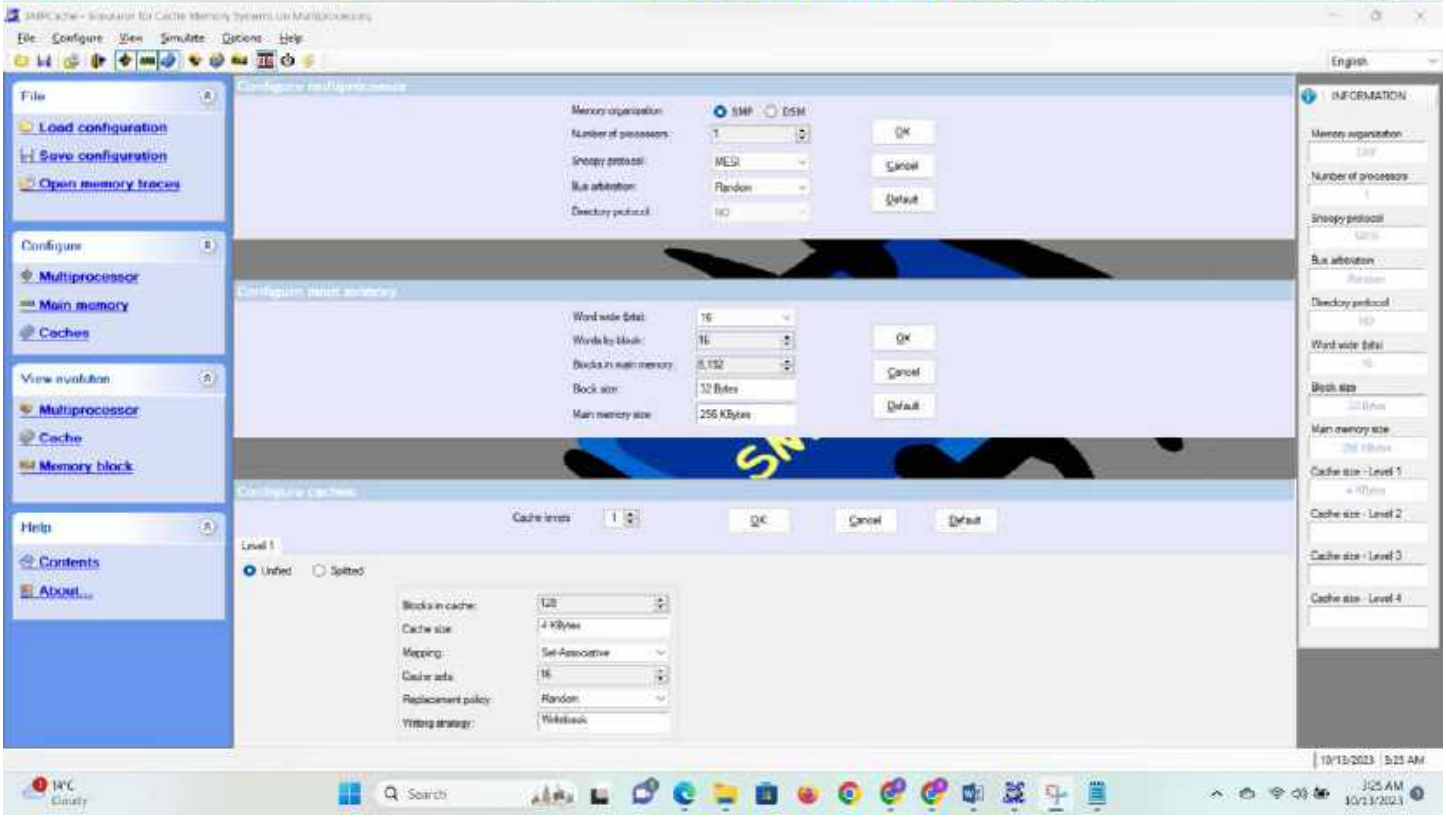
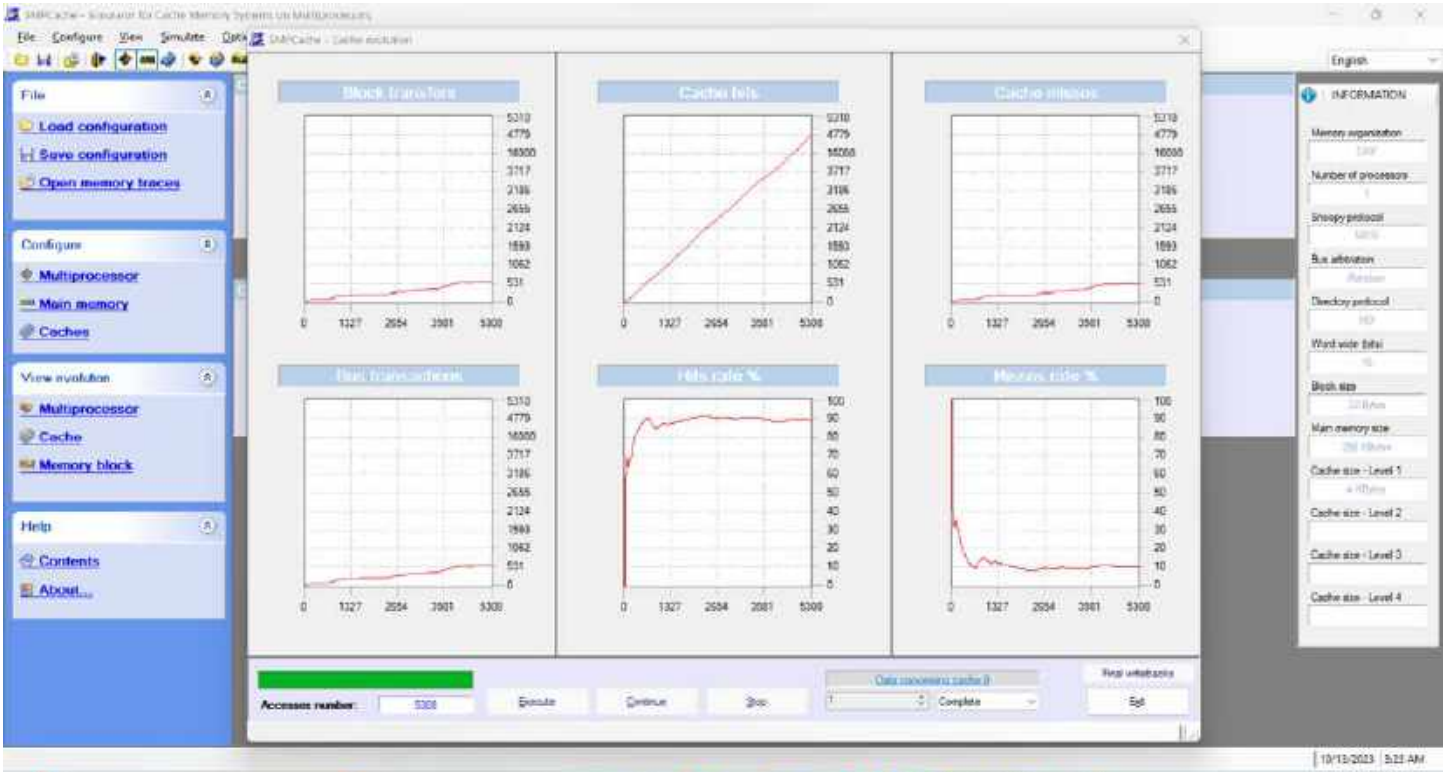
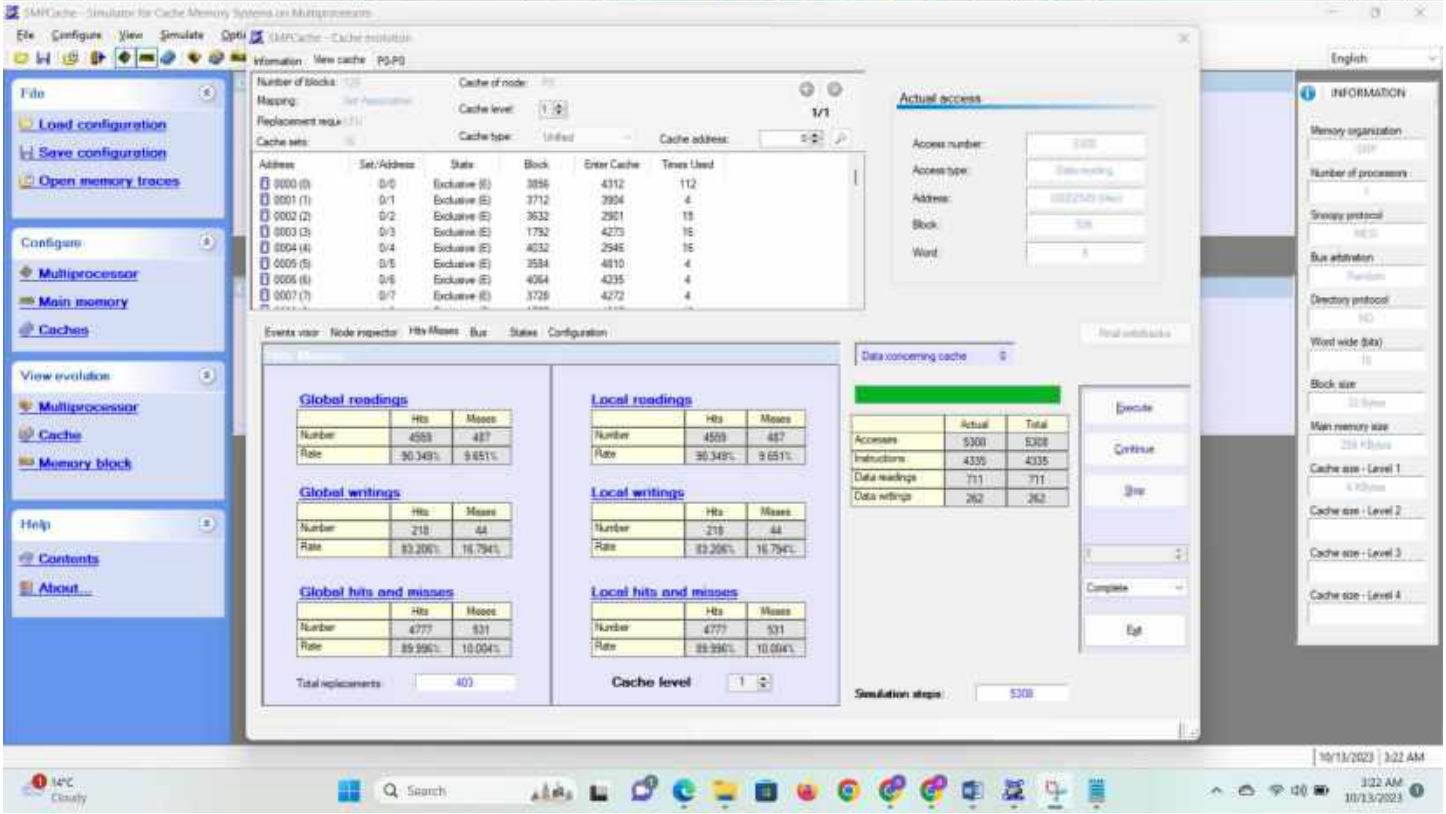
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
Default
INFORMATION

Ear


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transactions
Cache hits
Cache misses
Hits ratio %
Misses ratio %
Accesses number:
Execute
Continue
Stop
Exit
INFORMATION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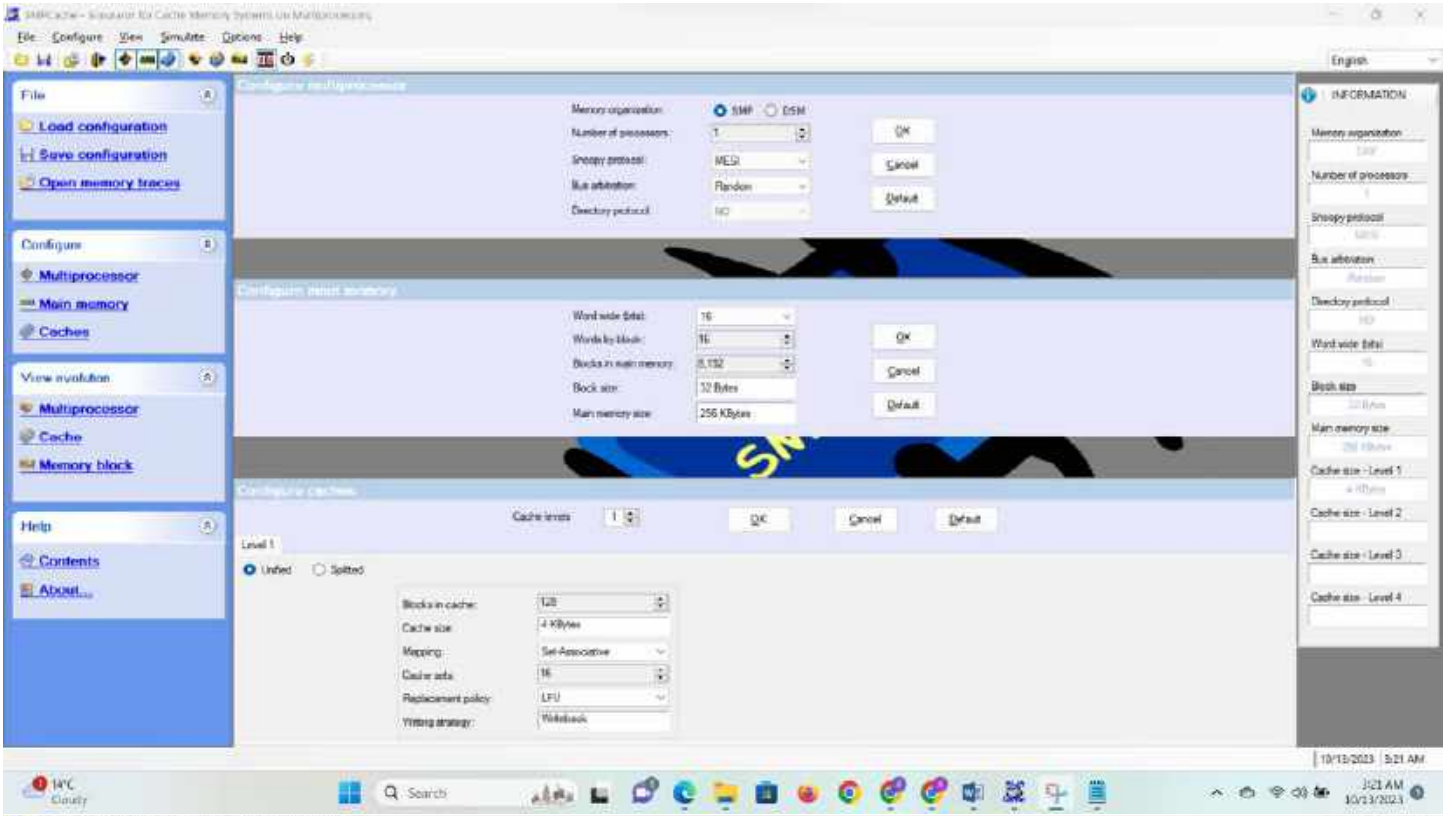
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
Execute
Continue
Stop
Exit
INFORMATION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Save configuration
Open memory traces
Configure
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Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
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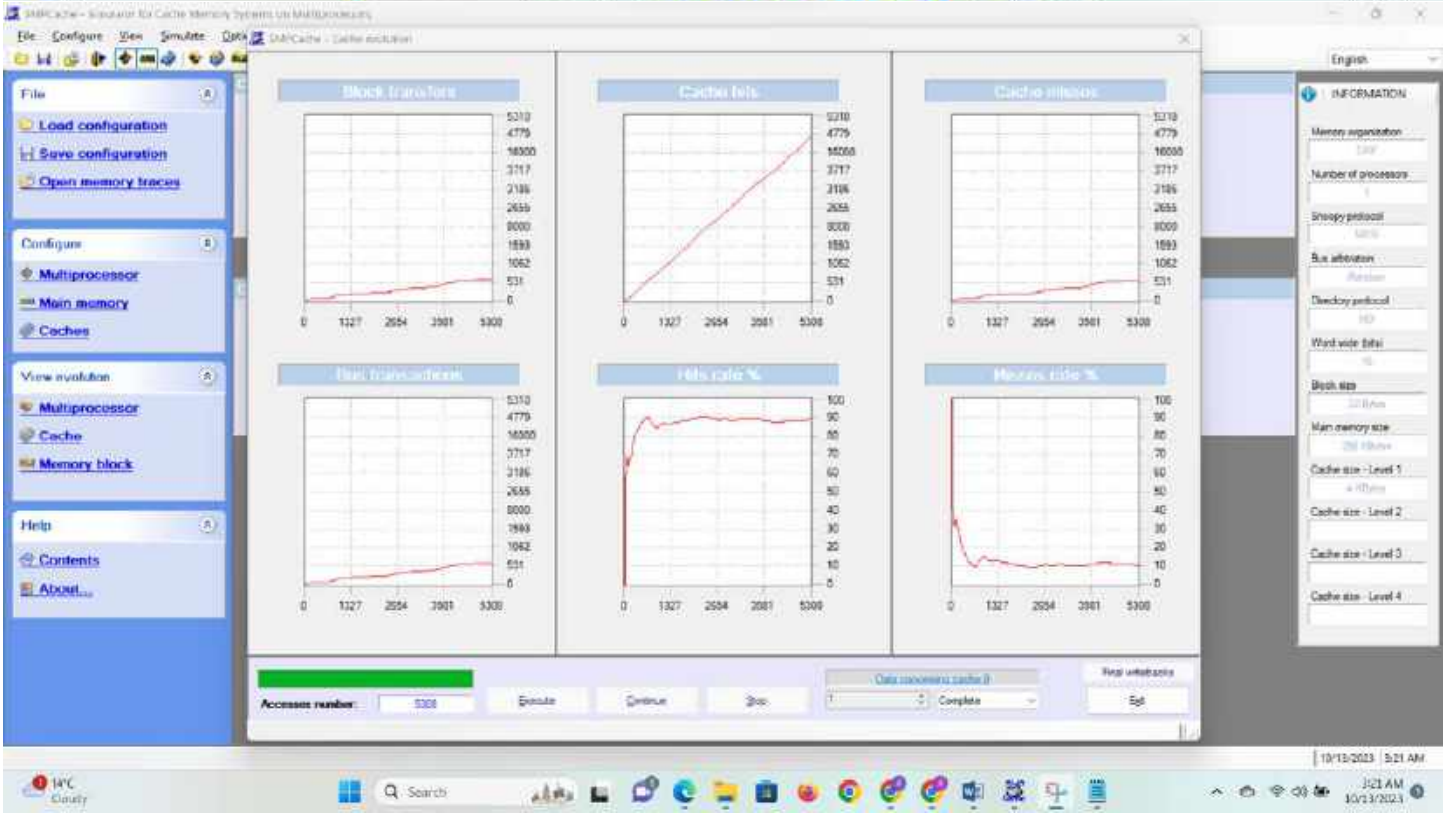
About...
INFORMATION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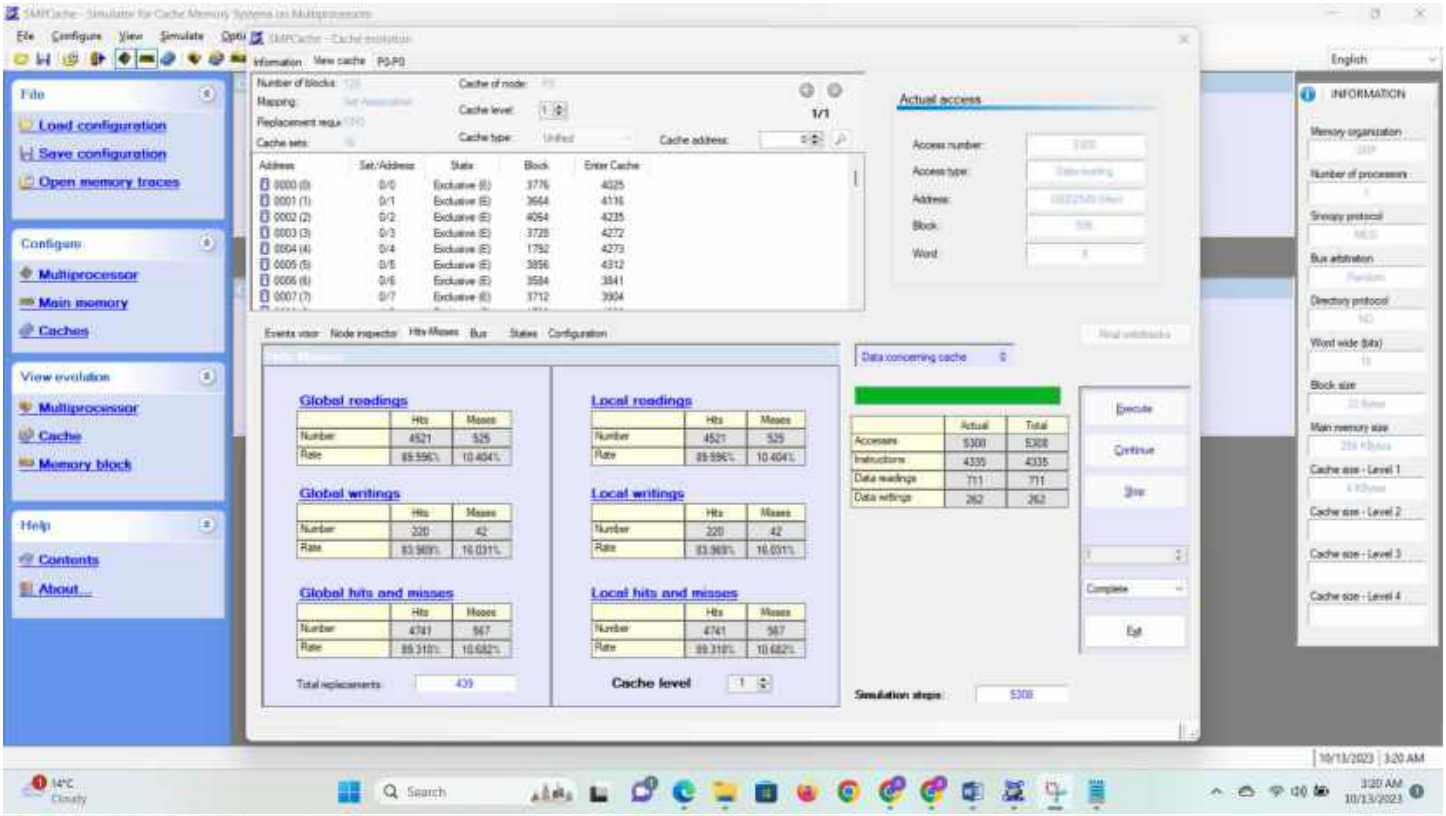
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Accesses number:
Execute
Continue
Stop
Exit


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
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Memory block
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
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Continue
Step
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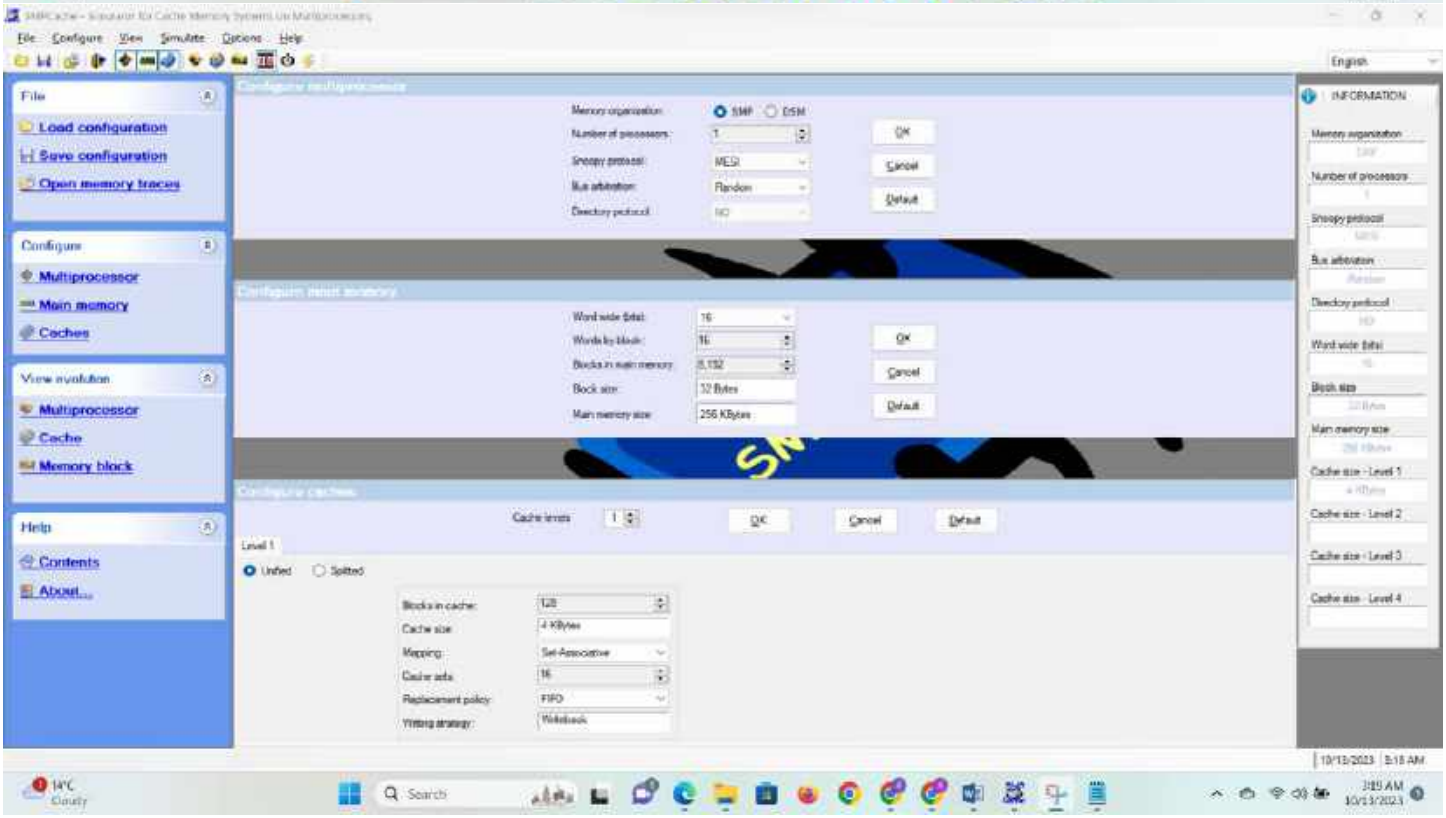
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
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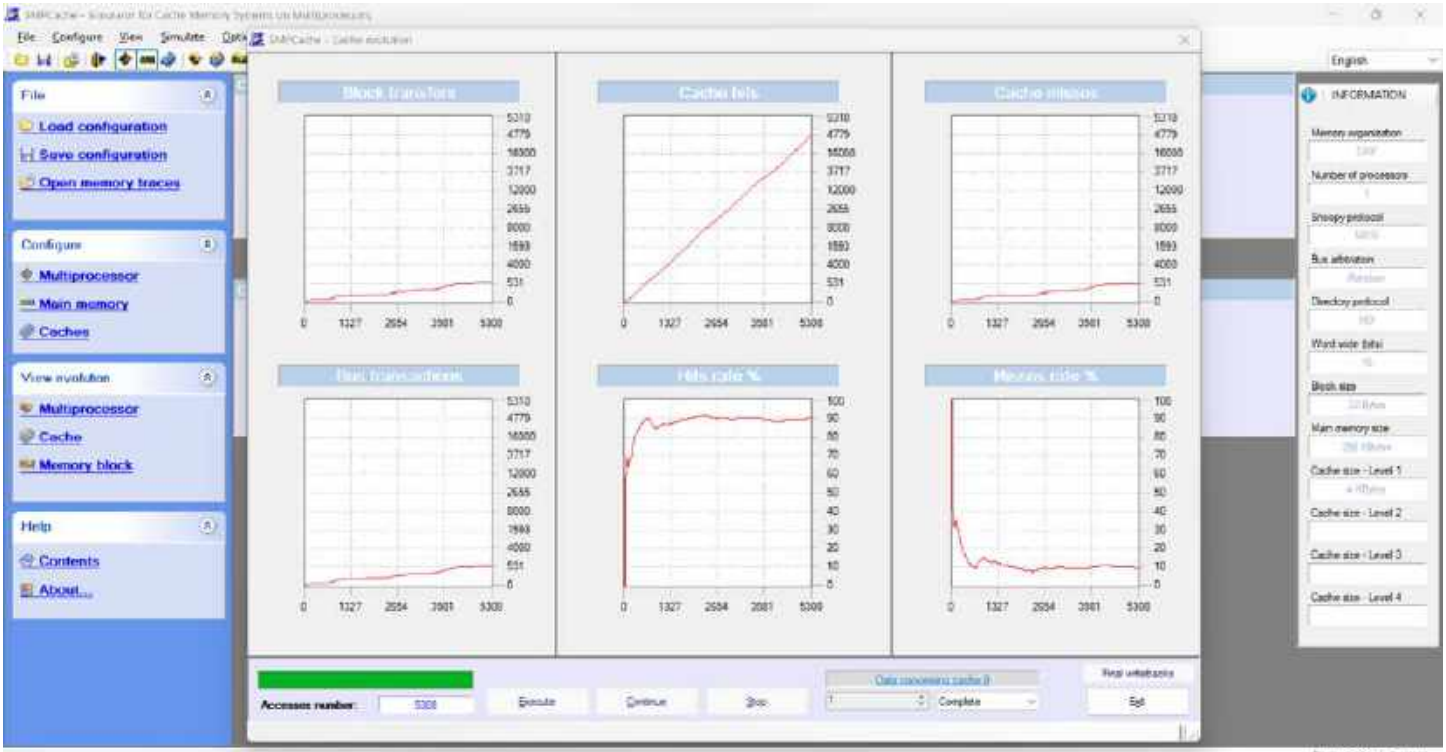
INFORMATION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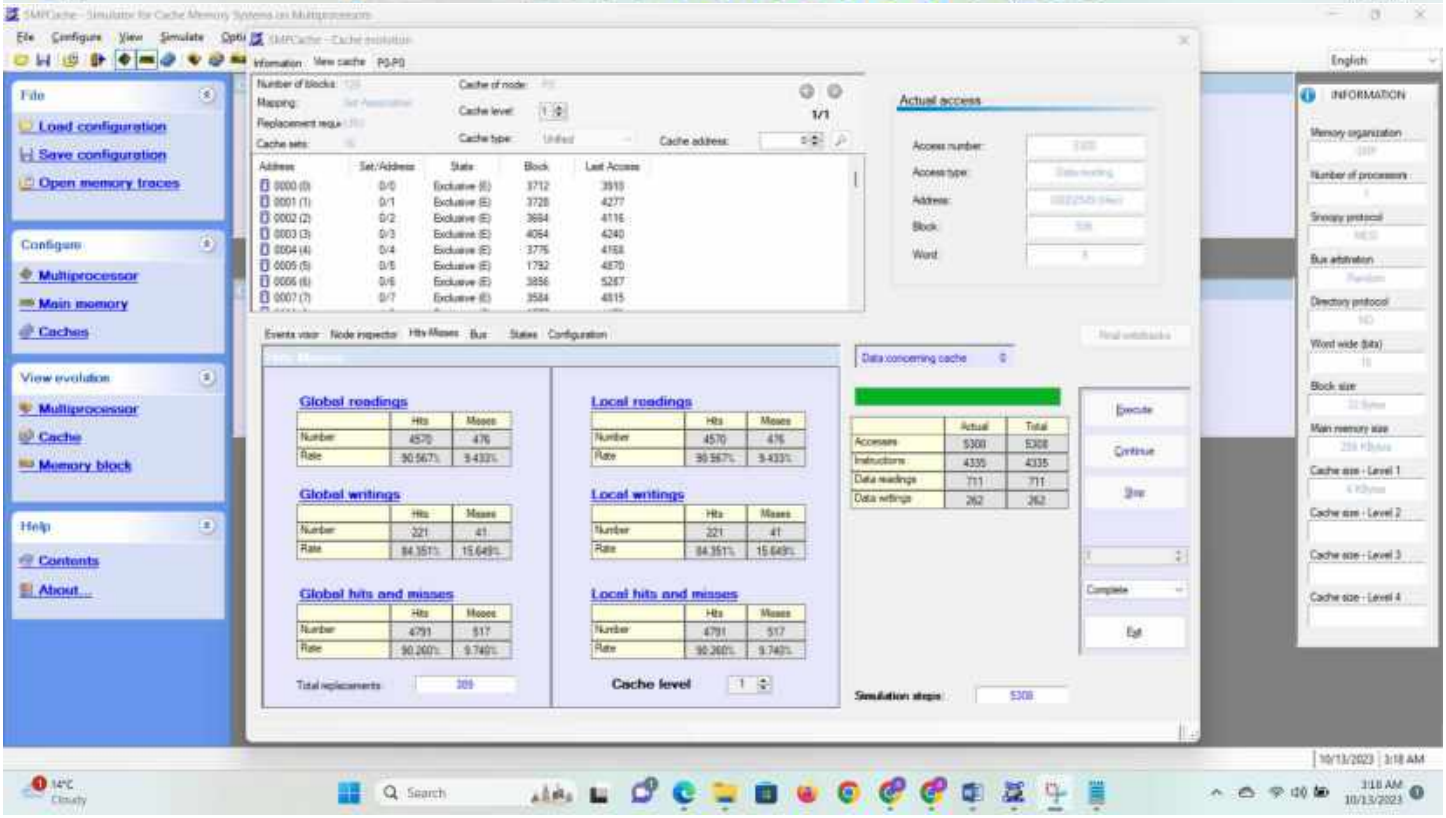
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
Execute
Continue
Stop
Complete
Exit
INFORMATION


Load configuration
Save configuration
Open memory traces
Multiprocessor
Main memory
Caches
Multiprocessor
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Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
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Execute
Continue
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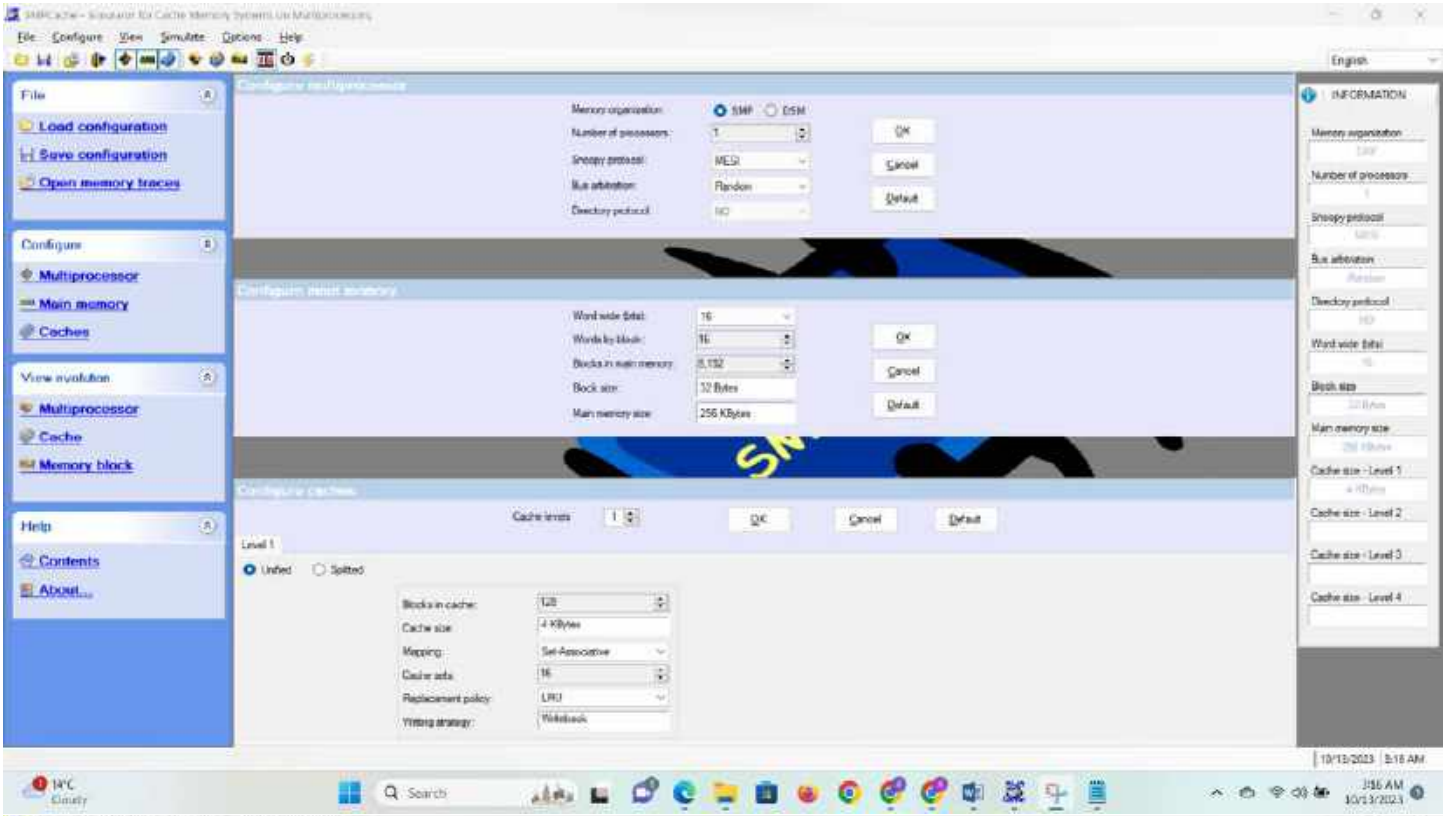
INFORMATION


File
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Save configuration
Open memory traces
Configure
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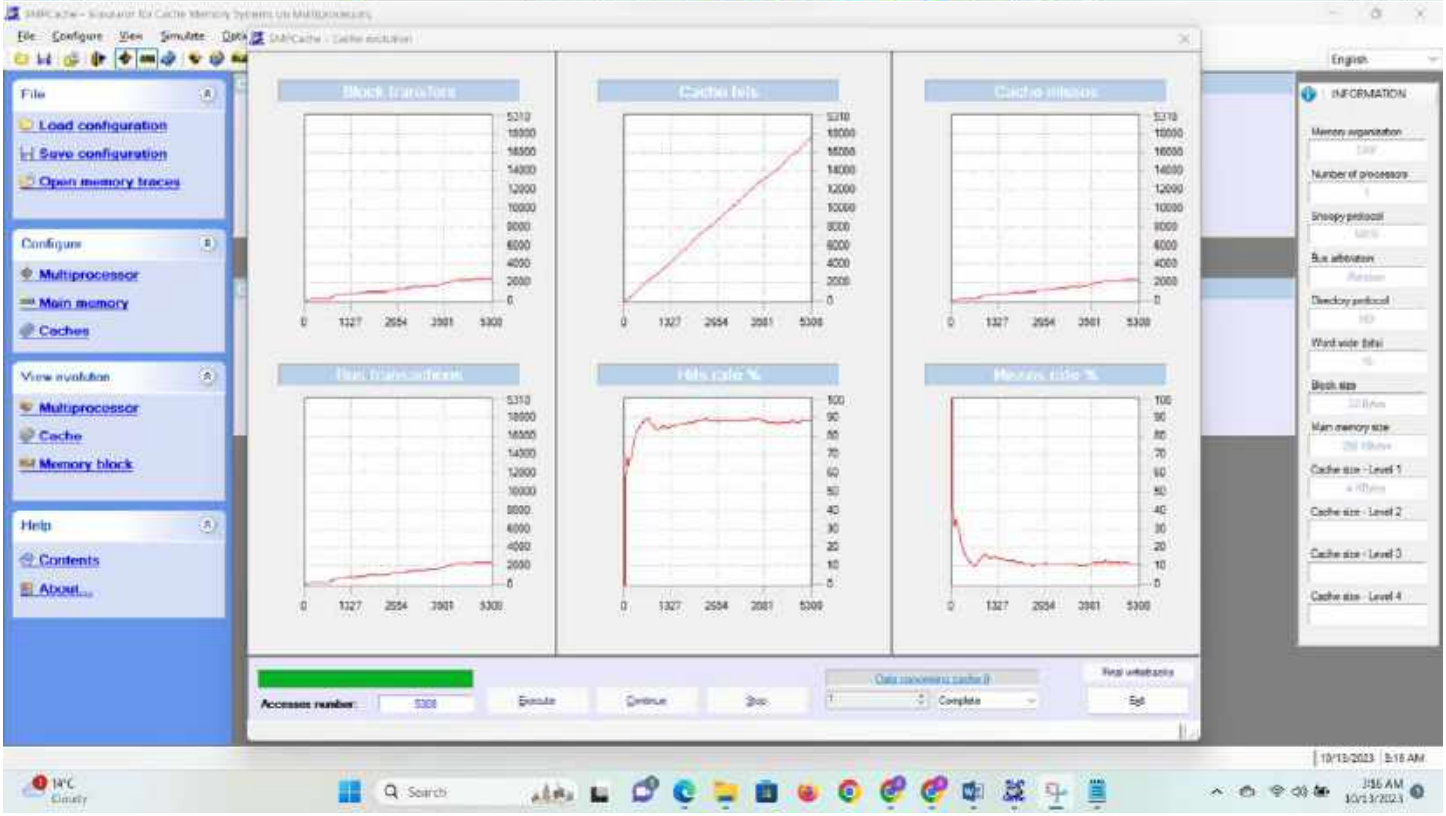
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION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Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
INFORMATION
Accesses number:
Execute
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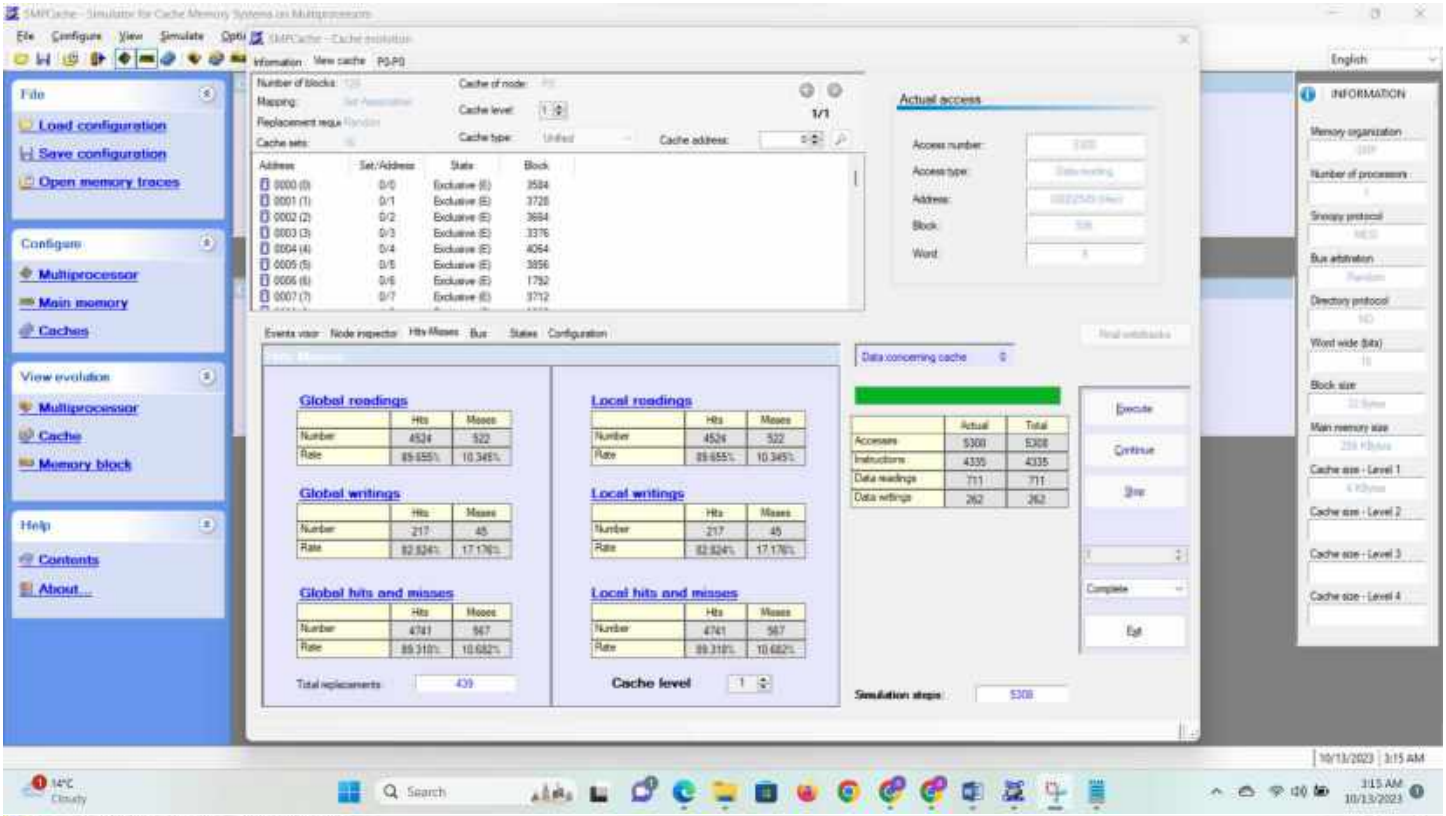
Stop
Exit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Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
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View evolution
Multiprocessor
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Memory block
Help
Contents
About...
Actual access
Global readings
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Global writings
Local writings
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Local hits and misses
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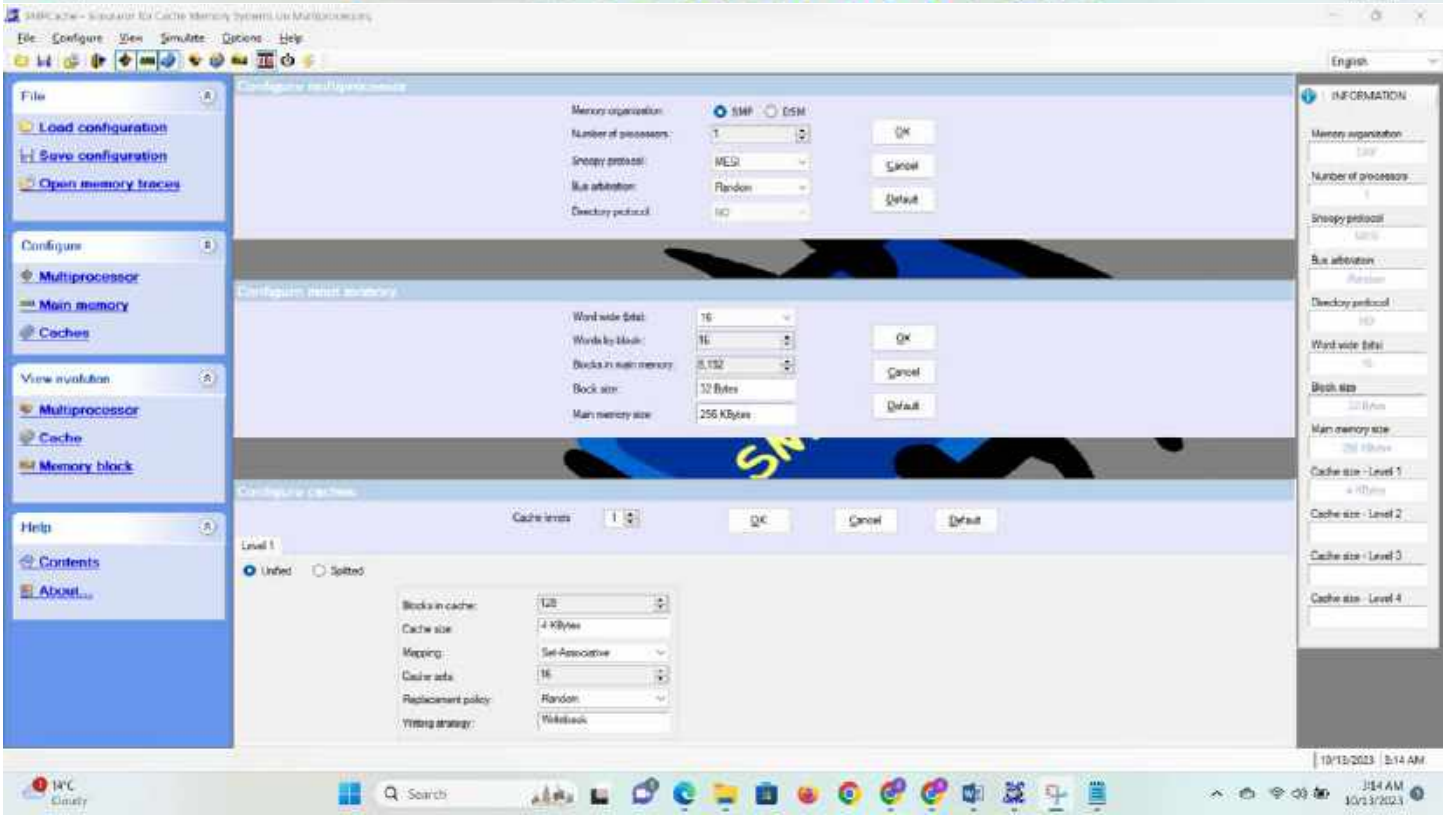
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Load configuration
Save configuration
Open memory traces
Configure
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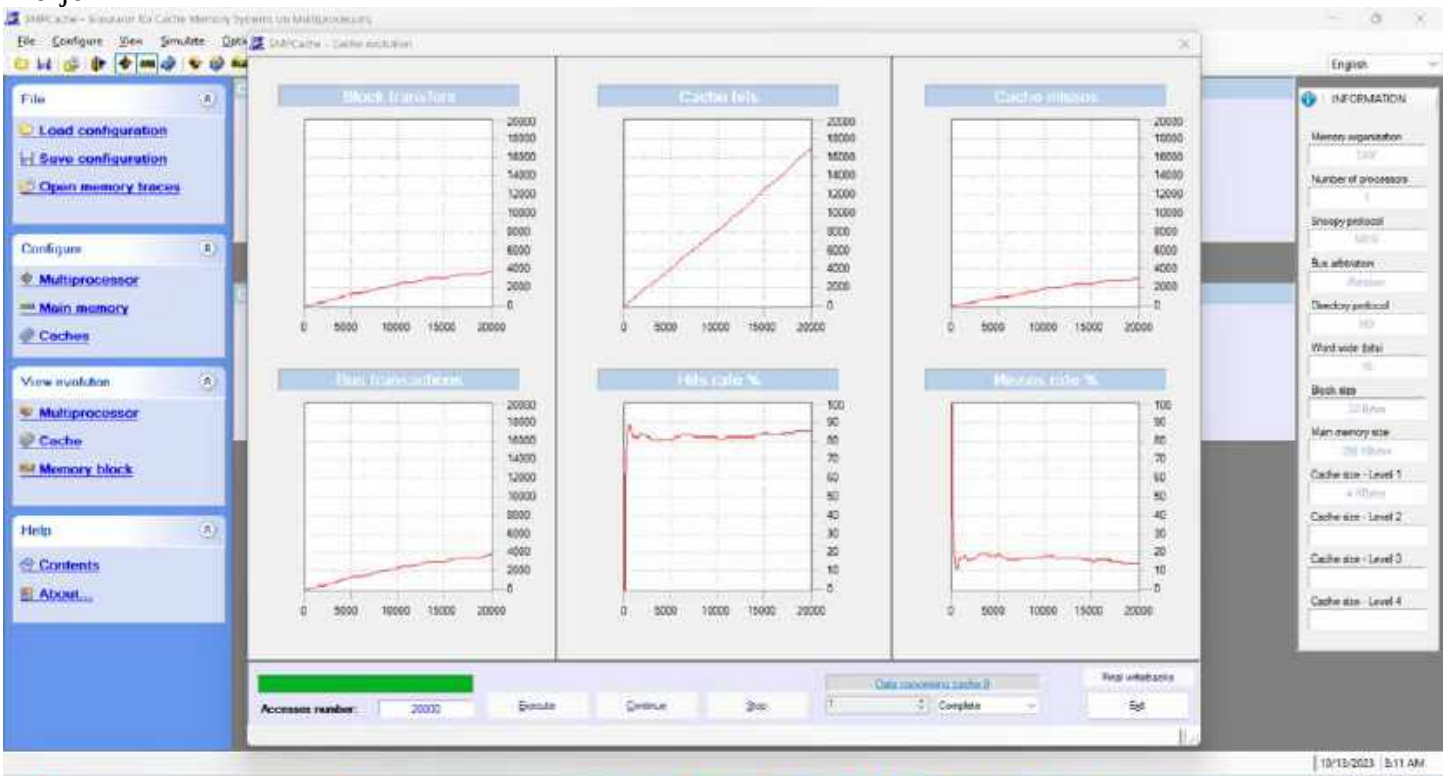
Main memory
Caches
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
OK
Cancel
Default
INFORMATION

Mdljd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Load configuration
Save configuration
Open memory traces
Configure
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View evolution
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Contents
About...
Block transfers
Cache hits
Cache misses
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Misses rate %
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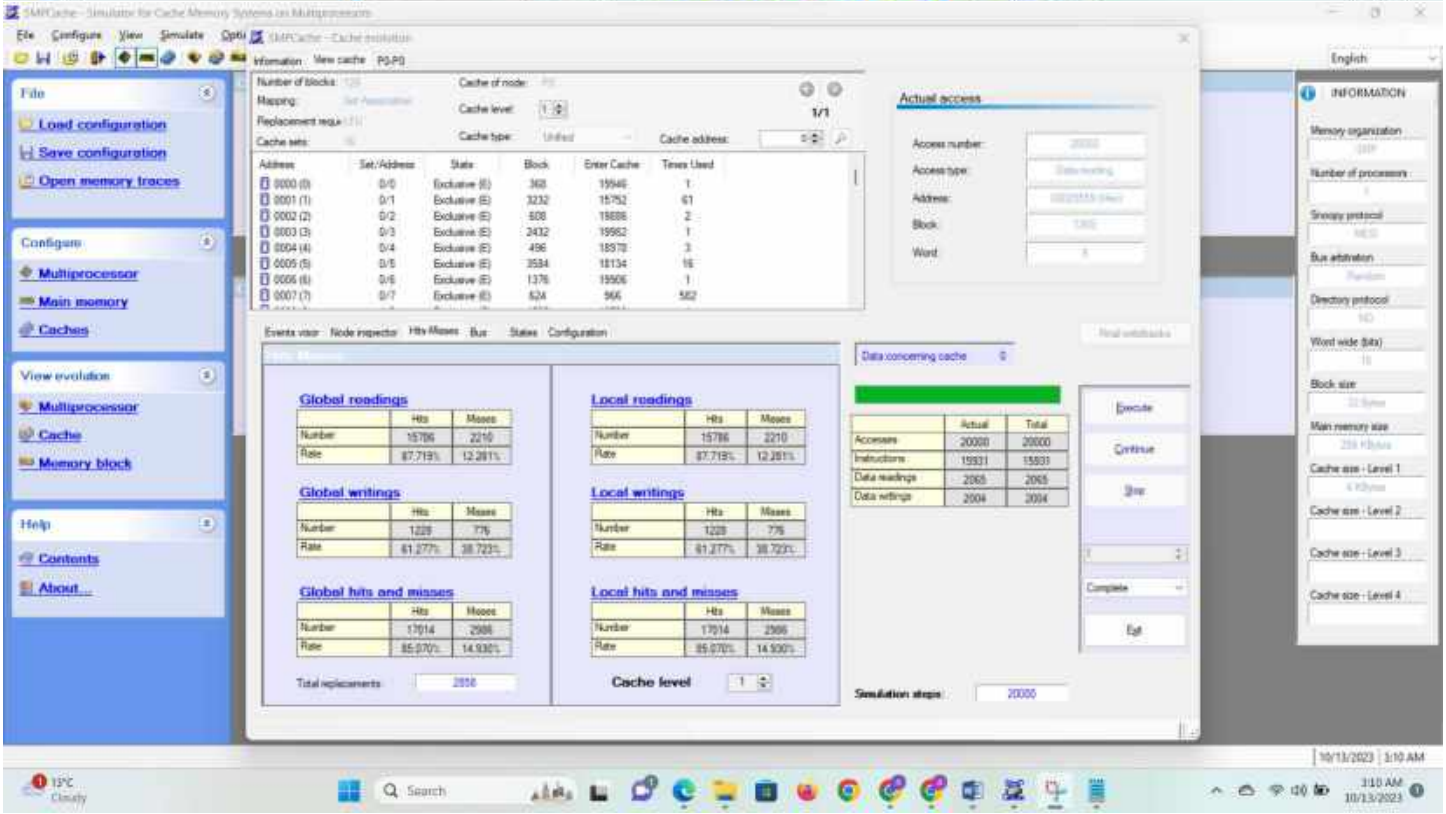
INFORMATION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Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
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Memory block
Help
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About...
Actual access
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Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
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Simulation steps:
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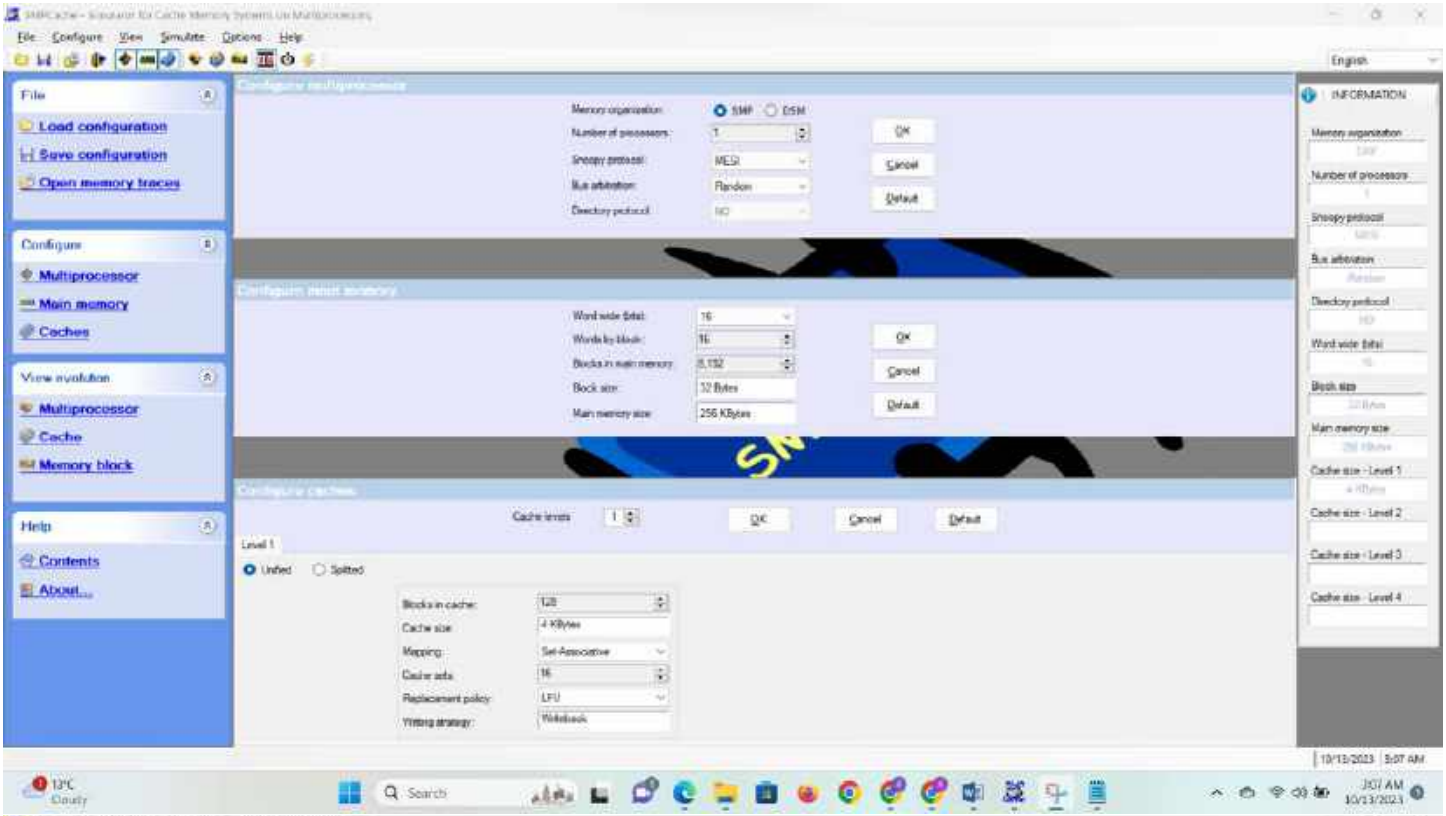
INFORMATION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Open memory traces
Configure
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Main memory
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View evolution
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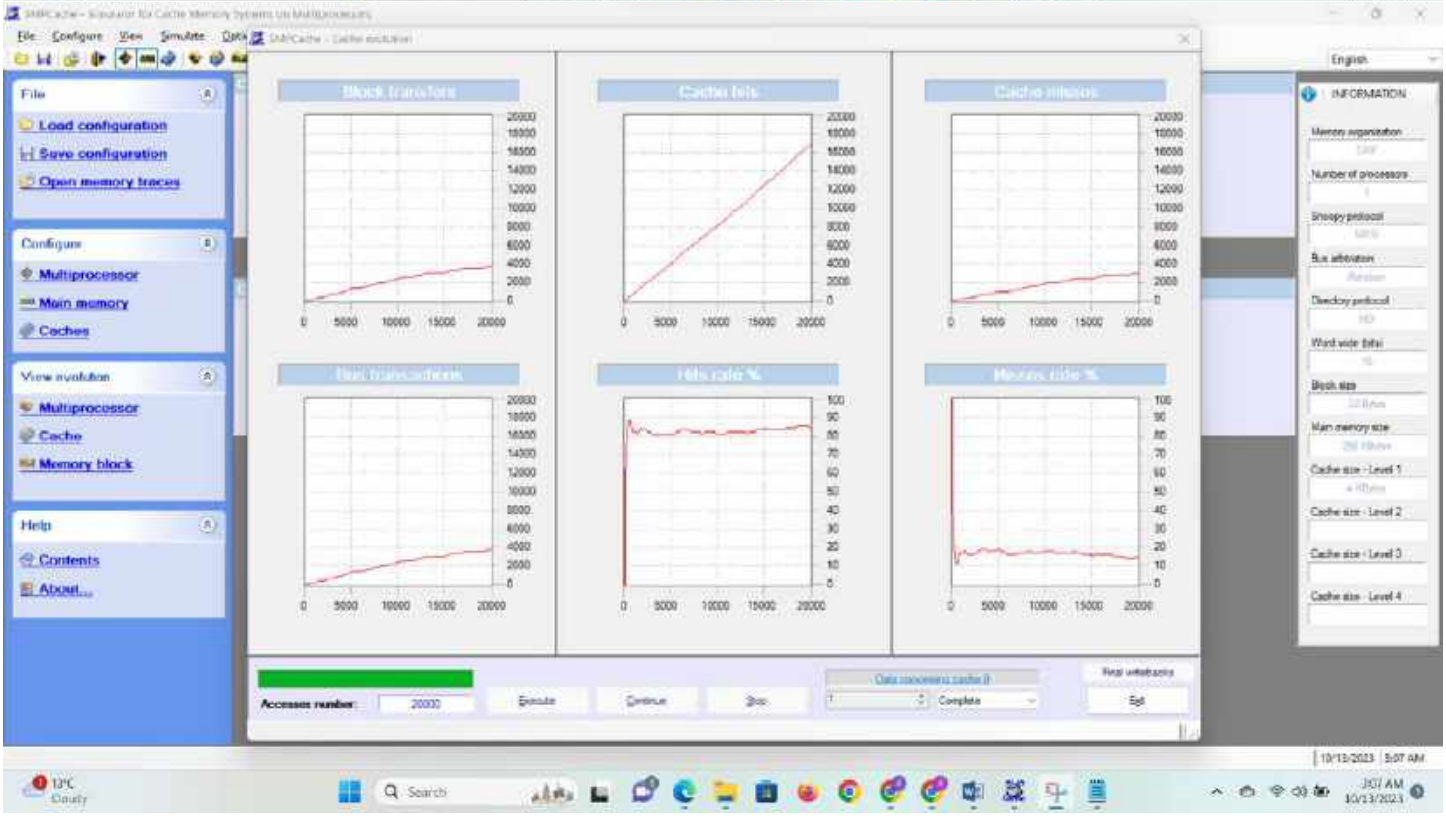
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Save configuration
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About...
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Accesses number:
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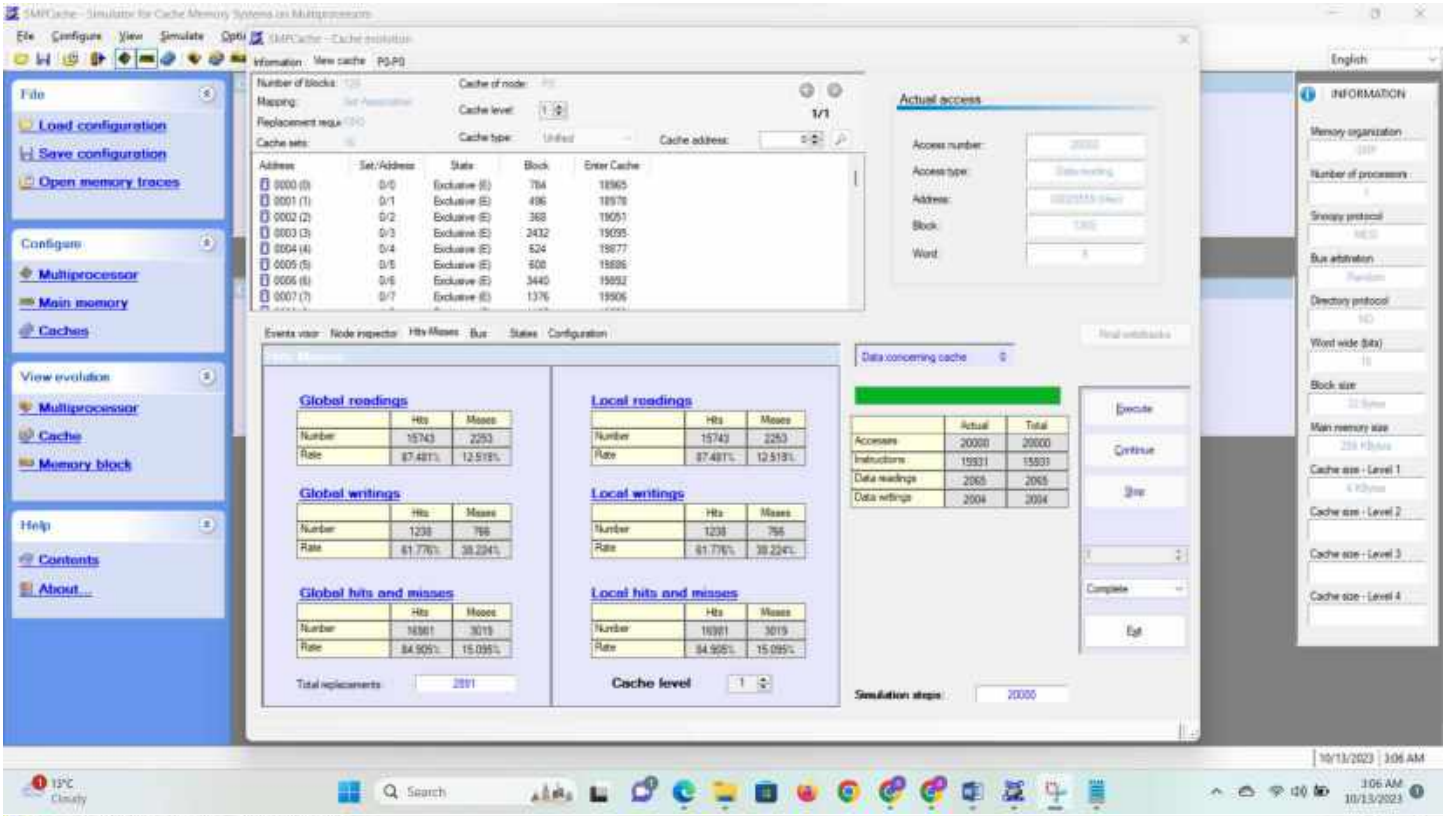
Exit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Load configuration
Save configuration
Open memory traces
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About...
Actual access
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Local hits and misses
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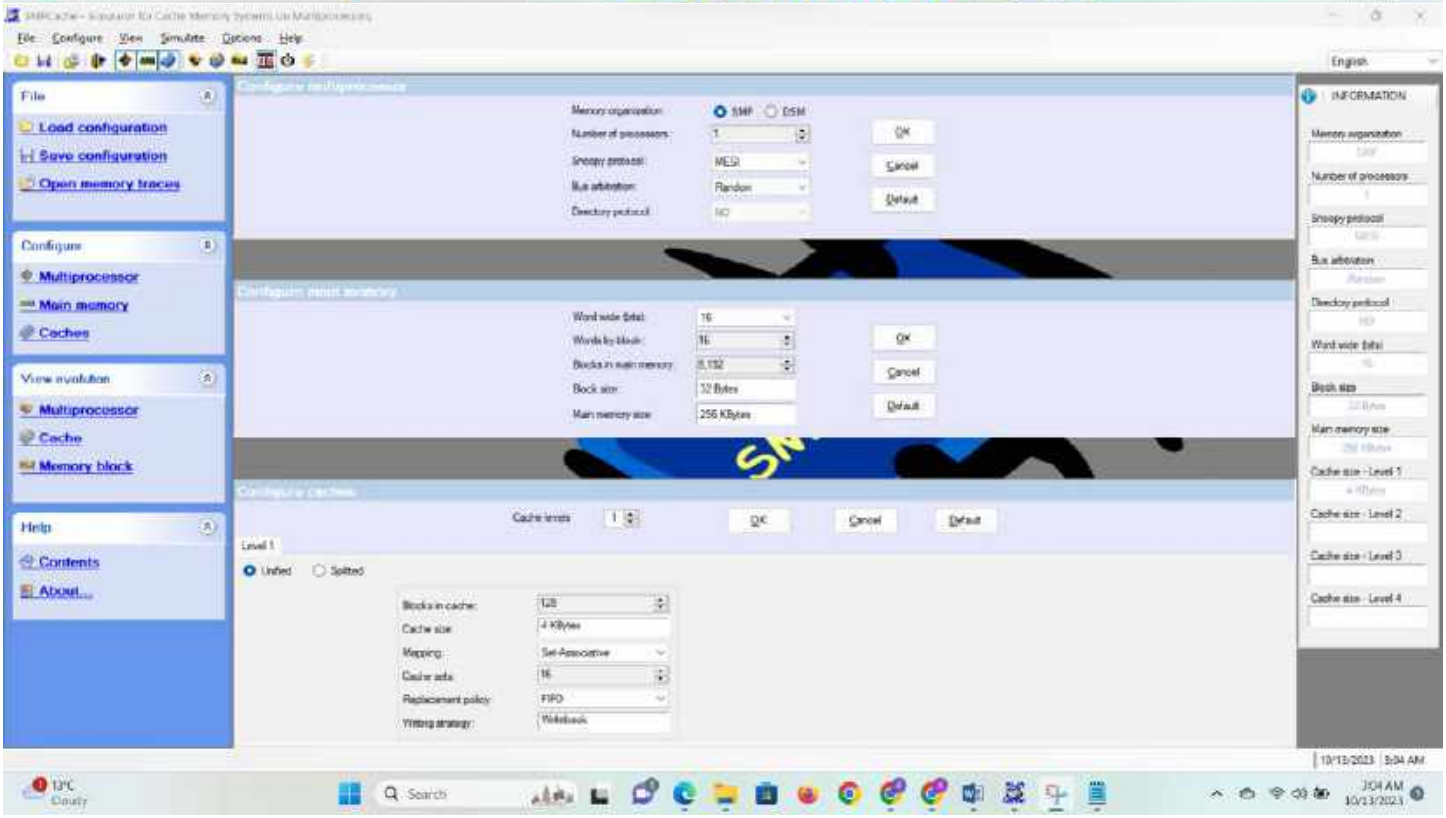
INFORMATION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Save configuration
Open memory traces
Configure
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Hits rate %
Misses rate %
Accesses number:
20000
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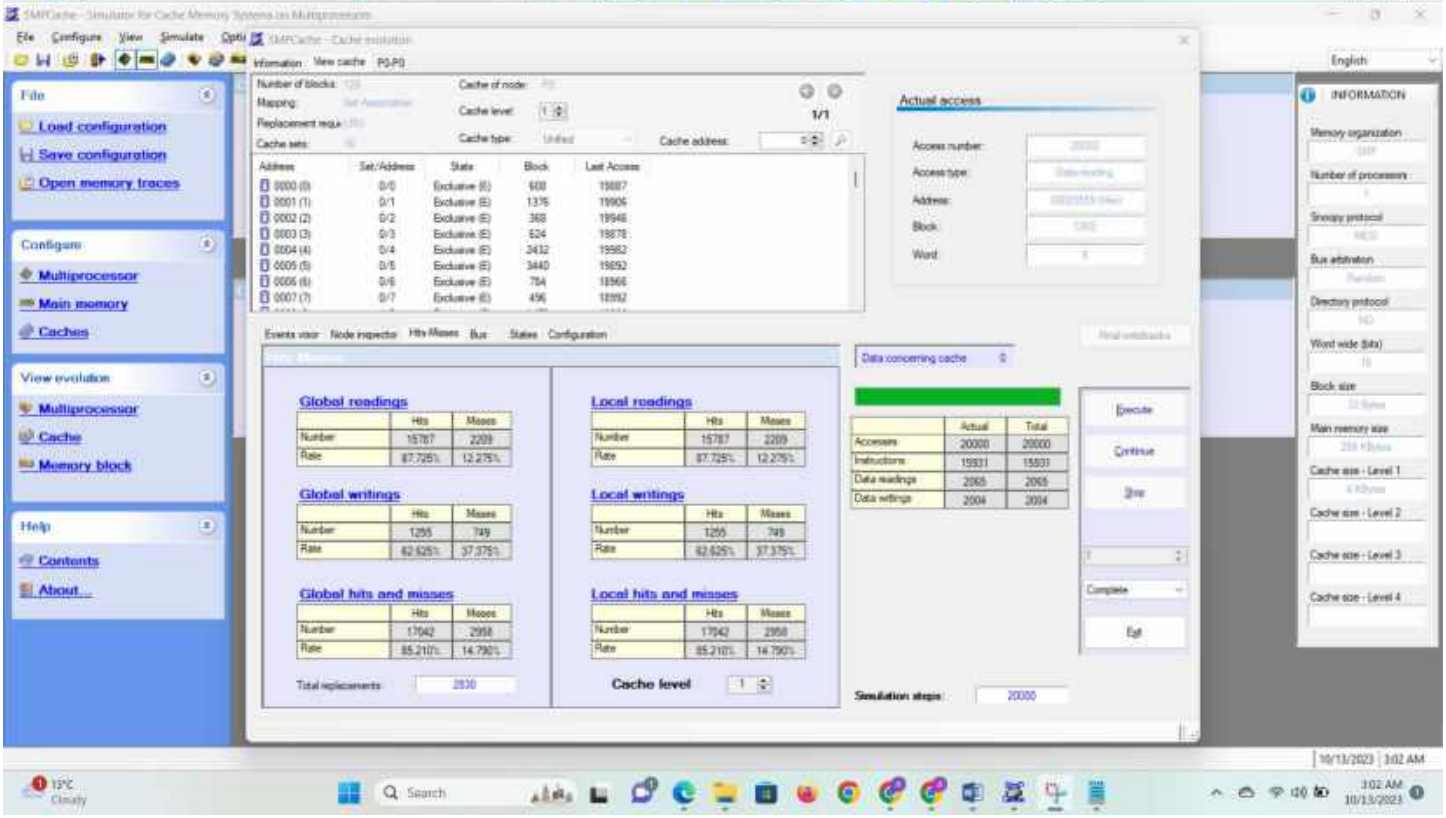
Stop
Complete
Exit
INFORMATION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About...
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Access type:
Address:
Block:
Word:
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Local writings
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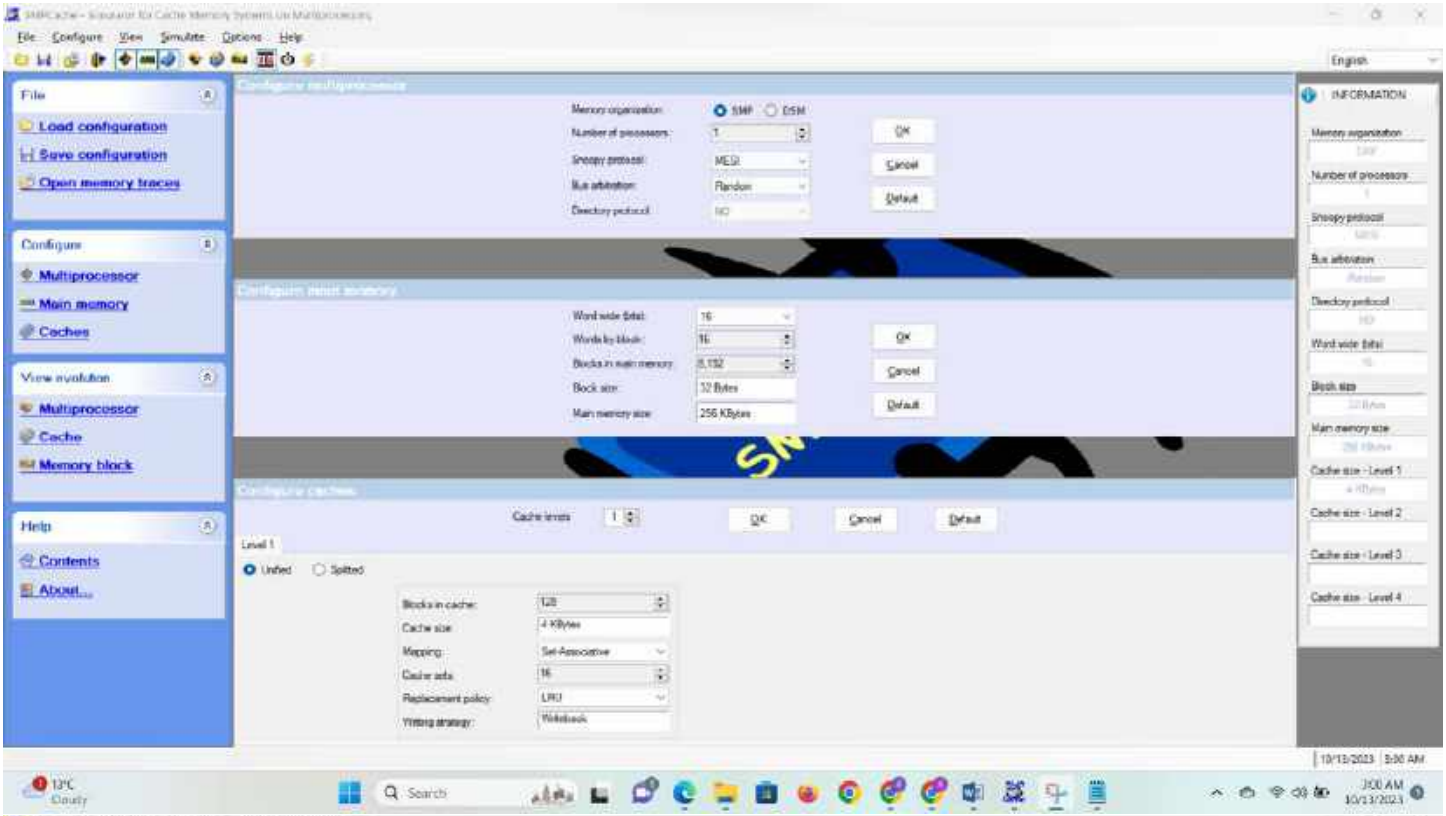
INFORMATION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Save configuration
Open memory traces
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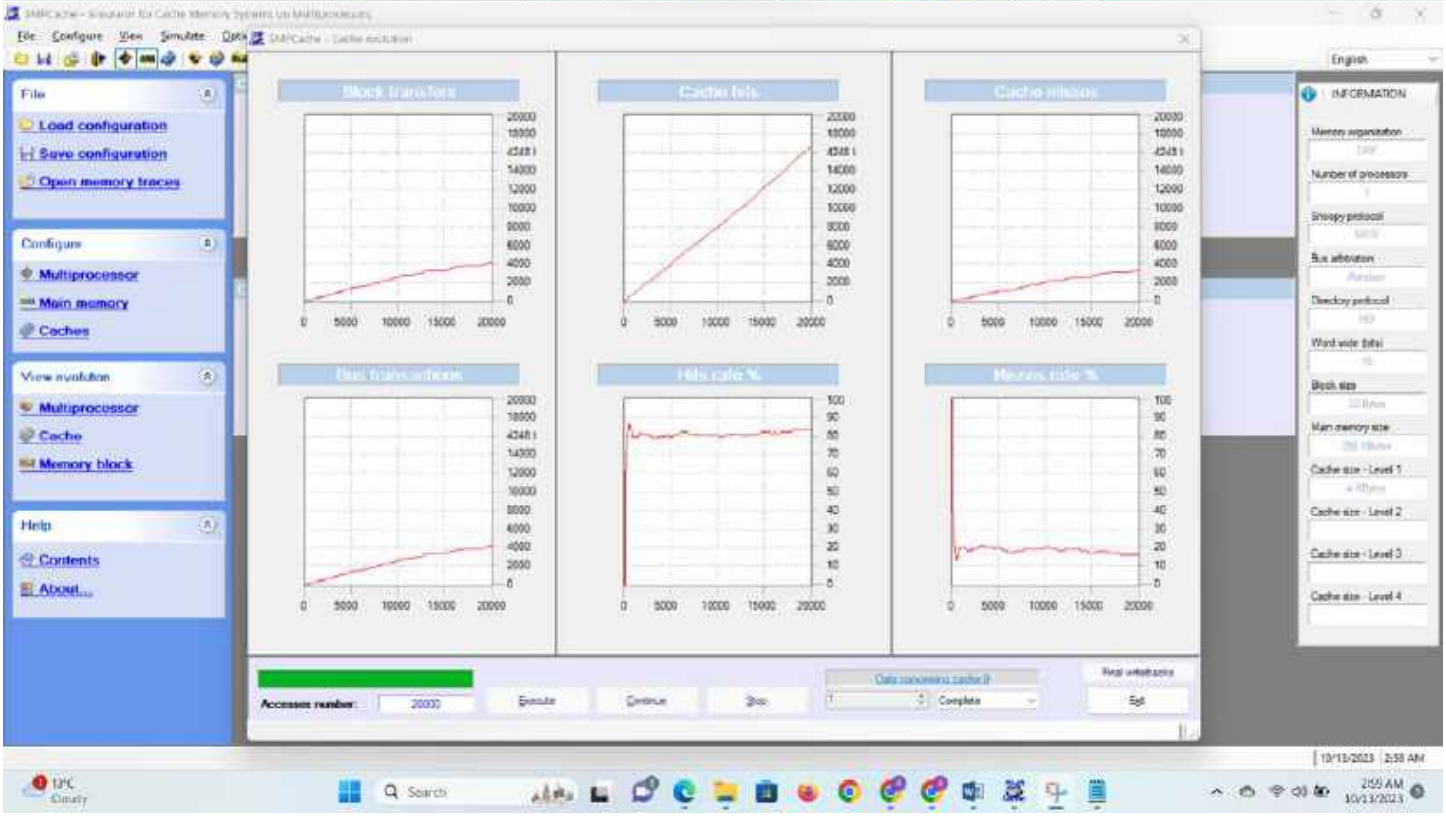
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Save configuration
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Contents
About...
INFORMATION
Accesses number:
20000
Execute
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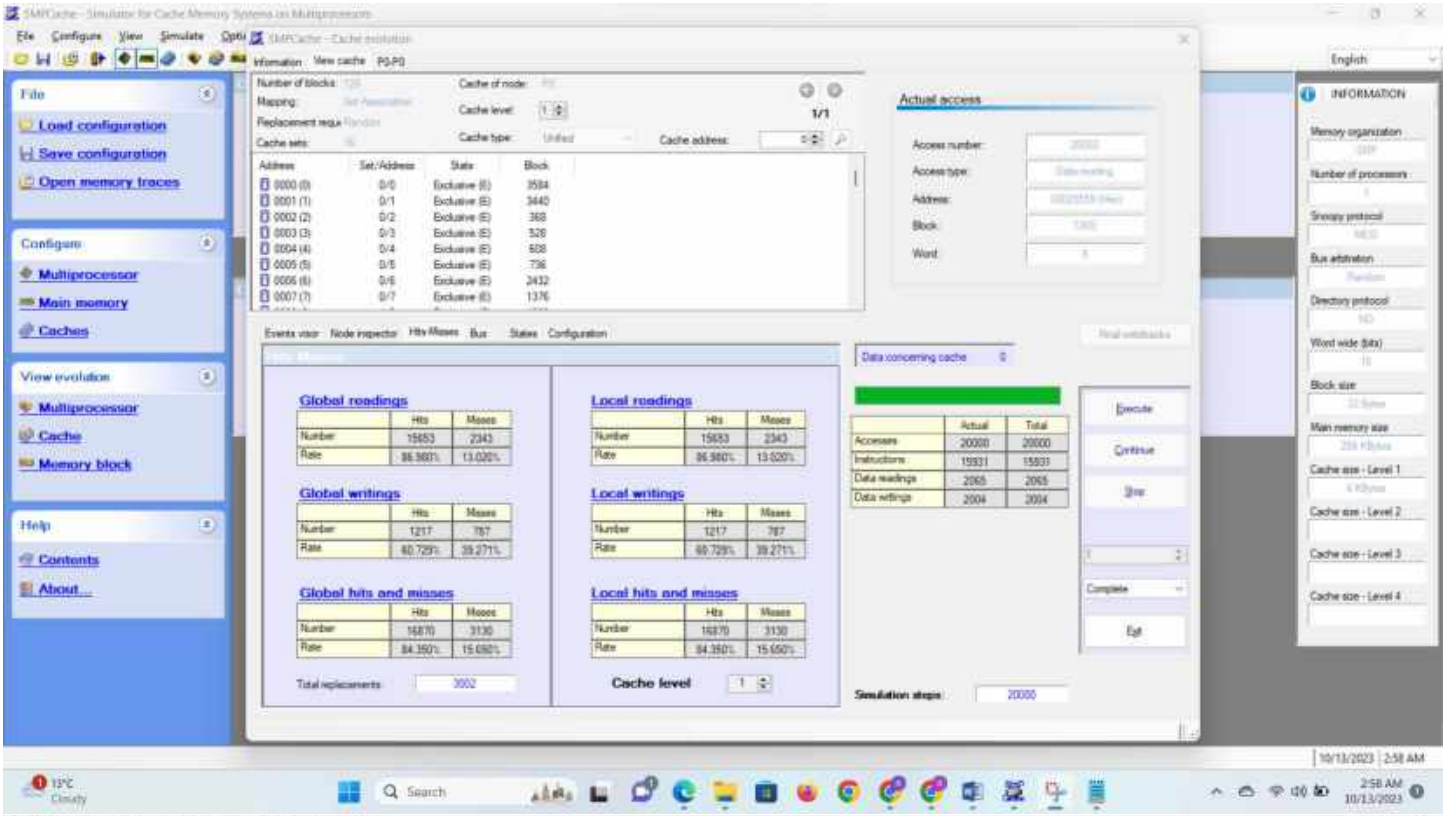
Stop
Exit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Save configuration
Open memory traces
Configure
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About...
Actual access
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Local readings
Global writings
Local writings
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Local hits and misses
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Continue
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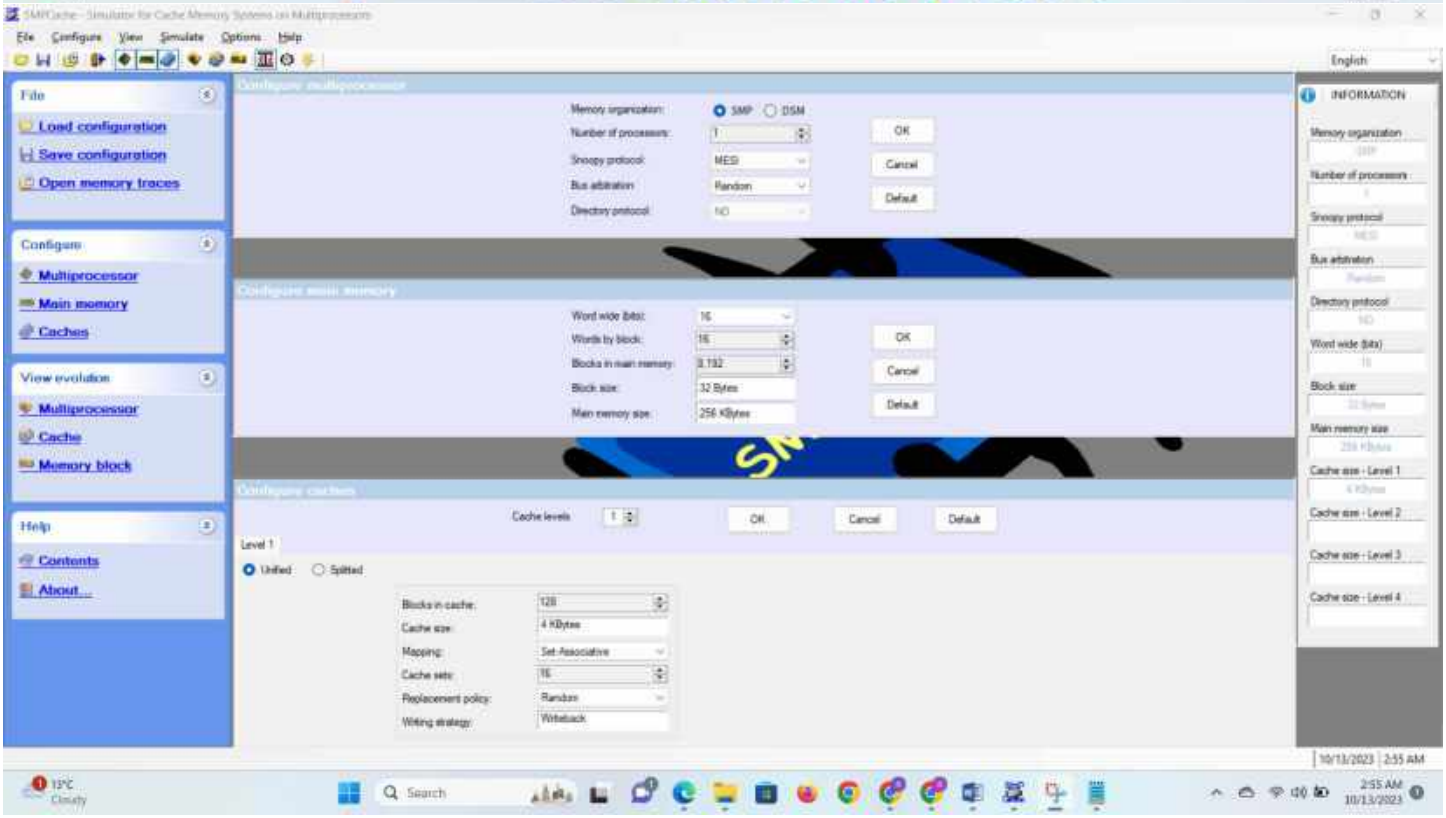
INFORMATION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Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
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View evolution
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About...
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DSM
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MESI
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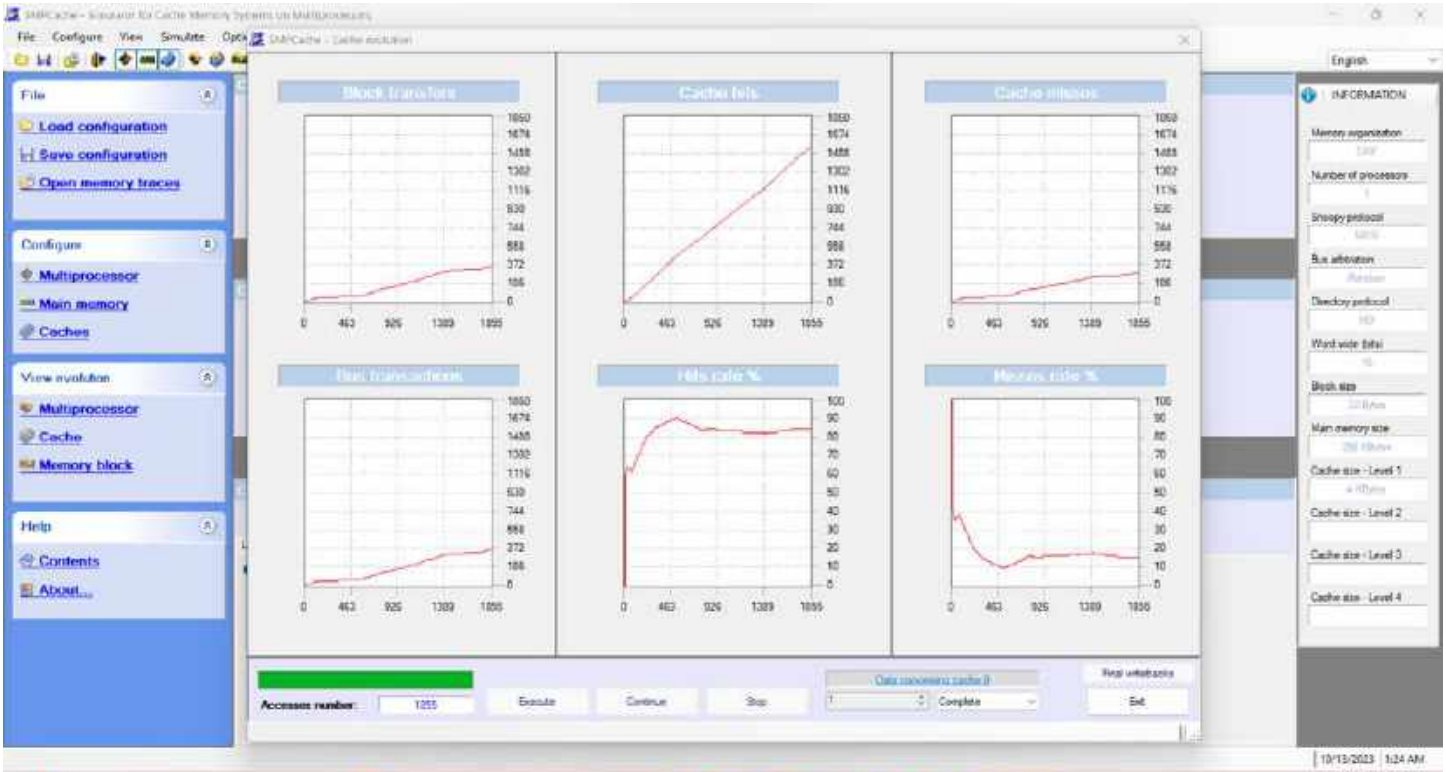
Splitted
Blocks in cache
128
Cache size
4 KBytes
Mapping
Set-Associative
Cache sets
16
Replacement policy
Random
Writing strategy
Writeback
INFORMATION

Nasa


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
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View evolution
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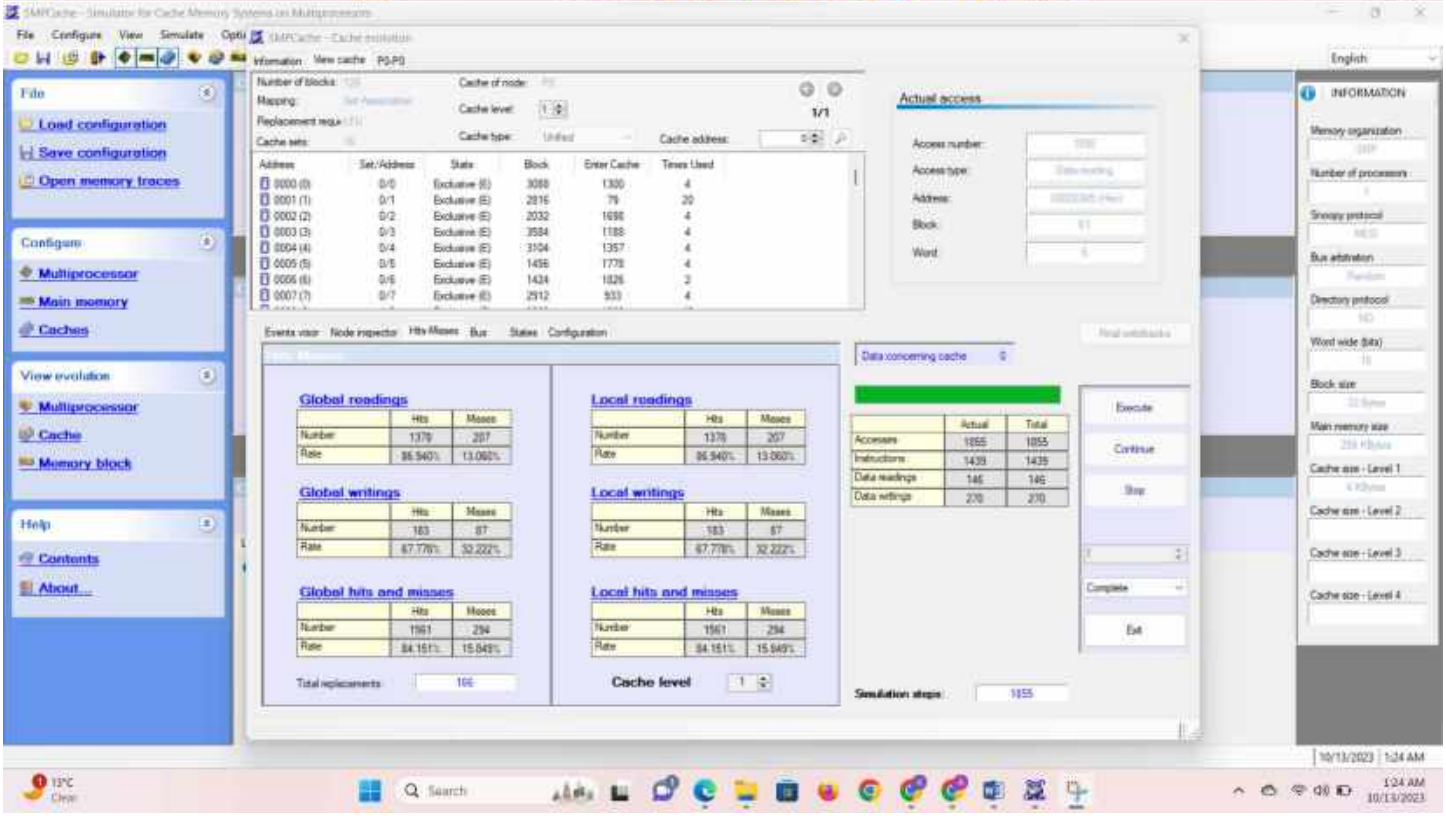
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Hits rate %
Misses rate %
Accesses number:
Execute
Continue
Stop
Exit
INFORMATION


File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
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View evolution
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Help
Contents
About...
Actual access
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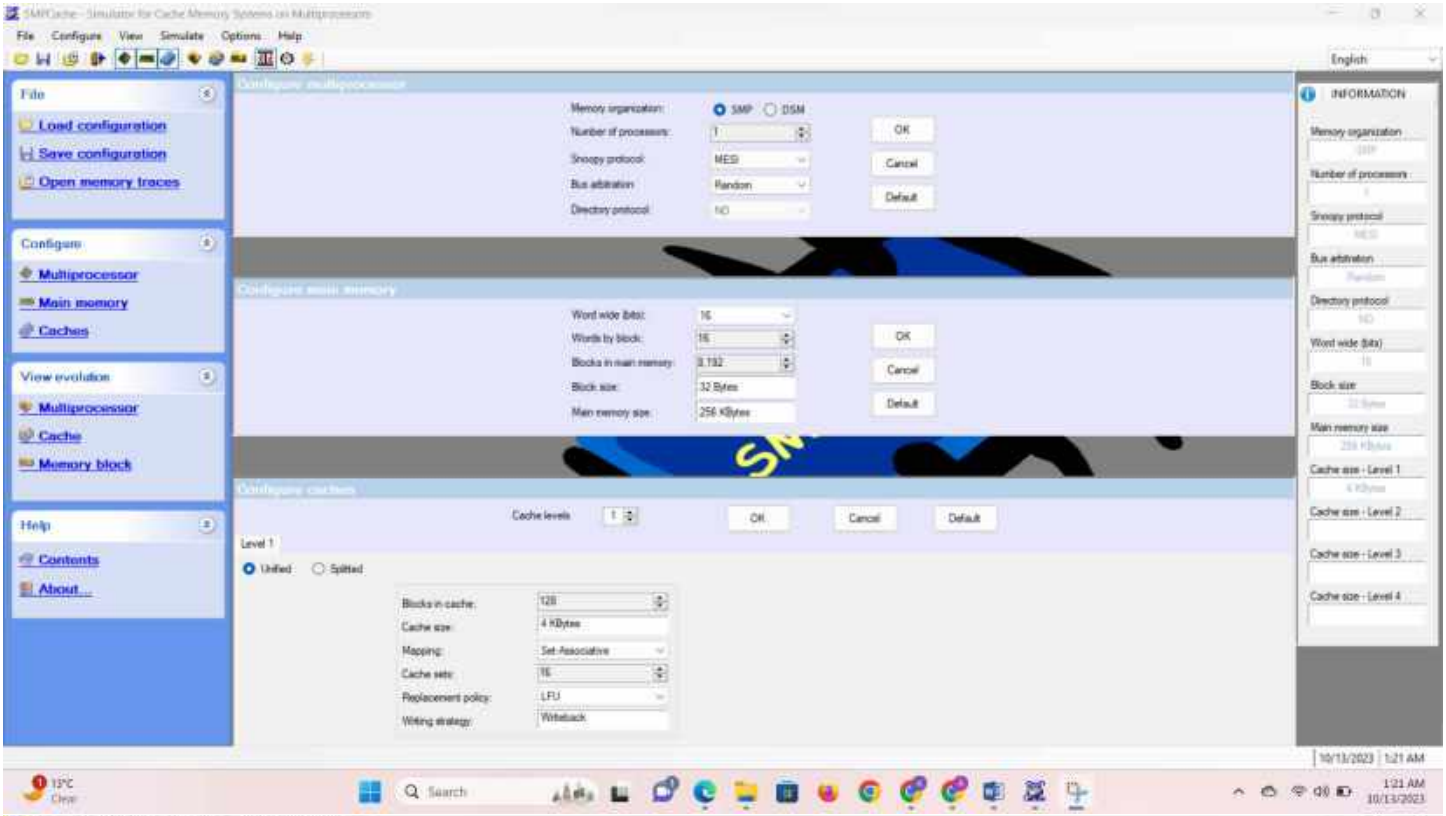
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION


File
Configure
View
Simulate
Options
Help
English
File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
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Memory organization:
SMP
DSM
Number of processors:
Snoopy protocol:
MESI
Bus arbitration:
Random
Directory protocol:
NO
OK
Cancel
Default
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8.192
Block size:
32 Bytes
Main memory size:
256 KBytes
Cache levels
Level 1
Unified
Splitted
Blocks in cache:
128
Cache size:
4 KBytes
Mapping:
Set-Associative
Cache sets:
16
Replacement policy:
LFU
Writing strategy:
Writeback
INFORMATION
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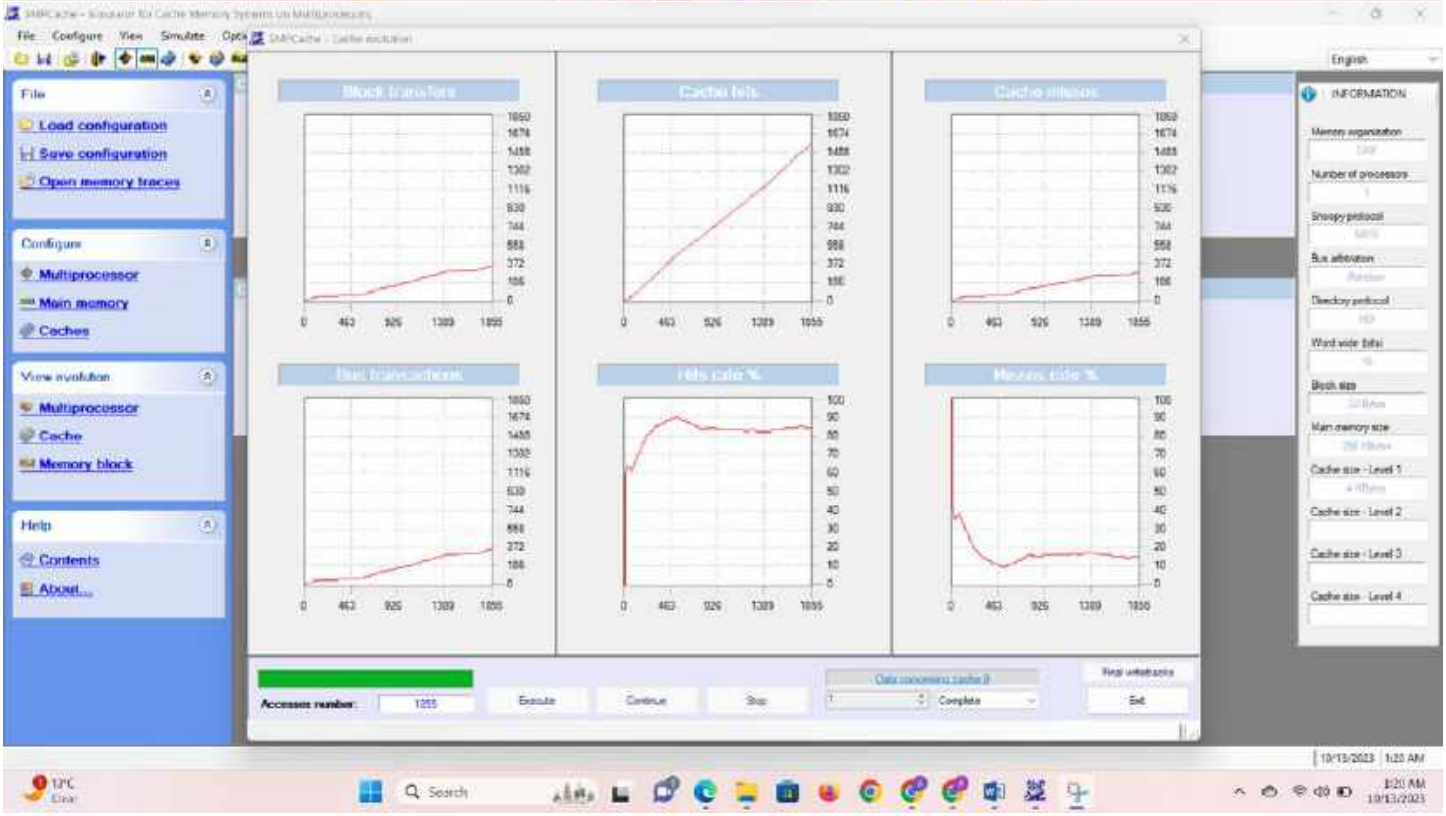
Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
10/13/2023 1:21 AM


File
Configure
View
Simulate
English
File
Load configuration
Save configuration
Open memory traces
Configure
Multiprocessor
Main memory
Caches
View evolution
Multiprocessor
Cache
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Cache fails
Cache misses
Bus transactions
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Misses cache %
0
463
926
1389
1855
Accesses number:
1855
Execute
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Complete
Exit
INFORMATION
Memory organization
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Snoopy protocol
Bus arbitration
Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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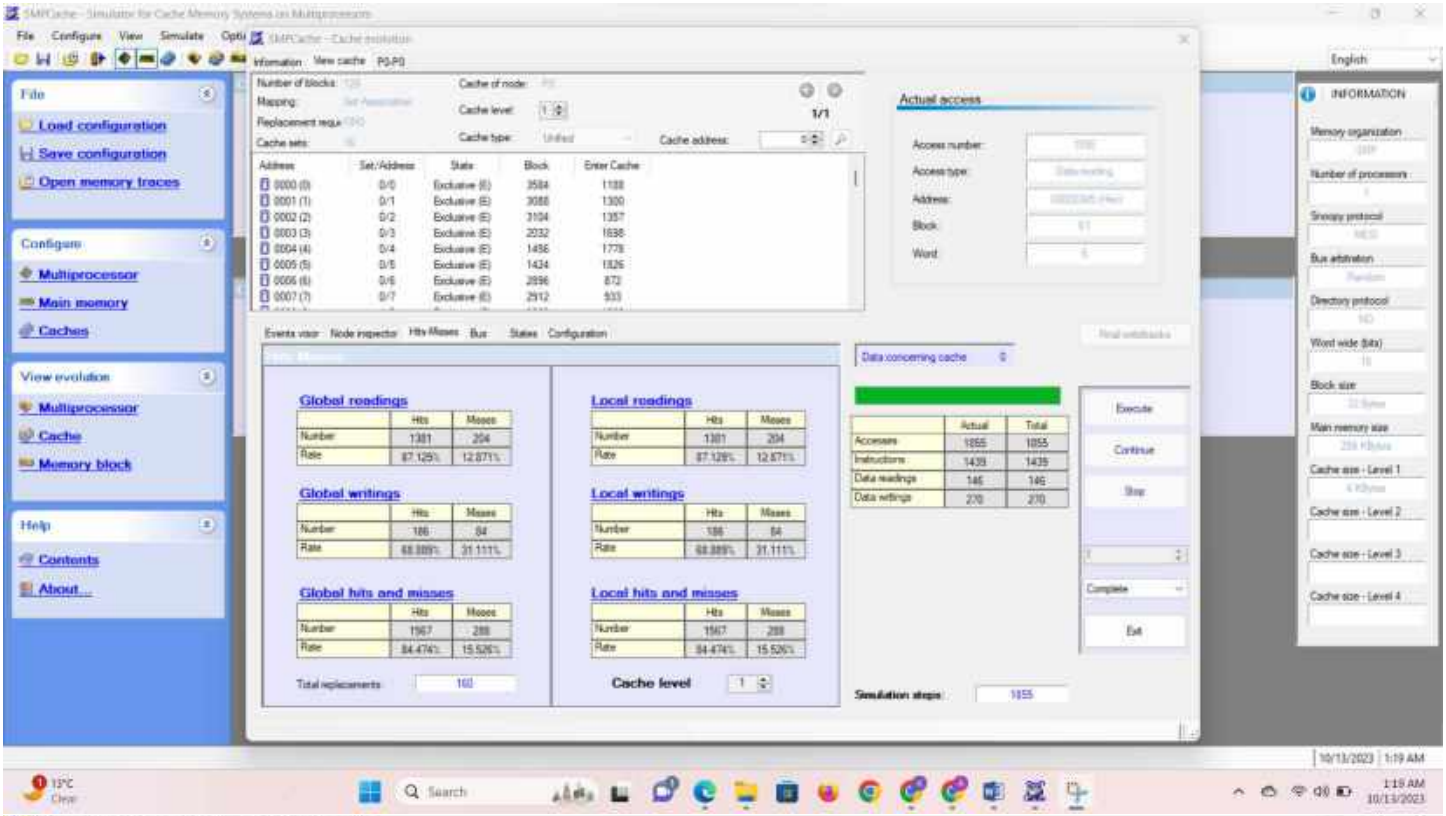
File
Load configuration
Save configuration
Open memory traces
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Multiprocessor
Main memory
Caches
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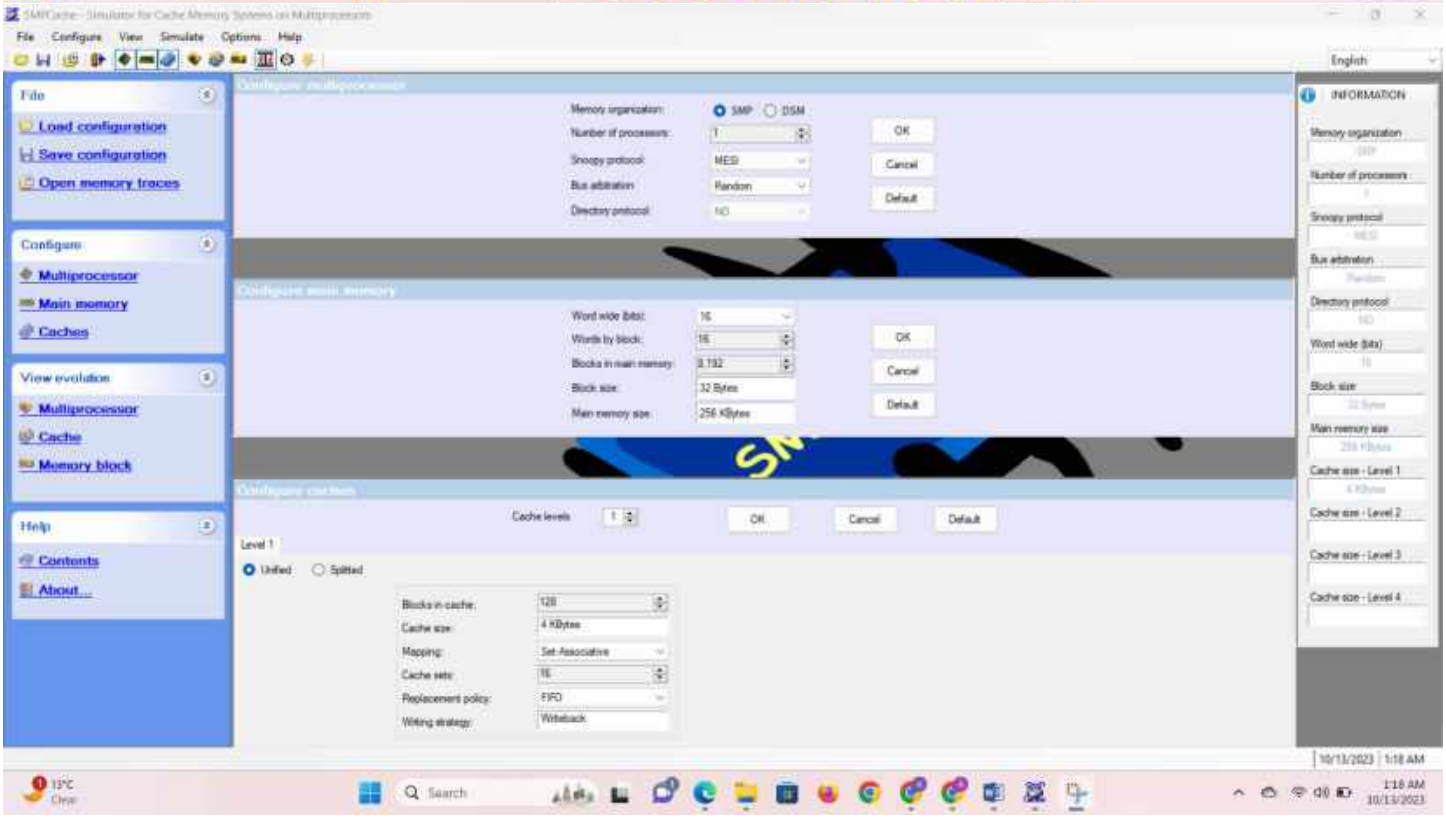
Help
Contents
About...
Actual access
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Execute
Continue
Stop
Exit
INFORMATION


File
Load configuration
Save configuration
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Memory block
Help
Contents
About...
Memory organization
SMP
DSM
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Snoopy protocol
MESI
Bus arbitration
Random
Directory protocol
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Cancel
Default
Word wide (bits)
Words by block
Blocks in main memory
Block size
32 Bytes
Main memory size
256 KBytes
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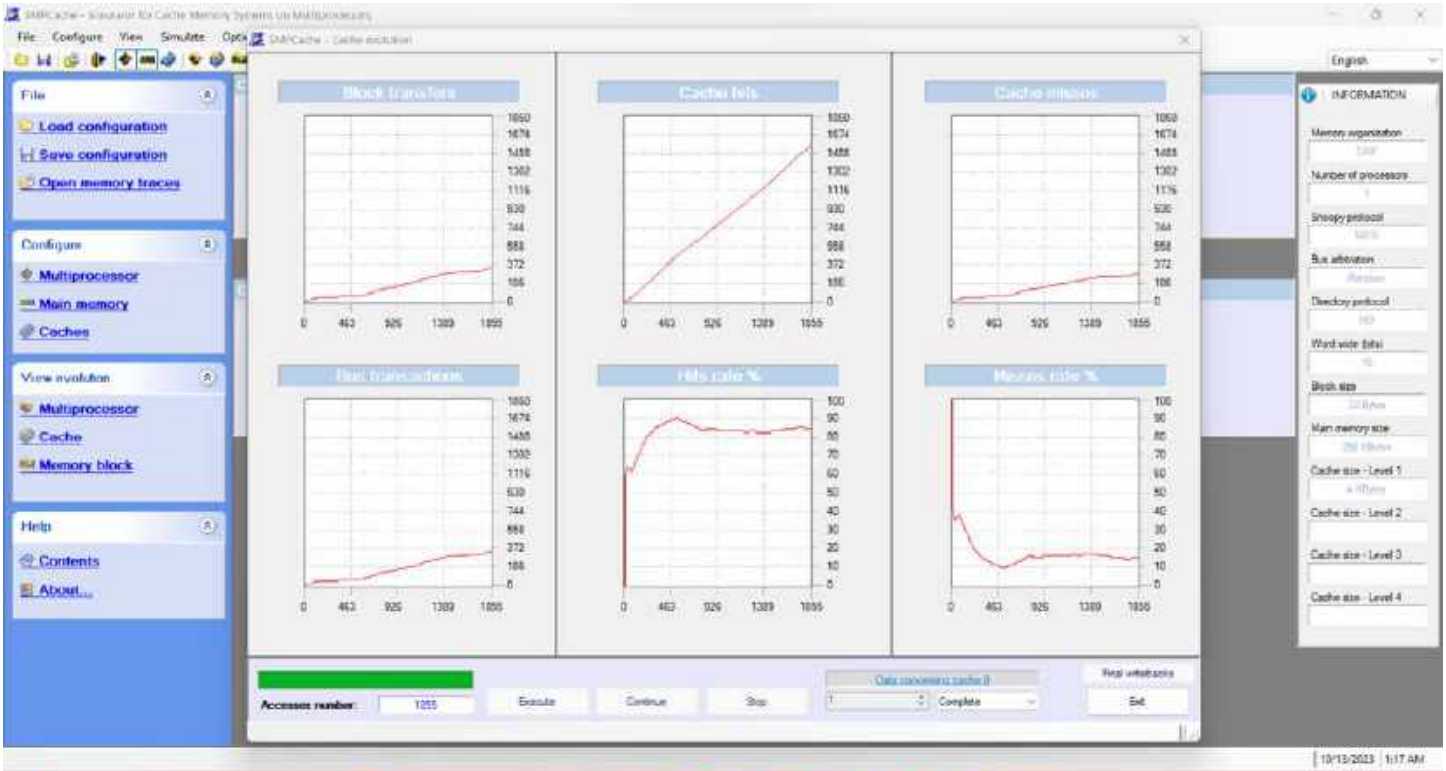
Level 1
Unified
Splitted
Blocks in cache
128
Cache size
4 KBytes
Mapping
Set-Associative
Cache sets
16
Replacement policy
FIFO
Writing strategy
Writeback
INFORMATION


File
Load configuration
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Open memory traces
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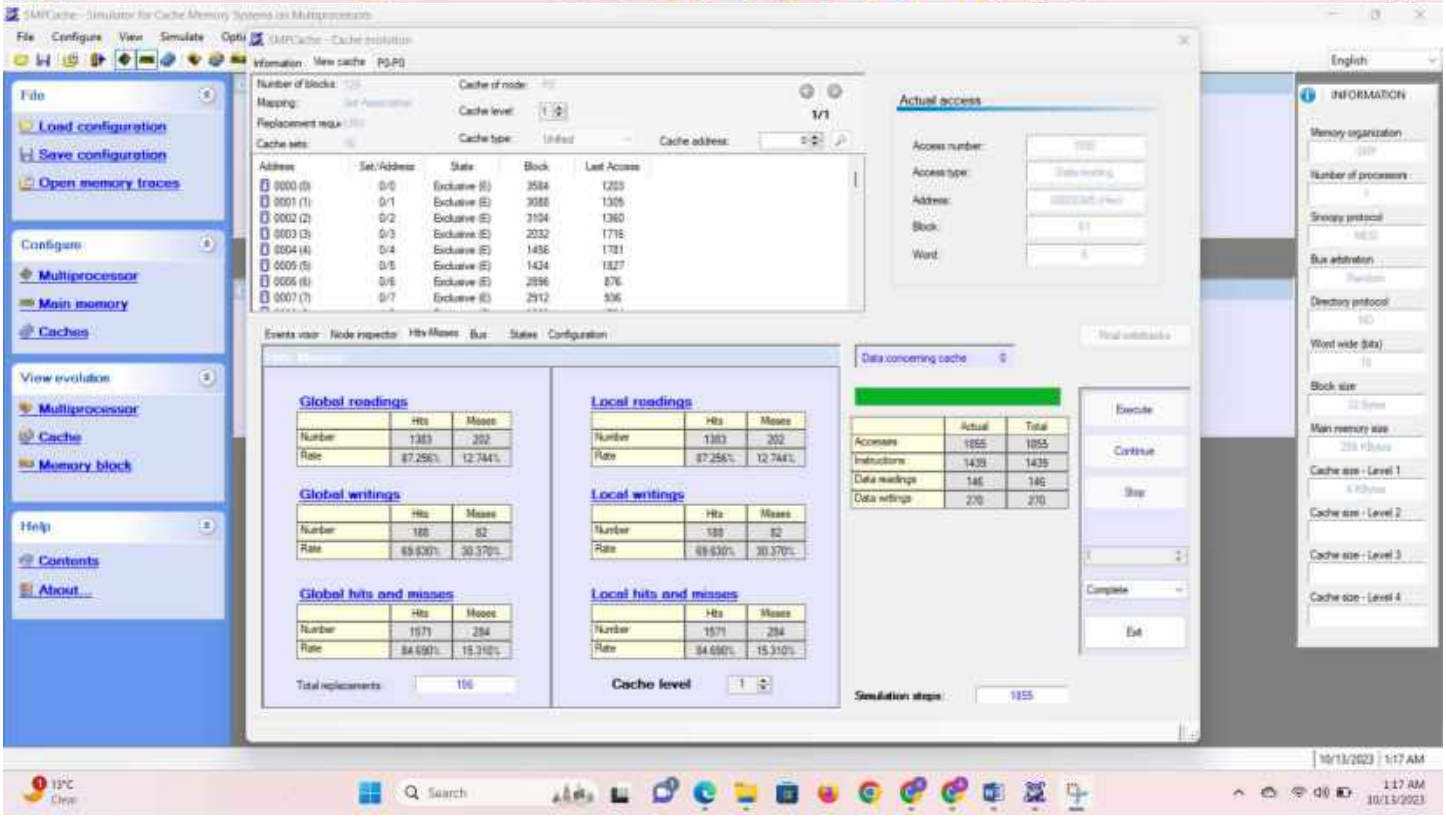
View evolution
Multiprocessor
Cache
Memory block
Help
Contents
About...
Block transfers
Cache hits
Cache misses
Bus transactions
Hits rate %
Misses rate %
Accesses number:
1055
Execute
Continue
Stop
Complete
Exit
INFORMATION
English


File
Load configuration
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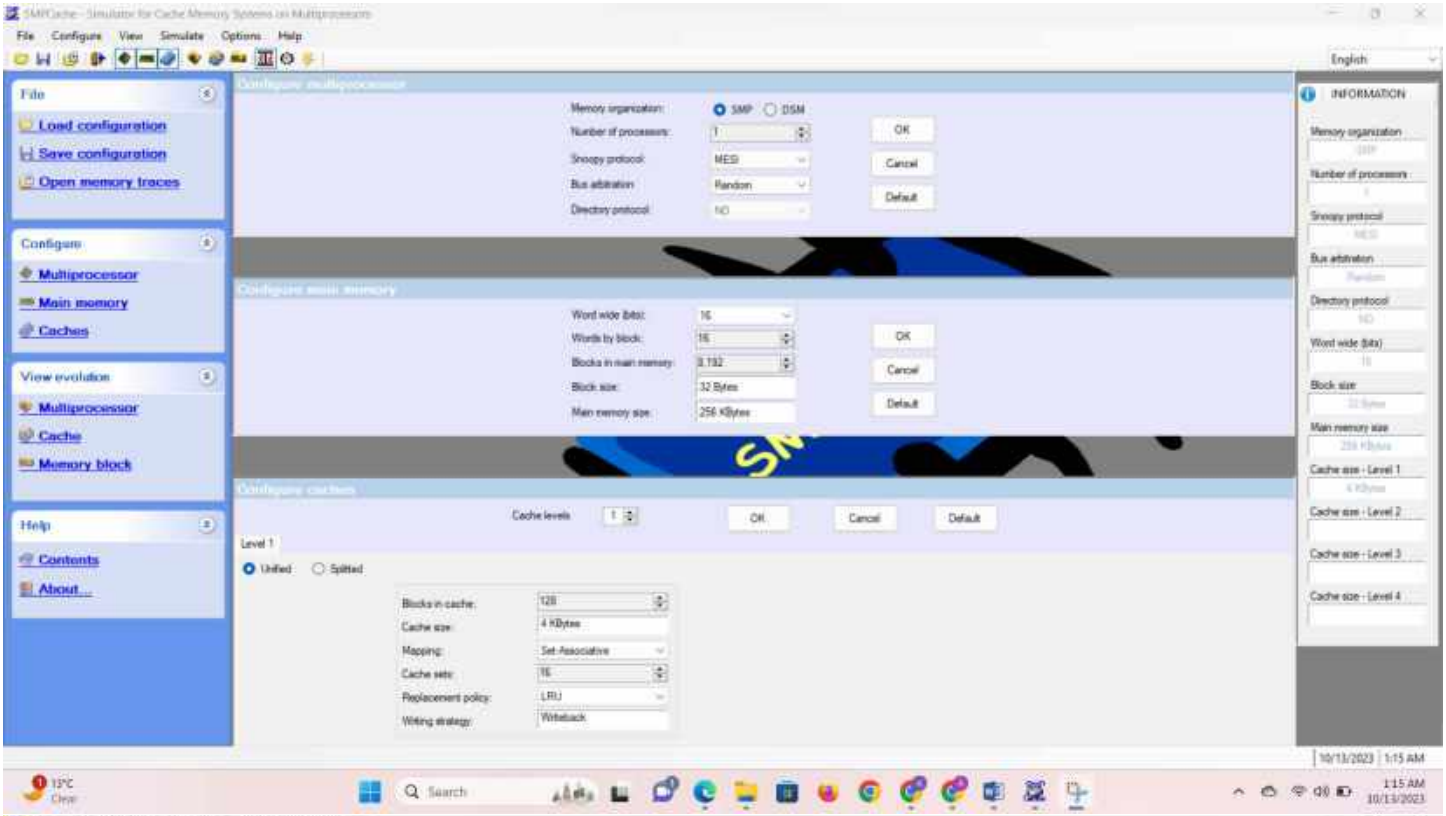
Help
Contents
About...
Actual access
Access number:
Access type:
Address:
Block:
Word:
Global readings
Local readings
Global writings
Local writings
Global hits and misses
Local hits and misses
Cache level
Simulation steps:
1055
Execute
Continue
Stop
Complete
Exit
INFORMATION
English


File
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About...
Memory organization:
SMP
DSM
Number of processors:
Snoopy protocol:
MESI
Bus arbitration:
Random
Directory protocol:
NO
OK
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Default
Word wide (bits):
16
Words by block:
16
Blocks in main memory:
8.192
Block size:
32 Bytes
Main memory size:
256 KBytes
Cache levels
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Splitted
Blocks in cache:
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Cache size:
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Word wide (bits)
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Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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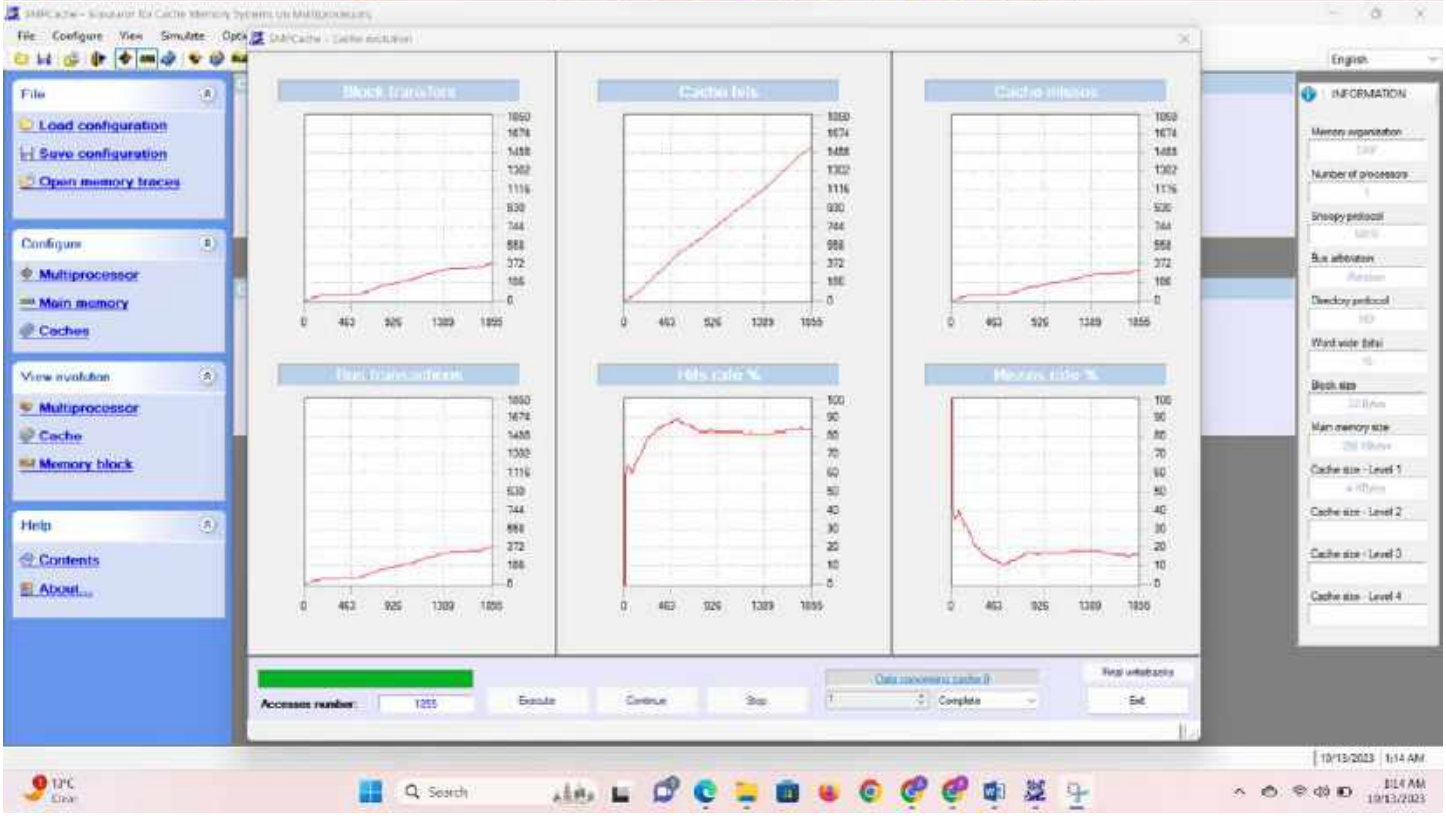
File
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Block transfers
Cache fails
Cache misses
Bus transactions
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Misses cache %
0
463
926
1389
1855
Accesses number:
1855
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INFORMATION
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Directory protocol
Word wide (bits)
Block size
Main memory size
Cache size - Level 1
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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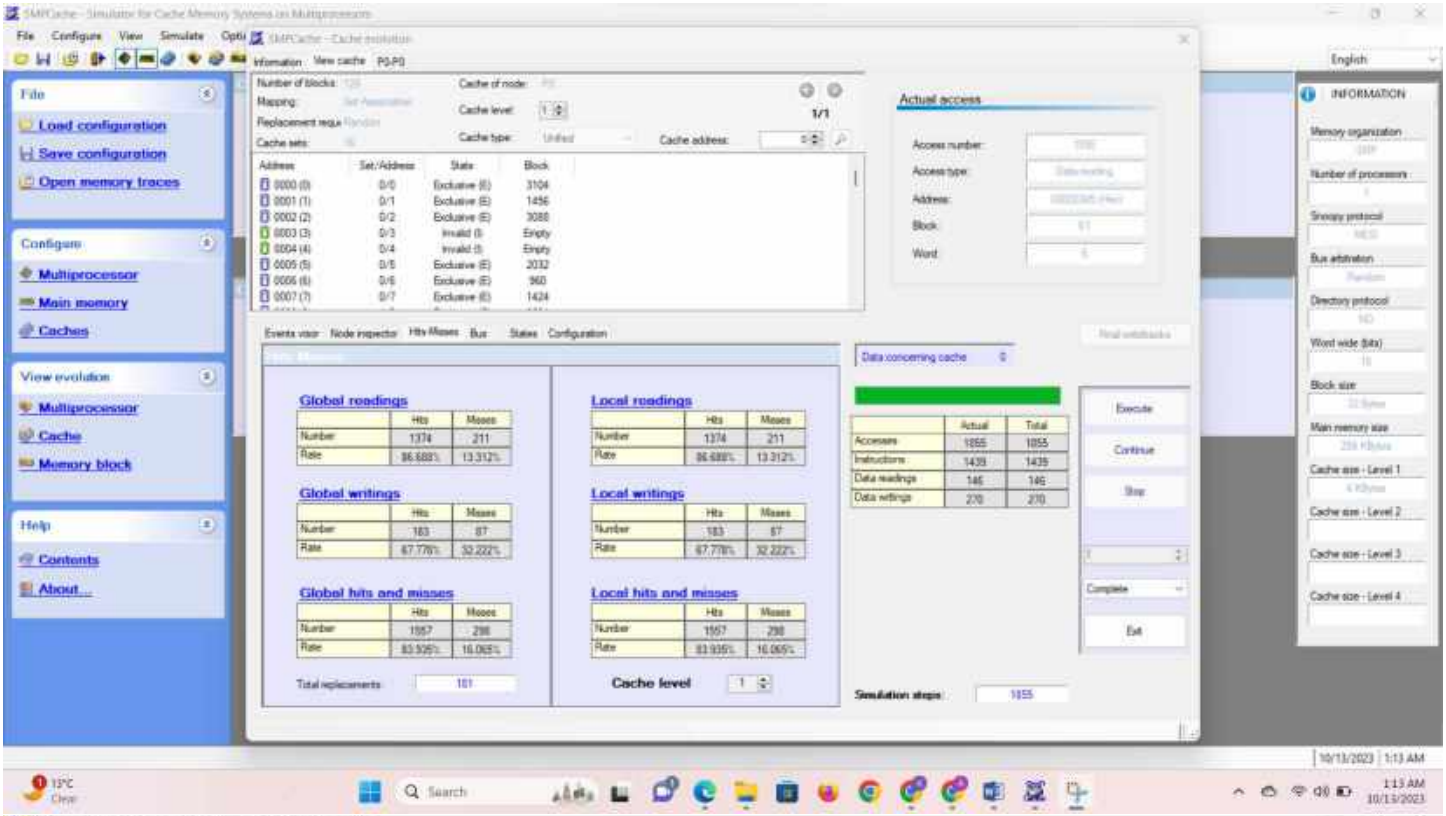
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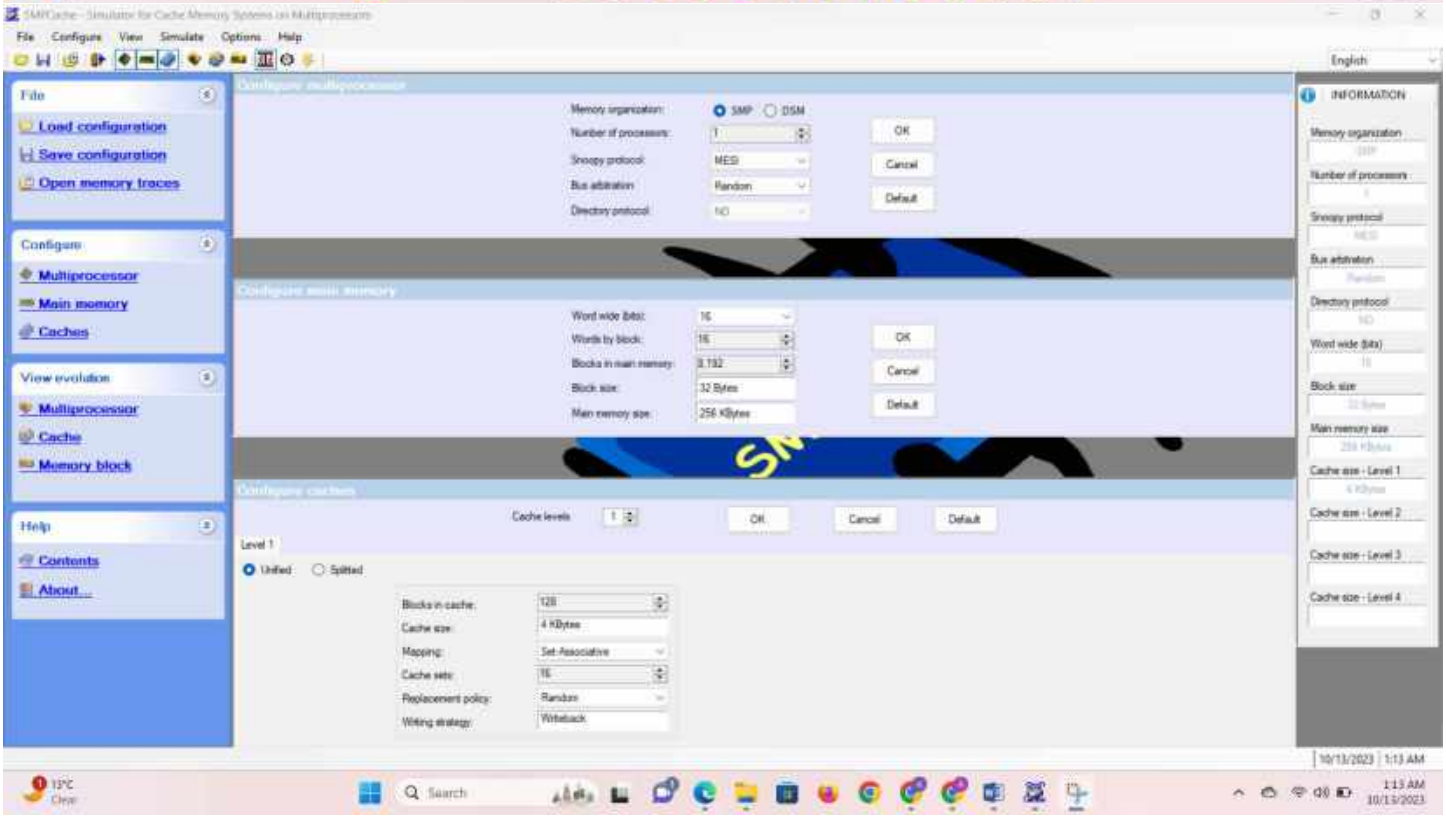
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OK
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Default
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In general, which is the replacement policy with the best miss rate? And which does it have the worst? Do the benefits of LFU and FIFO policies happen for all the benchmarks or do they depend on the different locality grades?

A. The Least Recently Used (LRU) policy appears to be the most effective replacement strategy, resulting in the lowest miss rate. On the other hand, Random stands out as the least effective replacement policy, resulting in the highest miss rate. Generally, a lower miss rate signifies a superior replacement policy.

The efficacy of Least Frequently Used (LFU) and First-in-First-Out (FIFO) policies varies based on the distinct locality characteristics of a particular trace file. It is observed that under the LFU policy, the miss rates recorded by hydro and UComp are notably lower compared to those of wave. A similar pattern is observed with FIFO. This observation confirms that the advantages offered by LFU and FIFO vary across different benchmarks.

Q. For a direct-mapped cache, would you expect the results for the different replacement policies to be different? Why or why not?

A. The utilization of various replacement policies does not yield differing miss rate outcomes. This is because direct-mapping allows for only a single available line for each specific block, leaving no room for choice or variation.

Q.In conclusion, does the use of a concrete replacement policy improve the system performance? If the answer is yes, in general, which is the step with more benefits: from Random to LRU, from Random to LFU, or from Random to FIFO? Why (consider the cost/performance aspect)?

A. Indeed, a specific replacement policy can enhance system performance. Shifting from Random to LFU is a favorable choice because LFU proves to be an ideal option—offering substantial benefits while being cost-effective. LFU shares nearly the same functionality as LRU but at a lower cost, primarily because it does not require the storage of "age bits" associated with LRU.