VLSI Technology and Design

(DSE-1)

Practical File

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S.No.	Programs	Pg.	Date	Remarks
1.	**Experiment 1: PN Junction Diode IV Characteristics** **AIM**: To simulate the forward and reverse IV characteristics of a PN junction diode, extract the knee voltage, analyse contour plots at voltages around the knee voltage, and evaluate the electric field profiles and depletion regions in the n- and p-regions. Additionally, study the effect of varying ambient temperature (300K, 325K, 350K, 375K, 400K) on these metrics.			
2.	**Experiment 2: NPN Transistor in Common Emitter Configuration** **AIM**: To design and simulate an NPN transistor in the common emitter configuration, analyse its input and output characteristics, and investigate the impact of base width and doping on collector performance. Evaluate contour plots and electric field profiles across the junctions in active, saturation, and cutoff modes, and study temperature effects (300K, 325K, 350K, 375K, 400K) on electric field, depletion region, and transistor performance.			
3.	**Experiment 3: NPN Transistor in Common Base Configuration** **AIM**: To simulate the operation of an NPN transistor in the common base configuration, study its input and output characteristics, and observe the impact of base width and doping relative to the collector region. Analyse contour plots and electric field profiles across junctions in active, saturation, and cutoff modes, and evaluate temperature effects (300K, 325K, 350K, 375K, 400K) on electric field distribution, depletion region, and overall device behaviour.			
4.	**Experiment 4: NPN Transistor in Common Collector Configuration** **AIM**: To simulate an NPN transistor in the common collector configuration, analyse its input and output characteristics, and study the influence of base width and doping on performance. Evaluate the contour plots and electric field profiles across junctions in active, saturation, and cutoff modes, and investigate the effects of temperature variations (300K, 325K, 350K,			

	375K, 400K) on electric field, depletion region, and transistor operation.			
5.	**Experiment 5: MOS Capacitor C-V Characteristics** **AIM**: To simulate a MOS capacitor with p-type bulk silicon and study its capacitance-voltage (C-V) characteristics at frequencies between 10 Hz and 1 kHz. Determine the maximum and minimum capacitance values, analyse threshold voltage for surface inversion, and verify surface inversion through structural files in OFF and ON states. Investigate the effect of ambient temperature (300K, 325K, 350K, 375K, 400K) on C-V characteristics and threshold voltage.			
6.	**Experiment 6: N-Channel MOSFET Scaling Effects** **AIM**: To simulate the output and transfer characteristics of an n-channel MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyse the performance implications of scaling.			
7.	**Experiment 7: N-Channel NMOSFET vs. PD-SOI MOSFET** **AIM:** To simulate and compare the output and transfer characteristics of an n-channel NMOSFET and a partially-depleted (PD) SOI MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyze the performance implications of scaling.			

8.	**Experiment 8: Comparison of N-Channel NMOSFET, PD-SOI MOSFET, and FD-SOI MOSFET** **AIM:** To simulate and compare the output and transfer characteristics of an n-channel NMOSFET, a partially-depleted (PD) SOI MOSFET, and a fully-depleted (FD) SOI MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyze the performance implications of scaling.			

Experiment - 01

PN Junction Diode IV Characteristics

Aim: To simulate the forward and reverse IV characteristics of a PN junction diode, extract the knee voltage, analyse contour plots at voltages around the knee voltage, and evaluate the electric field profiles and depletion regions in the n- and p-regions. Additionally, study the effect of varying ambient temperature (300K, 325K, 350K, 375K, 400K) on these metrics.

Theory:

A **PN diode** is a basic semiconductor device that consists of a junction between **p-type** and **n-type** materials. Its operation is fundamental to many electronic devices, as it allows current to flow in one direction while blocking it in the opposite direction.

1. **Formation of the PN Junction**

- A **PN junction** forms when p-type and n-type semiconductor materials are joined together.
- In the **p-type** region, the majority carriers are **holes** while in the **n-type** region, the majority carriers are **electrons**.
- Upon forming the junction, electrons from the n-region move into the p-region, and holes from the p-region move into the n-region.
- This movement creates a **depletion region** at the interface, where there are no free charge carriers. An **electric field** forms across the depletion region due to the fixed ions left behind.

2. **Built-in Potential (Barrier Potential)**

- As electrons and holes diffuse across the junction, they leave positive ions in the n-region and negative ions in the p-region.
- This leads to the creation of an **internal electric field** in the depletion region, which opposes further movement of charge carriers.
- The voltage difference across the depletion region is called the **built-in potential**.
- This built-in potential prevents further diffusion of majority carriers across the junction.

3. **Current-Voltage Characteristics**

- **Forward Bias**: In forward bias, the diode shows an exponential increase in current with voltage, described by the diode equation:

$$I = I_S(e^{qV/kT} - 1)$$

  Where:
  - I_S is the saturation current,
  - q is the charge of an electron,
  - V is the applied voltage,
  - k is Boltzmann's constant, and
  - T is the temperature in Kelvin.
- **Reverse Bias**: In reverse bias, the current is very small and mainly due to minority carriers, effectively negligible until breakdown occurs at high reverse voltage.

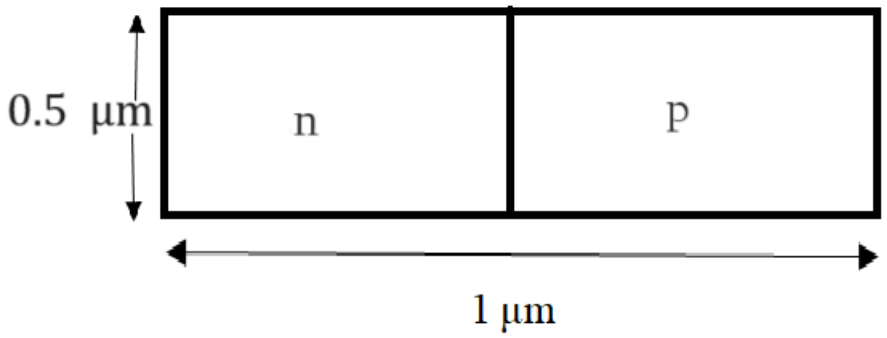
4. **Breakdown**

- **Avalanche Breakdown**: Occurs in reverse bias at high voltages where carriers gain enough energy from the electric field to create electron-hole pairs, leading to a large current.

- **Zener Breakdown**: Occurs at lower reverse voltages in heavily doped diodes, where a strong electric field can cause electron tunnelling across the junction.

Procedure:

1. Go to any browser and search for "nanohub", open the first link and sign up with google account and then login.
2. Go to "search" in the top right corner of the nanohub webpage and search for "silvaco". Open the link named "Silvaco TCAD" .
3. Click on "Accept" and then go to "Deckbuild" option in the top left corner. Now window of "Deck" section is opened where you can write the code.
4. Before writing the code, first make a blueprint of the component you want to simulate with specific length, width and mesh spacing (all distances to be measured in micro meter).
5. Lets take a diode of length 1 μm (in X-direction) , width 0.5 μm (in Y-direction) with mesh spacing 0.1 μm and divide n and p regions at 0.5 μm.



6. Implement the above blueprint to simulate a pn diode in the deck section with code.
7. Set the method system by executing the mathematical model and saving the str file.
8. Run the program and visualize IV characteristics, Depletion Region, Electric Field, by using TonyPlot.

Simulation Code:

```
go victorydevice

mesh width = 1

# x - mesh #
x.m l=0.00 s=0.01
x.m l=0.50 s=0.01
x.m l=1.00 s=0.01

# y- mesh#
y.m l=0.0 s=0.02
y.m l=0.5 s=0.02

#Region#
region num=1 x.min=0 x.max=1.0 y.min=0 y.max=0.5 mat=air
region num=2 x.min=0 x.max=1.0 y.min=0 y.max=0.5 mat=Si

# Doping #
doping uniform p.type conc=1e19 x.min=0.0 x.max= 0.5 y.min = 0.0 y.max = 0.5
doping uniform n.type conc=1e16 x.min=0.5 x.max= 1.0 y.min = 0.0 y.max = 0.5

# Electrodes #
elec name= anode x.min = 0.00 x.max = 0.00 y.min= 0.0 y.max = 0.5
elec name= cathode x.min=1.00 x.max = 1.00 y.min= 0.0 y.max = 0.5
```

```
# contact #
contact name = anode neutral
contact name = cathode neutral

# models #
models print srh temp = 300

#output#
output con.band val.band

#method#
method newton trap maxtrap=30 itlim=30

solve init

save outf= Diode_at_Vanode_0V_T300_n16_p16.str

#IV#
log outf=IV_T300_n16_p16.log
solve vanode=0 vstep=0.05 vfinal=1 name = anode

#IV  RB#
solve vanode=0 vstep=0.05 vfinal=1 name = anode
log outf=IV_RB_T300_n19_p19.log
solve vcathode=0 vstep= -0.5 vfinal= -10 name cathode

quit
```

Results and Discussions:

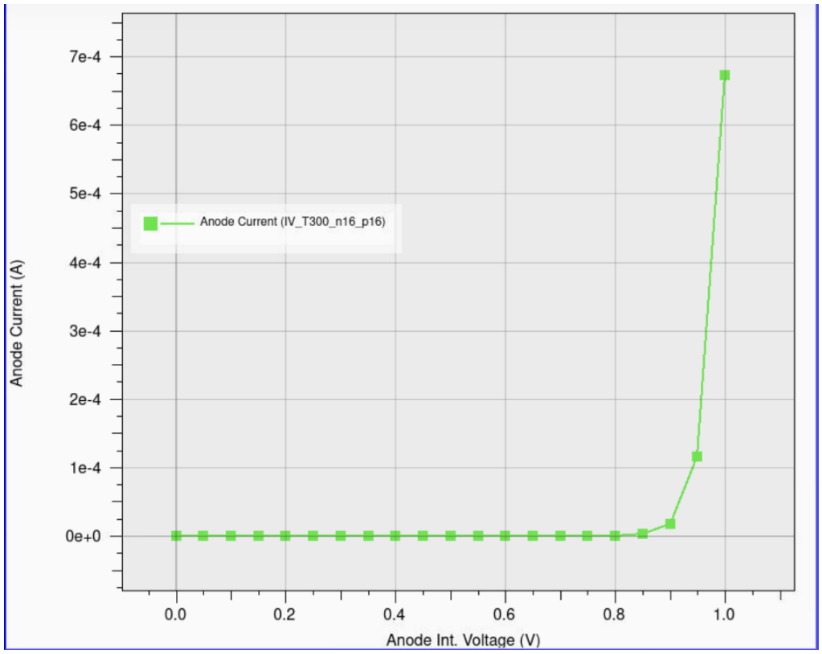


Fig. I : Forward Characteristics at 300K

This graph shows the relationship between **Anode Current (A)** and **Anode Int. Voltage (V)** i.e. **I-V (current-voltage) characteristic curve** for the diode.

- For voltages below approximately 0.8 V, the current remains close to zero, suggesting minimal conduction in this range.
- After about 0.8 V, the current increases rapidly, indicating the onset of significant conduction.
- The sharp rise in current near 1.0 V suggests a **threshold voltage** or **turn-on voltage**, beyond which the material or device becomes conductive.

• This behavior is typical in **diodes or semiconductor junctions**, where current remains very low until a certain threshold voltage is reached, after which it rises sharply. The graph may be used to characterize the material's or device's electrical properties, such as forward voltage and current response.

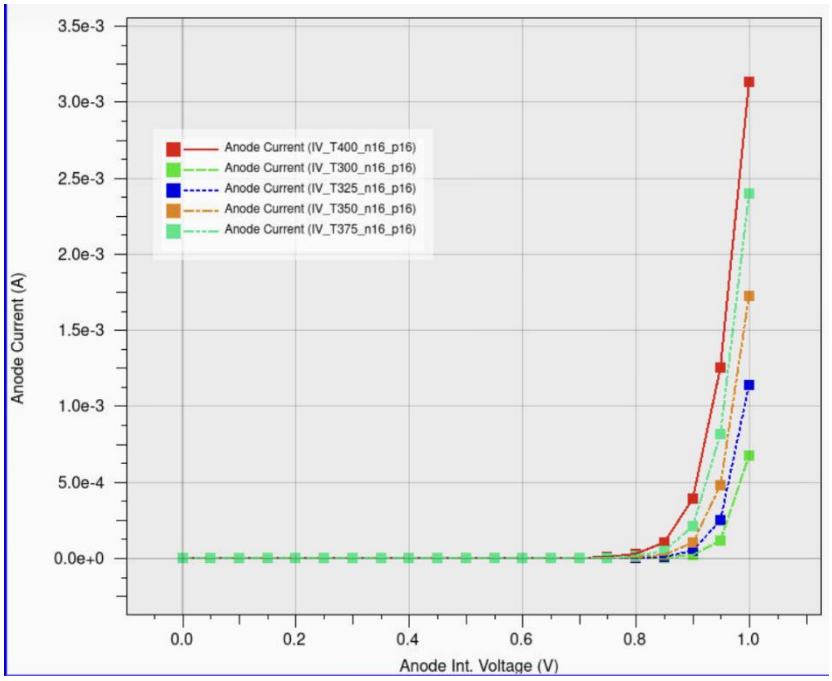


Fig: II. Forward Characteristic of pn diode at different temperatures

This graph displays the I-V characteristics for a device or material under varying temperatures. Each curve represents the anode current for a different temperature:

- Red (T=400): Highest current at a given voltage, indicating increased conductivity at higher temperatures.
- Green (T=300): Blue (T=325), Orange (T=350), Yellow (T=375): Intermediate curves, with current values increasing as the temperature rises.
- For voltages below 0.7–0.8 V, all curves show very low current, indicating minimal conduction.
- After this threshold, the current rises sharply, with higher temperatures resulting in higher currents at the same voltage.

The increased current at higher temperatures suggests thermal activation, where temperature enhances charge carrier mobility, reducing resistance and increasing current. This behavior is typical in semiconductors or materials with thermally activated conduction, showing that conductivity increases with temperature.

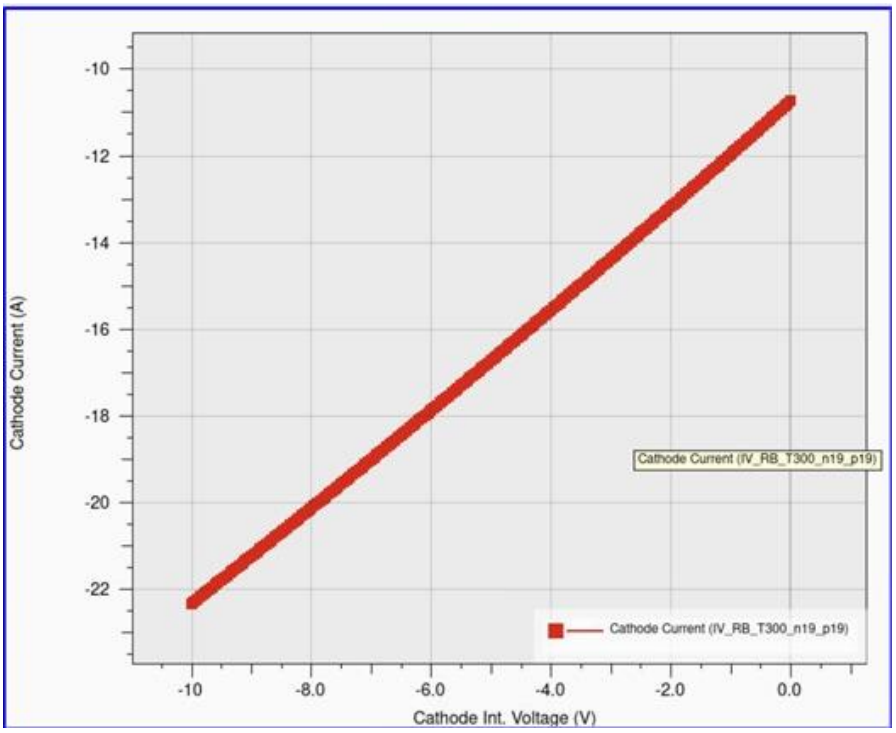


Fig.III: Reverse Characteristics at 300K

This graph represents the reverse bias characteristics of a pn junction diode. In reverse bias, the diode's cathode is connected to a higher potential than the anode, causing the current to be limited primarily by the leakage across the junction until breakdown occurs. The plot shows a steady increase in reverse current with increasing reverse voltage, though the current remains relatively low, consistent with typical reverse-bias

behavior. The linear increase in current suggests that the diode is approaching its breakdown region, but full breakdown has not yet occurred within the range shown. This characteristic is often used to analyze diode properties, such as leakage current and breakdown voltage.

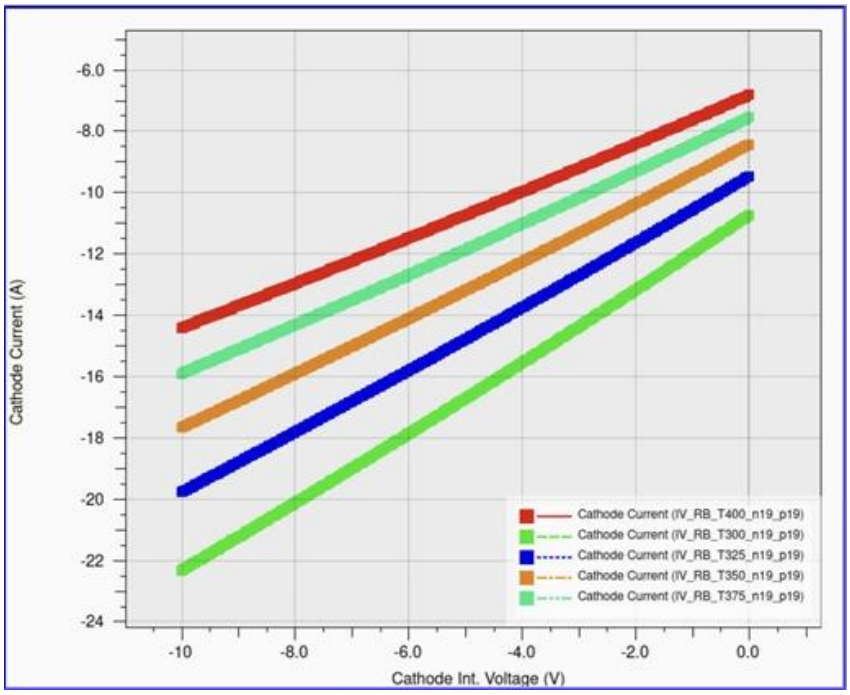


Fig. IV Reverse Characteristics at different temperatures

This graph represents the reverse bias characteristics of a pn junction diode at various temperatures, as indicated by different colored lines. Each line corresponds to a specific temperature setting, labeled as T300, T325, T350, T375, and T400, showing the variation in cathode current with cathode internal voltage.

As the reverse voltage increases (moving left along the x-axis), the reverse current also increases, but it remains relatively low until breakdown occurs. The red line, representing the highest temperature (T400), shows the highest reverse current for a given voltage, while the green line (T300) shows the lowest current. This trend is typical in pn junction diodes, where the reverse leakage current increases with temperature due to higher carrier generation rates. The graph clearly illustrates how temperature influences the diode's reverse characteristics, with higher temperatures leading to increased reverse current at any given reverse bias voltage.

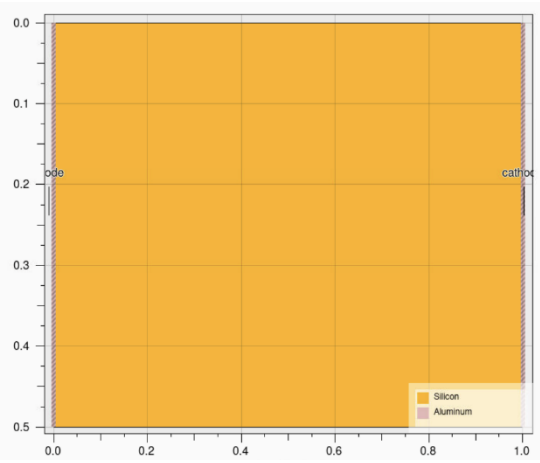


Fig. V: Structure profile

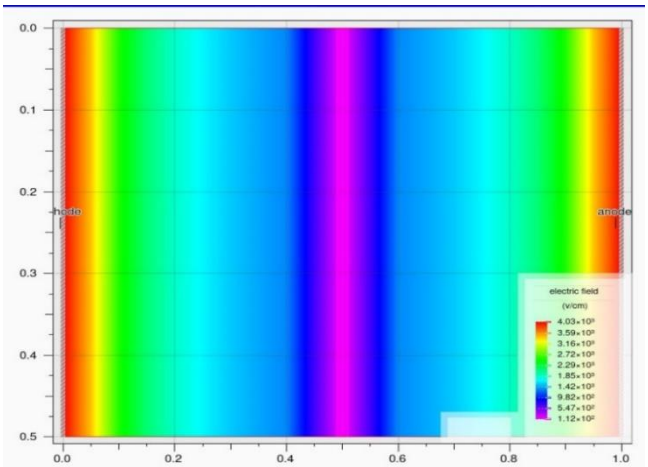


Fig.VI: Electric Field

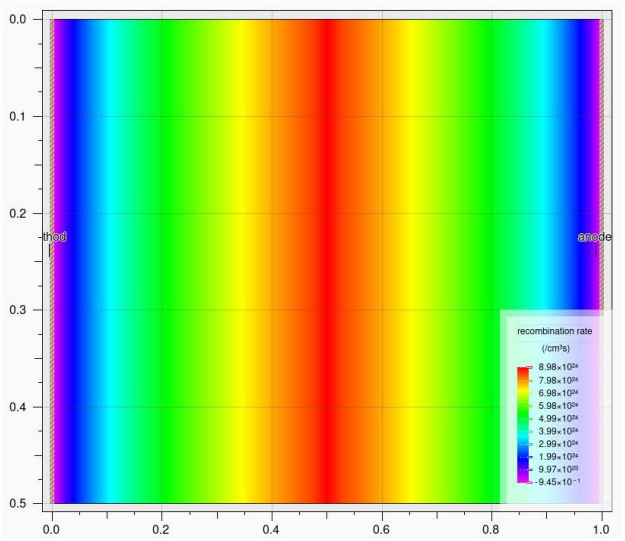


Fig. VII: Recombination

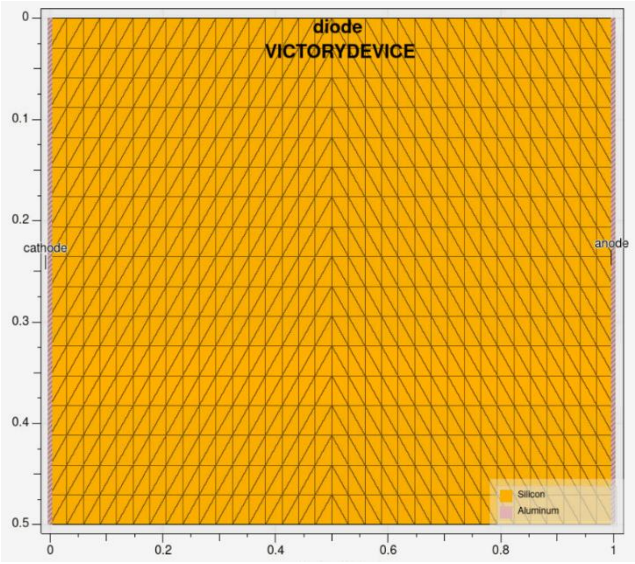


Fig. VIII. Meshing

Observations:

In the IV characteristic of pn diode, the knee voltage of PN diode decreases with increase in temperature. This happened because of several reasons:

1. Increased Intrensic Carrier Concentration:
   In a pn junction, the intrinsic carrier concentration increases with a rise in temperature. This is because an increase in the number of thermally generated electron-hole pairs occurs as a result of the increased temperature, which eventually increases exponentially with a rise in the temperature. The higher the carriers' concentration, the more the current to be witnessed.
2. Enhanced Carrier Mobility;
   With the increase of temp lead to increase thermal energy for carriers which overcomes the barrier potential. Resultant a lower forward voltage to reach the same level of current, thus lowering the knee voltage.
3. Lower Band gap Energy
   The increasing temperature reduces the energy gap. Easy transition of electrons from a valence band to a conduction band due to lowered energies allows an increase in electron and hole concentrations, eventually raising the current.

These Factors collectively cause the knee voltage to decreases as the temp increases.

Sources of Error:

- Inadequate meshing, especially near junctions, can cause inaccuracies; fine meshing is necessary in regions with high electric fields. Improperly defined contacts (e.g., non-ideal ohmic or Schottky) can introduce unexpected voltage drops or resistive effects.
- Incorrect doping concentrations or gradients can result in deviations from expected I-V characteristics. Ensure accurate material properties (e.g., bandgap, permittivity, mobility) and configure temperature effects correctly for non-standard conditions.
- Diode behavior is temperature-dependent; incorrect modeling of thermal effects can lead to deviations. Use appropriate recombination models (e.g., SRH, Auger) in high-injection regions to avoid inaccuracies.

Conclusion:

In conclusion, simulating the reverse bias characteristics of a pn diode in Silvaco provides valuable insights into the diode's behavior under varying conditions, such as temperature and applied reverse voltage. The simulation effectively demonstrates key properties like reverse leakage current, temperature dependency, and the approach to breakdown, which are crucial for understanding diode performance in real-world applications.

Through the simulation, it becomes evident that as temperature increases, the reverse current also increases, indicating a strong temperature dependence due to enhanced carrier generation. This characteristic is critical when designing diodes for temperature-sensitive applications, as higher leakage currents can affect circuit stability.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze

Experiment-02

NPN Transistor in Common Emitter Configuration

Aim: To design and simulate an NPN transistor in the common emitter configuration, analyze its input and output characteristics, and investigate the impact of base width and doping on collector performance. Evaluate contour plots and electric field profiles across the junctions in active, saturation, and cutoff modes, and study temperature effects (300K, 325K, 350K, 375K, 400K) on electric field, depletion region, and transistor performance.

Theory:

A transistor is a semiconductor device with three terminals whereby it allows the flow of current between two of its terminals while one terminal controls such a current flow. The transistors come in two major types: the bipolar junction transistor (BJT) and the field-effect transistor (FET). In this experiment, we shall show the characteristics of a BJT.

Transistors can be divided into two types: PNP (where there's an n-type layer sandwiched between two p-type layers) and NPN (where there's a p-type layer sandwiched between two n-type layers). For this experiment, we will discuss an NPN-type BJT.

A transistor can be thought of as two p-n junction diodes in series with three regions that have three terminals; the emitter, the base, and the collector.

1) Emitter In an NPN transistor, it is present on the left side of the transistor and its primary function is to inject majority charge carriers into the base. In short, the emitter always has to be forward biased with respect to the base so that the charge carriers are injected. Also, it has to be heavily doped for injecting a large number of carriers.

2) Collector: It is placed at the right and its basic function is to collect most of the charge carriers. Kept at reverse bias, this helps pull the charge carriers away from the junction with the base and thus has moderate doping.

3) Base: This is the middle, thin section of the transistor that is very lightly doped and hence allows most of the injected charge carriers from the emitter to the collector.

There are two p-n junctions in any type of transistor: between the emitter and base, which is known as the emitter-base junction, and between the base and collector, which is known as the collector-base junction.

Transistor is a three terminal device as discussed previously. Hence for connecting it in a circuit one terminal is connected common to input and output circuits. There are three types of configurations for a BJT:

1) Common Emitter (CE)
2) Common base (CB)
3) Common Collector (CC)

In this experiment all the characteristics will be demonstrated on common emitter configuration.

Common Emitter Configuration In this configuration input is connected between base and emitter whereas the output is taken between collector and emitter. In this type of configuration, the emitter is common to input and output circuits. Here the biasing voltages are applied between collector and emitter and base and emitter. The emitter base junction is forward biased and the base is made more positive whereas collector emitter junction is reverse biased and the collector is made more positive than emitter. In this configuration the base bias voltage must be less than collector bias collector bias voltage.

Input Characteristics: Input characteristics the curve drawn between base current and base emitter voltage for a given value of collector emitter voltage. The input characteristics of CE configuration of transistor are quite similar to those of forward biased diode because the base emitter region of the transistor is a diode, and it is forward biased.

Output Characteristics: It is the curve drawn between collector current and current emitter voltage for given value of base current. The transistors are always operated above 1V.

Operating Modes:

The CE configuration demonstrates three fundamental operating modes:

1) CE Active Mode
2) CE Saturation Mode
3) CE Cutoff Mode

- CE Active Mode: In the active region, base-emitter junction is forward biased and the collector-base junction is reverse biased. This operation mode is primarily utilized in analog circuits for amplification.
- CE Saturation Mode: In this configuration, both the base-emitter and collector-base junctions are forward-biased. In this condition, the transistor allows the maximum amount of current to flow from collector to emitter, hence acting more like a closed switch. For switching in digital circuits, where the transistor should be "on," conducting the maximum possible amount of current in the circuit, this mode is adopted.
- CE Cutoff Mode: The base-emitter junction in the cutoff region is not forward-biased, hence does not allow much current through the collector. The base and collector currents are nearly zero, hence, it is like an open switch. This mode is taken in digital circuits for switching, where the transistor has to be "off," and no current flow will be allowed.

Procedure:

1. Open Silvaco TCAD software, Create a new project and name it appropriately.
2. Use the `Mesh` command to define the mesh for your NPN transistor structure. This includes specifying the grid points and spacing.
3. Define Regions using the `Region` command to define the different regions of the NPN transistor, such as the emitter, base, and collector regions.
4. Use the `Electrode` command to define the emitter, base, and collector electrodes.
5. Specify Material Specification by the `Material` command for each region (e.g., silicon for the semiconductor regions) and define the doping concentrations for the emitter, base, and collector regions using the `Doping` command.
6. Specify the `Model` command to specify the physical models for the simulation
7. Run the Simulation using `Run` command to start the simulation, Monitor the simulation progress and check for any errors or warnings.
8. Analyze Results and Save the simulation results and plots for further analysis and documentation.

Simulation Code:

```
go victorydevice

mesh width = 1

#x-mesh #
x.m l=0.00 s=0.01
x.m l=0.50 s=0.01
```

```
x.m l=0.51 s=0.01
x.m l=0.59 s=0.01
x.m l=0.6 s=0.01
x.m l=1.6 s=0.01

#y-mesh#
y.m l=0 s=0.01
y.m l=0.5 s=0.01

#region#
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =air
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =Si

#Doping#
doping uniform n.type conc=1e18 x.min=0.0 x.max=0.5 y.min=0 y.max=0.5
doping uniform p.type conc=1e18 x.min=0.5 x.max=0.6 y.min=0 y.max=0.5
doping uniform n.type conc=1e17 x.min=0.6 x.max=1.6 y.min=0 y.max=0.5

#Electrode#
elec name=emitter x.min=0 x.max=0 y.min=0 y.max=0.5
elec name=base x.min=0.51 x.max=0.59 y.min=0 y.max=0
elec name=collector x.min=1.6 x.max=1.6 y.min=0 y.max=0.5

#contact#
contact name=emitter neutral
contact name=base neutral
contact name=collector neutral

#models #
models print srh temp=300

#output#
output con.band val.band

#method#
method newton trap maxtrap=30 itlim=30
solve init
save outf=bjtinput.str

#IV Input#
solve vcollector=1 vstep=0 vfinal=1 name=collector
log outf=bjtIV_input.log
solve vbase=0 vstep=0.1 vfinal=1 name=base

#IV Output#
solve vbase= 0.2 vstep=0 vfinal=0.2 name=base
Contact name=base current
Solve ibase=100.e-6
log outf=bjt.IV-output-ib-50uA.log
Solve Vcollector=0 vstep=0.5 vfinal=10 name=collector

#turn Off logging#
log off

#save final structure#
```

```
save outf =bjt_CE_final.str
quit
```

Result and discussion:

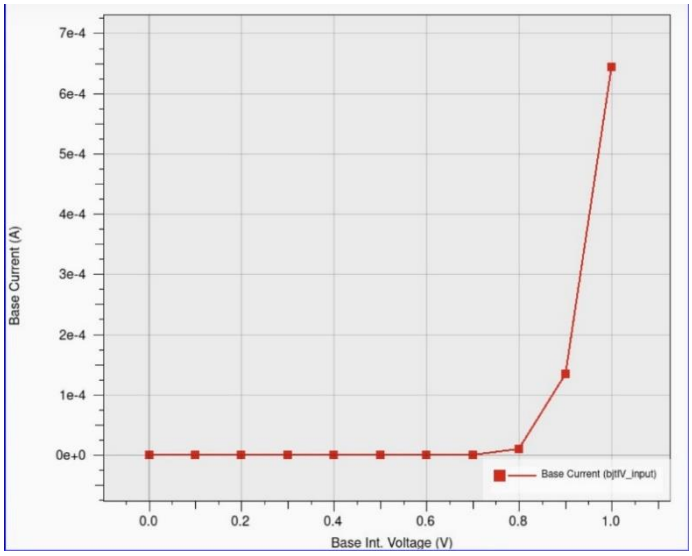
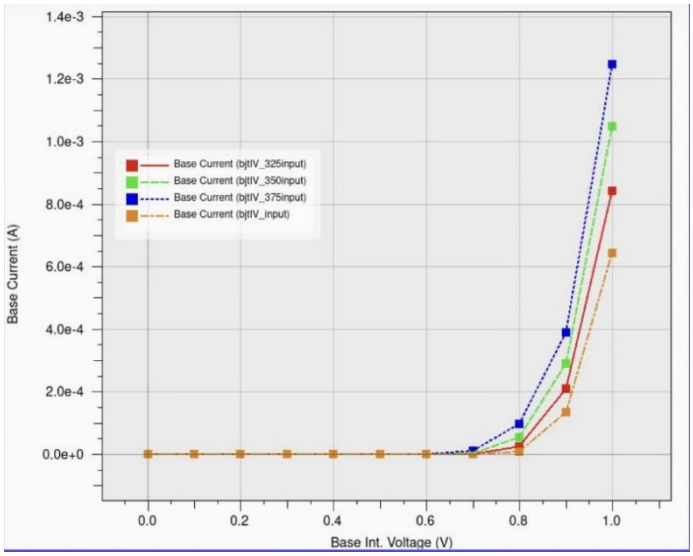


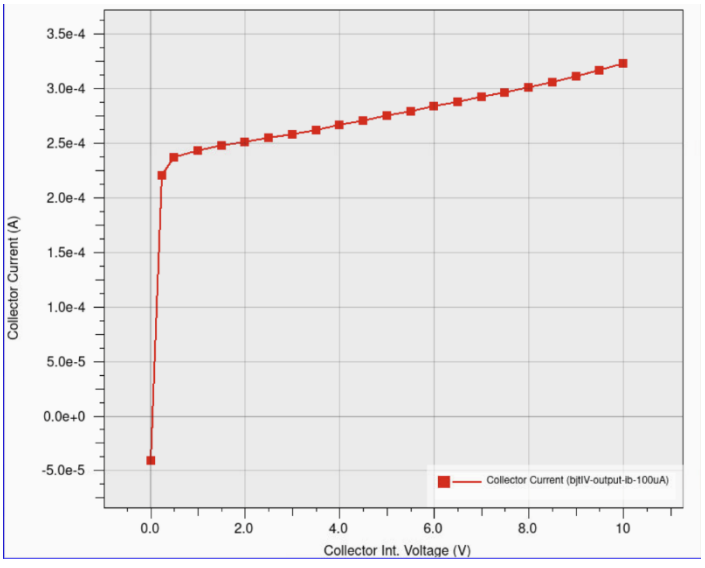
Fig: I. Input characteristic at 300K

This graph illustrates the Base Current (A) as a function of Base Int. Voltage (V), likely for a transistor or similar semiconductor device. The plot shows that the base current remains very low and nearly constant for voltages below approximately 0.8 V. Beyond this point, there is a sharp increase in current, indicating a threshold or turn-on voltage near 0.9–1.0 V, after which the base current rises steeply. This behavior suggests that the device has a non-linear response, with minimal conduction until a critical voltage is reached, at which point significant current flows through the base.



This plot shows the relationship between base current (A) and base input voltage (V) for a transistor at different temperatures i.e. 300K, 325K, 350K, and 375K, along with a general input setting. Each color represents a different input condition, with the corresponding line styles marking the trend of the base current as the base voltage increases. As the voltage approaches around 0.8 V and higher, there is a noticeable exponential increase in base current, indicating the activation region for the transistor where it starts conducting more current with a slight increase in voltage.

Fig: II. Input Characteristics at 300K, 325K, 350K,375K



This plot shows the relationship between collector current (A) and collector input voltage (V) i.e. output characteristics. The graph indicates that at low collector voltages, there is a rapid increase in collector current, which then stabilizes as the voltage increases. This behavior is characteristic of the transistor's active region, where the current remains relatively constant despite increases in voltage, showing a saturation trend. The collector current stabilizes around 3.0e-4 A, illustrating the transistor's operation in its active region with minimal variation in current at higher voltages.

Fig. III: Output Characteristics at 300K

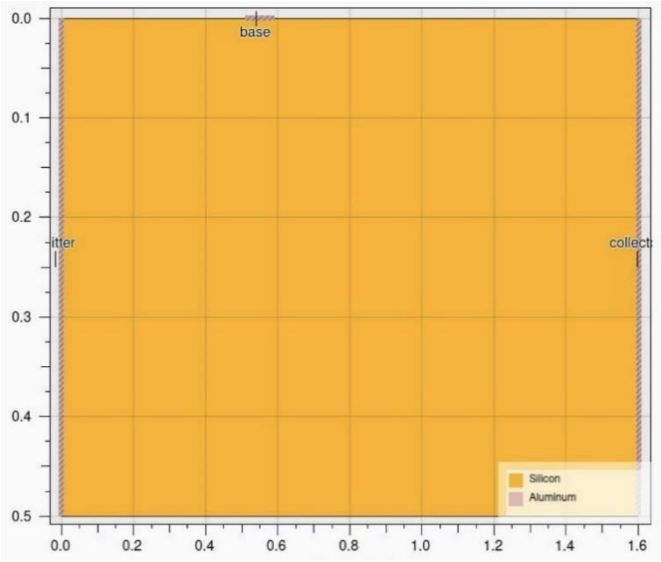


Fig. IV: Structure (Material) Profile

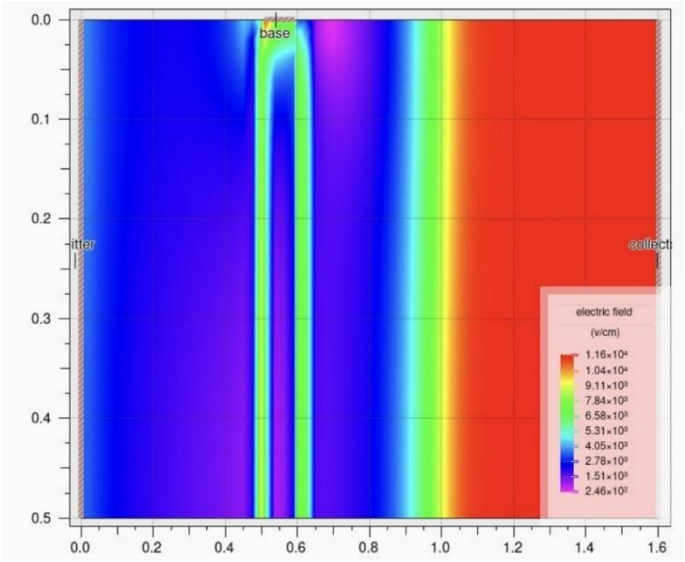


Fig.V: Electric Field Profile

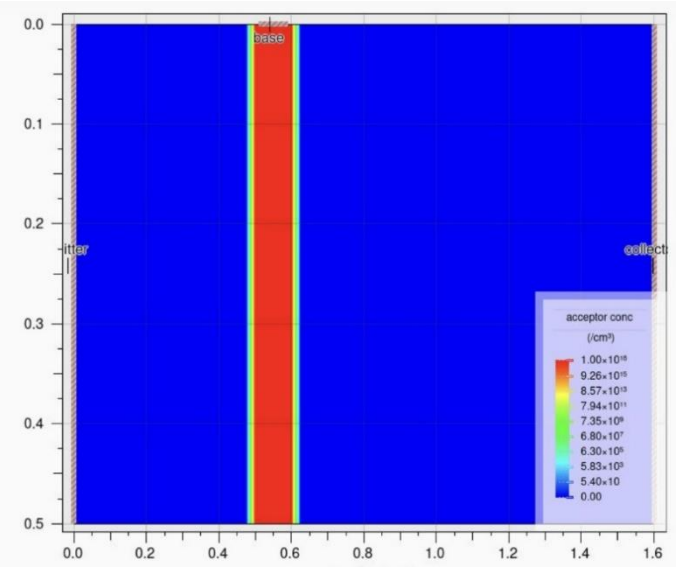


Fig.VI: Acceptor Concentration

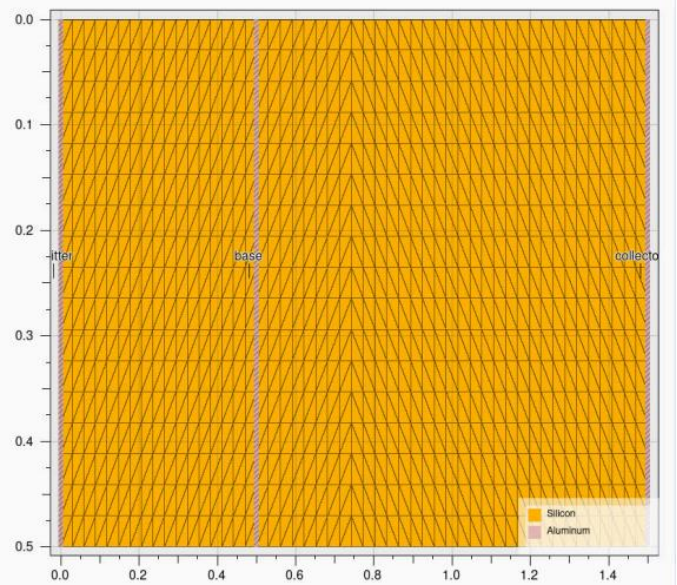


Fig. VII: Meshing

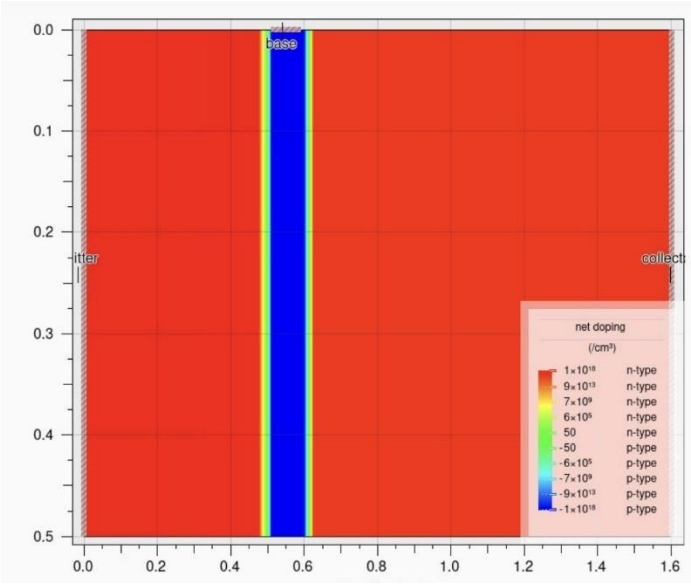


Fig.VIII: Net Doping Profile

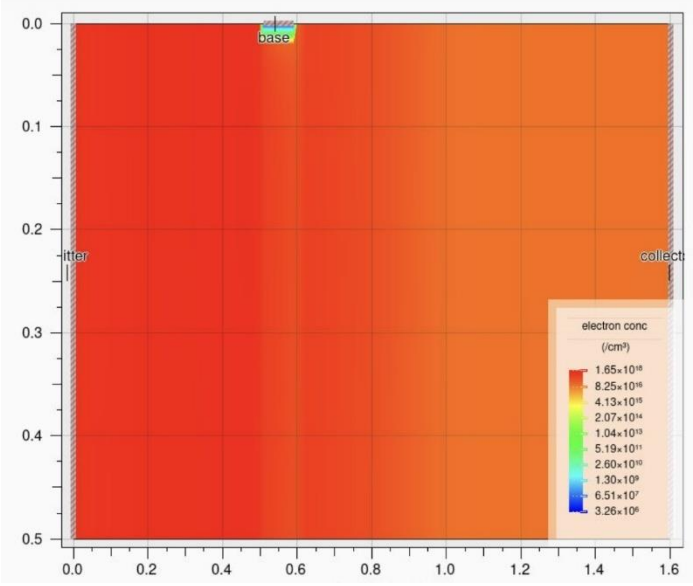


Fig.IX: Electron Concentration

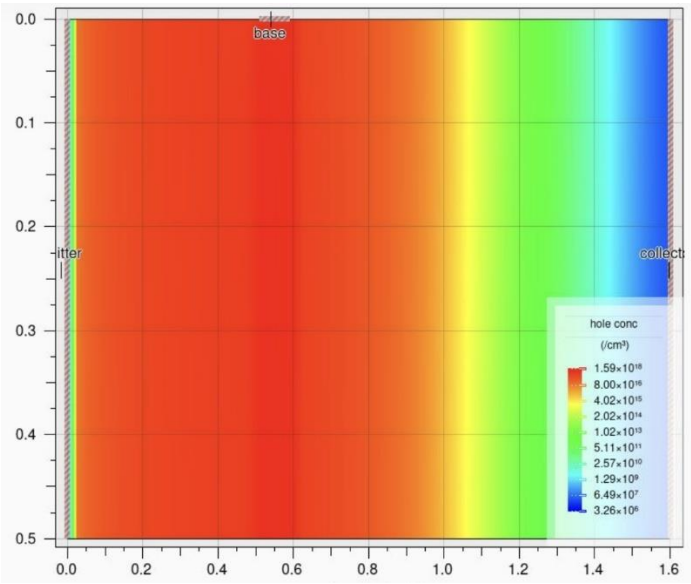


Fig: Hole Concentration

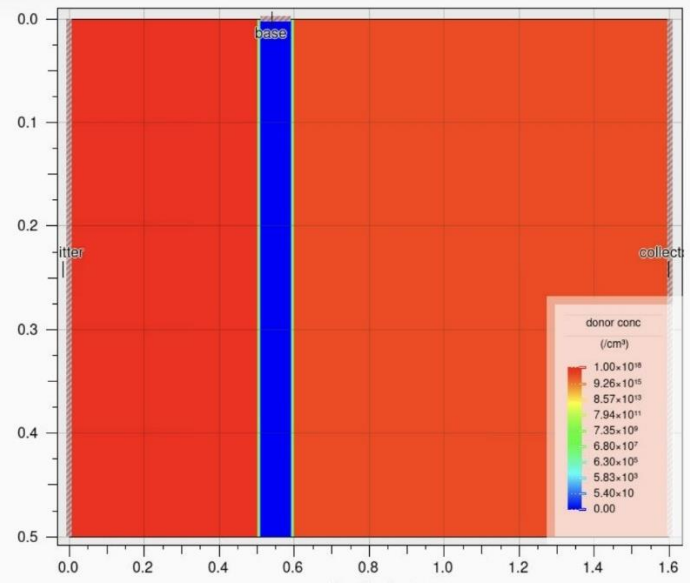


Fig: Donor Concentration

Observation:

1. Structure Profile: The NPN transistor consists of three regions: the emitter (n-type), base (p-type), and collector (n-type).The emitter is heavily doped to provide a high concentration of electrons, while the base is lightly doped and thin to facilitate efficient charge transfer.

2. Electric Field Profile:Electric fields are strongest at the junctions between emitter-base and base-collector. The emitter-base junction has a forward bias, while the base-collector junction is reverse-biased, creating an electric field that accelerates electrons from emitter to collector.

3. Acceptor Ion Concentration: In the p-type base, acceptor ions provide a concentration of holes. The acceptor concentration in the base is lower than the donor concentration in the emitter and collector.

4. Meshing: Fine meshing is typically used near the junctions for accurate simulations of electric fields and carrier concentrations. Coarser meshing may be applied in the bulk regions of the emitter, base, and collector.

5. Net Profile Doping: The emitter is heavily doped (n+), the base is lightly doped (p), and the collector is moderately doped (n). This doping profile helps in achieving high current gain and efficient carrier injection.

6. Electron Concentration: Highest in the n-type emitter, moderate in the n-type collector, and very low in the p-type base. Electrons injected from the emitter into the base diffuse through the base and are swept into the collector.

7. Hole Concentration: Highest in the p-type base, where holes are the majority carriers. Hole concentration is low in the n-type emitter and collector.

8. Donor Concentration: Donor concentration is high in the n-type emitter and collector regions. This concentration provides the primary source of electrons in these regions, crucial for current flow through the transistor.

Sources of Errors:

- Fine meshing is necessary around the emitter-base and base-collector junctions, where electric fields are high; poor meshing can lead to inaccurate results. Properly define contacts for each terminal (emitter,

base, and collector) to ensure accurate current flow; incorrect boundary conditions can introduce unwanted resistive effects.

- Incorrect doping levels or gradients in the emitter, base, and collector regions can impact the transistor's I-V characteristics and gain. Ensure accurate material properties, such as bandgap, mobility, and permittivity; temperature-dependent parameters must also be correctly set.

- NPN transistor performance is highly temperature-sensitive; incorrect temperature modeling can alter current gain and switching behavior.

- Accurate recombination models (e.g., SRH, Auger) are essential, particularly in the base region, to reflect real recombination rates and carrier dynamics.

Conclusion:

Contour plots were used to illustrate various concentrations including acceptor, donor, electron and hole concentrations. Furthermore, the colors of each contour plot from the VIBGYOR spectrum depict the concentration in the majority of the plots. We also seem to have illustrated a contour plot for the electric field profile towards the last stages of input and output characteristic analysis.

A simple BJT (Bipolar Junction Transistor) which operates in the active region where the emitter-base (EB) is forward biased and collector-base (CB) is reverse biased results in amplification of current.

It should be noted that for the case of the EB junction, upon increasing the base-emitter voltage the depletion region becomes reduced. This in contrast to the case of the CB junction, where the depletion region broadens under reverse bias, which is very important in effective collection of carriers. There are two fields in the BJT, at the EB junction, electric field facilitates carrier injection while at the CB junction, electric field assists in collection of carriers, both enhancing gain of the transistor. We looked at variations of input and output characteristics of the BJT (in common emitter configuration) with temperature variations of 300K, 325K, 350K, 375K, 400K: With respect to input characteristics as the temperature increases the current drops. This can be attributed to the electric field that changes as can be observed in the profile of the electric field.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze

Experiment -03

NPN Transistor in Common Base Configuration

Aim: To simulate the operation of an NPN transistor in the common base configuration, study its input and output characteristics, and observe the impact of base width and doping relative to the collector region. Analyze contour plots and electric field profiles across junctions in active, saturation, and cutoff modes, and evaluate temperature effects (300K, 325K, 350K, 375K, 400K) on electric field distribution, depletion region, and overall device behavior.

Theory:

An NPN transistor is a type of bipolar junction transistor (BJT) made up of three layers of semiconductor material: N-type, P-type, and N-type. These layers are referred to as the emitter, base, and collector. In the common-base (CB) configuration, the base is the common terminal for both the input and output circuits.

The common-base configuration is often used for high-frequency applications, and it has certain distinctive characteristics:

- Input Characteristics: The input characteristic curve for the CB configuration shows the relationship between the input voltage and the input current. It is essentially a plot of emitter current versus emitter-base voltage.
- Output Characteristics: The output characteristic curve shows the relationship between the output voltage and the output current at various base currents .

In the common-base configuration, the voltage gain is typically high, and the input impedance is low. However, it provides no current gain, unlike the common-emitter configuration, where both current and voltage gains are significant.

The common-base configuration is less common than the common-emitter configuration but is still useful in certain applications, particularly where high-frequency operation or low input impedance is required.

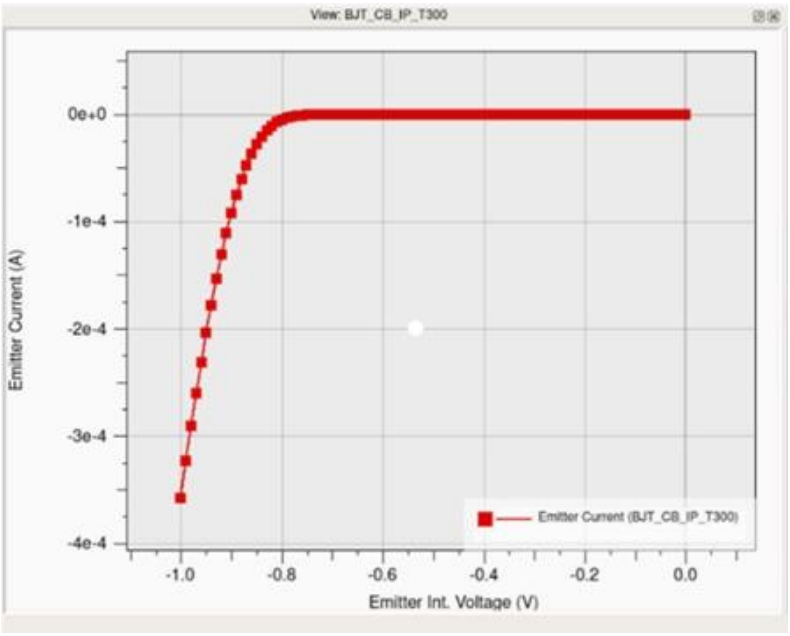
Procedures:

1. Open Silvaco TCAD software, Create a new project and name it appropriately.
2. Use the `Mesh` command to define the mesh for your NPN transistor structure. This includes specifying the grid points and spacing.
3. Define Regions using the `Region` command to define the different regions of the NPN transistor, such as the emitter, base, and collector regions.
4. Use the `Electrode` command to define the emitter, base, and collector electrodes.
5. Specify Material Specification by the `Material` command for each region (e.g., silicon for the semiconductor regions) and define the doping concentrations for the emitter, base, and collector regions using the `Doping` command.
6. Specify the `Model` command to specify the physical models for the simulation
7. Run the Simulation using `Run` command to start the simulation, Monitor the simulation progress and check for any errors or warnings.
8. Analyze Results and Save the simulation results and plots for further analysis and documentation.

Simulation Code:

```
go victorydevice

mesh width = 1
#x-mesh #
x.m l=0.00 s=0.01
x.m l=0.50 s=0.01
x.m l=0.51 s=0.01
x.m l=0.59 s=0.01
x.m l=0.6 s=0.01
x.m l=1.6 s=0.01

#y-mesh#
y.m l=0 s=0.01
y.m l=0.5 s=0.01

#region#
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =air
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =Si

#Doping#
doping uniform n.type conc=1e18 x.min=0.0 x.max=0.5 y.min=0 y.max=0.5
doping uniform p.type conc=1e18 x.min=0.5 x.max=0.6 y.min=0 y.max=0.5
doping uniform n.type conc=1e17 x.min=0.6 x.max=1.6 y.min=0 y.max=0.5

#Electrode#
elec name=emitter x.min=0 x.max=0 y.min=0 y.max=0.5
elec name=base x.min=0.51 x.max=0.59 y.min=0 y.max=0
elec name=collector x.min=1.6 x.max=1.6 y.min=0 y.max=0.5

#contact#
contact name=emitter neutral
contact name=base neutral
contact name=collector neutral

#models #
models print srh temp=300

#output#
output con.band val.band

#method#
method newton trap maxtrap=30 itlim=30
solve init
save outf=bjtinput.str

#IV Input#
log outf=IV_CB_input.log
solve vemitter=0 vstep=-0.05 vfinal=-1 name=emitter
quit
```

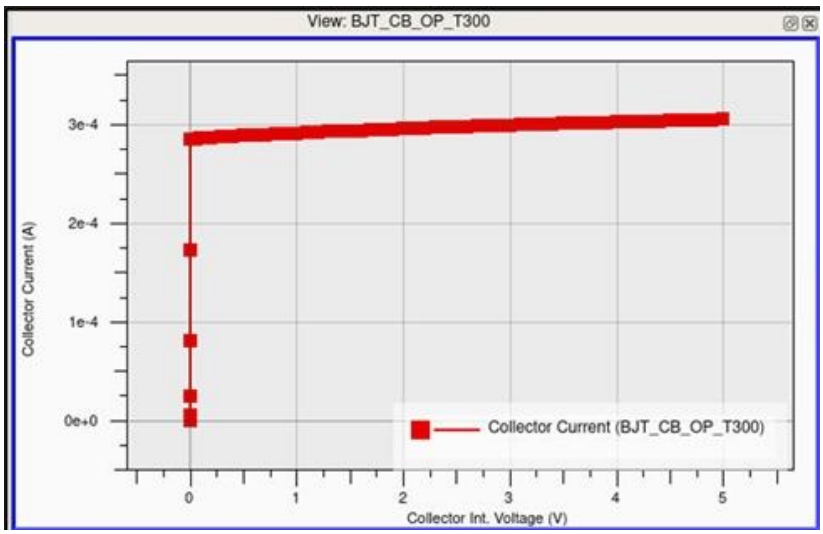
Results and Discussions:



This graph represents the input characteristics of an NPN bipolar junction transistor (BJT) in the common base (CB) configuration. The plot shows the emitter current (in amperes, A) as a function of emitter internal voltage (in volts, V) at a specified temperature, 300K.

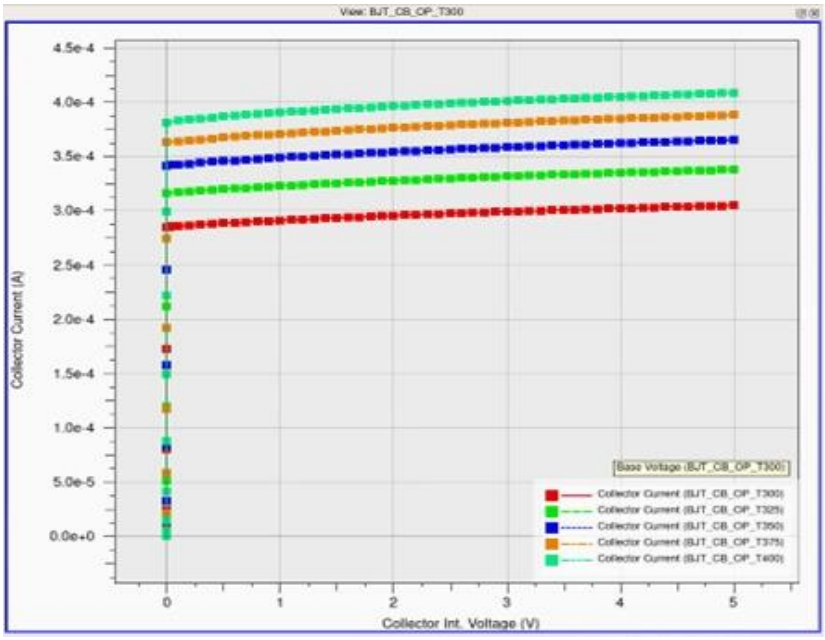
In the common base configuration, the emitter current increases rapidly with a slight increase in emitter voltage, indicating the exponential relationship characteristic of a forward-biased emitter-base junction. As the emitter voltage approaches zero, the emitter current saturates, reaching a stable value. This behavior reflects the diode-like response of the emitter-base junction, where the current quickly rises with the applied voltage until it stabilizes near zero volts.

Fig. I: Input Characteristics of CB at 300K



The output characteristics of an NPN BJT in common base configuration show the relationship between the collector current and collector-emitter voltage for different emitter currents.
Cutoff Region: Low collector-emitter voltage, minimal collector current, BJT is "off."
Active Region: Collector current is stable and mainly dependent on emitter current, ideal for amplification.
Saturation Region: High emitter current but low collector-emitter voltage; BJT is fully "on."

Fig.II: Output Characteristics of CB at 300K



The output characteristics of an NPN transistor in the common-base (CB) configuration are significantly affected by temperature. As temperature increases, the saturation current rises exponentially, leading to a higher collector current for a given base current and collector-emitter voltage. The base-emitter voltage decreases with temperature, making it easier for the transistor to conduct. The output characteristic curves shift upward, indicating higher collector current at the same collector-emitter voltage .

Fig. III: Output Charac. at different temp.

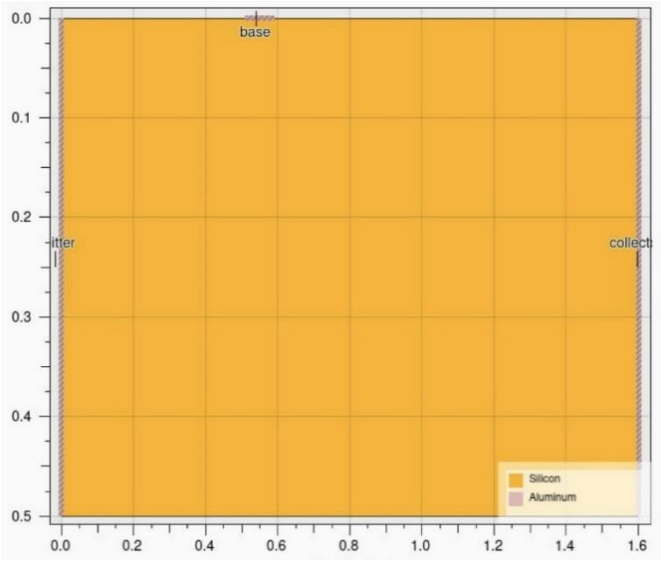


Fig. IV: Structure Profile

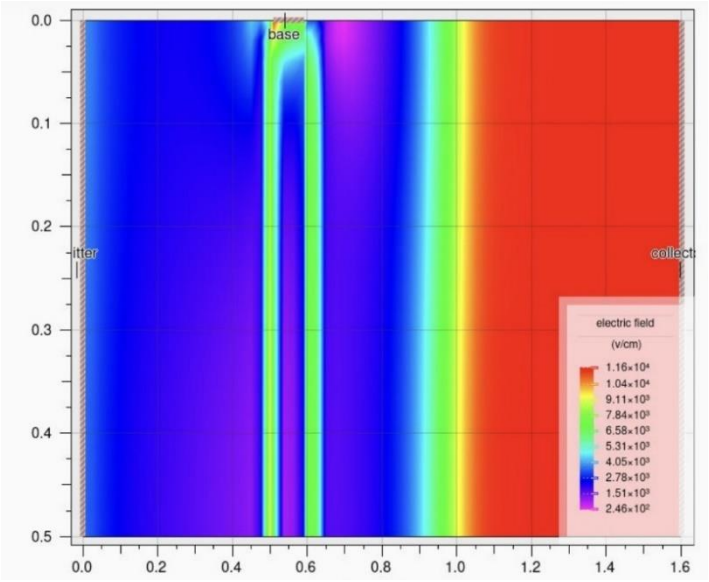


Fig. V: Electric Field

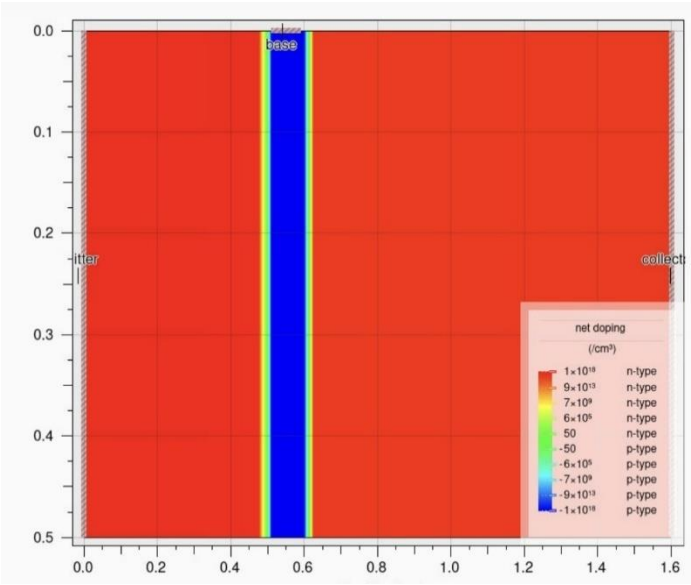


Fig: VI.Net Doping Profile

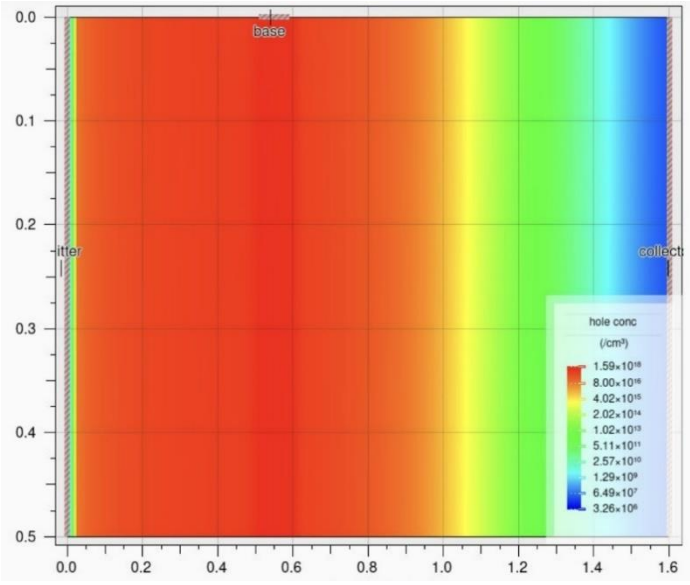


Fig: VIII.Hole Concentration

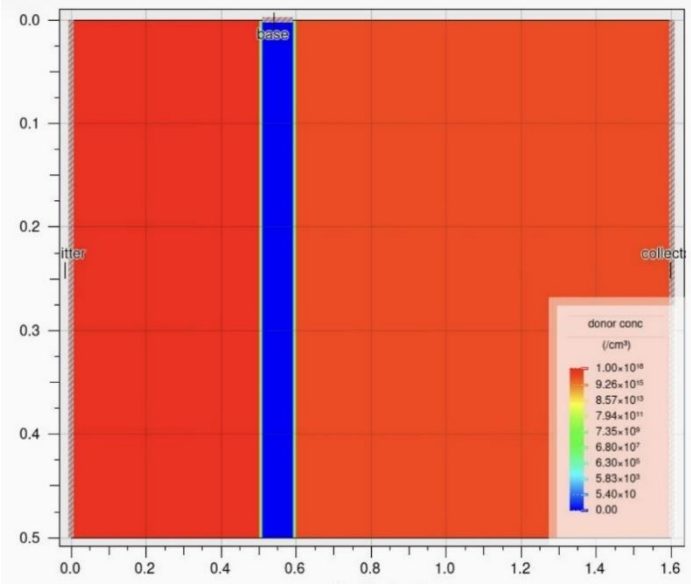


Fig. IX: Donor Conc.

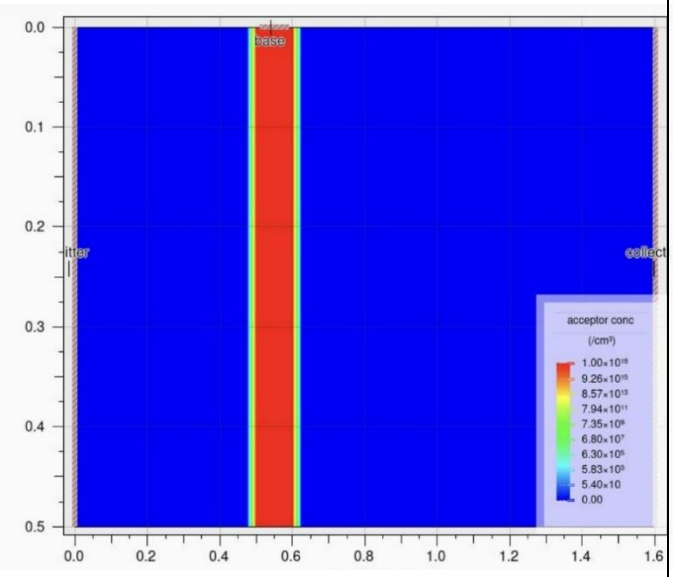


Fig. X: Acceptor Conc.

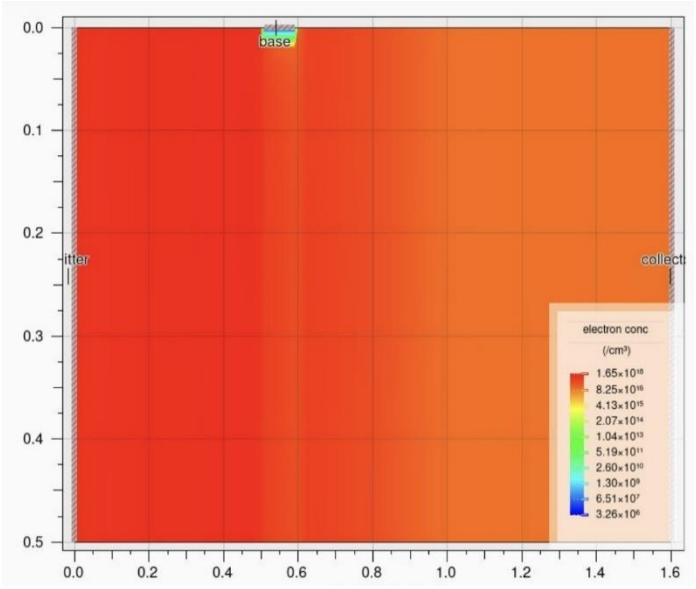


Fig. XI: Electron Conc.

Observations:

1. Structure Profile: The NPN transistor has three main regions: emitter (n-type), base (p-type), and collector (n-type). The emitter is heavily doped to supply a high concentration of electrons, the base is thin and lightly doped, and the collector is moderately doped.

2. Electric Field Profile: Strong electric fields are present at the emitter-base and base-collector junctions. The base-collector junction is reverse-biased, creating an electric field that sweeps electrons from the base to the collector, while the emitter-base junction is forward-biased, allowing electron injection into the base.

3. Acceptor Ion Concentration: Located in the p-type base, acceptor ions provide holes as majority carriers. The acceptor concentration in the base is lower than the donor concentration in the emitter and collector.

4. Meshing: Fine meshing is applied near the junctions for detailed simulation of the electric fields and carrier transport. Coarser meshing can be used in the bulk of the emitter, base, and collector regions for computational efficiency.

5. Net Profile Doping: The emitter is heavily doped (n+), ensuring a high electron injection rate. The base is lightly doped (p), while the collector is moderately doped (n) to support high voltage operation.

6. Electron Concentration: Highest in the n-type emitter, moderate in the n-type collector, and very low in the p-type base. Electrons injected from the emitter diffuse through the base and are swept into the collector by the electric field at the base-collector junction.

7. Hole Concentration: Highest in the p-type base, where holes are the majority carriers. Hole concentration is low in the n-type emitter and collector regions.

8. Donor Concentration: High donor concentration in the n-type emitter and collector. This high donor concentration supplies the primary source of electrons, crucial for the conduction process through the transistor.

Sources of Errors:

- Fine meshing is necessary around the emitter-base and base-collector junctions, where electric fields are high; poor meshing can lead to inaccurate results. Properly define contacts for each terminal (emitter,

base, and collector) to ensure accurate current flow; incorrect boundary conditions can introduce unwanted resistive effects.

- Incorrect doping levels or gradients in the emitter, base, and collector regions can impact the transistor's I-V characteristics and gain. Ensure accurate material properties, such as bandgap, mobility, and permittivity; temperature-dependent parameters must also be correctly set.

- NPN transistor performance is highly temperature-sensitive; incorrect temperature modeling can alter current gain and switching behavior.

- Accurate recombination models (e.g., SRH, Auger) are essential, particularly in the base region, to reflect real recombination rates and carrier dynamics.

Conclusion:

In this experiment, we found the following:

- We created contour plots showing various concentrations, including acceptors, donors, electrons, and holes.
    - These concentrations are represented by colors in the VIBGYOR spectrum.
- A contour plot of the electric field profile was also observed after analyzing the input and output characteristics.
- We examined the input and output characteristics of the BJT in the Common Base configuration at different temperatures (300K, 325K, 350K, 375K, and 400K).
    - For the input characteristics, as temperature increases, the current increases, and the threshold voltage decreases. This is due to the effects of the electric field, as shown in the electric field profile.
    - For the output characteristics, the current also increases with temperature, again due to changes in the electric field.
- When we adjusted the doping profile, there was no noticeable change in the input and output characteristics. However, we did observe differences in the contour plots for electron and hole concentrations, as well as a clear change in the BJT's electric field profile.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze

Experiment-04

NPN Transistor in Common Collector Configuration

Aim: To simulate an NPN transistor in the common collector configuration, analyze its input and output characteristics, and study the influence of base width and doping on performance. Evaluate the contour plots and electric field profiles across junctions in active, saturation, and cutoff modes, and investigate the effects of temperature variations (300K, 325K, 350K, 375K, 400K) on electric field, depletion region, and transistor operation.

Theory:

This is one of the basic BJT amplifier configurations, commonly known as the Common Collector (CC) configuration or emitter follower. Here, the collector forms the common terminal for both input and output circuits. The input is taken between base and collector, and the output is taken between the emitter and collector.

The basic application of the CC configuration is impedance matching and as a buffer of voltage, since the input impedance is high, and the output impedance is low. Additionally, the output voltage is an exact replica of the input voltage; thus, it is useful when an above-average strength of the output signal that matches the input voltage is required.

Input Characteristics:

Input characteristics In CC configuration, input characteristics represent the relationship between base-emitter voltage and the base current. For a given value of collector-emitter voltage It essentially has all characteristics of a forward-biased p-n junction because in active mode base-emitter junction is forward-biased.

Output Characteristics

The output characteristics in the CC configuration describe how the collector-emitter voltage varies with the emitter current for different levels of base current These curves show how the emitter current changes with collector-emitter voltages at fixed values of base current.

- **Active Region**: $V_{be}$is forward-biased, V_{ce} is high enough to keep the transistor active. The output voltage follows the input voltage.
- **Saturation Region**: Both : V_{be} and , V_{ce} are forward-biased, and the transistor acts like a closed switch, with maximum current flowing.
- **Cutoff Region**: The base-emitter junction is not forward-biased, resulting in minimal current flow, effectively turning the transistor off.

Procedure:

1. Open Silvaco TCAD software, Create a new project and name it appropriately.
2. Use the `Mesh` command to define the mesh for your NPN transistor structure. This includes specifying the grid points and spacing.
3. Define Regions using the `Region` command to define the different regions of the NPN transistor, such as the emitter, base, and collector regions.
4. Use the `Electrode` command to define the emitter, base, and collector electrodes.
5. Specify Material Specification by the `Material` command for each region (e.g., silicon for the semiconductor regions) and define the doping concentrations for the emitter, base, and collector regions using the `Doping` command.
6. Specify the `Model` command to specify the physical models for the simulation
7. Run the Simulation using `Run` command to start the simulation, Monitor the simulation progress and check for any errors or warnings.
8. Analyze Results and Save the simulation results and plots for further analysis and documentation.

Simulation Code:

```
go victorydevice

mesh width = 1
#x-mesh #
x.m l=0.00 s=0.01
x.m l=0.50 s=0.01
x.m l=0.51 s=0.01
x.m l=0.59 s=0.01
x.m l=0.6 s=0.01
x.m l=1.6 s=0.01

#y-mesh#
y.m l=0 s=0.01
y.m l=0.5 s=0.01

#region#
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =air
region num=1 x.min=0 x.max=1.6 y.min=0 y.max=0.5 mat =Si

#Doping#
doping uniform n.type conc=1e18 x.min=0.0 x.max=0.5 y.min=0 y.max=0.5
doping uniform p.type conc=1e18 x.min=0.5 x.max=0.6 y.min=0 y.max=0.5
doping uniform n.type conc=1e17 x.min=0.6 x.max=1.6 y.min=0 y.max=0.5

#Electrode#
elec name=emitter x.min=0 x.max=0 y.min=0 y.max=0.5
elec name=base x.min=0.51 x.max=0.59 y.min=0 y.max=0
elec name=collector x.min=1.6 x.max=1.6 y.min=0 y.max=0.5

#contact#
contact name=emitter neutral
contact name=base neutral
contact name=collector neutral

#models #
models print srh temp=300
#output#
output con.band val.band

#method#
method newton trap maxtrap=30 itlim=30
solve init
save outf=bjtinput.str
#IV Input#
log outf=IV_CB_input.log
solve vbase=0 vstep=0.05 vfinal=1 name=base
quit
```

Result And Discussion:

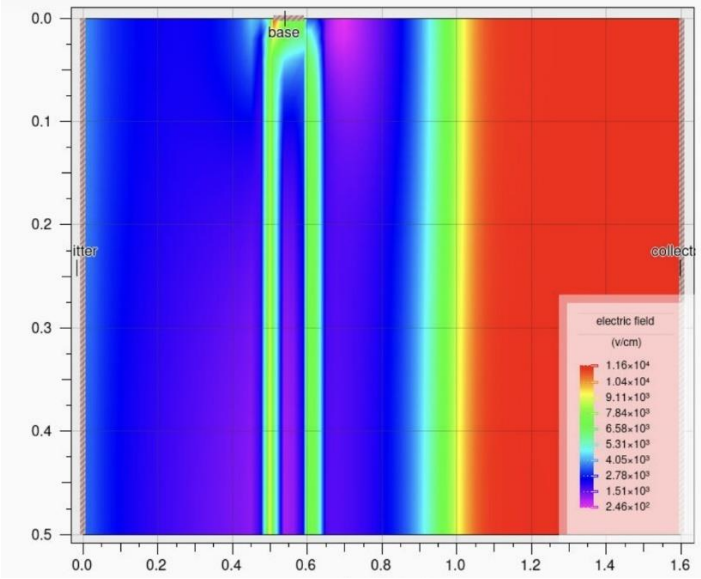


Fig:I. Electric Field Profile

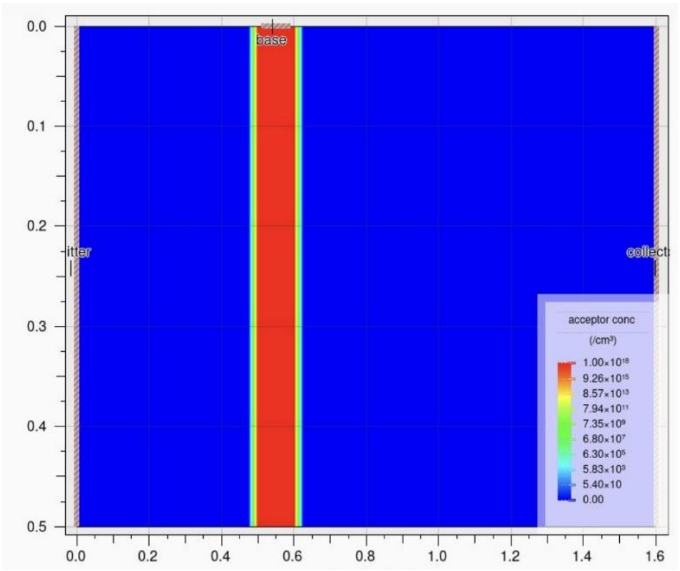


Fig:II. Acceptor Concentration

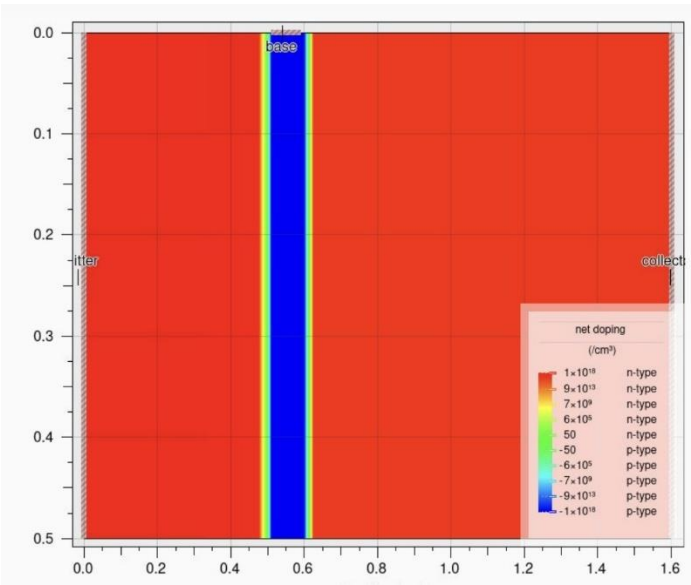


Fig:III. Net Doping Profile

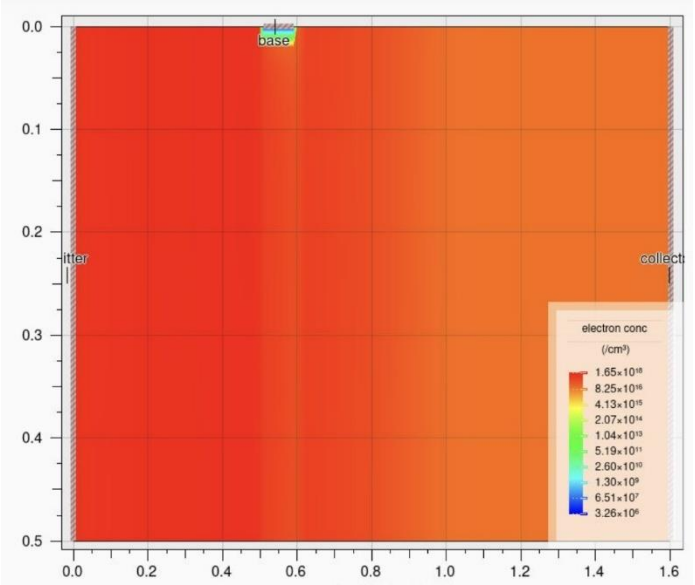


Fig:IV. Electron Concentration

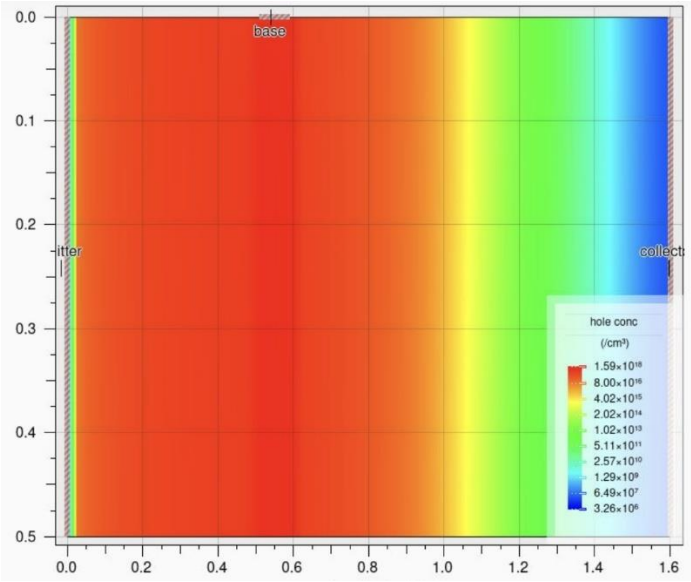


Fig:V. Hole Concentration

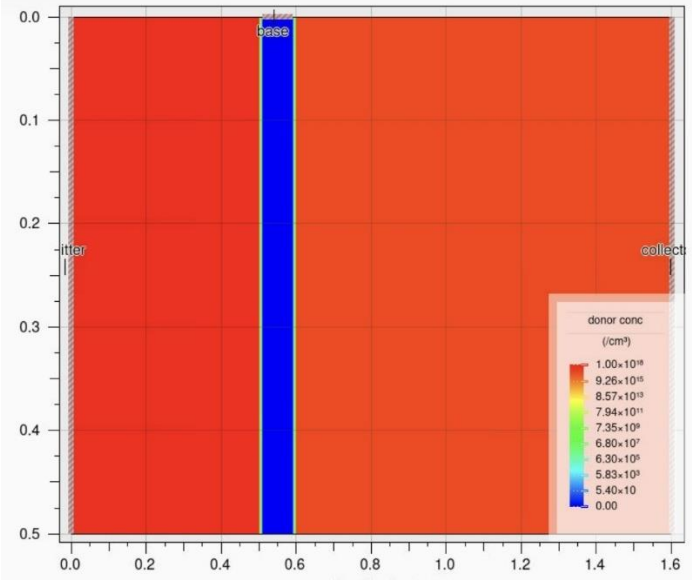


Fig:VI. Donor Concentration

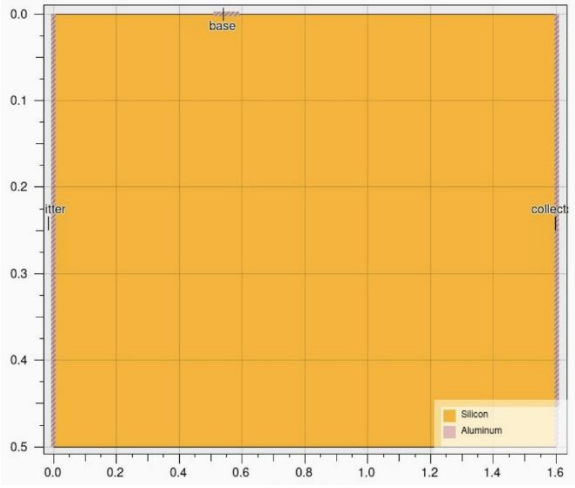


Fig.VII. Structure Profile

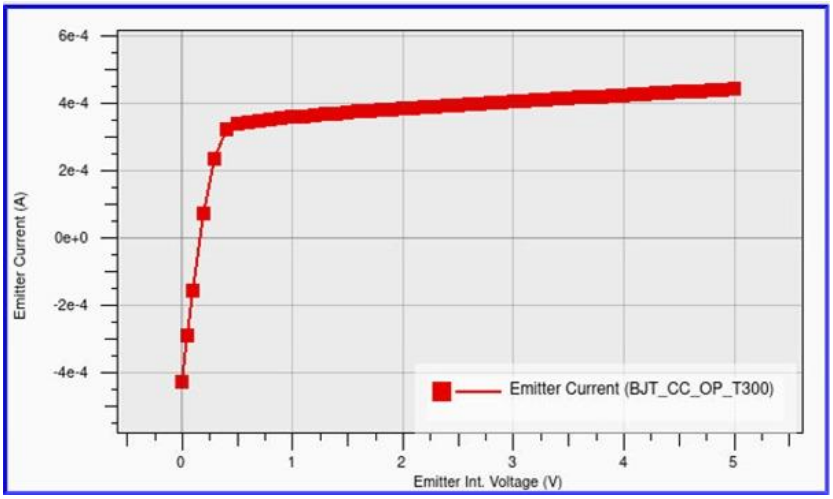


Fig. VIII. Output Characteristics of CC

The output characteristics of an NPN transistor in the common-collector (CC) configuration, often called an emitter follower, show the relationship between the collector-emitter voltage and the collector current for different base currents. In the CC configuration, the base is the input terminal, and the emitter serves as the output terminal. The output characteristics typically show a near-constant collector current (which is nearly equal to the emitter current) as collector-emitter voltage increases, once the transistor is in the active region. This results in a flat output curve with a slight rise in collector current at low collector-emitter voltage values due to the transistor's operation in the active region. The voltage gain is close to 1 (unity) in the CC configuration, making it useful for impedance matching, while the current gain is high. The output curve shows that collector-emitter voltage remains relatively stable, and any variations in collector current are primarily controlled by changes in the base current base current, which results in small variations in emitter current. Overall, the common-collector configuration provides high current gain, a low output impedance, and is often used in buffering and impedance matching applications.

Observations:

1. Structure Profile: The NPN transistor consists of three regions—the emitter (n-type), base (p-type), and collector (n-type). The emitter is heavily doped to ensure a high concentration of electrons, the base is lightly doped and thin to allow efficient electron flow, and the collector is moderately doped.

2. Electric Field Profile: Electric fields are concentrated at the emitter-base and base-collector junctions. The forward bias at the emitter-base junction allows electron injection into the base, while the reverse bias at the base-collector junction creates an electric field that directs electrons from the base toward the collector.

3. Acceptor Ion Concentration: Acceptor ions in the p-type base region provide a concentration of holes as majority carriers. The base doping (acceptor concentration) is lower compared to the donor concentration in the emitter and collector.

4. Meshing: For accurate simulation, fine meshing is applied near the junctions where the electric fields and carrier gradients are highest. Coarser meshing is used in the bulk areas of the emitter, base, and collector to optimize computational efficiency.

5. Net Profile Doping: The emitter is heavily doped (n+) to provide a strong source of electrons, while the base is lightly doped (p) to allow easy passage of electrons without much recombination. The collector is moderately doped (n) to handle high voltages.

6. Electron Concentration: The electron concentration is highest in the n-type emitter, moderate in the n-type collector, and very low in the p-type base. Electrons injected from the emitter move through the base and are attracted to the collector.

7. Hole Concentration: Hole concentration is highest in the p-type base region, where holes are the majority carriers. It is low in the n-type emitter and collector regions.

8. Donor Concentration: High donor concentration in the n-type emitter and collector regions supplies the electrons necessary for current flow through the transistor.

Sources of Errors:

- Fine meshing is necessary around the emitter-base and base-collector junctions, where electric fields are high; poor meshing can lead to inaccurate results. Properly define contacts for each terminal (emitter, base, and collector) to ensure accurate current flow; incorrect boundary conditions can introduce unwanted resistive effects.
- Incorrect doping levels or gradients in the emitter, base, and collector regions can impact the transistor's I-V characteristics and gain. Ensure accurate material properties, such as bandgap, mobility, and permittivity; temperature-dependent parameters must also be correctly set.
- NPN transistor performance is highly temperature-sensitive; incorrect temperature modeling can alter current gain and switching behavior.
- Accurate recombination models (e.g., SRH, Auger) are essential, particularly in the base region, to reflect real recombination rates and carrier dynamics.

Conclusion:

- Contour plots were created to show the concentrations of acceptors, donors, electrons, and holes.
    - The concentration levels in these plots are shown by the colors of the VIBGYOR spectrum.
- We also generated a contour plot of the electric field profile after analyzing the input and output characteristics.
- Active Region: In the Common Collector (CC) configuration, the BJT works efficiently with the emitter-base (EB) junction forward-biased and the collector-base (CB) junction reverse-biased. This setup allows most electrons from the emitter to reach the collector. The emitter current is closely tied to the base current, and the output voltage closely follows the input voltage, minus the base-emitter drop.
- Depletion Region: The EB junction's depletion region is narrow, while the CB junction's depletion region widens under reverse bias. This affects how carriers move and recombine.
- Electric Field Profile: The electric field in the EB junction helps inject carriers, while the strong field in the CB junction ensures efficient carrier collection.
- We observed the input and output characteristics of the BJT in the Common Collector configuration at different temperatures (300K, 325K, 350K, 375K, and 400K).
    - For the input characteristics, the threshold voltage increases as temperature increases, due to changes in the electric field.
    - For the output characteristics, the current also increases with temperature, again due to the electric field changes.

- When we adjusted the doping profile, there was no significant change in the input and output characteristics. However, we did see differences in the contour plots for electron and hole concentrations, and a noticeable change in the electric field profile of the BJT.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze

Experiment-05

MOS Capacitor C-V Characteristics

Aim: To simulate a MOS capacitor with p-type bulk silicon and study its capacitance-voltage (C-V) characteristics at frequencies between 10 Hz and 1 kHz. Determine the maximum and minimum capacitance values, analyse threshold voltage for surface inversion, and verify surface inversion through structural files in OFF and ON states. Investigate the effect of ambient temperature (300K, 325K, 350K, 375K, 400K) on C-V characteristics and threshold voltage.

Theory:

MOS capacitance is the capacitance observed in the structure of MOS, which is made up of a metal gate and an oxide insulating layer with a semiconductor, typically silicon. It is an essential building block for the MOSFETs and plays a significant role in how such a device switch on/off.
When the applied voltage is given to the metal gate, it affects the charge distribution in a semiconductor. Depending upon the applied voltage, MOS capacitors can function in three different regions,

1. **Accumulation:** Accumulation occurs when the gate voltage is low. In such a scenario, with a positive voltage for an n-type and a negative for a p-type semiconductor, the majority carriers, i.e., electrons for an n type or holes for a p type, accumulate near the oxide layer, and the capacitance increases.

2. **Depletion:** If the gate voltage is increased above the threshold, then this forces most of the majority carriers away from the oxide layer and puts them into depletion region of immobile ions, and consequently, capacitance decreases.

3. **Inversion:** At even higher gate voltages, minority carriers (holes in an n-type or electrons in a p-type) are attracted to the surface, forming an inversion layer of carriers that aids in current conduction. This inversion layer acts as if it were a conductive channel; the MOS capacitance is stable.
The MOS capacitance varies with applied voltage, as the depletion region width depends on the magnitude of the electric field between the gate and semiconductor. This is why MOS capacitors are of prime importance in understanding the behavior of MOSFETs in any digital circuit where they act as switches by flipping between the on and off states.

The I-V (current-voltage) characteristics of p-type MOS capacitor describe how the current in the metal gate changes with the applied voltage to the semiconductor (p-type) underneath. As the gate voltage varies, the p-type MOS capacitor goes through various modes-accumulation, depletion, and inversion. Under accumulation mode-negative gate voltage), holes are in accumulation near the oxide layer, thereby leading to minimum current. As the gate voltage increases-as is less negative-the device goes into depletion mode, where holes are pushed away, and a depletion region with immobile ions forms that cuts off current. At a sufficiently positive gate voltage, inversion occurs, and electrons-minority carriers-form a conductive layer near the oxide interface, which permits current flow as if the surface were n-type. This behavior defines the characteristic I-V response of the p-type MOS capacitor, which is of paramount importance for switching and charge storage in MOSFETs.

Electric Field Profiles of P-type MOS Capacitor:- The voltage-graded profile of electric field in a p-type silicon substrate-based metal-oxide-semiconductor (MOS)
capacitor must be understood first in order to examine the variations of charge carrier behaviour and capacitance with applied voltages.
Physics based models invoked in TCAD code:
In TCAD simulations of a p-type MOS capacitor, various physics-based models are used to capture detailed behaviors of carrier dynamics, electric field distributions, and capacitance variations for different biasing conditions. The key models and their relevance to the simulation are presented in the subtopics below:

1. **Drift-Diffusion Model :-**

This model represents carrier motion by drift (response to electric fields) and diffusion (response to gradients in carrier concentration).

2. **Poisson's Equation Solver :-**

The MOS structure must be solved in terms of Poisson's equation for the determination of electric field and potential distribution along the MOS structure.

3. Shockley-Read-Hall (SRH) Recombination Model :-

This model takes into account recombination of electrons with holes through trap states in the bandgap. This generally happens due to semiconductor defects or impurities.

4. **Quantum Mechanical Effects :-**

As the device dimensions have become smaller, quantum mechanical effects, especially quantum confinement of carriers at the semiconductor-oxide interface, become important.
Quantum mechanical models are essential to predict the appropriate behavior of the p-type MOS capacitor at very small scales, especially when high electric fields become involved and the traditional classical models fail to account for the spatial quantization of carriers near the oxide interface.

5. **Thermal Effects Model :-**

This model incorporates temperature dependence for carrier mobility and generation-recombination rates, as these are sensitive to thermal energy.

All these physics-based models are essential in simulating the behavior of the p-type MOS capacitor for a range of operating conditions such as accumulation, depletion, and inversion. With such models included, the TCAD is gaining insights into crucial characteristic factors, for instance, capacitance variation, electric field distribution, and leakage currents .

Procedure:

1. Open Silvaco TCAD software, Create a new project and name it appropriately.
2. Use the `Mesh` command to define the mesh for the MOS Diode structure. This includes specifying the grid points and spacing.
3. Define Regions using the `Region` command to define the different regions of the MOS Diode, such as the gate, body.
4. Use the `Electrode` command to define the gate, body electrodes.
5. Specify Material Specification by the `Material` command for each region (e.g., silicon for the semiconductor regions) and define the doping concentrations for the p and n regions using the `Doping` command.
6. Specify the `Model` command to specify the physical models for the simulation
7. Run the Simulation using `Run` command to start the simulation, Monitor the simulation progress and check for any errors or warnings.
8. Analyze Results and Save the simulation results and plots for further analysis and documentation.

Simulation Code:

```
go victorydevice

mesh width = 1

# x - mesh #
x.m l=0.0 s=0.025
x.m l = 1 s = 0.025

# y- mesh#
y.m l=0.0 s=0.025
y.m l=0.010 s=0.025
```

```
y.m l=0.012 s=0.025
y.m l=0.212 s=0.025
y.m l=0.222 s=0.025

#Region#
region num=1 x.min=0 x.max=1 y.min=0 y.max=0.222 mat=air
region num=2 x.min=0 x.max=1 y.min=0.0 y.max=0.012 mat=oxide
region num=3 x.min=0 x.max=1 y.min=0.012 y.max=0.222 mat=Si

# Doping #
doping uniform p.type conc=1e15 x.min=0.0 x.max= 1 y.min = 0.012 y.max = 0.212

# Electrodes #
elec name= gate x.min = 0 x.max = 1 y.min= 0.0 y.max = 0.0
elec name= body x.min = 0 x.max = 1 y.min= 0.212 y.max = 0.222

# contact #
contact name = gate work = 4.2
contact name = body neutral

# models #
models print mos

#output#
output con.band val.band

#method#
method newton trap maxtrap=30 itlim=30
solve init
save outf=mos.str

#CV#
solve vgate=0 vstep= -0.2 vfinal= -2 name = gate
log outf = CV_1000Hz.log

solve vgate= -2 vstep=0.05 vfinal=2 name=gate ac freq = 1000

#turn off logging#
log off
#save final structure#
save outf=mos_final.str

quit
```

Result and Discussion:

The **C-V characteristics** of a **MOS diode** show the relationship between the **capacitance** and the **applied gate voltage**. These characteristics typically exhibit three key regions:

1. **Accumulation**: When a negative voltage is applied (for a p-type substrate), the capacitance is high and is dominated by the oxide capacitance, as the surface of the semiconductor accumulates charge.
2. **Depletion**: As the voltage approaches 0V, the capacitance decreases due to the widening depletion region at the oxide-semiconductor interface.
3. **Inversion**: With a sufficiently positive gate voltage (for p-type substrate), an inversion layer forms, and the capacitance becomes very small, dominated by the oxide layer again.

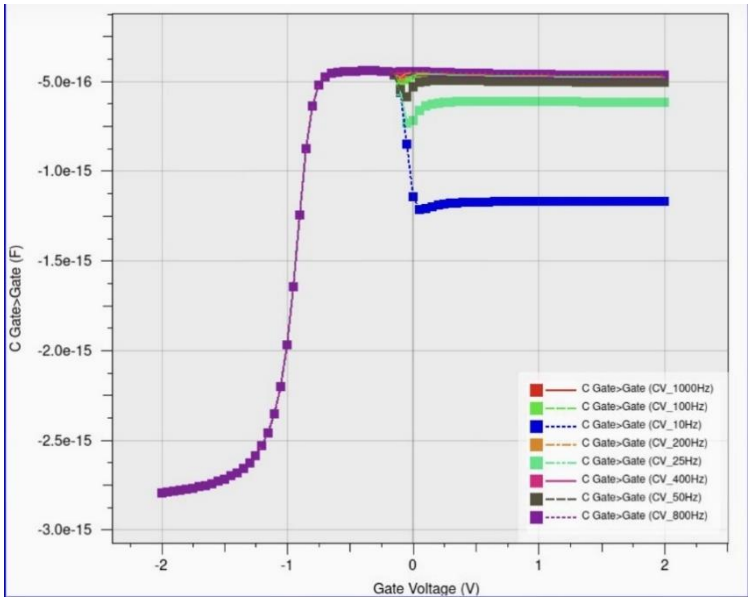


Fig.I: CV Characteristics of MOS diode

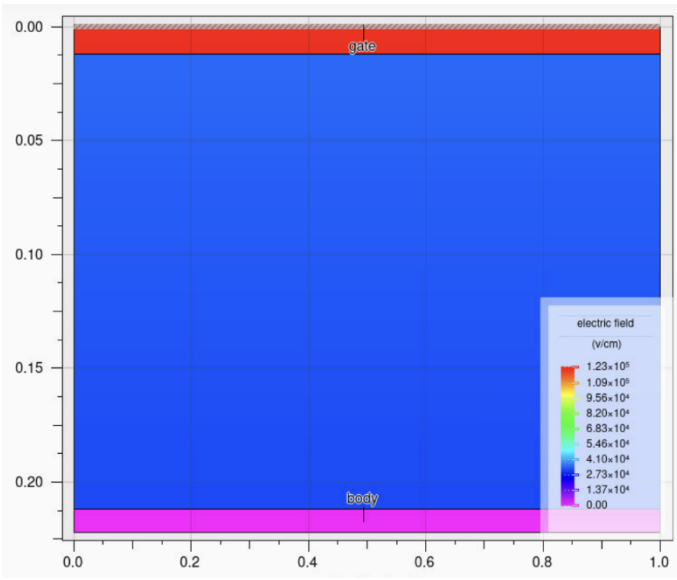


Fig: II. Electric field of MOS Diode

Sources of Errors:

- Using inaccurate values for oxide thickness, doping concentrations, or mobility can lead to incorrect simulation results.
- Improperly set boundary conditions or non-ideal contacts can result in inaccurate simulations.
- Failing to account for temperature variations can result in errors in characteristics like threshold voltage or capacitance.

Conclusion:

Temperature Effects:
Because of their influence on carrier mobility, intrinsic carrier concentration, and recombination rates, it has a big effect on semiconductor devices' behavior and characteristics. In devices like diodes and MOS capacitors, saturation current increases with higher temperatures, but in MOSFETs, it tends to decrease with greater values of threshold voltage. These effects are highly crucial to the overall device performance, especially where the thermal stability factor would be considered important in power applications. The predictions made by the help of varying temperatures over the behavior of a device will help us to design for better reliability and efficiency.
Depletion Region and Electric Field:
Understanding the nature of an electric field and a depletion region helps in understanding the nature of operation of MOS devices under accumulation, depletion, or inversion modes or the behavior of a PN junction under forward and reverse bias. The strength of the electric field within the depletion region decides how charges spread out spatially around the same and that influences the value of high potentials as barriers to conduction or non-conduction. These factors decide these abilities and are essentially very essential in a device, particularly transistors, which can control current flow and switching time; these effects increase with minimization sizes.
Specific Performance Parameters for Individual Devices Each semiconductor device has specific performance parameters; for instance, the diodes are expressed as knee voltage, base width, switching properties, and conduction properties. MOSFETs, on the other hand are described by other parameters of threshold voltage, on/off ratio, and susceptibility to short channel effects for a scaled-down technology. Those parameters describe the efficiency, speed, and scaling of a device-a holy trinity of factors in creating precision and reliability for both digital and analog electronics.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze

Experiment – 06
N-Channel MOSFET Scaling Effects

Aim: To simulate the output and transfer characteristics of an n-channel MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyse the performance implications of scaling.

Theory:

MOSFETs

A Metal-Oxide-Semiconductor Field-Effect Transistor is one of the transistors that can be used to amplify or switch electronic signals. It is a core component in modern electronics present in computers, mobile phones, and many industrial applications.

Structure

A MOSFET consists of a three-layered structure which includes the metal gate, the oxide layer, and the semiconductor body. The semiconductor body has normally two layers doped differently: one is usually called source and the other is called drain, the former being controlled by the latter as to how the current flows between them.

Working Principle

MOSFETs are based on the electric field effect where their operation depends on applying a voltage to the gate terminal. This creates an electric field that modifies the conductivity of the semiconductor channel between the source and the drain. Thus, the current from the source to the drain is controlled by the gate voltage.

1. Threshold Voltage (Vth): The minimum gate voltage required to create the channel of conduction between the source and drain
2. Operation Modes: There are three modes of operation in a MOSFET depending upon the gate-source voltage Vgs
    - Cut-off Mode- When the source-gate voltage Vgs< Vth, no current flows through the channel.
    - Triode Mode- For Vgs> Vth and Vds < (Vgs - Vth), it acts as a resistor.
    - Saturation Mode: Vgs > Vth and Vds >= (Vgs - Vth), the device is turned fully on, and current flow is controlled by Vgs.

n-Channel MOSFET

An n-channel MOSFET (nMOS) uses electrons as charge carriers; compared to a p-channel MOSFET, the use of electrons leads to higher mobility of electrons over holes. Thus, for specific applications, devices made of nMOS are normally faster and more efficient compared to pMOS.

nMOS

1. Source and Drain: Both are n-type semiconductors.
2. Substrate: Typically, p-type.
3. Current Flow: When the voltage applied to the gate is positive, it attracts electrons toward the gate and hence a conductive channel would be formed between the n-type source and drain.
4. Applications: Due to their speed and efficiency, nMOS transistors have more instances in digital circuits, power management, and RF applications.

Short-Channel Effects (SCEs)

• Threshold Voltage Roll-Off: This is since threshold voltage goes downward with decrease in channel length, which will deteriorate the turn-on characteristics.
• DIBL (Drain Induced Barrier Lowering): The threshold voltage will further degrade with an increase in the drain voltage, and there will be more leakage current due to DIBL.
• Subthreshold Slope: As the channel length comes down, the subthreshold slope decreases and reduces the capability to switch the transistor fully off.

Temperature Dependency

• Maximum Drain Current: In general, higher temperature increases the carrier mobility that can be used to enhance the maximum drain current.

• Threshold Voltage: The threshold voltage depends on temperature; therefore, it becomes a cause of noise and deteriorates the performance of the device.
• Early Effect: The Early effect or channel length modulation is sensitive to fluctuation in temperature and, therefore affects the output characteristic.
•Channel Length Modulation: At high temperatures, the channel length modulation. Therefore, linearity suffers in this case.

Scaling Implications to Improve Performance

•Speed and Power Consumption: Thus, with shrinking gate lengths, switching indeed occurs much faster but power consumption is much higher than leakage current.
•Reliability: The short-channel effect coupled with the variation in temperature reduces the lifetime as well as the reliability of a device.
• Design Complexity: With the increasing miniaturization of the device, these effects become much harder to control and require sophisticated materials along with advanced design techniques.

Procedures:

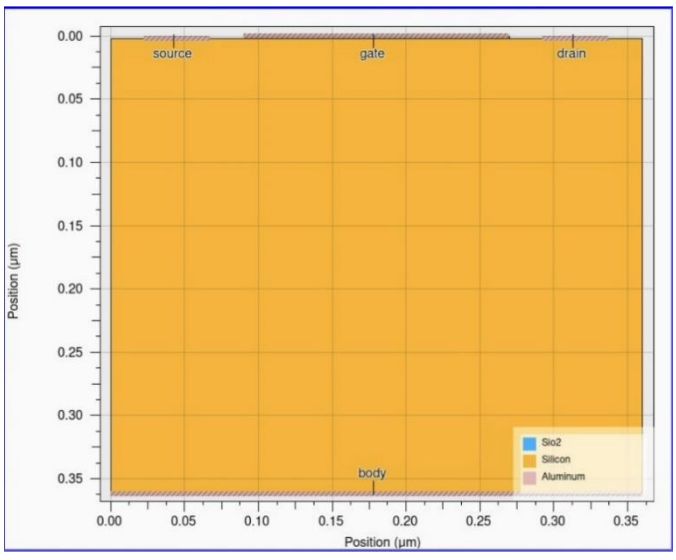
1. Open Silvaco TCAD software in nanohub.org, create a new project and name it properly.
2. Now in `Mesh` define mesh for MOSFET structure, for which you have to define grid points and spacing.
3. Specify different Regions of the MOSFET, such as the silicon substrate, the oxide layer, and air using the `Region` command.
4. Specify Electrodes by using the `Electrode` command to specify the source, drain, and gate electrodes.
5. Specify Material using the `Material` command to identify the material for each region; for example, silicon, silicon dioxide.
6. Use the `Doping` command to specify the doping concentrations for the source, drain, and substrate regions.
7. Give Model Specification by using the `Model` command to specify the physical models for your simulation, such as mobility models and recombination models.
8. Run the Simulation by using the `Run` command to start running the simulation. Monitor the progress of the simulation to ensure that there are no error or warning messages.
9. Analyse the results obtained from the simulation with plots for analysis and documentation.

Simulation Code:

```
go victorydevice

mesh width = 1

# x - mesh #
x.m l=0.00 s=0.025
x.m l=0.09 s=0.025
x.m l=0.27 s=0.025
x.m l=0.36 s=0.025

# y- mesh#
y.m l=0.000 s=0.025
y.m l=0.002 s=0.025
y.m l=0.092 s=0.025
y.m l=0.362 s=0.025

#Region#
region num=1 x.min=0.00 x.max=0.36 y.min=0.0 y.max=0.362 mat=air
region num=2 x.min=0.09 x.max=0.27 y.min=0.0 y.max=0.002 mat=oxide
region num=3 x.min=0 x.max=0.36 y.min=0.012 y.max=0.362 mat=Si

# Doping #
```

```
doping uniform n.type conc=1e19 x.min=0.00 x.max=0.09 y.min = 0.002 y.max = 0.092
doping uniform p.type conc=1e15 x.min=0.00 x.max=0.36 y.min = 0.092 y.max = 0.362
doping uniform p.type conc=1e15 x.min=0.09 x.max=0.27 y.min = 0.002 y.max = 0.092
doping uniform n.type conc=1e19 x.min=0.27 x.max=0.36 y.min = 0.002 y.max = 0.092

# Electrodes #
elec name= gate x.min = 0.09 x.max = 0.27 y.min= 0.0 y.max = 0.0
elec name= source x.min = 0.01 x.max = 0.08 y.min= 0.002 y.max = 0.002
elec name= drain x.min = 0.28 x.max = 0.35 y.min= 0.002 y.max = 0.002
elec name= body x.min = 0 x.max = 0.36 y.min= 0.362 y.max = 0.362


# contact #
contact name = gate work = 4.2
contact name = body neutral
contact name = source neutral
contact name = drain neutral

# models #
models print mos temp=300
#output#
output con.band val.band
#method#
method newton trap maxtrap=30 itlim=30
solve init
save outf=n_mosfet.str
#IV#
solve vdrain=0 vstep= 0.2 vfinal= 0.2 name = drain
log outf = IdVg_Vds300.log
solve vgate= -2 vstep=0.6 vfinal=20 name=gate
#turn off logging#
log off
#save final structure#
save outf=mos_final.str
quit
```

Result And Discussion:



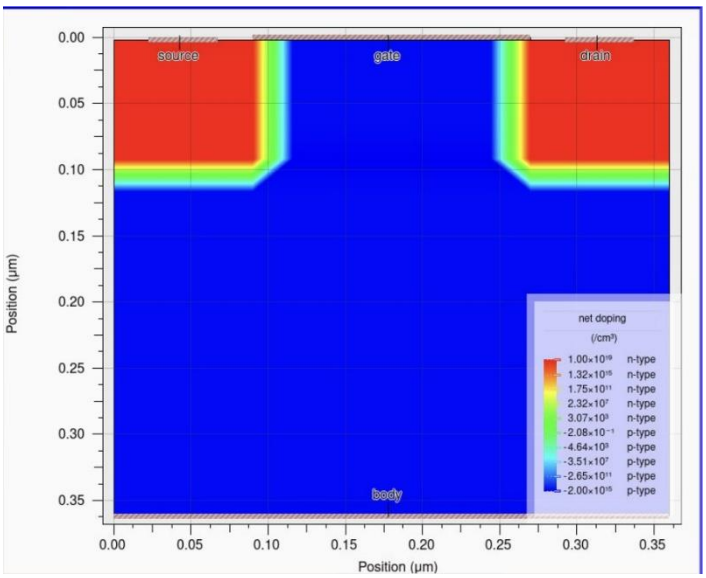


Fig.I: Structure Profile

Fig.II : Net Doping

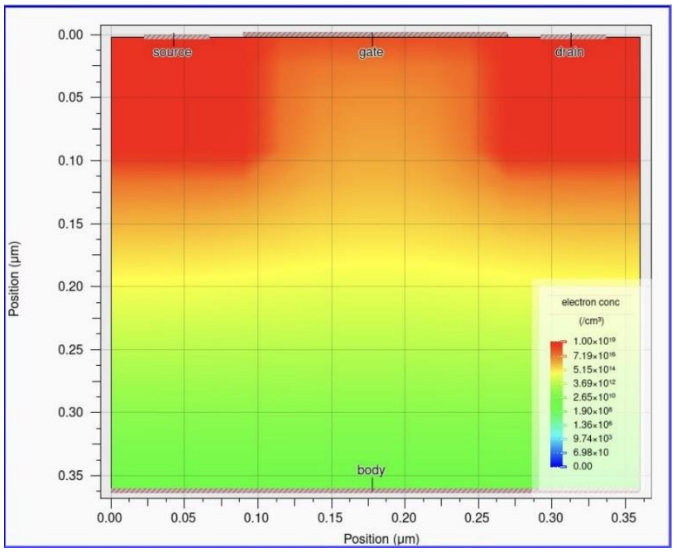


Fig:III. Electron Concentration

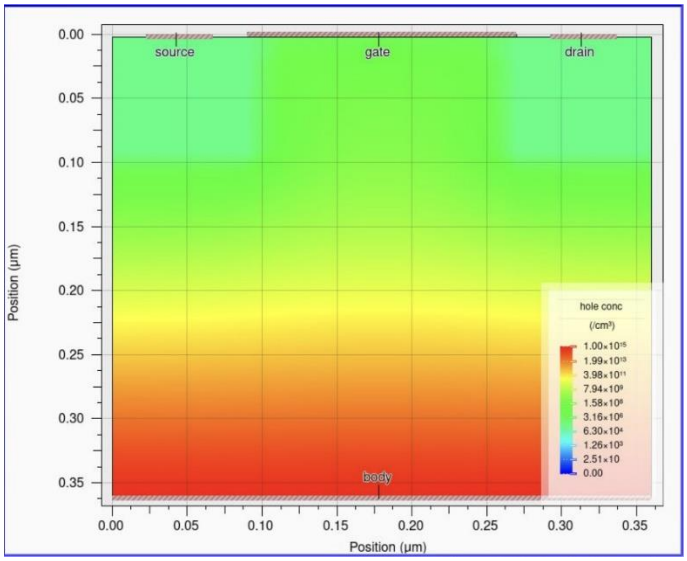


Fig:IV. Hole Concentration

Input Characteristics:

The IV characteristics of an N-MOSFET are essential for understanding its behaviour in different regions of operation and designing circuits that utilize MOSFETs for switching and amplification. The key parameters influencing the characteristics include the threshold voltage (Vth), gate-source voltage (VGS), and drain-source voltage (VDS).

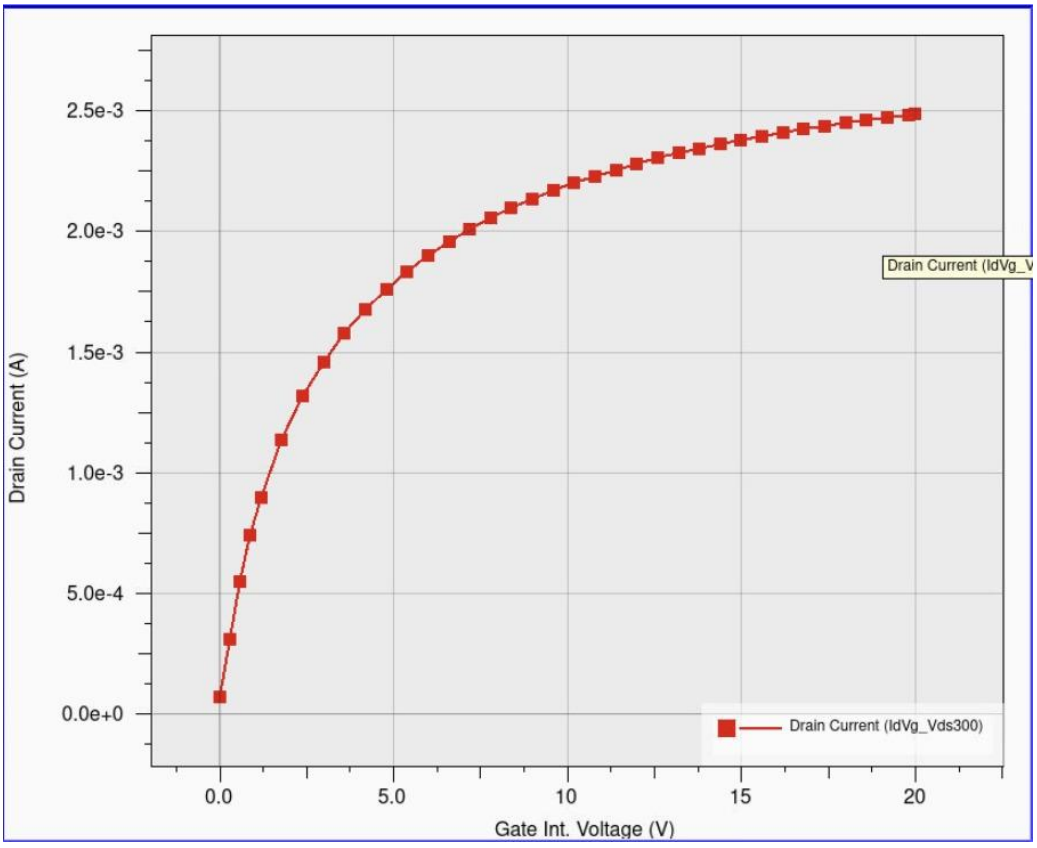


Fig. V. I-V Characteristic of N-MOSFET at 300 K

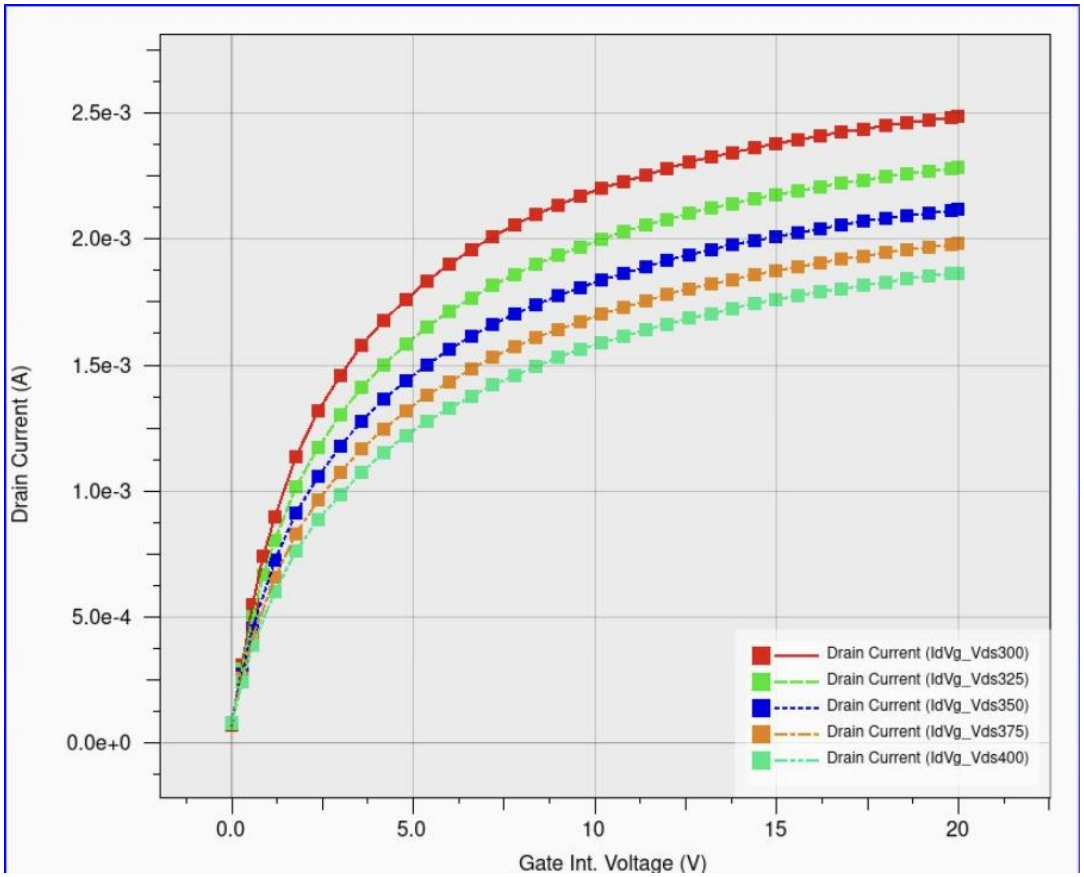


Fig. VI. I-V Characteristics of N-MOSFET at different temp. (300K, 325K, 350K, 375K, 400K)

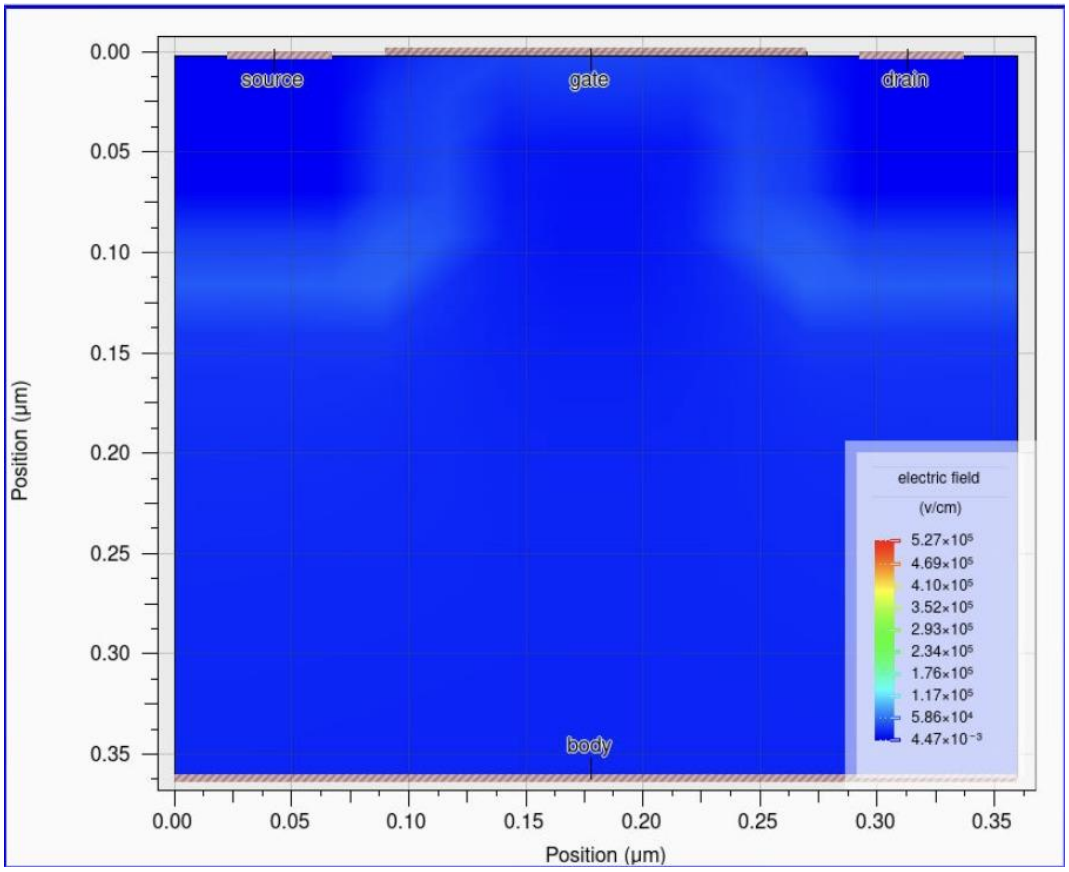


Fig:VII. Electric Field Profile

Observations:

1. Temperature Effects:
    - Threshold Voltage decreases with increasing temperature.
    - Subthreshold slope becomes steeper, making the MOSFET switch on more sharply.
    - Leakage currents increase due to higher intrinsic carrier concentration.

2. Doping Concentration Effects:
    - Higher doping reduces Vth and increases channel conductivity.
    - Increased doping can reduce carrier mobility due to scattering.

3. Electric Field Effects:
    - Higher electric field increases inversion, enabling more current flow.
    - At high electric fields, velocity saturation occurs, reducing mobility and current.
    - Excessive electric fields can cause avalanche breakdown.

4. Carrier Concentration Effects:
    - Electron concentration increases in the inversion layer for n-channel MOSFETs, boosting Id.
    - Hole concentration increases for p-channel MOSFETs, enabling current conduction.
    - Mobility decreases with higher temperature and doping levels.

5. Gate-Source Voltage Effects:
    - In the linear region, Id increases with Vgs.
    - In the saturation region, Id becomes mostly dependent on Vgs and less on Vds.

Sources of Error

- Using inaccurate values for oxide thickness, doping concentrations, or mobility can lead to incorrect simulation results.
- Improperly set boundary conditions or non-ideal contacts can result in inaccurate simulations.
- Failing to account for temperature variations can result in errors in characteristics like threshold voltage or capacitance.
- Simplified models may not account for effects like quantum tunneling**,** interface traps**,** or oxide defects**,** leading to discrepancies in the simulation.

Conclusion:

The simulation of the MOSFET provides valuable insights into device behavior, including the impact of temperature, doping, and electric fields on performance. Accurate simulation requires precise material parameters, refined meshing, and proper solver settings for convergence. While simulations offer detailed I-V characteristics, they must be validated against experimental data to ensure reliability. Parasitic effects, such as contact resistance and capacitances, should also be considered for high-accuracy results, especially for high-speed applications.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze
3. Silvaco User Guide Manual.

Experiment-07

N-Channel NMOSFET vs. PD-SOI MOSFET

Aim: To simulate and compare the output and transfer characteristics of an n-channel NMOSFET and a partially-depleted (PD) SOI MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyze the performance implications of scaling.

Theory:

N-Channel NMOSFET

An N-channel Metal-Oxide-Semiconductor Field-Effect Transistor (NMOSFET) is a type of FET in which an electric field governs the channel's conductivity made from n-type semiconductor material. This is one of the most commonly used transistors in any of the digital and analog circuits because it has high mobility for electrons and it can be switched very quickly. Here is a decomposition of its structure, operation, and characteristics:

Structure

1. Substrate: NMOSFET is based on the substrate of p-type. It serves as a base to form n-type regions for source and drain.

2. Source and Drain: They are n-type regions in the p-type substrate. Source is where the carriers-electrons-enter and drain is where they leave.

3. Gate: The top layer contains a conductive gate mostly from polysilicon. Beneath this gate, lies an extremely thin layer of SiO_2 insulating material. This means that the gate may be considered as a bridge controlling the flow of current between the source and the drain.

4. Insulator: The gate is separated from the silicon, thus realizing a MOS-type of structure.

Working:

- Threshold Voltage (V_{TH}) : Minimum V_{GS} required to invert the region under the gate and thus create a conducting n-channel. For $V_{GS} < V_{TH}$, NMOSFET is in the cutoff region with zero current between drain and source.
- Linear (Triode) Region: For $V_{GS} > V_{TH}$ and V_{DS} being small, an n-channel is established between the source and drain. NMOSFET behaves like a resistor, and the current I_D varies linearly with V_{DS}.
- Saturation (Active) Region: As V_{DS} increases, the channel near the drain pinches off when V_{DS} approaches V_{GS} - V_{TH}. In this region, the NMOSFET is in the form of a constant current source where I_D is a function of V_{GS}, thus good for use in amplification.

Partially Depleted SOI (PD-SOI) MOSFET

A PD-SOI MOSFET is a type of standard MOSFET, but here an insulating layer, typically silicon dioxide, is placed between the semiconductor body and the substrate. It is mostly applied in high-speed, low-power applications due to its better isolation and decreased parasitic capacitances.

Structure:

1. BOX Layer: The SiO_2 is an insulating layer provided between the silicon layer, which is thin, on which the MOSFET channel is formed, and the underlying silicon substrate.

2. Thin Silicon Layer: It has source, drain, and channel in this layer but is so thin that only a part of it gets depleted during operation; hence, it is referred to as partially depleted.

3. Gate, Source, and Drain: The PD-SOI MOSFETs have a gate, source, and drain regions similar to the conventional MOSFET, but they are formed on a thin silicon layer above the BOX.

Operation:

- Depletion: When a voltage is applied to the gate, the silicon layer beneath it will become partially depleted. Thus, only part of this layer is depleted, and still, a part of the silicon is unchanged; it inherently influences the capacitance and, in turn, influences the performance of the device.
- Self-Heating: The BOX layer does not permit the flow of heat. Thus, PD-SOI MOSFETs are faced by self-heating, and due to that, the threshold voltage as well as the total performance may degrade in case of long-term operations.

Advantages:

1. Reduced Parasitics: It separates the silicon layer containing active semiconductor material from the substrate, reducing parasitic capacitances, and enhancing switching speed.

2. Improved Short-Channel Effects: Isolation reduces short-channel effects, thereby making PD-SOI MOSFETs useful for advanced digital and analog applications.

3. High-Speed Performance: Reduced capacitance and isolation provide faster switching speed with low power consumption in high-frequency applications.

Disadvantages:

1. Self-Heating Effects: BOX layer is such that heat dissipation is not possible, which causes localized heating.

2. Complex Fabrication: The manufacturing process of PD-SOI MOSFET is more complex and expensive as compared to the conventional bulk MOSFET.

Applications:

The PD-SOI MOSFETs are primarily used in high speed and low power applications wherein the leakage current is lesser and temperature performance improves. A few of the common applications include mobile, RF circuits, and microprocessors.

Short-Channel Effects (SCEs)

- Threshold Voltage Roll-Off: When the channel length L becomes small enough, source and drain overlap regions compete each other and control by the gate over the channel will be reduced and threshold voltage will decrease.
- Drain-Induced Barrier Lowering (DIBL): When drain voltage is applied, a high potential barrier at the source-channel junction is reduced by increasing leakage current. As a result, threshold voltage will be reduced.
- Subthreshold Slope This is another parameter that captures the efficiency of shutting down the MOSFET. Greater slope generally means better for low-power applications, as it implies that the device can be turned off by a rarely different change in gate voltage.

Procedures:

NMOSFET Simulation

1. Launch Silvaco TCAD and Create a New Project by selecting File > New Project.
2. Define Device Parameters such as the substrate, gate material, and doping concentrations. Specify the gate lengths you want to simulate (180nm, 90nm, 45nm, 32nm, and 22nm).
3. Generate a fine mesh for the device to ensure accurate simulation results and adjust the mesh density in critical regions like the channel, source, and drain.
4. Define the boundary conditions for the device terminals (source, drain, gate, and substrate). Apply voltages to the gate, source, and drain terminals as required.
5. Select appropriate physics models for the simulation, such as drift-diffusion, mobility models, and impact ionization. Enable short-channel effects models to study threshold voltage roll-off and DIBL.
6. Set up simulations at different temperatures (300K, 325K, 350K, 375K, 400K) to study the impact of temperature variations.
7. Execute the simulations for each gate length and temperature setting. Use the simulator within Silvaco TCAD to run the simulations.
8. Extract output characteristics and transfer characteristics. Analyze parameters such as threshold voltage, maximum drain current, subthreshold slope, and DIBL.

PD-SOI MOSFET Simulation

1. Open Silvaco TCAD software. Create a new project by selecting File > New Project.
2. Set up the PD-SOI MOSFET structure by defining the SOI substrate, gate material, and doping concentrations. Specify the gate lengths you want to simulate (180nm, 90nm, 45nm, 32nm, and 22nm).
3. Generate a fine mesh for the device to ensure accurate simulation results. Adjust the mesh density in critical regions like the channel, source, drain, and the SOI layer.
4. Define the boundary conditions for the device terminals (source, drain, gate, and substrate). Apply voltages to the gate, source, and drain terminals as required.
5. Select appropriate physics models for the simulation, such as drift-diffusion, mobility models, and impact ionization. Enable SOI-specific models to study the floating body effect and reduced parasitic capacitance.
6. Set up simulations at different temperatures (300K, 325K, 350K, 375K, 400K) to study the impact of temperature variations.
7. Execute the simulations for each gate length and temperature setting. Use the simulator within Silvaco TCAD to run the simulations.
8. Extract output characteristics and transfer characteristics. Analyze parameters such as threshold voltage, maximum drain current, subthreshold slope, and DIBL.

Simulation Code:

```
go victorydevice

mesh width=1.6

# X mesh #
x.mesh location=-0.180 s=0.01
x.mesh location=-0.090 s=0.01
x.mesh location=0.000 s=0.01
x.mesh location=0.090 s=0.01
x.mesh location=0.180 s=0.01

#Y mesh #
y.mesh location=0.000 s=0.0002
y.mesh location=0.002 s=0.002
y.mesh location=0.110 s=0.005
```

```
y.mesh location=0.260 s=0.02
y.mesh location=0.360 s=0.02

# Material #
region num=1 y.min=0 y.max=0.360 mat=air
region num=2 x.min=-0.180 x.max=0.180 y.min=0.090 y.max=0.260 mat=oxide
region num=3 y.min=0.260 y.max=0.360 mat=silicon
region num=4 y.min=0.002 y.max=0.110 mat=silicon

#Doping #
doping uniform p.type conc=1e16 x.min=-0.090 x.max=0.090 y.min=0.002 y.max=0.110
doping uniform n.type conc=1e18  x.min=-0.180 x.max=-0.090 y.min=0.002 y.max=0.110
doping uniform n.type conc=1e18 x.min=0.090 x.max=0.180 y.min=0.002 y.max=0.110
doping uniform p.type conc=1e16 x.min=-0.180 x.max=0.180 y.min=0.260 y.max=0.360

#Electrode #
electrode name=source x.min=-0.180 x.max=-0.090 y.min=0.002 y.max=0.002
electrode name=drain x.min=0.090 x.max=0.180 y.min=0.002 y.max=0.002
electrode name=gate x.min=-0.090 x.max=0.090 y.min=0.000 y.max=0.000

# Contact #
contact name=source neutral
contact name=drain neutral
contact name=gate  workfunction=4.2

# Models #
models print srh temp=300

output con.band val.band band.par

solve init
save outf=test.str

# IV
#solve vdrain=0 vstep=0.1   vfinal=1.5   name=drain
#log outf=IDVGpdsoi100mV.log

#solve vgate=0 vstep=0.1 vfinal=2.5 name=gate
#OUTPUT CHARACTERISTICS
log outf=PDMOS_GATE_100nm_300.log

solve vgate=0.5
contact name=gate voltage
solve vdrain=0 vstep=0.05 vfinal=2 name=drain


solve vgate=1.0

solve vdrain=0 vstep=0.05 vfinal=2 name=drain

solve vgate=1.5

solve vdrain=0 vstep=0.05 vfinal=2 name=drain

#transfer characteristics
```

```
log outf=PDMOS_Transfer_300_GATE_100nm.log

solve vdrain=0.5
contact name=drain voltage
solve vgate=0 vstep=0.05 vfinal=2 name=gate

solve vdrain=1.0

solve vgate=0 vstep=0.05 vfinal=2 name=gate


solve vdrain=1.5

solve vgate=0 vstep=0.05 vfinal=2 name=gate

#save structure
#save outf=PDMOSFET_Transfer_300_100nm.str

quit
```

Results:

Output Characteristics (I_D vs V_D)

1. **NMOSFET**:

    - **180nm Gate Length**: The drain current (IDI_D) increases linearly with drain voltage (VDV_D) at low VDV_D and saturates at higher VDV_D. The maximum drain current is relatively high due to the longer channel length.
    - **90nm Gate Length**: Similar behavior as 180nm but with higher maximum drain current and more pronounced short-channel effects.
    - **45nm Gate Length**: The drain current saturates quicker, indicating increased short-channel effects like DIBL and threshold voltage roll-off.
    - **32nm Gate Length**: Significant short-channel effects are observed, with the maximum drain current further increased.
    - **22nm Gate Length**: The shortest gate length exhibits the highest drain current but also the most severe short-channel effects, including substantial threshold voltage roll-off and DIBL.

2. **PD-SOI MOSFET**:

    - **180nm Gate Length**: The output characteristics are similar to NMOSFET with high maximum drain current and linear-saturation behavior.
    - **90nm Gate Length**: Exhibits better control over short-channel effects compared to NMOSFET, with lower DIBL and threshold voltage roll-off.
    - **45nm Gate Length**: The drain current remains stable, and short-channel effects are less severe than in NMOSFET.
    - **32nm Gate Length**: Exhibits excellent control over short-channel effects, maintaining high drain current with minimal DIBL.
    - **22nm Gate Length**: The PD-SOI MOSFET continues to perform well with reduced SCEs, showing only a slight increase in DIBL and threshold voltage roll-off.

Transfer Characteristics (I_D vs V_G)

1. **NMOSFET**:

- **180nm Gate Length**: The transfer curve shows a steep subthreshold slope, indicating good gate control. The threshold voltage is relatively high and stable.
- **90nm Gate Length**: The subthreshold slope becomes slightly less steep, indicating the onset of short-channel effects. The threshold voltage begins to roll off.
- **45nm Gate Length**: The subthreshold slope degrades further, and the threshold voltage roll-off is more pronounced. Higher DIBL is observed.
- **32nm Gate Length**: The threshold voltage continues to decrease, and subthreshold slope degradation is more significant.
- **22nm Gate Length**: The most severe short-channel effects are observed, with a substantial decrease in threshold voltage and a less steep subthreshold slope.

2. **PD-SOI MOSFET**:

- **180nm Gate Length**: Similar steep subthreshold slope as NMOSFET, indicating excellent gate control. The threshold voltage is stable.
- **90nm Gate Length**: Maintains a steep subthreshold slope and stable threshold voltage, with minimal short-channel effects.
- **45nm Gate Length**: Exhibits good control over SCEs, with a slight decrease in threshold voltage but maintaining a steep subthreshold slope.
- **32nm Gate Length**: Slight increase in DIBL and threshold voltage roll-off, but still better controlled than NMOSFET.
- **22nm Gate Length**: The PD-SOI MOSFET performs well with reduced short-channel effects, maintaining a relatively stable threshold voltage and good subthreshold slope.

Temperature Impact

- **NMOSFET**:
  1. **300K to 400K**: As the temperature increases, the leakage current increases, and the threshold voltage decreases. These effects are more pronounced at shorter gate lengths.
  2. Higher temperatures lead to increased thermal generation of carriers, resulting in higher off-state leakage currents.
- **PD-SOI MOSFET**:
  1. **300K to 400K**: The PD-SOI MOSFET shows better stability with temperature variations. Although the threshold voltage decreases and leakage current increases, these changes are less severe compared to NMOSFET.
  2. The insulating layer in PD-SOI helps to mitigate the impact of temperature variations.

Observations:

- **Short-Channel Effects (SCEs)**:

  1. NMOSFETs exhibit significant short-channel effects as the gate length decreases. This includes a pronounced threshold voltage roll-off and increased DIBL.
  2. PD-SOI MOSFETs demonstrate better control over short-channel effects, with less severe threshold voltage roll-off and lower DIBL across all gate lengths.

- **Temperature Variations**:
  1. Both NMOSFET and PD-SOI MOSFET show increased leakage current and reduced threshold voltage with rising temperatures. However, PD-SOI MOSFETs are less affected by temperature variations due to the insulating layer.
- **Device Performance**:
  1. NMOSFETs perform well at longer gate lengths but suffer from severe SCEs at shorter gate lengths.

2. PD-SOI MOSFETs maintain good performance even at shorter gate lengths, making them more suitable for advanced technology nodes.

- **Subthreshold Slope**:
  1. NMOSFETs show degradation in the subthreshold slope with reduced gate lengths, indicating less effective gate control.
  2. PD-SOI MOSFETs maintain a steeper subthreshold slope, indicating better gate control even at shorter gate lengths.

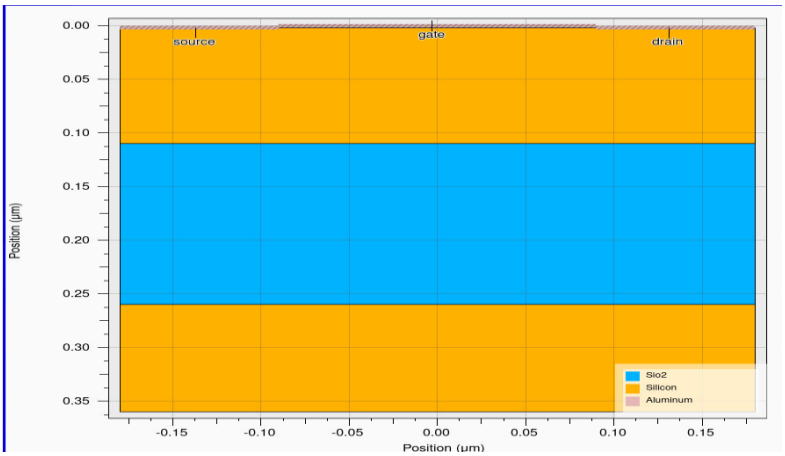


Fig.1. Structure

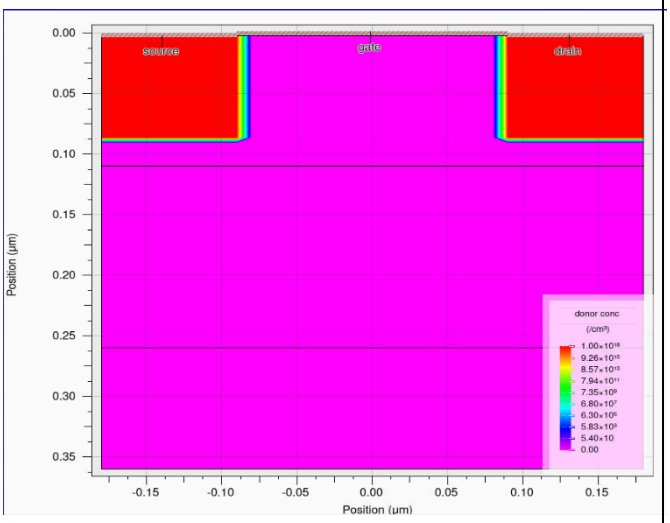


Fig.2. Donor Conc.

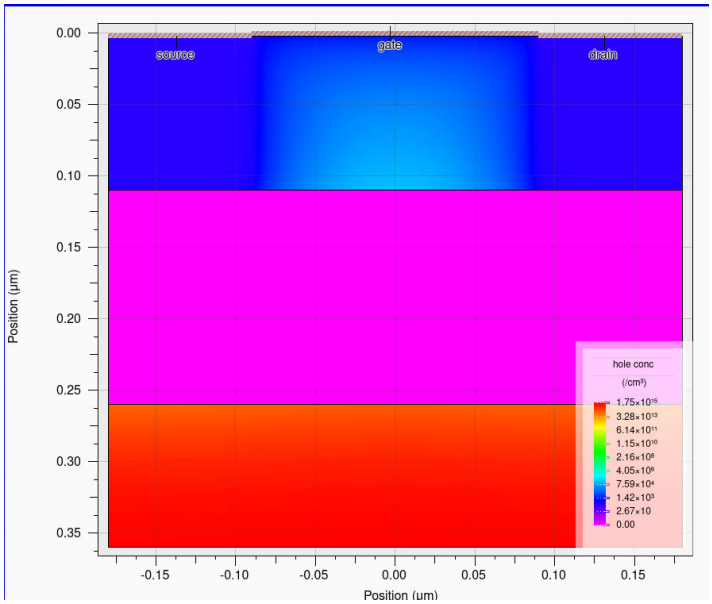


Fig.3. Hole Conc.

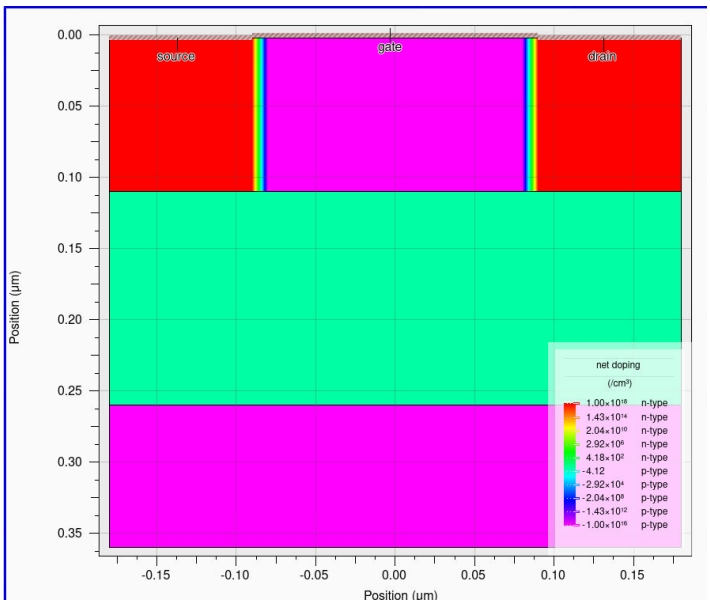
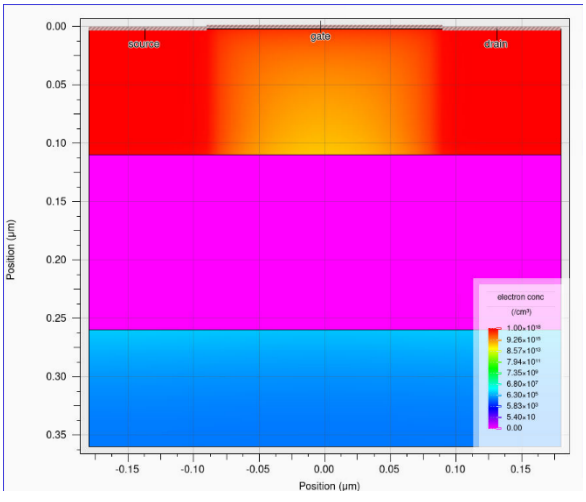
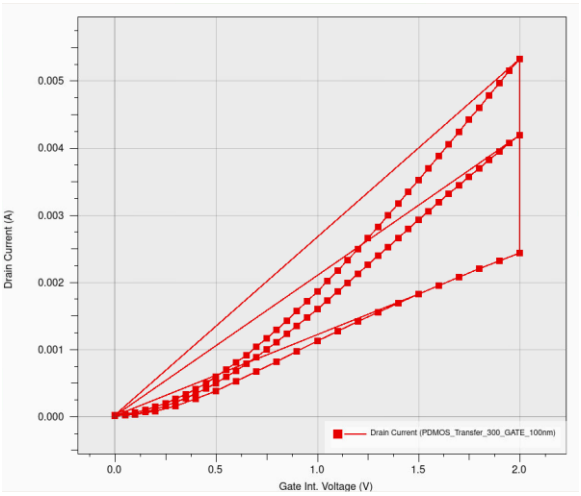


Fig.4. Net Doping





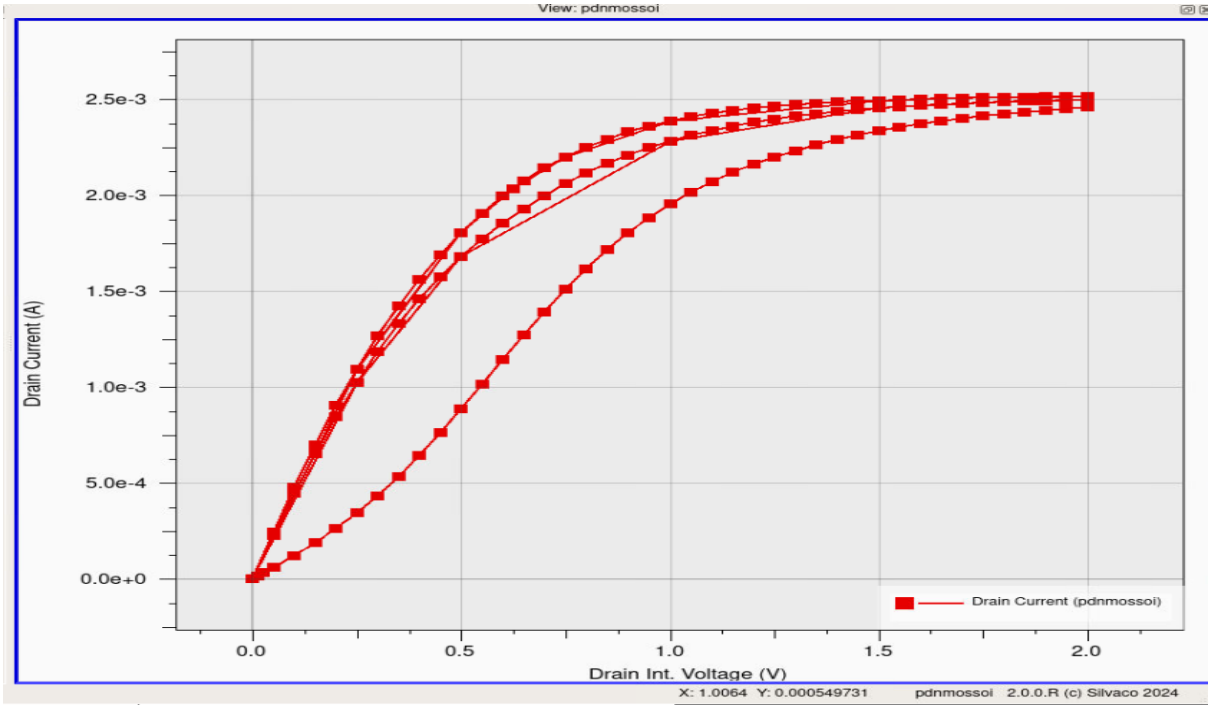


Fig.7. Drain Characteristics

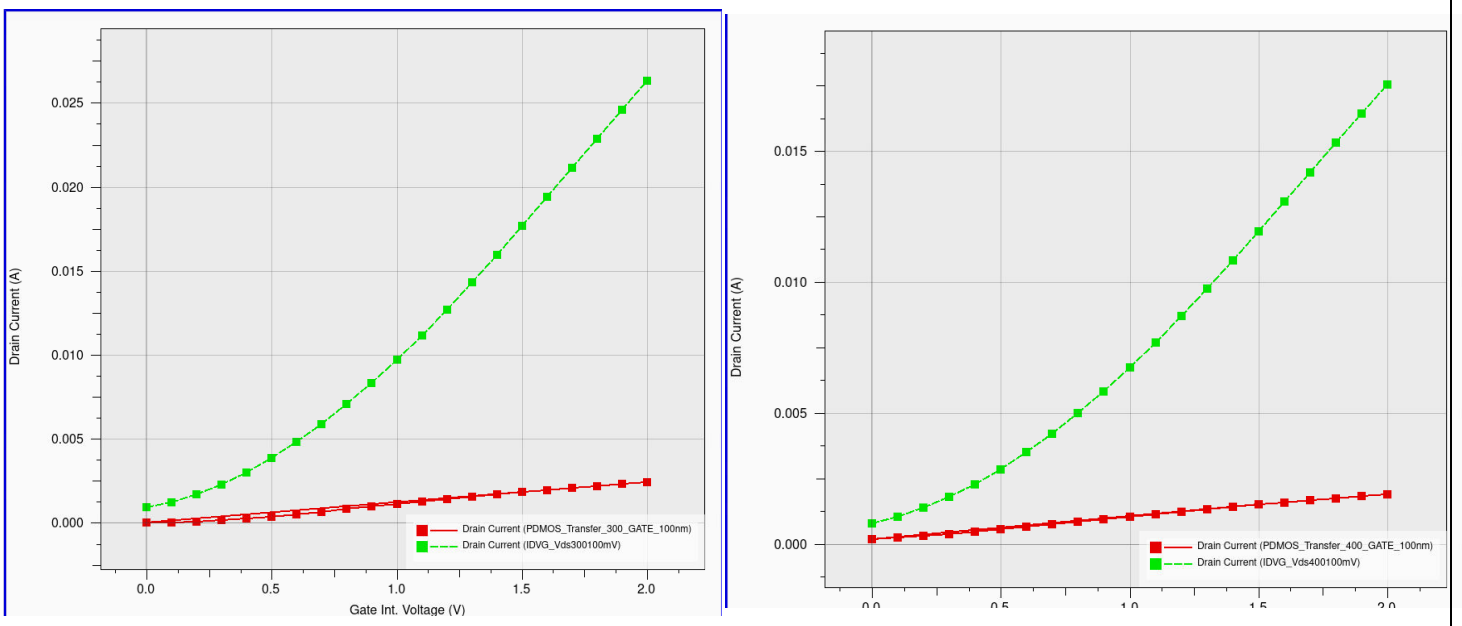


Fig.8&9. Transfer Characteristics of PD-MOSFET and NMOSFET at 300K and 400K respectively.

Sources of Errors:

- Modeling Errors: The inaccuracies in device models and the respective parameter values used in the simulations.
- Numerical Errors: Numerical errors stemming from the approximate degree of precision in numbers used and the algorithms used in the simulation software.
- Assumptions and Simplifications: In the simulation setup, assumptions are made on idealized material properties, assuming some physical effects to be negligible, which could result in the mismatch of the simulated results with the real situation.

Conclusion:

The experiment was successfully carried out for demonstrating how the two transistors, NMOSFET, and PD-SOI MOSFET, perform at different gate lengths and temperatures. NMOSFETs have stronger SCEs, such as Vth roll-off and DIBL, which reduce the performance at shorter gate lengths. The SCEs for PD-SOI MOSFETs are more controllable, and the temperature-sensitive performance degradation is reduced. These advantages will help PD-SOI MOSFETs in advanced technology nodes that have stringent scaling requirements. This comparison shows the significance of proper choice of MOSFET architecture in appropriate applications where issues like gate length, temperature sensitivity, and overall device performance become relevant. NMOSFETs are used because they form a simple and effective switching mechanism, whereas PD-SOI MOSFETs are preferred for particular applications on account of reduced parasitics and increased speed at the expense of heat dissipation and cost.

References:

1. ATLAS User Manual (Silvaco TCAD Manual)
2. Semiconductor Physics by SM. Sze
3. Silvaco User Guide Manual.

Experiment - 08

Comparison of N-Channel NMOSFET, PD-SOI MOSFET, and FD-SOI MOSFET

Aim: To simulate and compare the output and transfer characteristics of an n-channel NMOSFET, a partially-depleted (PD) SOI MOSFET, and a fully-depleted (FD) SOI MOSFET across gate lengths of 180nm, 90nm, 45nm, 32nm, and 22nm, studying short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope. Investigate the impact of temperature variations (300K, 325K, 350K, 375K, 400K) on maximum drain current, threshold voltage, early effect, and channel length modulation, and analyze the performance implications of scaling.

Theory:

The **Fully Depleted MOSFET (FDMOSFET)** is a type of MOSFET that is built on a Silicon-On-Insulator (SOI) substrate and is designed to operate with a fully depleted channel. This design offers several advantages over traditional bulk MOSFETs, especially in terms of reducing short-channel effects and improving device performance at nanoscale dimensions.

Structure:

- **SOI Substrate**: The FDMOSFET is fabricated on an SOI substrate, which consists of a thin silicon layer on top of an insulating layer (usually silicon dioxide) and a bulk silicon substrate beneath.
- **Gate Stack**: The gate stack includes a gate oxide (typically SiO2) and a gate electrode (usually polysilicon or metal).
- **Source and Drain**: The source and drain regions are heavily doped n-type regions on either side of the gate.

Operation:

- **Fully Depleted Channel**: In FDMOSFETs, the silicon layer is thin enough that the channel region is fully depleted of carriers when the device is in the off state. This means that the entire channel region is depleted of free carriers, leading to better control of the channel by the gate.
- **Reduced Parasitic Capacitance**: The insulating layer in the SOI substrate reduces parasitic capacitance between the source/drain and the substrate, improving switching speed and reducing power consumption.

Advantages

1. **Reduced Short-Channel Effects (SCEs)**: The fully depleted channel provides better electrostatic control over the channel, reducing SCEs such as threshold voltage roll-off and drain-induced barrier lowering (DIBL).
2. **Lower Power Consumption**: Reduced parasitic capacitance leads to lower dynamic power consumption, making FDMOSFETs suitable for low-power applications.
3. **Improved Performance at Nanoscale**: FDMOSFETs perform better at shorter gate lengths due to reduced SCEs and improved gate control.
4. **Thermal Stability**: The insulating layer in the SOI substrate helps to mitigate the impact of temperature variations on device performance.

Short-Channel Effects (SCEs)

Threshold Voltage Roll-Off: As the channel length decreases, the depletion regions from the source and drain begin to overlap, reducing the control of the gate over the channel and causing a decrease in threshold voltage.

Drain-Induced Barrier Lowering (DIBL): A high drain voltage can lower the potential barrier at the source-channel junction, leading to an increase in leakage current and a reduction in threshold voltage.

Subthreshold Slope: The subthreshold slope measures how effectively the gate voltage can control the channel current. A steeper slope is desirable for low-power applications as it means the device can turn off with a smaller change in gate voltage.

Applications

FDMOSFETs are used in various applications, including:

- **Low-Power Electronics**: Due to their low power consumption and reduced leakage currents, FDMOSFETs are ideal for battery-powered devices and energy-efficient circuits.
- **High-Frequency Circuits**: The improved switching speed and reduced parasitic capacitance make FDMOSFETs suitable for high-frequency applications.
- **Analog and Mixed-Signal Circuits**: The better control over the channel and reduced SCEs make FDMOSFETs suitable for analog and mixed-signal applications.

Procedures:

FD-SOI MOSFET Simulation

1. Open Silvaco TCAD software. Create a new project by selecting File > New Project.
2. Set up the PD-SOI MOSFET structure by defining the SOI substrate, gate material, and doping concentrations. Specify the gate lengths you want to simulate (180nm, 90nm, 45nm, 32nm, and 22nm).
3. Generate a fine mesh for the device to ensure accurate simulation results. Adjust the mesh density in critical regions like the channel, source, drain, and the SOI layer.
4. Define the boundary conditions for the device terminals (source, drain, gate, and substrate). Apply voltages to the gate, source, and drain terminals as required.
5. Select appropriate physics models for the simulation, such as drift-diffusion, mobility models, and impact ionization. Enable SOI-specific models to study the floating body effect and reduced parasitic capacitance.
6. Set up simulations at different temperatures (300K, 325K, 350K, 375K, 400K) to study the impact of temperature variations.
7. Execute the simulations for each gate length and temperature setting. Use the simulator within Silvaco TCAD to run the simulations.
8. Extract output characteristics and transfer characteristics. Analyze parameters such as threshold voltage, maximum drain current, subthreshold slope, and DIBL.

Simulation Code: