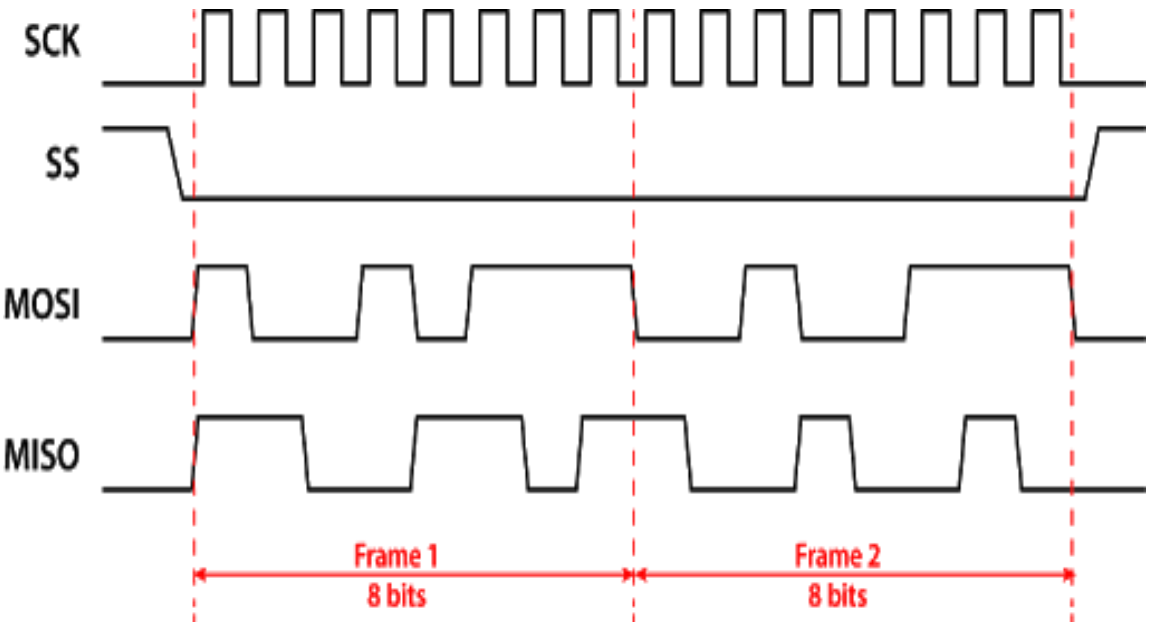
SPI

- SPI stands for Serial Peripheral Interface.
- It is hardware control protocol based on wired system.
- It is serial protocol and synchronous due to presence of clock line.
- Basically, used for low speed peripherals (peripherals that operates from low frequency clock).
- SPI has 4 pins –
    - SCLK (SCK) -> Serial Clock
    - SDI (MISO) -> Master Input Slave Output
    - SDO (MOSI) -> Master Output Slave Input
    - CE (SS') (NSS) -> Slave Select
- Lesser packet size and power consumption.
- SPI bus speeds are 10 mbps.
- * 3 wire interfaces: single data pin.
- SPI is full duplex and unidirectional.
- SPI has single master and have one or multi slave-devices. Which are supported through selection with individual slave select (SS).



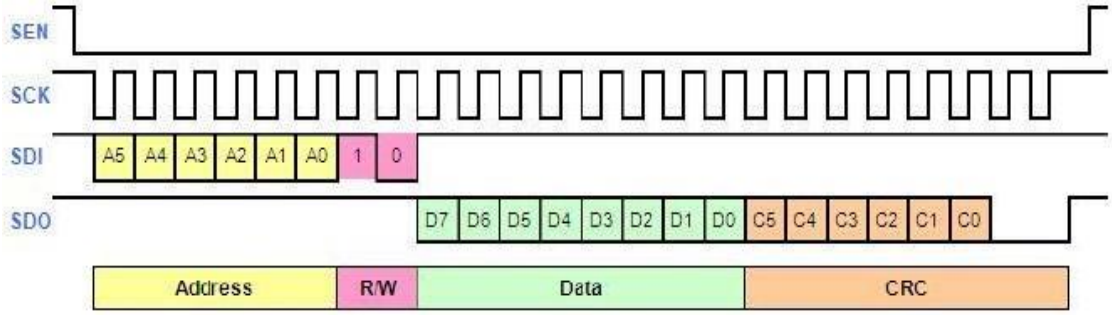
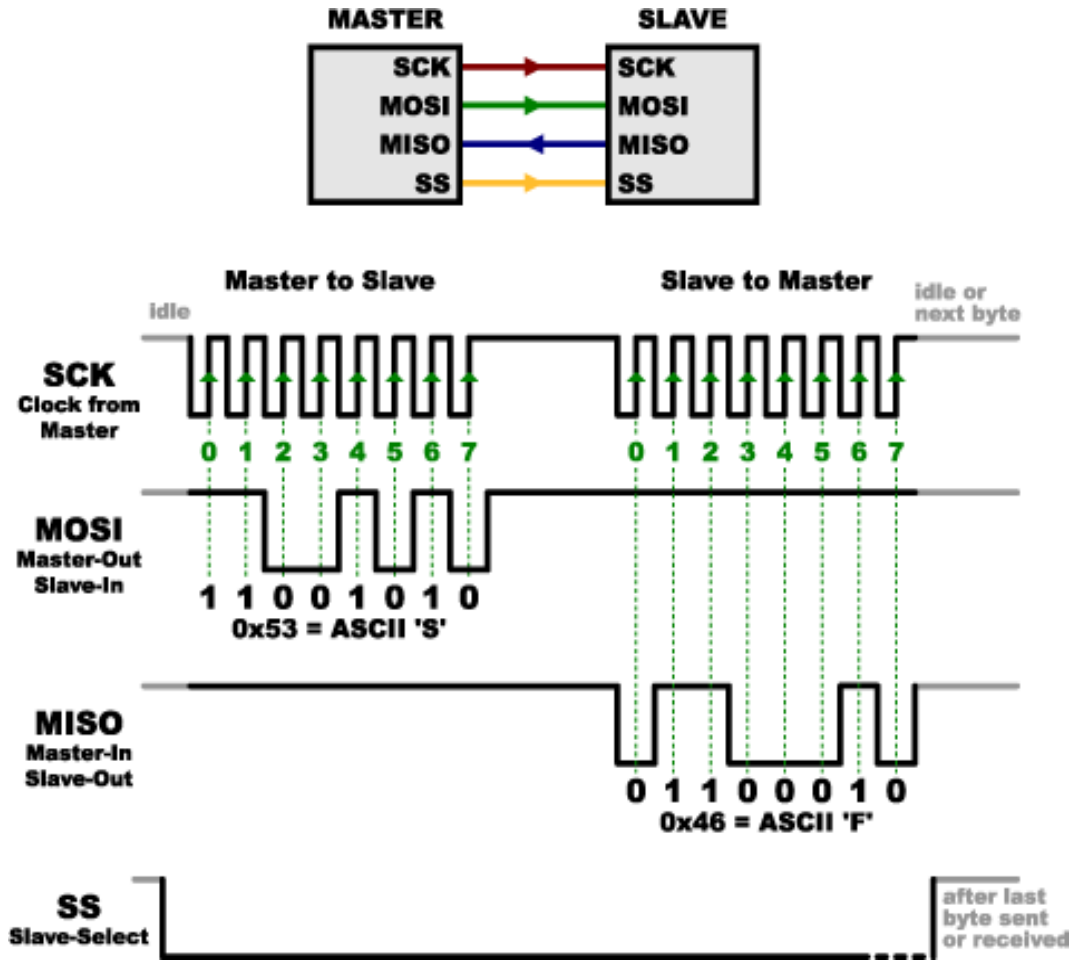


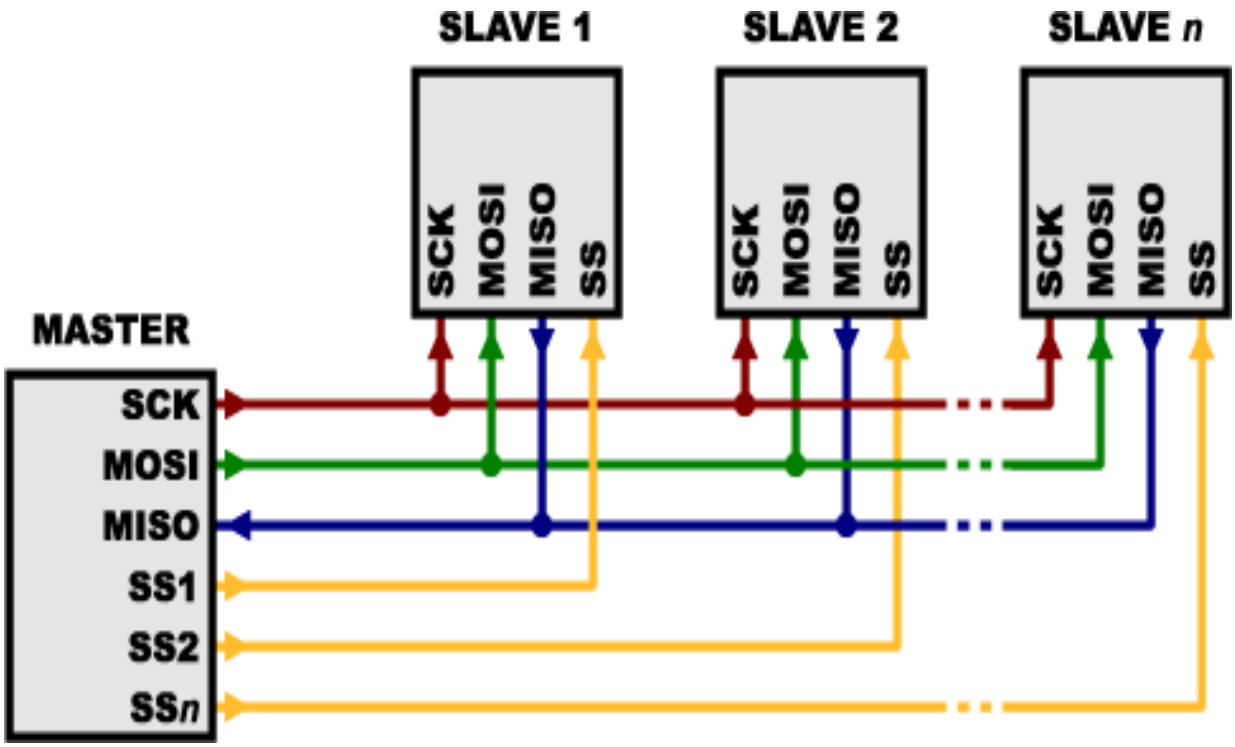
Figure 30. Read Operation Format

- **Slave Select –**
  - Single or several slave can be used at the same time, SS' is used to select which slave we want to communicate to.
  - If SS' is held in low state, the SPI is activated.
  - **Single Slave:**

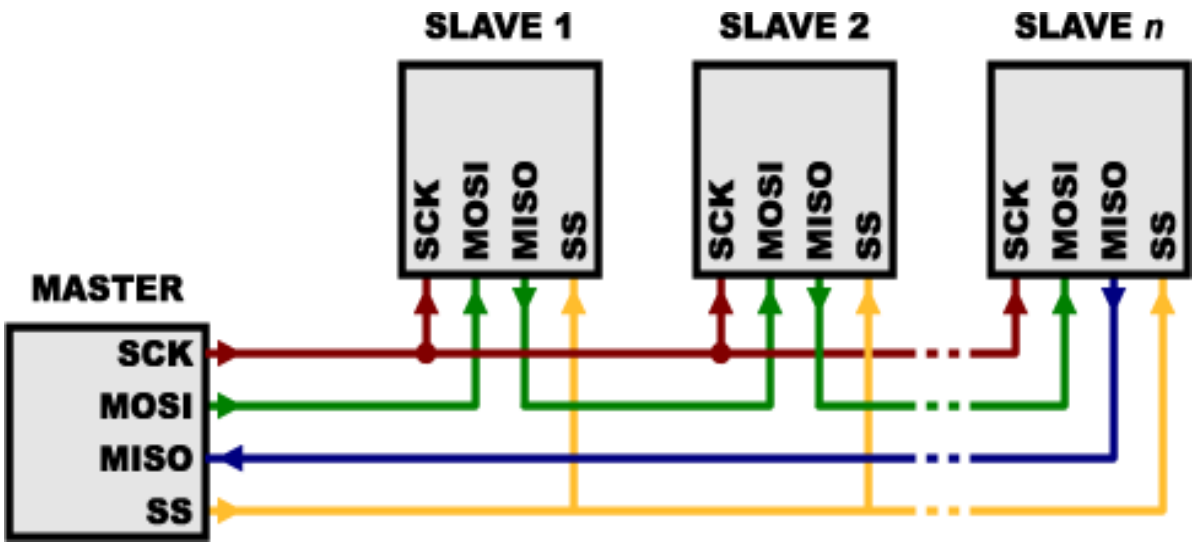


- **Multi Slave:**

  In general, each slave will need a separate SS line. To talk to a particular slave, we will make that slave's SS line low and keep the rest of them high (you don't want two slaves activated at the same time, or they may both try to talk on the same MISO line resulting in garbled data). Lots of slaves will require lots of SS lines.



- **Daisy Chain –**
  - A single SS' line can also go to all the slaves i.e. daisy-chained together.
  - With the MISO (output) of one going to the MOSI (input) of the next. In this case, once all the data is sent, the SS line is raised, which causes all the chips to be activated simultaneously.
  - For this layout, data overflows from one slave to the next, so to send data to any one slave, you'll need to transmit enough data to reach all of them. Also, keep in mind that the first piece of data you transmit will end up in the last slave.



Master Side Algo

- Set MOSI as output.
- Set SCK as output.
- Set SS' as output.
- Set SPI as a Master.
- Initiate data transfer.
- MSB first.
- Wait for transmission to complete.
- The received data is placed in register.

Slave Side Algo

- Set MISO as output.
- Set SPI as a Slave.
- MSB first.
- Send data on master request.
- Wait for reception to complete.
- The receiver data is placed in register.