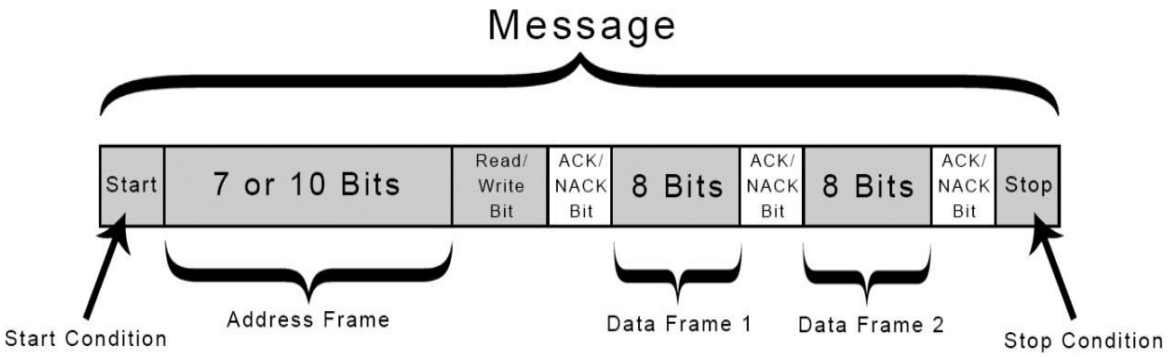
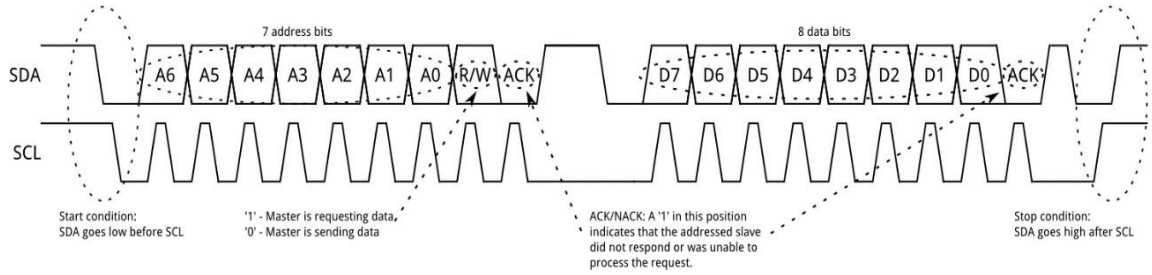
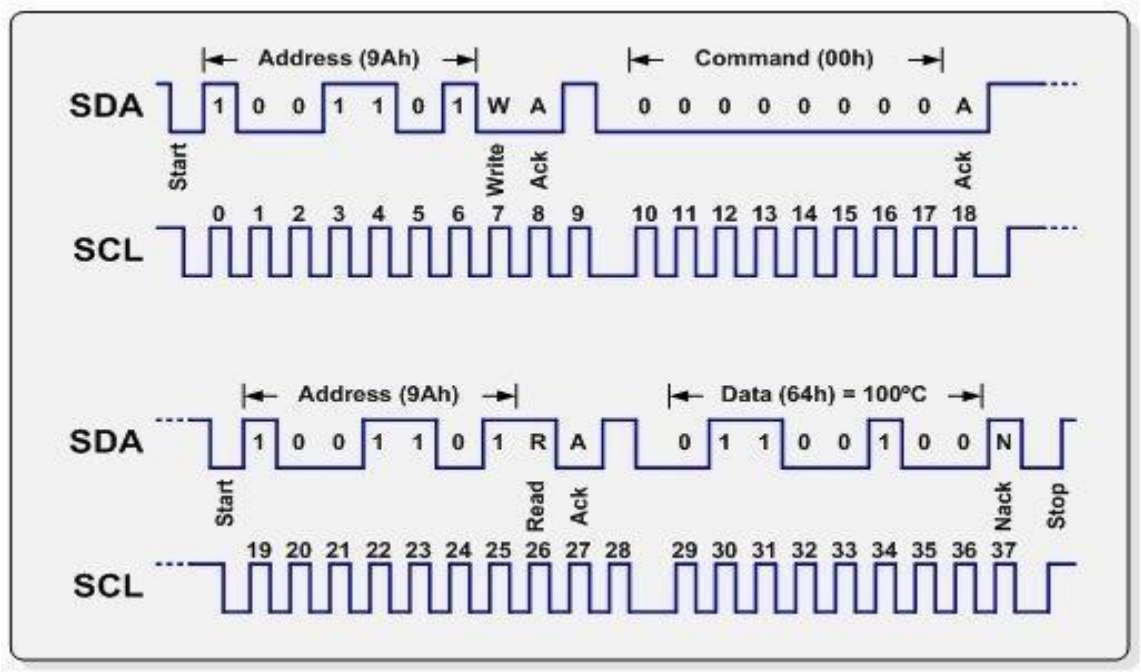
I2C

- I2C stands for inter integrated circuit.
- Signal Levels –
  - Float High (logic 1)
  - Drive Low (logic 0)
- It is hardware control protocol based on wired system.
- It is serial protocol and synchronous due to presence of clock line.
- Basically, used for low speed peripherals (peripherals that operates from low frequency clock).
- Used for reliable communication over short distance (approx. 10 meters).
- Use only two pins – SCL (Serial Clock Line) and SDA (Serial Data Line). Which reduce power consumption and packet size.
- I2C bus speeds –
  - Low speed mode – 10 kbps
  - Standard mode – 100 kbps
  - Fast mode – 400 kbps
  - Fast mode plus – 1 mbps
  - High speed mode – 3.4 mbps
  - Ultra fast mode – 5 mbps
- I2C is half duplex and bidirectional. Both master and slave can receive or transmit data.
- 4 modes –
  - Master Transmitter
  - Master Receiver
  - Slave Transmitter
  - Slave Receiver
- It supports multi-master concept. It can have unlimited masters and only 1008 slaves.
- Each node can act as Master or Slave.
- Master is a device that generates the clock, can initiate and terminate operation.
- Slave is the one which receives the clock and is addressed by the master.

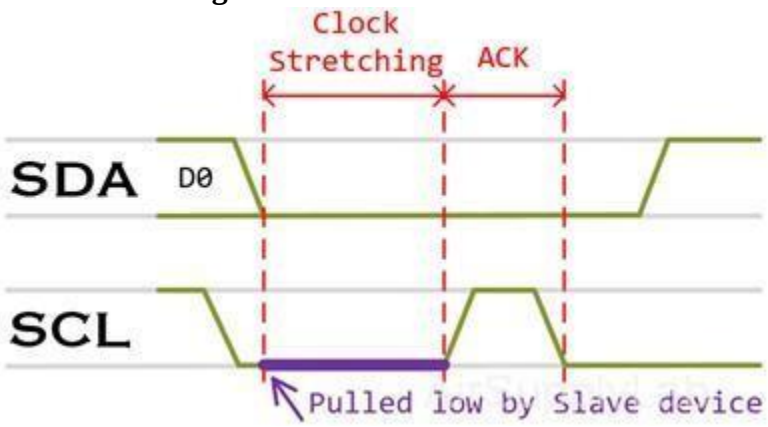




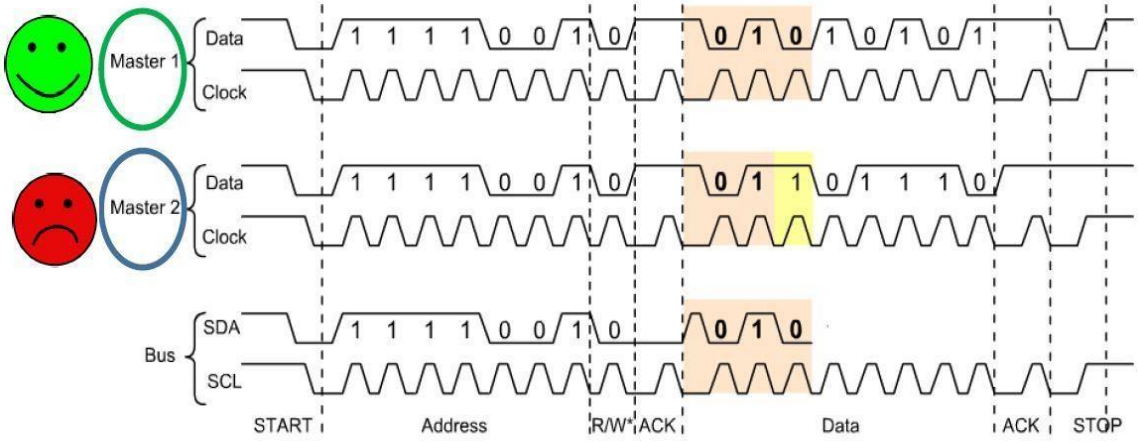


- I2C Frame Details –
  - S → Start
  - Address → Address
  - A → Acknowledgment
  - Data → Data
  - P → Stop
  - Rs → Repeat - Start
- Each Packet is of 9 bits: address or data.
- First 8 bits are used by the transmitter and the 9th bit is for ACK/NACK used by the receiver.
- START & STOP are generated by the master.
- START is generated by a high to low change in the SDA line when SCL is high.
- STOP is generated by low to high change in the SDA line when SCL is high.
- BUS is busy between a pair of START and STOP and no other node tries to take control of the bus.
- R/W: Read (1) and Write (0).

- ACK is when the recipient drives SDA low.
- **Clock Stretching –**



  - Clock stretching allows an I2C slave device to force the master device into a wait state.
  - A slave device may perform clock stretching when it needs more time to manage data, such as store received data, or prepare to transmit another byte of data.
  - If slave is not ready to respond to data, it will draw the SCL to zero.
  - Only slave device can initiate the clock stretch.
  - Wired AND (if one device pulls a line low it stays low) logic are used.
- **Arbitration –**



  - If two nodes start acting as Master at the same time, then arbitration occurred.
  - Each transmitter (master) has to check the level of the bus and compare it to the level it expects; if it does not match, the transmitter has lost the arbitration.
  - Master A wants to put 00100000 on the bus.
  - Master B wants to put 00011110 on the bus.
  - Master A lost in third cycle.
- **Repeated START –**
  - If a master which has control of the bus wants to initiate a new transfer and does not want to release the bus, then it issues a REAPEATED START condition.