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RESEARCH ARTICLE

# Hardware implementation of optical switching node for data center networks

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**Abstract**

In high performance data center networks, switching the data from source node to destination node needs a proper signal processing to decode the address bits and switch the data and to avoid contention. In this article, we propose the hardware design for switching the data from one node to other bi-directionally. The design is verified in an experimental test bed.

**KEYWORDS**

data center networks, hardware implementation, optical switching

## 1 | INTRODUCTION

Large bandwidth availability in optical networks, make it a promising technology for current internet and communication networks which deals with enormous data. In an optical network, the data transfer from one end to another end is through multiple switching nodes and paths. To reach the desired destination node from a source node, the path has to be selected via the intermediate nodes. The routing through the selected paths is based on the address bits. Each packet has data bits and address bits. In order to switch the optical data from one node to another node, the packet has to be decoded and processed at the bit level. The lack of bit level processing and buffering are the major limitations in optical domain.[1] Therefore, the optical data needs to be converted to electrical data and the bit level processing can be carried out in the electronics domain to choose the desired path. This may increase the processing time in each switching node. Since the decision is made at every node level, the contention can be reduced. Therefore, the optical networks without electronic signal processing may reduce the processing time but bit level signal processing may not be achieved.

For example, in a multistage interconnection network, if the data has to be transmitted from two different input ports to 2 different output ports as shown in Figure 1, the electronic signal processing is required to switch the data to the desired destination. If the entire data is converted into electrical domain, then the delay and error during the conversion will be predominant.[2] Also one cannot leverage the complete optical data rates. Therefore, the entire data can be split into 2 fields namely header and payload. To minimize the burden on electronic counter parts and utilize the optical data speed, only the header part can be converted into electrical domain and based on the decision made in the electrical logic circuit the data can be transmitted from one switching node to another.[3]

The switches are interconnected to build a passive optical network. In the optical environment along with other bidirectional devices, such as Semiconductor Optical Amplifier (SOA), Erbium Doped Fiber Amplifier (EDFA), coupler, cross connects; optical bi-directional switch can also be connected in a network so as to have high throughput and capacity.[4] Owing to the optical bandwidth capacity and bi-directional capability, the number of port counts can be increased in both the directions. The wavelength routing is used in all optical passive networks to direct the packet to its desired destination.[5] However, the data center networks like, shuffle net, Benes, Data Vortex, Torus are highly scalable and require electronic signal processing at every node to dynamically direct the packet to its desired destination.[6]

In this article, we demonstrate, $2 \times 2$ bi-directional optical packet switching node with electronic signal processing module (ESPM) to direct the packet to the desired destination link. Also, we propose the design of ESPM with minimum electronics to give the control input to the desired destination link. Therefore, the speed of optical data is not compromised. In this work, the entire optical to electrical conversion is saved by extracting the address bits from the data bits and switching the signal based on the address bits.

  

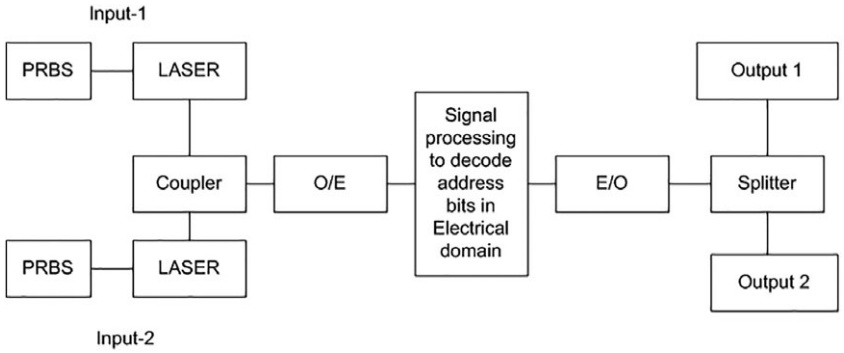


**FIGURE 1** Basic optical switching architecture

The rest of the article is organized as follows: Section 2 gives the proposed hardware model of optical bidirectional switching node with ESPM to extract the address bits. Section 3 presents the testbed of the proposed model and Section 4 gives the observed results. Section 5 gives the concluding remarks.

## 2 | PROPOSED HARDWARE MODEL OF OPTICAL BIDIRECTIONAL SWITCHING NODE WITH ESPM

In this paper, we demonstrate the 2 × 2 bi-directional optical packet switching node with ESPM (Figure 2). In the highly scalable multistage interconnection network like Benes, data vortex[7–9] there is "N" number of inputs and outputs where multiple paths are available to reach the desired destination. In such networks, decoding the address bits at every node is crucial. Since there are multiple paths, it is desirable to choose the appropriate path so that low latency and high throughput can be achieved. Also, if the address bits are decoded and tested with node address then the data packets can be transmitted to the desired destination without any delay and congestion. Therefore, it is important to extract the address bits. Here, we demonstrate a suitable optical switch along with the ESPM. Unlike the model shown in Figure 1, here we decode only the address bits at every node. In multistage network like Benes and data vortex, the number of address bits required to trace its desired destination depends on the number of stages. The number of stage ($S$) in turn depends on the number of ports ($N$) as $S = log_2 N$. For example, for a 3-stage network, the number of bits required is 3, and in general for N stage network $N$ bits. At every stage the address bits are compared with the node address so as to reach the appropriate output port. To facilitate this, we need ESPMwith minimum control logic at every node.

In this paper, we assume at one particular time slot, the data packets will be sent from any one of the input. The optical data has to be switched to either output 1 or 2. Now, the decision has to be made to choose the desired output. This is done with the help of ESPM.

## 3 | TESTBED SETUP

The block diagram of the proposed hardware model of optical bidirectional switching node is shown in Figure 2 and the hardware testbed is shown in Figure 3. The testbed consists of a Pseudo Random Binary Sequence (PRBS) which can generate random data at a maximum rate of 40 Mbps (Table 1).[10] Laser sources operating in the range of 1550 to 1552 nm, passive devices 80:20 coupler and photo detectors. A 2 × 2 optical MEMS switch with a switching capability of

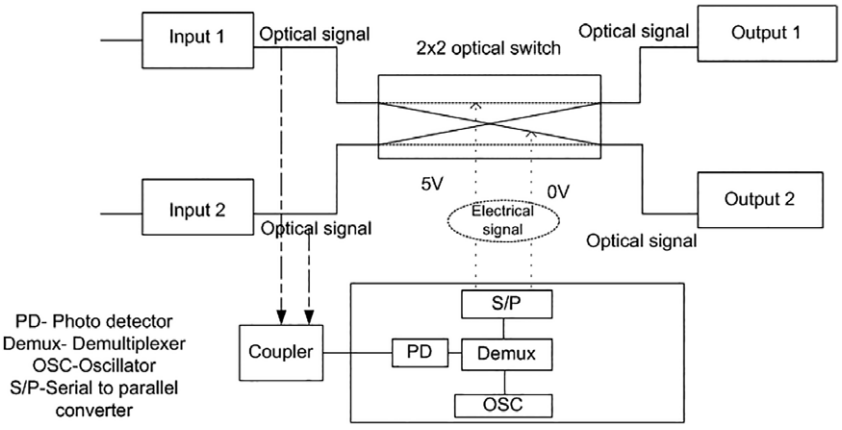


**FIGURE 2** Proposed hardware model of optical bidirectional switching node with ESPM

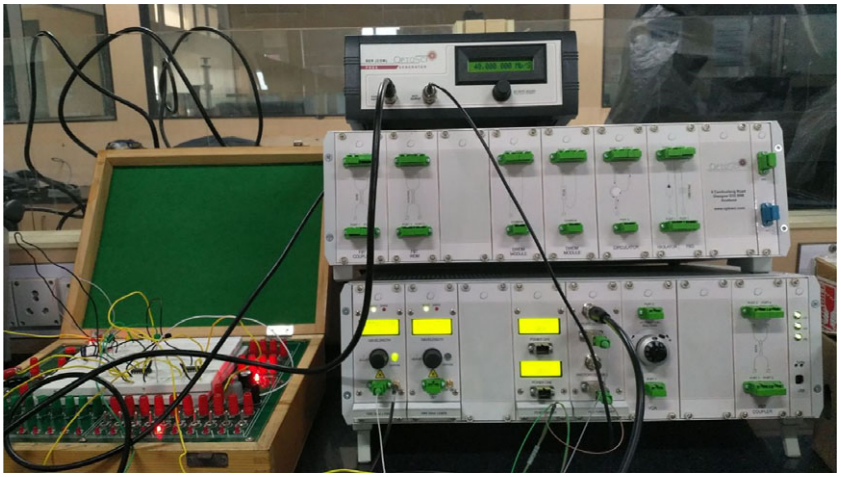

**FIGURE 3** Hardware testbed setup [Colour figure can be viewed at wileyonlinelibrary.com]

**TABLE 1** Parameters of Testbed setup

| Parameter | Value |
|---|---|
| Data rate | 40 Mbps |
| Slot time | 10 ms |
| Switching time of 2 × 2 switch | 1 ms |

1 ms is used for the data switching. The ESPM gives the control signal to the optical switch.

### 3.1 | Electronic signal processing module

The copy of incoming optical data is given to electronic signal processing module where the header bits are extracted. The bits are matched with the node address. If the address matches, ESPM gives logic 1 as the output and the data is routed to output 1, else the ESPM gives logic 0 as the output and data is routed to output 2 as shown in Figure 3.

### 3.2 | Extracting address bits

The optical data from input 1 or 2 is passed through an optical coupler, which is then passed to a photodetector. The photo detector converts the optical signal to electrical signal and this is in turn passed to de-multiplexer. The control signal to a 2 × 1 de-multiplexer is given from an oscillator to alternately pick up the data stream from input 1 or 2. The output of the de-multiplexer is given to the serial to parallel converter. The clock signal to the serial to parallel is given in such a way that only the header bits are extracted and given to the ESPM. Based on the control signal received from the ESPM, the optical switch directs the data to output 1 or 2.

## 4 | RESULTS

In this section, we present the results obtained from the hardware testbed. The ESPM is implemented using minimum discrete electronic components. In this testbed, we have verified data flow in both the directions. To verify the data flow the eye diagram is observed in both the directions. Figure 4 shows the data observed on output 1 in the forward direction, and Figure 5 shows the data observed on output 1 in the reverse direction. Figure 6 shows the eye diagram of the data obtained in the output port. The same has been observed in the reverse direction. Figure 7 shows the power


**FIGURE 4** Data on output 1 [Colour figure can be viewed at wileyonlinelibrary.com]

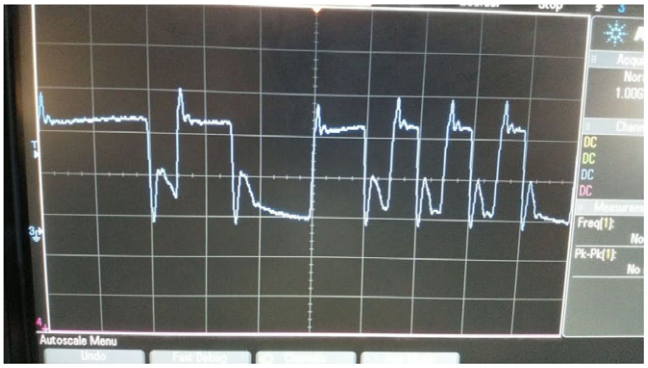


**FIGURE 5** Data in reverse direction [Colour figure can be viewed at wileyonlinelibrary.com]


**FIGURE 6** Eye diagram of output 1 [Colour figure can be viewed at wileyonlinelibrary.com]


**FIGURE 7** Output power in both the channels [Colour figure can be viewed at wileyonlinelibrary.com]

obtained at different ports. From the figure it can be observed that the power obtained in output port 1 is −0.07 dBm and the power obtained in the other port is totally negligible. From the implemented circuit we observed that the processing time is approximately 80 ns.

## 5 | CONCLUSION

In this paper we have proposed and implemented a prototype for optical bidirectional switching node. The data transmission in both the direction has been successfully implemented with minimum electronics in the ESPM. The results are verified with the help of eye diagram and power meter. The total processing delay incurred in the ESPM is around 80 ns which is negligible compared to the switching speed of 2 × 2 switches. Therefore, the data can be transmitted with minimum delay in both the directions.


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