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RESEARCH ARTICLE

Hardware implementation of contention aware optical switching node for data center networks

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Abstract

In the multistage bidirectional networks, the same node is accessed multiple times in the same time slot resulting in contention. In this article, we experimentally demonstrate the contention resolution with minimum electronics. This is verified in the experimental testbed and the data is switched from one node to other node without contention. The results are verified in terms of eye diagram in both the directions.

KEYWORDS

bidirectional networks, contention resolution, testbed implementation

1 | INTRODUCTION

Highly scalable optical packet switched networks with large number of port counts are deployed in data center networks to obtain high throughput while achieving the low latency.[1] Multistage bidirectional optical network is a suitable candidate to sustain the huge internet traffic. The multistage network includes more than 10 000 port counts in which every source and destination node may have multiple paths.[2] The data are transferred from source node to destination node by crossing multiple node and paths. It is obvious that the same node is accessed multiple times in the same time slot.[2] Therefore, the contention should be resolved so that only one packet is processed in a time slot at any node. This can be achieved with a suitable signal processing module. In the all optical networks, the contention is handled by wavelength routing.[3,4] But the bidirectional data traffic needs multiple wavelengths for contention resolution and increases the complexity. Therefore, we propose the suitable control logic to resolve the contention with minimum electronics. The bit level processing in the electronics domain resolves contention and aids simple routing of data from source to destination node. We have demonstrated the bidirectional communication with electronics signal processing in Reference 5. In many multistage interconnection networks like Benes, Butterfly, Shuffle net, there are more than one path available from any source node to any destination node. Since, every packet has to reach the desired destination node from a source node, by selecting the path via the intermediate nodes, there is a possibility of choosing the same intermediate node while selecting the path from different input ports. Therefore, there is a possibility of contention and has to be resolved to achieve better throughput otherwise the contented packet may go into an indefinite loop wherever the default path is available and may not allow the new packet to enter into the network. In this article, we choose a multistage interconnection network to explain and demonstrate the contention resolution with minimum electronics.

The rest of the article is organized as follows: section 2 discusses the contention in a multistage network. Section 3 gives the proposed hardware model to resolve contention. In section 4, implementation of contention resolution in a testbed is demonstrated. Section 5 gives observed results and discussions. Section 6 gives the concluding remarks.

2 | CONTENTION IN MULTISTAGE NETWORK

Optical multistage networks with multiple port counts have become important for next-generation networks. Many different technologies are available to realize optical multistage networks. The first generation optical network architectures consist of point to point WDM links. Such networks are comprised of several point to point links at which all traffic arriving to a node is converted from optics to electronics, processed electronically, and converted from electronics to optics before departing from the node. This conversion at every node in the network involves significant overhead in terms of switch complexity and electronic processing cost. Alternative approach is to have a packet with header and

data bits, where only the header bits can be converted for switching the appropriate node. We have demonstrated the optical bidirectional switching node in which header bits are processed and allowed to choose the appropriate link.[5] In many chained multistage interconnection network, every packet passes through multiple nodes before reaching its destination node. Since it is multistage network, more than one path is available between every source and destination node, even if the packets with different destination uses the same set of nodes in the same time slot then there will be a contention. This contention is resolved minimum electronics so that only one packet can be used in one time slot.

To implement the contention resolution in a hardware testbed, we assume a bidirectional chained multistage network.[6,7] Every node is assumed to have two inputs and two outputs in both directions as shown in Figure 1. At every node, packets may arrive and leave in both directions. Therefore, there is a high possibility of contention at every node. For example, node 13 can receive (as well send) packet from (to) node 20 and 9 in one direction and node 16 and node 29 in the opposite direction. But every node can process only one packet in a time slot.

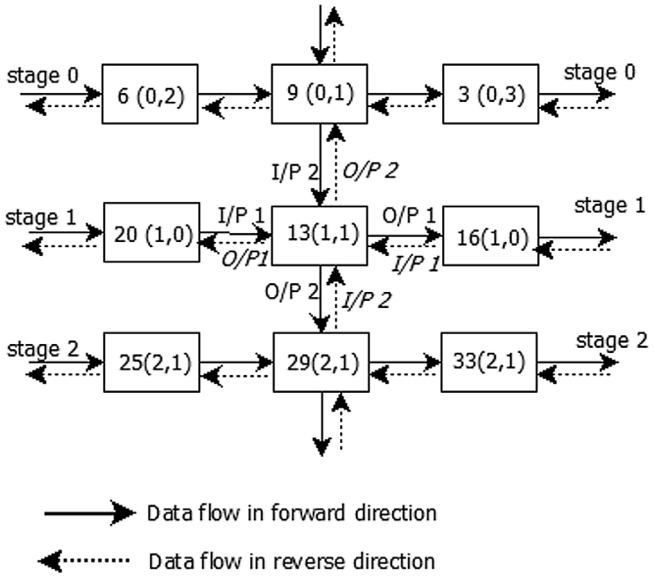

FIGURE 1 Group of nodes in a bidirectional multistage interconnection network

3 | PROPOSED HARDWARE MODEL TO RESOLVE CONTENTION

Now, in this article, the proposed hardware model in Figure 2 along with electronic signal processing module (ESPM) resolves contention shown in Figure 1. Each node is a 2 x 2 switch node (two input links and two output links). In Figure 2, all the four neighboring nodes (node 20, node 16, node 9, and node 29) are connected to node 13 as discussed in section 2. The hardware model includes, forward transmitter module, forward receiver module; reverse transmitter module; reverse receiver module; switch module; and

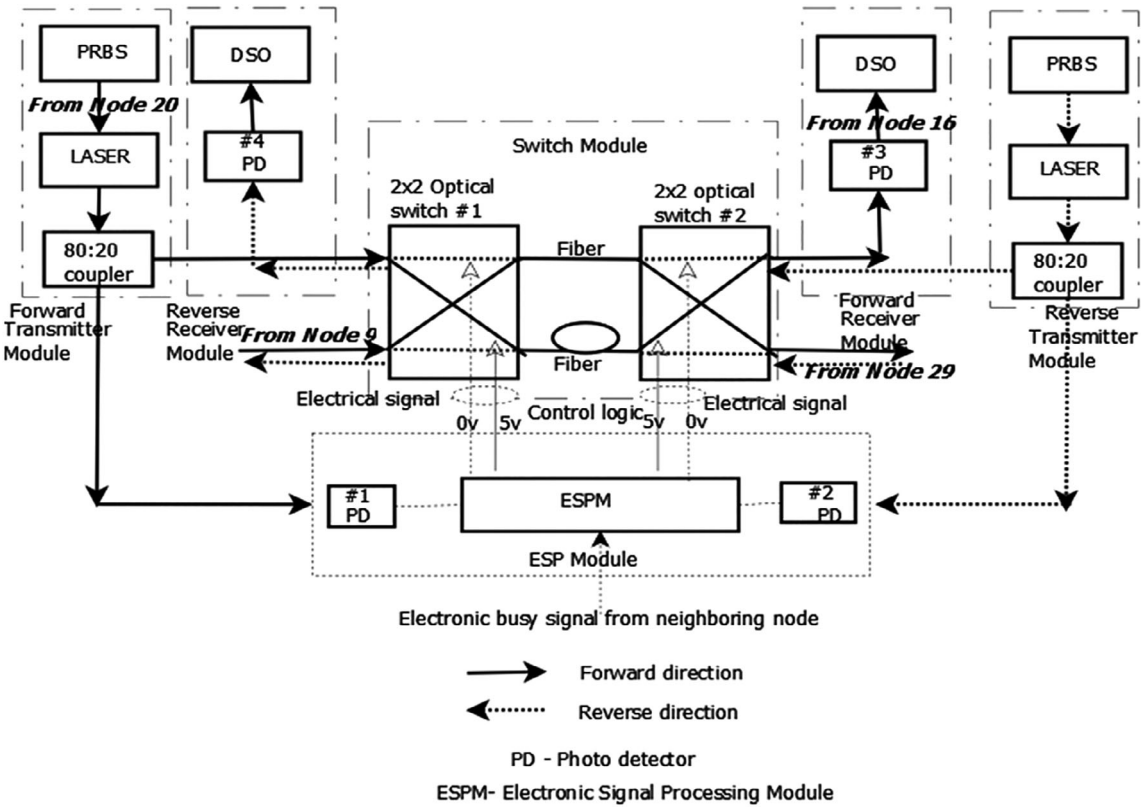

FIGURE 2 Hardware model for a bidirectional switching node for contention resolution

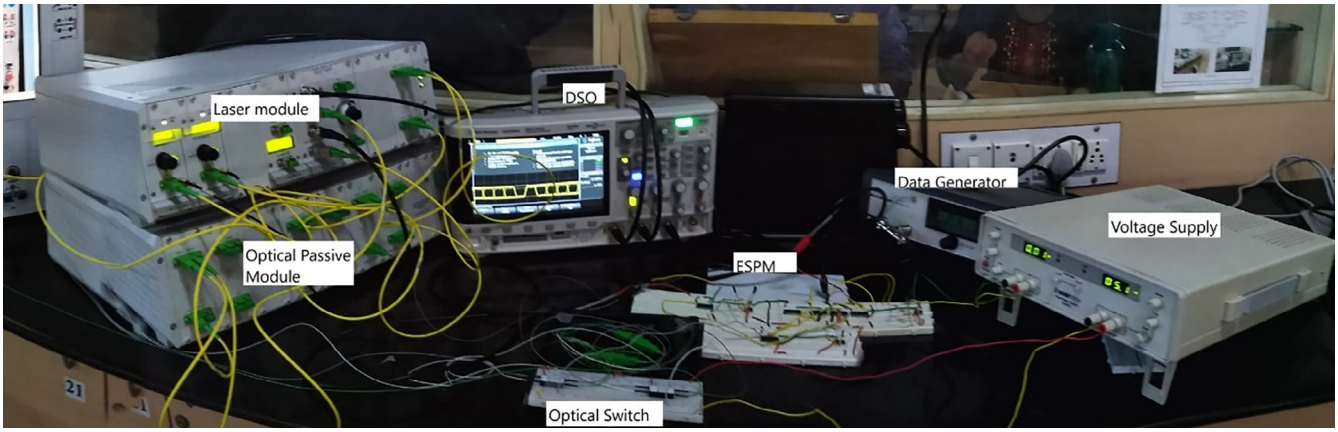

FIGURE 3 Testbed setup [Color figure can be viewed at wileyonlinelibrary.com]

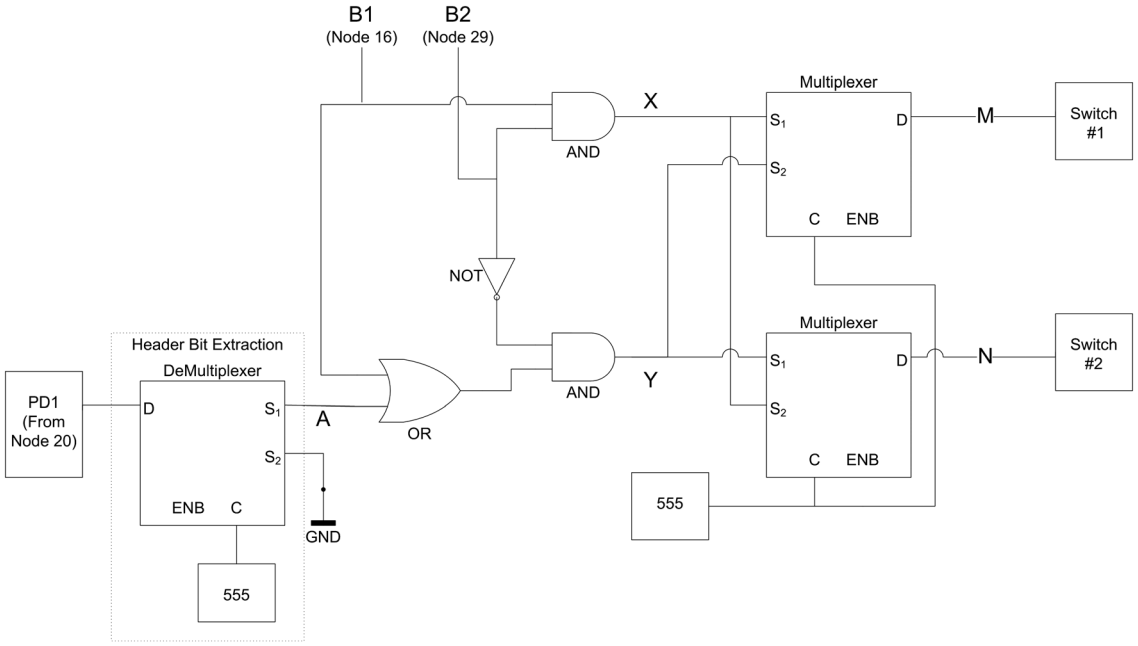

FIGURE 4 Electronic signal processing module in node 13

ESPM. Figure 3 shows the hardware implementation of the proposed model. Every incoming packet consists of header bits (destination address) and payload (data bits). The packet is generated from the PRBS and modulates the LASER. Here, using 80:20 coupler, the data are tapped and given to photo detector. From the photodetector, the electrical signal is given to signal processing module. In the signal processing module, the decision to switch the appropriate link is made and optical data from the 80:20 coupler is sent to the desired destination node. From the packet, the header bits are decoded, out of which the first bit (framing bit) is used to indicate the direction (forward(1)/reverse(0)). Based on the size of the network, the number of address bits is decoded. The address bits are indicated in binary d1,d2,…dn. The number of bits to be decoded to find the desired destination depends on $\log_2 N$-1. Here, we consider a four stage network, which includes 12 nodes. Therefore, only three bits are used to indicate the destination address. Header bits are compared with the node address. If the address matches, then it is compared with busy signal from the neighboring nodes. If the next node is free then the packet is sent to that node. For example, if the packet comes from node 20 which has to be sent to node 29 through node 13. Then the ESPM of node 13 performs the address matching and also checks status of node 29 whether it is busy/free. From the packet, which comes from node 20, the address bits are extracted and compares with the busy signal. If node 29 is free then the packet is forwarded. Otherwise, the packet is deflected to the neighboring node present in the same stage (node 16). If both nodes are free then according to the priority the packet is forwarded to next stage node that is to node 29, moving toward the destination. If the packets are coming simultaneously from both directions, that is, from node 16 to node 20 then alternative priority is maintained. If both nodes are busy, then the packet is delayed in the fiber loop for one time slot. The same logic is followed for all the nodes and is implemented in hardware. The priority condition, busy status and address bit decoding is carried out using electrical signals (ESPM). The timing

TABLE 1 Truth table for packet from node 20 (forward) and node 16 (reverse)

Truth table for packet from node 20 (forward)							
Busy 1 (B1) node 16	**Busy 2 (B2) node 29**	**Address matching (A)**	**Forward/reverse output node**	**Output (X/Y)**	**Priority**	***M***	***N***
0	0	No	16	Y	0 (forward)	0	0
0	0	Yes	29	Y	0 (forward)	0	1
0	1	$X_{(do\ not\ care)}$	16	Y	0 (forward)	0	0
1	0	Yes	29	Y	0 (forward)	0	1
1	0	No	Fiber delay line				
1	1	$X_{(do\ not\ care)}$	Fiber delay line	X	0 (forward)	1	$X_{(do\ not\ care)}$
Truth table for packet from node 16 (reverse)							
Busy 1 (B1) node 20	Busy 2 (B2) node 9	Address matching (A)	Forward/reverse output node	Output (X/Y)	Priority	*M*	*N*
0	0	No	20	Y	1 (reverse)	0	0
0	0	Yes	9	Y	1 (reverse)	1	0
0	1	$X_{(do\ not\ care)}$	20	Y	1 (reverse)	0	0
1	0	Yes	9	Y	1 (reverse)	1	0
1	0	No	Fiber delay line				
1	1	$X_{(do\ not\ care)}$	Fiber delay line	X	1 (reverse)	$X_{(do\ not\ care)}$	1

TABLE 2 Truth table for 2 x 2 switch

Input	***M***	***N***	**SW1**	**SW2**	**Output**
20 (forward)	1	1	Cross	Cross	Delay
	1	0	Cross	Bar	Delay
	0	1	Bar	Cross	29
	0	0	Bar	Bar	16
16 (reverse)	1	1	Cross	Cross	Delay
	1	0	Cross	Bar	9
	0	1	Bar	Cross	Delay
	0	0	Bar	Bar	20

TABLE 3 Parameters used

Parameter	**Value**
LASER wavelength	1550 nm (forward) 1549 nm (reverse)
LASER power	1 mW
Data rate	40 Mbps
Slot time	5 ms
Packet size	40 Kb
Delay	1 ms
Switching time of 2 x 2 switch	<1 ms
Insertion loss	<1.0 dB
Fiber type	Single mode
Select (3.3-5 V)	Cross state
Select (0 V)	Bar state
Electrical power consumption for 2 x 2 switch	10 mW
Mode	Non-Latching (CMOS/TTL logic)

synchronization is maintained using appropriate delay lines. In this bidirectional data flow, the entire payload is in optical domain and only the header bits alone are converted into electrical. This aids in reducing the processing delay. This hardware model is a suitable prototype and can be extended to "N" number of nodes by suitably modifying the electronic counterpart. However, the logic followed for extraction of address bits and transmission of data remains the same.

4 | IMPLEMENTATION OF CONTENTION RESOLUTION IN A TESTBED

As a packet enters the node through the 80:20 coupler, 80% of the power is used to send the data packet to its destined output port and 20% of the power is used to monitor the header bits and is sent to ESPM. We assume the ESPM is in node 13 (Figure 4). The packet can come from node 20 in the forward direction and from node 16 in the reverse direction (Figure 1). Only one packet is processed in one time slot. In the ESPM module, the data from photodiode is extracted and is given to a de-multiplexer. The output from 555 timer module which generates a clock of 1 ms time period and duty cycle of 99% (ie, $T_{on}/T_{off} = 99/1$) is given

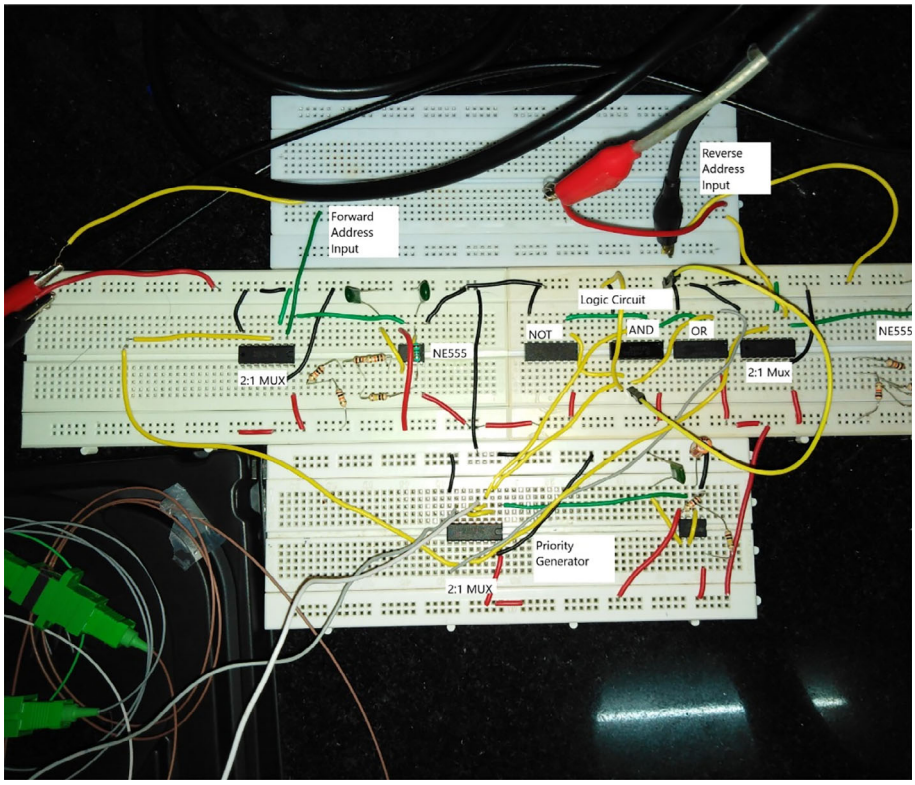

FIGURE 5 Electronic signal processing module [Color figure can be viewed at wileyonlinelibrary.com]

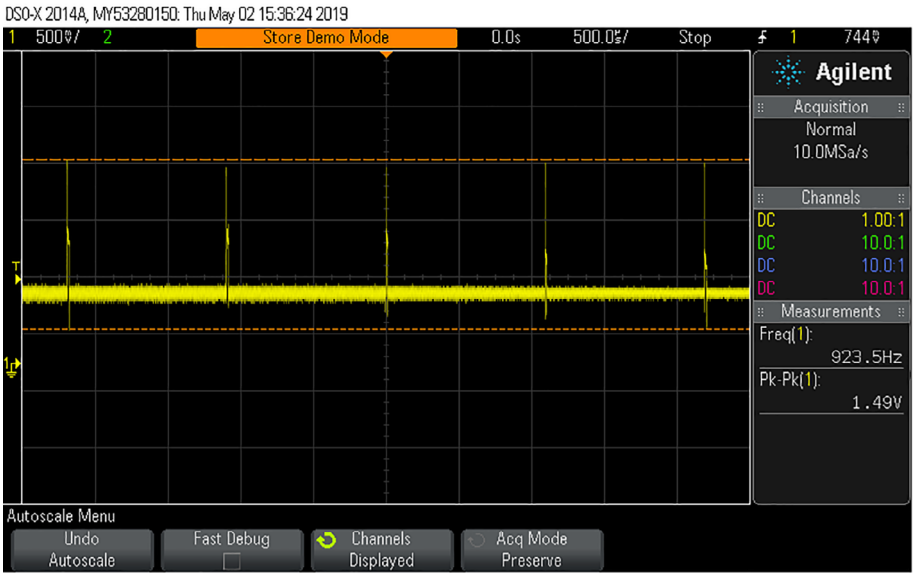

FIGURE 6 Extracted header bits [Color figure can be viewed at wileyonlinelibrary.com]

as the select line of the demutiplexer. The required address bits are taken from the de-multiplexer. Based on the first bit the direction is decided. If the first bit is "0" then the data flow is in the forward direction and if it is "1" then the data flow is in the reverse direction. The second bit is matched with node address, if matches then compared with busy signal from the neighboring nodes. If the neighboring node is free then the data is forwarded to the next stage node 29 as given in Table 1. The corresponding data from the input port is directed to the 2 x 2 MEMS switch based on the decision made from ESPM. The control signal from ESPM is given to switch#1 and switch#2 in such a way that, switch#1 is in Bar state and switch #2 is in cross state as given in Table 2. Based on the select line given, the switch operates in the bar state or cross state (if select = 1). If the address does not match or the

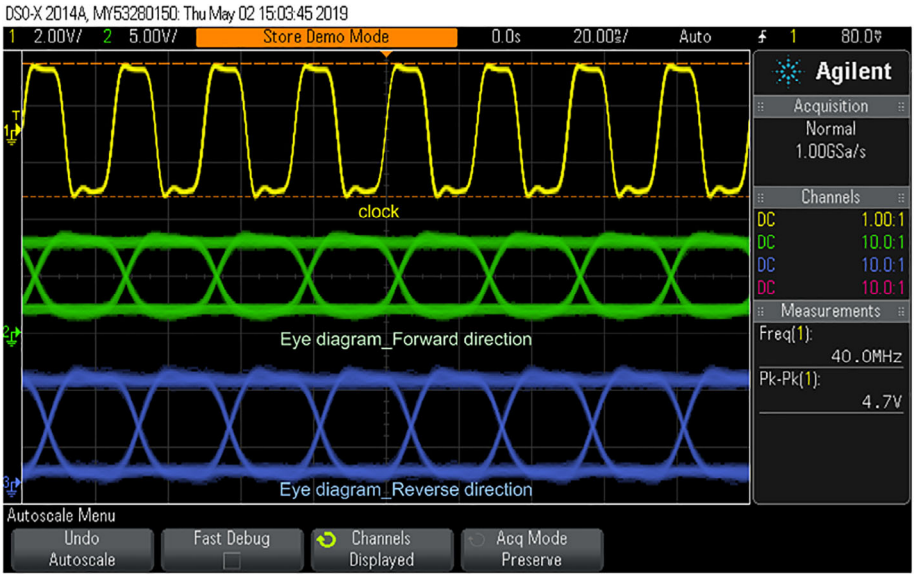

FIGURE 7 Eye diagram observed in forward and reverse direction after contention resolution [Color figure can be viewed at wileyonlinelibrary.com]

neighboring node is busy then the data is deflected in the same stage node 16. The data are routed to the desired destination through the appropriate switches as per the Table 1. The same routing logic is followed throughout the network. The parameters used in the testbed are given in Table 3. The same hardware arrangement for ESPM module is shown in Figure 5.

5 | RESULTS

In this section, we present the results obtained from the hardware testbed. The ESPM is implemented using minimum discrete electronic components. The header bits are extracted from the packet and are shown in Figure 6. As discussed in section 4, the address bits are decoded to decide the direction of the data flow. Further, the header bits are compared with the busy signal to route the packet to the appropriate destination node. In this testbed, we have verified the contention resolution in a group of nodes, in both the directions. To verify the correctness of the data flow, the eye diagram is observed in both forward and reverse directions. Figure 7 shows the eye diagrams observed in forward and reverse direction after contention resolution. Since the contention is resolved appropriately the packets are forwarded in different time slots, the eye diagrams are verified in the same display. The hardware model is implemented for a group of nodes and the decision making of ESPM is in only one node. The packet is passed through only one node (maximum two hops) in any of the directions in a time slot. Therefore, the signal degradation is negligible. This can be observed from the eye patterns shown in Figure 7.

6 | CONCLUSION

In this article, we have proposed and demonstrated the contention resolution of a multistage optical bidirectional network. The data transmission in both the direction has been successfully implemented by handling the priority check between the directions, address matching and busy signals from the neighboring nodes in the ESPM with minimum control logic. The results are verified with the help of eye diagram.

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REFERENCES

[1] Shacham A, Small BA, Ladouceur OL, Bergman K. A fully implemented 12x12 data vortex optical packet switching interconnection network. *J Lightwave Technol*. 2005;23(10):3066-3075.

[2] Sangeetha RG, Chandra V, Chadha D. Optical interconnection bidirectional data vortex network: architecture and performance analysis. *IEEE J Lightwave Technol*. 2013;31(8):1283-1294.

[3] Berry RA. Wavelength Routing for all Optical Networks [PhD dissertation]. USA: MIT; 1993.

[4] Gong J, Xu J, Luo M, et al. All-optical wavelength conversion for mode division multiplexed superchannels. *Opt Express*. 2016;24:8926-8939.

[5] Mishra S, Yadav V, Hemanth C, Sangeetha RG. Hardware implementation of optical switching node for data center networks. *Microw Opt Technol Lett*. 2019;61:843-846.

[6] Sangeetha RG, Hemanth C. Performance analysis of chained K-ary data centre networks. India: 13th International Conference on Fiber Optics and Photonics, OSA Technical Digest (online) Optical Society of America; 2016.

[7] Chandra V, Chadha D, Sangeetha RG. Bidirectional optical data packet switching interconnection network. U.S. Patent No. 9, 031, 407, 2015.

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