

A Project Report
On
IMPLEMENTATION OF OPTIMIZED CLA (CARRY LOOK AHEAD ADDER).

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Under the supervision
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ACKNOWLEDGEMENT

I wish to acknowledge the importance of this project titled "**IMPLEMENTATION OF OPTIMIZED CLA(CARRY LOOK AHEAD ADDER)**" Provided by Dr.Parikshit Sahatiya of EEE department.

From this project, I will gain knowledge and about the use of low power designing techniques, by implementation of one such technique on CLA (carry look ahead adder).

I wish to express my appreciation to Birla Institute of Technology and Science for keeping these project as a disciplinary elective for Higher Degree (HD) ME Microelectronics (EEE Department).

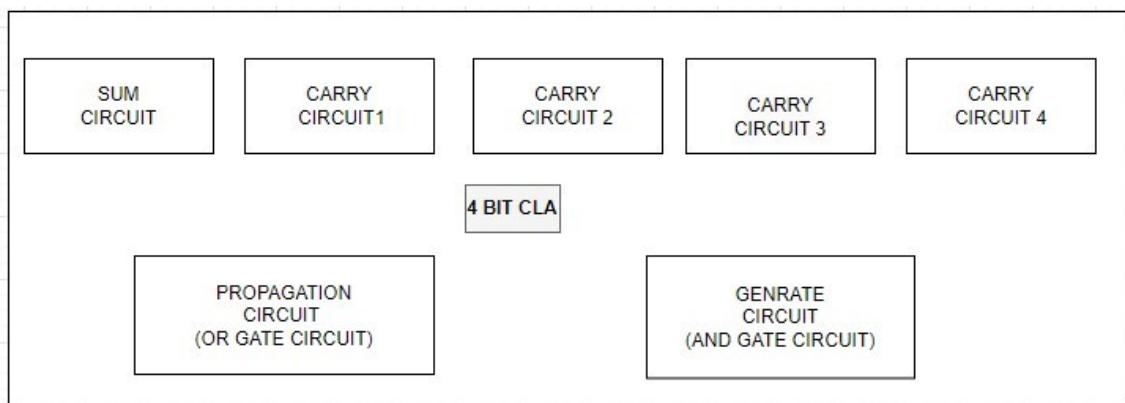
ABSTRACT

Any analogue, digital, or DSP control system's basic operation is addition. Almost all digital systems depend on the adder's performance for dependability and performance. To attain the best power, delay, and powerdelay product (PDP) results, numerous adder topologies have been suggested during the past ten years, and numerous other research projects are in progress. As a result, we created a Carry Look Ahead Adder (CLA) and used MTCMOS technology to optimize its power usage.

INTRODUCTION

The circumscribed battery life places strict constrictions on the overall power expenditure of ultrahigh density VLSI chip designs, and power consumption (heat dissipation) must be controlled as portability becomes more and more decisive. On the other hand, the operating swiftness is the only factor that the supply voltage can affect in terms of power consumption. Similar numbers of CPUs have adders as part of their critical path. Adder is a crucial block in the ALU that does a number of tasks.

A fast adder, also known as a carrylookahead adder, is a kind of electronic adder used in the design of digital logic. Performance and other factors are crucial for the design of an IC. By introducing more intricate circuitry, a carry adder decreases propagation time.



Block diagram of CLA

OPTIMIZING TECHNIQUE

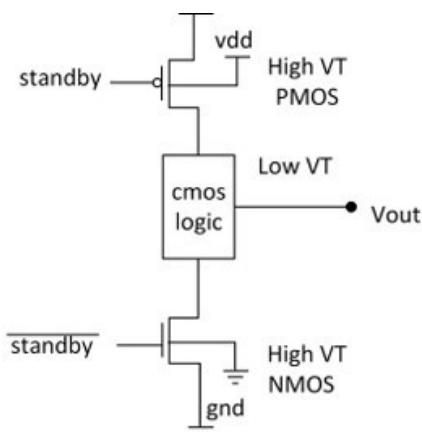
MTCMOS

As CMOS technology scales, supply voltages and threshold voltages drop. The sub-threshold leakage current increases exponentially as the threshold voltage is brought down. More than 40% of the total active-mode energy in today's high-performance integrated circuits (ICs) is lost as leakage currents. Leakage current will quickly outweigh the overall power consumption of high performance integrated circuits as more and more transistors are put on a chip. Multi-threshold voltage CMOS (MTCMOS) is an established low-leakage circuit technique.

The two main structures of multi-threshold CMOS technology are as follows. First of all, for effective power management, the "Active" and "Sleep" operating modes are integrated with MTCMOS technology. Second, Nchannel and Pchannel MOSFETs in a single device use two separate threshold voltages.

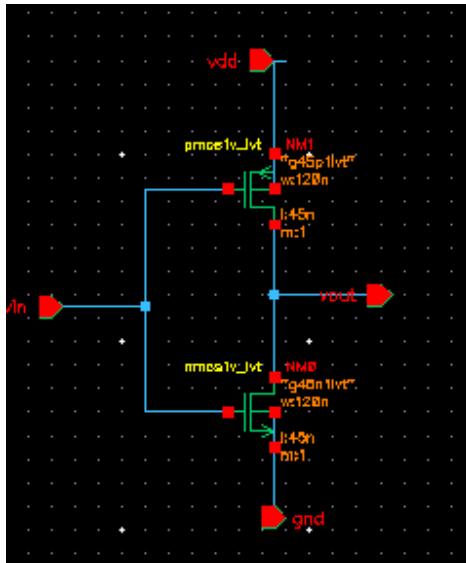
The term "power gating" refers to the method of isolating the low threshold voltage (low V_t) logic gates from power and ground by shutting down off the high threshold voltage (high V_t) sleep transistor.

To implement the logic, low threshold voltage transistors are used. In order to avoid leakage dissipation during standby (sleep) mode, high threshold voltage transistors are employed to detach low threshold voltage transistors from supply and ground. In the active mode, sleep transistors are activated, allowing the logic made up of low V_t transistors to operate quickly and efficiently. The high V_t transistors are incapacitated when the circuit is in sleep mode, isolating the low V_t transistor from supply voltage and ground and decreasing sub-threshold leakage current.

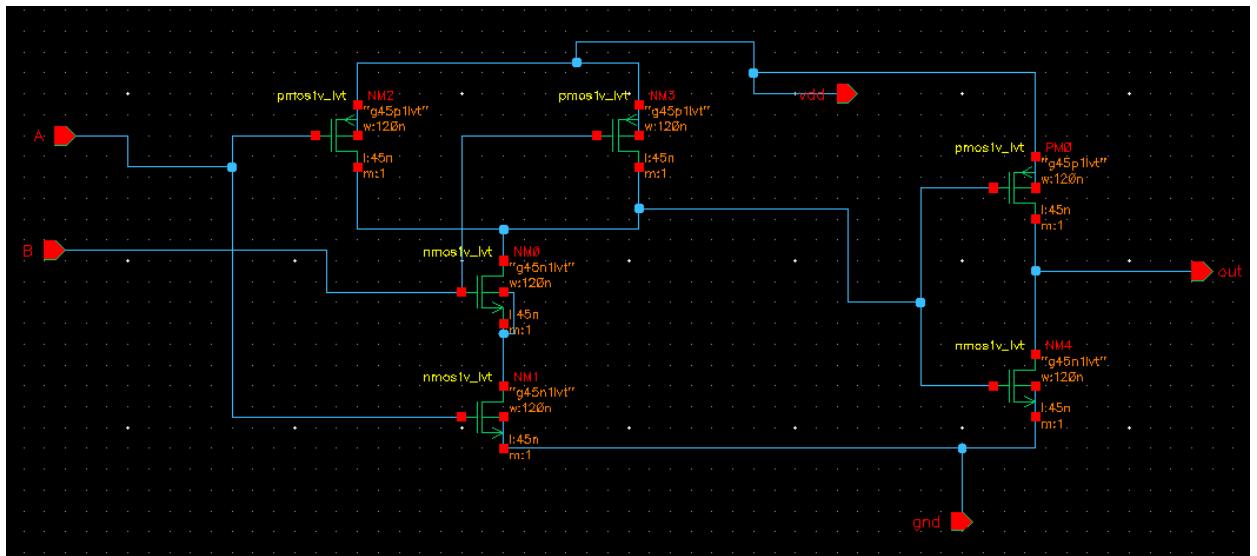


MTCMOS LOGIC

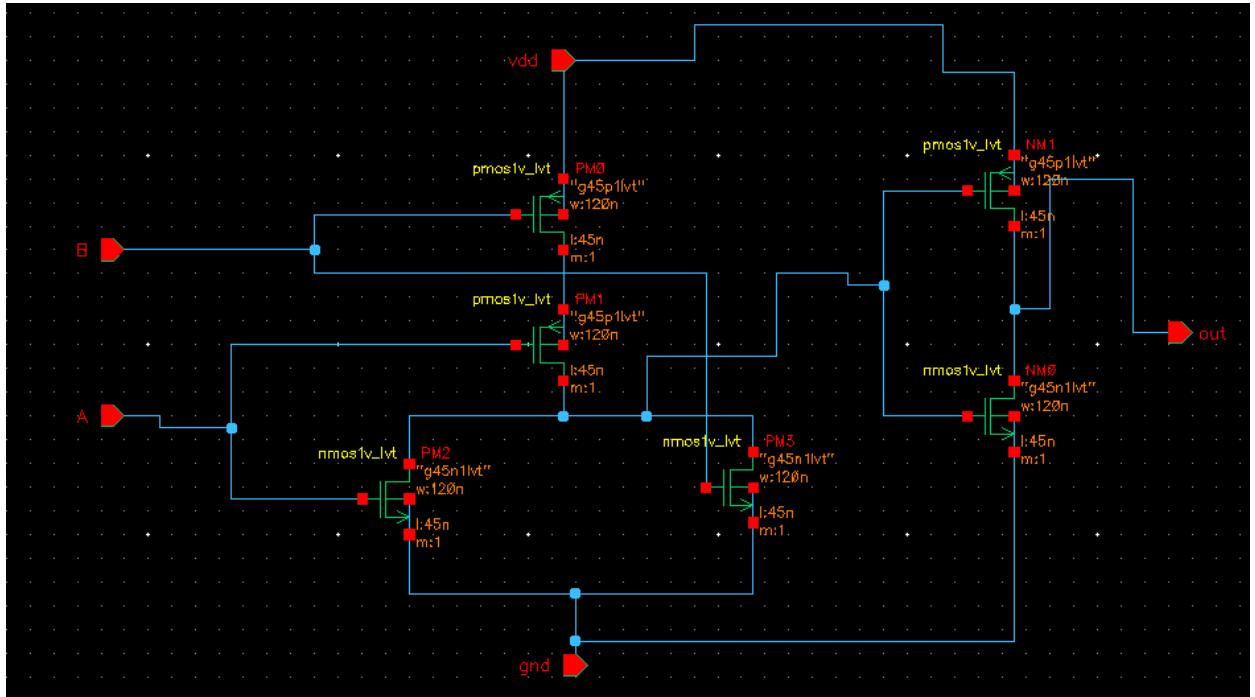
IMPLEMENTATION OF CLA



Inverter Schematic



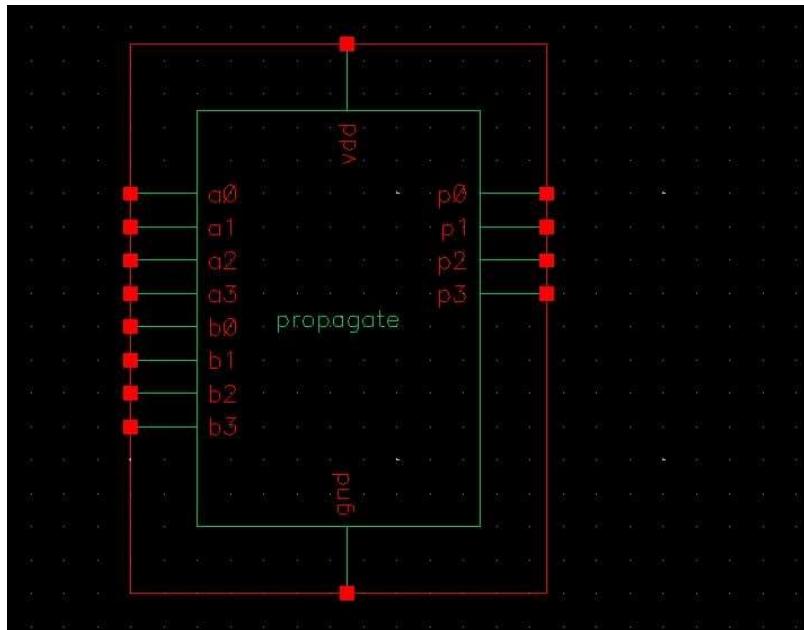
And Gate Schematic



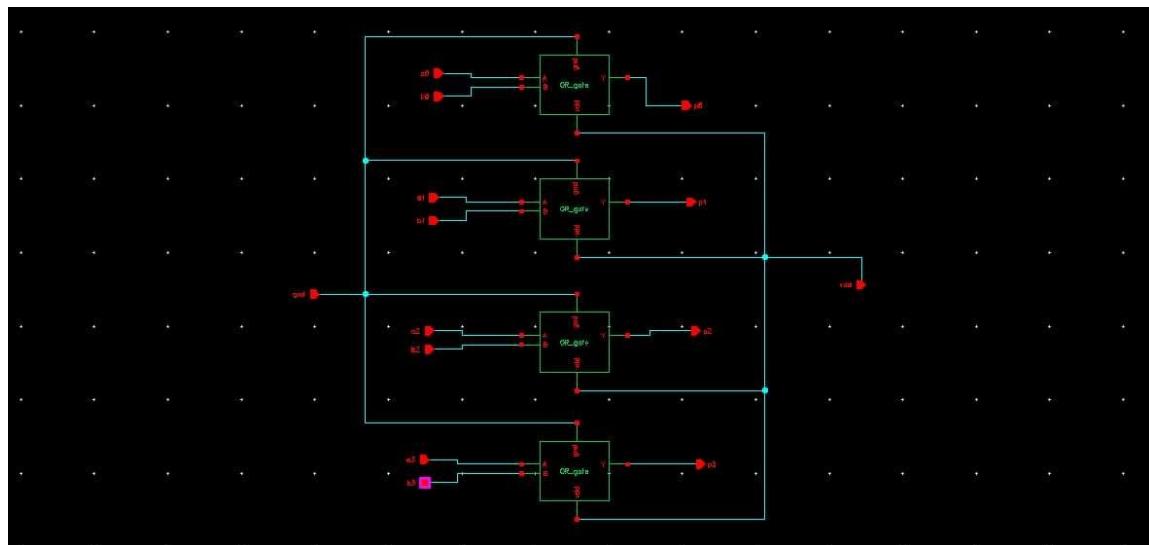
OR gate Schematic

Propagate block equation

$$\overline{P_i} = A_i \oplus B_i$$



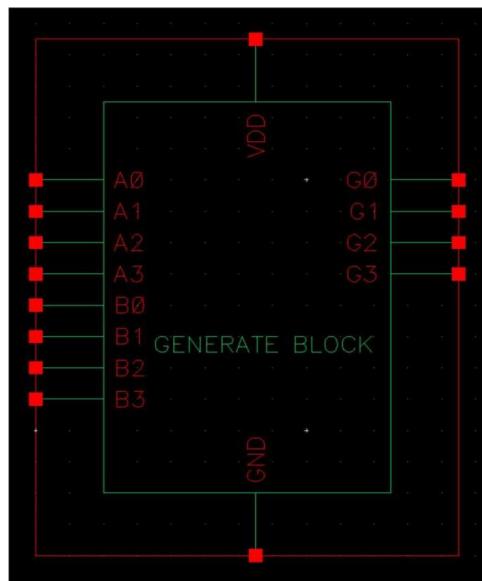
Propagate Block



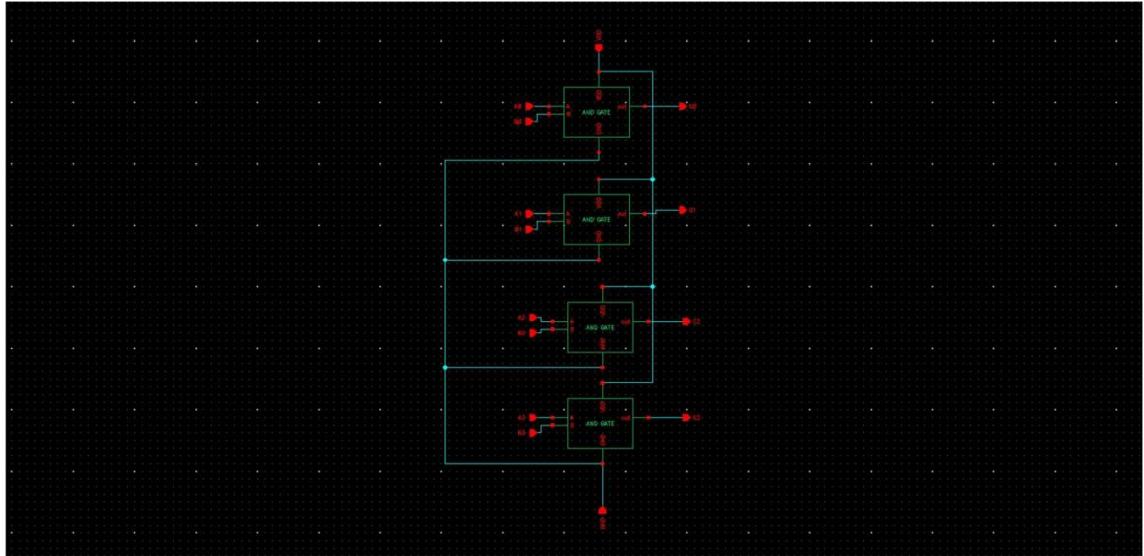
Propagate Block Schematic

GENERATE block equation

$$G_i = A_i B_i$$



Generate Block



Generate Block Schematic

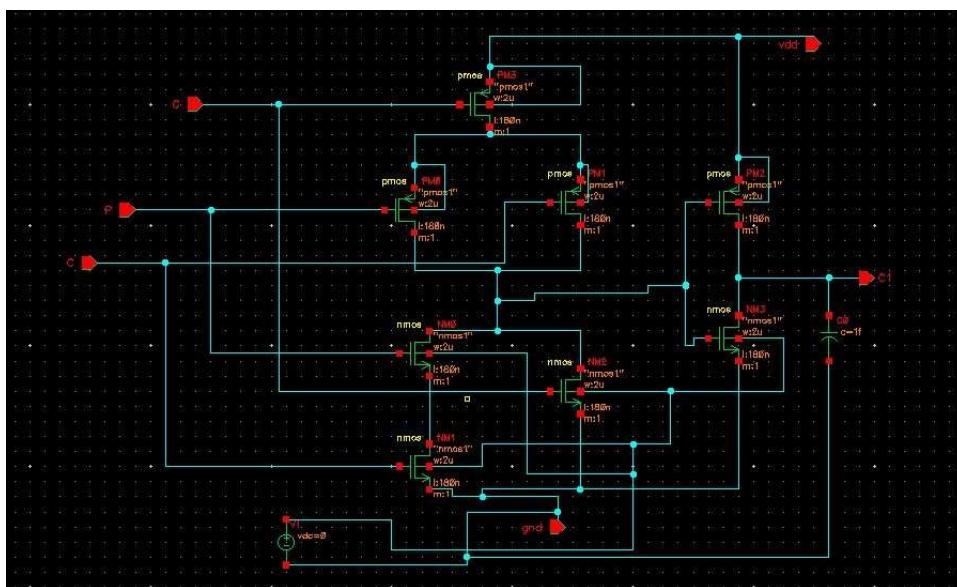
CARRY BLOCKS EQUATIONS

$$C_1 = G_0 + P_0 C_{in}$$

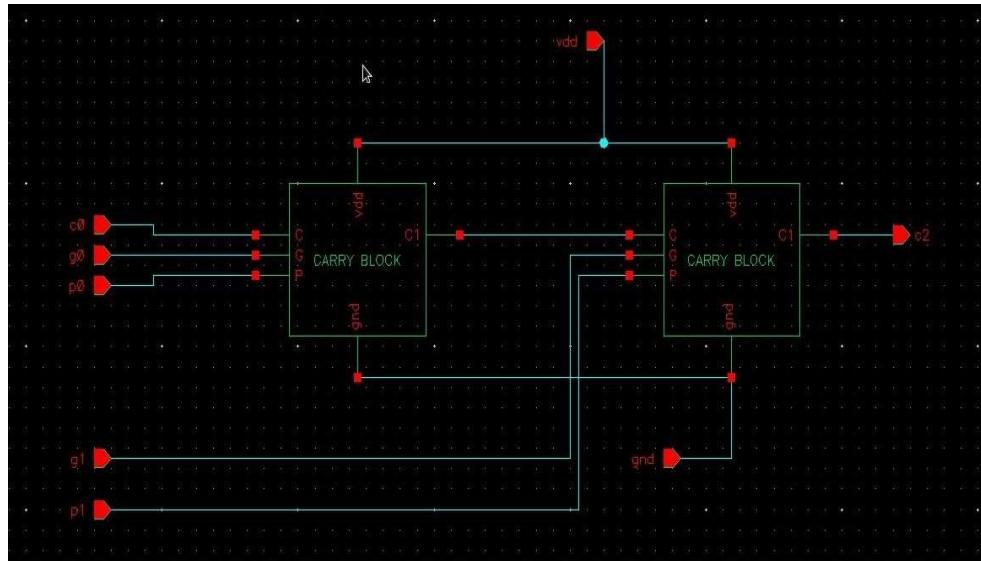
$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{in}$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$$

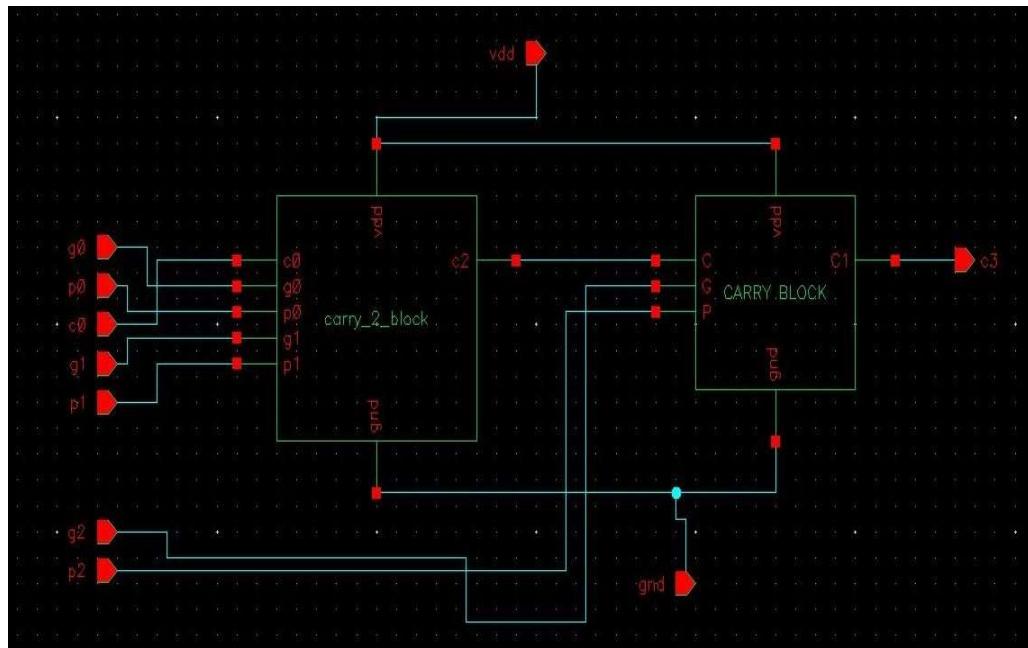
$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{in}$$



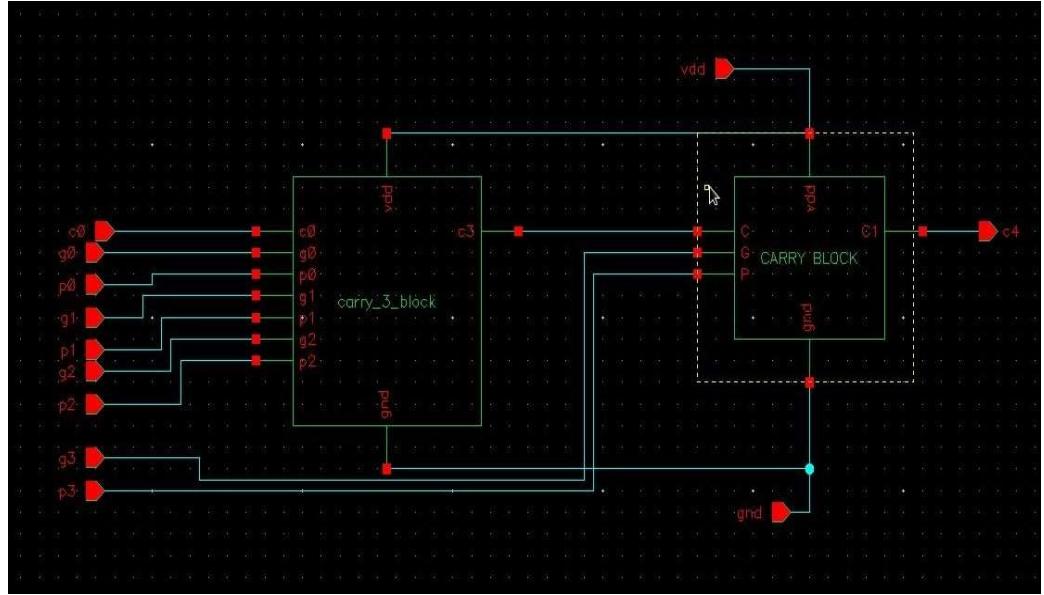
Carry 1 Block Schematic



Carry 2 Block Schematic



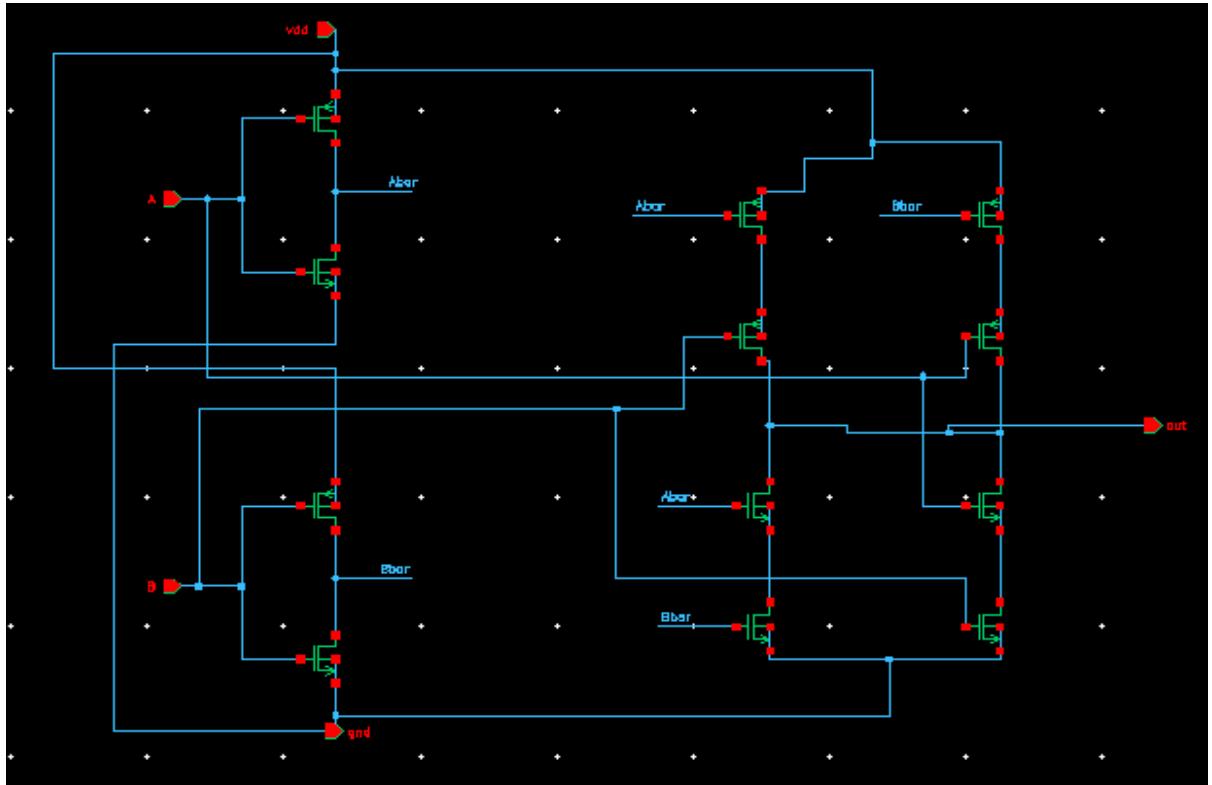
Carry 3 Block Schematic



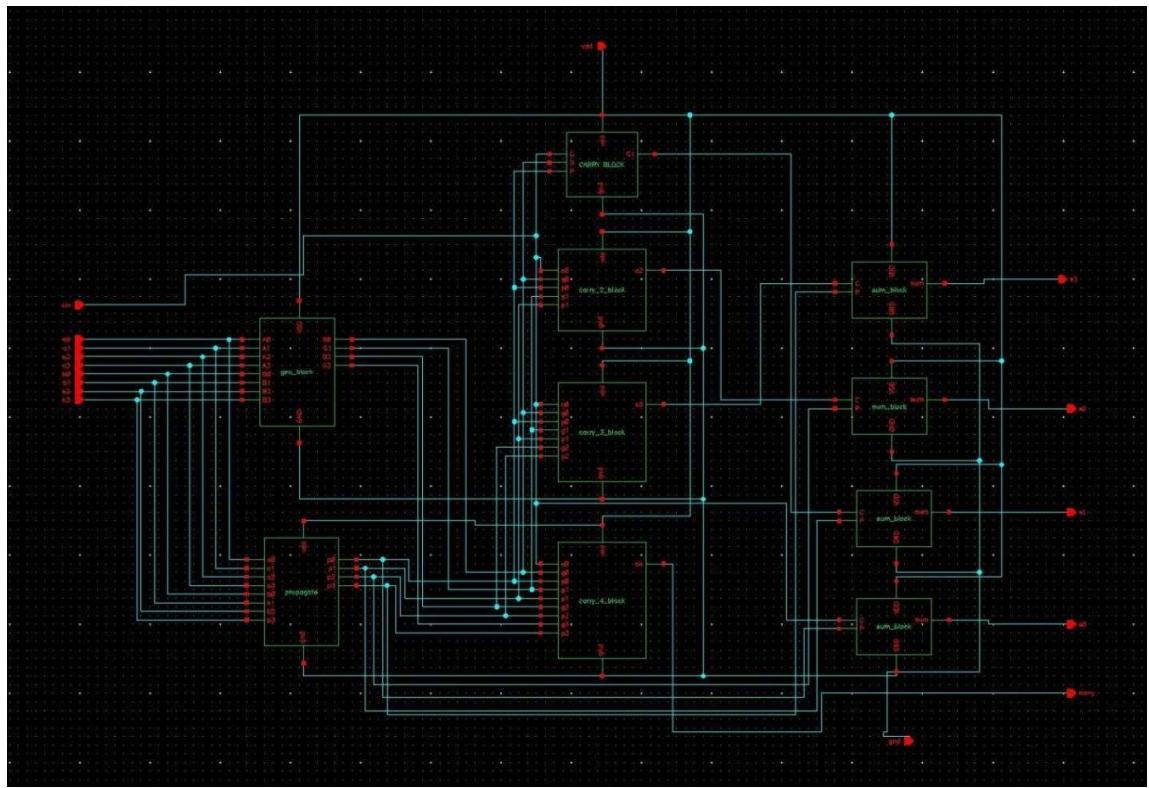
Carry 4 Block Schematic

SUM BLOCK EQUATION

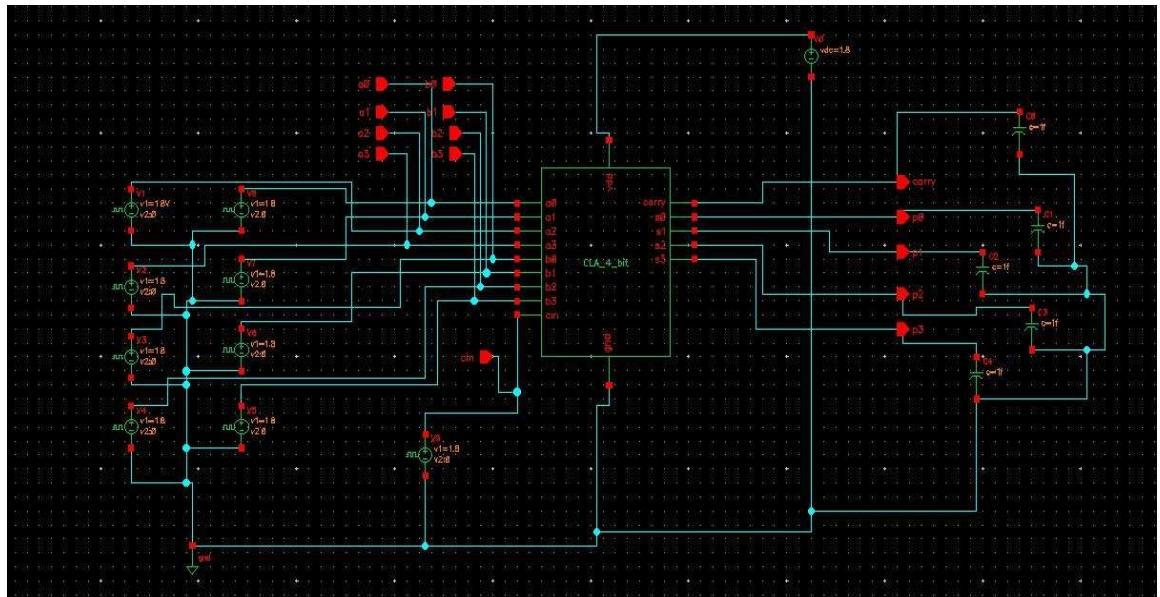
$$S_i = P_i \oplus C_i$$



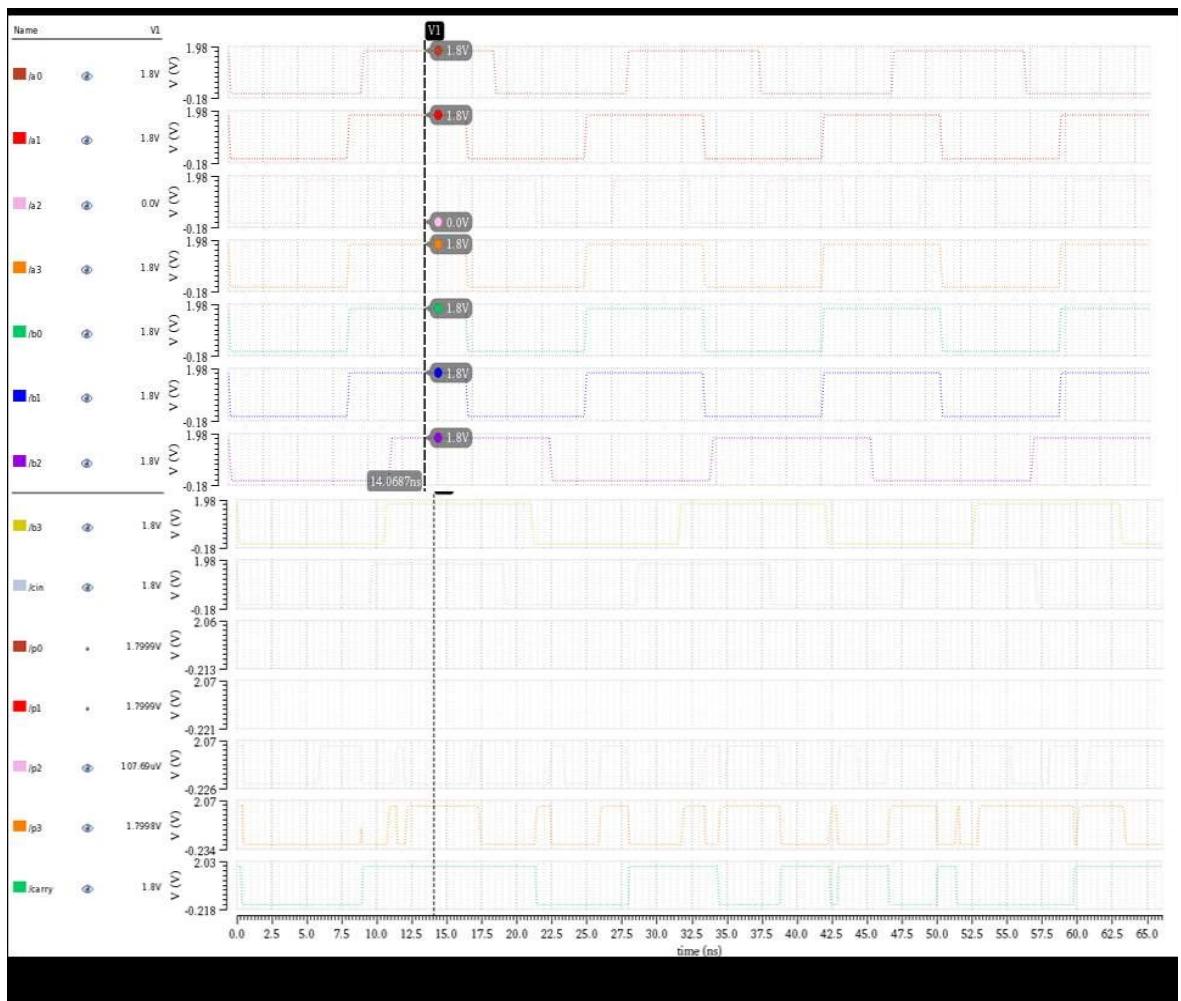
SUM BLOCK SCHEMATIC



CLA DESIGN



CLA SCHEMATIC



CLA WAVEFORM

As per the waveform

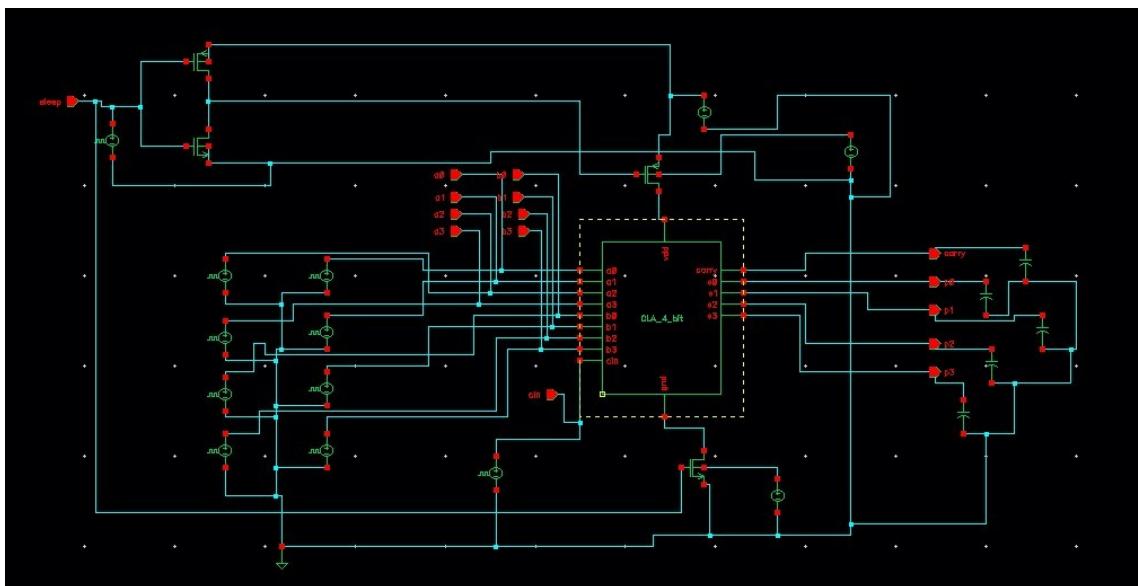
Inputs : A=1011

B =1111

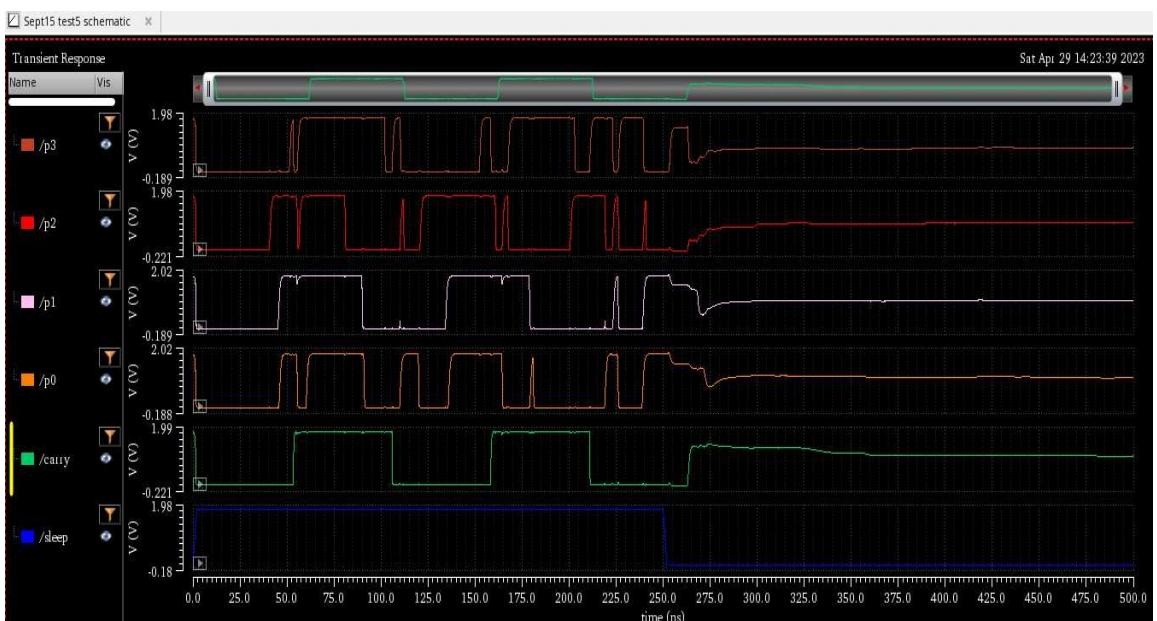
Cin = 1

Output : Sum = 1011

Carry= 1



OPTIMIZED CLA DESIGN



OPTIMIZED CLA WAVEFORM

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

cadence

Expression	Value
1 average(getData("pwr") ?result "tra...")	84.30E-6

NORMAL CLA POWER

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

cadence

Expression	Value
1 average(getData("pwr") ?result "tra...")	52.79E-6

OPTIMIZED CLA POWER (sleep on&off)

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

cadence

average(getData(":pwr" ?result "tra...")

Expression	Value
1 average(getData(":pwr" ?result "tra...")	81.89E-6

OPTIMIZED CLA POWER (sleep on)

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

cadence

average(getData(":pwr" ?result "tra...")

Expression	Value
1 average(getData(":pwr" ?result "tra...")	1.059E-9

NORMAL CLA Static POWER

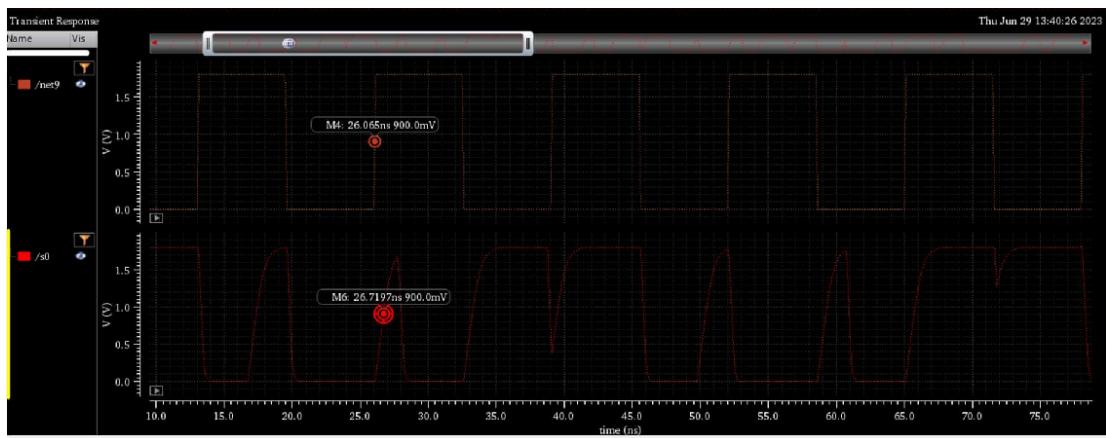
Virtuoso (R) Visualization & Analysis XL Table

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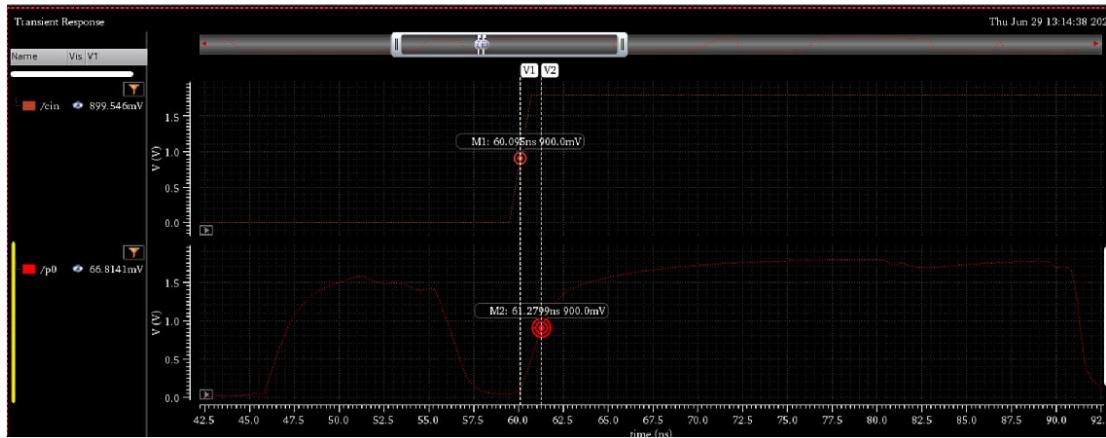
cadence

Expression	Value
1 average(getData(":pwr" ?result "tra...")	27.57E-12

Optimized CLA Static POWER



NORMAL CLA



OPTIMISED CLA

As calculated from above timing

graph:Normal CLA (tp)= 0.0.8859ns

Optimized CLA (tp)=0.979ns

Conclusions-

- We can clearly deduce by looking at the delay the optimized CLA is taking more time for producing the output, while the power is getting reduced. Hence establishing the power and performance trade off.
- Also, the Optimized CLA's static power is reduced drastically compared to normal CLA .so we can say that leakages in optimised CLA are reduced significantly.

Objective Achieved:

- 1) Successfully implemented 4-bit CLA using cadence (gdk 45 library).
- 2) Successfully implemented optimized 4-bit CLA in cadence (gdk 45 library), using Mtcmos technology.
- 3) Comparing power of both CLA, static power is reduced in optimized CLA.

References and bibliography:

- [1] Ch.Dayal sagar, T.Krishna moorti, "Design of low power flip- flop using MTCMOS Techniques"
International journal of computer application
and information technology Vol.1, No.1, July
2012
- [2] Hematha S , Dhawan A and Kar H , "Multithreshold CMOS Design for low power digital circuits" ,TENCON 2008-2008 IEEE Region 10 Conference,pp.1-5,2008.
- [3] K. Roy, S. Mukhopadhyay , and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometerCMOS circuits, "Proc. IEEE, vol.91, no. 2,pp. 305-327, Feb. 2003
- [4] Pawar Chander, Pokala Santhosh, Prasad Kurhe, "VLSI DESIGN OF FULL SUBTRACTOR USING MULTI-THRESHOLD CMOS TO REDUCE LEAKAGE CURRENT AND GROUND BOUNCE NOISE", ISSN, Volume-2, Issue-2, 2015.