

Brief Report

Analysis of CMOS Technology

Content:

- **Tool : Synopsys HSPICE 2016**
- **Transfer and Output Characteristics (DC Analysis)**
- **Rise Time and Fall Time Analysis (AC Analysis)**
- **Analysis with Temperature Variation (Current Variation across channel)**
- **16nm low power**
- **22 nm – Low, high power & bulk**
- **32 nm – Low, high power & bulk**
- **45 nm – Low, high power & bulk**
- **Model cards from Berkeley University**

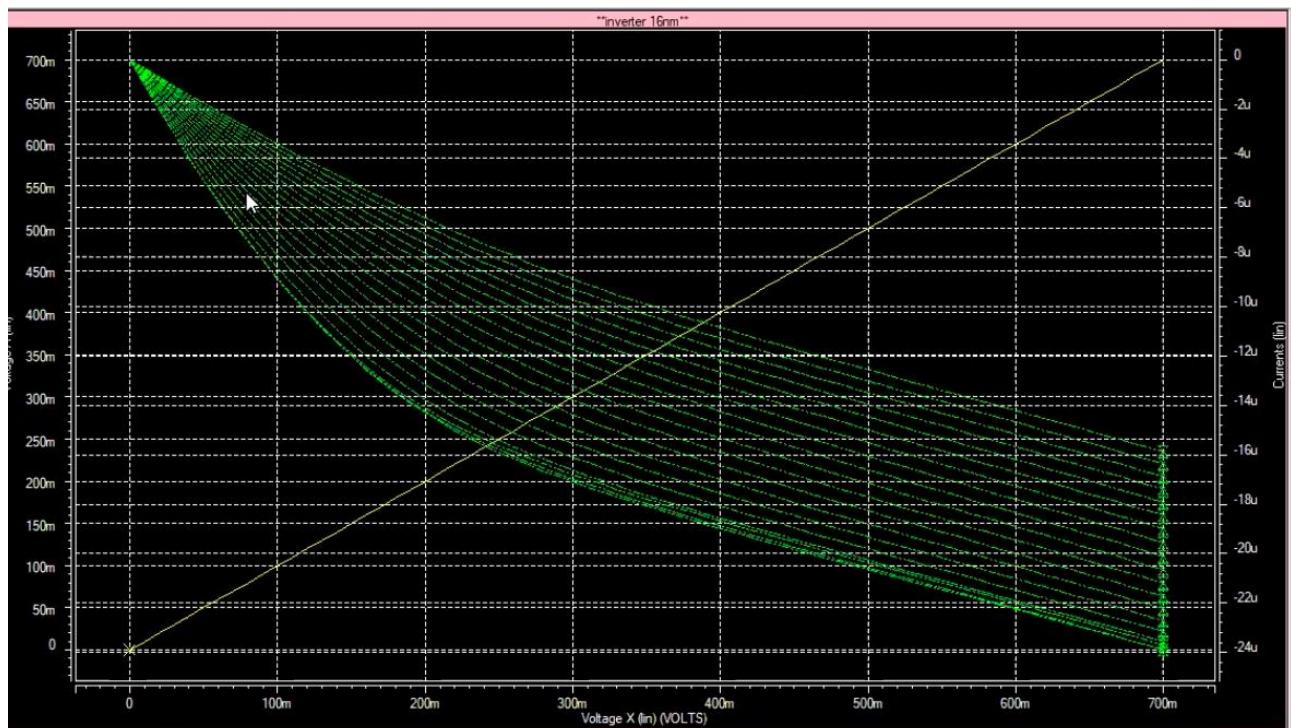
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Janki Vaya
Siddh Virani

Guided By:
Prof. Marmik Soni

16 hp(high power) nm model analysis

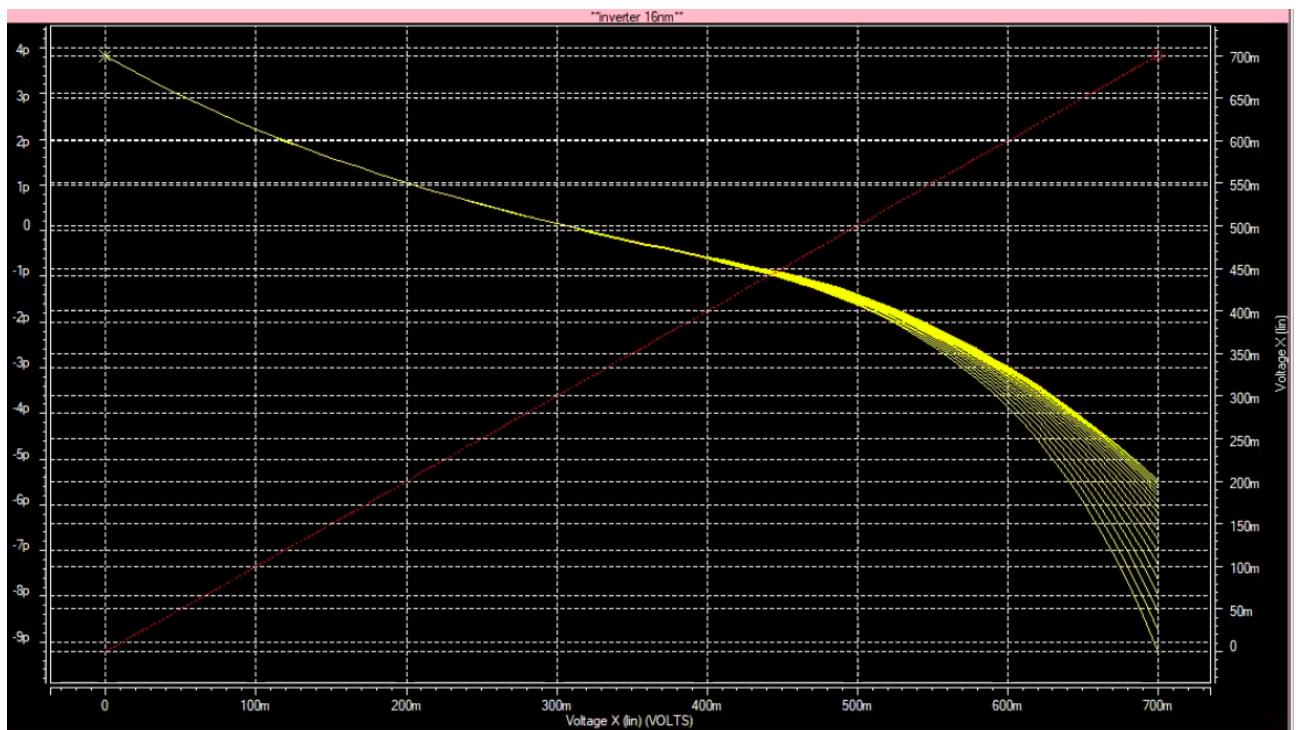
- High k
- Strained silicon
- $V_{th}(nmos) = 0.47965$, $V_{th}(pmos) = -0.43121$
- Biasing voltage=0.7 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=16nm, w=16nm
- pmos l=16nm, w=32nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis



1) V_{ds} vs I_{ds}

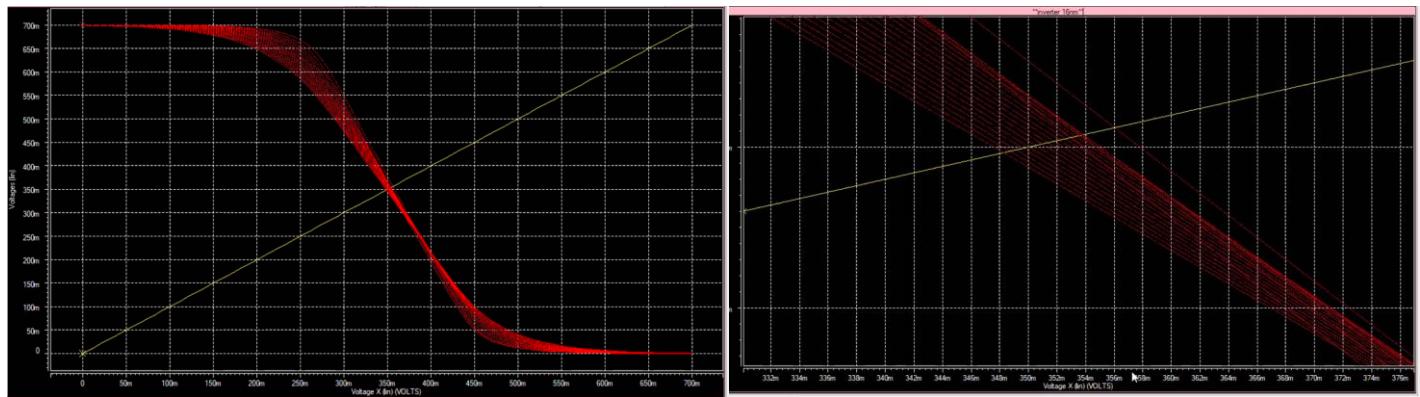
this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.



2) V_{gs} vs I_{ds}

this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

3) Voltage transfer characteristics

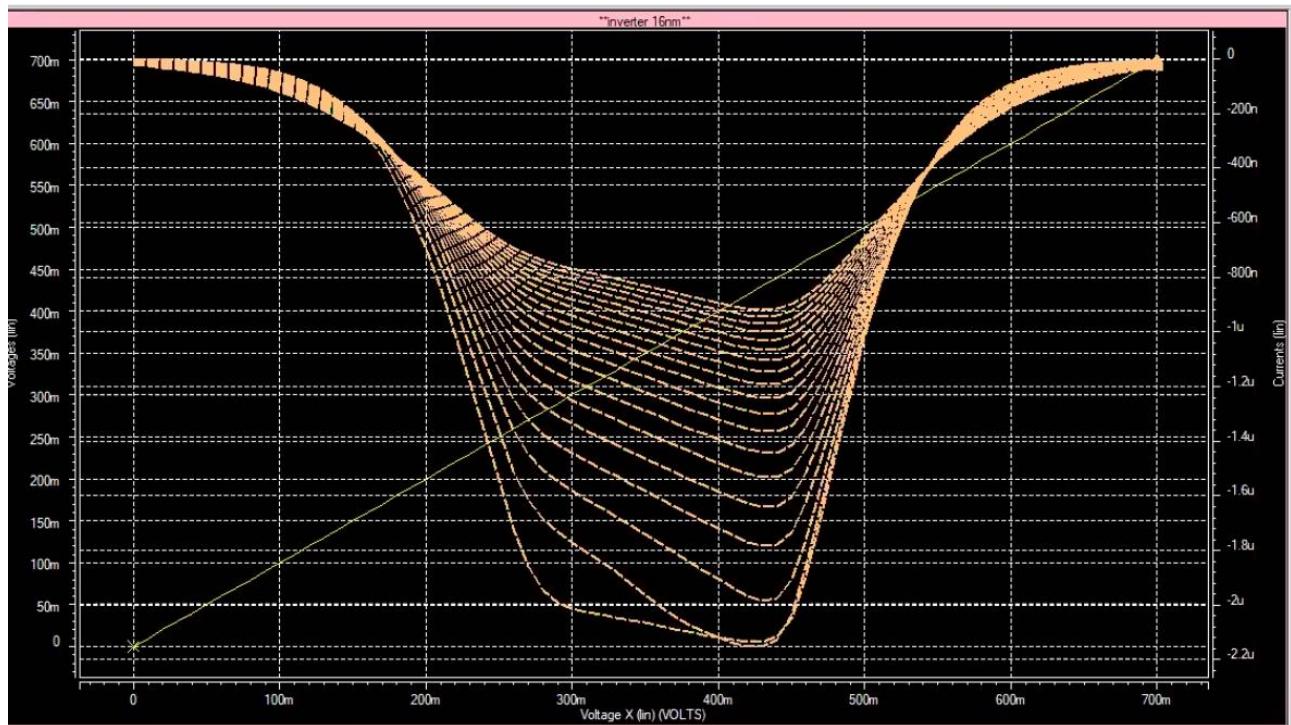


This graphs shows the variation in midpoint voltage because of temp.

At -55 C = 0.356 v

At 125 C = 0.348 v

Midpoint current



This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

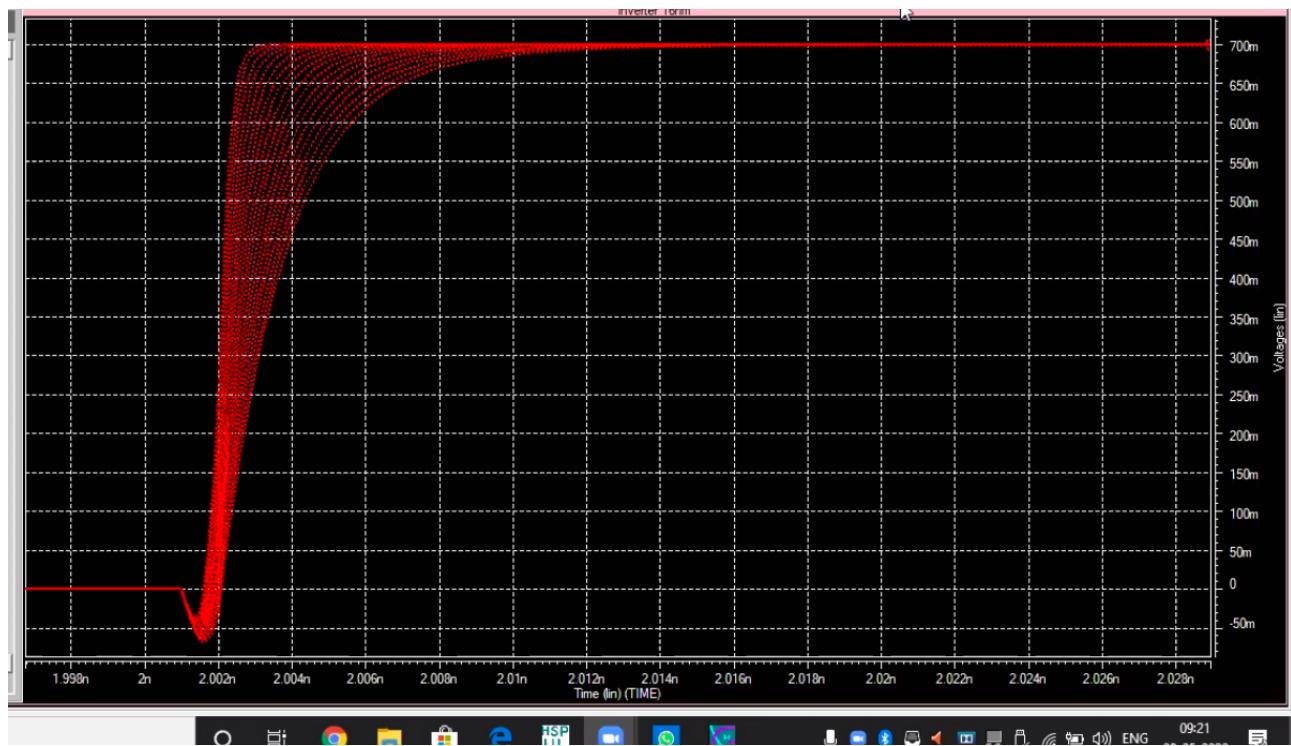
At -55 C = 2.13 uA

At 25 C = 1.29 uA

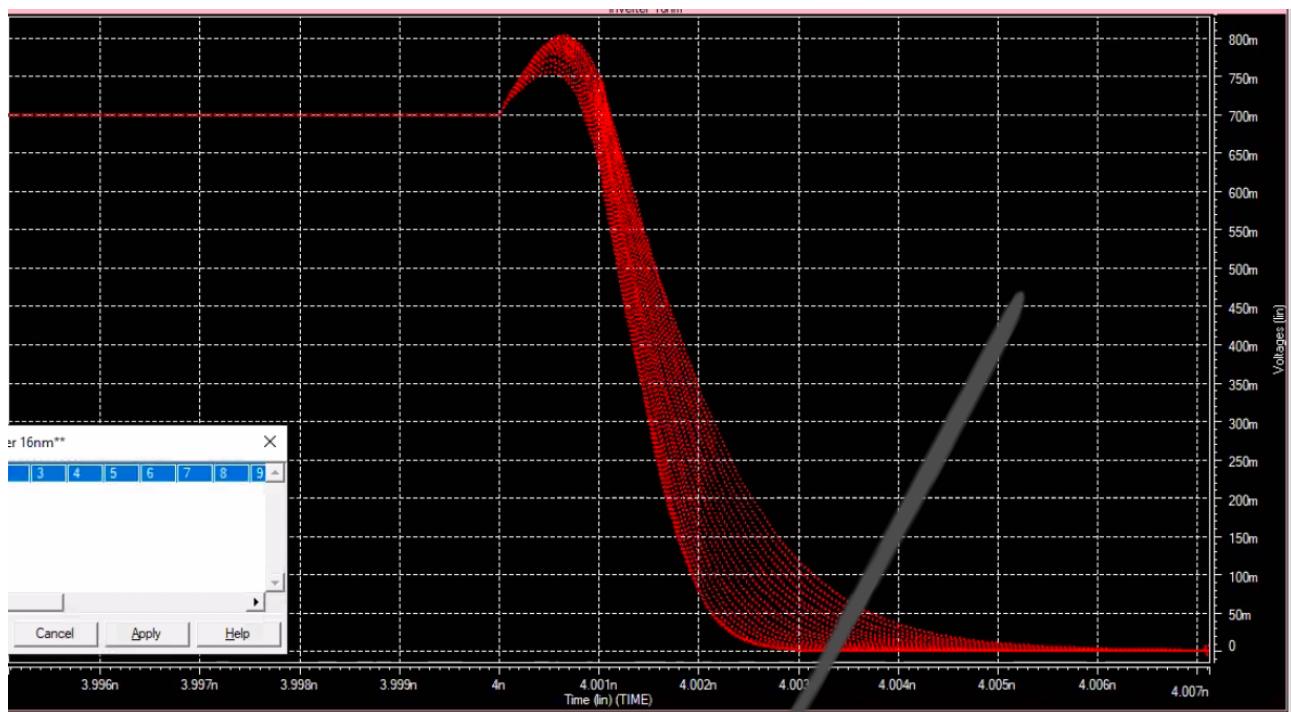
At 125 C = 0.915 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows

graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise time at 125 C

In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

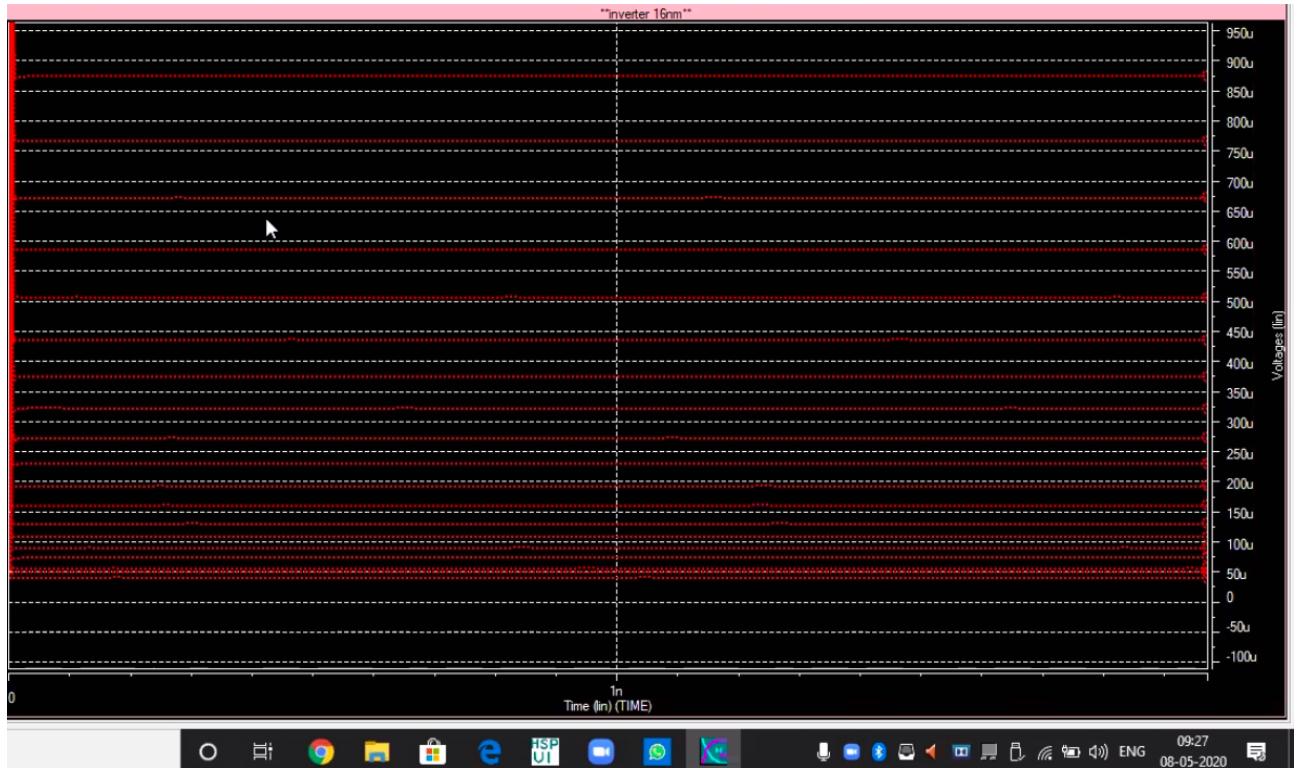
Temperature	Rise time	Fall time
-55 c	0.0025 ns	0.0035 ns
25 c	0.007 ns	0.0045 ns
125 c	0.015 ns	0.007 ns

Logic values at different temp.

Temperature	High logic	Low logic
-55 c	0.6995 v	40 uV
25 c	0.6993 v	192 uV
125 c	0.699 V	875 uV

Noise margins ,at stable high voltage and low voltage

From this graph we can say that there is no continuous stable high and low logic levels

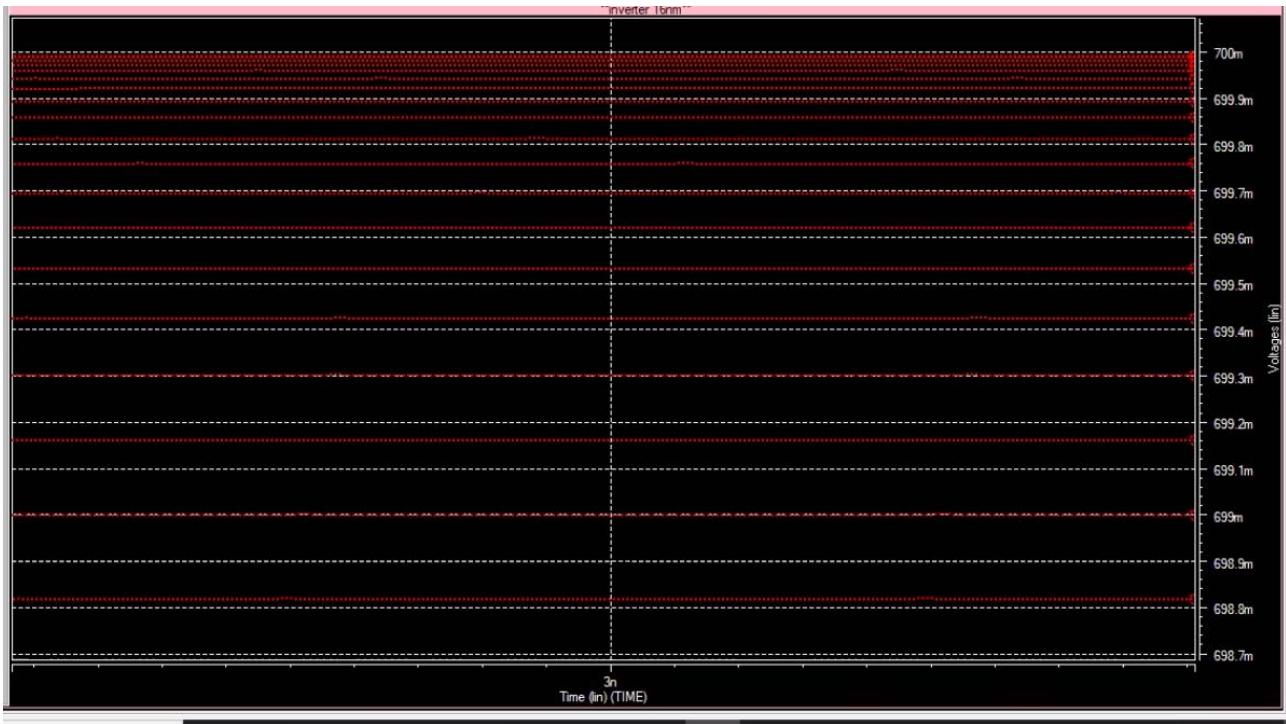


5) Current analysis of inverter

Temperature	leakage current
-55 °C	18.7 nA
25 °C	36.6 nA
125 °C	59.4 nA

Charging and discharging current (input time period is 4ns)

Temperature	Charging current	Discharging current
-55 °C	33 uA	18.5 uA
25 °C	25 uA	13.1 uA
125 °C	21 uA	12.8 uA



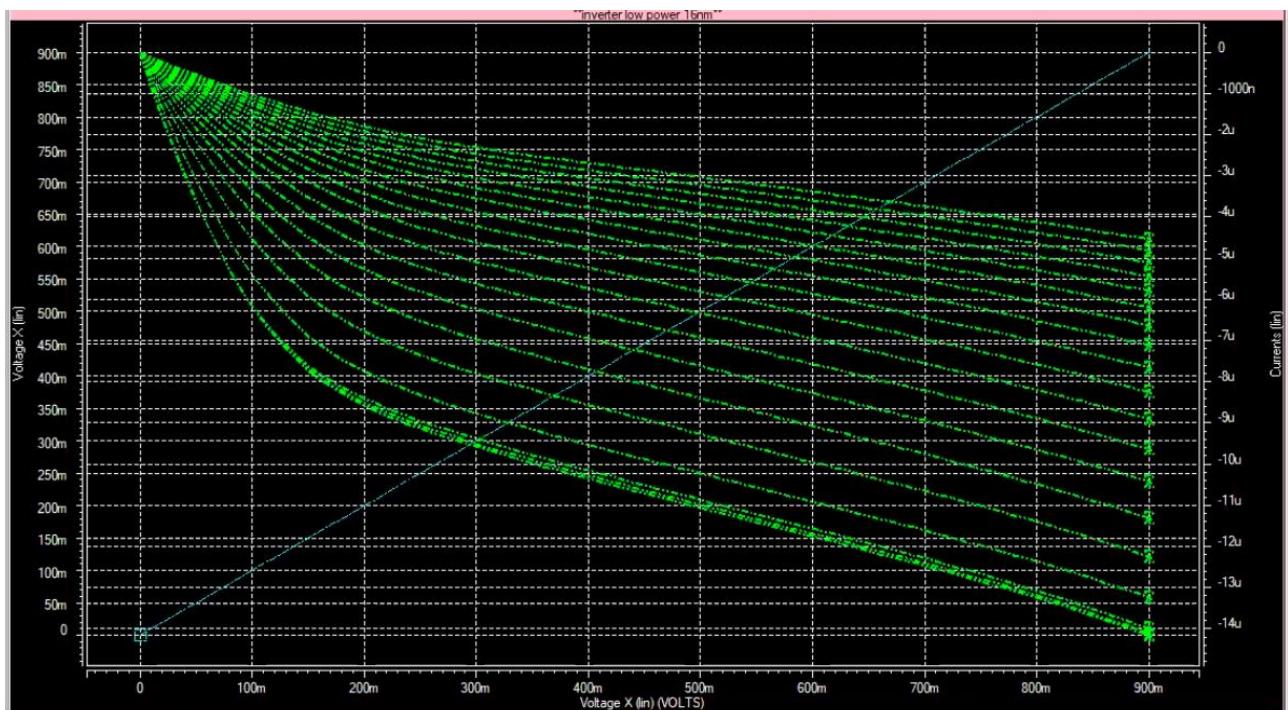
Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

16 lp(low power) nm model analysis

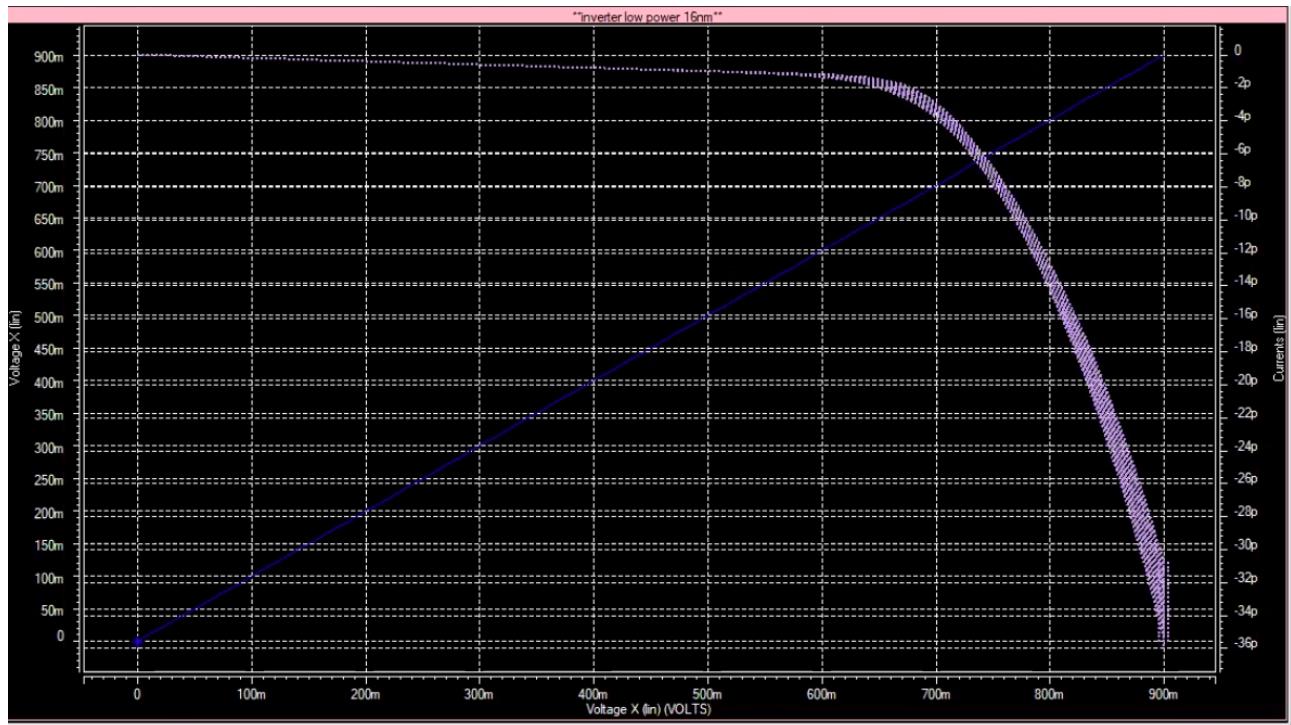
- High k
- Strained silicon, metal gate
- $V_{th}(nmos) = 0.68191$, $V_{th}(pmos) = -0.6862$
- Biasing voltage=0.9 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=16nm, w=16nm
- pmos l=16nm, w=32nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis

1) Vds vs Ids



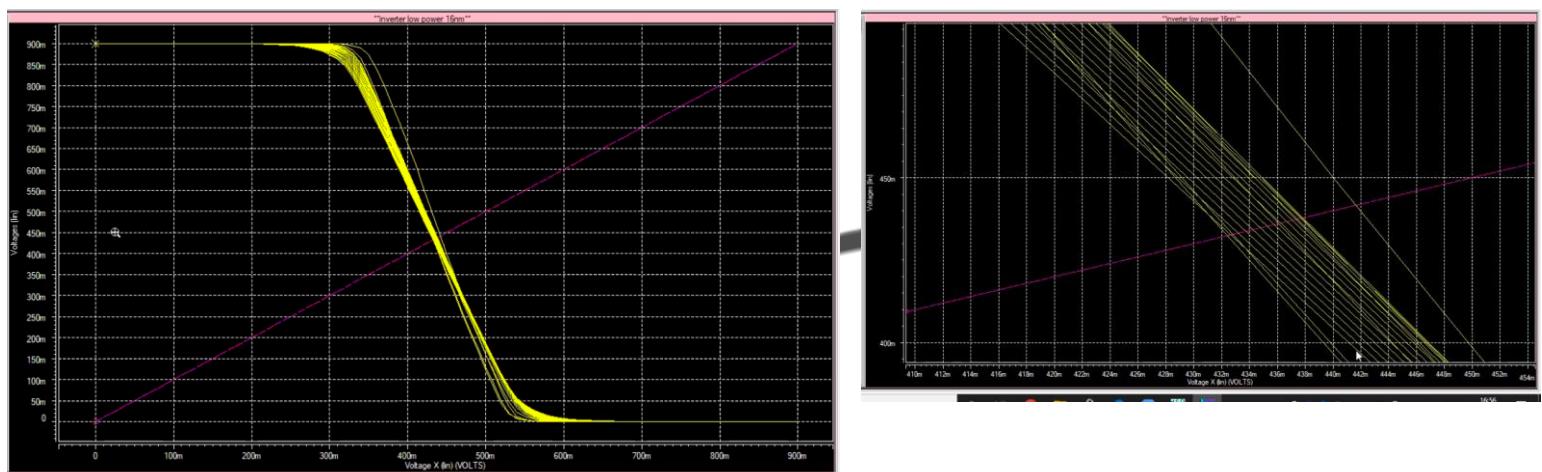
this shows the graph at -55 centigrade. As temperature increase the current will decrease



2) Vgs vs Ids

this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

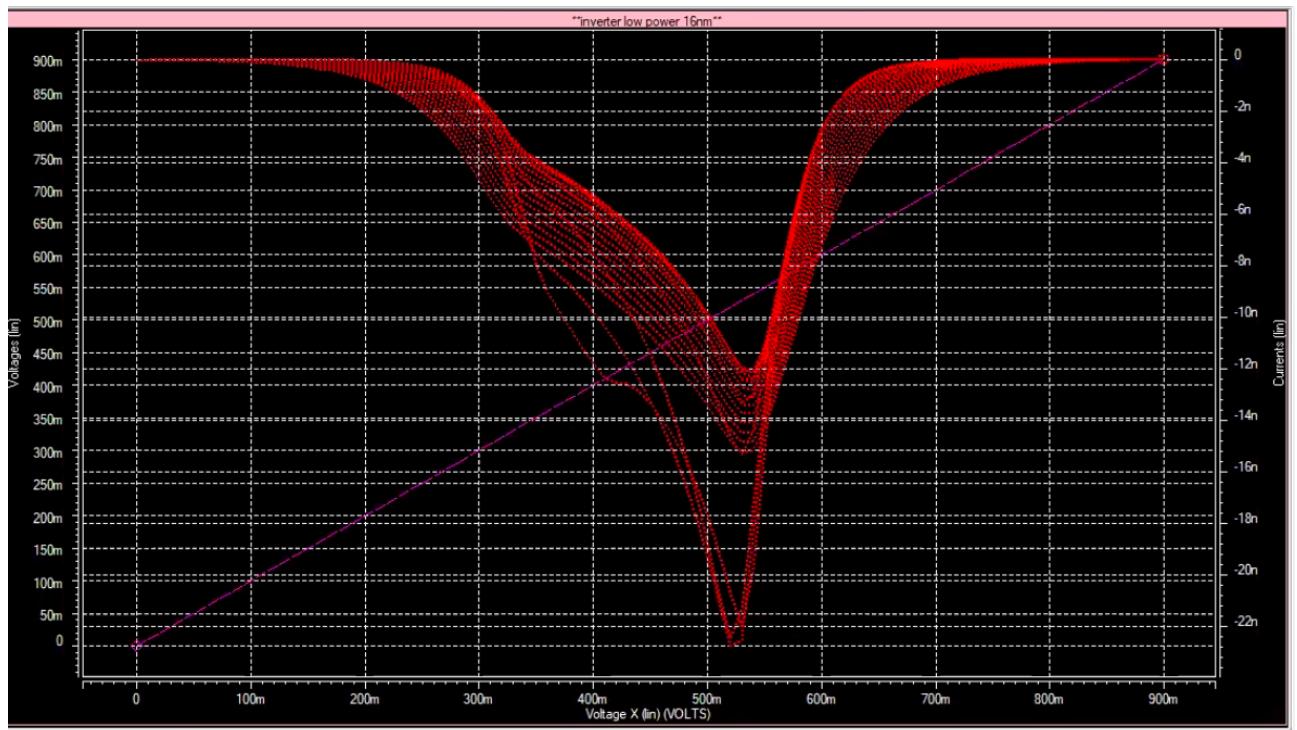
3) Voltage transfer characteristics



This graphs shows the variation in midpoint voltage because of temp.

At -55 C = 0.441 v

At 125 C = 0.432 v



Midpoint current

This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

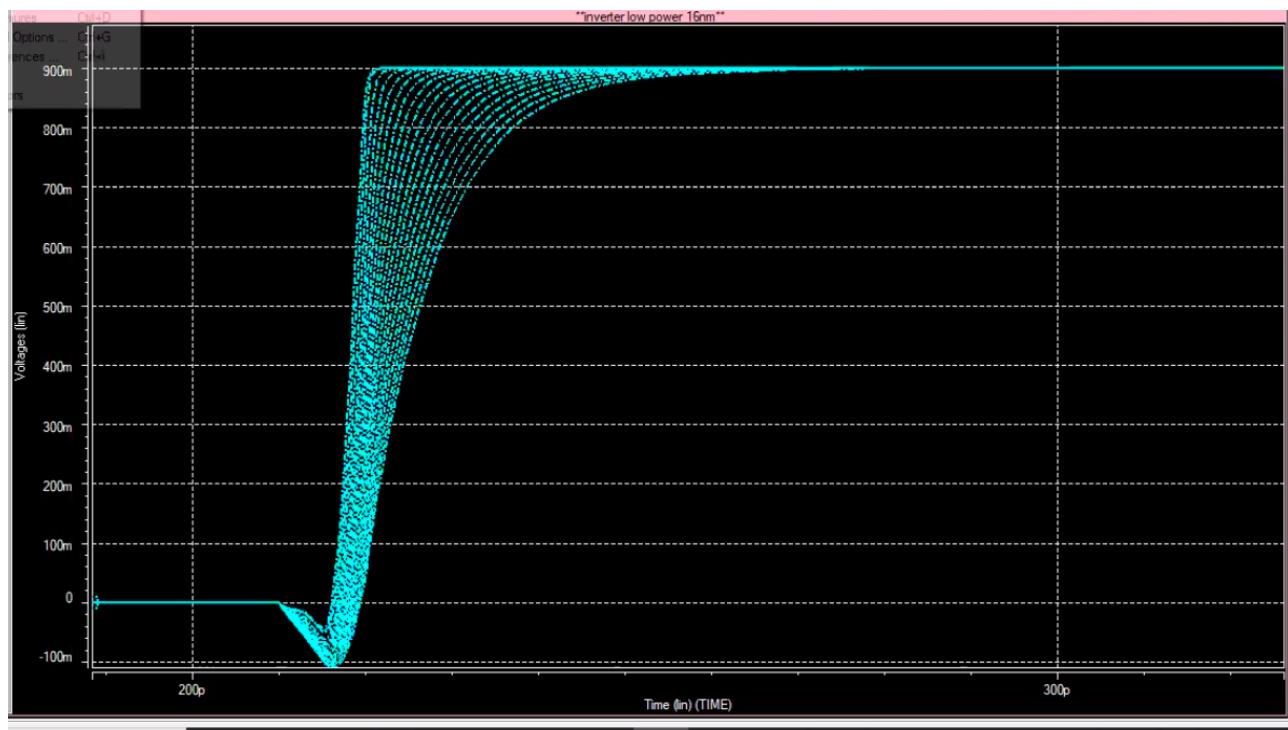
At -55 C = 22.8 nA

At 25 C = 12.8 nA

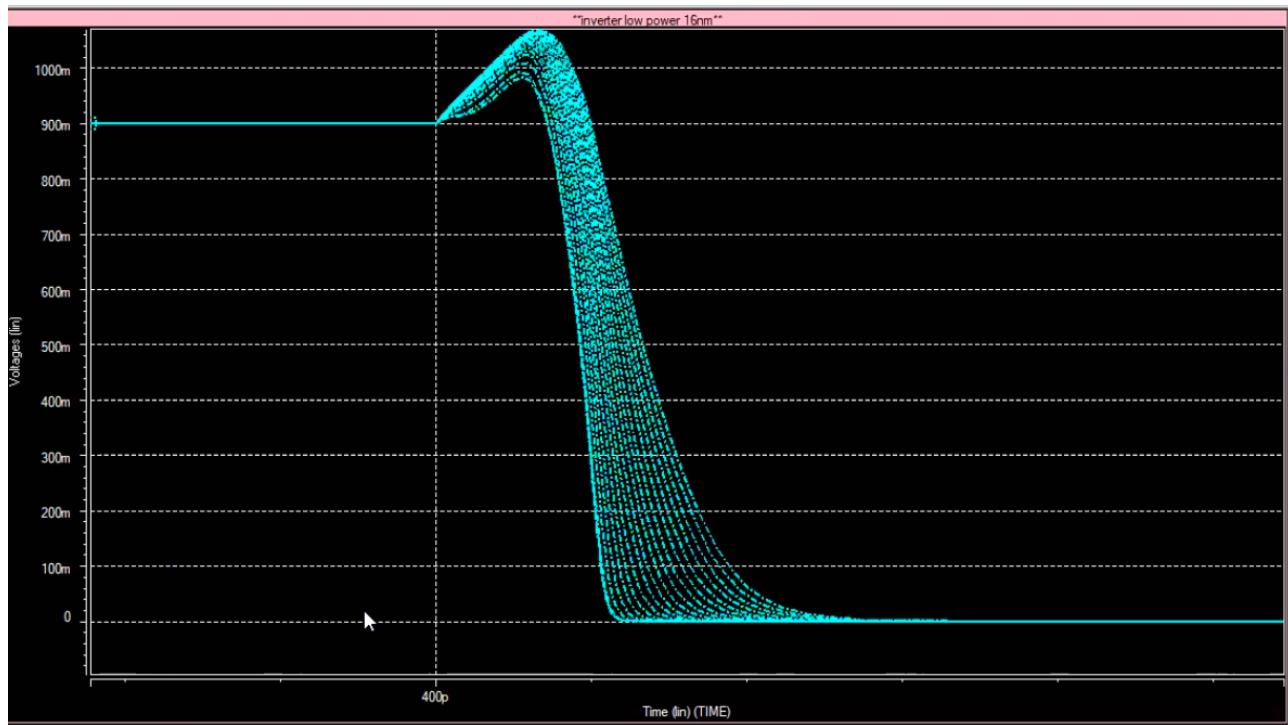
At 125 C = 15.2 nA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise tome at 125 C

In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 c	13 ps	12 ps
25 c	27 ps	17 ps
125 c	76 ps	28 ps

Logic values at different temp

In this model there is steady voltages.Low logic voltage is in range of -2 to 6 uv.

5) Current analysis of inverter

Temperature	leakage current
-55 c	15.3 nA
25 c	7.23 nA
125 c	4.26 nA

Charging and discharging current (input time period is 4ns)

Temperature	Charging current	Discharging current
-55 c	6.98 uA	2.49 uA
25 c	5.5 uA	1.94 uA
125 c	3.84 uA	1.83 uA

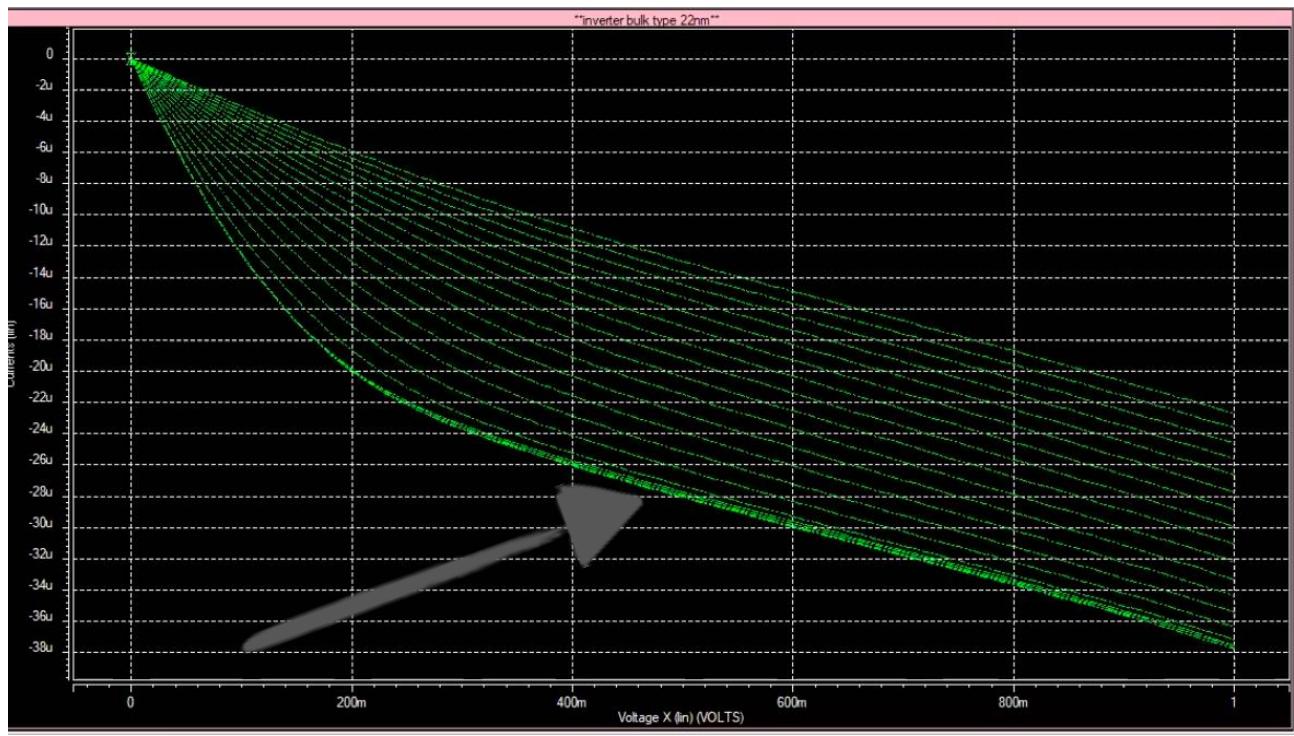
Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

22 nm technology(bulk)

- $V_{th0}(nmos) = 0.51$, $V_{th0}(pmos) = -0.372$
- Biasing voltage=1 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=22nm, w=22nm
- pmos l=22nm, w=44nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis

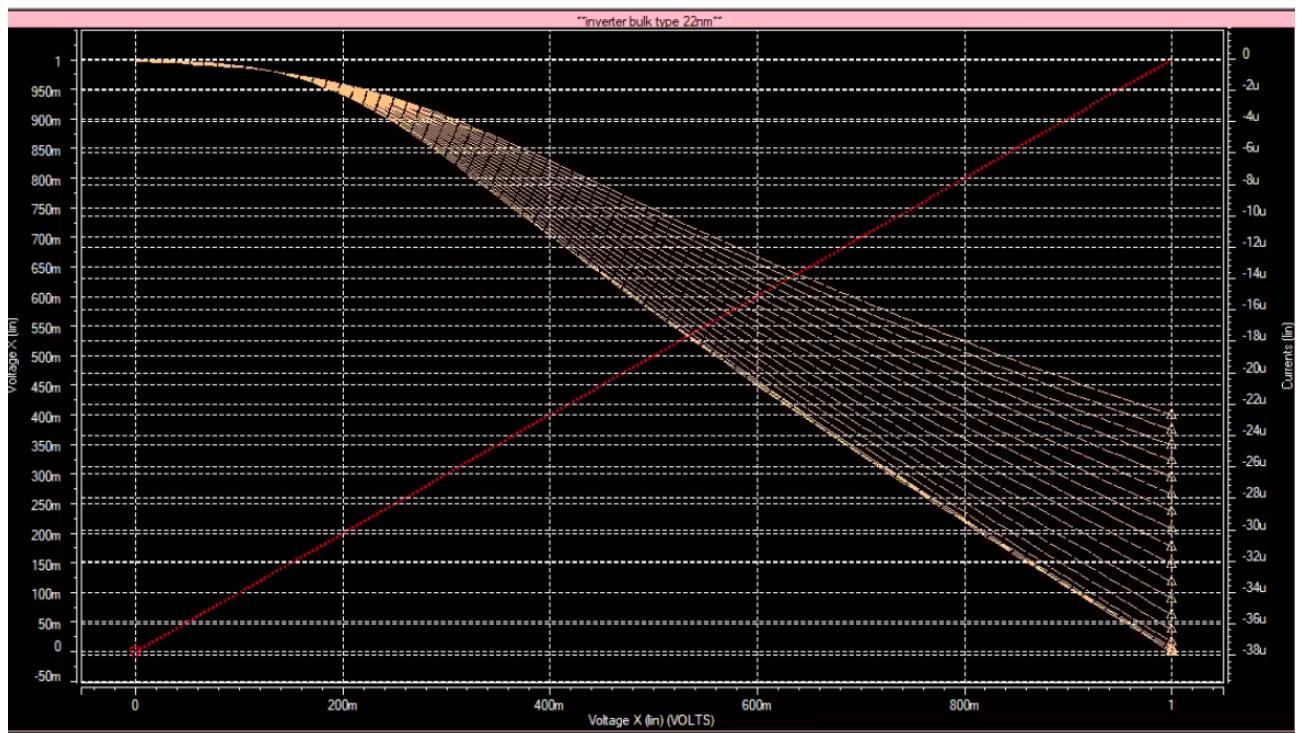
1) V_{ds} vs I_{ds}



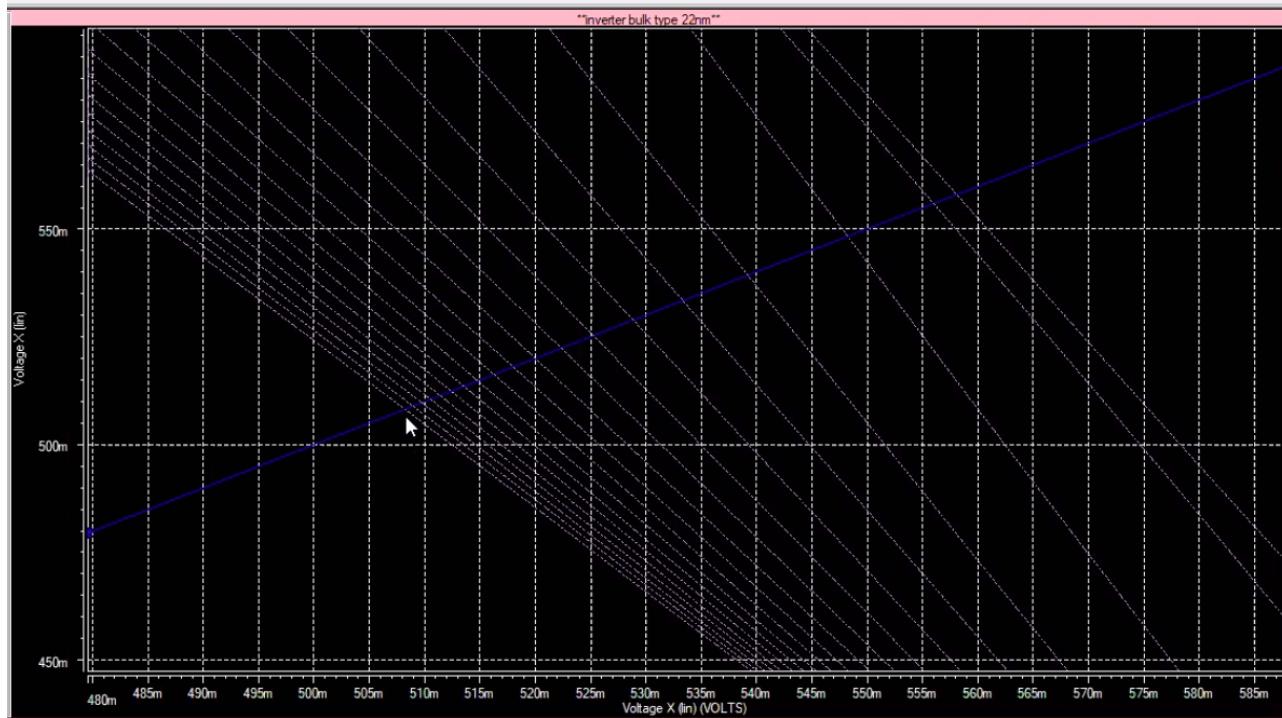
arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

Here at 125 c temp characteristics is no proper.

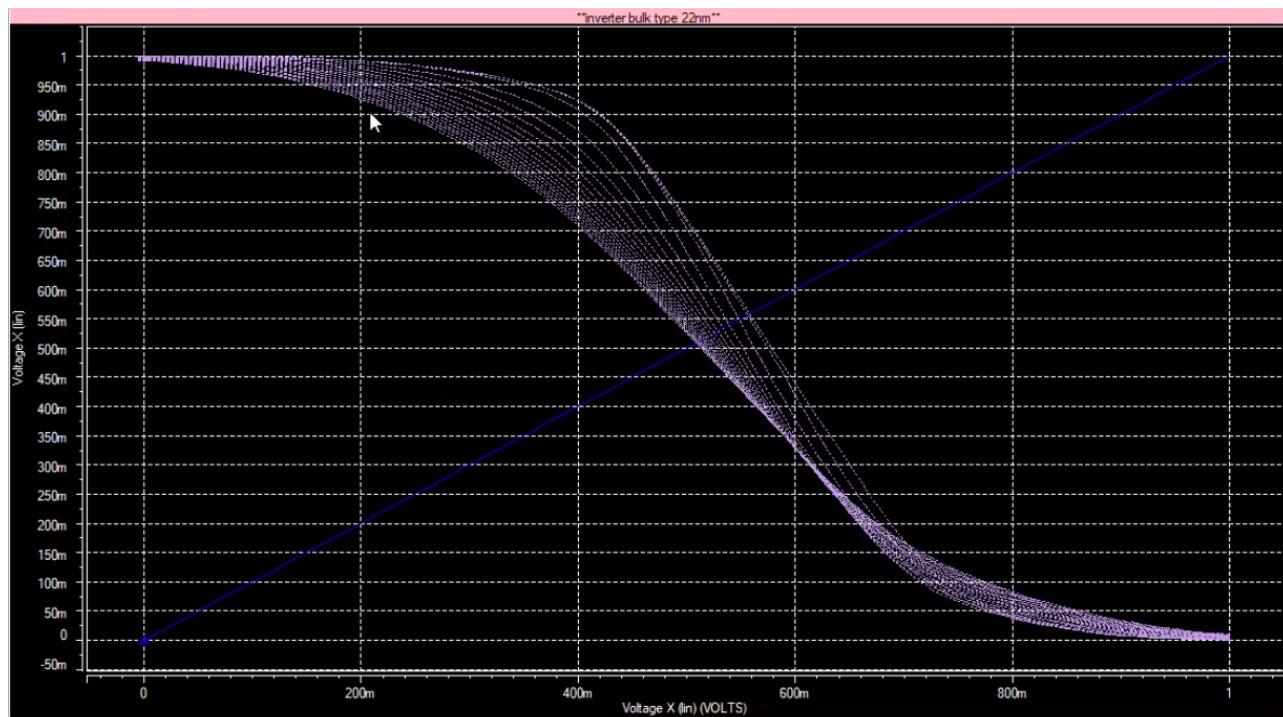
2) Ids vs Vgs



Here you can see in the graph the threshold voltage is very low in comparison with the theoretical value which is mentioned above and this is the first model in which we observed this kind of graph(doubt).



3) Voltage transfer characteristics



Arrow shows midpoint voltage at -55 c

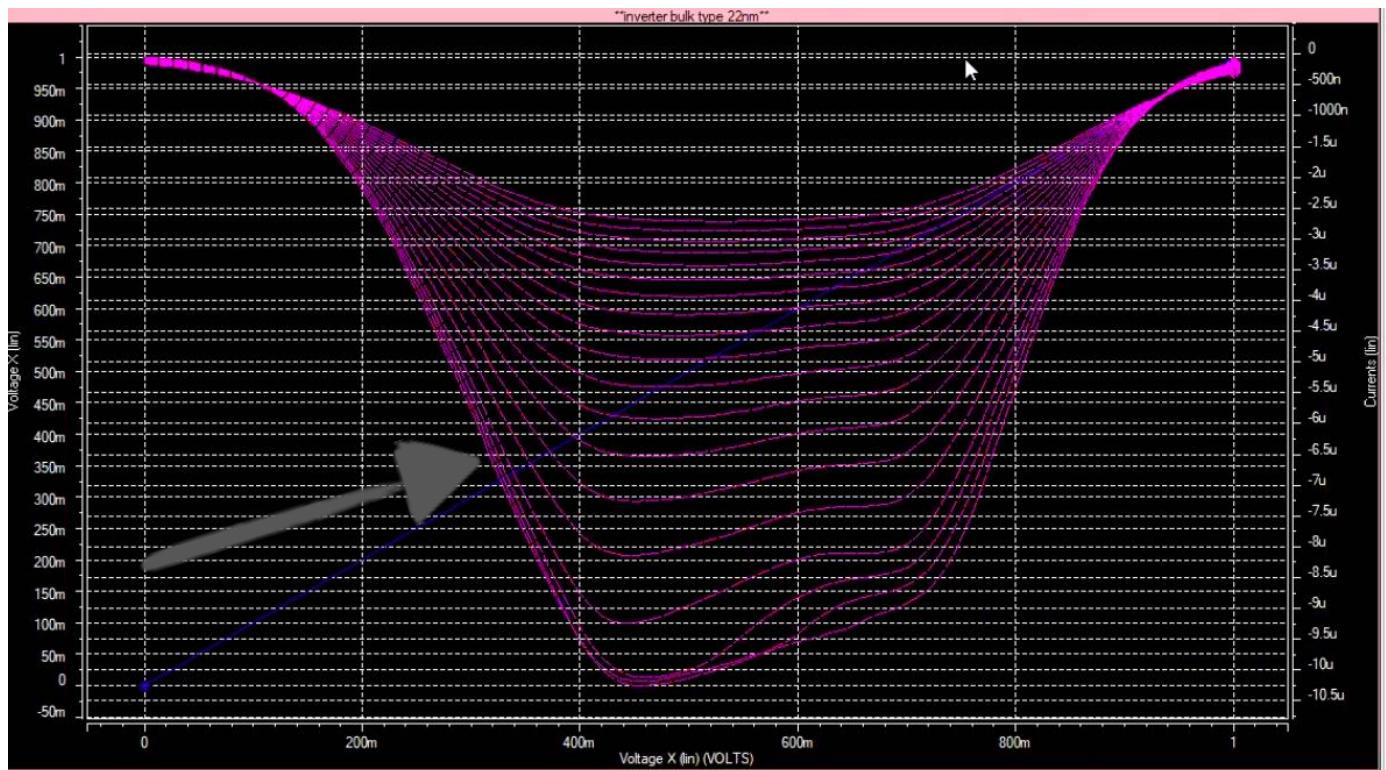
This graphs shows the variation in midpoint voltage because of temp.

Less effect of positive temp.

At -55 C =0.557 v

At 125 C = 0.507 v

For the current, the model of the pmos it is very sensitive to temperature compared to nmos, which you can observe from VTC curve .same is in vtc curve also



This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

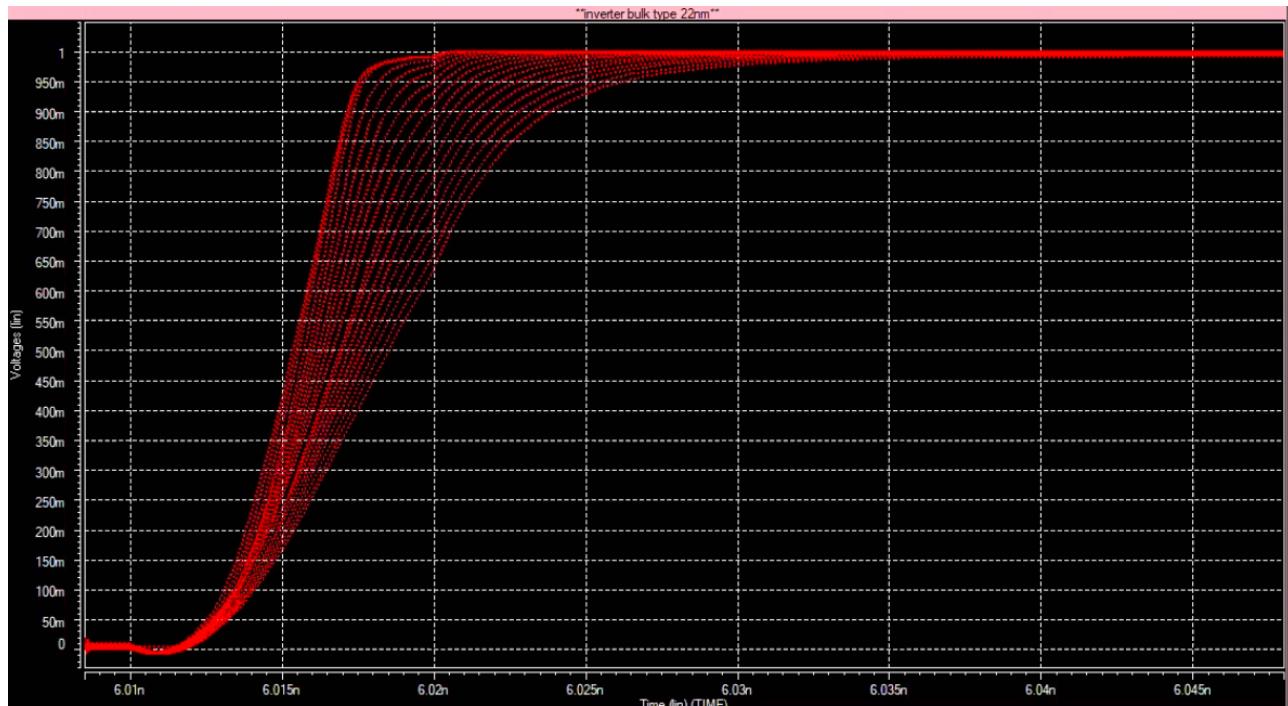
At -55 C = 10.25 uA

At 25 C = 6.98 uA

At 125 C = 2.57 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis

Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature.

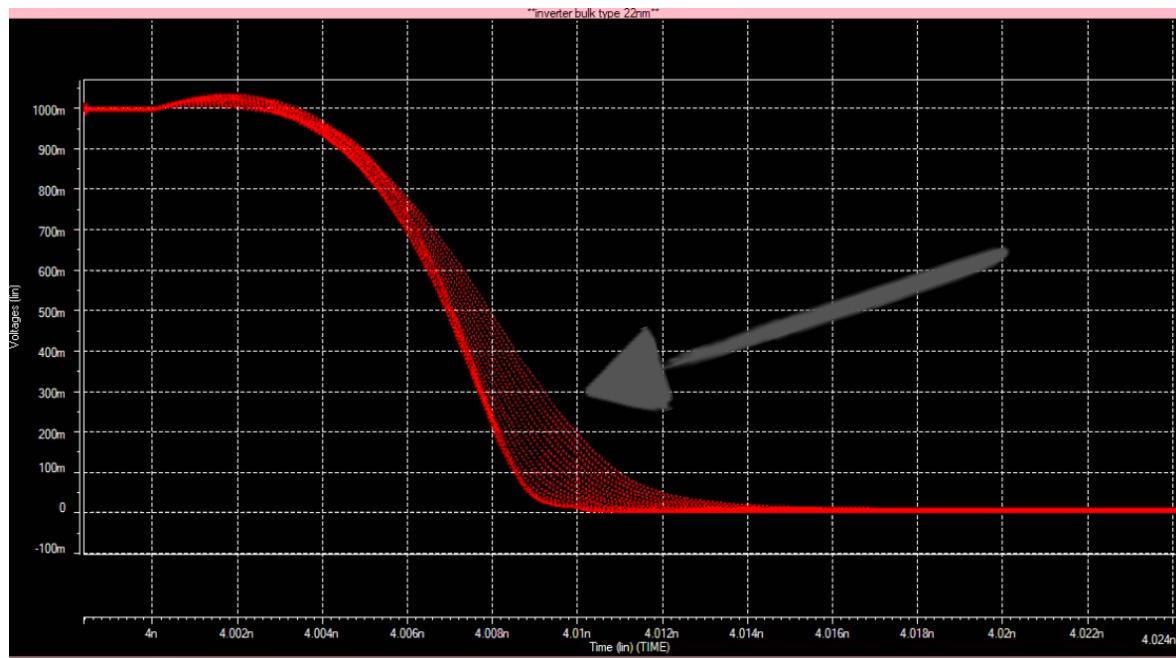
In the graph of rise time and fall with temperature increasing.

Here we have observed that the strained silicon models

Arrow shows graph of rise tome at 125 C(below)

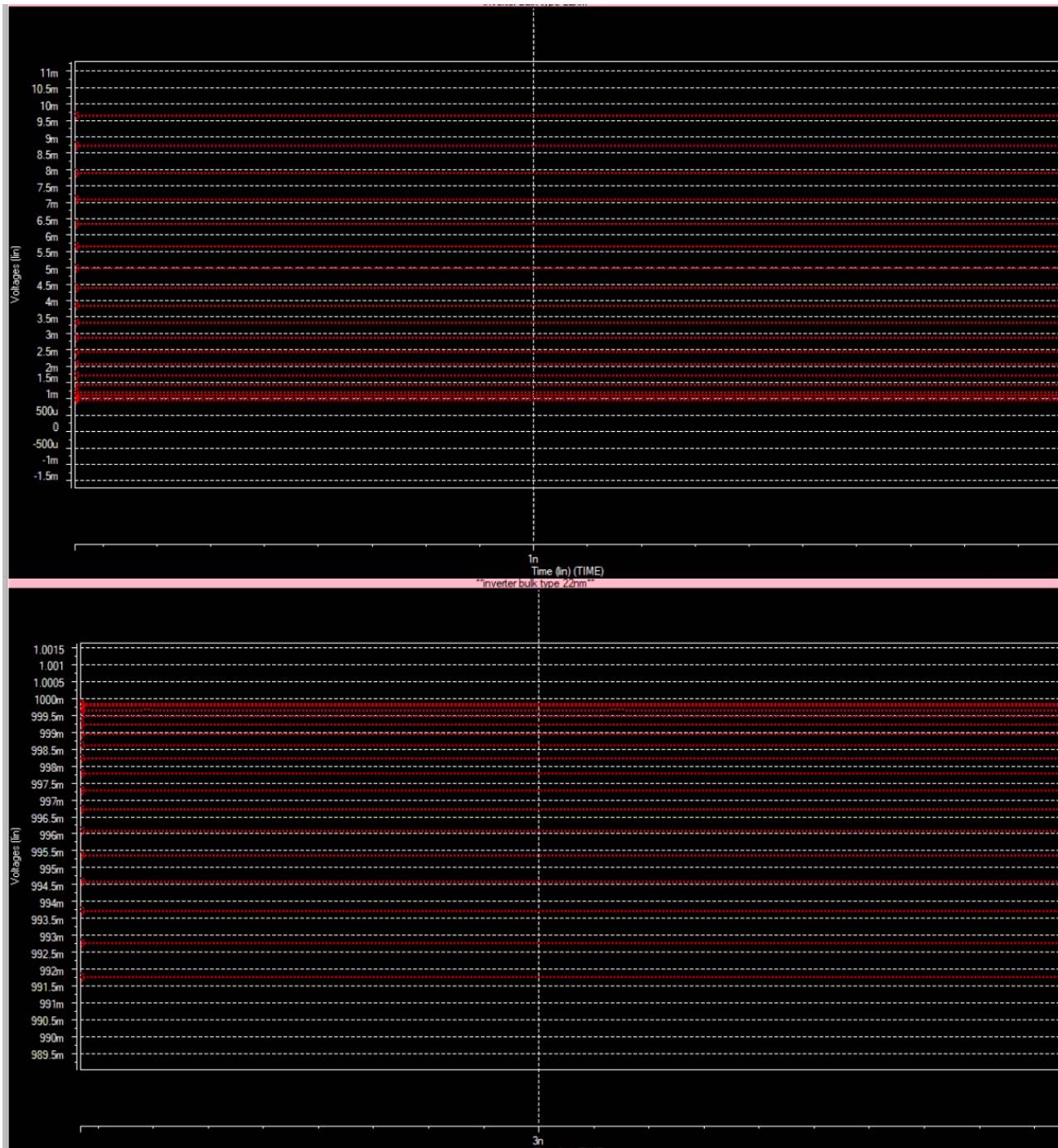
time we can see that here the overshoot is increasing

overshoot is very very less in comparison with the



Temperature	Rise time	Fall time
-55 °C	0.01 ns	0.001 ns
25 °C	0.015 ns	0.012 ns
125 °C	0.035 ns	0.016 ns

]

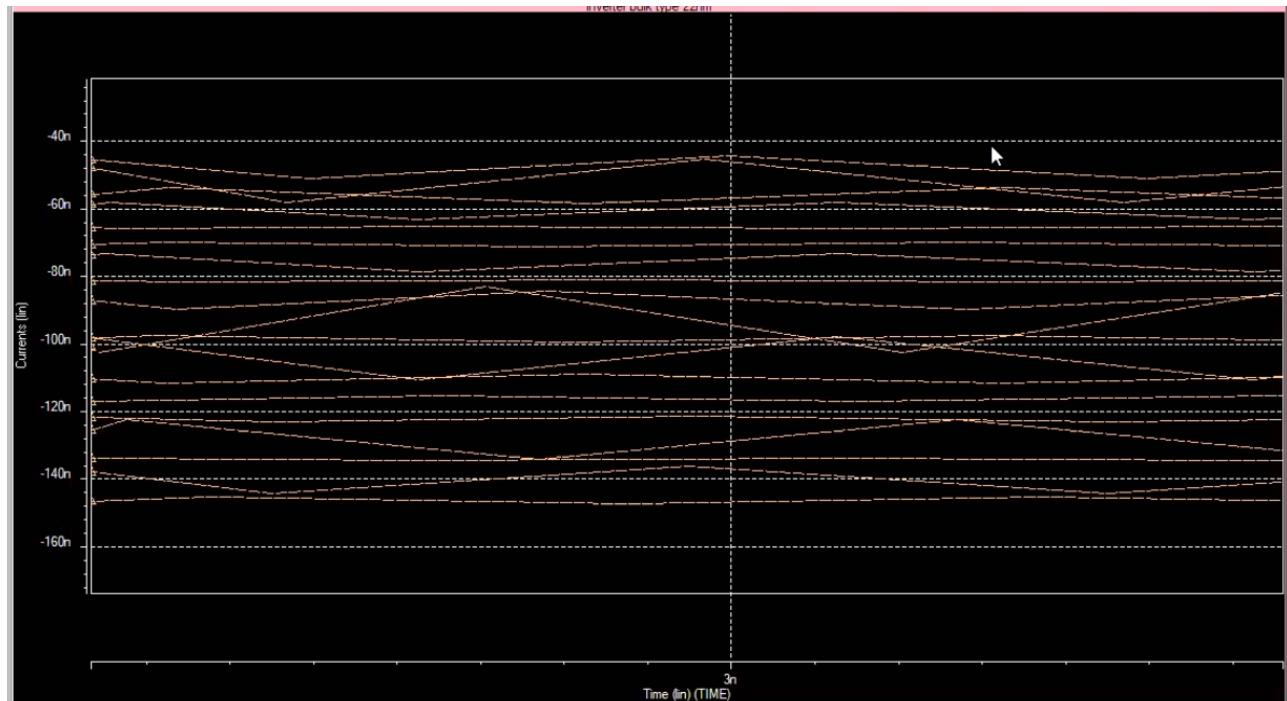


Logic values at different temp

Temperature	High logic	Low logic
-55 c	1 v	1 mV
25 c	0.99825 v	3 mV

Temperature	High logic	Low logic
125 °C	0.99175 V	9.6 mV

5) Current analysis of inverter



Leakage current analysis

Temperature	leakage current
-55 °C	50 nA
25 °C	90 nA
125 °C	150 nA

6)

In this tables result is not proper(doubt)

Input frequency(4 ns)

Temperature	Discharging current	Charging current

Temperature	Discharging current	Charging current
-55 c	14.5 uA	3.91 uA
25 c	9.45 uA	3.93 uA
125 c	6.80 uA	3 uA

Input frequency (0.04 ns)

Temperature	Discharging current	Charging current
-55 c	280 uA	370 uA
25 c	270 uA	320 uA
125 c	280 uA	290 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

Here in this model frequency response of inverter is not proper.

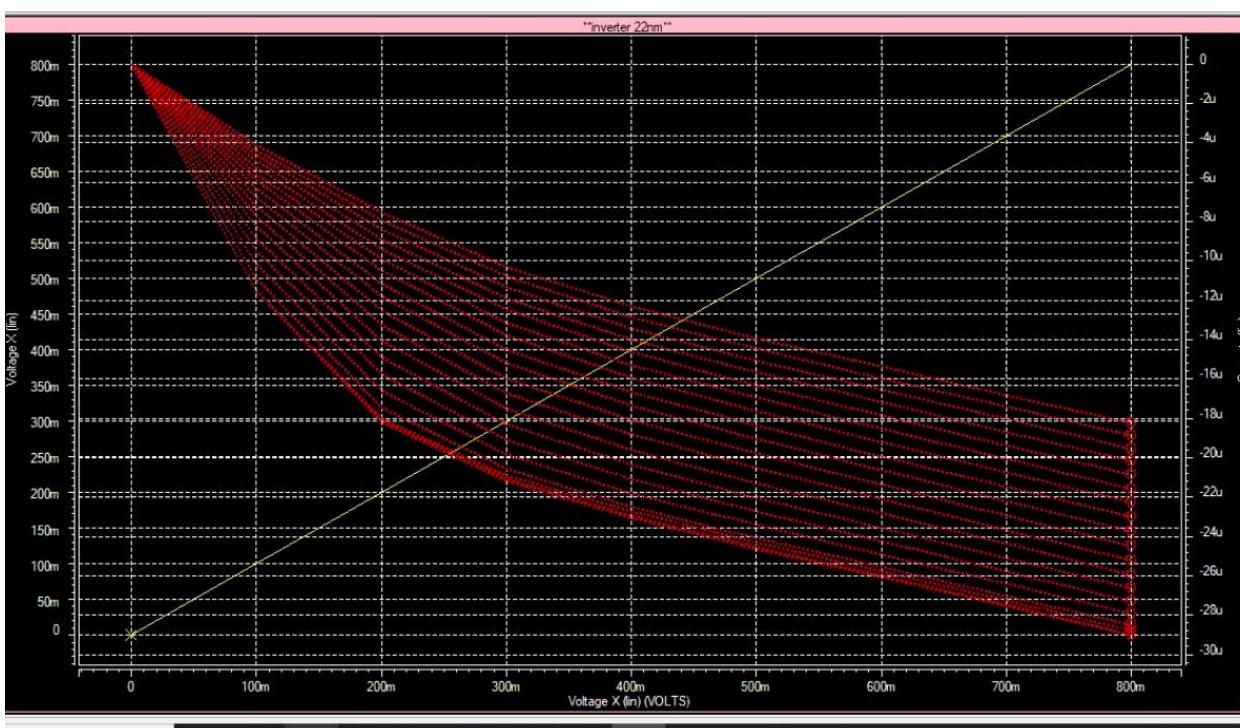
Ideally what should be that as frequency increase current should be increase but in this model we can't observe this result.

Here charging and discharging current should be decrease with the temp. Increase
But here it's not happened

22 hp(high power) nm model analysis

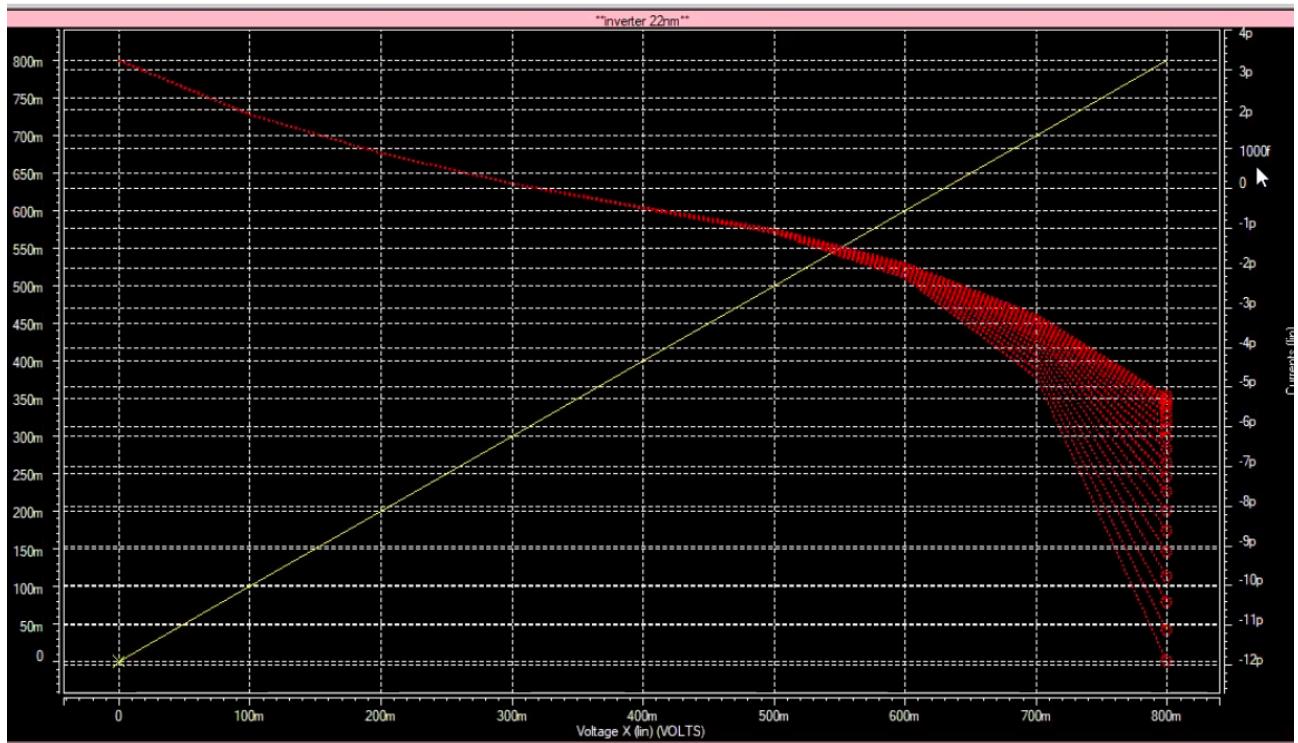
- High k
- Strained silicon
- $V_{th}(nmos) = 0.50308$, $V_{th}(pmos) = -0.49155$
- Biasing voltage=0.8 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=22nm, w=22nm
- pmos l=22nm, w=44nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis



1) V_{ds} vs I_{ds}

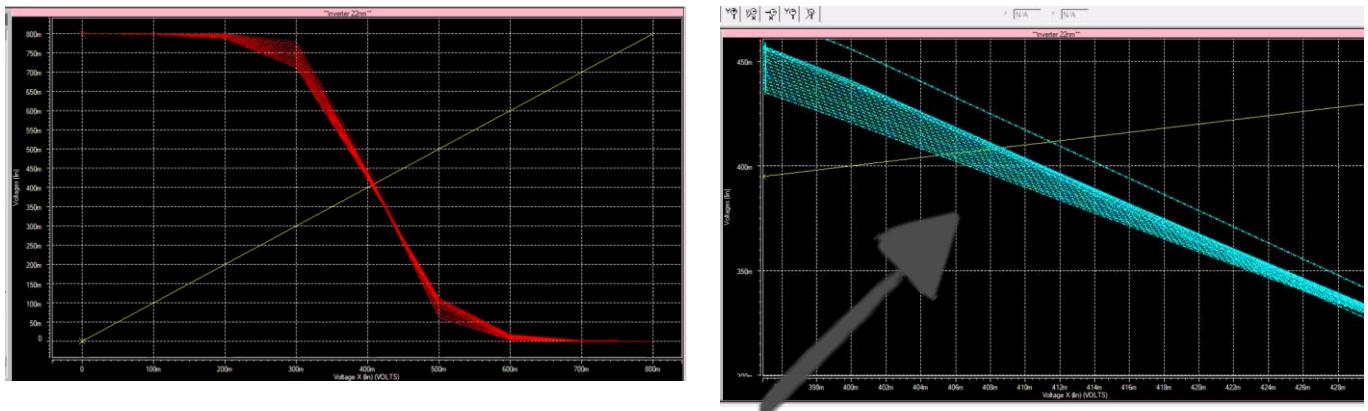
this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.



2) Vgs vs Ids

this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

3) Voltage transfer characteristics

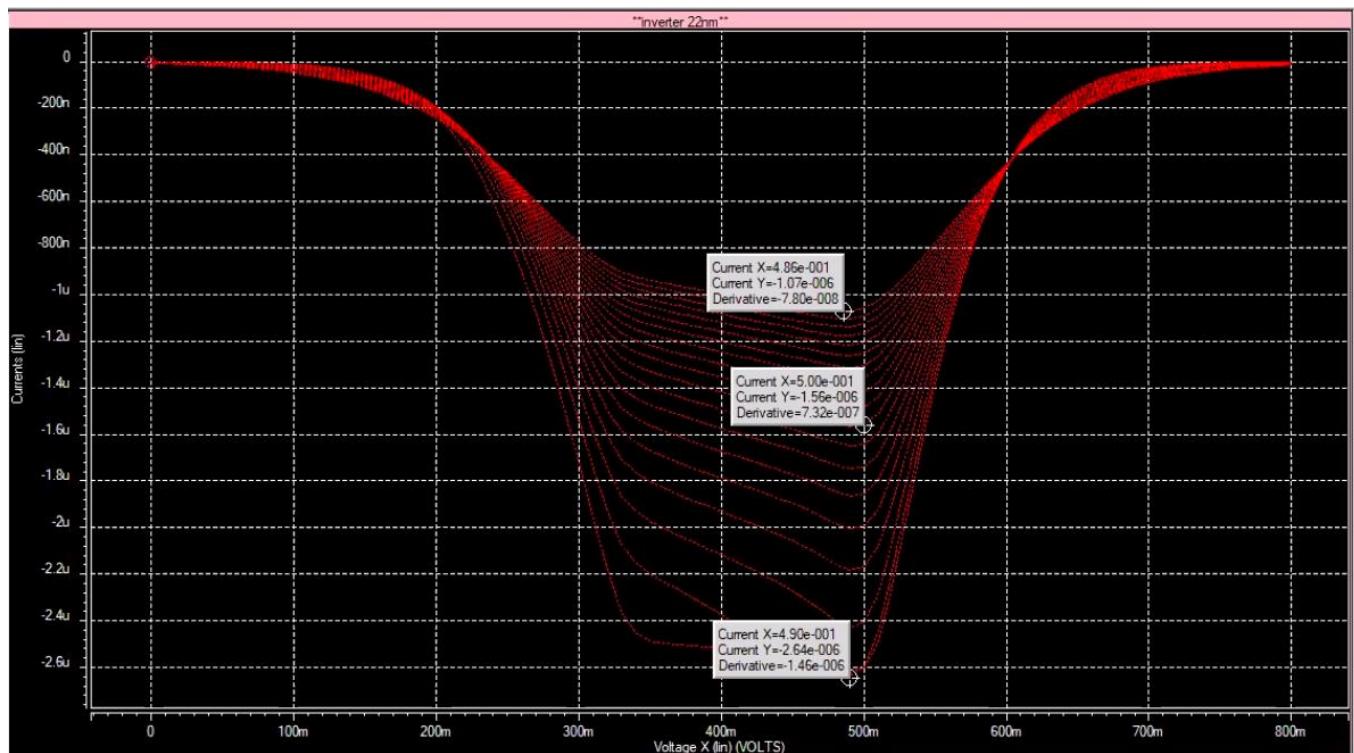


This graph shows the variation in midpoint voltage because of temp.

At -55 C = 0.412 v

At 125 C = 0.405 v

Midpoint current



This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

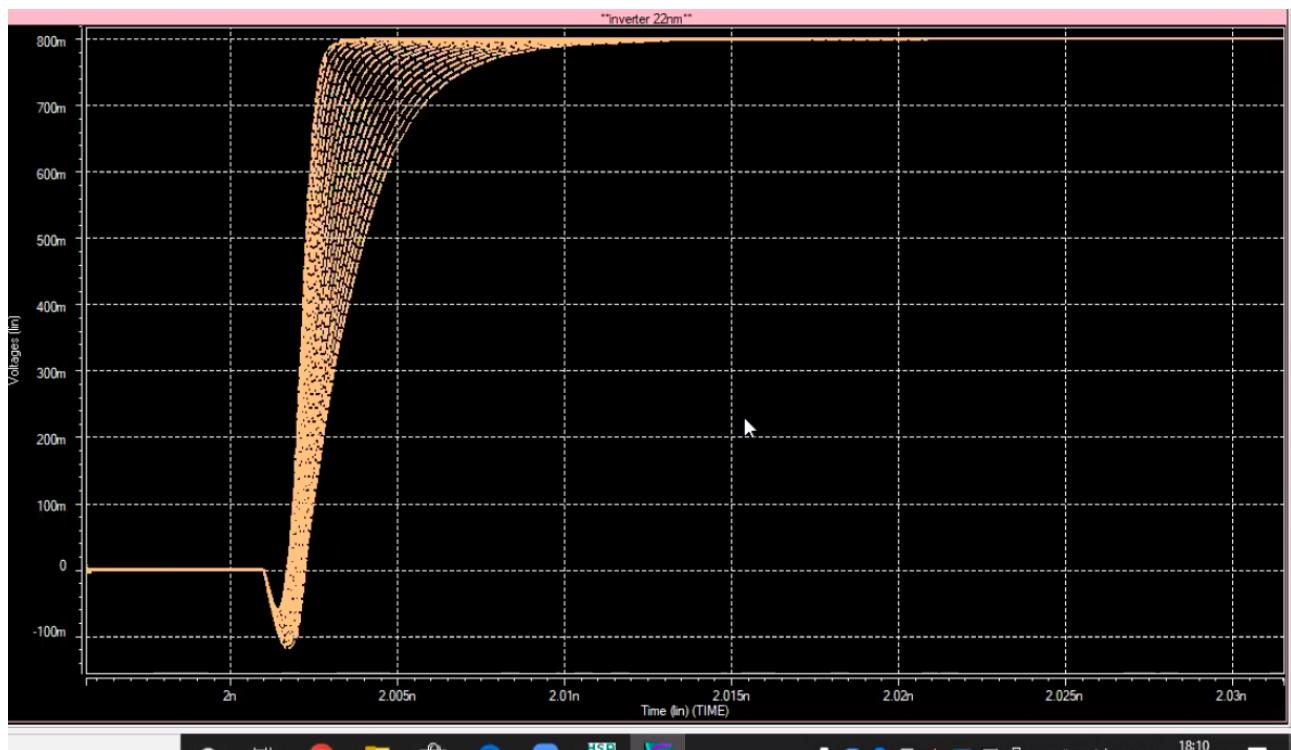
At -55 C = 2.64 uA

At 25 C = 1.55 uA

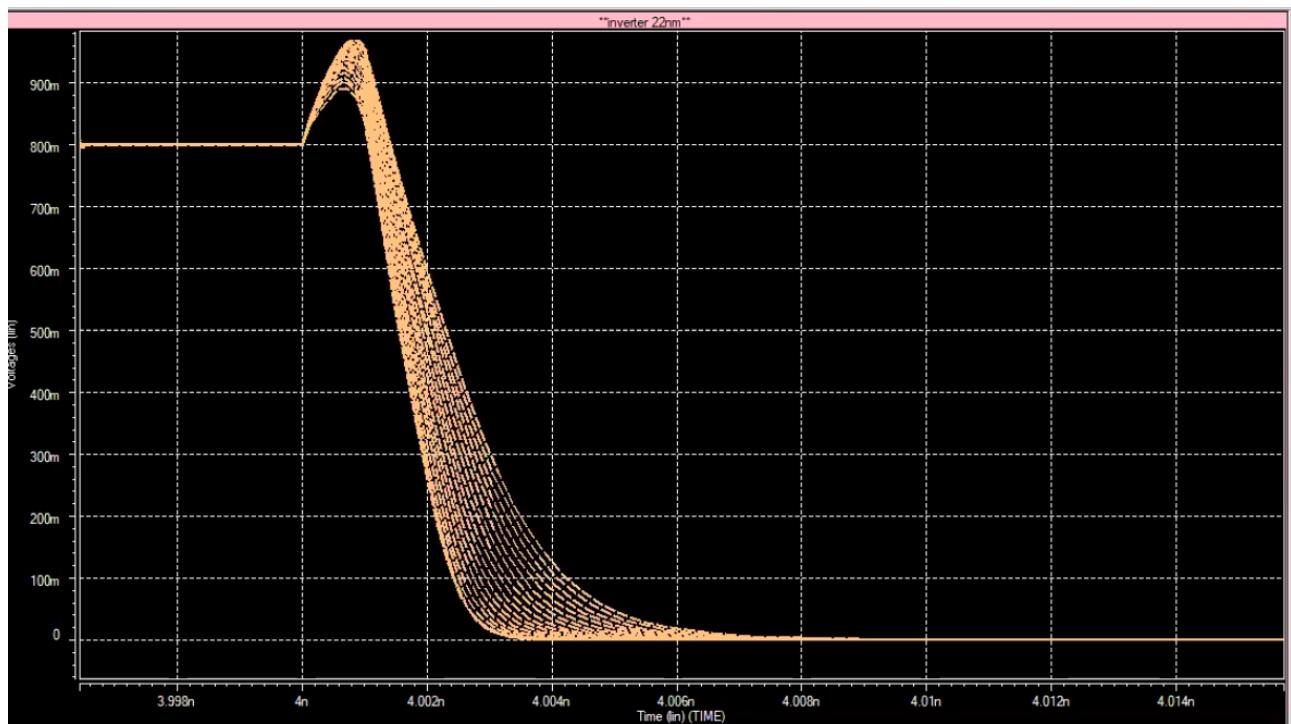
At 125 C = 1.07 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise time at 125 C

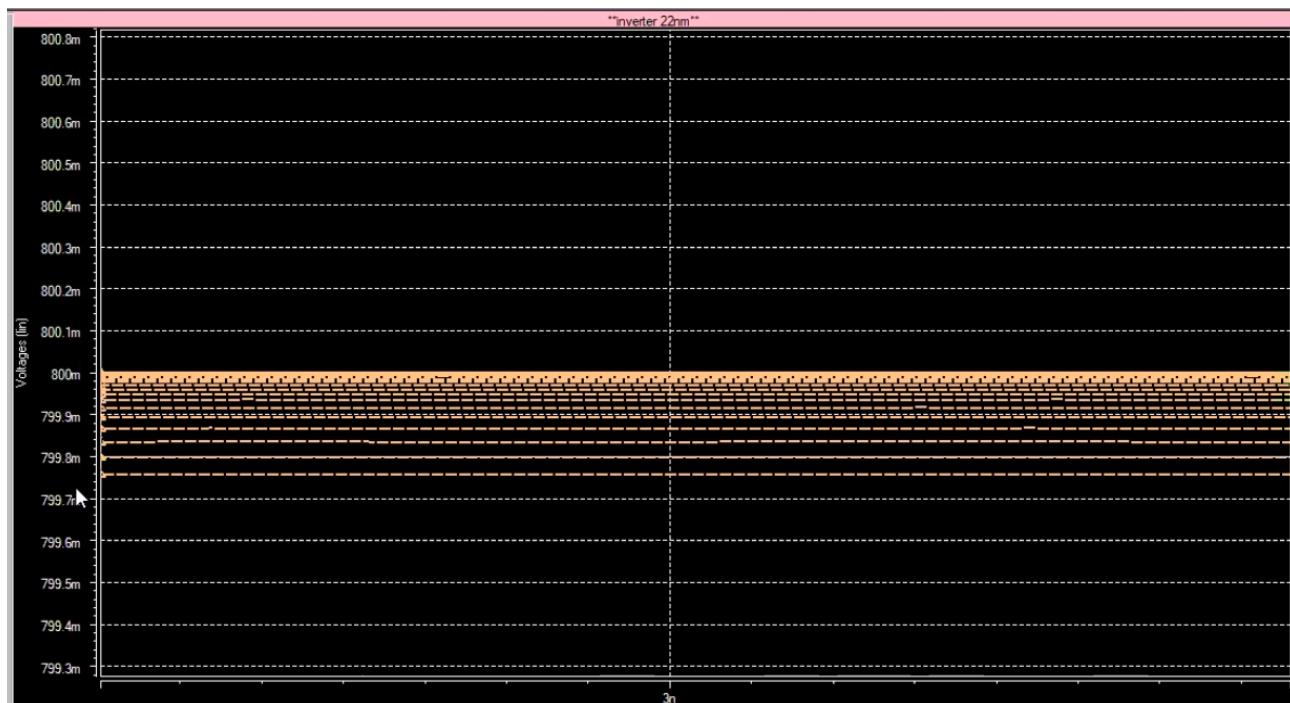
In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 c	0.0035 ns	0.004 ns
25 c	0.0065 ns	0.006 ns
125 c	0.015 ns	0.01 ns

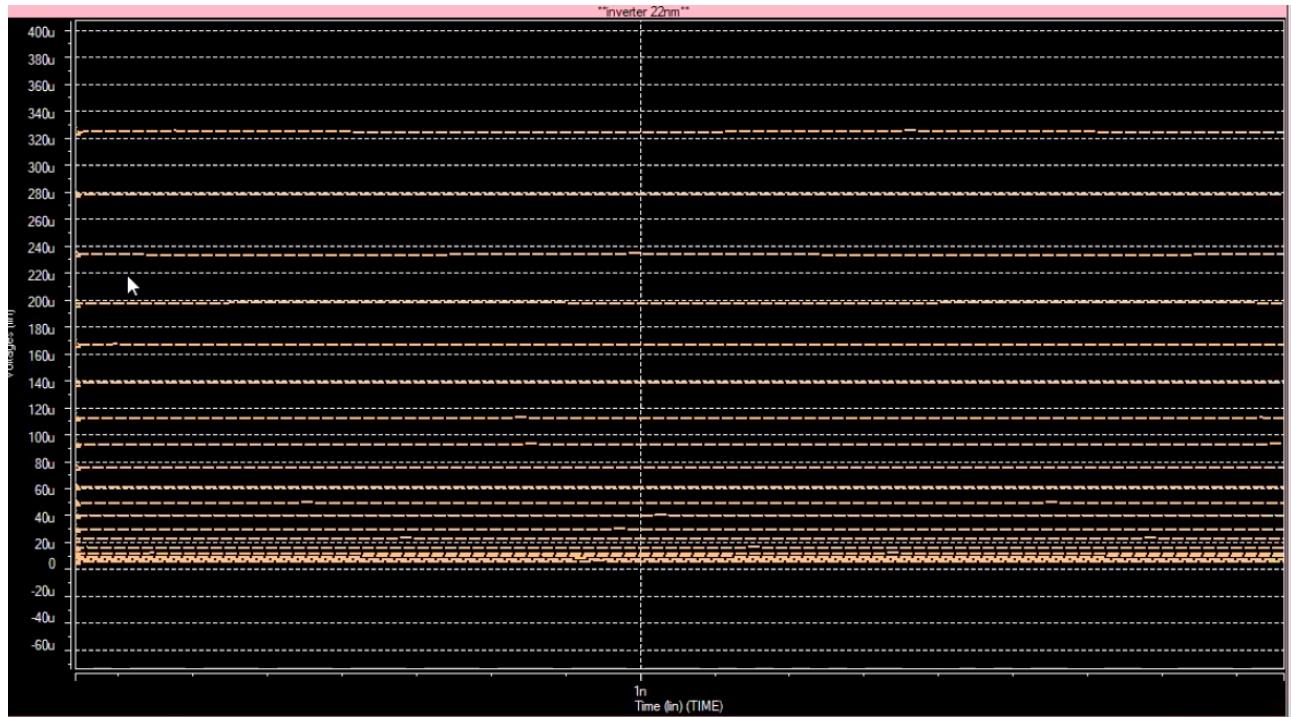
Logic values at different temp

Temperature	High logic	Low logic
-55 c	0.8 v	0.3 uV
25 c	0.8 v	7.64 uV
125 c	0.8 V	80 uV

Noise margins, at stable high voltage



From this graph we can say that there is no continuous stable high and low logic levels



5) Current analysis of inverter

Temperature	leakage current
-55 °C	90 nA
25 °C	0.12 uA
125 °C	0.15 uA

Charging and discharging current (input time period is 4ns)

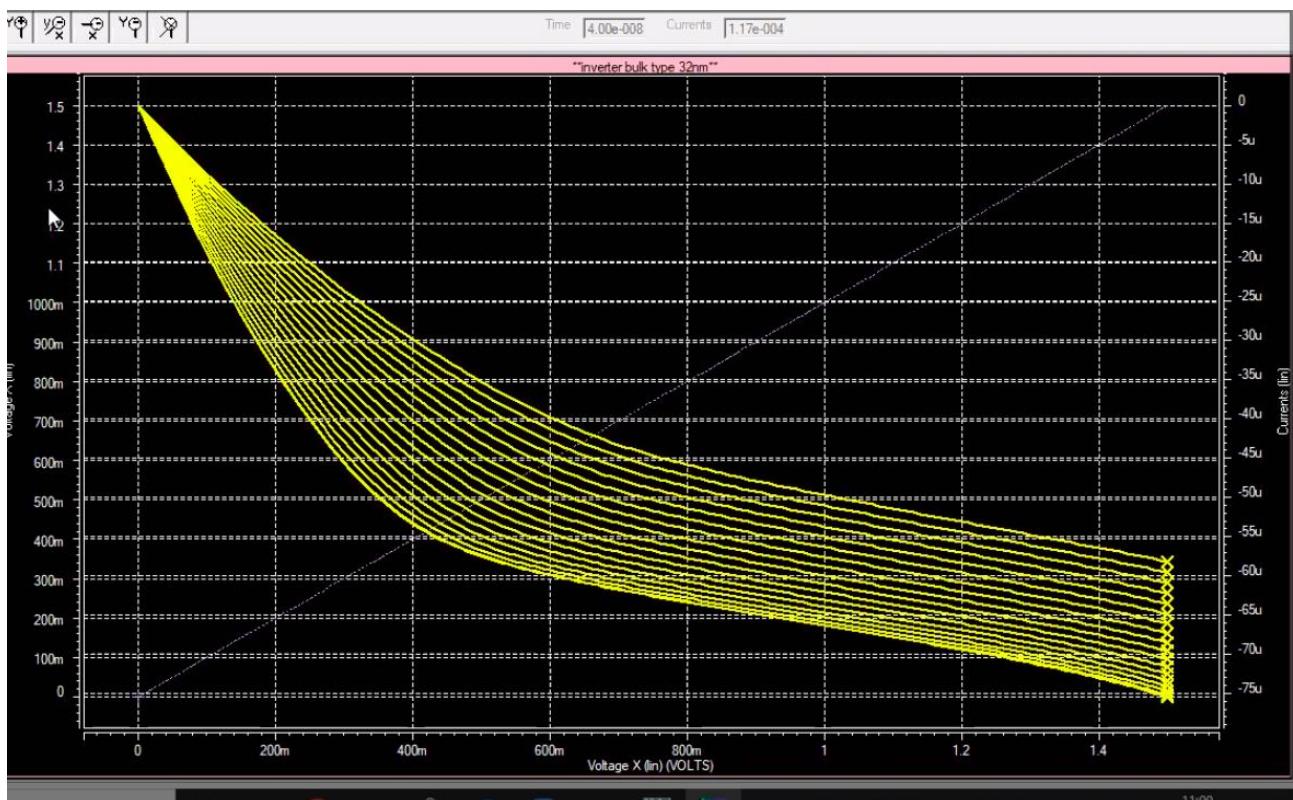
Temperature	Charging current	Discharging current
-55 °C	56.7 uA	28.7 uA
25 °C	45.5 uA	25.1 uA
125 °C	37.3 uA	24.1 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

32 nm technology(bulk)

- $V_{th0}(nmos) = 0.5088$, $V_{th0}(pmos) = -0.450$
- Biasing voltage = 1.2 v
- For inverter aspect ratio of nmos=1, pmos=2
- nmos l=32nm, w=32nm
- pmos l=32nm, w=64nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

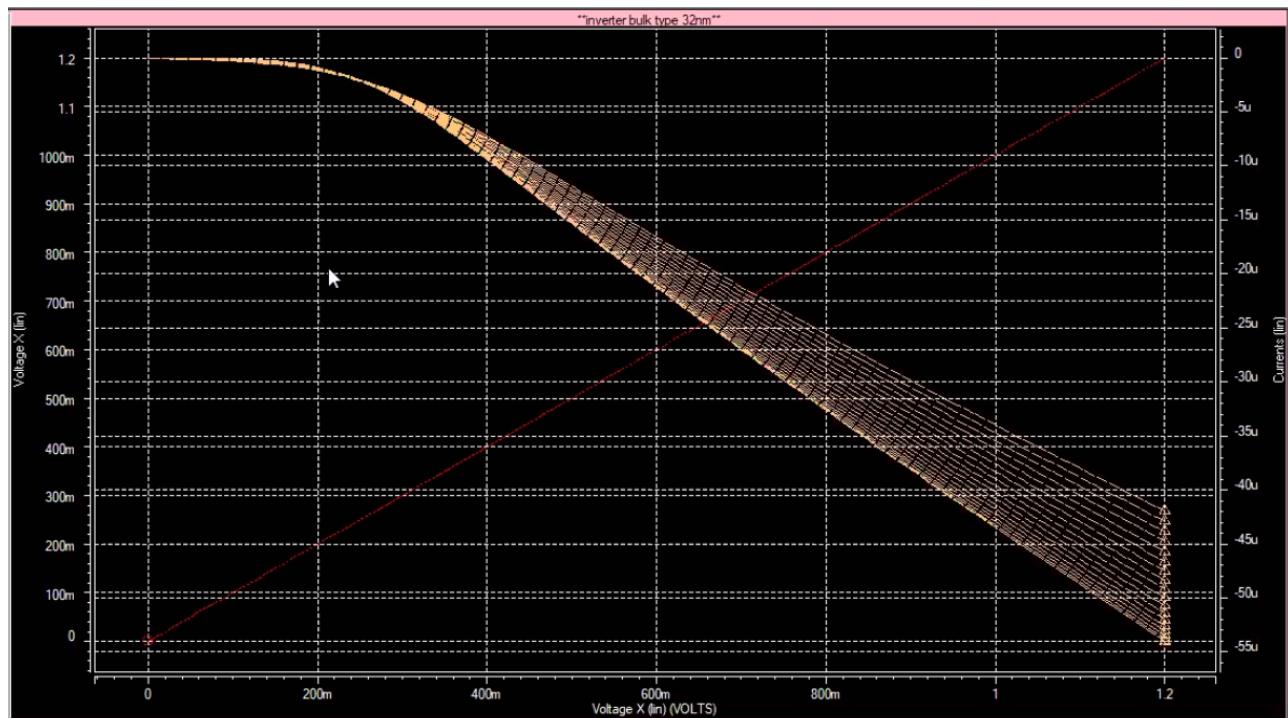
Nmos analysis



1) V_{ds} vs I_{ds}

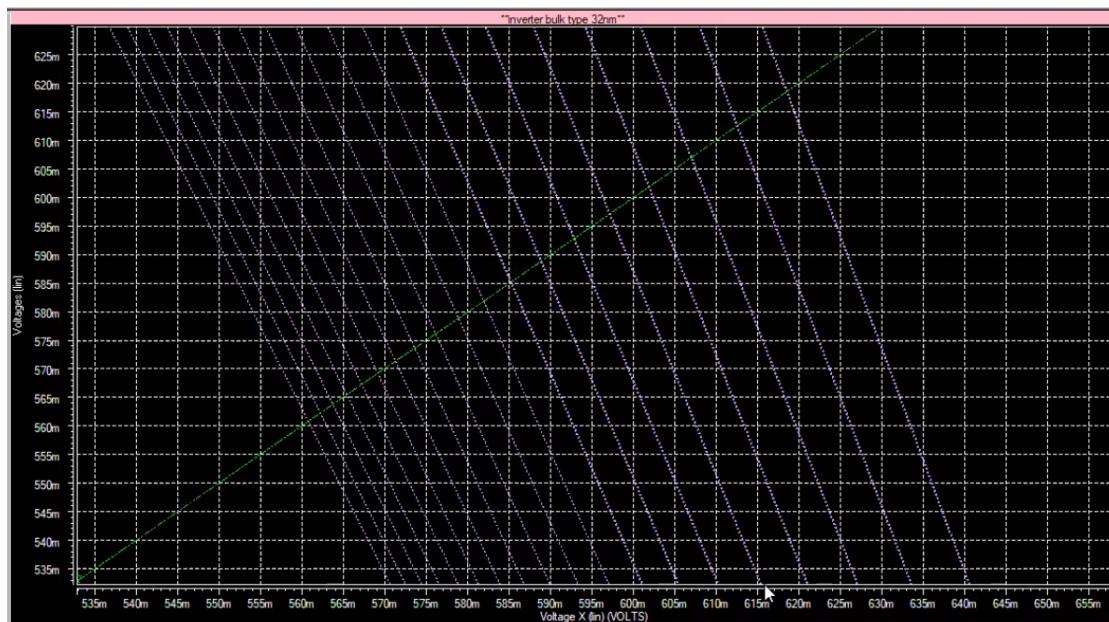
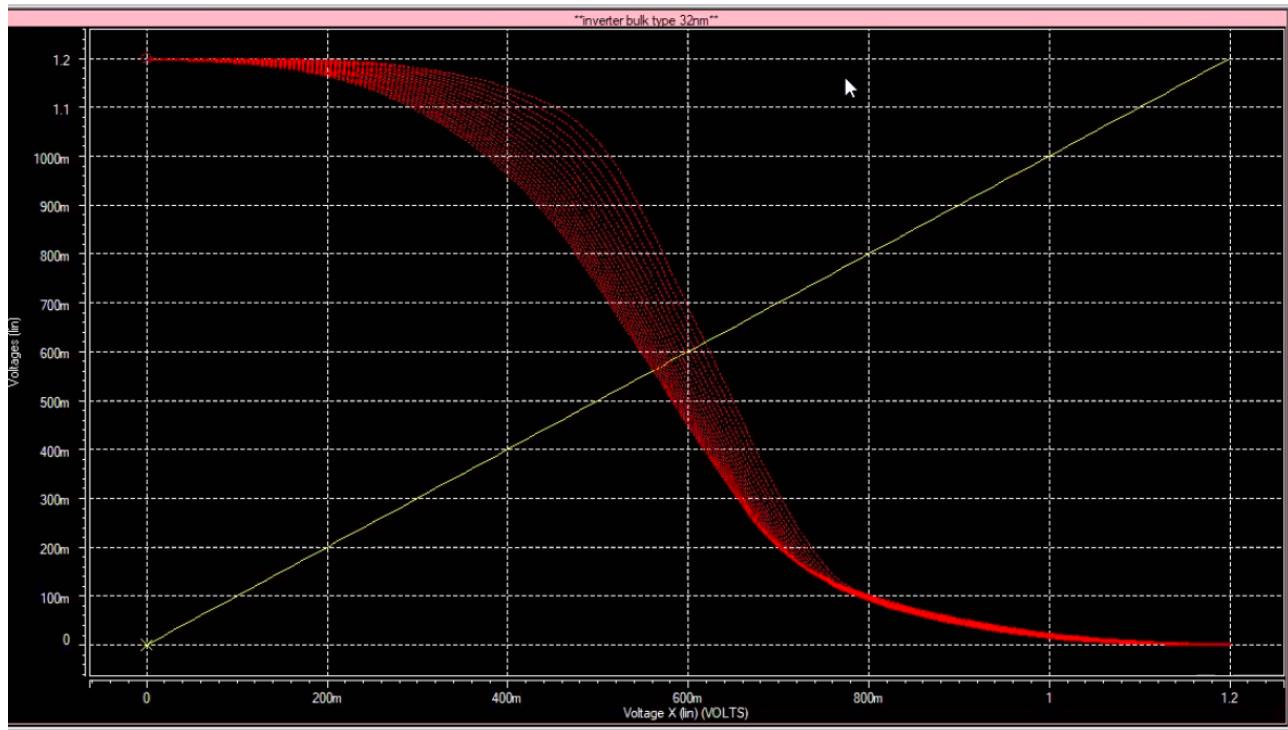
arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

2) Vgs vs Ids



Here you can see in the graph the threshold voltage is very low in comparison with the theoretical value which is mentioned above and this is the first model in which we observed this kind of graph(doubt).

3) Voltage transfer characteristics



Arrow shows midpoint voltage at -55 C

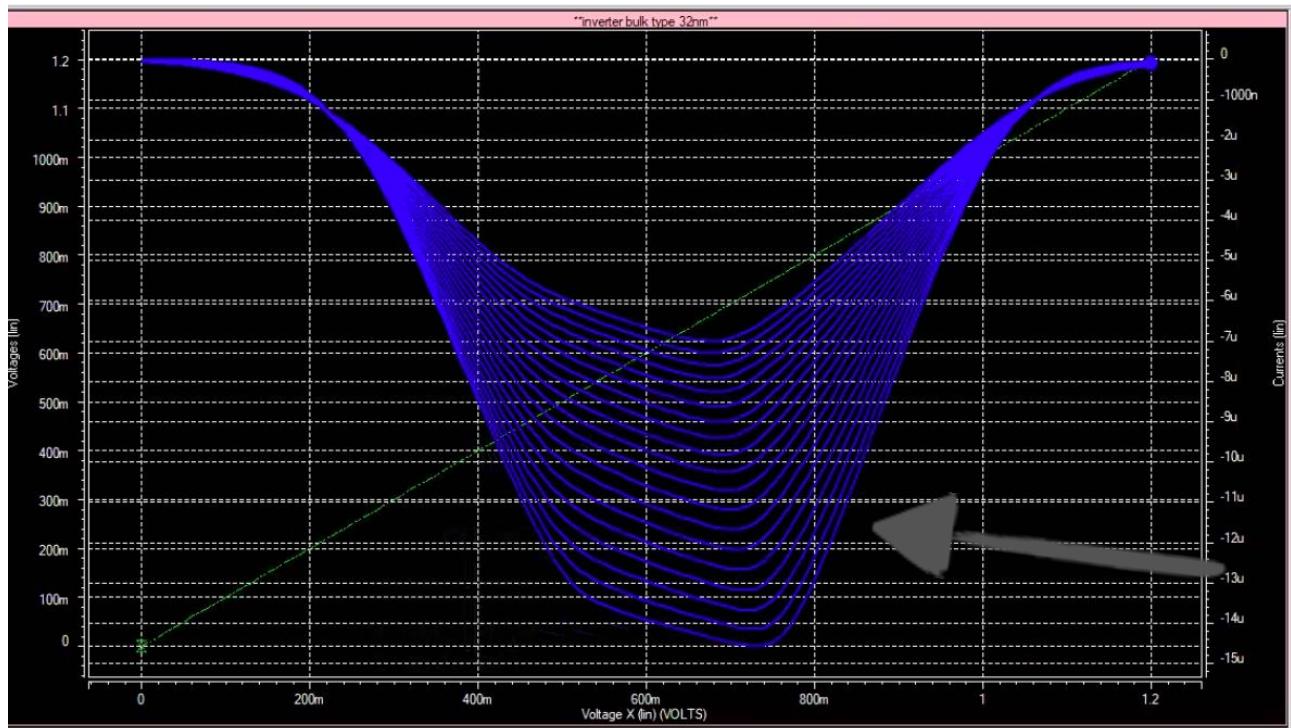
This graph shows the variation in midpoint voltage because of temp.

Less effect of positive temp.

At -55 C = 0.617 v

At 125 C = 0.562 v

For the current, the model of the pmos it is very sensitive to temperature compared to nmos, which you can observe from VTC curve .same is in vtc curve also



This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

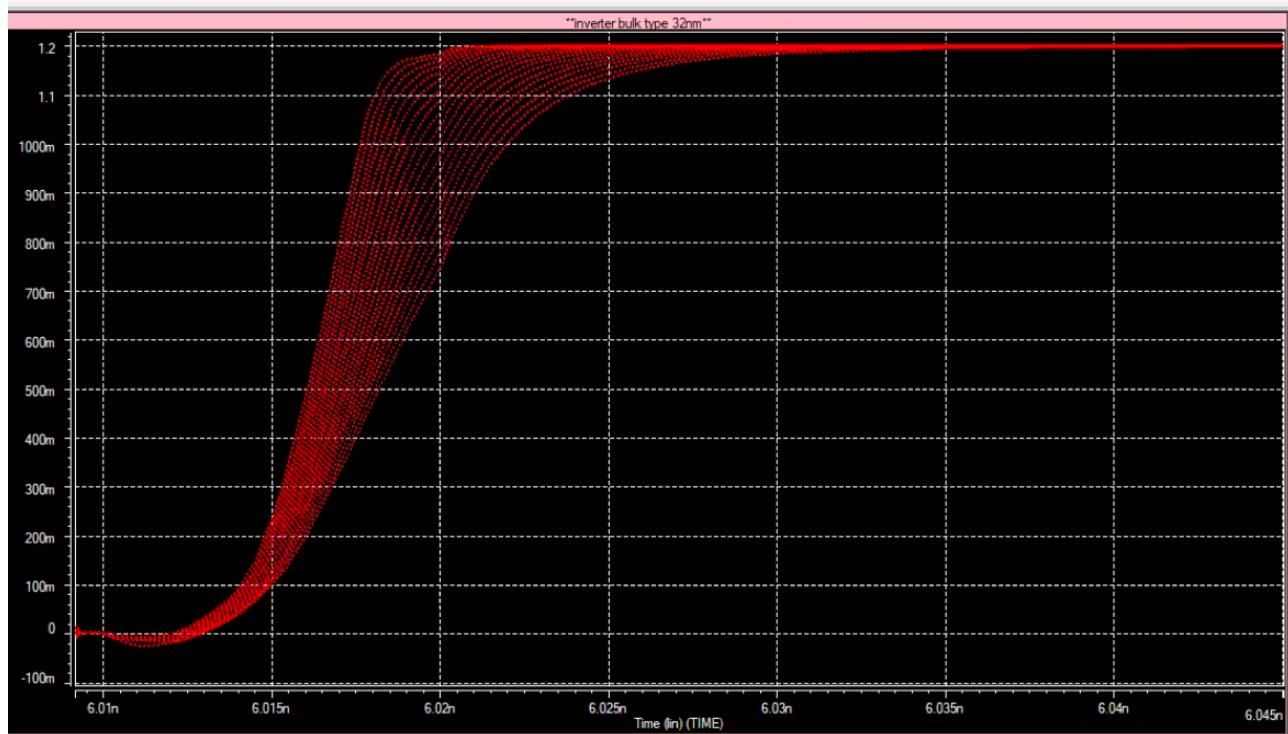
At -55 C = 15 uA

At 25 C = 11.2 uA

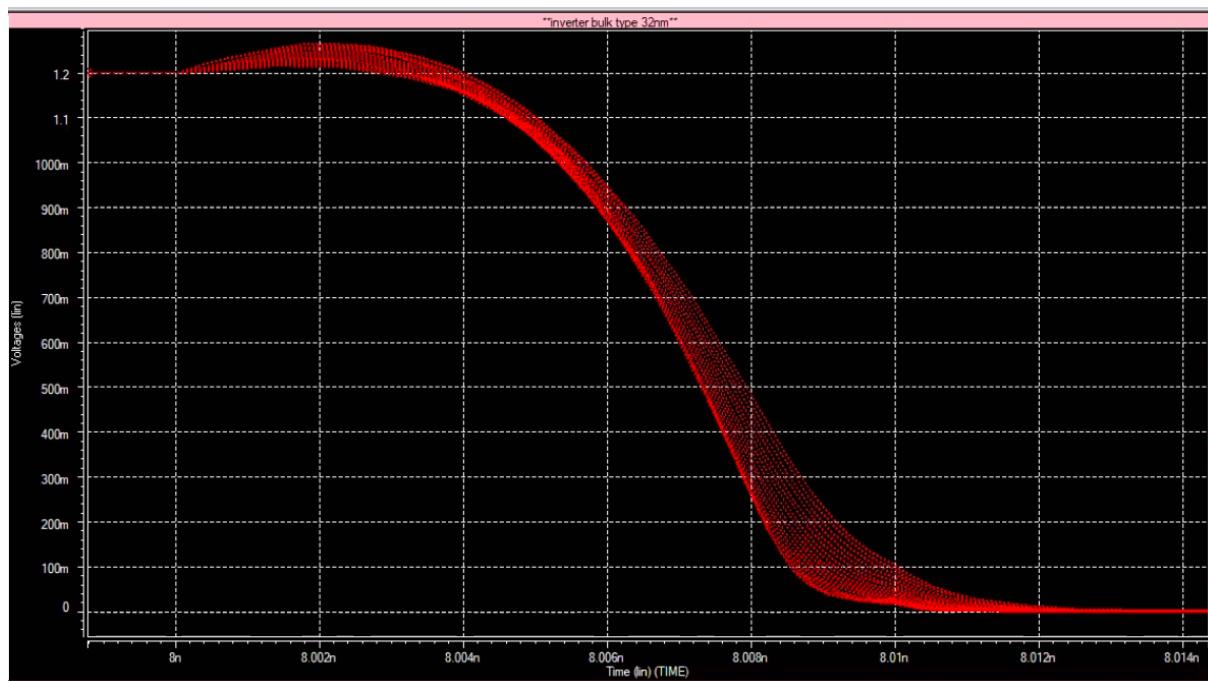
At 125 C = 7 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



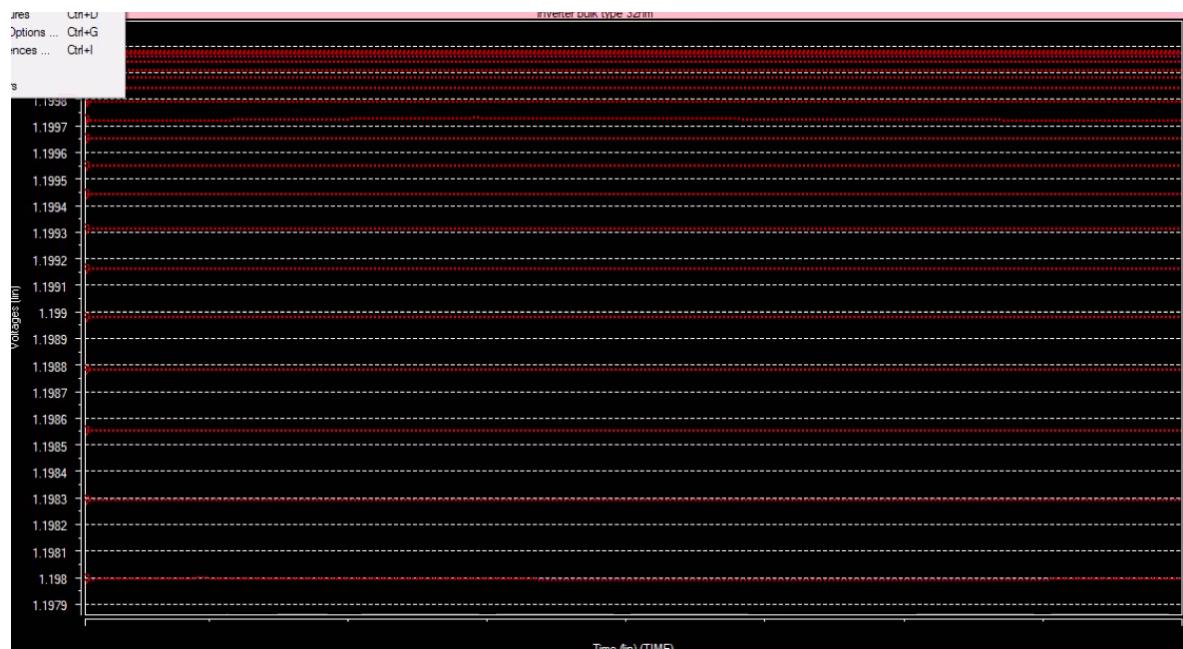
Rise time at different temperature. graph of rise tome at 125 C.

Fall time at different temperature. shows graph of rise tome at 125 C

In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

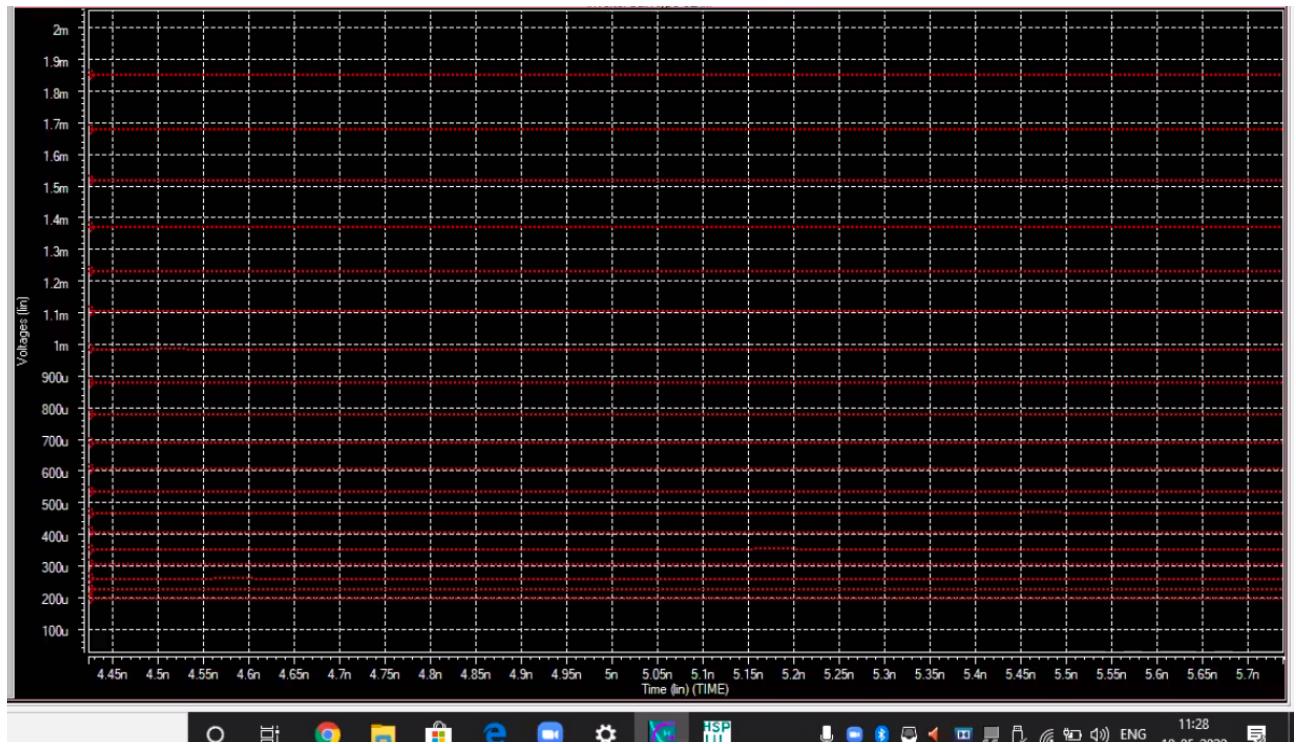
Here we have observed that the overshoot is very very less in comparison with the strained silicon models

Temperature	Rise time	Fall time
-55 c	0.011 ns	0.0011 ns
25 c	0.016 ns	0.012 ns
125 c	0.025 ns	0.014 ns



Logic values at different temp

Temperature	High logic	Low logic
-55 c	1.2 v	200 uV
25 c	1.1997 v	550 uV
125 c	1.198 v	1860 uV



5) Current analysis of inverter

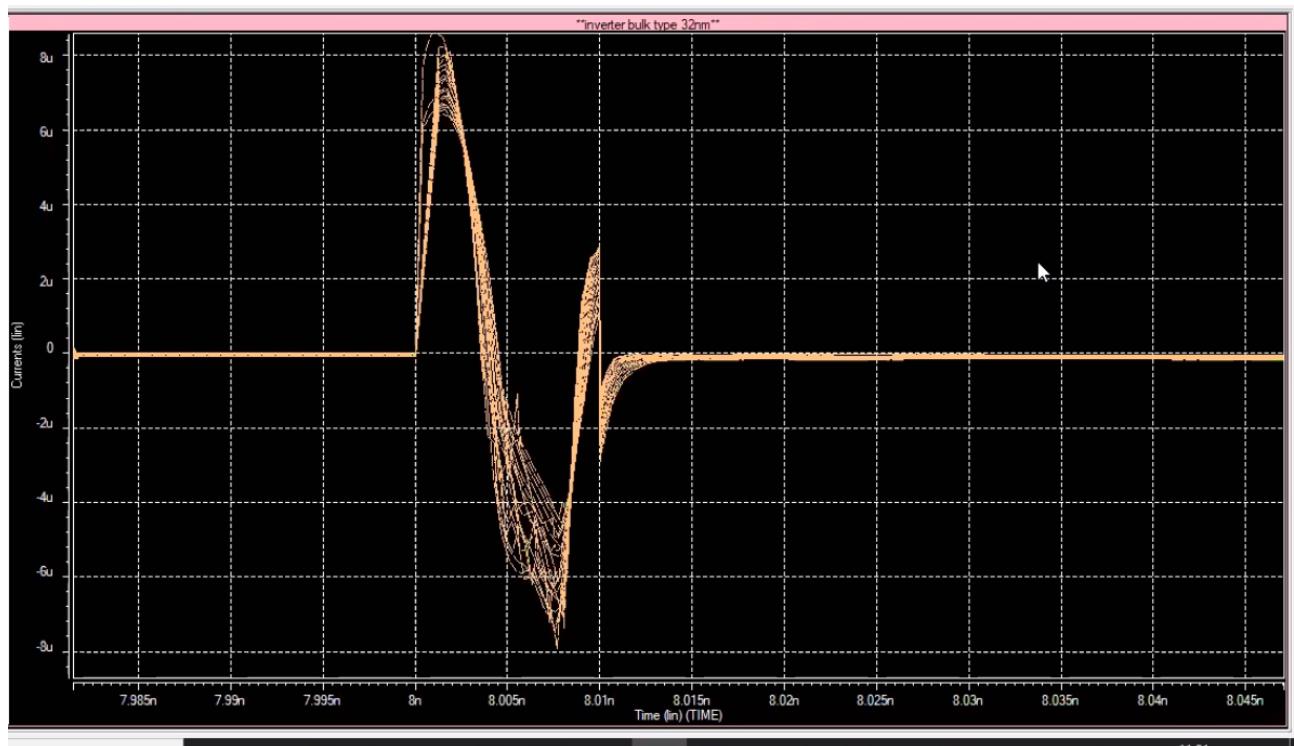
Leakage current analysis



Temperature	leakage current
-55 c	10 nA
25 c	25 nA
125 c	75 nA

6) Charging and discharging current (input time period is 4ns)

This is the graph of the discharging current. We observed this type of graph of discharging current first time(doubt)



In this tables result is not proper

Temperature	Discharging current	Charging current
-55 c	8.23 uA	25 uA
25 c	7.63 uA	18.8 uA
125 c	8.65 uA	15 uA

At input frequency is 0.04 ns

Temperature	Discharging current	Charging current
-55 c	69 uA	110 uA
25 c	60 uA	95 uA
125 c	81 uA	59 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

Here in this model frequency response of inverter is not proper.

Ideally what should be that as frequency increase current should be increase but in this model we can't observe this result.

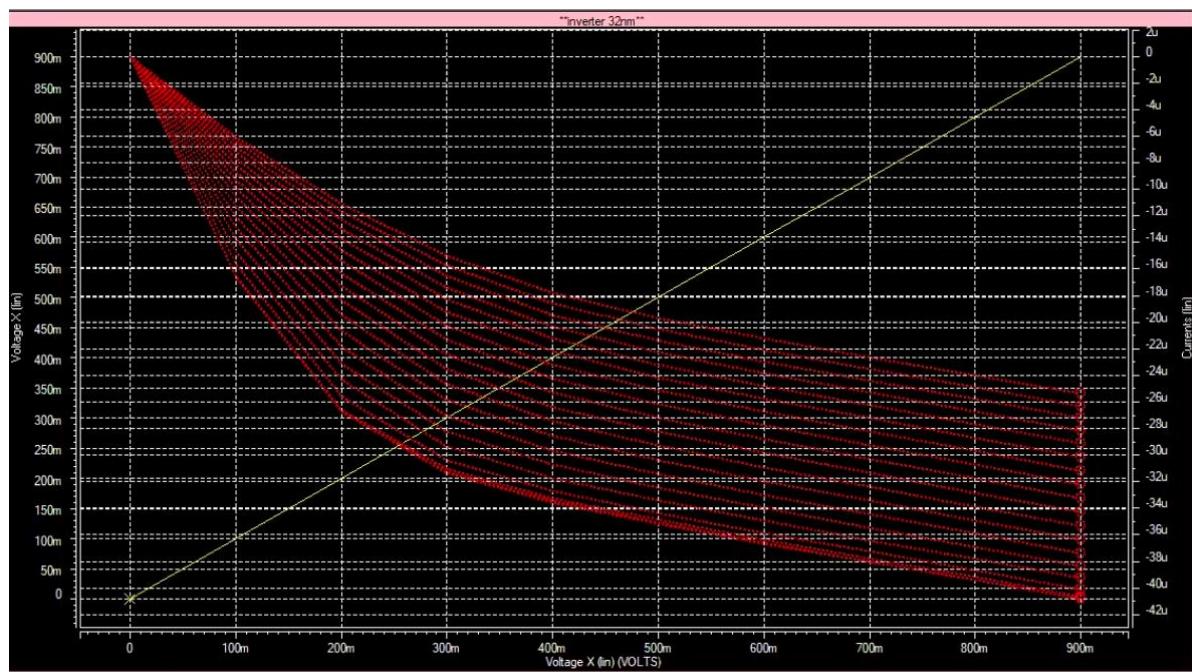
Here charging and discharging current should be decrease with the temp. Increase !

But here it's not happened

32 hp(high power) nm model analysis

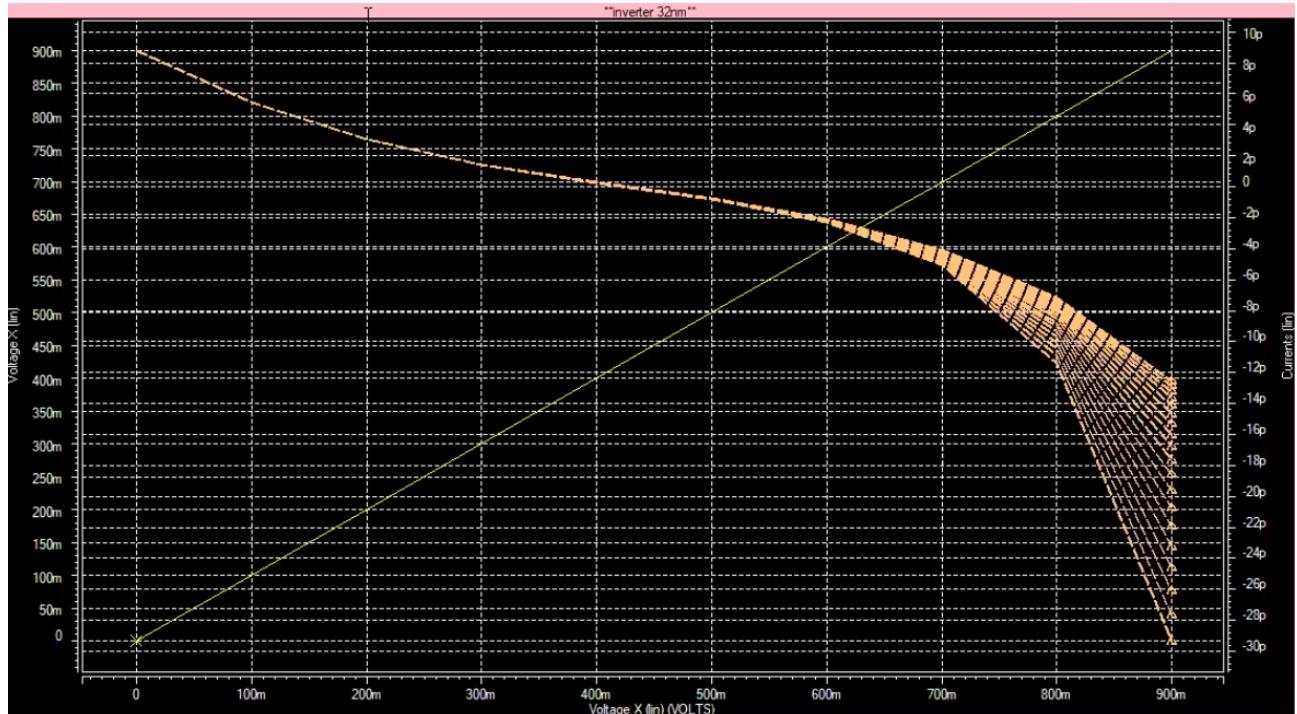
- High k
- Strained silicon
- $V_{th}(nmos) = 0.49396v$ $V_{th}(pmos) = -0.49155$
- Biasing voltage=0.9 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=32nm, w=32nm
- pmos l=32nm, w=64nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis



1) Vdd vs Ids

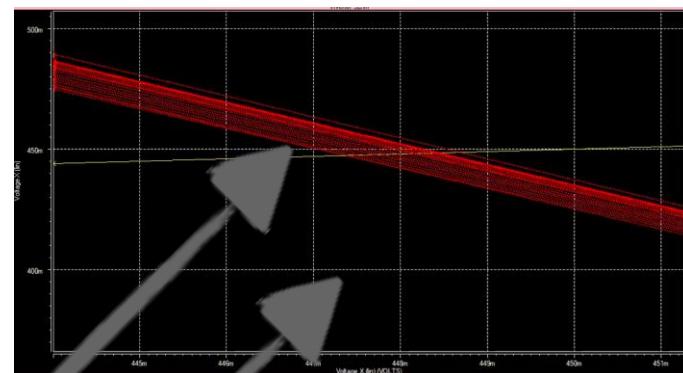
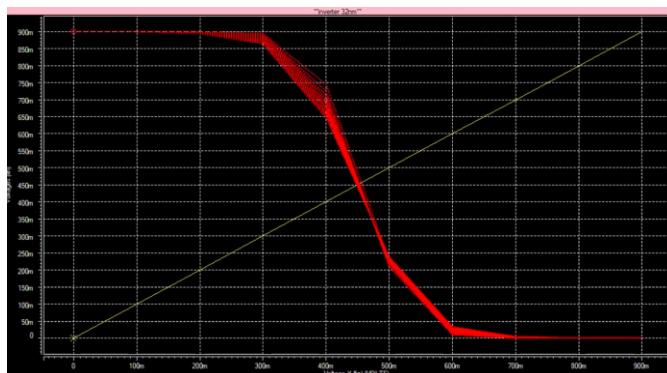
the graph at -55 centigrade. As temperature increase the current will decrease.



2) Vgs vs Ids

the graph shows at -55 temp. As temperature increase the current will decrease.

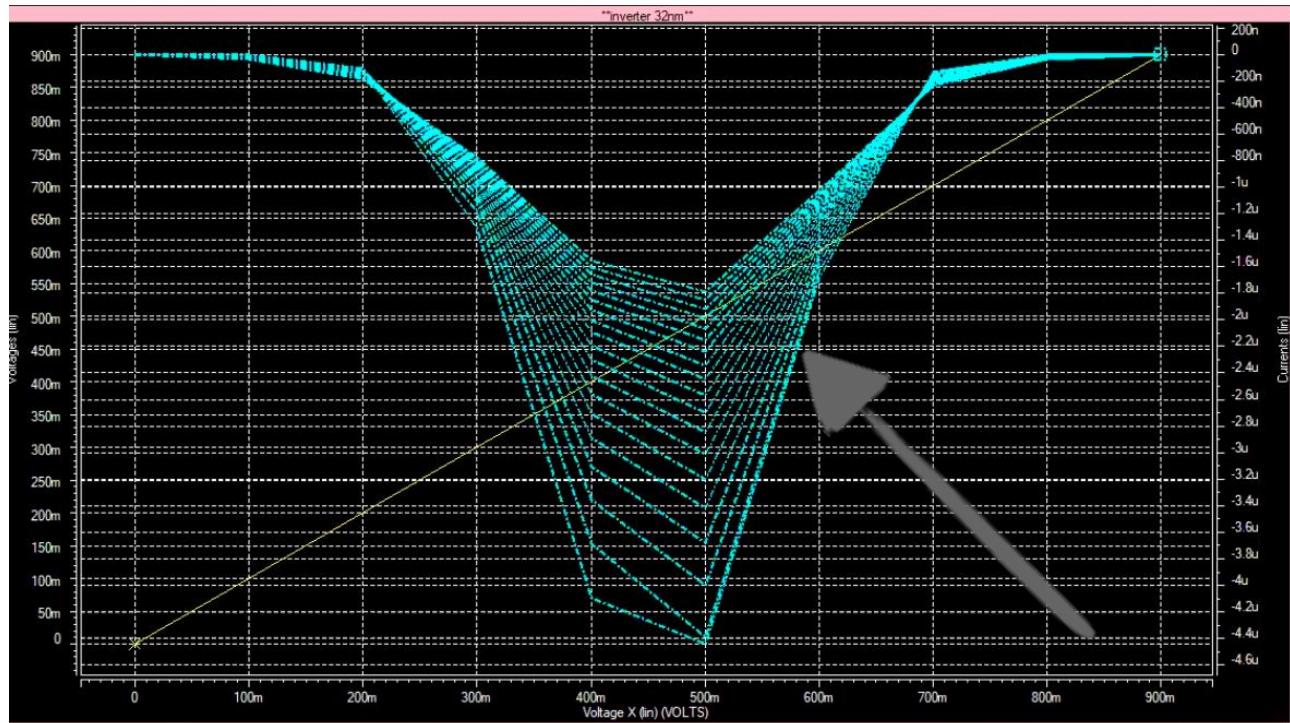
3) Voltage transfer characteristics



This graphs shows the variation in midpoint voltage because
At -55 C = 0.457 v
At 125 C = 0.456 v

of temp.

Midpoint current

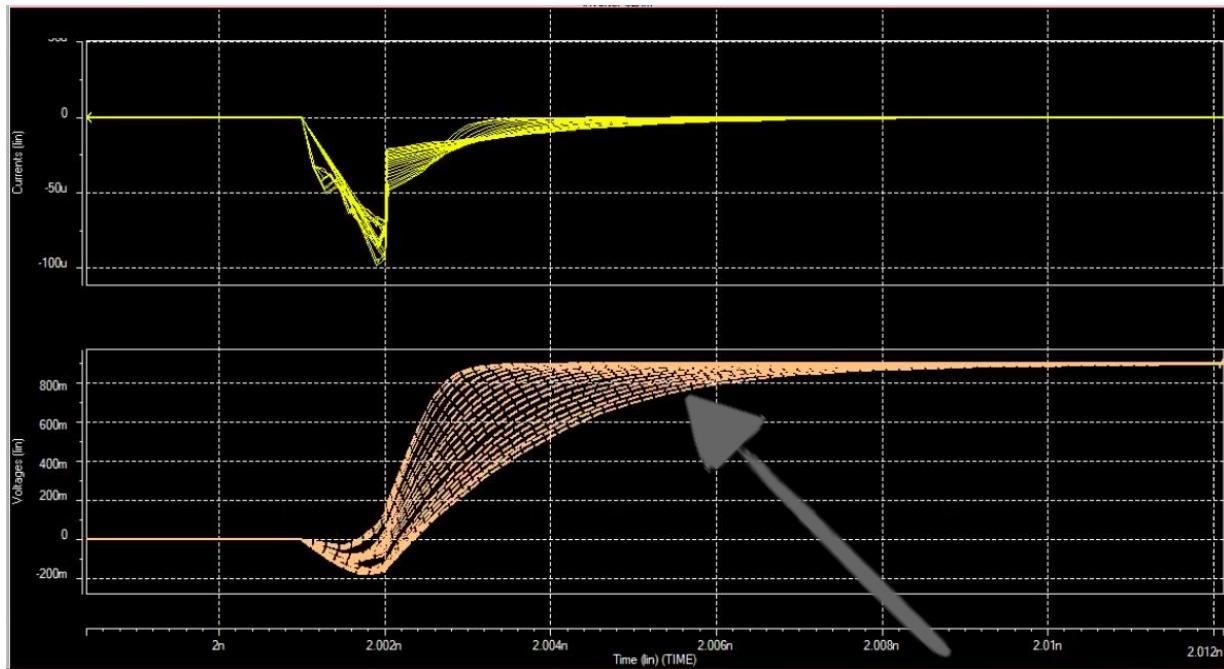


This arrow shows the graph at -55 temp.
Drain current of inverter(at mid point voltage)
At -55 C = 4.44 uA
At 25 C = 2.7 uA
At 125 C = 1.79 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

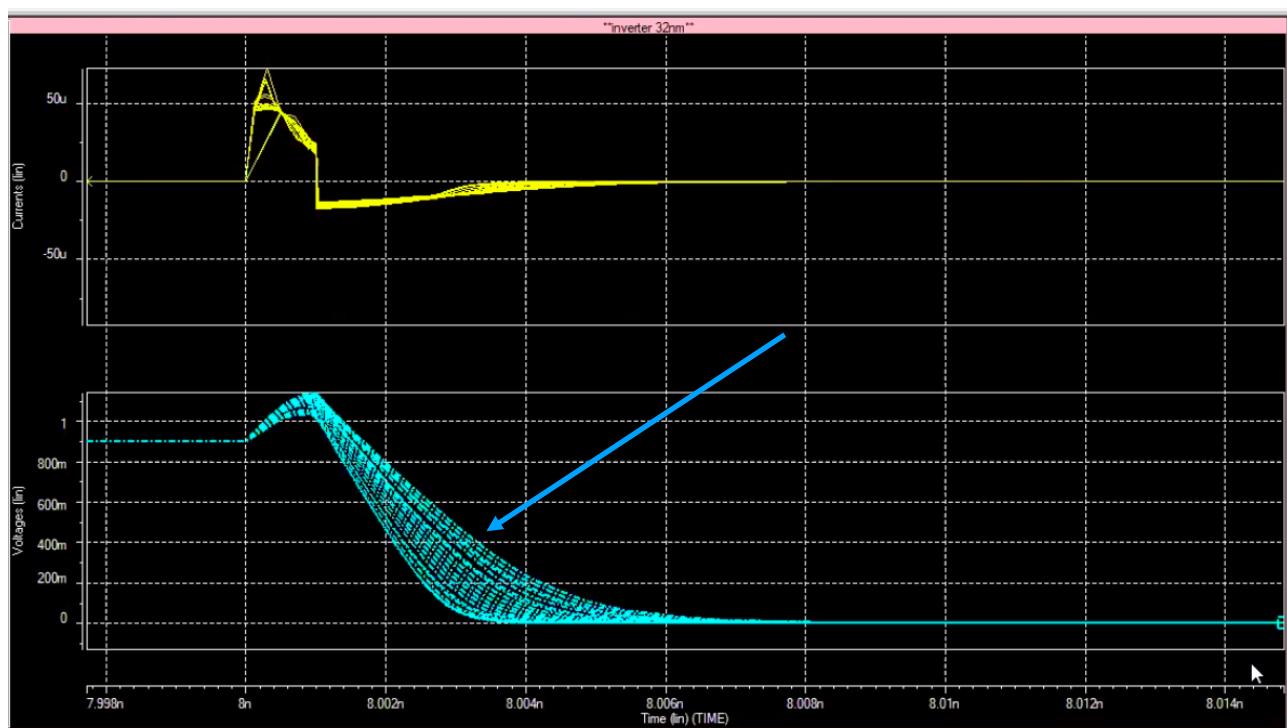
Inverter analysis

4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise tome at 125 C



In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

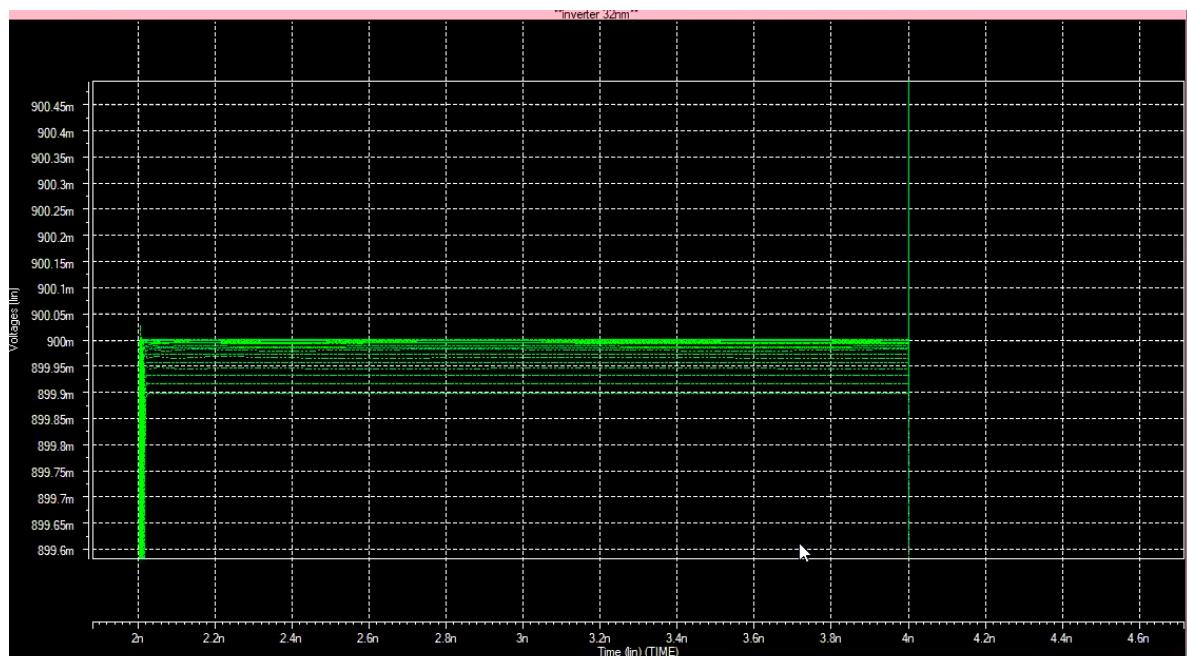
Temperature	Rise time	Fall time
-55 °C	0.003 ns	0.004 ns
25 °C	0.007 ns	0.006 ns
125 °C	0.014 ns	0.008 ns

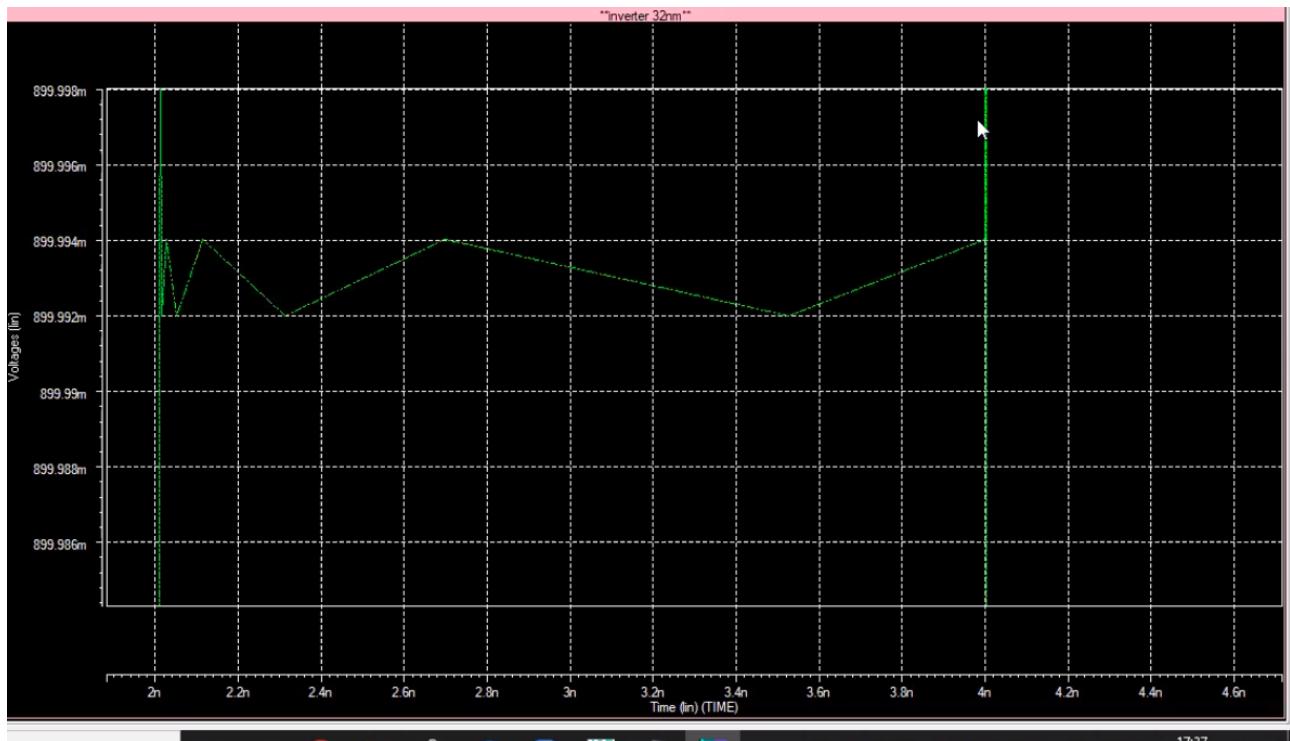
Logic values at different temp

Temperature	High logic	Low logic
-55 °C	0.9 V	0.3 uV
25 °C	0.9 V	7.64 uV
125 °C	0.9 V	80 uV

Noise margins ,at stable high voltage

From this graph we can say that there is no continuous stable high and low logic levels .





5) Current analysis of inverter

Leakage current analysis

Temperature	leakage current
-55 c	4.56 nA
25 c	95.3 nA
125 c	125 nA

Charging and discharging current (input time period is 4ns)

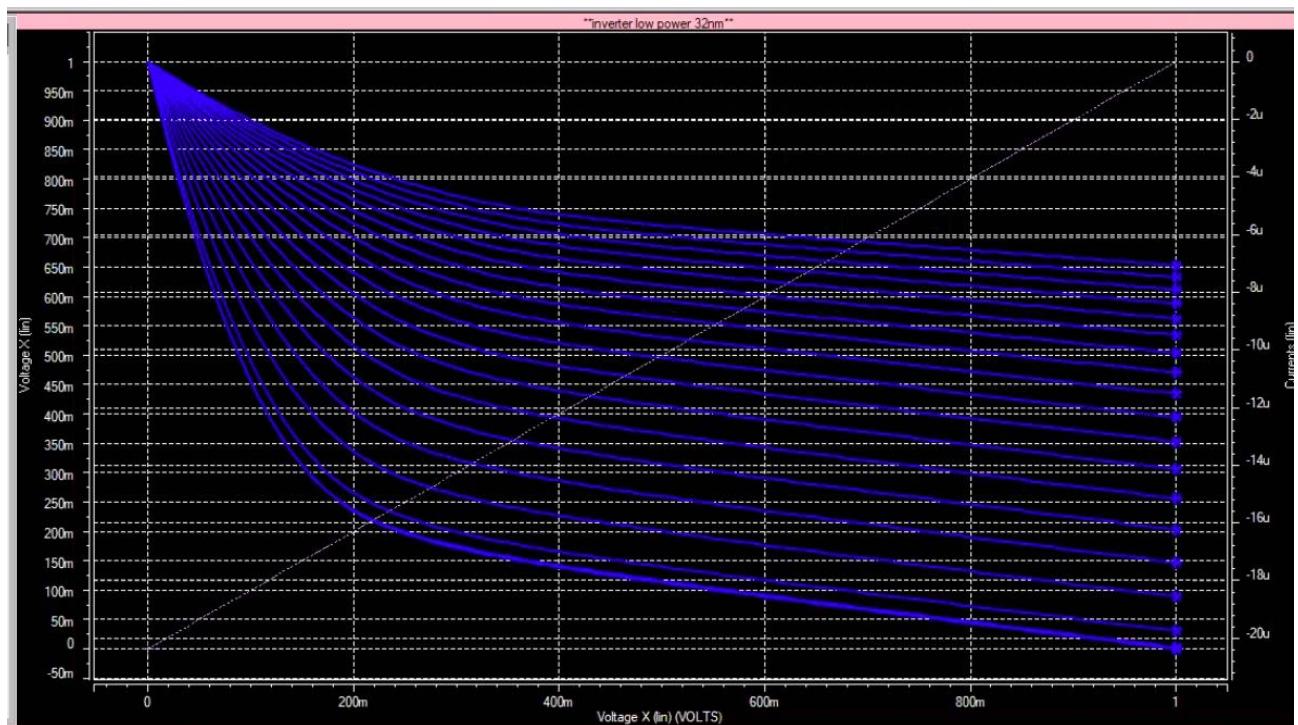
Temperature	Charging current	Discharging current
-55 c	99.5 uA	74 uA
25 c	82.8 uA	64.8 uA
125 c	68.4 uA	46.4 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time than charging discharging current will increase drastically.

32 lp(low power) nm model analysis

- High k
- Strained silicon
- $V_{th}(nmos) = 0.63$, $V_{th}(pmos) = -0.5808$
- Biasing voltage=1 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=32nm, w=32nm
- pmos l=32nm, w=64nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade

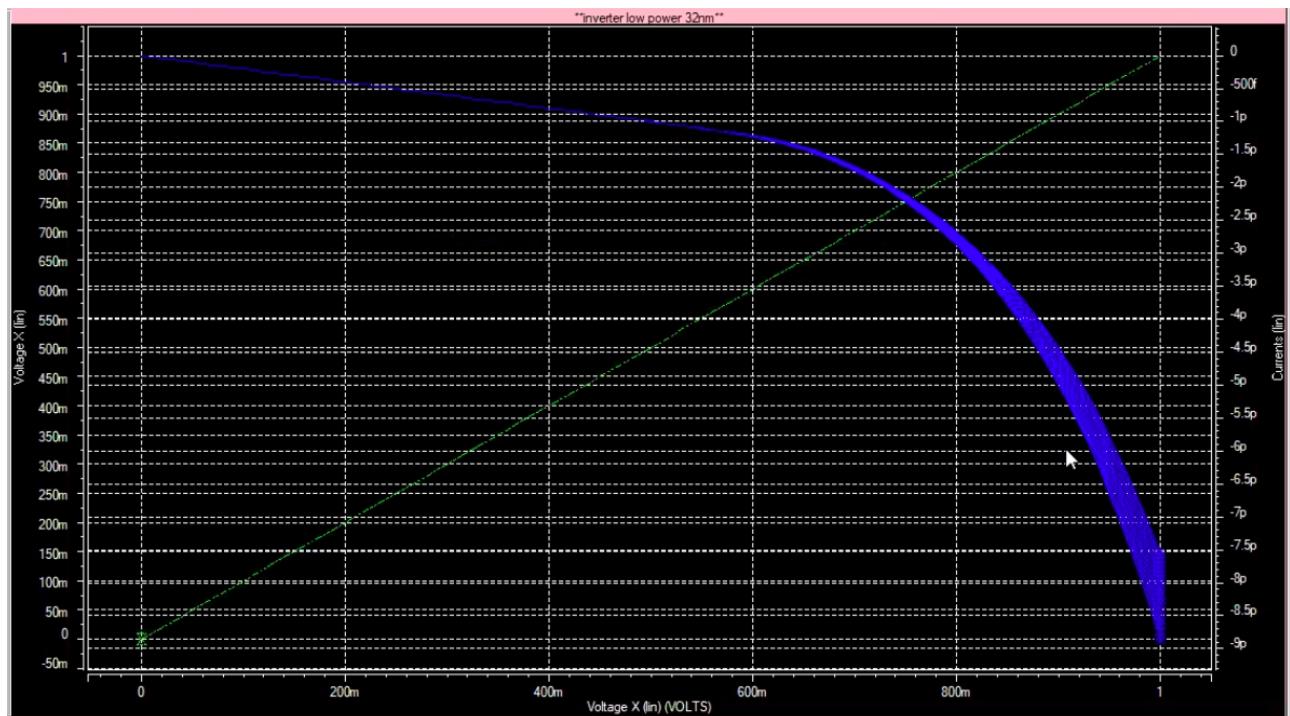
Nmos analysis



1) V_{ds} vs I_{ds}

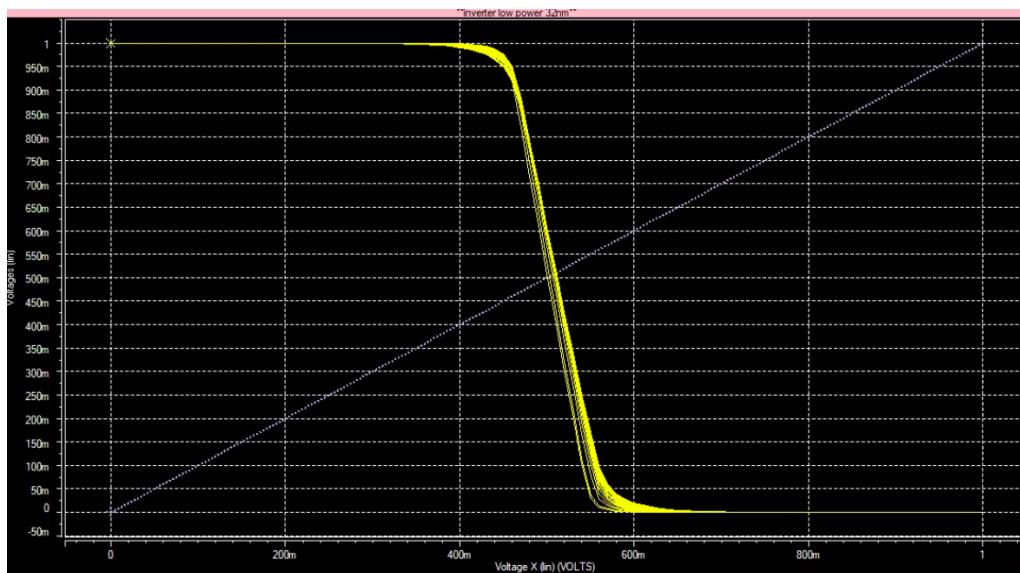
the graph at -55 centigrade. As temperature increase the current will decrease.

2) Vgs vs Ids



The graph shows at -55 centigrade. As temperature increase the current will decrease.

Voltage transfer characteristics

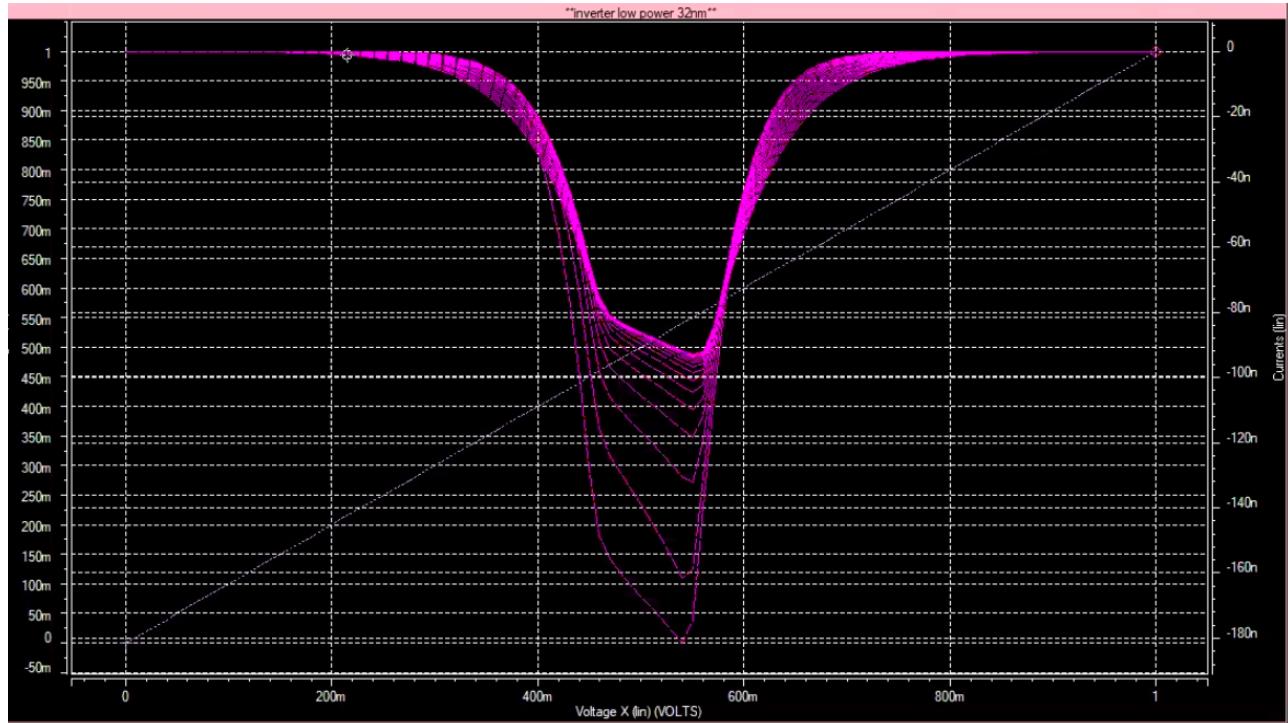


This graphs shows the variation in midpoint voltage because of temp.

At -55 C = 0.511 v

At 125 C = 0.501 v

Midpoint current



This arrow shows the graph at -55°C .

Drain current of inverter(at mid point voltage)

At $-55^\circ\text{C} = 0.18 \mu\text{A}$

At $25^\circ\text{C} = 96.5 \text{ nA}$

At $125^\circ\text{C} = 92.2 \text{ nA}$

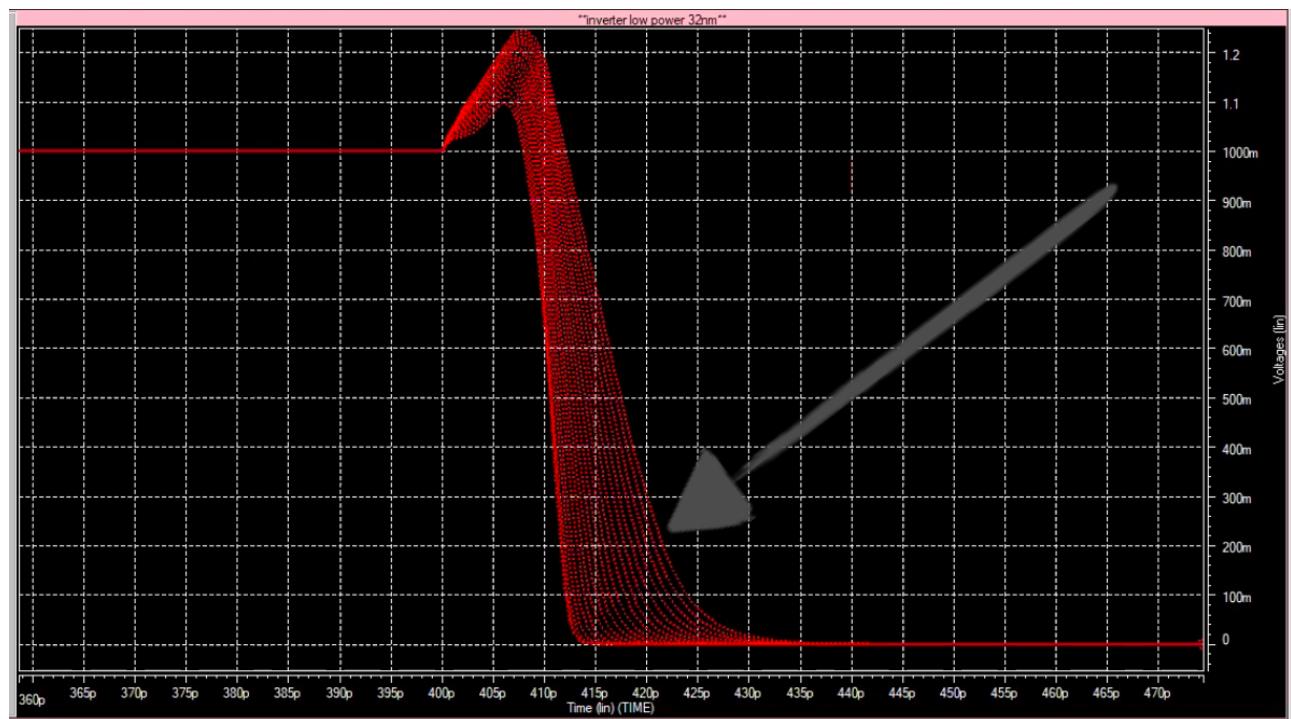
Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.



Inverter analysis

3) Rise time and Fall time analysis

Rise time at different temperature. Arrow shows graph of rise tome at 125 C.



Fall time at different temperature. Arrow shows graph of rise tome at 125 C

In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 c	23 ps	15 ps
25 c	32 ps	21 ps
125 c	50 ps	36 ps

Logic values at different temp

In this model there is steady voltages.Low logic voltage is in range of -2.5 to 2.5 uv.

4) Current analysis of inverter

Temperature	leakage current
-55 c	11.5 nA
25 c	36 nA

Charging and discharging current (input time period is 4 ns)

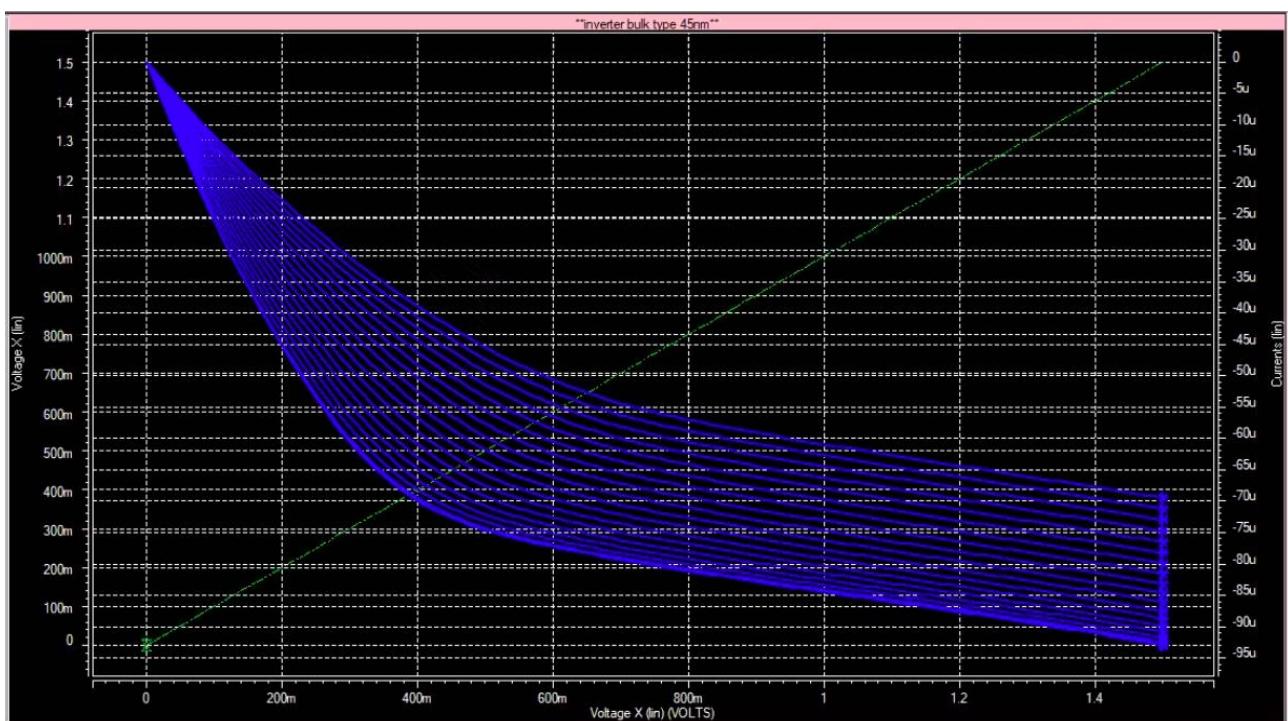
Temperature	Charging current	Discharging current
-55 c	23.2 uA	8.77 uA
	16.8 uA	7.52 uA
125 c	12.2 uA	6.68 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

45 nm technology(bulk)

- $V_{th0}(nmos) = 0.4339$, $V_{th0}(pmos) = -0.4118$
- Biasing voltage = 1.5 V
- For inverter aspect ratio of nmos=1, pmos=2
- nmos l=45nm, w=45nm
- pmos l=45nm, w=90nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

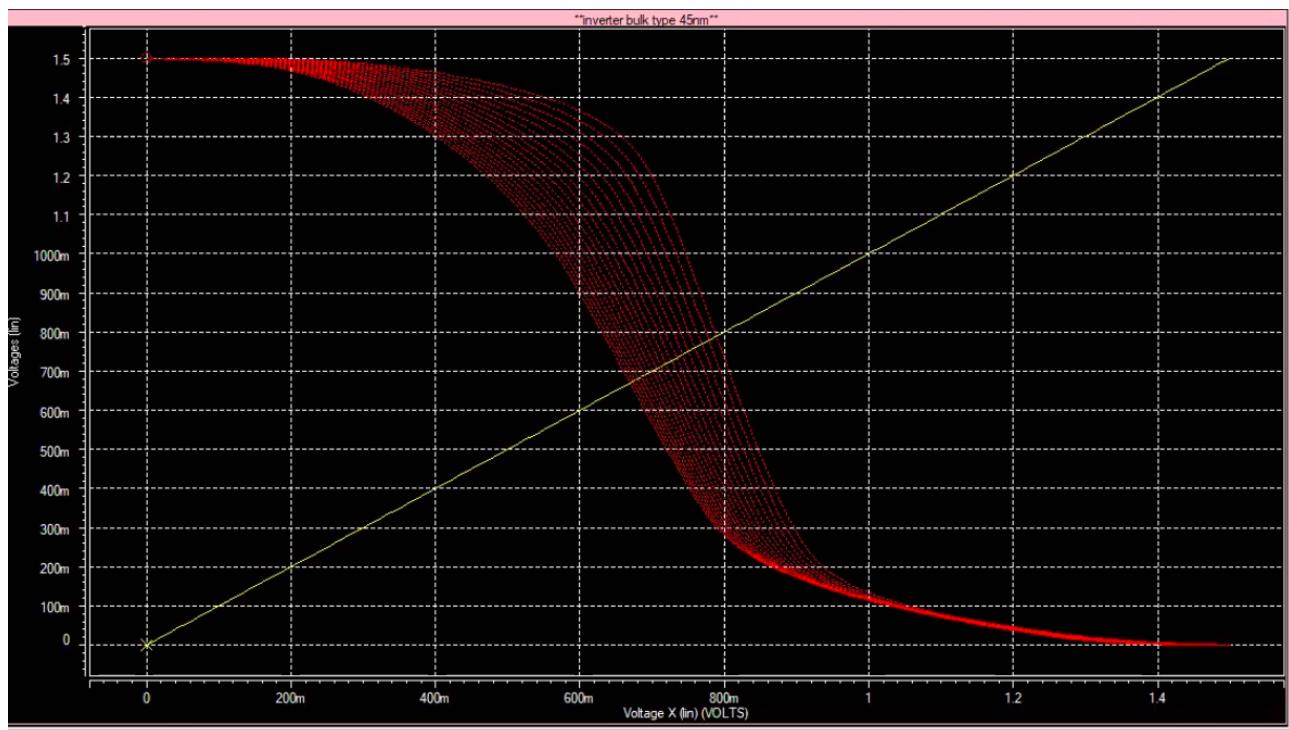
Nmos analysis



1) V_{dd} vs I_{ds}

arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

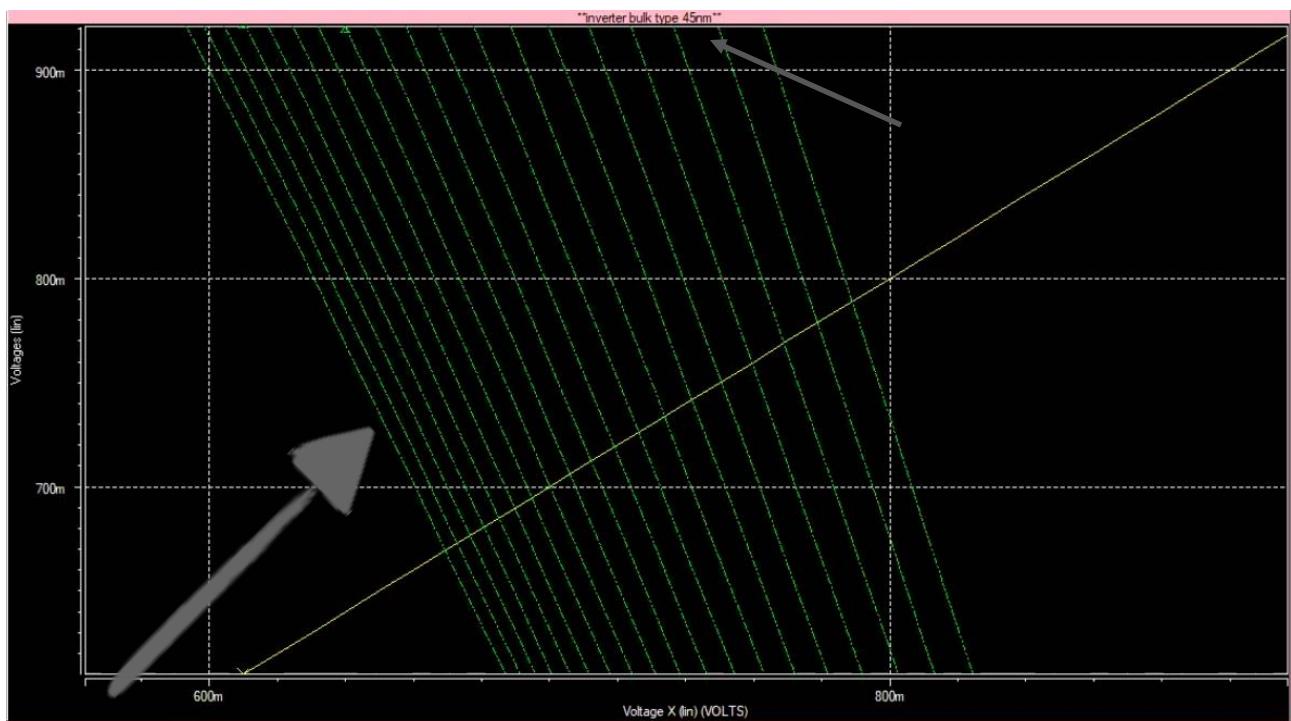
2) Vgs vs Ids



Arrow shows midpoint voltage at -55 c

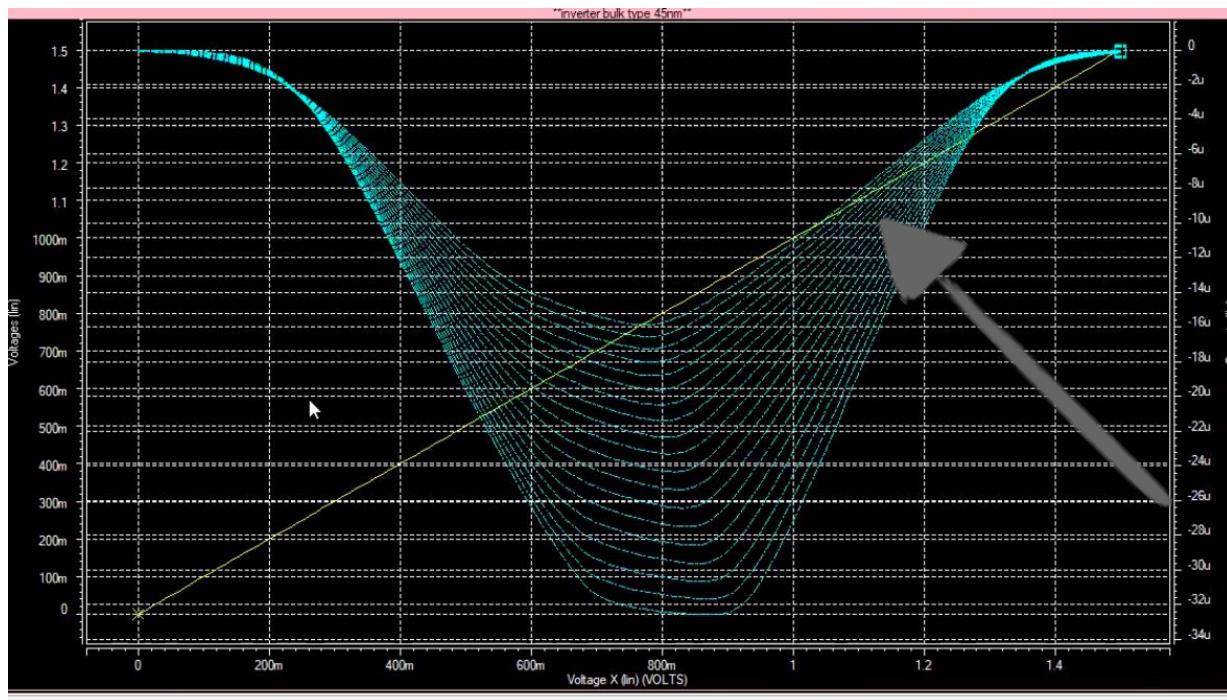
This graphs shows the variation in midpoint voltage because of temp.

At -55 C =0.785 v At 125 C =0.650 v



3) Voltage transfer characteristics

for current model of pmos it is very sensitive to temperature compared to nmos, which you can observe from VTC curve .same is in etc cu



This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

At -55 C = 32.5 uA

At 25 C = 24.3 uA

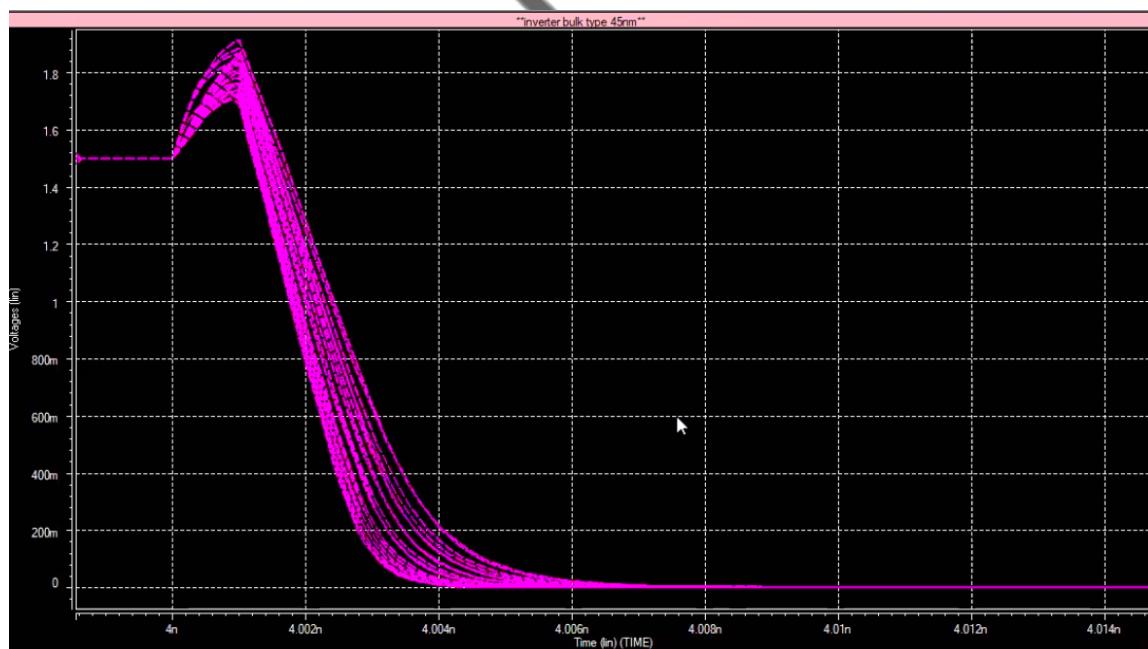
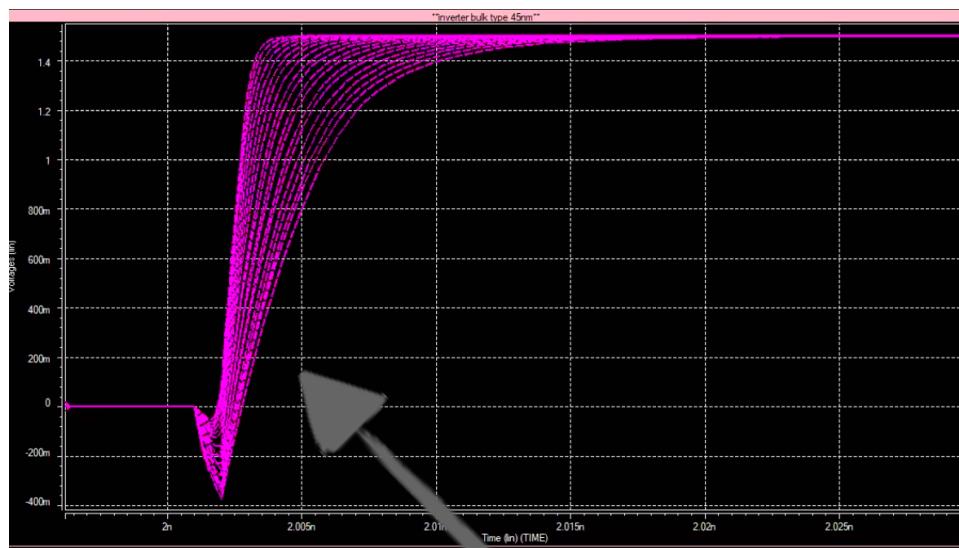
At 125 C = 15.8 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis

4) Rise time and Fall time analysis

Rise time at different temperature. Arrow shows graph of rise time at 125 C.



Fall time at different temperature. Arrow shows graph of rise time at 125 C

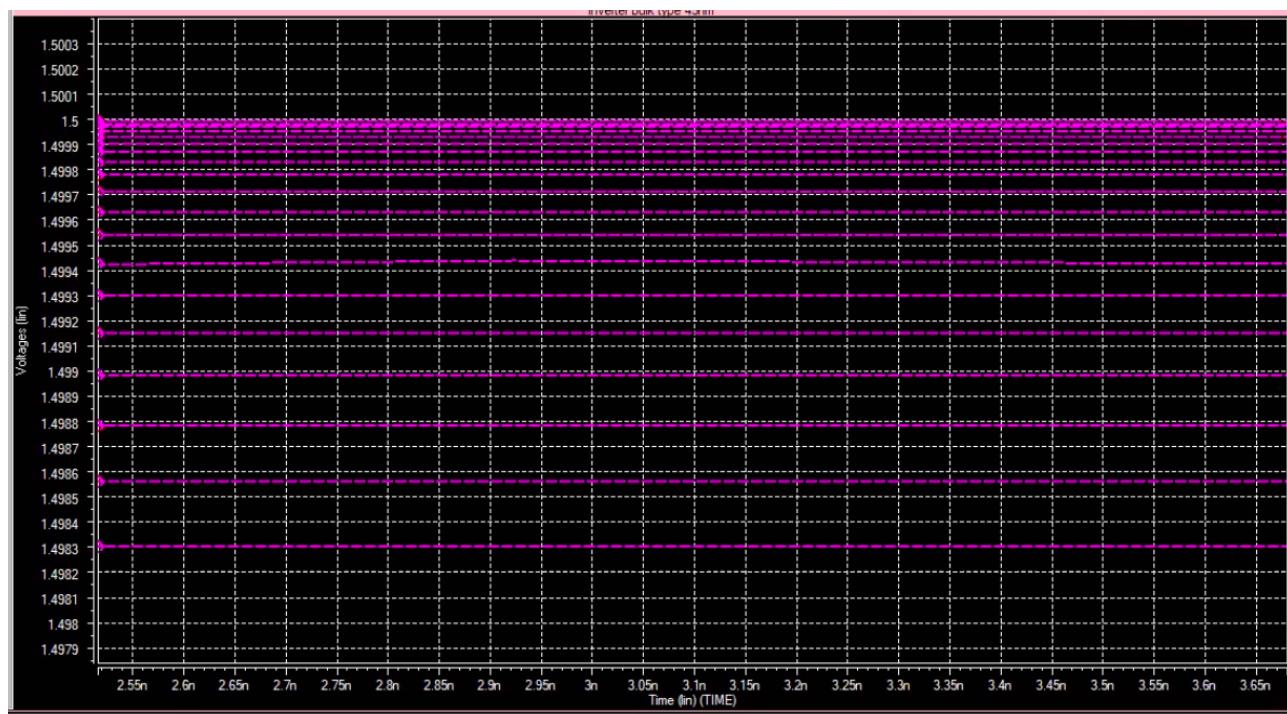
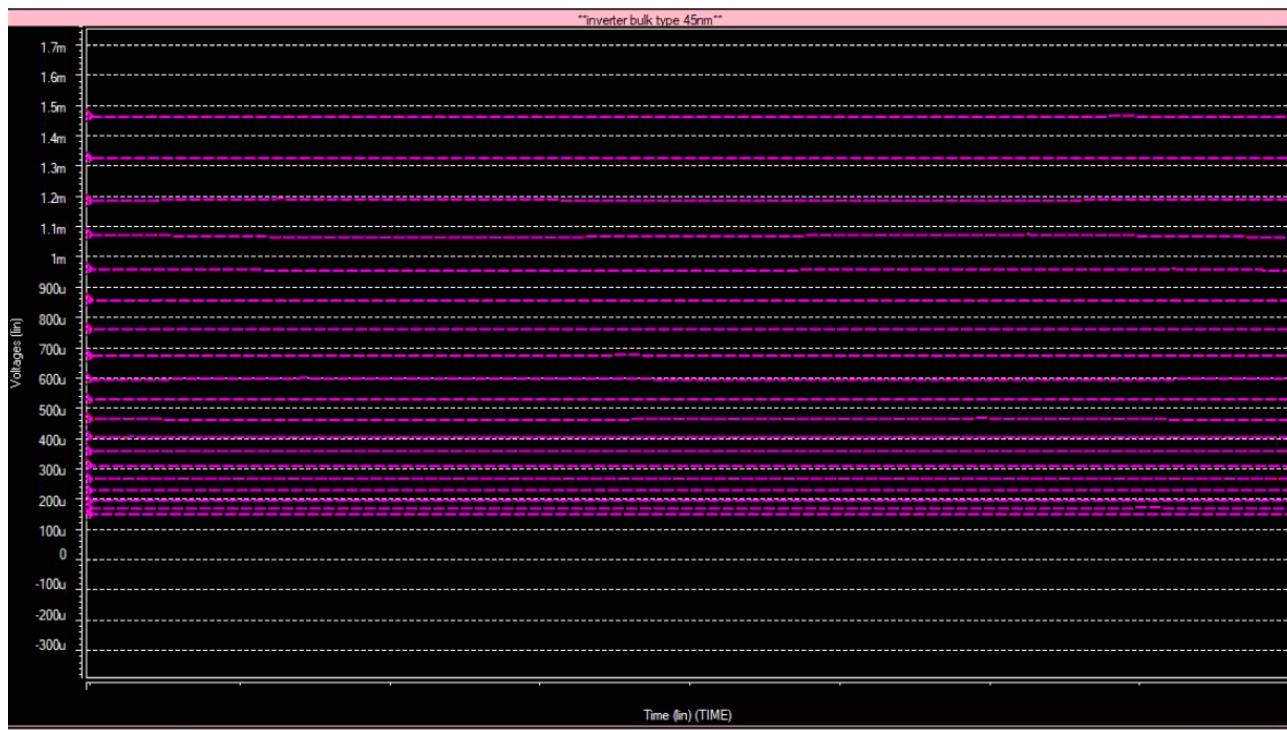
In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 c	0.0045 ns	0.0045 ns
25 c	0.013 ns	0.006 ns
125 c	0.019 ns	0.009 ns

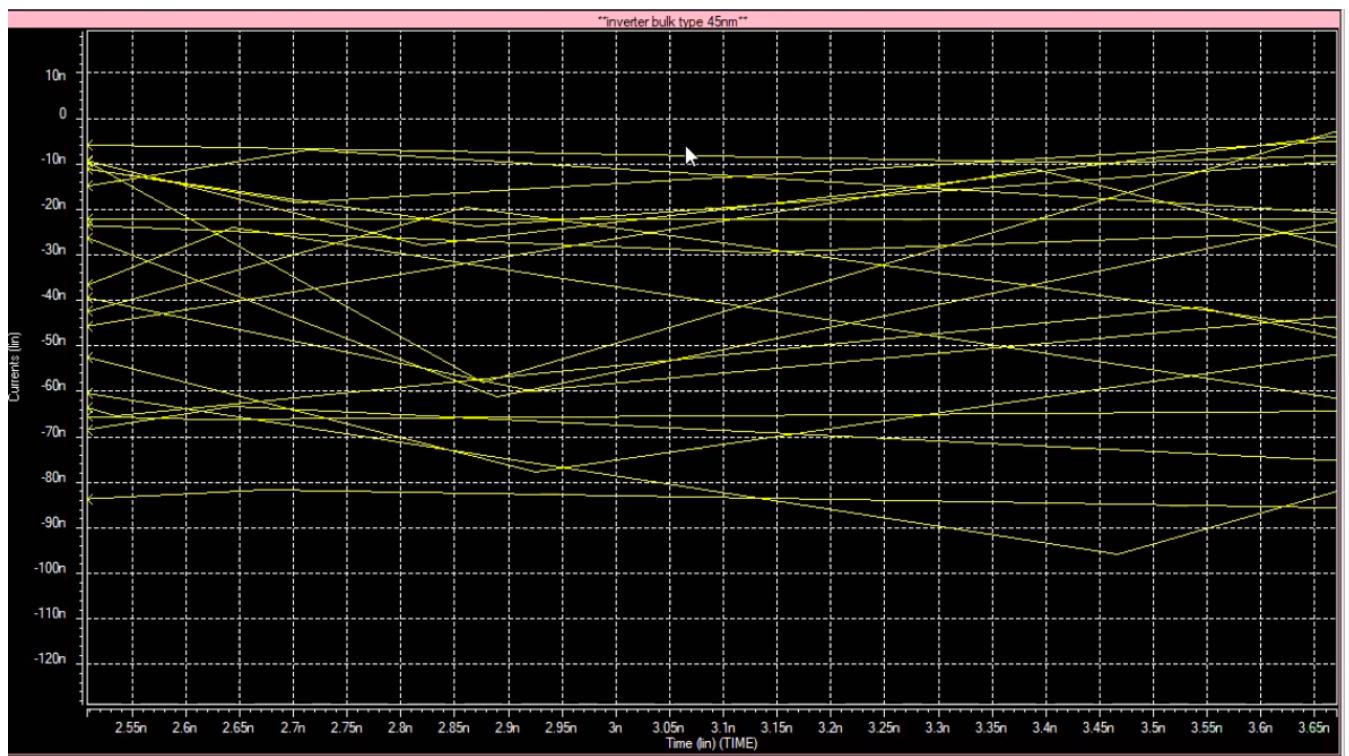
Logic values at different temp

Temperature	High logic	Low logic
-55 c	1.5 v	150 uV
25 c	1.4998 v	460 uV
125 c	1.4983 V	1460 uV

Graphs of (high/low) logic values at different temp.



5) Current analysis of inverter



Leakage current analysis

Temperature	leakage current
-55 °C	9.82 nA
25 °C	45 nA
125 °C	85 nA

Charging and discharging current (input time period is 4ns)

Temperature	Charging current	Discharging current
-55 °C	223 uA	146 uA
25 °C	187 uA	125 uA
125 °C	159 uA	119 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

Here in this model frequency response of inverter is not proper.

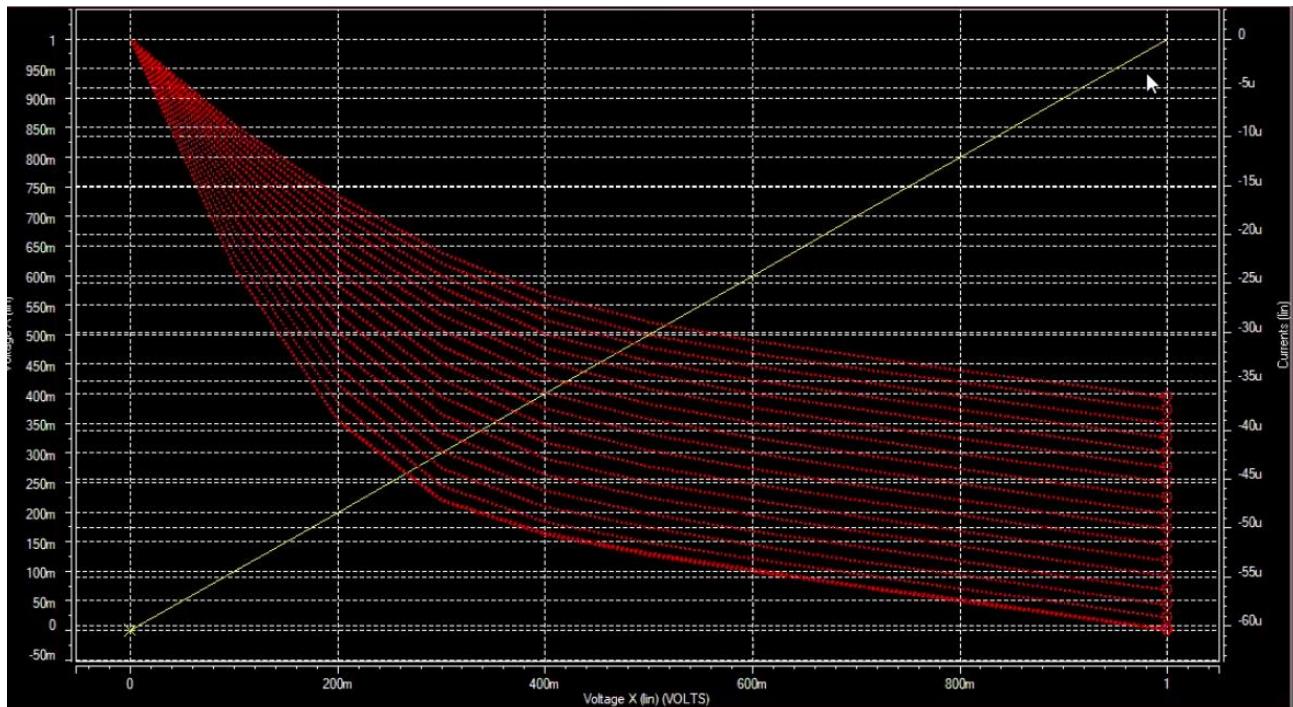
Ideally what should be that as frequency increase current should be increase but in this model we can't observe this result.

45 hp(high power) nm model analysis

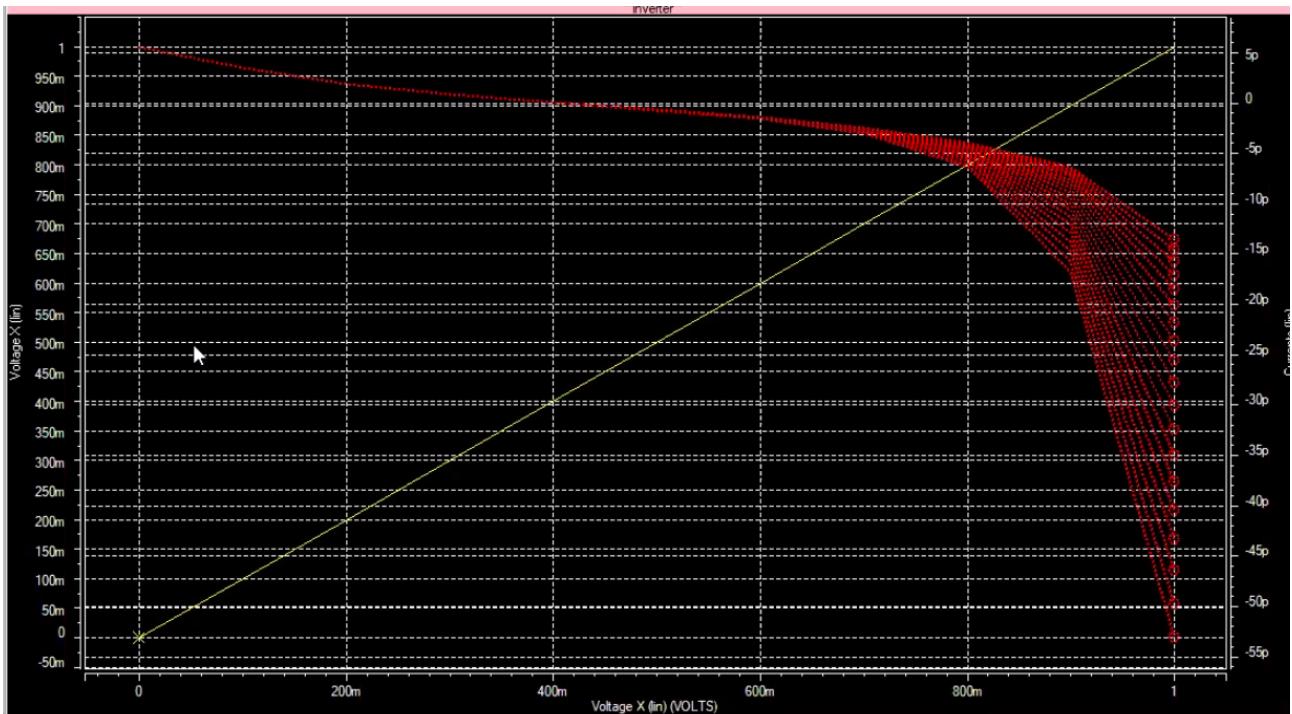
- High k
- Strained silicon
- $V_{th}(nmos) = 0.46893$, $V_{th}(pmos) = -0.49158$
- Biasing voltage=1 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=45nm, w=45nm
- pmos l=45nm, w=90nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

Nmos analysis

1) Vds vs Ids



this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.



2) Vgs vs Ids

this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

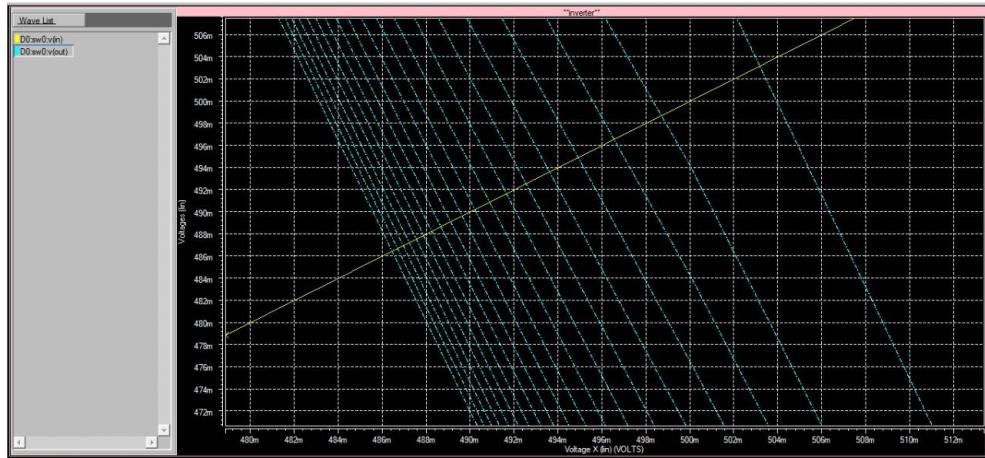


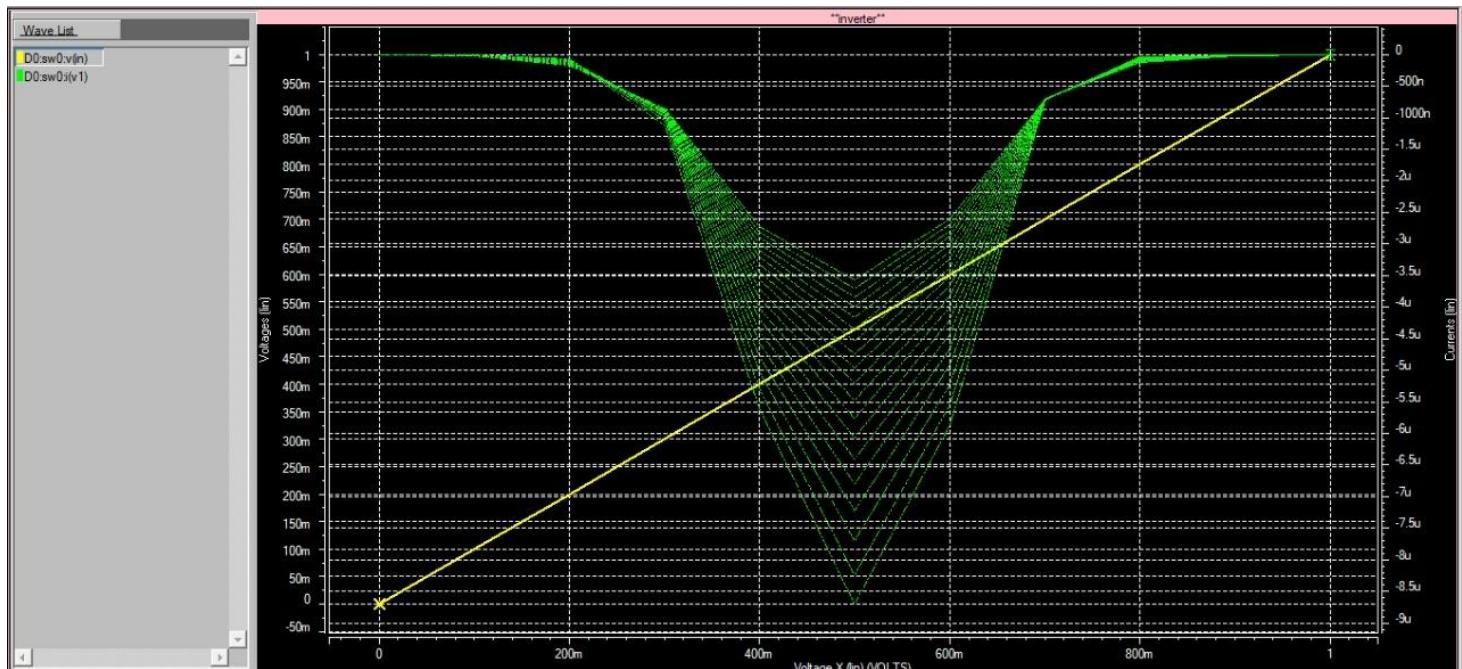
3) Voltage transfer characteristics

This graphs shows the variation in midpoint voltage because of temp.

At -55 C = 0.503 v

At 125 C =0.486 v





Midpoint current

This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

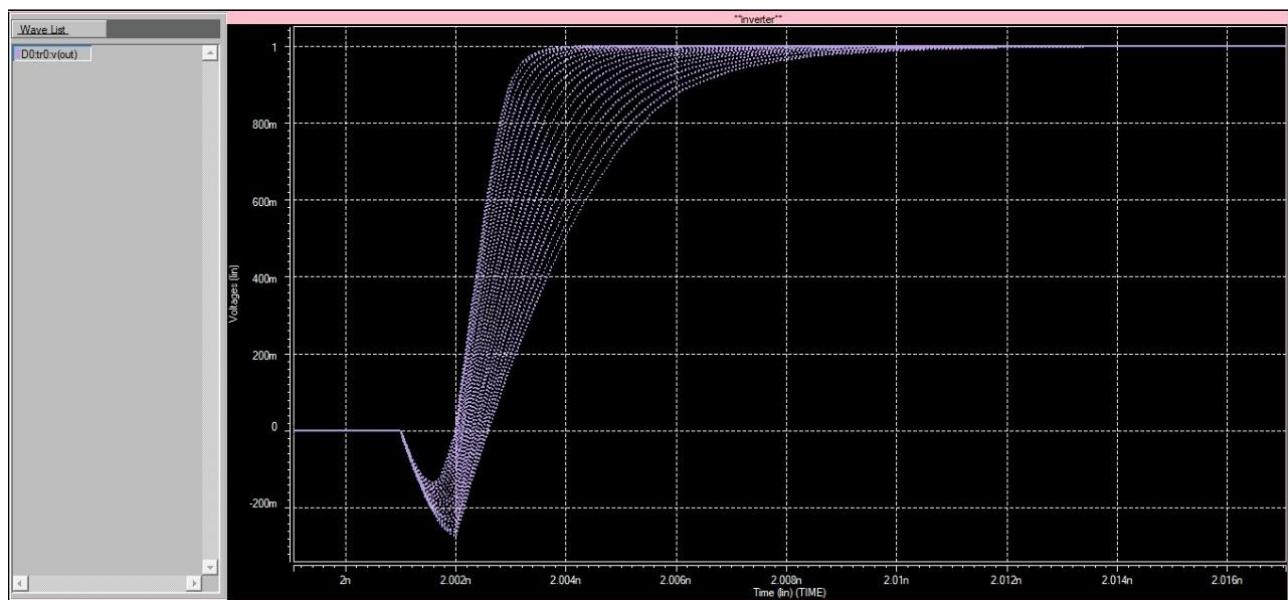
At -55 C = 8.7 uA

At 25 C = 5.47 uA

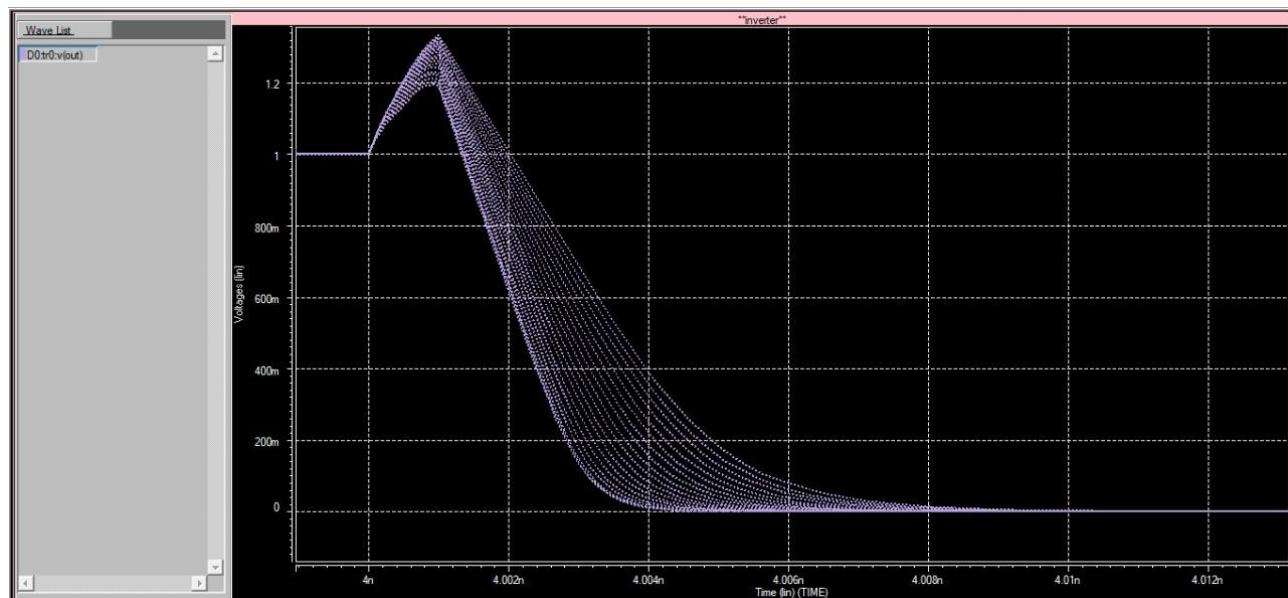
At 125 C = 3.57 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise tome at 125 C

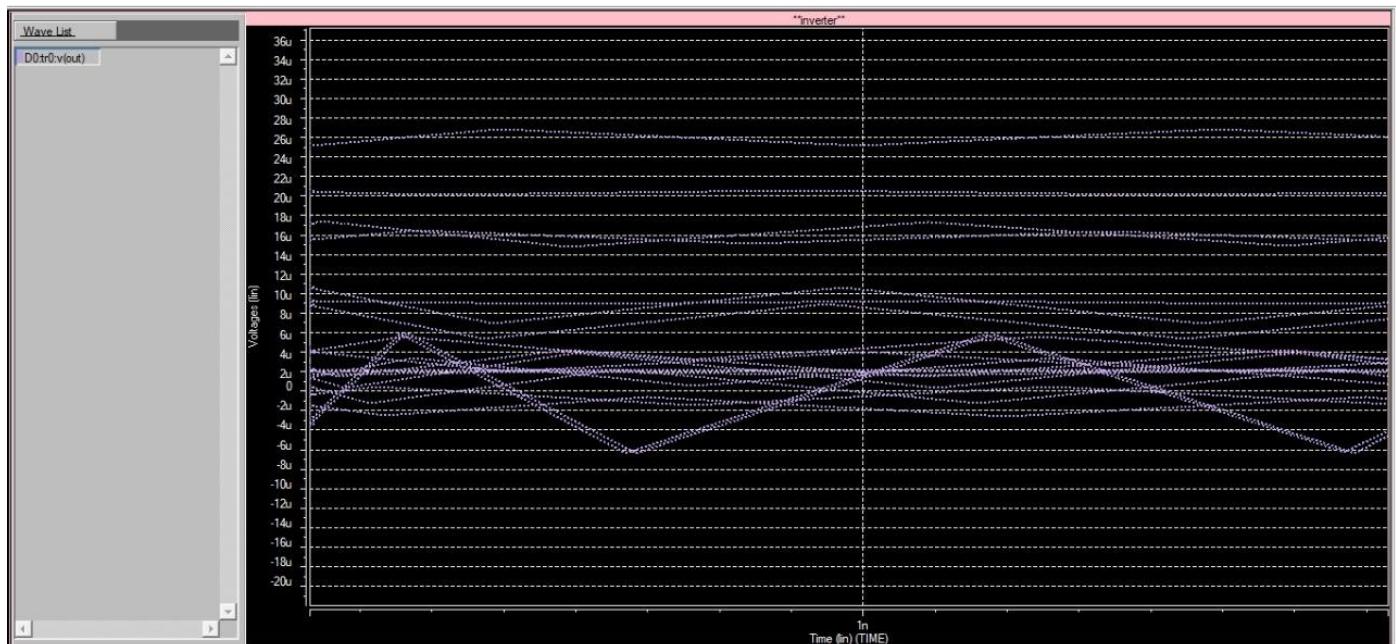
In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 °C	0.0035 ns	0.006 ns
25 °C	0.01 ns	0.01 ns
125 °C	0.016 ns	0.01 ns

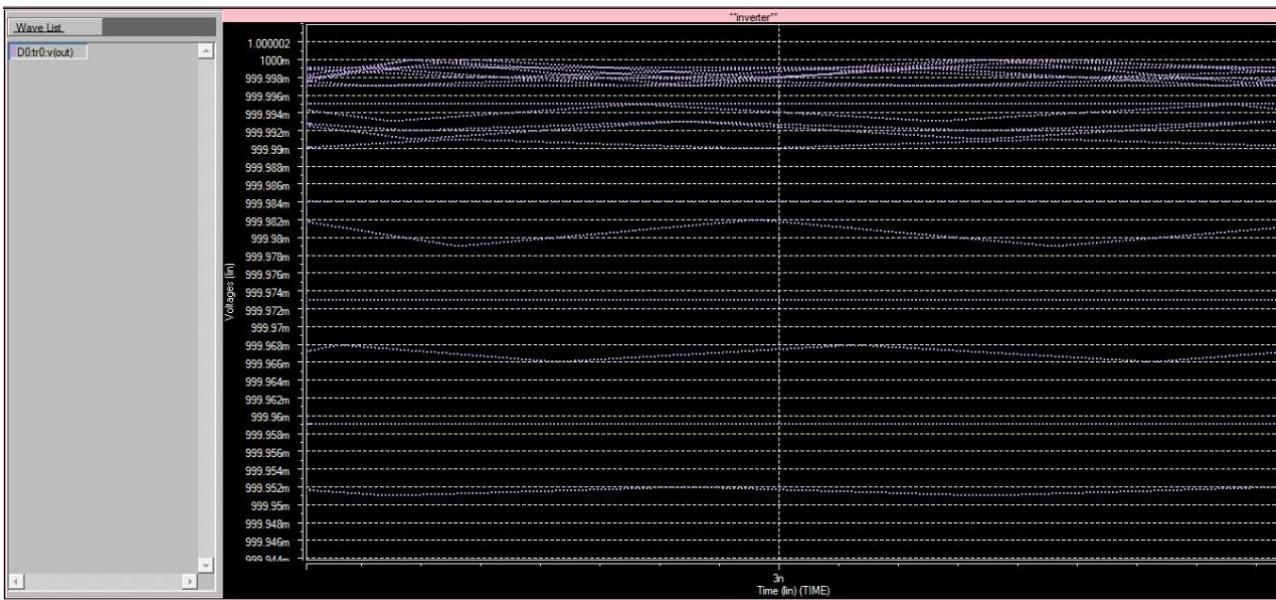
Logic values at different temp

Temperature	High logic	Low logic
-55 °C	1 V	1.17 uV
25 °C	1 V	1.18 uV
125 °C	1 V	26.9 uV

Noise margins ,at stable high voltage and low voltage



From this graph we can say that there is no continuous stable high and low logic levels



5) Current analysis of inverter

Temperature	leakage current
-55 c	9.73 nA
25 c	36.9 nA
125 c	71.1 nA

Charging and discharging current (input time period is 4ns)

Temperature	Charging current	Discharging current
-55 c	0.16 mA	0.1 mA
25 c	0.13 mA	88.5 uA
125 c	0.117 mA	84.3 uA

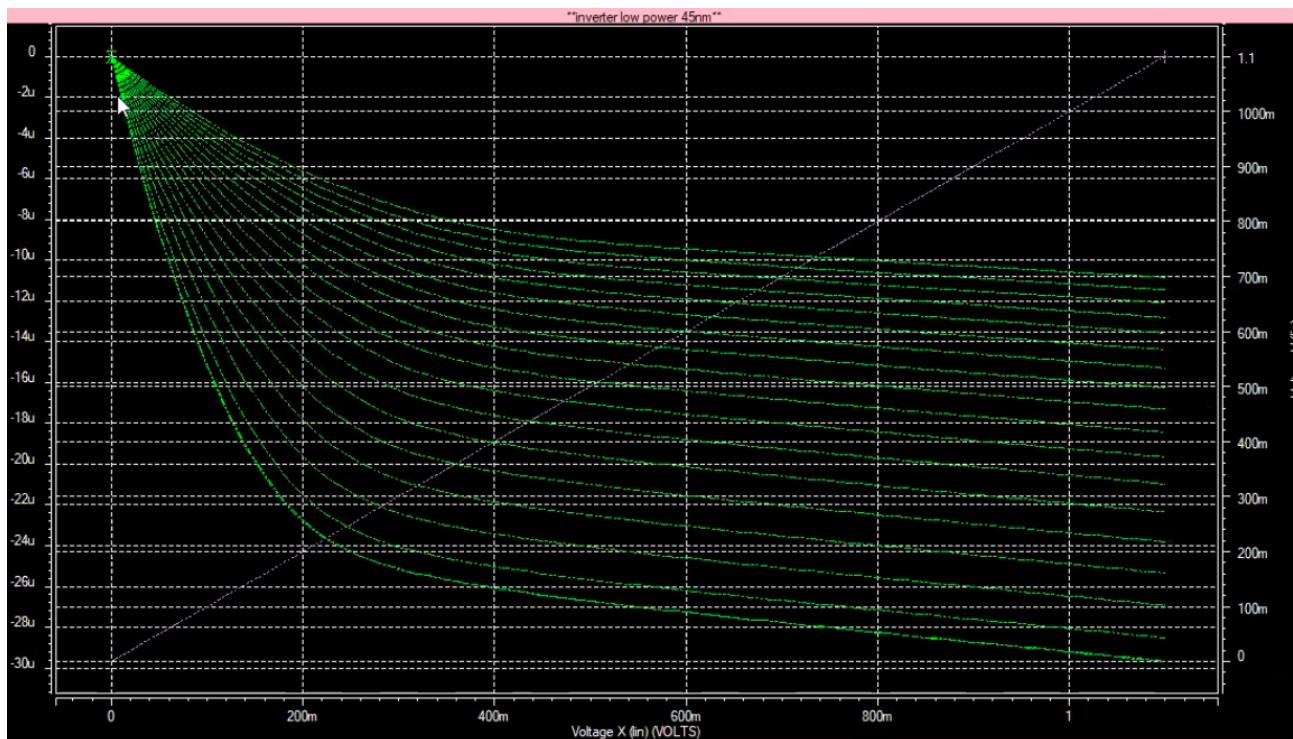
Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time then charging discharging current will increase drastically.

45 lp(low power) nm model analysis

- High k
- Strained silicon, metal gate
- $V_{th}(nmos) = 0.62261$, $V_{th}(pmos) = -0.587$
- Biasing voltage=1.1 v
- For inverter aspect ratio of nmos=1,pmos=2
- nmos l=45nm, w=45nm
- pmos l=45nm, w=90nm
- Here the graph is plotted at -55 to 125 centigrade temp .
In the gap of 10 centigrade.

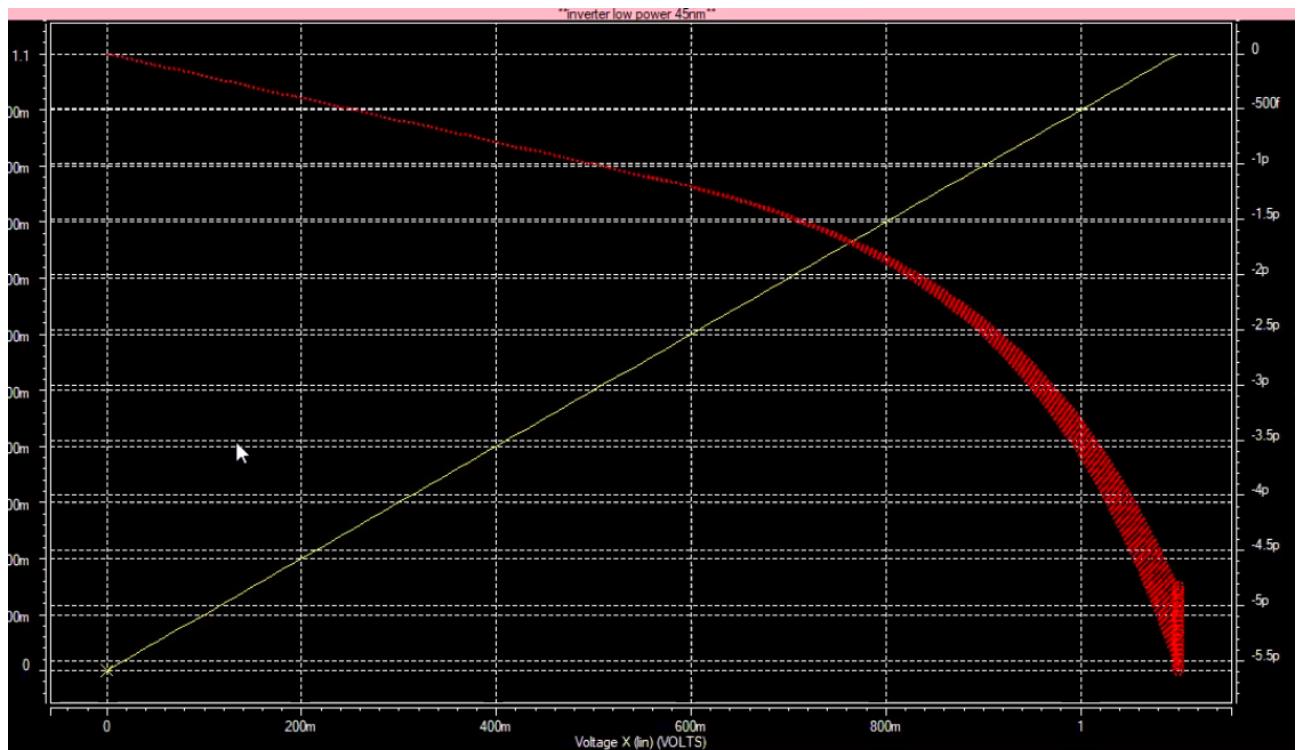
Nmos analysis

1) Vds vs Ids



this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

2) Vgs vs Ids



this arrow shows the graph at -55 centigrade. As temperature increase the current will decrease.

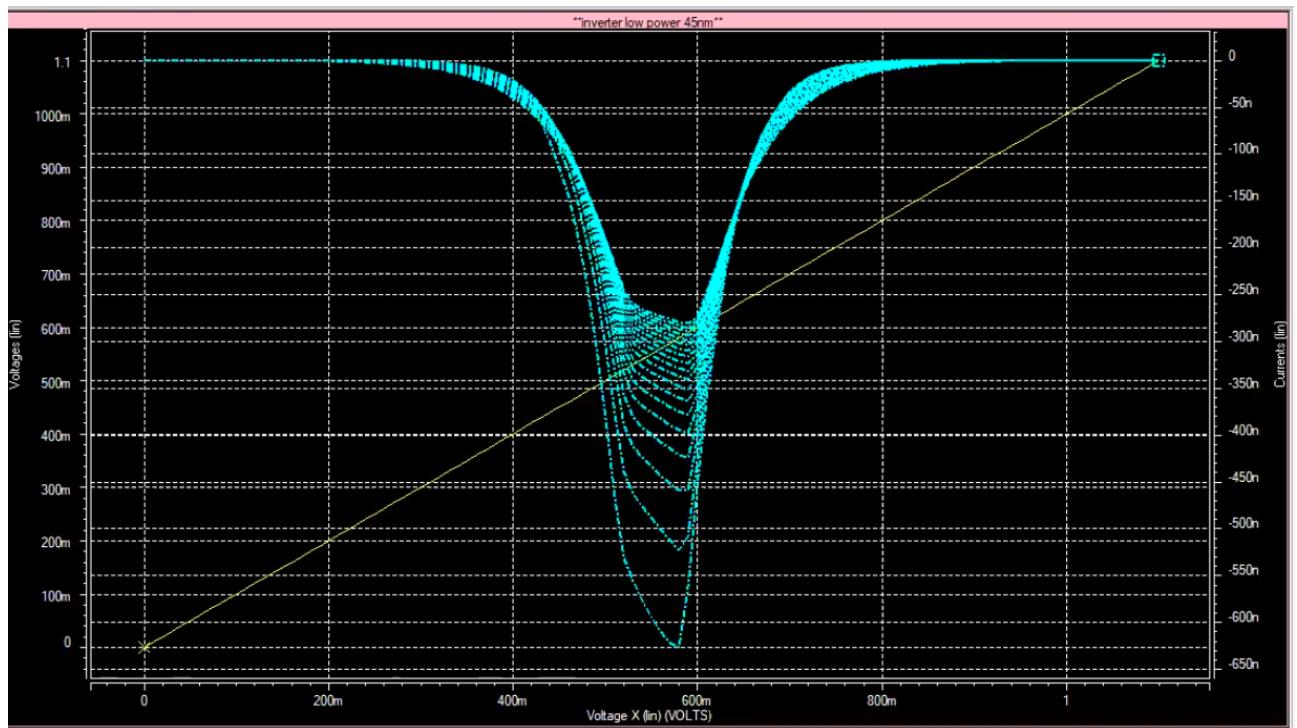
3) Voltage transfer characteristics



This graphs shows the variation in midpoint voltage because of temp.

At -55 C = 0.356 v

At 125 C = 0.348 v



Midpoint current

This arrow shows the graph at -55 temp.

Drain current of inverter(at mid point voltage)

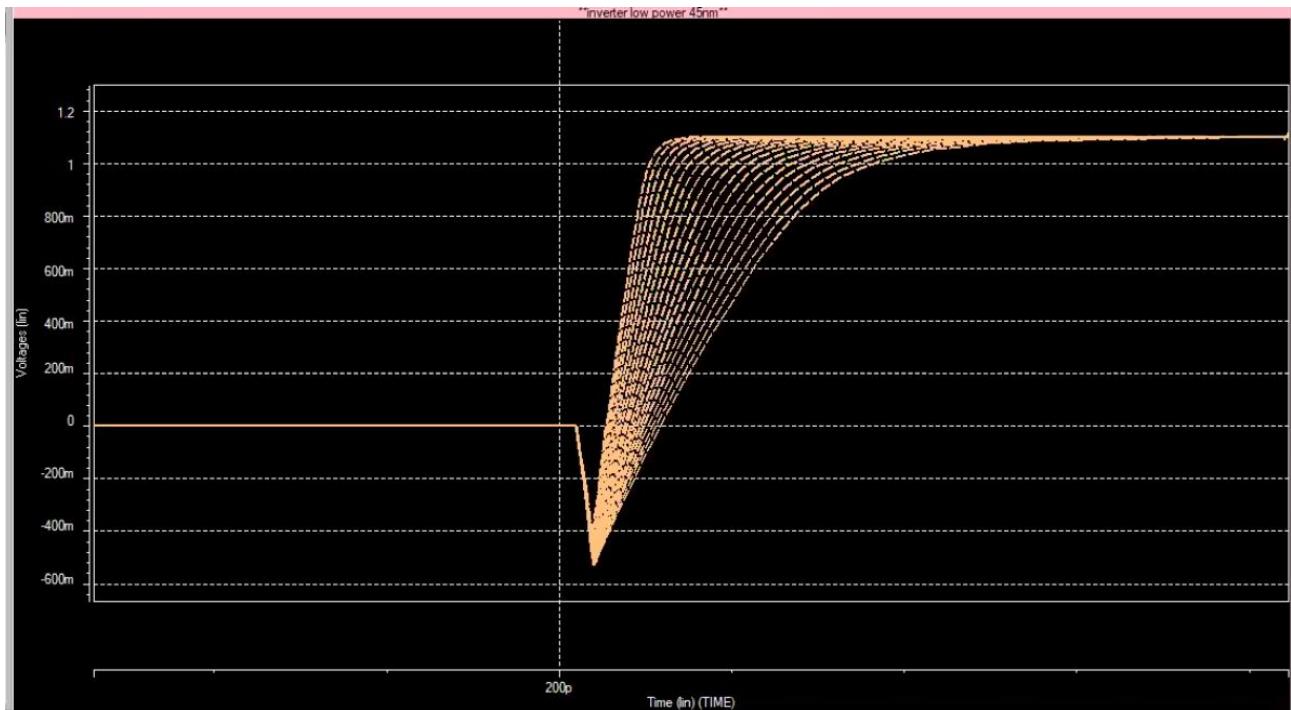
At -55 C = 0.62 uA

At 25 C = 0.34 uA

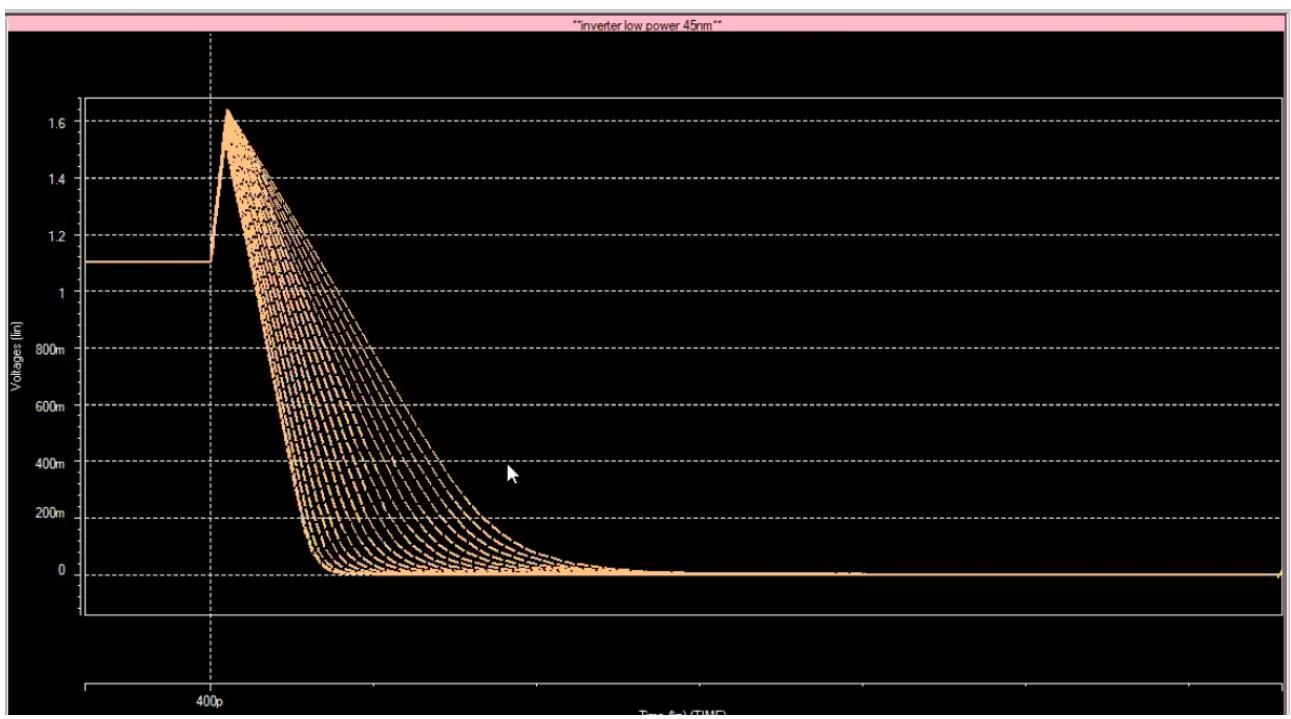
At 125 C = 0.28 uA

Here in this above graph you can say that there is very big effect of negative temp. On midpoint current.

Inverter analysis



4) Rise time and Fall time analysis



Rise time at different temperature. Arrow shows graph of rise tome at 125 C.

Fall time at different temperature. Arrow shows graph of rise time at 125 C

In the graph of rise time and fall time we can see that here the overshoot is increasing with temperature increasing.

Temperature	Rise time	Fall time
-55 c	7 ps	10 ps
25 c	14 ps	15 ps
125 c	32 ps	32 ps

Logic values at different temp

In this model there is steady voltages.Low logic voltage is in range of -5 to 5 uv.

5) Current analysis of inverter

Temperature	leakage current
-55 c	6 nA
25 c	0.5 nA
125 c	2.77 nA

Charging and discharging current (input time period is 4ns)

Temperature	Charging current	Discharging current
-55 c	38.1 uA	16.2 uA
25 c	27.5 uA	13.9 uA
125 c	20.4 uA	12.3 uA

Here we observe that as we increase the frequency the current will be increase. As input signal reaches near to the rise time and fall time than charging discharging current will increase drastically.