BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
WORK INTEGRATED LEARNING PROGRAMMES

COURSE HANDOUT

Part A: Content Design

Course Title	Computer Organization and Software Systems
Course No(s)	SS ZG516
Credit Units	5 (1 + 2 + 2) Unit split between Class Hours + Lab/Design/Fieldwork + Student preparation respectively; each unit translates to 32 hours
Course Author	Lucy J Gudino / Chandra Shekhar
Version No	2.0
Date	04/04/2020

Course Objectives

No	Course Objective
CO1	Introduce students to systems aspects (i.e. Computer Organization and Operating Systems) involved in software development
CO2	Equip the student to understand the computer architectural and operating systems related issues that affect the performance and nature of a software
CO3	To prepare students to be in a position to evaluate/correlate high level software performance based on its system level features (i.e. architectural and operating systems)

Text Book(s)

T1	Stallings William, ***Computer Organization & Architecture***, Pearson Education, 10th Ed. 2013
T2	A Silberschatz, Abraham and others, ***Operating Systems Concepts***, Wiley Student Edition, 9th Ed.

Reference Book(s) & other resources

R1	Patterson, David A & J L Hennenssy, ***Computer Organization and Design – The Hardware/Software Interface***, Elsevier, Revised 4th Ed.
R2	Randal E. Bryant, David R. O'Hallaron, ***Computer Systems – A Programmer's Perspective,*** Pearson, 2nd Ed, 2016.
R3	Tanenbaum, ***Modern Operating Systems,*** Pearson New International Edition, Pearson Education, 2013 (Pearson Online)
R4	Stallings, ***Operating Systems: Internals and Design Principles***, International Edition, Pearson Education, 2013 (Pearson Online)

Modular Content Structure

1. **Introduction to Computer Systems**
   - 1.1. Hardware Organization of a computer
   - 1.2. Running a Hello Program
   - 1.3. Instruction Cycle State Diagram
   - 1.4. Operating System role in Managing Hardware
     - 1.4.1. Processes
     - 1.4.2. Threads
     - 1.4.3. Virtual Memory
     - 1.4.4. Files
   - 1.5. Performance Assessment
     - 1.5.1. MIPS Rate
     - 1.5.2. Amdahl's Law

2. **Memory Organization**
   - 2.1. Storage Technologies
     - 2.1.1. Random Access Memory
     - 2.1.2. Disk Storage
     - 2.1.3. Solid State Disks
     - 2.1.4. Storage Technology Trends
   - 2.2. Locality
     - 2.2.1. Locality of Reference to Program Data
     - 2.2.2. Locality of instruction fetches
   - 2.3. Memory Hierarchy
   - 2.4. Cache Memories
     - 2.4.1. Generic Cache Memory Organization
     - 2.4.2. Direct-Mapped Caches
     - 2.4.3. Fully Associative Caches
     - 2.4.4. Set Associative Caches
     - 2.4.5. Issues with Writes
     - 2.4.6. Performance Impact of Cache Parameters
     - 2.4.7. Writing Cache friendly Codes

2.4.8. Replacement Algorithms

3. Instruction Set Architecture - CISC Vs RISC

3.1. CISC Instruction Set (Intel x86 as an example)
- 3.1.1. Machine Instruction Characteristics
- 3.1.2. Types of Operands
- 3.1.3. Types of Operations
- 3.1.4. Addressing Modes
- 3.1.5. Instruction Formats

3.2. RISC Instruction Architecture (MIPS as an Example)
- 3.2.1. Machine Instruction Characteristics
- 3.2.2. Types of Operands
- 3.2.3. Types of Operations
- 3.2.4. Addressing Modes
- 3.2.5. Instruction Formats
- 3.2.6. Single cycle implementation
- 3.2.7. Multicycle Implementation

3.3. Control Unit
- 3.3.1. Microprogrammed control unit
- 3.3.2. Hardwired Control Unit (MIPS as an example)

3.4. Pipeline
- 3.4.1. Overview of pipeline
- 3.4.2. Resource Hazard
- 3.4.3. Data Hazard : Forwarding versus Stalling
- 3.4.4. Control Hazard

4. Process Management

4.1. Concept of Process
4.2. Process State Diagram
4.3. Operations on Processes : Process creation and termination examples
4.4. Process vs. Threads
4.5. Multithreading Models
4.6. Process Scheduling criteria
4.7. Process Scheduling Algorithms -FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue

5. Process Coordination

5.1. The Critical section problem
5.2. Peterson's Solution
5.3. Synchronization Hardware
5.4. Semaphores
5.5. Deadlock:
- 5.5.1. System Model
- 5.5.2. Deadlock Characterization

5.6. Methods of Handling Deadlocks
- 5.5.2.1. Deadlock Prevention
- 5.5.2.2. Deadlock Avoidance: Banker's Algorithm
- 5.5.2.3. Deadlock Detection
- 5.5.2.4. Recovery from Deadlock

6. Memory Management

6.1. Memory-Management Strategies
6.2. Swapping
6.3. Partitioning
6.4. Paging
6.5. Segmentation
6.6. Virtual-Memory
6.7. Demand Paging
6.8. Page Replacement Algorithms: FIFO, Optimal, LRU, and LFU

7. **Optimizing Program Performance**
   - 7.1. Capabilities and Limitations of Optimizing Compilers
   - 7.2. Expressing Program Performance
   - 7.3. Eliminating Loop Inefficiencies
   - 7.4. Reducing Procedure Calls
   - 7.5. Eliminating Unneeded Memory References
   - 7.6. Understanding Modern Processors
   - 7.7. Loop Unrolling
   - 7.8. Enhancing Parallelism

Learning Outcomes:

No	Learning Outcomes
LO1	To **apply** the knowledge of performance metrics to find the performance of systems.
LO2	To **Investigate** high performance architecture design
LO3	To **Examine** different computer architectures and hardware
LO4	Students will **Analyze and Compare** of process management concepts including scheduling, synchronization ,deadlocks
LO5	Students will **Examine** multithreading and system resources sharing among the users
LO6	Students will **Outline** of file system interface and implementation

Part B: Contact Session Plan

Academic Term	SEM II, 2019-20
Course Title	Computer Organization and Software Systems
Course No	SS *ZG516
Lead Instructor	Dr. Lucy J Gudino
Instructors	Prof. Chandrashekar R K, Prof. Pruthvi Kumar, Prof. Sarma, Prof. Balamurali Shankar.

Course Contents

Sl. No.	Contact Hour #	List of Topic Title (from content structure in Part A)	Topic # (from content structure in Part A)	Text/Ref Book/external resource
1	1-2	**Introduction to Computer Systems** • Hardware Organization of a computer (T1: 3.1) • Running a Hello Program (R2: 1.2,	1.1-1.4	T1, T2, R2

		1.4-1.6)
		• Instruction Cycle State Diagram (T1: 3.2)
		• Operating System role in Managing Hardware (T2: 1.1, 1.4, 1.5, R2: 1.7)
		  ○ Processes
		  ○ Threads
		  ○ Virtual Memory
		  ○ Files		

2	3-4	**Introduction to Computer Systems (Contd.)**
		• Performance Assessment (R1: 1.4, T1: 2.3)
		  ○ MIPS Rate
		  ○ Amdahl's Law
		Memory Organization
		• Storage Technologies (T1: 5.1, R2: 6.1)
		  ○ Random Access Memory
		  ○ Disk Storage
		  ○ Solid State Disks
		  ○ Storage Technology Trends
			1.5, 2.1	Class Notes, T1 , R1, R2

3	5-6	**Memory Organization (Contd..)**
		• Locality (Class Notes)
		  ○ Locality of Reference to Program Data
		  ○ Locality of instruction fetches
		• Memory Hierarchy (T1: 4.1)
		• Cache Memories (T1: 4.2-4.3)
		  ○ Generic Cache Memory Organization
		  ○ Direct-Mapped Caches
		  ○ Fully Associative Caches
			2.2 – 2.3, 2.4 (2.4.1-2.4.3)	T1

4	7-8	**Memory Organization (Contd..)**
		• Cache Memories (Contd..)
		  ○ Set Associative Caches (T1: 4.3)
		  ○ Issues with Writes (T1: 4.3)
		  ○ Performance Impact of Cache Parameters (T1: 4.3)
		  ○ Writing Cache friendly Codes (R2: 6.5)
		  ○ Replacement Algorithms (Class Notes)
			2.4 (2.4.4-2.4.8)	T1, R2

5	9-10	**Instruction Set Architecture - CISC Vs RISC** • CISC Instruction Set (Intel x86 as an example) (T1: 12.1 – 12.5, 13.1 – 13.4)	3.1	T1

		○ Machine Instruction Characteristics ○ Types of Operands ○ Types of Operations ○ Addressing Modes ○ Instruction Formats		
6	11-12	**Instruction Set Architecture - CISC Vs RISC (Contd…)** • RISC Instruction Architecture (MIPS as an Example) (R1: Selected topics from Chapter 2 and Chapter 4, and Class Notes) ○ Machine Instruction Characteristics ○ Types of Operands ○ Types of Operations ○ Addressing Modes ○ Instruction Formats ○ Single cycle implementation	3.2(3.2.1-3.2.6)	R1
7	13-14	• **Instruction Set Architecture - CISC Vs RISC (Contd…)** (Selected topics from T1, R1: Chapter 4 and Class Notes) • RISC Instruction Architecture (MIPS as an Example) (Contd..) ○ Multicycle Implementation • Control Unit ○ Microprogrammed control unit ○ Hardwired Control Unit (MIPS as an example)	3.2.7, 3.3	T1, R1
8	15-16	**Instruction Set Architecture - CISC Vs RISC (Contd…)** • Pipeline (T1: 14.4) ○ Overview of pipeline ○ Resource Hazard ○ Data Hazard : Forwarding versus Stalling ○ Control Hazard	3.4	T1
MID SEM EXAMINATION				
9	17-18	**Process Management** (T2: 3.1-3.3 and 4.1-4.3) • Concept of Process • Process State Diagram • Operations on Processes : Process creation and termination examples • Process vs. Threads • Multithreading Models	4 .1-4.6	T2
10	19-20	**Process Management (Contd…)** (T2: 6.1-	4.7	T2

		6.3) • Process Scheduling criteria • Process Scheduling Algorithms - FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue		

11	21-22	**Process Coordination** (T2: 5.1-5.6, 7.1, 7.2)
		• The Critical section problem
		• Peterson's Solution
		• Synchronization Hardware
		• Semaphores
		• Deadlock:
		  ○ System Model
		  ○ Deadlock Characterization
			5.1-5.5	T2

12	23-24	**Process Coordination (Contd…)**
		• Methods of Handling Deadlocks (T2: 7.3-7.7)
		  ○ Deadlock Prevention
		  ○ Deadlock Avoidance: Banker's Algorithm
		  ○ Deadlock Detection
		  ○ Recovery from Deadlock
			5.6	T2

13	25-26	**Memory Management** (T2: 8.1-8.6) • Memory-Management Strategies • Swapping • Partitioning • Paging • Segmentation	6.1-6.4	T2
14	27-28	**Memory Management (Contd…)** (T2: 9.1-9.4) • Virtual-Memory • Demand Paging • Page Replacement Algorithms: FIFO, Optimal, LRU and LFU	6.5-6.8	T2
15	29-30	**Optimizing Program Performance (R2: 5.1:5.5)** • Capabilities and Limitations of Optimizing Compilers • Expressing Program Performance • Eliminating Loop Inefficiencies • Reducing Procedure Calls	7.1-7.4	R2
16	31-32	**Optimizing Program Performance** (R2: 5.6:5.9) • Eliminating Unneeded Memory References • Understanding Modern Processors • Loop Unrolling • Enhancing Parallelism	7.5-7.8	R2

Comprehensive Examination

Evaluation Scheme

Evaluation Component	**Name** (Quiz, Lab, Project, Midterm exam, End semester exam, etc)	**Type** (Open book, Closed book, Online, etc.)	**Weight**	**Duration**	**Day, Date, Session, Time**
EC – 1	Quizzes / Assignment	Online	5+25%	NA	To be announced
EC – 2	Mid-term Exam	Closed book	30%	-	To be announced
EC – 3	End Semester Exam	Open book	40%	-	To be announced

Note *- Evaluation components can be tailored depending on the proposed model.*

Important Information

Syllabus for Mid-Semester Test (Closed Book): Topics in Weeks 1-8 (1-18 Hours)
Syllabus for Comprehensive Exam (Open Book): All topics given in plan of study

Evaluation Guidelines:

1. EC-1 consists of either two Assignments or three Quizzes. Announcements regarding the same will be made in a timely manner.
2. For Closed Book tests: No books or reference material of any kind will be permitted. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
3. For Open Book exams: Use of prescribed and reference text books, in original (not photocopies) is permitted. Class notes/slides as reference material in filed or bound form is permitted. However, loose sheets of paper will not be allowed. Use of calculators is permitted in all exams. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
4. If a student is unable to appear for the Regular Test/Exam due to genuine exigencies, the student should follow the procedure to apply for the Make-Up Test/Exam. The genuineness of the reason for absence in the Regular Exam shall be assessed prior to giving permission to appear for the Make-up Exam. Make-Up Test/Exam will be conducted only at selected exam centres on the dates to be announced later.

It shall be the responsibility of the individual student to be regular in maintaining the self-study schedule as given in the course handout, attend the lectures, and take all the prescribed evaluation components such as Assignment/Quiz, Mid-Semester Test and Comprehensive Exam according to the evaluation scheme provided in the handout.