HomeWork Question on Session_03

Q-1) Consider a direct mapped cache with four cache lines. Suppose that the reference pattern of a program is such that it accesses the following sequence of blocks: 0, 4, 8, 0, 4, 4, 8, 2, 1. Compute the following :

i. To which cache line, block 5 maps to?
ii. What is the Hit ratio?

Q-2) Consider a byte-addressable machine with a main memory of 4 Mbytes and a direct mapped cache of 1024 lines. The main memory block size is 32 bytes. Answer the following questions by specifying clearly the formulae used:

i. What is the number of bits needed for representing main memory address?
ii. What is the size of each cache line?
iii. Specify the number of bits needed for tag, line and word offset.
iv. To which cache line, the main memory address 0x33A9FF is mapped to?

Q-3) Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is a 16-bit memory address divided into tag, line number, and byte number?
b. Into what line would bytes with each of the following addresses be stored?
   0001 0001 0001 1011, 1100 0011 0011 0100, **1010 1010 1010 1010**
c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
d. How many total bytes of memory can be stored in the cache?

Q-4) Assume that a read request takes 50 nsec on a cache miss and 5 nsec on a cache hit. While running a program, it is observed that 80% of the processor's read requests result in a cache hit. What is the average read access time ?

Q-5) A byte addressable computer has a cache of 128 KB, line size of 256 bytes. Main memory address is of 32 bit. Calculate the number of bits required for tag, line and word offset in the memory address if direct mapping is used.